Lab Report 1

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1 Profiles and Layout

1.1 Section A

Hand drawings will be included at the end.

1.2 Section B

Hand drawings will be included at the end.

2 Process Procedures

2.1 Section A

Describe the monitoring measurements that were done during processing. That is, how it was measured, why a particular technique was used, and what information it provided in regards to that process step.

Film Color

How - Film color was determined through observation from an optical microscope.
Why - Measured to determine and verify which thin film layer was present, whether it was PR, oxide, poly, or aluminum.
Information Provided - For all process steps, the film color helped determine whether our etch time was sufficient to etch the current film. During oxide growth, film color helped to determine thickness of the oxide.

Line Width

How - Measured using images from an optical microscope at a 50x magnification and ImageJ.
Why - This was the simplest way; there's no real ruler you can put unto your wafer to measure linewidths. Imagej was used as the software that the microscope used didn't allow for any measurements to be taken immediately.
Information Provided - Allowed us to see the degree of etching in our process, and whether we had overetched, underetched, or etched our film layer for just the right amount of time.

Thickness

How - Film thicknesses were measured using the Nanospec machine in the lab.
Why - There are two reasons as to why we measure thicknesses via Nanospec. 1) Color alone can be difficult to determine what exactly the film is underneath. The measurements from Nanospec can help confirm what film is being measured. 2) Exact thicknesses can help us determine how long our etch should be and how deep ion implantations need to be.
Information Provided - The exact thicknesses provided allow us to determine possible non-idealities within our process (whether our machines were performing as we expected).

Resistivity

How - A four point probe measured the sheet resistance of a test wafer that underwent the same procedures our process wafers went through.
Why - We used a test wafer as it was the least destructive way. Also, the layer we might have been testing for might not have been easily measured on our wafer, as it might have just been a tiny portion of the wafer; there is no real way to guarantee that it was being measured.
Information Provided - Sheet resistance of a wafer allows us to measure the dopant concentration at the surface of the wafer.

2.2 Section B

Field Oxide

Overetched 15% down to the wafer to ensure exposure of wafer for gate oxide growth.

Gate Oxide

Overetched 20% compared to the control wafer; the overetch is performed for the process latitude, i.e. oxide thickness and the etch rate both may vary across a wafer and among wafers.

Polysilicon

Overetched 15% compared to control wafer, color should be completely changed to black to ensure that it is etched down to the gate and none remains on the field oxide.

Contact

Overetched 100% compared to the thick control wafer, to make sure the intermediate oxide across the source and drain is completely etched away to make a good contact hole.

Metal

Overetched to prevent a short circuit, as we can't see the two micron line.

2.3 Section C

To measure this, find where one of the lines on the left vernier is exactly in the middle of two of the right lines. The misalignment is read as the number of lines from the long line on the left structure times the offset, 0.2 μm in this case.
If the vernier is drawn correctly, the ends wrap around. This helps when the misalignment is very large. If there is a large misalignment, greater than the line width, you will notice that the fingers which align are in the opposite direction of which you would expect. So, if the right vernier were shifted up by more than a line, but less than a line and a space, the fingers which match would be below the reference instead of above. If the alignment is greater than the width of one line and one space, you will need to add the extra distance of the line and space, or multiple line and space pairs depending on the degree of misalignment.

In the following figure, the first black line that fits perfectly between two grey lines is shown. We then see that it is the 3rd step from the long black line. So, the misalignment is 0.2 μm x 3 = 0.6 μm.

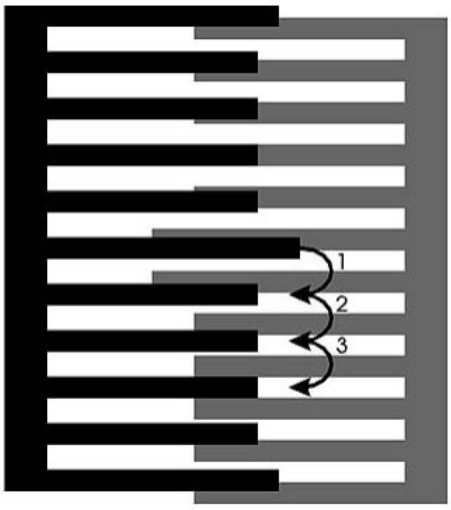


Figure 1: Misaligned Vernier Marks

2.4 Section D

ACTV

No intentional misalignment or misalignment here, as this is the first step on a virgin wafer, hence no Vernier marks.

Polysilicon

Intentional misalignment on the wafer to ensure complete coverage of polysilicon on the gate. If we dont make the polysilicon go beyond the ideal alignment, there is a chance that the device will be shorted (both wells).

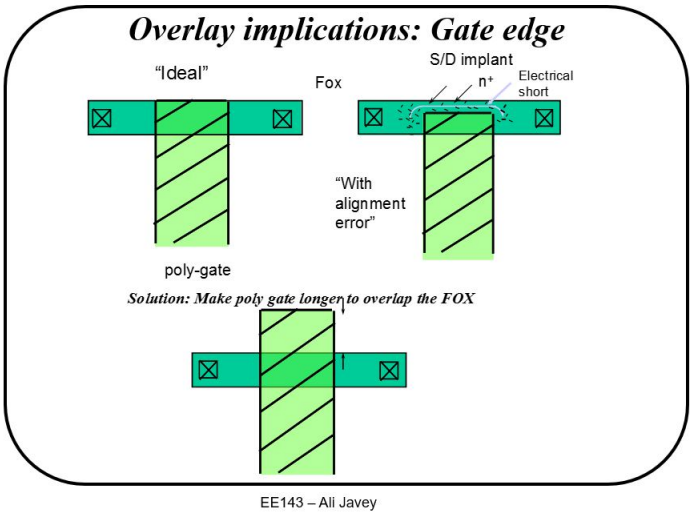


Figure 2: Visual representation of how the short will occur on polysilicon

Misalignment can be around 2 μm (downwards as in the figure), otherwise the device will short because of the absence of an insulator.

Contact

The contacts here were meant to be misaligned with the previous mask, because the previous mask was meant to be misaligned. This was meant to counteract the polysilicon's misalignment.

Misalignment for this layer can be around 10 μm, as we only need one contact for our device to work. However, the resistance on our device will be much greater the fewer contacts there are.

Metal

The metal mask was not intentionally misaligned. Misalignment will cause the devices to be connected to each other and short, especially if we etch it to the right time. To try to make up for misalignment, we overetch the metal. It can tolerate a misalignment of up to 2 μm.

3 Process Deviations

3.1 Section A

Table 1: Film Thicknesses Targeted and Measured

Layer	Target Thickness (Å)	Measured Thickness (Å)
Field Oxide	4500-5000	4779
Polysilicon	4000	7248
Gate Oxide	700 - 1000	706
Interm. Oxide	1000	678
Aluminum	8000	10500

Measured Thickness vs Target Thickness

Field Oxide - Did not deviate from our target thickness at all.
Polysilicon - Compared to 4300 Å- 4800 Åfor 3 hours 30 minutes, 5000 Å 5800 Åfor 4 hours, in Tystar10 (Fall 13), the GSI grew it for 720 minutes at 120 C which is longer than normal. Hence our polysilicon is thicker.
Gate Oxide - Measured thickness fell into our target thickness.
Intermediate Oxide - Batch processing could have affected the gas flow within the furnace, and the temperature difference during the slow loading, as well as during the process, with the gas flowing, could have attributed to different growth rates.
Aluminum - A layer of aluminum oxide is formed quickly, temperature and composition of etchant could be off as compared to ideal =¿ change in etch rate (which we used to calculate Aluminum thickness). Also, we overetched and that increases the etch time and consequently the apparent thickness of Aluminum film. From the resistivity data, the thickness calculated is way off because we may have a layer of Al_2O_3 in the film which increases the resistivity.

Discrepancies and their Effects

Field Oxide - Just acts as a separation between two transistors. No problem if it is too thick. But if it is to thin, it will be connect all devices through the silicon wafer.
Polysilicon - Thinner polysilicon as an electrode will lead to a higher gate leakage current and it will affect the performance of the transistor. We have to dope more to thicker polysilicon at higher temperature to maintain a high doping level in poly-Si to make the working voltage low.
Gate Oxide - A thin gate oxide will make it easier for current to leak into the silicon wafer and dopant to penetrate while too thick gate oxide will increase the input power which costs too much energy.
Intermediate Oxide - If it is too thin, it will also be broke when the voltage is high. If it is thick, it will still play the role of protecting the polysilicon electrode and separating the aluminum and polysilicon.
Aluminum - Thick aluminum may result in short circuiting while too thin will make it hard to find the metal electrode when measuring or even cannot connect to the probe we use.

3.2 Section B

Table 2: Targeted and Measured PR Linewidths

Layer	Target PR Linewidth ()μm)	Measured PR Linewidth ()μm)
Field Oxide (ACTV)	2, 3, 4, 8	3.14, 3.53, 5.01, 7.998
Polysilicon (POLY)	2, 3, 4, 8	2.04, 3.00, 4.07, 7.43
Interm. Oxide (CONT)	2, 3, 4, 8	2.14, 3.43, 4.14, 7.52
Aluminum (METL)	2, 3, 4, 8	N/A

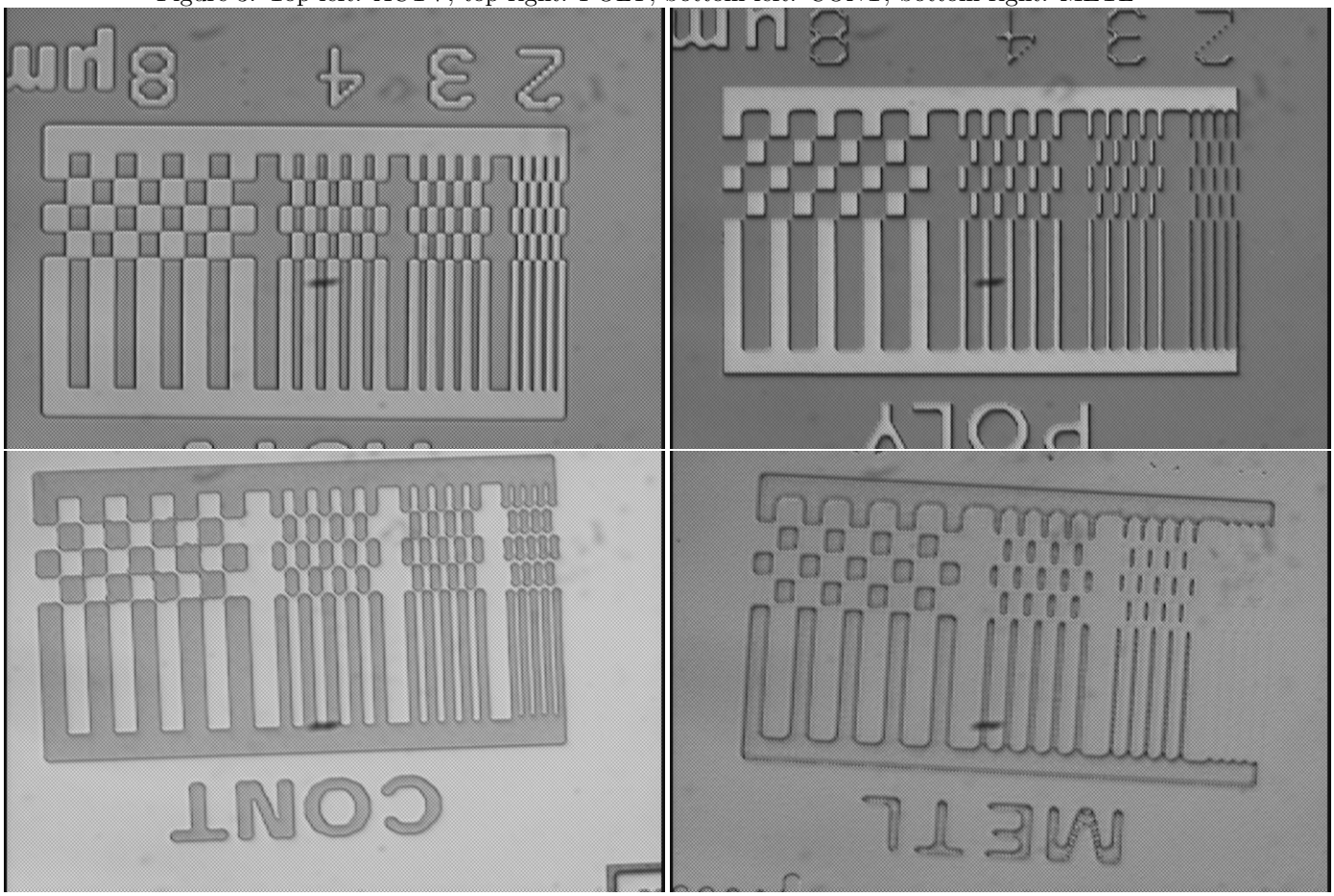
In contact lithography, the resolution gets worse and worse as your process continues. The mask gets degraded after use and may cause increase in feature size. The lamp was old initially, and hence there may be under-exposure; additionally, the lamp was changed for the aluminum step, which could have led to an over-exposure. The incident light is not completely coherent. Also, the non-uniformity of the photoresist will cause a little difference between the target and the result we measured.

Table 3: Etched Layer Linewidths

Layer	Measured PR Linewidth (μm)	Measured Layer Linewidth (μm)	% Overetch
Field Oxide (ACTV)	3.14, 3.53, 5.01, 7.998	2.86, 3.76, 4.95, 8.57	8.9, -6.51, 1.19, -7.15
Polysilicon (POLY)	2.04, 3.00, 4.07, 7.43	0.54, 1.14, 2.72, 6.002	73.52, 62, 33.17, 19.22
Interm. Oxide (CONT)	2.14, 3.43, 4.14, 7.52	2.626, 3.179, 3.823, 7.629	-22.71, 7.32, 7.66, -1.44
Aluminum (METL)	N/A	0, 0.957, 2.104, 5.873	100, 21.56, 21.2, 2.6

ACTV - This layer needs to be overetched for process latitude. It is okay to overetch because the etch mask is silicon itself which is unaffected by HF. But if it is underetched, a layer of field oxide will remain on the substrate and gate oxide thickness will be compromised.(Etch time was 7 mins 30s, greater than 4 mins 40s, to make sure the field oxide is fully etched).
POLY - Should be overetched to properly expose the source and drain regions because the phosphorus has to diffuse

Figure 3: Top left: ACTV, top right: POLY, bottom left: CONT, bottom right: METL



into the substrate in the subsequent step. Oxide layer will act as a diffusion barrier and the device will not work.(Etch time was 15 mins which is greater than expected because the thickness of the polysilicon is thicker than expected.)
CONT - It should be overetched to make sure the circuit can be completed as intermediate oxide is an insulator. If it is underetched, the aluminum will not be able to contact the source/drain region.(Our etch time of 2 mins is greater than the expected 55 seconds in order to make sure it is fully etched down to contact the source/drain region.)
METL - Better to use a bit longer (but not too much longer!) develop time as the undeveloped PR residue on Al is hard to see and might create short circuits (if underetched) and ruin the whole process after Al etch. If overetched too much, the wire will disappear. (Our etch time was 105 seconds. The expected time depend on the temperature and the concentration and the etchant. Theoretically, it should be etched until the bubbling subsides, as we don't have complete control over the actual thickness deposited.)

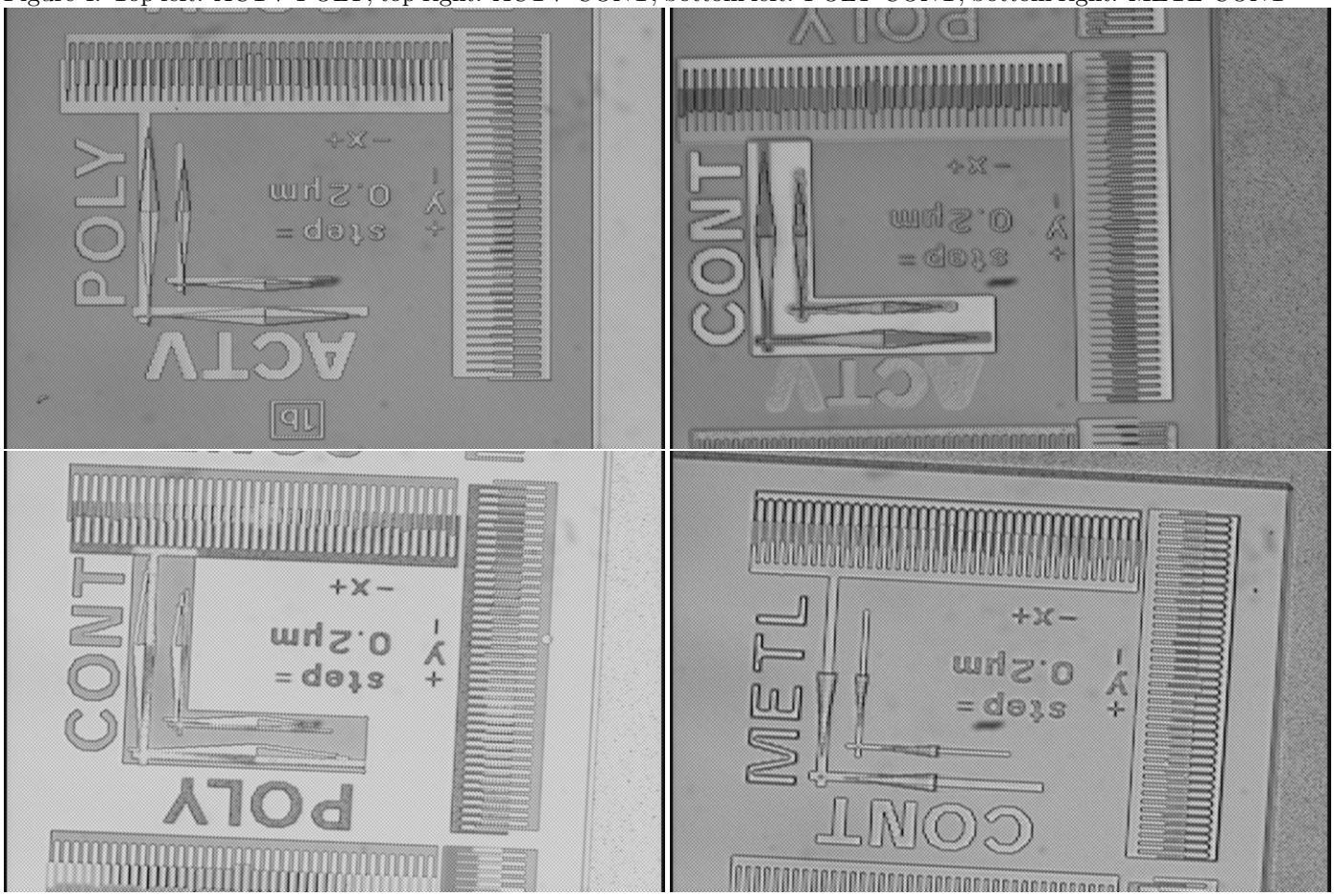
3.3 Section C

Table 4: X and Y Misalignment

Layer	X Misalignment (μm)	Y Misalignment (μm)
ACTV-POLY	-0.4	0.2
ACTV-CONT	0	0
POLY-CONT	-0.2	0.4
CONT-METL	-0.2	-0.4

The misalignment will be not be problematic for some of the components. For example, POLY-CONT will not be a problem because the position of the contact doesnt matter as much as the depth of the contact hole. But it will be an issue for source/drain regions (contact - metal) because it can cause electrical short.

Figure 4: Top left: ACTV-POLY, top right: ACTV-CONT, bottom left: POLY-CONT, bottom right: METL-CONT



Misalignment Tolerances

ACTV-POLY - 2 μm (hence intentional misalignment)
ACTV-CONT - 8 μm
POLY-CONT - 8 μm (assuming we require all the contact holes)
METL-CONT - 5 μm

3.4 Section D

Field Oxidation

Non-idealities - Temperature gradients were the largest source of error, as well as having enough water vapor to . We avoided this largely by using the nanolab furnace, which has three different temperature zones that are calibrated often.
Deviation Repercussions - As long as the oxide thickness is uniform for individual wafer, and it is thick enough to insulate the wafer completely, wafer-to-wafer uniformity does not matter.
Measurement Devices - Nanospec for film thickness, and the four-point probe for sheet resistance.

Gate Oxidation

Non-idealities - The furnace may not have been calibrated well enough in all zones, and the loading was extremely slow. As such, a thin oxide might have begun to grow during the wafers entering the furnace. Furthermore, the zone where the wafers were growing might not have been at a uniform temperature, or the gas flow might not have been sufficient to create the situation where the reaction is diffusion limited.

Device Repercussions - Dielectric constant increases with thickness of the dielectric material. And that in turn increases short channel effects. In general the dielectric thickness should be 1/10th of the gate thickness. Conversely if the gate oxide is too thin, the gate itself will not be able to affect the device, i.e., it will not act as a barrier for the carriers moving from source to drain and hence wont be able to control flow of current.
Measurement Devices - Nanospec was used for thickness, and the four-point probe for sheet resistance.

Poly Deposition

Non-idealities - Gas flow profile around wafer edges and from wafer to wafer is non-uniform. There amount of gas reaching the surface of the wafer is lower and lower the further away the wafer is from the source. We could not do anything to that, besides flowing the gas in as uniform a way as possible.
Device Repercussions - If poly is too thin, the intermediate oxide will eat into it. If the poly is too thick, the IV characteristics will change (will worsen).
Measurement Devices - Four-point probe to measure sheet resistance, and Nanospec for thickness (on a monitor wafer).

Source/Drain Pre-Diffusion

Non-idealities - There were possible temperature gradients within the furnace that we used, which could lead to different diffusion rates (as well as an uneven oxide growth). We pushed the wafers in at 1 inch every 10 seconds to avoid a large thermal gradient on the wafers and also pulled it out after the pre-diffusion at the same rate. We also let the wafers cool on the thermal rest area near the microscopes before proceeding to the SOG removal.
Device Repercussions - It will affect drive-in step as its recipe is based on certain pre-diffusion conditions.
Measurement Devices - No monitoring tools were used.

Drive-In and Intermediate Oxidation

Non-idealities - Temperature gradients in the furnace, as in our other processes, could lead to deviations. The water level should fall close to, but below, the opening in the bubbler apparatus which admits steam into the gas flow to the furnace. Make sure the release valve (cap)on the bubbler is loosely capped, or open the cap in case the steam pressure built up in the bubbler might push water into the furnace. Pushing in and pulling out wafer batch at 1 inch/10 seconds.
Device Repercussions - The intermediate oxide is too thick, it will eat into the polysilicon and the gate will not function/will disappear.
Measurement Devices - Nanospec for thickness, four-point probe for sheet resistance (on a monitor wafer).

Aluminum Evaporation

Non-idealities - The bell jar was not sealed properly, as the o-ring was damaged. Oxygen and water could have been inside of the chamber as a result, and damaged our aluminum film. Our GSI tried to ensure that the pressure went as low as possible before evaporation, so as to remove as many contaminants as possible.
Device Repercussions - The layer of Al2O3 is an insulator, not a conductor. So, the conductivity of the wire will be lowered. Additionally, mean free path of aluminum will be lowered and the atoms will interact with the molecules in the air.
Measurement Devices - Four-point probe for sheet resistance.

Sintering

Non-idealities - No sources of error. It is done at 400 C so slow push/pull is also not required. This step is done for better contact of aluminum and silicon, and to repair Si/SiO_2 interface.
Device Repercussions - If we don't sinter, we risk the aluminum and the silicon to not form a good contact with each other. It also allows hydrogen atoms to tie up "loose ends" at the oxide-channel interface.
Measurement Devices - None.

3.5 Section E

ACTV Photolithography - This step didn't matter all that much. The main deviation in this part of the process would be our develop and etch time. We overetched a tiny bit to make sure we got down to the wafer; this allows us to grow our gate oxide and make the rest of our MOSFET. Monitoring measurements used: ACTV linewidths

POLY Photolithography - The alignment of our mask, and develop time would have been our main deviations. We intentionally misaligned the mask to make sure the poly-silicon will cover the active area so that we can avoid short circuit when we do SOG diffusion. We also overetched slightly so that our gate oxide would be exposed for doping; if we didn't, our gate oxide wouldn't have been exposed and our phosphorous concetrations wouldn't have been as high, and our contacts might not have been deep enough. Monitoring measurements used: POLY-ACTV alignment markers, POLY linewidths.
SOG Deposition and SOG Strip - The distribution of the SOG might not have been uniform. During deposition, the slow push-in time might have also contributed to slightly different deposition times. We stripped as a group, so this step shouldn't have affected us too much (unless our SOG distribution isn't uniform, in which case the HF might have etched into our gate oxide). This would have made our wells deeper and closer to the silicon. No monitoring measurements, beyond temperature of the furnace and a timer.
CONT Photolithography - Our contacts were misaligned, which could lead to an increase in resistance for our devices. In addition, while we did the same etch time as everyone else, we might have had a different etch rate compared to others, as we did it separately. If we underetched, we could have gotten a contact well that wasn't deep enough into our oxide, which also could have resulted in an increase in resistance. Monitoring measurements: CONT linewidths, CONT alignment markers.
METL Photolithography - The alignment of our METL layer was basically spot-on, and so theoretically, this layer was perfect. Monitoring measurements: METL alignment markers.

4 Theoretical Calculations

4.1 Section A

Table 5: Oxide Thicknesses

Oxide	Theoretical Thickness Å	Measured Thickness Å	% Error
Field	4890	4779	2.26
Gate	800	706	11.75
Intermediate	1579	678	57.06

Field Oxide - The error might be due to non-idealities from batch processing. But it is in range of the expected values.
Gate Oxide - The error might be due to non-idealities in the furnace in EE143 lab. Compared to the furnace that the field oxide was grown in, this one is not calibrated for temperature.
Intermediate Oxide - This may be because the boiler lid is not properly sealed. Even in the fall 2013 batch, thickness varied a lot (750 - 9000 A) from run to run.

4.2 Section B

Pre-diffusion - Surface concentration of boron: $2.29 * 10^{16}$, surface concentration of phosphorous: $1.3 * 10^{21}$, theoretical junction depth: 0.95μm. Calculations in Appendix.
Drive-in - Surface concentration of boron: $3.8 * 10^{16}$, surface concentration of phosphorous: $1.48 * 10^{20}$, theoretical junction depth:

4.3 Section C

Table 6: Phosphorous

Step	Theoretical Surface Concentration	Measured Surface Concentration
Pre-Diffusion	$1.3 * 10^{21}$ cm^{-3}	$1.29 * 10^{21}$ cm^{-3}
Drive-in	$1.48 * 10^{20}$ cm^{-3}	

4.4 Section D

Calculations are in the Appendix, as well as the code used. Poly and sintering steps were omitted, as they do not contribute to the doping profiles compared to other steps.

Table 7: Boron

Step	Theoretical Surface Concentration	Measured Surface Concentration
Pre-Diffusion	0.95 μm	0.95 μm
Drive-in		

Figure 5: Boron profiles for all relevant steps

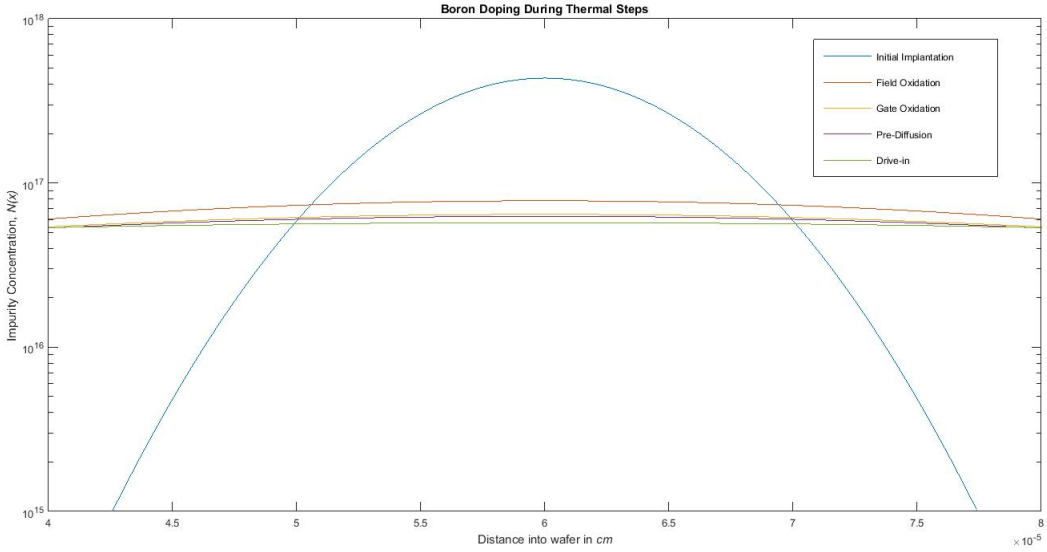
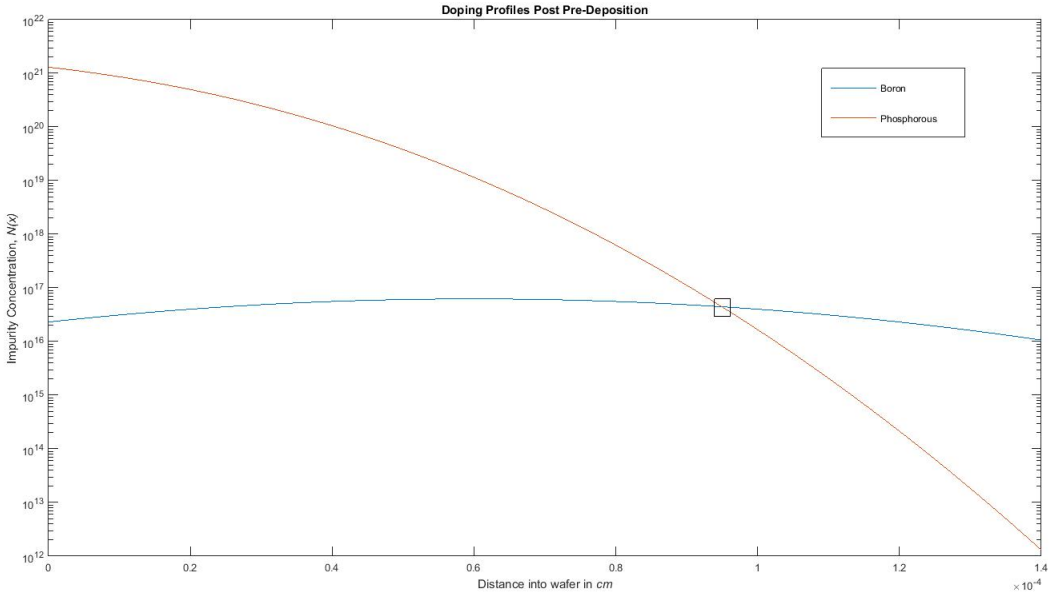


Figure 6: Boron and phosphorous profiles for pre-deposition step



4.5 Section E

We assume here that our diffusion is isotropic. As such, our lateral diffusion should reach as

5 Questions

5.1 Yellow Light Litho

Photolithography is done in yellow light because photoresist is sensitive to wavelengths ¡ 500 nm. If the wafer is exposed to fluorescent light before development, then desired pattern will not be transferred as the photoresist will get affected by the visible spectrum of light. After development, the wafer will not change since there are already patterns on them. Red light has wavelength 650-720 nm and hence wont affect the process.

5.2 Hard Bake

Hardbaking cross-polymerizes the PR polymer, making the photoresist physically hard, more adhesive, and less permeable to chemicals. If we skip the step, it can create cracks on the surface and delamination of the layer. The resist will harden so much that it wont be stripped as easily as expected and will damage the wafer.

5.3 Baking

The purpose is to dehydrate the wafers ; presence of water can damage the process. Baking after spinning on photoresist is to evaporate solvents and harden the resist. At such high temperatures, the photoresist properties might change and it will not react properly to the light.

5.4 PR

We use positive photoresist in the lab (OCG825) and it is G-line. I-line and G-line are different wavelengths, the former in the near UV region and the latter in visible region. On spinning, it adheres to the wafer surface due to HMDS presence. In the regions of exposure, the polymer chains break. On development, regions exposed to the light get dissolved.

5.5 Ethcing Time

In process detail, we can find that the etching rate of thermal SiO2 for 5:1 BHF is 1000A/min. Field Oxide: Theoretical time: 4 mins 47s*(1+15%) = 5 mins 30s
This is much lower than the experimental time 7mins 30s. Maybe because the concentration of BHF is lower than expected.
Etch rate: 2200 /min for poly-Si
Poly Silicon: Theoretical time: 3mins 18s*(1+15%)=3 mins 48s This is much lower than the experimental time 15mins. From the process detail, the etching time of poly-Si will increase a lot after exposed to air. Gate Silicon: Theoretical time: 43s*(1+20%)=52s
This is very close to the experimental time 45s.
Intermediate Oxide: Theoretical time: 41s*(1+100%)=1 min 22s
It is a little close to the experimental time 2mins. But actually it is still a long etching to make sure of good hole contacts.
Etch rate of Al is 100 /sec
Aluminum: 100 * 105s = 10500
Emperical:
Wafer turns black after etching polysilicon. The back side of the wafer de-wets (metallic in color) indicating no oxide present (contacts).

5.6 Wet vs Dry Oxides

Wet: Faster, low quality film.
Dry: Slower, high quality film.
We do not care about the quality of field/intermediate oxides as they are just for insulation from substrate and for making contacts respectively, i.e. they are sacrificial layers. Gate oxide, however, affects device performance and

thus needs to be thin (as a dielectric between channel and gate electrode) and of high quality. Annealing in nitrogen ensures repair of silicon lattice bonds.

5.7 5:1 vs 10:1 BHF

5:1 BHF allows for us to actually etch our features, whereas 10:1 BHF isn't strong enough to the point where it may eliminate features. BHF is used to maintain a more consistent etch rate (as opposed to regular HF).

5.8 Native Oxide

Presence of native oxide dramatically lowers rate of oxide growth and we wont get a true measurement of the thickness of our gate. And we do need to precisely control gate oxide thickness. Phosphorus is does not have a good diffusivity through oxide. So, it wont get into the wafer where we actually intend to have it.

5.9 Etch Selectivity

The ratio between the rate of etching of desired material to that of the material surrounding/under it.

5.10 HF Dip Skip

10. What would happen if we skipped the HF dip before metallization? [2 pts.] There would be a thin oxide layer on the parts where we need the metal, and oxides are insulators. So, our device wont function. Even if it does, conductivity will be low.

5.11 Al Etchant

Al etchant has a composition of (approximately) 80% Phosphoric acid, 10% H_2 , 5% acetic acid, and 5% nitric acid. If done at room temperature, the etch rate will be very low. Sintering is done to strengthen Si-Al bonds for better connection and also to repair silicon/silicon dioxide interface by hydrogen.

5.12 Roughing Pumps

Roughing pump can pump the chamber to about 10^3 Torr automatically but our target is $2 - 5 * 10^{-6}$ torr. So we have to pump it further to reach a low vacuum space with diffusion pump. Based on the figure from Ref website, the pressure range of the diffusion pump is from 10^{-2} Torr to 10^{-10} Torr. And the pump is sensitive to the gas so it cannot be too high pressure.

5.13 Alternate Methods

Sputtering instead of evaporation of metal - Tradeoff is expensive equipment.
Ion Implantation instead of spin-on glass - High equipment cost, maintenance cost, and space.

5.14 TSuprem4

Code will be included in Appendix.

Figure 7: Field Oxide

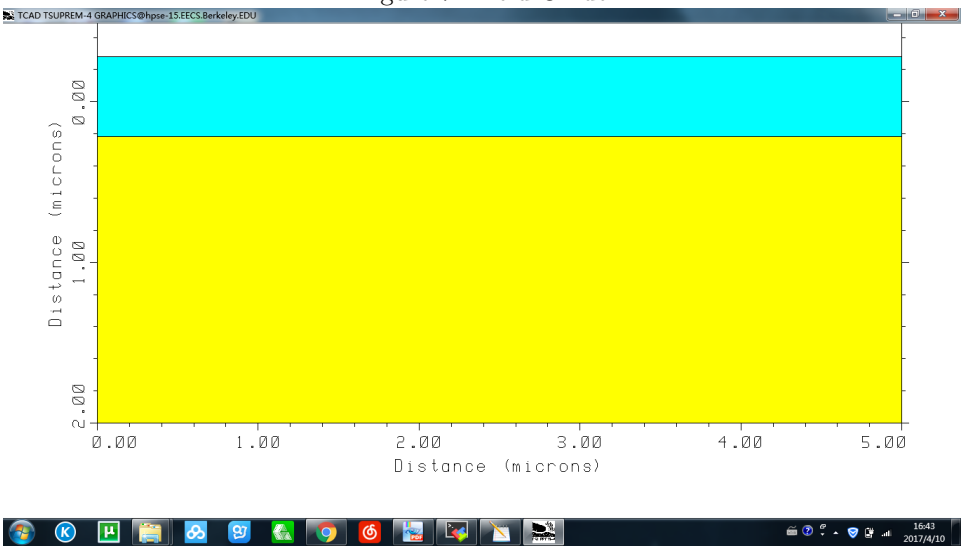
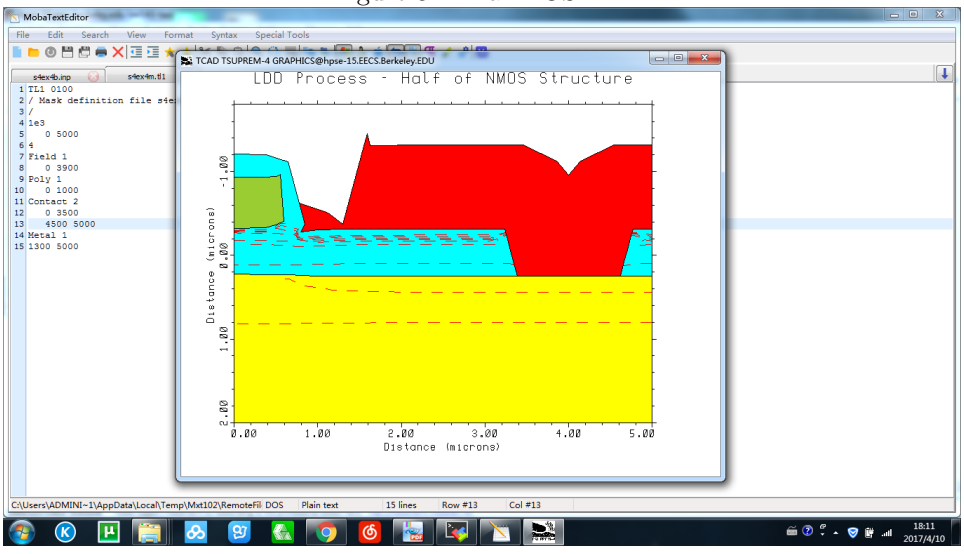


Figure 8: Final MOSFET



Appendices

1 Boron Calculations

To calculate our boron profiles, we used the equation

$$N(x) = N_p \exp[\frac{(x-R_p)^2}{2(\Delta R_p + \sqrt{Dt_{total}})^2}]$$

We use the expression $(\Delta R_p + \sqrt{Dt})$ because the initial equation for the ion implantation will give us our doping profile at the very beginning, but during all of our other thermal steps, our doping profile will change similarly to a limited source diffusion, and so we make our ΔR_p change with our Dt, as in the equations for limited source diffusion. To justify this, we made a few assumptions for our boron profiles. 1) The diffusion after implantation for Boron will still make the profile a Gaussian profile but the ΔR_p will increase while N_p will decrease because our dose Q will be constant. Therefore, all subsequent N_p values will be proportional to a known Q and initial N_p (e.g. $N_p \Delta R_p = N_{FieldOxide}(\Delta R_p + \sqrt{Dt_{FieldOxide}})$). 2) The Oxide is too thin to eat some dopant. 3) Diffusion only relates to the temperature and time so when calculating the profile, segregation at the interface is not taken into account. 4) The high concentration of phosphorous will not affect the diffusion of the low concentration of Boron.

2 Phosphorous/Irvin's Curves

For the pre-diffusion, we can use use the Irvin's curve from the reference and assume the profile is a erfc function. So by the multiplication of sheet resistance and the theoretical junction depth, we get the resistivity and with the N(background) to be about $10^(17)$, we can read out the surface concentration on the figure.
For the drive-in step, we still consider it as a erfc function so there will be some error between the measured one and the theoretical one. We can just consider a little bar at the surface so that it will diffuse like a gaussian profile. Since the dose will not change when the bar diffuse, the new surface concentration can be calculated by

$$N_{new} = \frac{N_{oldsurface}}{\sqrt{D_{drive} t_{drive}}} \sqrt{\frac{D_{prediffusion} t_{prediffusion}}{\pi}}$$

3 TSuprem4

Field Oxide

```
$ TMA TSUPREM4 NMOS transistor simulation
$   Part a:  Through field oxidation

SOURCE  TS4.config

$ Define the grid
MESH       GRID.FAC=1.5
METHOD     ERR.FAC=2.0

$ Read the mask definition file
MASK       IN.FILE=s4ex4m.tl1  PRINT  GRID="Field,Poly"

$ Initialize the structure
INITIALIZE <100>  BORON=5E15

$ Boron field implant
IMPLANT    BORON  DOSE=6E12  ENERGY=16  TILT=7  ROTATION=30

$ Field oxidation
METHOD     PD.TRANS  COMPRESS
DIFFUSION  TIME=5   TEMP=1000  DRYO2
DIFFUSION  TIME=85  TEMP=1000  WETO2
DIFFUSION  TIME=5   TEMP=1000  DRYO2

$ Save structure
SAVEFILE   OUT.FILE=S4EX4AS
```

```
$ Plot the initial NMOS structure
SELECT     Z=LOG10(BORON)  TITLE="LDD Process - NMOS Isolation Region"
PLOT.2D    SCALE GRID C.GRID=2 Y.MAX=2.0
PLOT.2D    SCALE  Y.MAX=2.0

$ Color fill the regions
COLOR      SILICON  COLOR=7
COLOR      OXIDE    COLOR=5

$ Plot contours of boron
FOREACH    X  (15 TO 20 STEP 0.5)
CONTOUR    VALUE=X  LINE=5  COLOR=2
$END

$ Replot boundaries
PLOT.2D    ^AX  ^CL

$ Print doping information under field oxide
SELECT     Z=DOPING
PRINT.1D   X.VALUE=4.5  X.MAX=3

savefile out.f=s4ex4a.tif tif
```

Mosfet

```
$ TMA TSUPREM4 NMOS transistor simulation
$   Part b:  Through source/drain metallization

SOURCE  TS4.config

$ Set grid spacing and accuracy parameters
MESH      GRID.FAC=1.5
METHOD    ERR.FAC=2.0

$ Read structure from initial simulation
INITIAL   IN.FILE=S4EX4AS

$ Read the mask definition file
MASK      IN.FILE=s4ex4m.tl1

$ Gate oxidation
METHOD     PD.TRANS  COMPRESS
DIFFUSION  TIME=45   TEMP=1100  DRYO2

$ Define polysilicon gate
MATERIAL  MAT=POLY ^POLYCRYS
DEPOSIT   POLYSILICON  THICK=0.7248  SPACES=2
DEPOSIT   PHOTORESIST  THICK=1.0
EXPOSE    MASK=Poly
DEVELOP
ETCH    POLYSILICON  TRAP  THICK=2.0  ANGLE=79
ETCH          PHOTORESIST  ALL

$PRE DIFFUSION
METHOD     PD.TRANS  COMPRESS
DIFFUSION  TIME=10   TEMP=1050  PHOSPHOR=1.3E21
```

```
$ Oxidize the polysilicon gate
DIFFUSION TIME=10  TEMP=1050  WETO2
DIFFUSION TIME=27  TEMP=1050  N2


$ Plot structure
SELECT    Z=LOG10(BORON)  TITLE="LDD Process - After LDD Implant"
PLOT.2D   SCALE  Y.MAX=2.0

$ Add color fill
COLOR     SILICON  COLOR=7
COLOR     OXIDE    COLOR=5
COLOR     POLY     COLOR=3
COLOR

$ Plot contours
FOREACH   X  (15 TO 18 STEP 0.5)
  CONTOUR   VALUE=X  LINE=5  COLOR=2
END
SELECT    Z=LOG10(ARSENIC)
FOREACH   X  (16 TO 20)
  CONTOUR   VALUE=X  LINE=2  COLOR=4
END

$ Replot boundaries
PLOT.2D   ^AX  ^CL

$ Deposit BPSG and cut source/drain contact holes
DEPOSIT   PHOTORESIST  POSITIVE  THICKNESS=1.0
EXPOSE    MASK=Contact
DEVELOP
ETCH      OXIDE  THICKNESS=1.0  TRAP  ANGLE=75
ETCH      PHOTORESIST  ALL

$ Define the metallization
DEPOSIT   ALUMINUM  THICKNESS=1.0
DEPOSIT   PHOTORESIST  POSITIVE  THICKNESS=1.0
EXPOSE    MASK=Metal
DEVELOP
ETCH      ALUMINUM  TRAP  THICKNESS=1.5 ANGLE=75
ETCH      PHOTORESIST  ALL

$ Save the final structure
SAVEFILE  OUT.FILE=S4EX4BS

$ Plot the half NMOS structure
SELECT    Z=LOG10(BORON)  TITLE="LDD Process - Half of NMOS Structure"
PLOT.2D   SCALE  Y.MAX=2.0  GRID C.GRID=2
PLOT.2D   SCALE  Y.MAX=2.0

$ Color fill
COLOR     SILICON  COLOR=7
COLOR     OXIDE    COLOR=5
COLOR     POLY     COLOR=3
COLOR     ALUM     COLOR=2
```

```
$ Plot contours
FOREACH   X  (15 TO 18 STEP 0.5)
  CONTOUR   VALUE=X  LINE=5  COLOR=2
END
SELECT    Z=LOG10(ARSENIC)
FOREACH   X  (15 TO 20)
  CONTOUR   VALUE=X  LINE=2  COLOR=4
END

$ Replot boundaries
PLOT.2D   ^AX  ^CL

$ Print doping through drain
SELECT    Z=DOPING
PRINT.1D  LAYERS  X.VALUE=2

savefile out.f=s4ex4b.tif tif
```

4 References

BYU Oxide Calculator - http://www.cleanroom.byu.edu/OxideThickCalc.phtml For calculations regarding theoretical oxide thicknesses.

Irvin's Curves - http://ac.els-cdn.com/003811019390257Q/1-s2.0-003811019390257Q-main.pdf?_tid=1346ea86-1e56-11e7-b236-00000aacb35e&acdnat=1491874249_6b03784e383af75b1e07deef0d9f1d78 For experimentally measured surface concentration.

Introduction to Microelectronic Fabrication by Richard C. Jaeger - For equations and constants regarding diffusion, as well as information on etching.

All of Javey's Lectures - For notes on BHF, graphs on equations needed, and possible issues in calculations.