Lab Report 2

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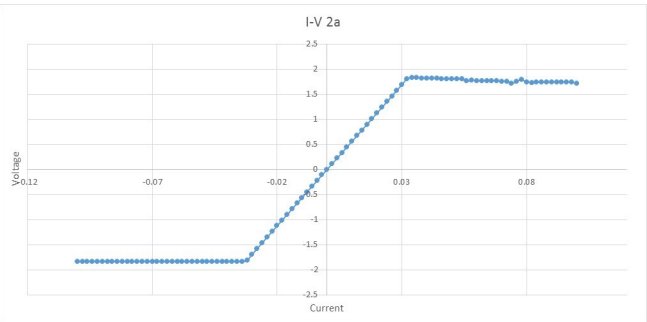
May 5, 2017

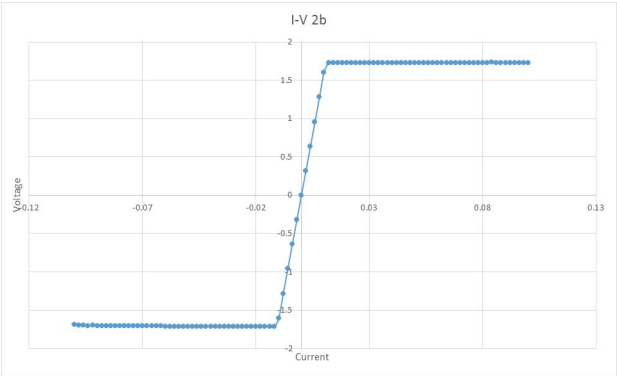
1 Devices & Procedures

Will be included at the end of the report.

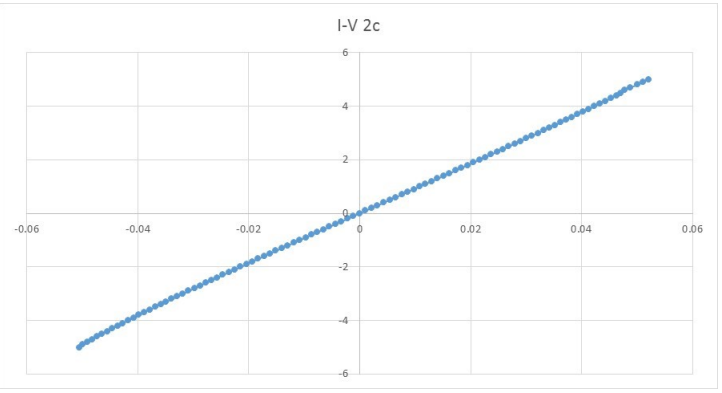
2 Measured Data

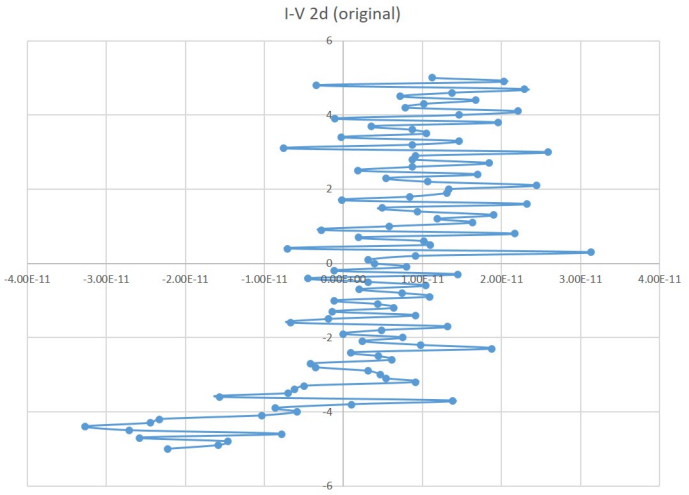
2.1 4-Point Resistors

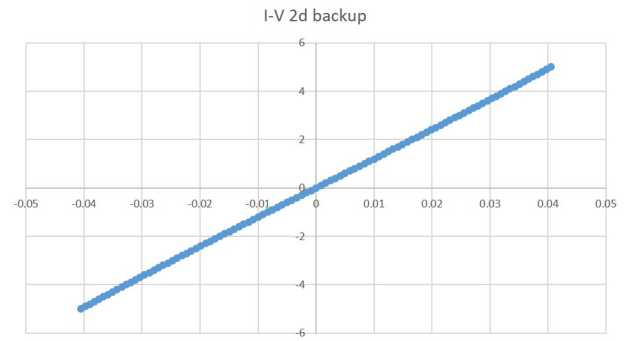




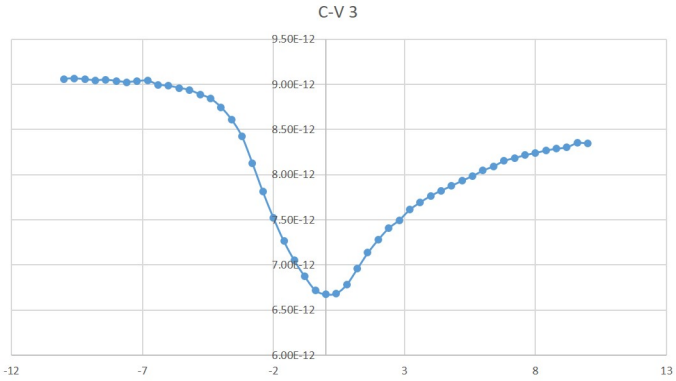
2.2 Contact-Chain Resistors

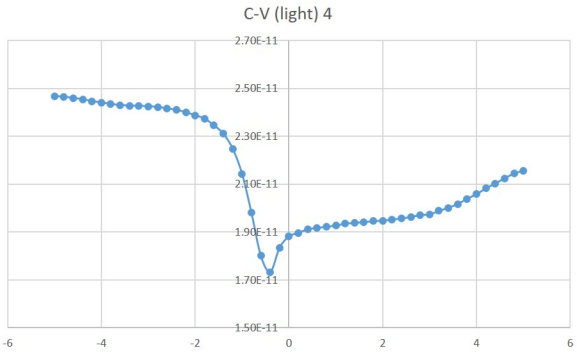


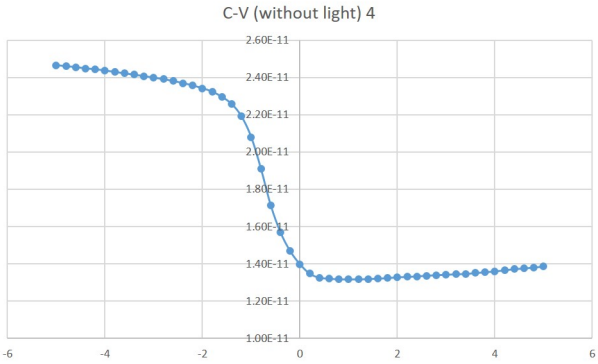


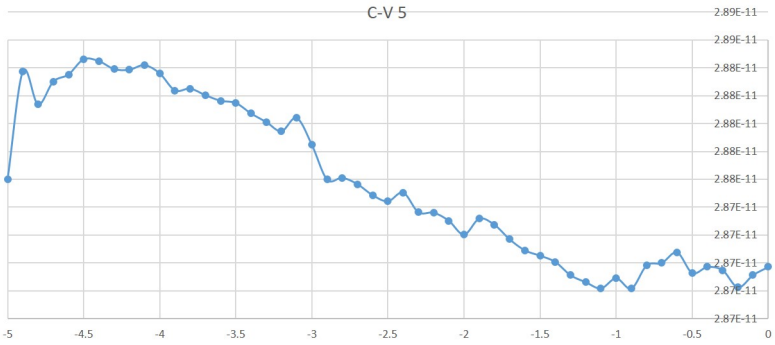


2.3 MOS Capacitors

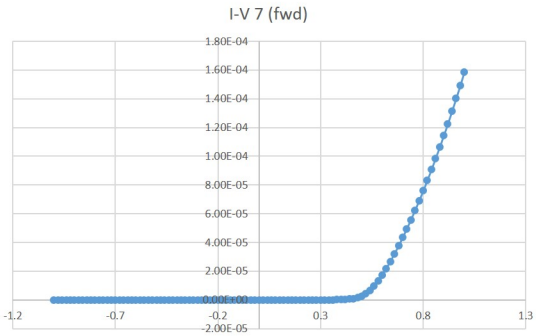


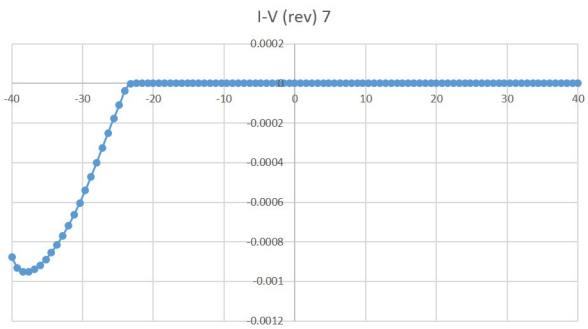






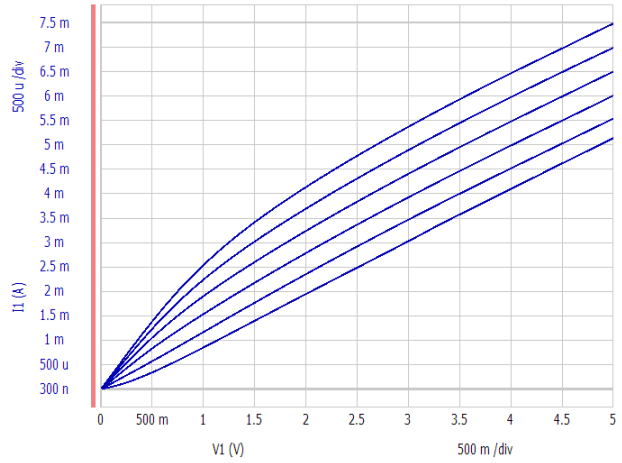
2.4 Diode

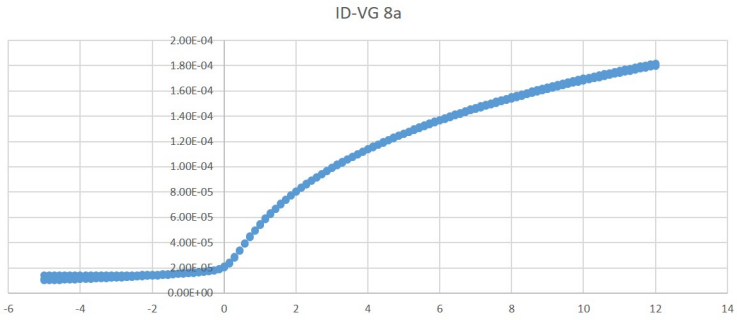


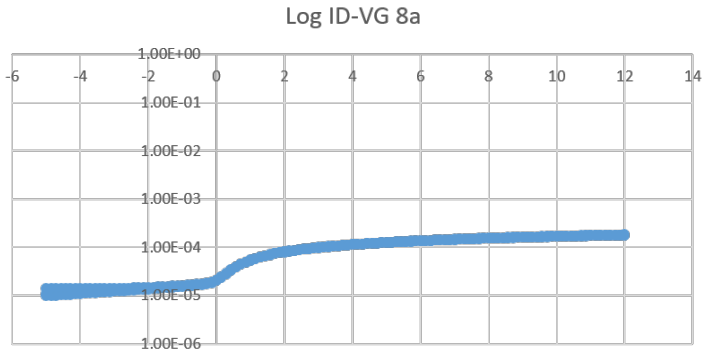


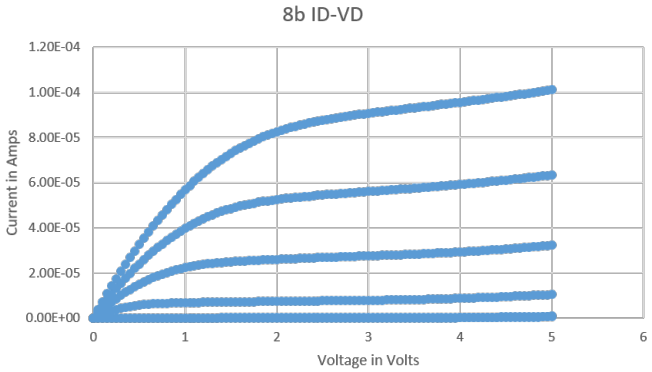
2.5 MOSFETs - Varying Length

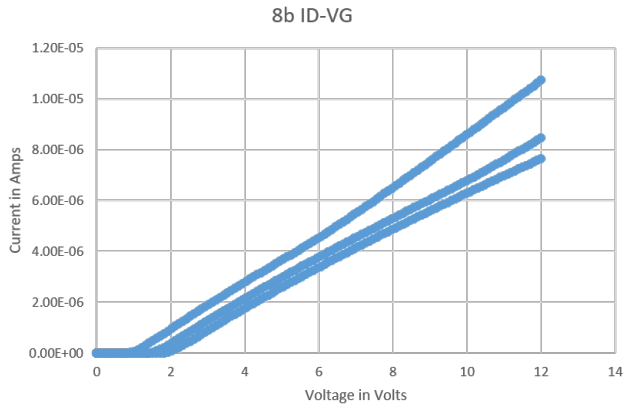
8a ID-VD graph from EasyExpert was used with permission from Kevin.

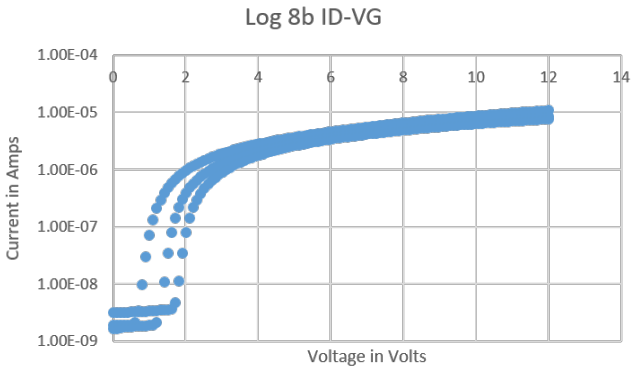


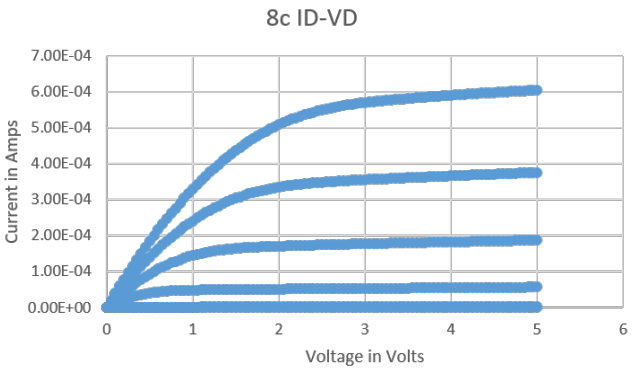


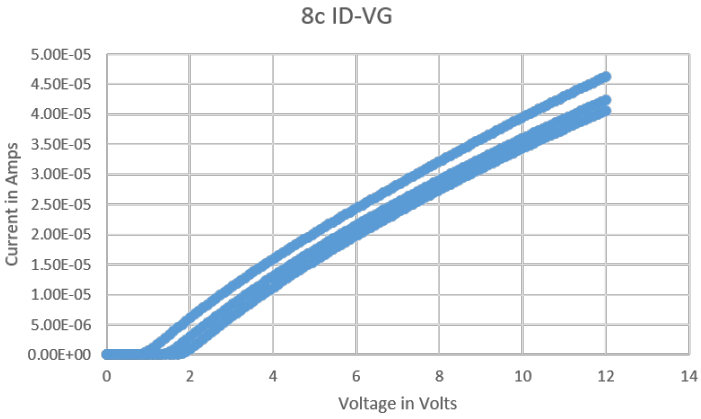


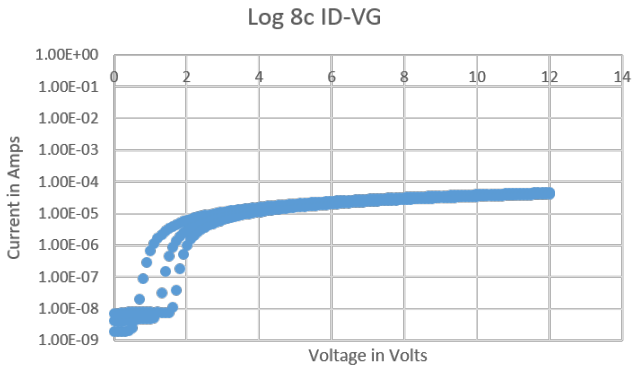


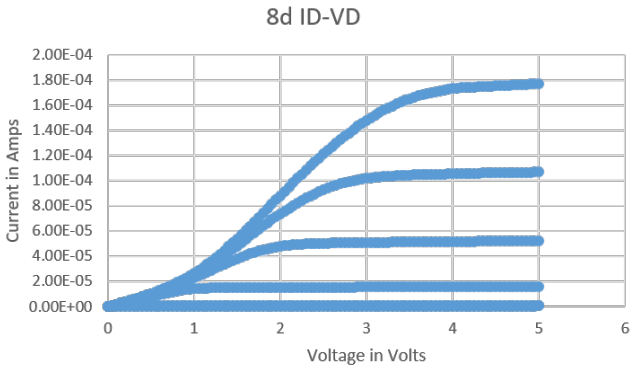


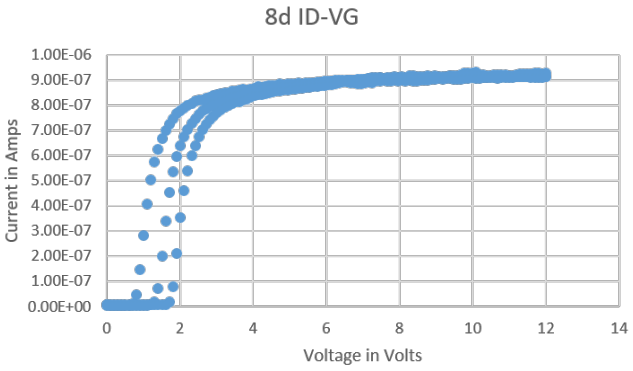


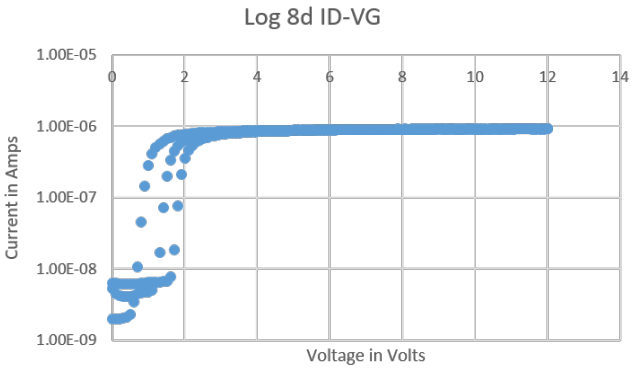

8c ID-VD
Current in Amps
7.00E-04
6.00E-04
5.00E-04
4.00E-04
3.00E-04
2.00E-04
1.00E-04
0.00E+00
0
1
2
3
4
5
6
Voltage in Volts


8c ID-VG
Current in Amps
5.00E-05
4.50E-05
4.00E-05
3.50E-05
3.00E-05
2.50E-05
2.00E-05
1.50E-05
1.00E-05
5.00E-06
0.00E+00
0
2
4
6
8
10
12
14
Voltage in Volts


Log 8c ID-VG
Current in Amps
1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
0
2
4
6
8
10
12
14
Voltage in Volts

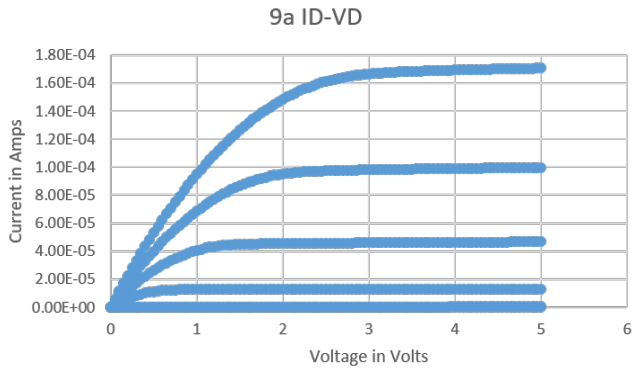

8d ID-VD
Current in Amps
2.00E-04
1.80E-04
1.60E-04
1.40E-04
1.20E-04
1.00E-04
8.00E-05
6.00E-05
4.00E-05
2.00E-05
0.00E+00
0
1
2
3
4
5
6
Voltage in Volts

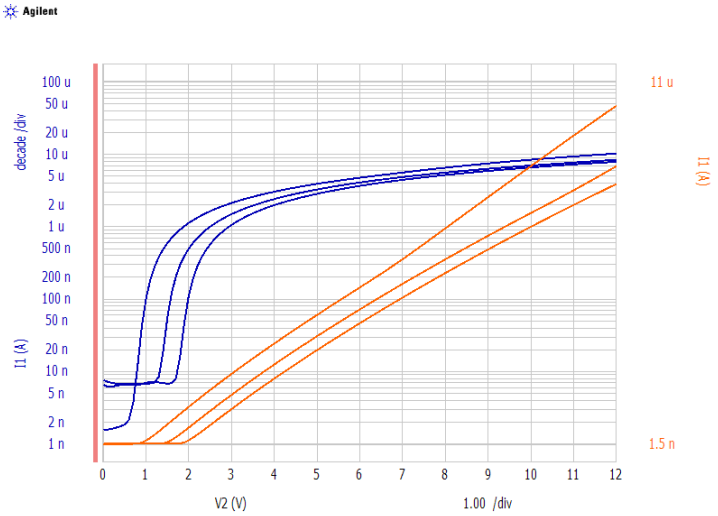

8d ID-VG
Current in Amps
1.00E-06
9.00E-07
8.00E-07
7.00E-07
6.00E-07
5.00E-07
4.00E-07
3.00E-07
2.00E-07
1.00E-07
0.00E+00
0
2
4
6
8
10
12
14
Voltage in Volts

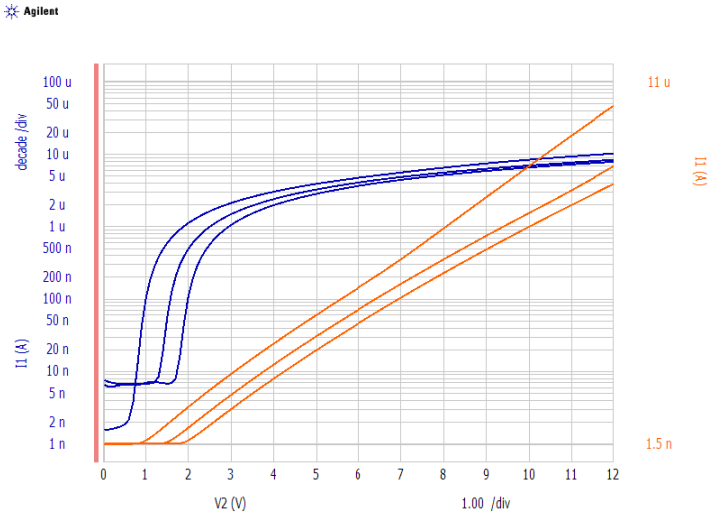

Log 8d ID-VG
Current in Amps
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
0
2
4
6
8
10
12
14
Voltage in Volts

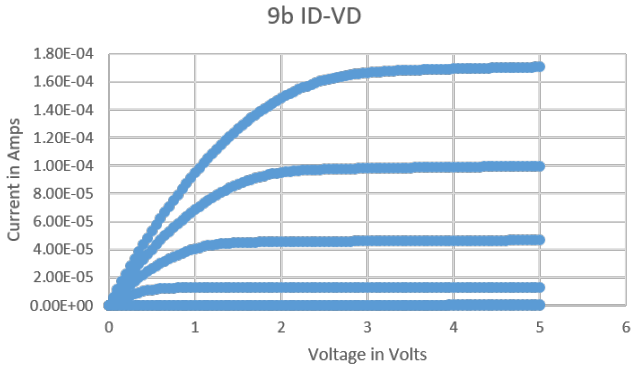
2.6 MOSFETs - Varying Width

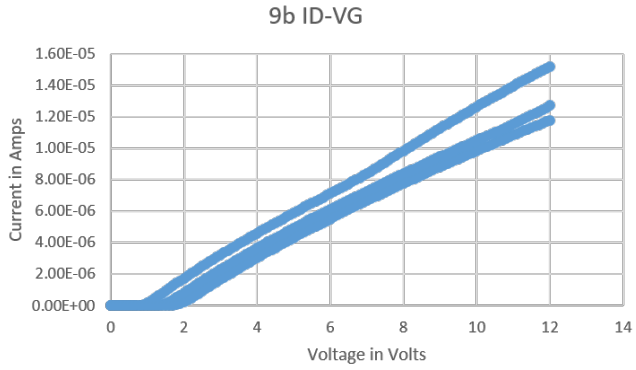
9a ID-VG graphs used with permission from Kevin.

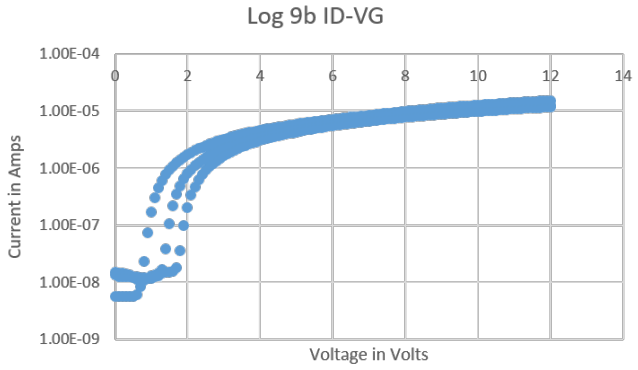


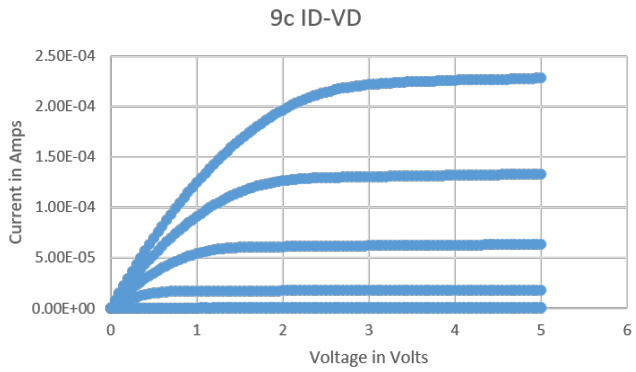


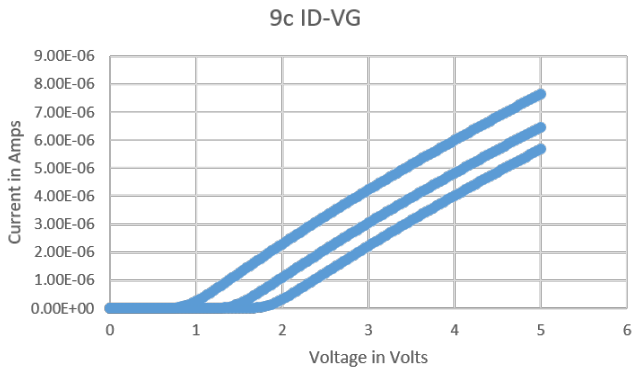


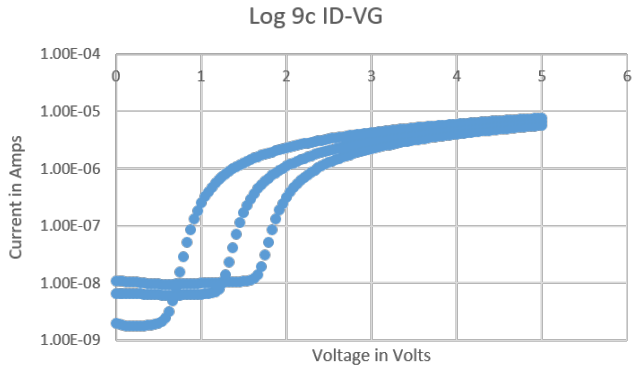




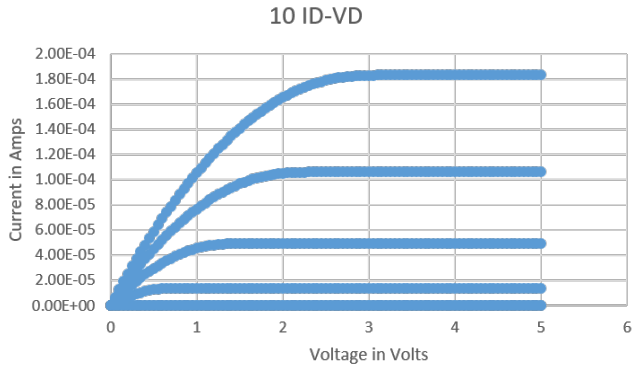


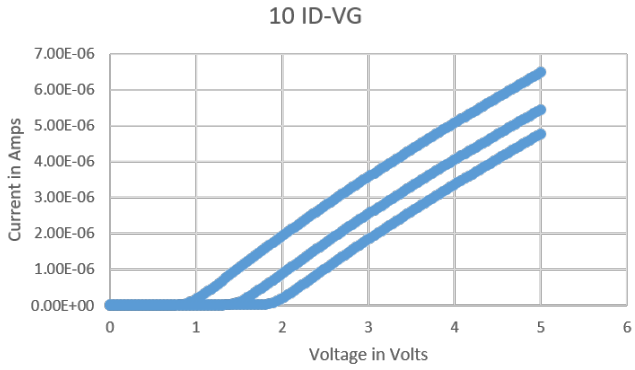


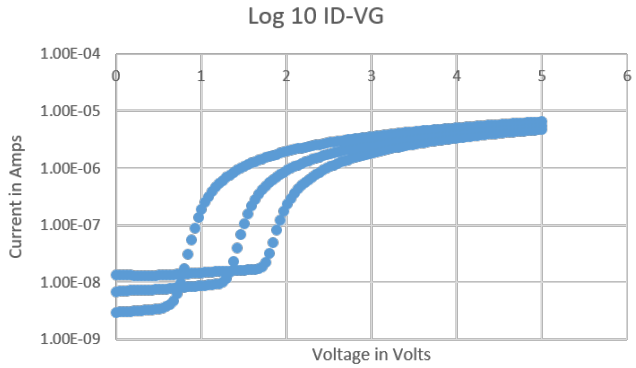


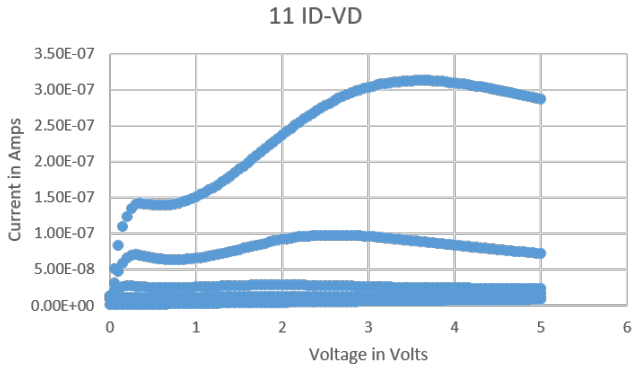


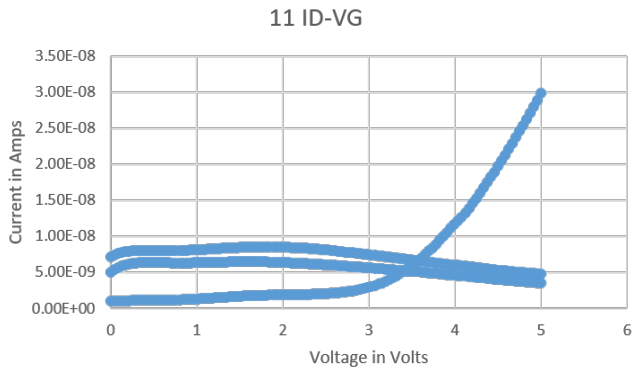
2.7 Other MOSFETs

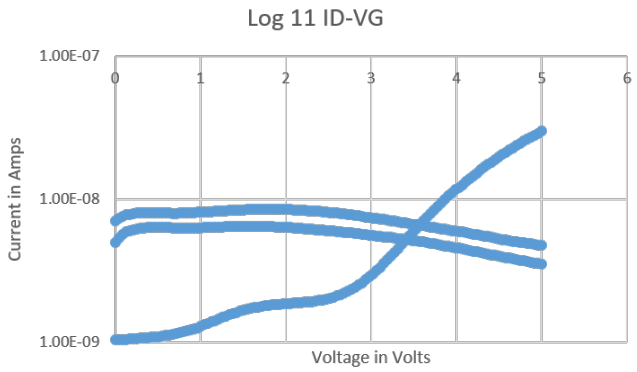


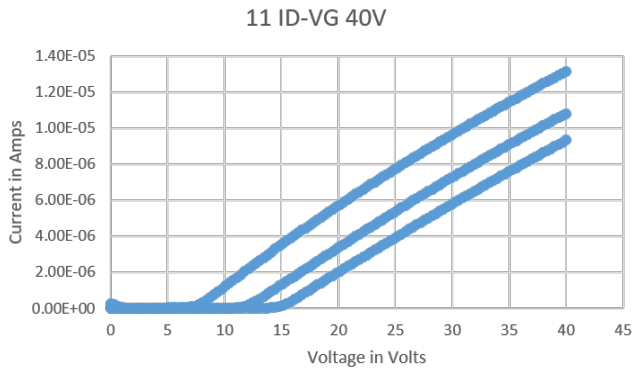


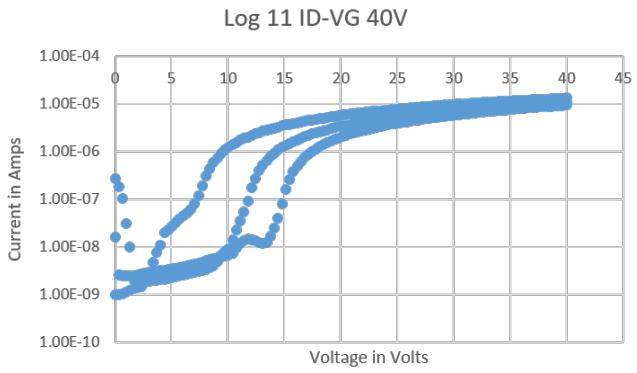




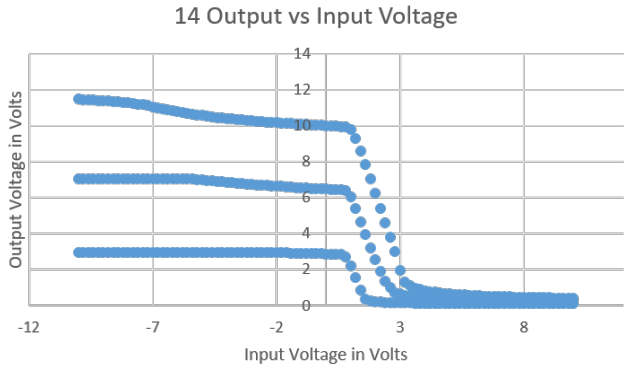








2.8 Inverter



3 Data Analysis

3.1 Line Width Overetch

Table 1: Overetch percentages for each layer

% Overetch	2 μm	3 μm	6 μm	8 μm
ACTV	8.9	-6.51	1.19	-7.15
POLY	73.52	62	33	19.22
CONT	-22.71	7.32	7.66	-1.44
METL	100	21.56	21.2	2.6

3.2 4-Point Resistors

Equations used were the 4-point probe resistance equations given in Section 7 of our lecture slides. Specifically, we used $\rho = \frac{\pi t}{ln2}\frac{V}{I}$, which we used because of our separation between our contact pads was much greater than our thickness, which we took to be our junction depth ($66.67\mu\text{m} >> 1.3\mu\text{m}$).

To calculate our post etch L and W, we use the above over/underetch percentages and apply them to their respective lines to calculate the total amount of over/underetch from our features.

$$8 \times -0.0715 = -0.572\mu\text{m}$$
$$6 \times 0.019 = 0.114\mu\text{m}$$
$$3 \times -6.51 = -0.1953\mu\text{m}$$
$$2 \times 0.089 = 0.178\mu\text{m}$$
$$\text{Etch Average for ACTV} = \frac{-0.572 + 0.114 - 0.1953 + 0.178}{4} = -0.4753\mu\text{m}$$

and end up with

$$L_{2a-post} = 200 - 0.4753 = 199.525\mu\text{m} \tag{1}$$
$$W_{2a-post} = 10 - 0.4753 = 9.525\mu\text{m} \tag{2}$$

We chose to use average of the etch percentages, as that should best represent the actual etching of the lines on the device.

Similarly, for 2b, we have

$$8 \times 0.1922 = 1.5376\mu\text{m}$$
$$6 \times 0.33 = 1.98\mu\text{m}$$
$$3 \times 0.62 = 1.86\mu\text{m}$$
$$2 \times .7352 = 1.47\mu\text{m}$$
$$\text{Etch Average for POLY} = \frac{1.5376 + 1.98 + 1.86 + 1.4704}{4} = 1.712$$

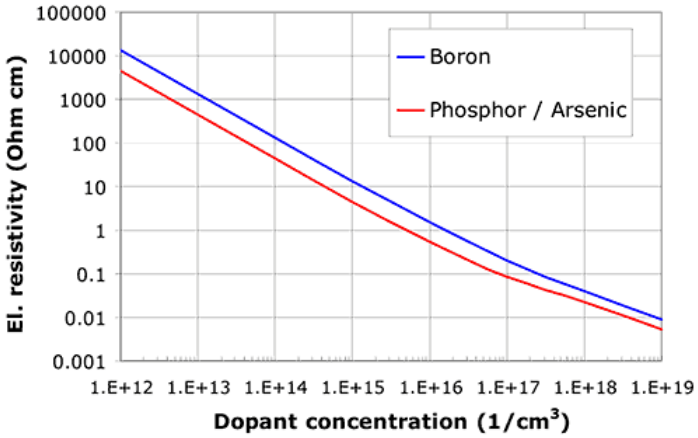
which results in

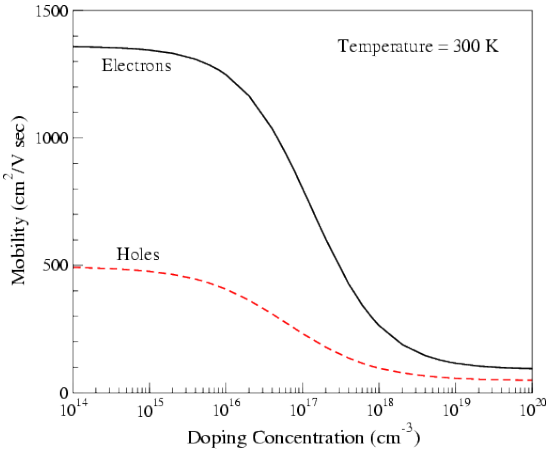
$$L_{2b-post} = 200 + 1.712 = 201.712\mu\text{m} \tag{3}$$
$$W_{2b-post} = 10 + 1.712 = 11.712\mu\text{m} \tag{4}$$

To calculate our resistances, we used $V = IR$ and chose any point on the plot (in this case, where our graph flattens out at the maximum current), to calculate our resistance. For 2a, we chose $V_a = 2\text{V}$ and $I_a = 0.03\text{A}$, and for 2b, $V_b = 1.72\text{V}$ and $I_b = 0.012\text{A}$.

$$R_a = \frac{V_a}{I_a} = \frac{2}{0.03} = 66.67\Omega \tag{5}$$
$$R_b = \frac{V_b}{I_b} = \frac{1.72}{0.012} = 143.33\Omega \tag{6}$$
$$\rho_a = \frac{\pi t}{\ln 2} R_a = \frac{\pi x_j}{\ln 2} R_a = 0.03926\Omega\text{cm} \tag{7}$$
$$\rho_b = \frac{\pi t}{\ln 2} R_b = \frac{\pi t_{poly}}{\ln 2} R_b = 0.047085\Omega\text{cm} \tag{8}$$

We took the thickness in ρ_a to be the junction depth because that is how deep the effective conductive layer is, and beyond that, the oxide just becomes a p-type silicon and it becomes uninteresting. We take the thickness in ρ_b to be the thickness of the polysilicon because the poly is our conductive layer.





For our N_D, we used the definition of electrical conductivity and rearranged it to go ahead and obtain a relationship between N_D.

$$\sigma = \frac{1}{\rho} = N_D \mu q$$

We're able to use this relationship because of our n-type doping. We then use this to obtain

$$N_D = \frac{1}{\rho \mu q} \tag{9}$$

We use standard resistivity plots for our μ value in crystalline silicon; from these we can deduce that our polysilicon μ is going to be 10 times smaller than our crystalline silicon μ from the graph below because $\rho \propto \frac{1}{\mu}$ (a relationship we can get above from (9)), and the crystalline silicon resistivity is consistently 10 times lower than polysilicon resistivity for the same dopant concentration.

From these plots, we can get that our $\mu_{crystalline} \simeq 120$ cm^2/(V*s), and so our $\mu_{poly} \simeq 12$ cm^2/(V*s), which we then use to find our N_D.

$$N_{D-poly} = \frac{1}{\rho \mu_{poly} q} = \frac{1}{0.047085 * 12 * 1.6 * 10^{-19}} = 1.1 * 10^{19} \tag{10}$$

$$N_{D-silicon} = 3.1 * 10^{17} \text{(From lab report 1)} \tag{11}$$

For the sheet resistance, we refer to an equation in Section 7 of our lecture notes in the four-point probe section, $R_s = \frac{pi}{\ln 2} \frac{V}{I} \simeq 4.53R$.

$$R_{s-a} = 4.53 * (66.67) = 302.015 \tag{12}$$

$$R_{s-b} = 4.53 * (143.33) = 649.285 \tag{13}$$

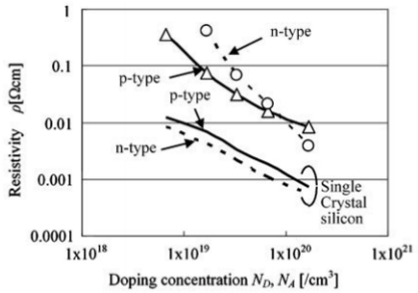


Fig. 4. Dependences of resistivities of fabricated p-type and n-type polysilicon resistors on doping concentration.

Table 2: Device 2a

R[kΩ]	W' [μm]	L'[μ]	R_s [ohm/sq]	x_j [μm]	ρ [ohm-cm]	N_D [cm^{-3}]
.066	9.525	199.525	302	1.3	0.03926	$3.1 * 10^{19}$

Table 3: Device 2b

R[kΩ]	W' [μm]	L'[μ]	R_s [ohm/sq]	x_j [μm]	ρ [ohm-cm]	N_D [cm^{-3}]
143.33	11.712	201.712	649.285	1.3	0.084	$1.1 * 10^{19}$

3.3 Contact-Chain Resistors

We had 14 contact pads and 7 resistive pads all linked in series. We estimate all of the pads to be squares, and so our total resistance works out to be

$$R_{total} = R_{contacts} + R_{pads} = 14R_{single-contact} + 7R_{single-pad} \tag{14}$$

The total resistance of our devices were worked out again from $V = IR$ and our values for V and I were obtained from our data.

$$V_c = 2.5; I_c = 0.0268$$
$$V_d = 1, I_d = 0.00833$$

We then used these values, and our sheet resistances from the previous devices, to obtain our values below.

$$R_c = \frac{2.5}{.0268} = 93.006\Omega \tag{15}$$
$$R_d = \frac{1}{0.00833} = 120.05\Omega \tag{16}$$
$$R_{contacts-c} = R_c - R_{pads-c} = R_c - 7R_{s-a} = 93.006 - 7(302.015) = -2021.04\Omega \tag{17}$$
$$R_{contacts-d} = R_d - R_{pads-d} = R_d - 7R_{s-b} = 120.05 - 7(649.285) = -4424.95\Omega \tag{18}$$
$$R_{single-contact-c} = \frac{R_{contacts-c}}{14} = \frac{-2021.04}{14} = -144.36\Omega/\text{sq} \tag{19}$$
$$R_{single-contact-d} = \frac{R_{contacts-c}}{14} = \frac{-4424.95}{14} = -316.068\Omega/\text{sq} \tag{20}$$

For area, we refer to our overetch rate chart above and instead of averaging out over all etches, we just do the 8, 6, and 3 μm lines and leave out the 2 μm line, as it is a pretty large outlier.

$$8 * .026 = 0.208$$
$$6 * .0766 = 0.4596$$
$$3 * .0732 = 0.2196$$
$$\text{Etch Average} = \frac{0.208 + 0.4596 + 0.2196}{3} = 0.2957$$

And so our contact area is

$$A_{contact} = (5 - 0.2957)^2 = 22.13\mu\text{m} \tag{21}$$

Contact resistivity calculations were made using the definition of sheet resistance, $\rho = R_s t$, where the thickness we used is the aluminum thickness we calculated from lab report 1 (1.05μm).

$$\rho_{c-c} = R_{s-contact-c} t_{alum} = -144.36\Omega * 1.05 * 10^{-4}\text{cm} = -0.0151\Omega - \text{cm}^2 \tag{22}$$
$$\rho_{c-d} = R_{s-contact-d} t_{alum} = -316.068\Omega * 1.05 * 10^{-4}\text{cm} = -0.0331\Omega - \text{cm}^2 \tag{23}$$

Table 4: Device 2c

R_{total} [kΩ]	$R_{contacts}$ [kΩ]	$R_{single-contact}$ [kΩ]	$A_{contact}$ [μm^2]	ρ_c[Ω-cm^2]
93.006	-2021.04	-144.36	22.13	-0.0151

Table 5: Device 2d

R_{total} [kΩ]	$R_{contacts}$ [kΩ]	$R_{single-contact}$ [kΩ]	$A_{contact}$ [μm^2]	ρ_c[Ω-cm^2]
120.05	-4424.95	-316.068	22.13	-0.0331

3.4 MOS Capacitors

Devices 3 and 5 are relatively low on the calculation side. The only calculation we have to make is in the area and the normalization.

For the area, we use the overetch from the METL area and apply it here, as the overetch from there should have affected the size of the metal die.

$$A_{cap-3} = A_{cap-5} = (200 - 0.2957)^2 = 39881.8\mu^2 = 3.99 * 10^{-4}\text{cm}^2 \tag{24}$$

$$C_{ox-normalized-3} = \frac{9 * 10^{-12}}{3.99 * 10^{-4}} = 2, .257 * 10^{-8} \tag{25}$$

$$C_{ox-normalized-5} = \frac{28.8 * 10^{-12}}{3.99 * 10^{-4}} = 7.2 * 10^{-8} \tag{26}$$

Table 6: Device 3

C_{ox} [pF]	A_{cap}[μm^2]	$C_{ox-normalized}$ [F/cm^2]	t_{ox}[nm]
9	39881.8	$2.257 * 10^{-8}$	152.5

Table 7: Device 5

C_{ox} [pF]	A_{cap}[μm^2]	$C_{ox-normalized}$ [F/cm^2]	t_{ox}[nm]
28.8	39881.8	$7.2 * 10^{-8}$	47.94

Device 4 characterization is more intense calculation-wise. To begin with, we look at the data we extracted from our devices and extract our C_{FB}, V_{FB}, C_{DEP-on}, $C_{DEP-off}$, V_T from the data. We look to the left of side of the graph (the negative voltages) to find our flatband values and when the values stabilize on the right side to find our depletion values. To make sure our voltages are correct, we cross reference the voltages between the light on and off data sets, and make sure the capacitances stabilize at the same place. Our t_{ox} is obtained from our lab report 1.

To determine the doping concentration of the silicon, we know that the capacitances are related by

$$\frac{1}{C_{DEP}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}}$$

The total voltage isn't entirely put into the oxide; some of the voltage is put into the substrate (Si) which affects the total capacitance of the overall device, just as a MOS device should. The depletion region is a direct result of this. We use the high-frequency case for inversion because with the light off, none of the electrons are able to react to the AC voltage and flatlines past the threshold voltage, and also gives us the above equation for capacitance at that depletion capacitance.

We rearrange for C_{Si} and using $C_{ox} = C_{FB} = 24.2$pF and $C_{DEP} = C_{DEP-off} = 13.3$pF,

$$C_{Si} = \frac{1}{\frac{1}{C_{DEP}} + \frac{1}{C_{Ox}}} = \frac{1}{\frac{1}{13.3} + \frac{1}{24.2}} = 29.52\text{pF}$$

We know that at high-frequency, $C_{Si} = \epsilon_{Si}A/W_T$ and $W_T = \sqrt{\frac{2\epsilon_{Si}}{qN_Si}2\phi_F}$ (from section 12 lecture notes), and that from Chenming Hu chapter 5, $\phi_F = \frac{kT}{q}\ln\frac{N_Si}{n_i}$ (which is a condition for the threshold) where k is the Boltzmann

constant, $T = 300$K (room temperature), A is the area of the capacitor, and $n_i = 1 * 10^10$ which is intrinsic donor concentration of silicon. Using these equations and rearranging, we have

$$\frac{\epsilon_{Si} A}{C_{Si}} = \sqrt{\frac{2\epsilon_{Si}}{qN_A} \frac{kT}{q} \ln \frac{N_{Si}}{n_i}} \tag{27}$$

$$1.39265 * 10^{-11} = \sqrt{1.67 * 10^7 \frac{1}{N_S i} \ln \frac{N_S i}{n_i}} \tag{28}$$

Within the calculations above, we converted all of the pertinent values to SI units. We then solve numerically for N_{Si} using Mathematica, and obtain

$$N_{Si} = 1.246 * 10^{23} \text{m}^{-3} = 1.246 * 10^{17} \text{cm}^{-3} \tag{29}$$

Table 8: Device 4

C_{FB} [pF]	V_{FB} [V]	C_{DEP-on} [pF]	$C_{DEP-off}$ [pF]	V_T [V]	t_{ox} [nm]	N_{Si} [cm^{-3}]
24.2	-3.5	19.2	13.3	0.5	67.8	$1.245 * 10^{17}$

3.5 Diode

The turn on voltage was determined from the forward bias data (when the curve begins) and the breakdown voltage is taken from the reverse bias, where the voltage starts to go from negative to positive.

Table 9: Device 7

$V_{turn-on}$ [V]	$V_{breakdown}$ [V]
0.56	-25.6

3.6 Individual MOSFET

We follow the directions and extract from the graphs the I_{on} and I_{off}.

For the subthreshold swing, we know that SS is equal to the inverse of the slope of the log ID-VG curve in the subthreshold region, so for our case,

$$SS = \frac{1.7 - 1.5}{1.8 * 10^{-4} - 1.5 * 10^{-4}} = 0.66 * 10^4 \text{V/decade} \tag{30}$$

For device mobility, the "Square Law" model was used, as introduced in section 12 of our lecture notes,

$$I_{D,sat} = \frac{Z\mu C_{ox}}{2L}(V_G - V_T)^2 \tag{31}$$

which applies only when $V_D > V_{DS,sat}; V_G > V_T$. So, to calculate our area normalized C_{ox}, we have

$$C_{ox} = \frac{\epsilon_{Si}}{t_{ox}} = \frac{3.9 * 8.85 * 10^{-12}}{706 * 10^{10}} = 0.0489 * 10^{-2} \text{F/m}^2 \tag{32}$$

and then use that to calculate our carrier mobility using our above saturation current equation,

$$2.28 * 10^{-4} = \frac{2 * \mu * 0.0489 * 10^{-2}}{2 * 20}(5 - 0.889)^2 \tag{33}$$

we rearrange for μ and find

$$\mu = 0.0557 \text{m}^2/Vs \tag{34}$$

Table 10: Device 9c

I_{on} [μA]	I_{off} [nA]	I_{on}/I_{off}	SS [mV/dec]	V_T [V]	μ_{device} [cm^2/Vs]
5.68	1.96	$2.89 * 10^3$	$0.66 * 10^4$	0.889	$5.57 * 10^{-6}$

3.7 MOSFET Yield

To do these calculations, the above equations for 9c were plugged into fields for Microsoft Excel to automate the calculations and achieve the results below.

Table 11: 8d yield rate

8d Device #	I_{on} [μA]	I_{off} [nA]	I_{on}/I_{off} [A]	SS	V_T	$I_{D,sat}$	μ	Works?
1	30.4	2.02	15049.5	61.36	0.819	0.000459823	0.0717	y
2	28	0.79	35443.04	57.5	0.863	0.000413798	0.0659	y
3	1.6	1.12	1428.571	61	0.866	0.000232993	0.0371	y
4	$2.33 * 10^{-7}$	\$1.58*10ˆ{-3}	0.147	N/A	N/A	N/A	N/A	n
5	1.91	1.4	1364.286	159	0.827	0.00313264	0.049	y
6	$6.65 * 10^{-3}$	$5.96 * 10^{-1}$	11.15	N/A	N/A	N/A	N/A	n
7	2.74	1.17	2341.88	56.5	0.781	0.000307994	0.0471	y
8	31.1	1.12	27767.86	194	0.834	0.000465077	0.0731	y
9	35.3	0.543	65009.21	17.6	0.705	0.000497804	0.0833	y
10	31.7	0.688	46075.58	50.6	0.746	0.000497804	0.075	y
Mean	20.34375	1.106375	19449.12	82.195	0.805125	0.000406854	0.063	
Median	29.2	1.12	8695.693	59.25	0.823	0.00436811	0.069	
Std Dev	15.256	0.4657	23165.13	53.95	0.050498	$9.93 * 10^{-5}$	0.014	

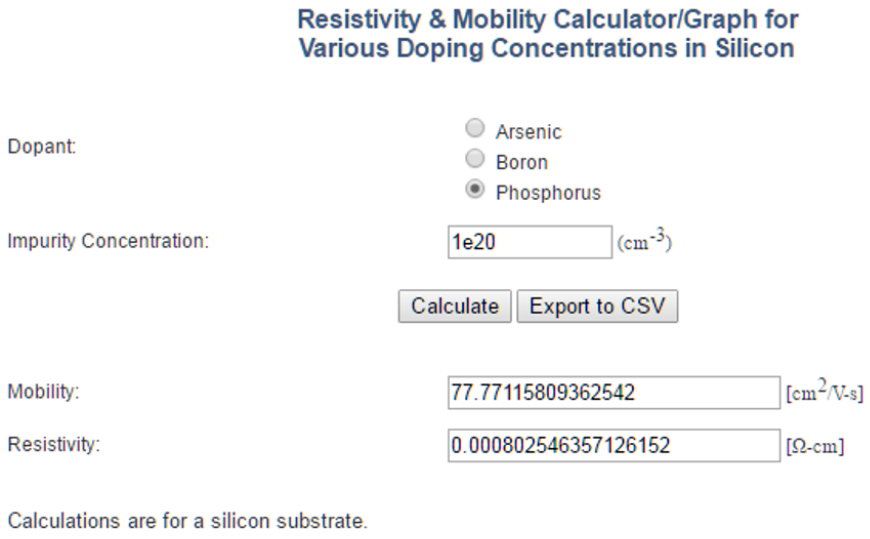
4 Theoretical Calculations

Table 12: From Lab 1

Parameter	Measured Value
Field t_{ox}	477.9 nm
Gate t_{ox}	70.6 nm
Intermediate t_{ox}	67.8 nm
x_j	1.3 μm
$x_{j-lateral}$	1.3 μm
$N_{surface}$	$1 * 10^{20}$ /cm^3
$N_{substrate}$	$1 * 10^{17}$ /cm^3

4.1 4-Point Resistors

2a



Ignore the effect of the doping concentration of Boron, just consider the effect of phosphorus which is $10^{20}/cm^3$.

We can get the resistivity is 8e-4ohm cm. X_j=1.3μm So R_s=resistivity/X_j=6.15ohm/Sq

2b

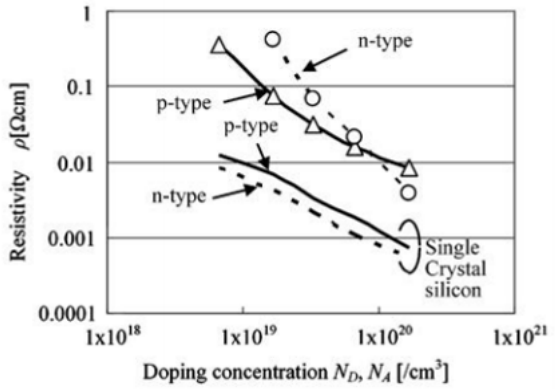


Fig. 4. Dependences of resistivities of fabricated p-type and n-type polysilicon resistors on doping concentration.

From Sensor and Material, Vol18, No.8(2006) 433-444, the resistivity of poly-Si is 10 times bigger than c-Si when they have the same doping concentration.

So the mobility of poly-Si is 7.77cm2/Vs. Resistivity=1/(q*mobility*doping concentration)=8.11e-3ohm cm R_s=resistivity/X_j=62.44ohm/Sq

4.2 Contact-Chain Resistors

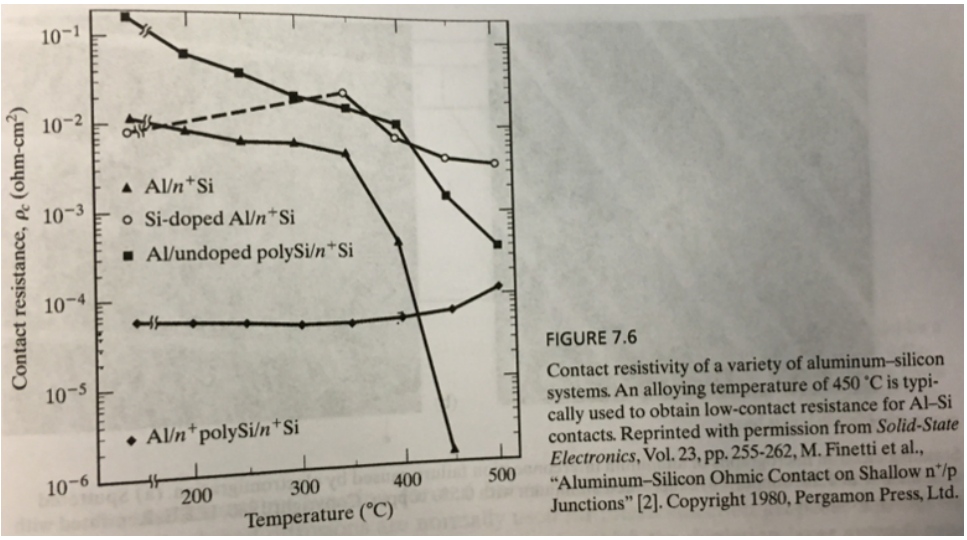


FIGURE 7.6
Contact resistivity of a variety of aluminum–silicon systems. An alloying temperature of 450 °C is typically used to obtain low-contact resistance for Al–Si contacts. Reprinted with permission from *Solid-State Electronics*, Vol. 23, pp. 255-262, M. Finetti et al., "Aluminum–Silicon Ohmic Contact on Shallow n$^+$/p Junctions" [2]. Copyright 1980, Pergamon Press, Ltd.

Figure 1: From p.157 Jaeger, at 400°C which is the sintering temperature in our lab.

For Al/n+ Si, contact mobility=4e-4ohm cm^2 For Al/n+ poly Si/n+ Si, conatct mobility=5.6e-5ohm cm^2

2c

For both 2c and 2d, A=W*L=2500μm^2 So for 2c, R$_c$=contact resistivity/A=16 ohm.

2d

For 2d, R$_c$ = contact resistivity/A = 2.24 ohm.

4.3 MOS Capacitors

We ignore the capacitance between the contact-Si and the field oxide which exists beside the device. But it is very small due to the large thickness. Also for the intermediate oxide, because there are too many electrons in the metal-like poly-Si with heavily n-type doped, so we can ignore the intermediate oxide capacitance.

$$V_{fb} = -\frac{[Eg + (Ev - Ef)]}{q}$$
$$V_b = 2kT\frac{ln(NA/ni)}{q}$$
$$p = N_v \exp(E_v - E_f)/kT$$
$$p = N_A = N_{back} = 1 * 10^{17}/cm^2$$
$$N_v = 1.04 * 10^{19}/cm^3$$
$$E_v - E_f = -0.12eV$$
$$n_i = 1 * 10^{10}/cm^3$$
$$V_{fb} = -(1.12 - 0.12) = -1.00V$$
$$V_b = 0.833V$$
$$A = 200\mu m * 200\mu m = 4 * 10^{-4}cm^2$$

We know that when $V < V_{fb}$ (under accumulation), we have $C_G = C_{ox}$

$$C_{ox} = C_{fb} = \frac{\epsilon_{ox}A}{t_{ox}} = \frac{3.9\epsilon_0 A}{t_{ox}} = 19.564pF$$

When $V_{fb} < V < V_b$ (under depletion), $C_G = C_{ox}C_s/(C_{ox} + C_s)$.

$$C_{ox} = 19.564pF$$
$$C_s = \epsilon_{Si}A/W$$
$$W = \sqrt{\frac{2\epsilon_{Si}V_s}{qN_A}}$$

where V_s is the surface potential. The voltage applied on the probe is not the actual potential at the surface of the device. It is a combination of potential drop in different material ($V = V_{fb} + V_{ox} + V_s$).

Together with

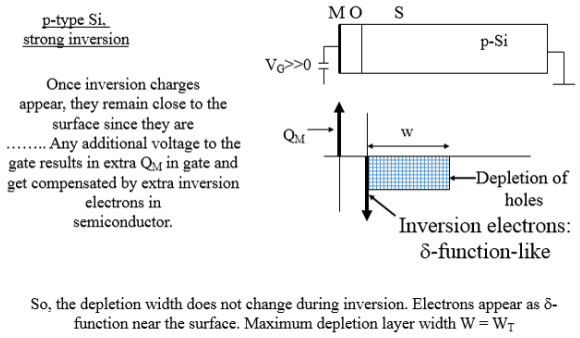
$$V_{ox} = \frac{Q}{U} = \frac{qN_AWA}{C_{ox}}$$
$$V_s = \frac{qN_AW^2}{2\epsilon_{Si}}$$

We can get $W = \epsilon_{Si}[\sqrt{\frac{A^2}{C_{ox}^2} + \frac{2(V-V_{fb})}{qN_A\epsilon_{Si}}}]$, and finally,

$$C_G = \frac{1}{\sqrt{\frac{1}{C_{ox}^2} + \frac{2(V-V_{fb})}{qN_A\epsilon SiA^2}}} = \frac{1 * 10^{-10}}{\sqrt{29.6467 + 3.52V}}F \tag{35}$$

When $V > V_b$ (under inversion), there are two cases:

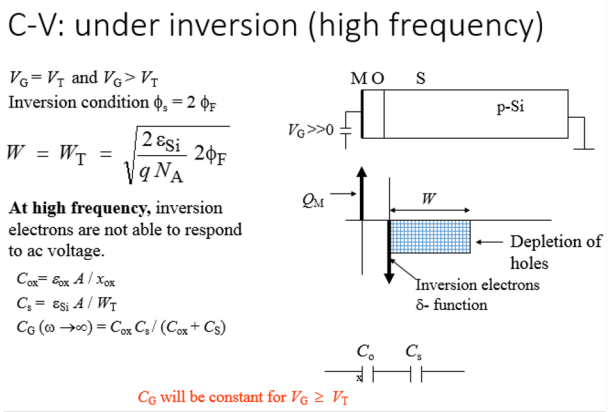
Charge Density - Inversion



So, the depletion width does not change during inversion. Electrons appear as δ-function near the surface. Maximum depletion layer width W = W_T

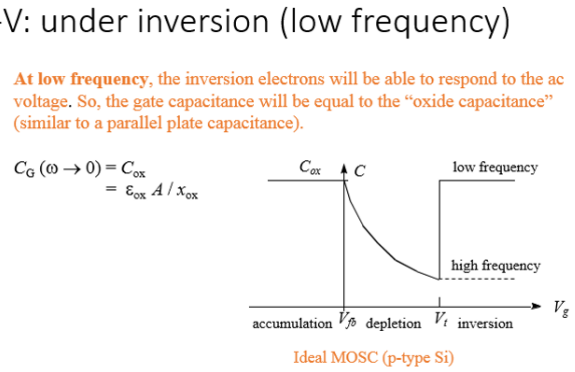
and, in the case of high frequency, the inversion electrons can't respond to the AC voltage.

C-V: under inversion (high frequency)

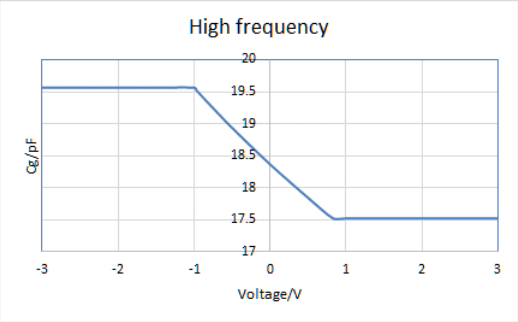


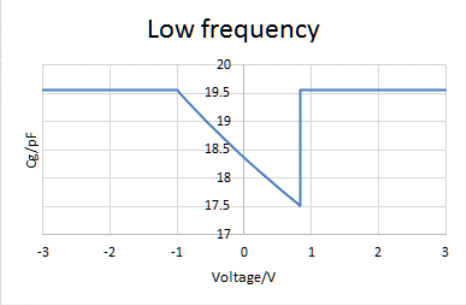
$$C_g = C_{dep} = C_g(V = V_t) = 17.52\text{pF} \tag{36}$$

When it is low frequency voltage, the inversion voltage will be able to respond to the ac voltage. So the gate capacitance will be equal to the oxide capacitance(similar to a parallel plate capacitance).



$$C_g = C_g(V = V_{fb}) = 19.564\text{pF} \tag{37}$$





If there is light, there will be some electrons and holes generated. So when $V > V_b$, even if the frequency of ac voltage is high, there will be some electrons respond to it, so C_g will become bigger when $V > V_b$. If there are enough electrons, C_g will recover to C_{ox} but actually there are not so many electrons to respond.

4.4 Diode

Using the doping concentration at the surface,

$$N_A = 1 * 10^{17}, N_D = 1 * 10^{20}\text{cm}^{-3}, T = 300\text{K} \tag{38}$$

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} = 1.012V \tag{39}$$

4.5 Individual MOSFET 9c

From lab report 1, consider a 1.5μm overetching for poly-Si in length. So L=18.5μm. But for the active region, from lab report 1, the overetching is about negative. So W=20.5μm

$$W/L = 20.5/18.5 = 1.11 \tag{40}$$

$$A = W * L = 3.7925e - 10\text{m}^2 \tag{41}$$

$$t_{ox} = 70.6nm \tag{42}$$

$$C_{ox} = \epsilon_{ox} A / t_{ox} = 4.756e - 14F \tag{43}$$

$$C_{ox}/A = 4.89e - 4F/m2 \tag{44}$$

$$V_t = 2kT \ln(N_A/n_i)/q = 0.833V \tag{45}$$

From instruction, V_{ds}=50mV. From Id-Vg curve and data, we choose V_g=5V I_d=7.56e-6A So the effective mobility is

$$L * I_d/(W * (C_{ox}/A) * (V_g - V_t) * V_{ds}) = 0.066835 m^2/Vs = 688.35 \text{cm}^2/Vs \quad (46)$$

5 Discussion

5.1 Table of Values

Table 13: Expected vs Measured

Device	Parameter	Theoretical	Measured/Extracted	% Error
2a	R_s	6.15 ohm/sq	302 ohm/sq	4810
2b	R_s	62.44 ohm/sq	649.285 ohm/sq	940
2c	$R_{single-contact}$	16 ohm	-144.36 ohm	-10000
2d	$R_{single-contact}$	2.24 ohm	-316.068 ohm	-14210
4	C_{FB}	$4.891 * 10^{-8}$ F/cm^2	$2 * 10^{-6}$ F/cm^2}	-59
	V_{FB}	-1.00 V	-3.5 V	250
	C_{Dep}	$4.38 * 10^{-8}$ F/cm^2	$3.3 * 10^{-8}$ F/cm^2	25
7	V_T	0.833 V	0.5 V	-40
	$V_{turn-on}$	1.012 V	0.56 V	-45
9c	C_{ox}	$4.89 * 10^{-4}$ F/m^2	$4.89 * 10^{-4}$ F/m^2	
	μ_{eff}	688.35 cm^2/Vs	557 cm^2/Vs	-19
	V_T	0.833 V	0.889 V	7

5.2 Device Deviations

2a

- Discrepancy - The measured resistance is much higher than theoretical one.
- Reason - There are some issue with our calculated surface doping concentration. Our calculated doping concentration is too high for 2a.
- Discrepancy - Width and length of the device line is smaller than projected.
- Reason - Slight overetching of the ACTV layer resulted in lines that are slightly smaller than projected.

2b

- Discrepancy - The measured resistance is much higher than theoretical one.
- Reason - The doping in poly-Si is different from c-Si. In our theoretical calculation, we assume the doping concentration in poly-Si is the same as the one in c-Si. But actually they are different. Also, we can see some scratch when measuring both 2a and 2b, these may cause some errors as well.

2d

- Discrepancy - Could not find a working device on our wafer.
- Reason - The poly contacts might not have penetrated deep enough into the polysilicon pads. The etch profile of the METL was odd, as the 2 micron line disappeared but all of the other lines were relatively untouched, and with our slight misalignments of the contacts, it could have resulted in our 2d devices having a minimum of one contact not connecting properly.

2c and 2d

- Discrepancy - The contact resistance are all negative.
- Reason - Both of them have the same issue with the Aluminum because we are not sure if the Aluminum is over etched to prevent a short circuit. If there is short between different contact, the contact resistance can be negative.

4

- Discrepancy - The measured C_{fb} and V_t is smaller than the theoretical one while the measured Cdep and V_{fb} is bigger than the theoretical one.
- Reason - For both the measured C_{fb}, C_{dep}, V_{fb} and V_t, we only read the data from the plot with our eyes. There is no clear cut-off point on the plot. So there must be some error when reading them. Also the field oxide will have some capacitance which affects the performance. In the lab, we also measured the capacitance of the interconnection which is very small (1.45 pF) to ignore the effect.
- Disrepancy - The flatband is not exactly a flatband.
- Reason - There is a delay in the accumulation in the accumulation region, possibly due to the electrons being too slow to react to the negative bias voltage, and as that voltage increases the electrons begin to react faster.

7

- Discrepancy - The measured Vturn-on is smaller than the theoretical one.
- Reason - We have an overestimation for the doping concentration of phosphorus so our theoretical is too big.

9c

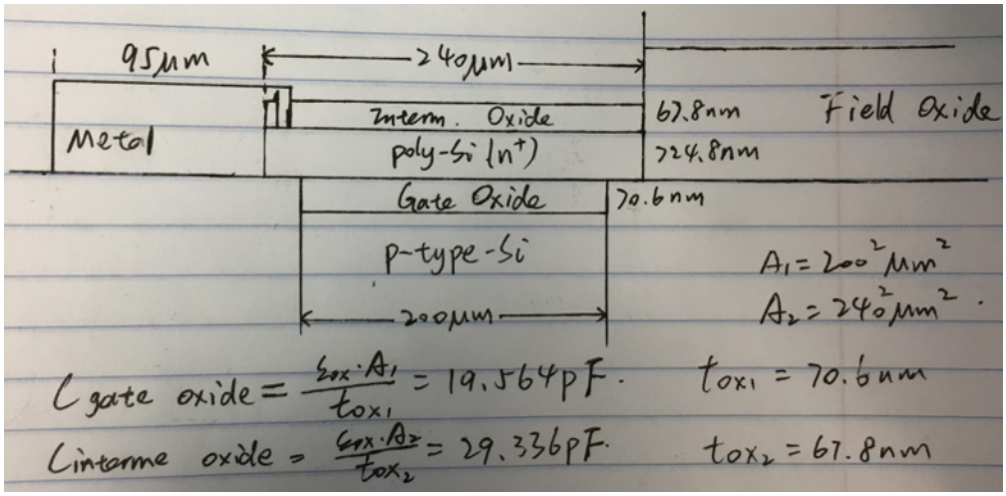
- Discrepancy - The effective mobility does not match and the measured Vt is a little bigger than the theoretical one.
- Reason - The formula we use to calculate the measured and theoretical mobility are different. They actually represent different cases For the measured Vt, the current we use is not 0 but the closet value we have for 0, the measured one is a little higher than the theoretical one. The measured calculation in section 3 used equation (30) (the Inverse Square Law), but for the theoretical measurement, we used $\mu_{eff} = \frac{L}{W}\frac{I_D}{C_{ox}(V_{GS}-V_t)V_{DS}}$ given by the lab instructions.

5.3 Yield Rate of 8d

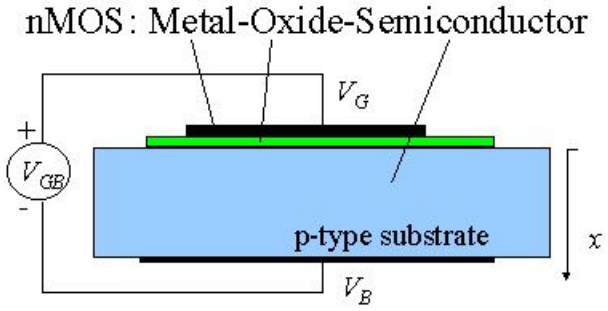
At lower potential values, a discrepancy exists because ID - VD technique is based on weak inversion current expression which is based on quasi-Fermi Dirac statistics, which may fail at low potentials. So ID - VD at low potentials yields wrong results at very weak inversion. The model takes into account only the surface states. (Muls Et. Al, 286)

6 Questions

6.1 Scale Drawing



6.2 MOS



MOS stands for Metal Oxide Semiconductor. the three regions are: Accumulation, Depletion and Inversion. For p-type substrate (i.e. nMOS): Accumulation occurs for negative voltages where the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Depletion occurs for positive voltages. The positive charge on the gate pushes the mobile holes into the substrate. Inversion occurs at voltages beyond the threshold voltage. In inversion, there exists a negatively charged inversion layer at the oxide-semiconductor interface in addition to the depletion-layer. This inversion layer is due to the minority carriers that are attracted to the interface by the positive gate voltage.

6.3 Intermediate Oxide

MOS capacitance includes two parts: Capacitance of dielectric and Capacitance of Silicon. The capacitance of Silicon cannot be constant with voltage increasing even in accumulation mode; it will be more obvious in thin oxide. The equivalent dielectric thickness from silicon occupies more percentage in the total equivalent dielectric thickness [$C_{tot} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{Si}}}$]. Poly-Si with heavily doped can be seen as a metal and the intermediate oxide capacitor can be seen as a parallel plate capacitor which does not change when applied a changing voltage.

6.4 Field Oxide

$C_{ox} = \frac{E_{ox}A}{t_{ox}}$ and $Q = C_{ox}V$. For field oxide, tox is very high. So very high potential difference will be required for carriers of the opposite type from the body aggregate at the surface (inversion).

6.5 Surface Mobility

The transport of carriers in the inversion layer is different from that in the bulk. Carriers in the channel region experience the irregularities at the Si/SiO interface. The resulting surface mobility is lower than the bulk mobility, since the carriers in the channel undergo surface roughness scattering in addition to the bulk scattering mechanisms.

6.6 4-Point Probe

The four point probe is preferable over a two-point probe because the contact and spreading resistances associated with the two point probe are large and the true resistivity can't be actually separated from the measured resistivity. In a four point probe, very little contact and spreading resistance is associated with the voltage probes and hence one can obtain a fairly accurate calculation of the resistivity. Using four probe eliminates measurement errors due to the probe resistance, the spreading resistance under each probe, and the contact resistance between each metal probe and semiconductor material.

6.7 8a Devices

Because the length of the device is too thin, after etching the poly-Si, the length will decrease below 4μm. When the contact area between poly-Si and oxide become smaller, it will be harder for the gate to attract enough electrons to make the device work.

6.8 Field Oxide MOSFET Performance

Its much thicker than the other oxide MOSFETs, thus affects gate control.So the $C_{field} = \frac{\epsilon ox}{t_{ox}}$ is much smaller than C_{gate}. So under the same voltage, there will be much fewer electrons be attracted which will affect the performance of the device.

7 References

- Advances in Electronics and Electron Physics Volume 47, Muls Et. Al p. 226
- Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, Chapter 5
- http://web.stanford.edu/class/ee410/TestStructures.pdf
- https://www.electrical4u.com/diode-working-principle-and-types-of-diode/
- http://www.radio-electronics.com/info/data/semicond/fet-field-effect-transistor/mosfet-basics-tutorial
  php
- http://www-inst.eecs.berkeley.edu/~ee40/fa03/lecture/lecture23.pdf
- http://www.iue.tuwien.ac.at/phd/entner/node33.html
- https://www.researchgate.net/figure/287158279_fig5_Figure-5-Graph-I-D-V-D-of-50nm-SOI-MOSFET
- http://www.sciencedirect.com/science/article/pii/S0026271402000276
- http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_s08/Homeworks/HW2_v1_sss.pdf
- http://www.microchemicals.com/uploads/pics/silicon_wafer_doping_concentration_resistivity_conductivity
  gif
- http://www.iue.tuwien.ac.at/phd/park/img264.png