Sai Sudarsan Chitrapu (Digital Design Engineer)

Ph. No.: (+91) 9000573582 | Email: sudarsan.chit@gmail.com| LinkedIn: linkedin.com/in/sudarsan-chit

Digital designer with experience in Low-power SoC and IP design, with an interest in allied fields of AI in semiconductor design and automation. Part of R&D team developing low-power/low-cost connectivity ICs (BLE and UWB) for automotive and industrial clients.

EXPERIENCE

DIGITAL DESIGN ENGINEER - TEXAS INSTRUMENTS (JUNE 2023 – PRESENT)

- Member of Low Power Connectivity HW R&D team, with design experience in sub-1 GHz and 2.4 GHz BLE SoCs
- SoC design experience includes Lint, CDC, and power intent specification (CPF/UPF) for heavily power-managed multi-power domain SoCs
- Owned power analysis, power optimization, power management (switches, level shifters, isolation, and retention) strategies, and LP verification for two products and 4 PGs
- IP design experience includes development and improvement of general-purpose timer and peripheral IPs (UART, I2C, and SPI) for 28nm family of devices
- Helped deploy an overlaid framework for peripheral IPs, which resulted in an area reduction of 30%

DIGITAL DESIGN INTERN - TEXAS INSTRUMENTS (AUGUST 2022 – JUNE 2023)

- Developed automation framework and flow for generating power intent of an MSIP in CPF and UPF formats.
- Reduced time required for SoC power intent bring-up by 85%.
  Skills: Common power format (CPF), Unified power format (UPF), Conformal low power, Python

IOT SUMMER INTERN – PLASTIC WATER LABS (MAY 2021 – JULY 2021)

- Designed a low-cost IoT-based automated irrigation system based on soil moisture content.
- Lead product development through ideation, product definition, prototyping, initial design, and testing phases. Led a group of 3 co-interns virtually, located in different cities.
- Achieved a reduction in water wastage by 25% and reduced labor costs for a 4-acre land.
  Skills: ESP32 development board, Interfacing sensors, GSM module

PUBLICATIONS

- "A performance-centric ML-based multi-application mapping technique for regular Network-on-Chip," Memories - Materials, Devices, Circuits and Systems,2023 - https://doi.org/10.1016/j.memori.2023.100059.
- "Power Intent Automation for Ultra Low Power Mixed-Signal SoC.". ET FE Track, Design Automation Conference 2023, San Francisco.

EDUCATION

- B.E. Electrical And Electronics (Minor In Robotics And Automation) 2019 – 2023
  (Birla Institute Of Technology And Science, Pilani)

COURSE/RESEARCH PROJECTS

Fault-Tolerant Multi-Application Mapping In Network on Chip(NoC) With Deep RL

- Worked on fault-tolerant multi-application mapping onto various NoC topologies using ML techniques.
- Worked towards optimizing the bandwidth requirements and energy efficiency of the applications.
- RL and GNN were used as the underlying ML models in the processes.
  Skills: Python, Pytorch

Dynamic Partial Reconfiguration of FPGA-Based Sensor Node

- Remote reconfiguration of an FPGA-based image processing sensor node using zynq-700
- Implemented a dynamically reconfigurable FPGA-based sensor node with three different reconfigurable image processing modules.
- Tested system with Sharp, Sobel, and Blur image processing convolutions.
  Skills: Verilog, Vivado, Vitis, C Programming, Zynq, AXI, UART

RISC V Pipelined Processor Implementation

- A 32-bit, 5-stage pipelined processor with Fetch, Decode, Execute, Memory, and Write-Back stages in Verilog.
- Implemented a forwarding and hazard-detection unit for resolving data, stall, and control hazards.
- The processor supports a few R-type, I-type, and B-type instructions from the RISC-V 32I ISA
  Skills: Verilog, Vivado

COURSES (AS PART OF B.E.)

Computer Architecture (RISC V and MIPS), Digital Design, FPGA System Design, Internet of Things, Microprocessors (x8086), AI for Robotics, ML

HOBBIES

Violin - Completed certificate course in Indian classical music. Gave about 15 regional and national performances.