

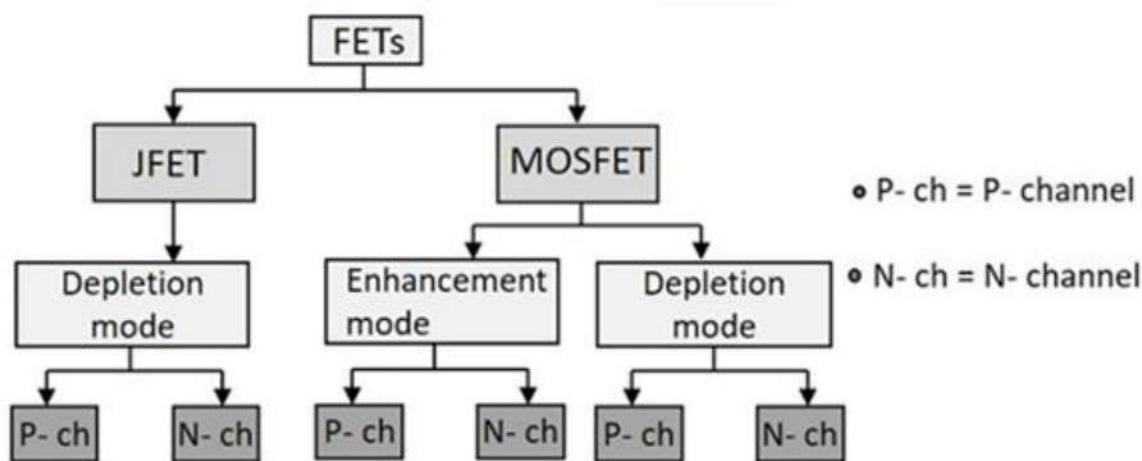
## UNIT-I

Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, pwell processes, BiCMOS, Comparison of bipolar and CMOS. Basic Electrical Properties of MOS And BiCMOS Circuits: Drain to source current versus voltage characteristics, threshold voltage, transconductance.

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### Types of FET

There are two main types of FETs. They are JFET and MOSFET. The following figure gives further classification of FETs.



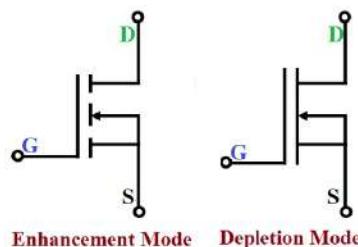
*Figure 1.1: Classification of Field Effect Transistor*

### Classification of MOSFET

The MOSFET is classified into two types based on the type of operations, namely **Enhancement mode MOSFET** (E-MOSFET) and **Depletion mode MOSFET** (D-MOSFET), these MOSFETs are further classified based on the material used for construction as n-channel and p-channel. So, in general, there are 4 different types of MOSFETs

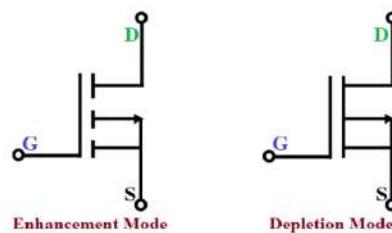
- N-Channel Depletion mode MOSFET
- P-Channel Depletion mode MOSFET
- N-Channel Enhancement mode MOSFET
- P-Channel Enhancement mode MOSFET

The N-channel MOSFETs are called **NMOS** and they are represented by the following symbols.



*Figure 1.2: Enhancement and Depletion Mode NMOS MOSFETs*

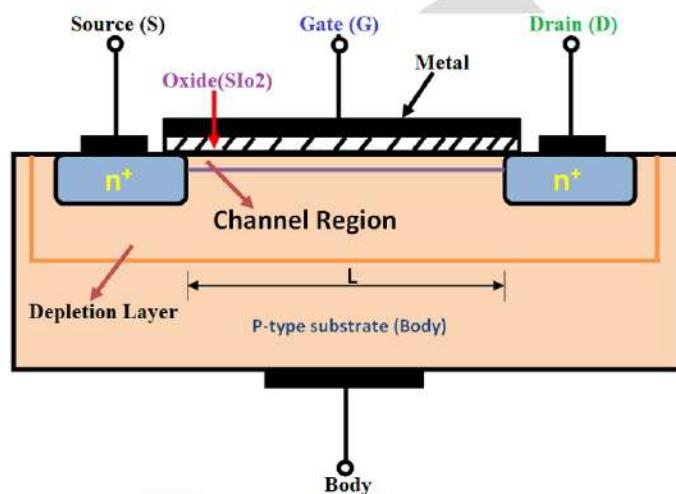
The P-Channel MOSFETs are called **PMOS** and they are represented by the following symbols.



*Figure 1.3: Enhancement and Depletion Mode PMOS MOSFETs*

### Construction Of MOSFET

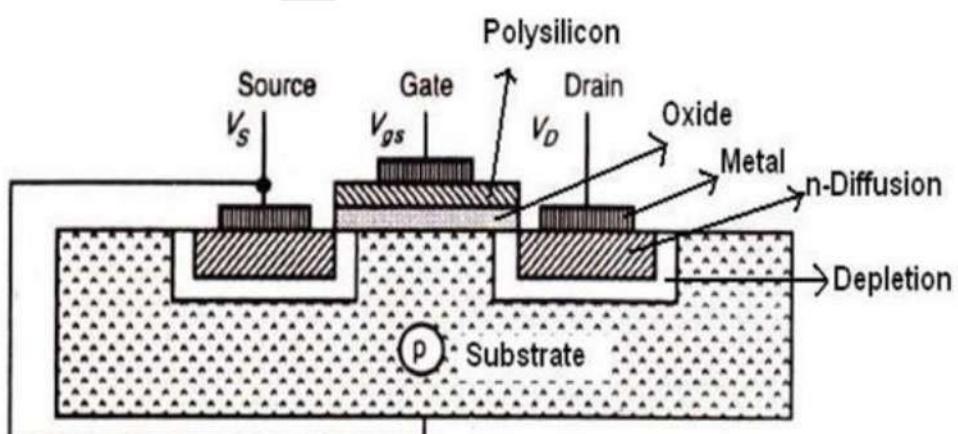
The MOSFET is an advanced form of FET and operates with the same three terminals as a FET the internal structure of the MOSFET is really different from the general FET.



*Figure 1.4: Block diagram of MOSFET*

The gate terminal is fixed on the thin metal layer which is insulated by a layer of Silicon Dioxide ( $\text{SiO}_2$ ) from the semiconductor, and two N-type semiconductors fixed in the channel region where the drain and source terminals are placed. The channel between the drain and source of the MOSFET is an N-type, opposite to this; the substrate is implemented as P-type. This helps in biasing MOSFET in both the polarities, either positive or negative. If the gate terminal of the MOSFET isn't biased, it will stay in the non-conductive state; hence the MOSFET is mostly used in designing switches and logic gates.

### Operation of MOSFET in Enhancement Mode:



*Figure 1.5: N Channel Enhancement Mode MOSFET*

The operation of MOSFET in Enhancement mode is similar to the operation of the open switch, it will start to conduct only if the positive voltage( $+V_{GS}$ ) is applied to the gate terminal and the drain current starts to flow through the device. The channel width and drain current will increase when the bias voltage increases. But if the applied bias voltage is zero or negative the transistor will remain in the OFF state itself.

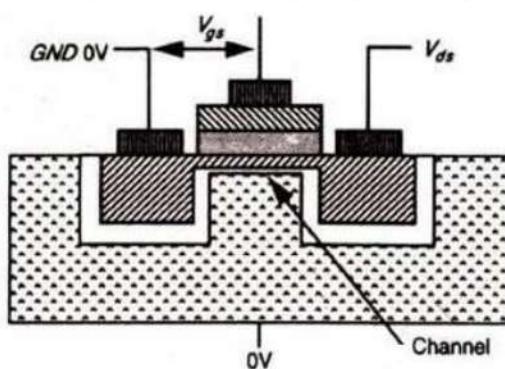
For an **enhancement-mode, n-channel MOSFET**, the four operational modes are:

❖ **Cut-off, sub threshold or weak-inversion mode:**

When  $V_{GS} < V_t$ , the transistor is turned off because two back to back diodes exits in series between D and S. These diodes prevent current conduction from D to S. So no current flows between D and S. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak- inversion current, sometimes called subthreshold leakage.

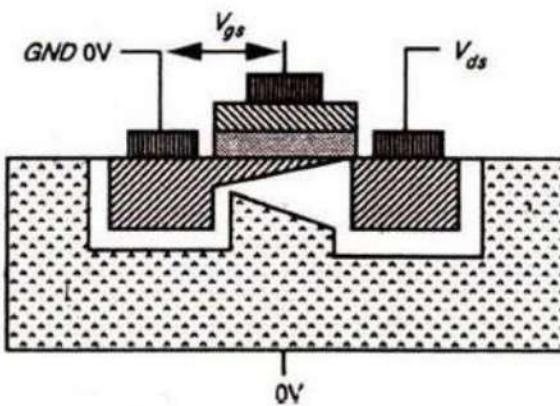
❖  **$V_{GS} > V_t$  and  $V_{DS} = 0$ :**

A small +ve  $V_{GS}$  is applied on the gate terminal. Due to  $V_{GS}$ , holes in the P type layer close to the silicon dioxide layer under the gate to be repelled down into the P type substrate, and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode bridging the gap between the heavily doped source and drain areas. This layer is called channel and also sometimes called an “inversion layer” because applying the gate voltage has caused the P type material immediately under the gate to firstly become “intrinsic” and then an N type layer within the P type substrate.



*Figure 1.6: N Channel Enhancement Mode MOSFET with  $V_{GS} > V_t$  and  $V_{DS} = 0$*

**Threshold voltage:** Establish channel between source and drain, a minimum voltage of threshold voltage  $V_t$  must be established between gate and source.

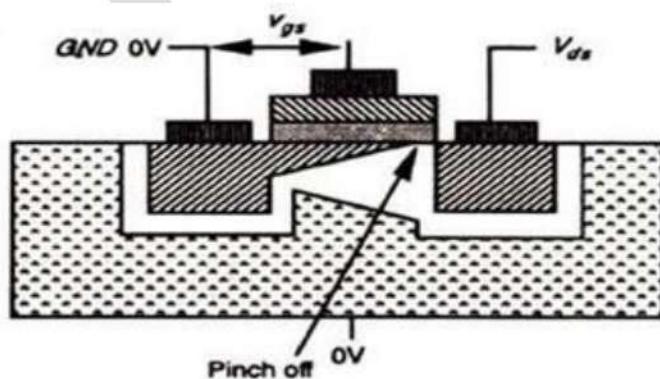


**Figure 1.7: N Channel Enhancement Mode MOSFET with  $V_{gs} > V_t$  and  $V_{ds}$  increases**

As  $V_{ds}$  is increased, then current flows in the channel. There must be a corresponding IR drop =  $V_{ds}$  along the channel. This develops a voltage between gate and channel varying with distance along the channel with the voltage being a maximum of  $V_{gs}$  at the source end. Due to this voltage variance across the channel, the channel is no longer uniform depth and its depth depends on the voltage across it. Therefore due to  $V_{ds}$ , the channel shape will be tapered. The channel being deepest at the source end and shallowest at the drain end.

Since the effective gate voltage is  $V_g = V_{gs} - V_t$  (no current flows when  $V_{gs} < V_t$ ), there will be voltage available to invert the channel at the drain end so long as  $V_{ds} \leq (V_{gs} - V_t)$ . The limiting condition comes when  $V_{ds} = V_{gs} - V_t$ . For all voltages  $V_{ds} < V_{gs} - V_t$ , the device operated in the non-saturated region.

**Saturation region when  $V_{gs} > V_t$  and  $V_{ds} > (V_{gs} - V_t)$ :** In this case, an IR drop equal to  $V_{gs} - V_t$  occurs over less than the whole length of the channel such that, near the drain, there is insufficient electric field available to give rise to an inversion layer to create the channel. The channel is, therefore, 'pinched off'. Diffusion current completes the path from source to drain in this case, causing the channel to exhibit a high resistance and behave as a constant current source. This region, known as saturation, is characterized by almost constant current for increase of  $V_{ds}$  above  $V_{ds} = V_{gs} - V_t$ .



**Figure 1.8: N Channel Enhancement Mode MOSFET with  $V_{gs} > V_t$  and  $V_{ds} > (V_{gs} - V_t)$ :**

**VI Characteristics:**

**VI characteristics of the enhancement-mode MOSFET** are drawn between the drain current ( $I_D$ ) and the drain-source voltage ( $V_{DS}$ ). The VI characteristics are partitioned into three different regions, namely ohmic, saturation, and cut-off regions. The cutoff region is the region where the MOSFET will be in the OFF state where the applied bias voltage is zero. When the bias voltage is applied, the MOSFET slowly moves towards conduction mode, and the slow increase in conductivity takes place in the ohmic region. Finally, the saturation region is where the positive voltage is applied constantly and the MOSFET will be staying in the conduction state.

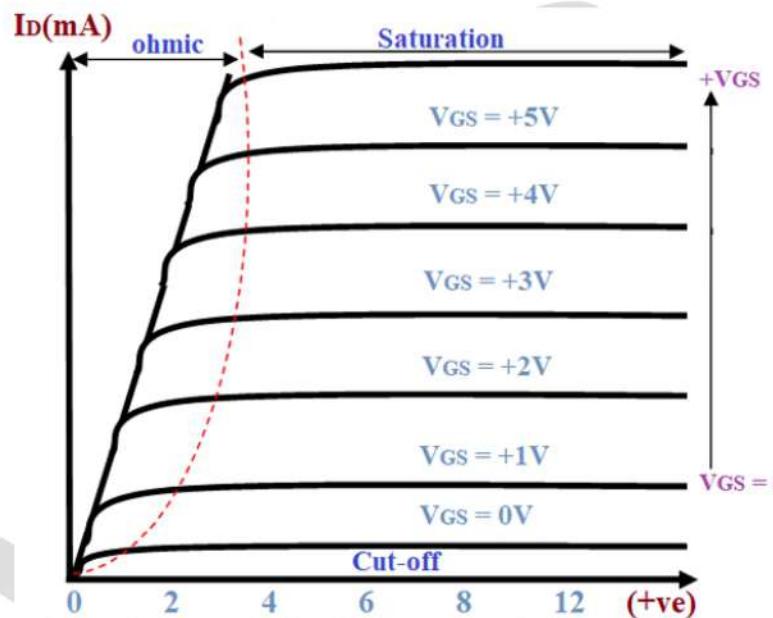


Figure 1.9: V-I Characteristics of N Channel Enhancement Mode MOSFET

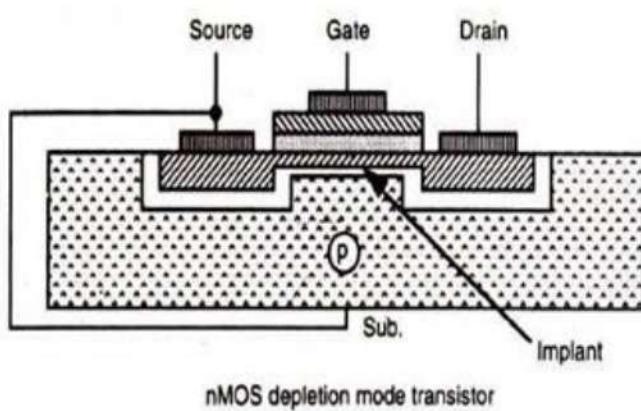
**N-CHANNEL DEPLETION MODE TRANSISTOR (DE-MOSFET):**

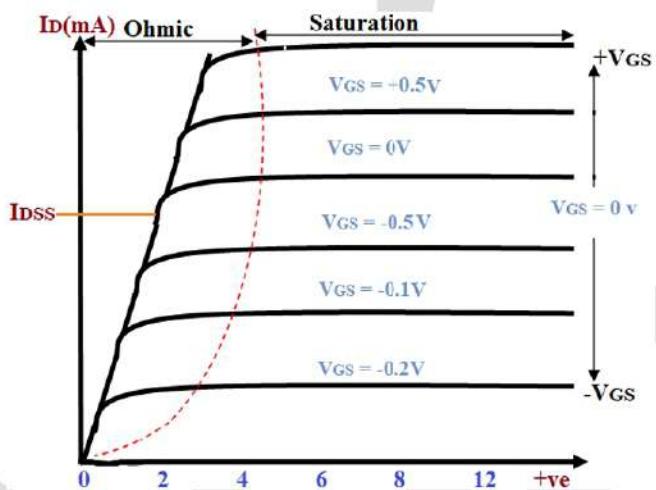
Figure 1.15: N Channel Depletion Mode MOSFET

The depletion-mode MOSFETs are usually called the “Switched ON” devices as they are generally in the closed state when there is no bias voltage at the gate terminal. When we increase the applied voltage to the gate in positive the channel width will be increased in depletion mode. This will increase the drain current

$I_D$  through the channel. If the applied gate voltage is highly negative, then the channel width will be less and the MOSFET might enter into the cutoff region.

**VI characteristics:**

The **V-I characteristics of the depletion-mode MOSFET** transistor are drawn between the drain-source voltage ( $V_{DS}$ ) and Drain current ( $I_D$ ). The small amount of voltage at the gate terminal will control the current flow through the channel. The channel formed between the drain and the source will act as a good conductor with zero bias voltage at the gate terminal. The channel width and drain current will increase if the positive voltage is applied to the gate whereas they will get decreased when we apply a negative voltage to the gate.



**Figure 1.10: V-I Characteristics of N Channel Depletion Mode MOSFET**

**EVOLUTION OF IC TECHNOLOGY**

It is based on the complexity of the circuit built on a single chip.

Year	Technology	No of transistors	Examples
1947-1950	Transistor	1	-
1951-1960	Discrete Component	1	FET, Diode
1961-1965	Small Scale Integration (SSI)	10	Logic Gates, Flip Flops
1966-1970	Medium Scale Integration (MSI)	100-1000	Counters, Multiplexers, Adders, Decoders

1970-1980	Large Scale Integration (LSI)	1000-20,000	RAM,ROM, 4-bit and 8-bit Micro-processors
1981-1990	Very Large Scale Integration (VLSI)	$20,000 - 10^6$	16 bit and 32 bit micro processors
1990-2000	Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$	Graphic Micro processor, Special processors, smart sensors
2000 onwards	Gaint Scale Integration (GSI)	$> 10^7$	Pentium Dual Core processor

**VLSI:** VLSI is the process of creating an Integrated Circuit (IC) by combining thousands of transistors into a single chip.

### Advantages of VLSI

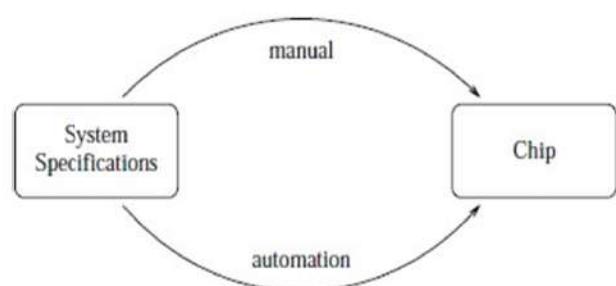
- Reduces the size of circuits
- Reduces cost of the devices
- Increasing operating speed of circuits
- Less power consumption
- High reliability
- Occupies less area

### Disadvantages of VLSI

- More expensive for high end products
- Heat dissipation
- May require a heat sink
- Low efficiency if input to output difference is large
- No advancements in fabrication

### Advantages of VLSI Design Style:

- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost



### MOORE's LAW

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles about every two years. Due to complexity in mounting, predicted cannot be reached.

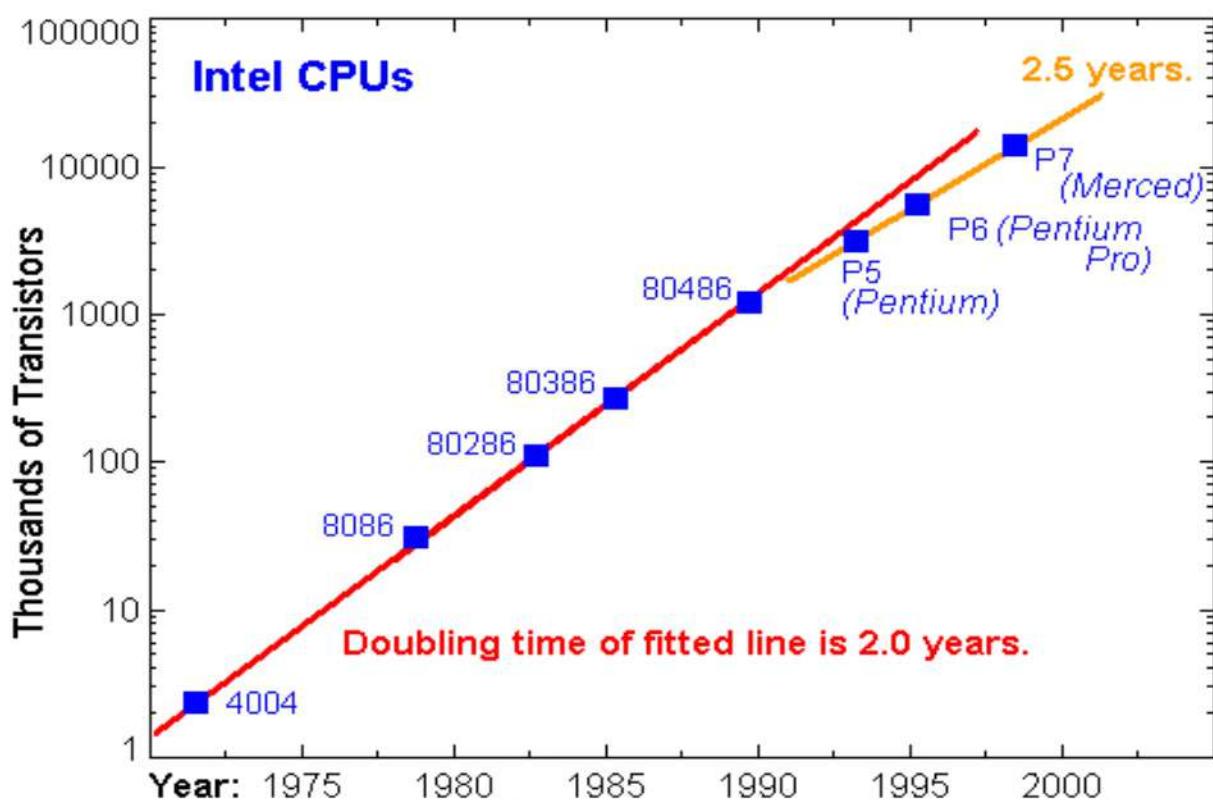


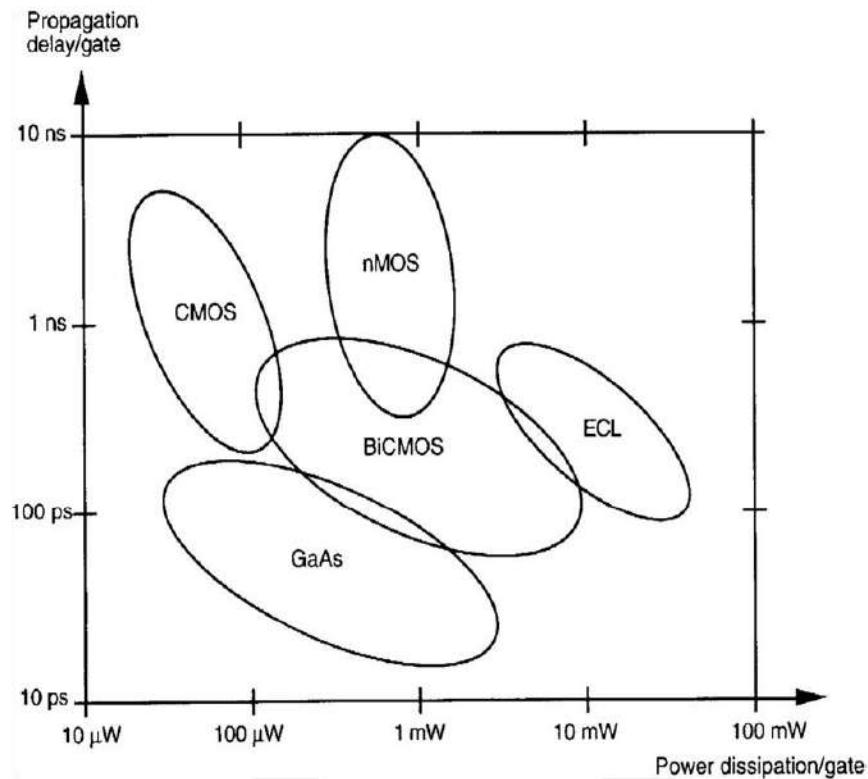
Figure 1.11: Evolution of IC Technology

### Speed Power Performance

IC technologies are classified depending on the “type of transistors” implemented on ICs and “type of wafer”

Wafer	Type of Transistor	IC Technology
Si	BJT(Bipolar Junction transistor)	BJT Technology
Si	MOS (Metal Oxide Semiconductor)	MOS Technology
	NMOS	NMOS Technology
	PMOS	PMOS Technology
	CMOS (both NMOS & PMOS)	CMOS Technology
	BiCMOS (BJT & CMOS)	BiCMOS Technology
	ECL (Emitter Coupled Logic)	ECL Technology

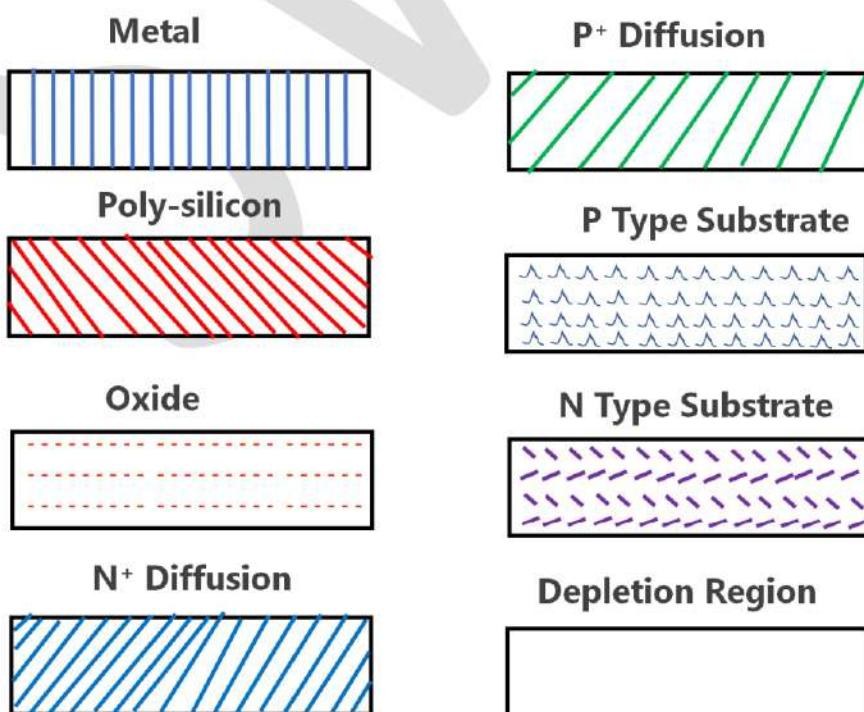
To know the best technology, we measure “Speed Power Product” in PJ(units). Propagation delay  $\times$  Power dissipation of a gate. Lowest SPP is the best technology.



*Figure 1.12: Comparison of Logic families*

- ❖ ECL-High power dissipation and Low delay
- ❖ NMOS- Moderate power dissipation and high delay
- ❖ CMOS- Low power dissipation and high delay
- ❖ BiCMOS-Moderate power dissipation and delay
- ❖ GaAs- Low power dissipation and low delay

#### MOS Transistor Symbolic representations



*Figure 1.13: MOS Transistor Symbolic representations*

**IC production process steps:**

Step1: Silicon Wafer Preparation

Step2: Oxidation

Step3: Masking and lithography

Step4: Etching

Step5: Doping

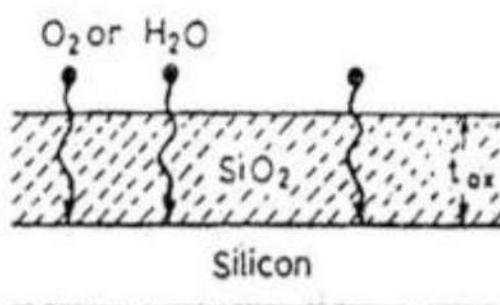
Step6: Metallization

Step7: Testing

Step8: Packaging

**OXIDATION**

- ❖ Oxidation is a process which converts silicon on the wafer into silicon dioxide.
- ❖ For an effective oxidation rate the wafer must be settled to a furnace with oxygen or water vapor at elevated temperatures.
- ❖ Silicon dioxide layers are used as high-quality insulators or masks for ion implantation.
- ❖ Formation of silicon dioxide layer on the surface of Si wafer
  - ❖ protects surface from contaminants
  - ❖ forms insulating layer between conductors
  - ❖ form barrier to dopants during diffusion or ion implantation
  - ❖ SiO<sub>2</sub> acts as the active gate electrode in MOS device structure.
  - ❖ It is used to isolate one device from another.
- ❖ Types of oxidation:
  - ❖ Dry Oxidation: Si reacts with O<sub>2</sub> to form SiO<sub>2</sub>
    - ❖ Si + O<sub>2</sub>-----> SiO<sub>2</sub> (Dry )
  - ❖ Wet Oxidation: Si reacts with water/steam to form SiO<sub>2</sub>
    - ❖ Si + 2H<sub>2</sub>O-----> SiO<sub>2</sub>+ 2H<sub>2</sub> (Wet )



*Figure 1.14: Oxidation Process*

## Lithography

The IC looks like a set of patterned layers. The layers are generally doped si, poly-silicon, metal and  $\text{SiO}_2$  soon. Generally a layer must be patterned (shaped) before the next layer of material is applied on the chip. The process used to patterning a layer is called lithography. Different lithographic techniques are available which are **photolithography**, **Electron lithography**, **X-ray lithography** and **Ion lithography**.

**Photolithography process:** First step in photolithography is to coat the surface with approx 1  $\mu\text{m}$  of photoresist (PR). Photoresist is an organic polymer i.e sensitive to light radiation in a certain wavelength range. The sensitivity causes either an increase or decrease in solubility of the polymer to certain chemicals. The photoresist is then exposed to UV (ultraviolet) radiation through a mask. The masks generated from information about device placement and connection. The UV radiation causes a chemical change in the PR. The PR is then developed using a chemical developer.

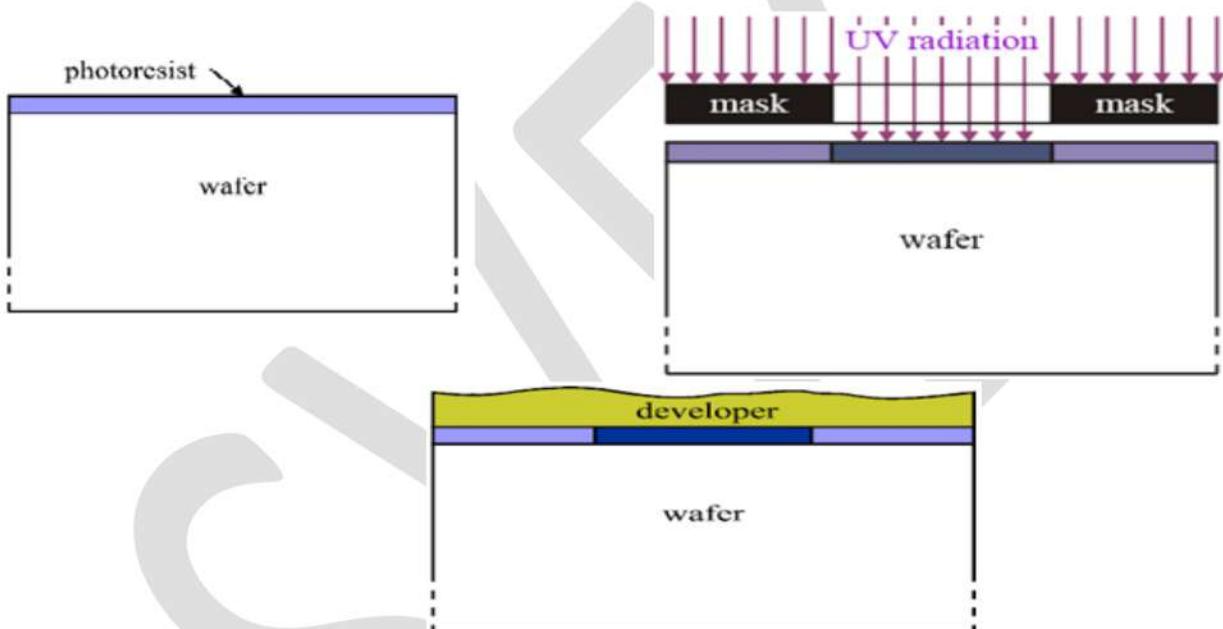


Figure 1.14: Lithography Process

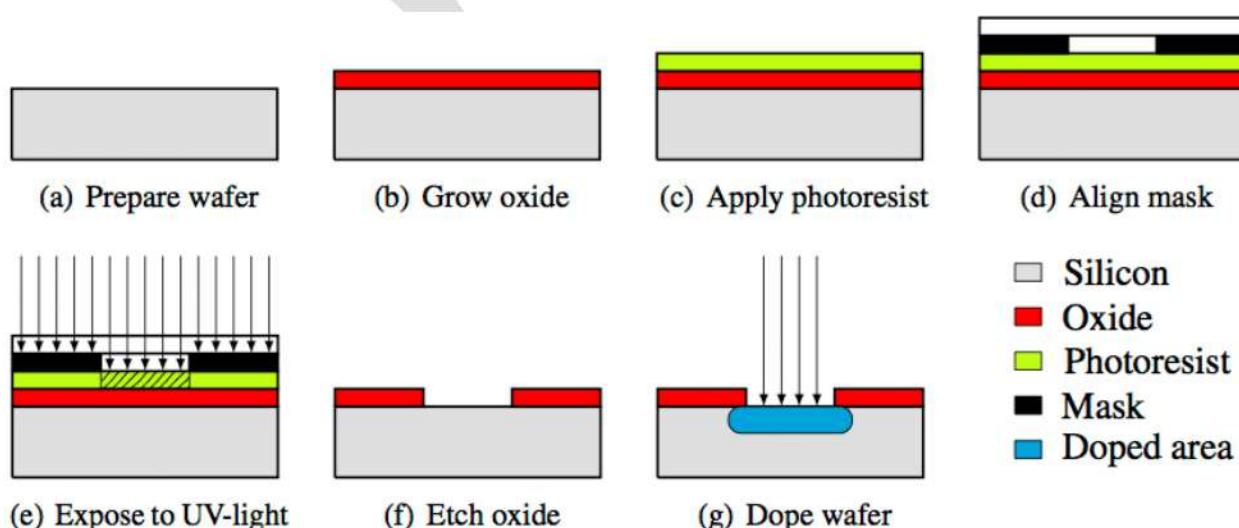
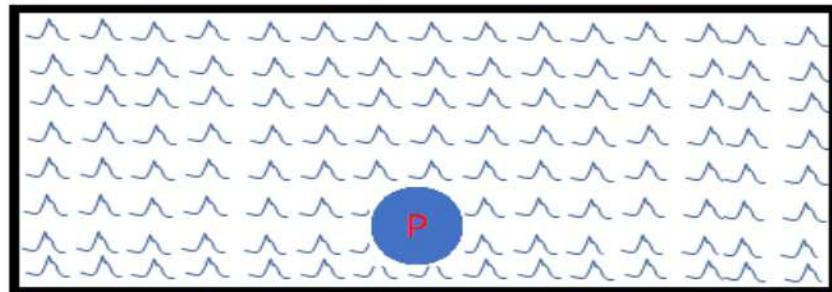


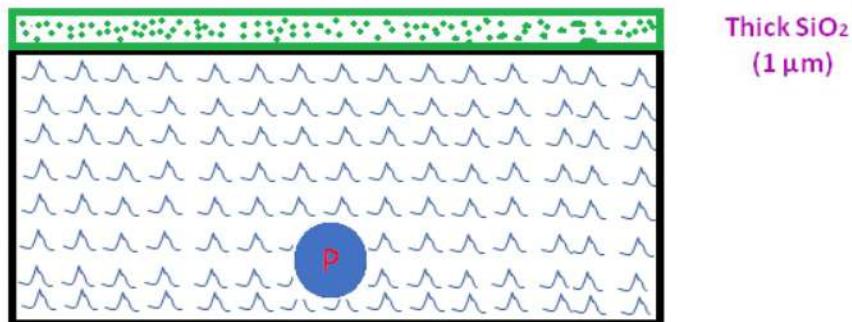
Figure 1.15: Lithography Process of Oxide

**NMOS Fabrication Steps:**

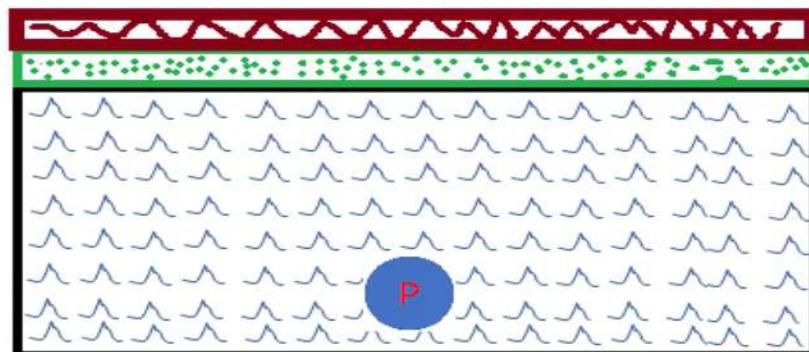
**STEP 1:** Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown. Such wafers are typically 75 to 150 mm in diameter and 0.4 mm thick and are doped with, say, boron to impurity concentrations of  $10^{15}/\text{cm}^3$  to  $10^{16}/\text{cm}^3$ .



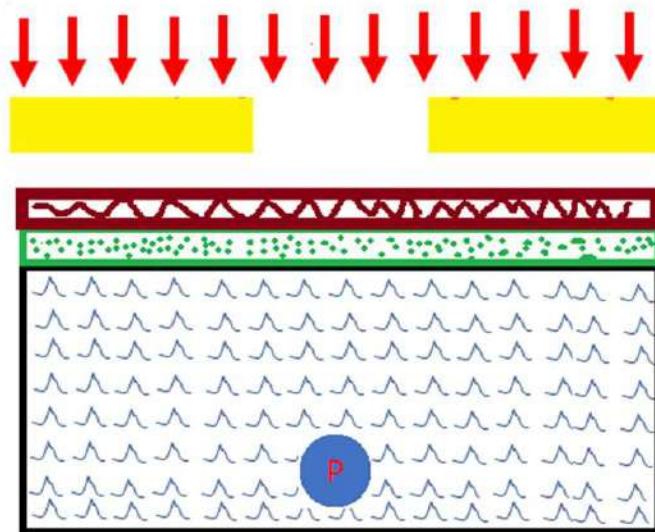
**STEP 2:** A Layer of  $\text{SiO}_2$ , typically of 1  $\mu\text{m}$  thickness all over the wafer surface to protect the surface. This oxide layer will act as a barrier to doping during subsequent processing and provide an insulating layer on which other patterned layers can be formed.



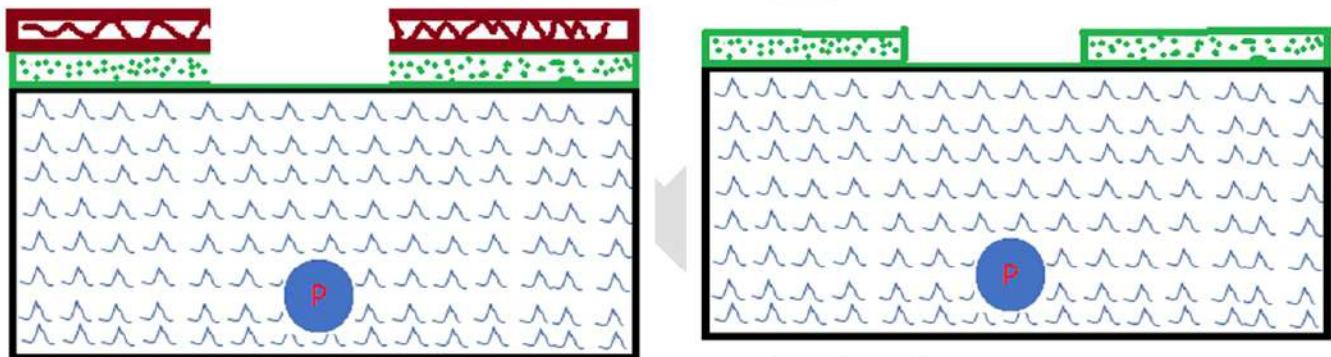
**STEP 3:** The surface is now covered with a photo-resist which is deposited onto the wafer and to achieve an even distribution of the required thickness.



**STEP 4:** The photo-resist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels. Assume, for example, that those areas exposed to ultraviolet radiation are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.

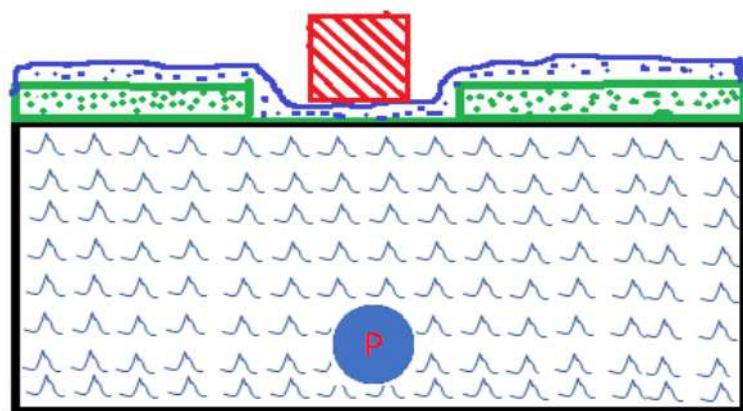


**STEP 5:** These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.



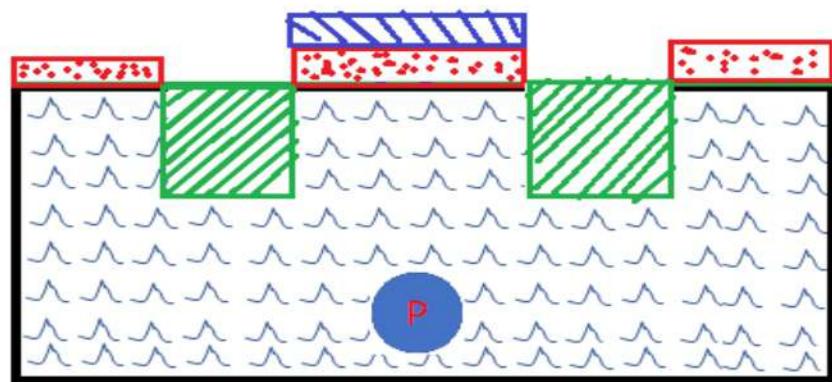
**STEP 6:** The remaining photo-resist is removed and a thin layer of  $\text{SiO}_2$  ( $0.1 \mu\text{m}$ ) is grown over the entire chip surface and the poly-silicon is deposited on top of this to form the gate structure.

Uses of poly-silicon: Used as gate electrode material and interconnection medium in silicon ICs.

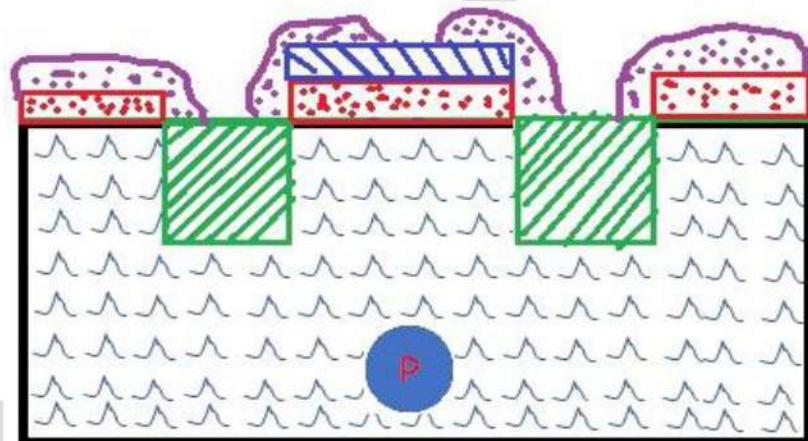


**STEP 7:** Thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity.

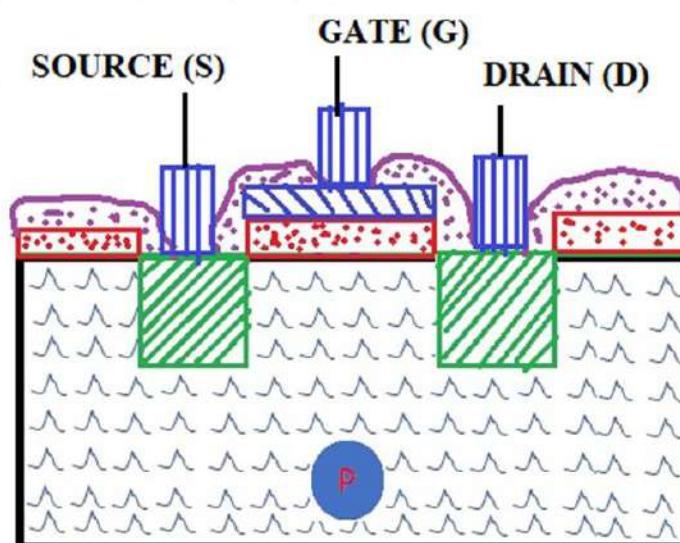
Forming the gate before source and drain regions process is referred as self aligned.



**STEP 8:** Once the source and drain regions are completed the entire surface is again covered with an insulating layer of  $\text{SiO}_2$ . Then  $\text{SiO}_2$  layer is patterned lithography techniques to provide contacts for source, drain and gate.

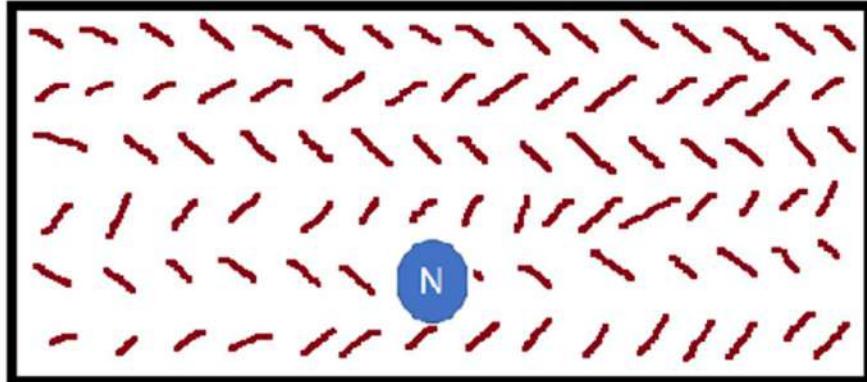


**STEP 9:** The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of  $1\mu\text{m}$ . This metal layer is then masked and etched to form the required interconnection pattern.

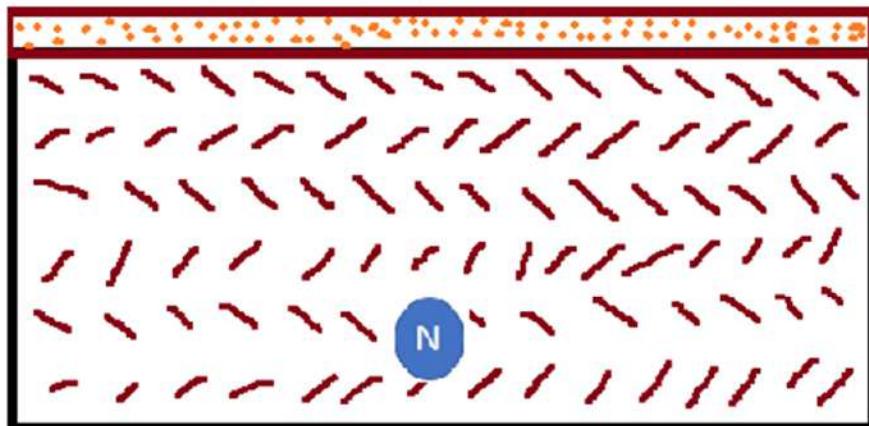


**PMOS Fabrication Steps:**

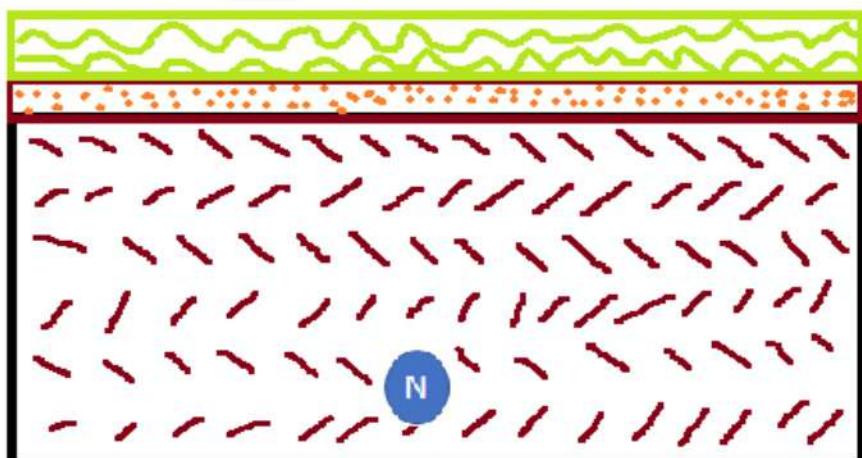
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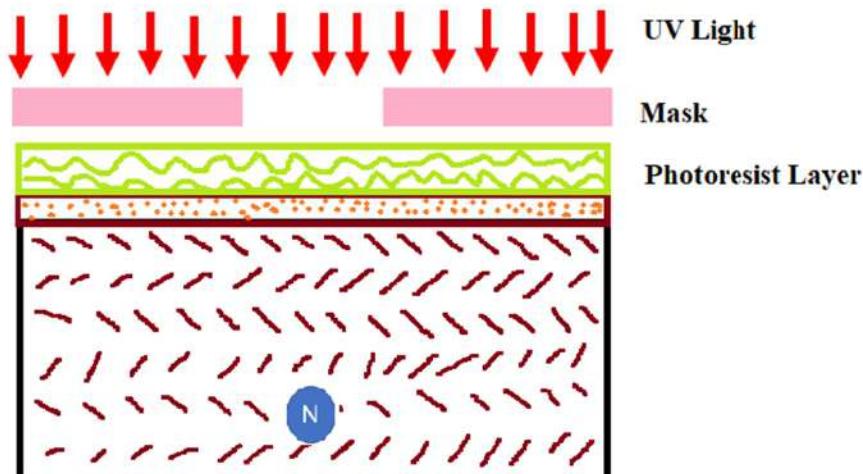
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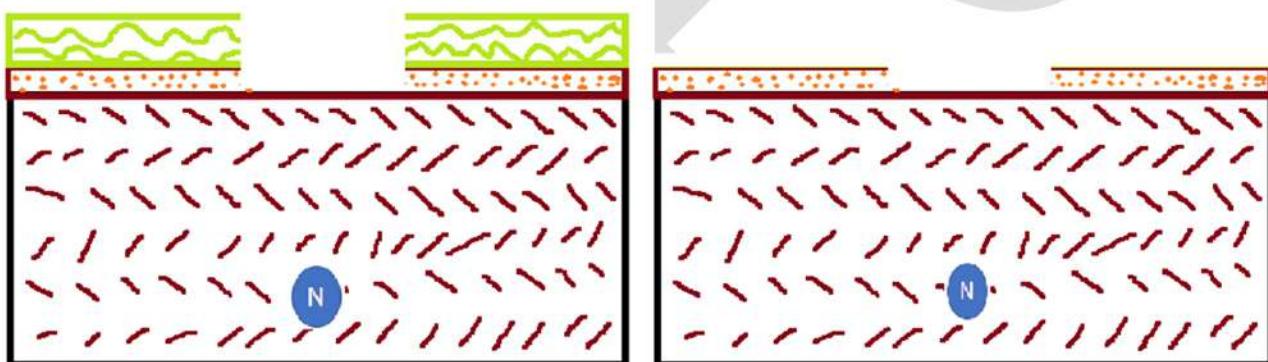
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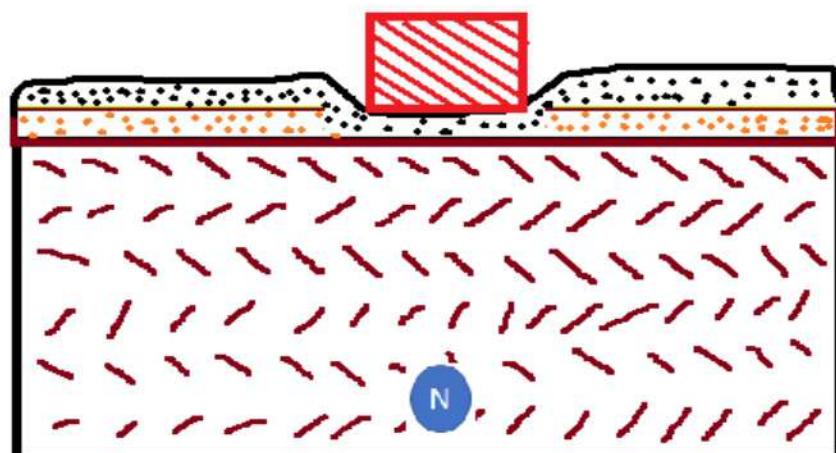


**STEP 5:** These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.

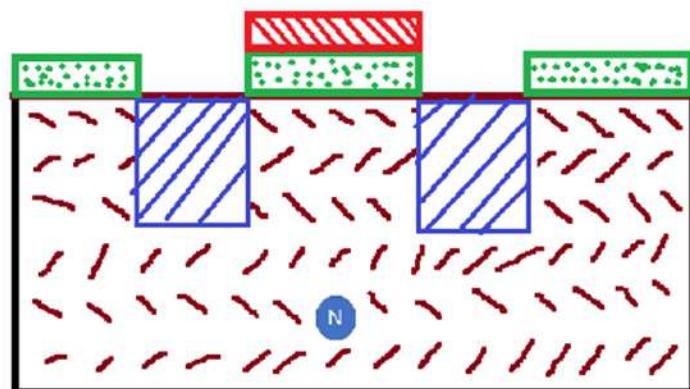


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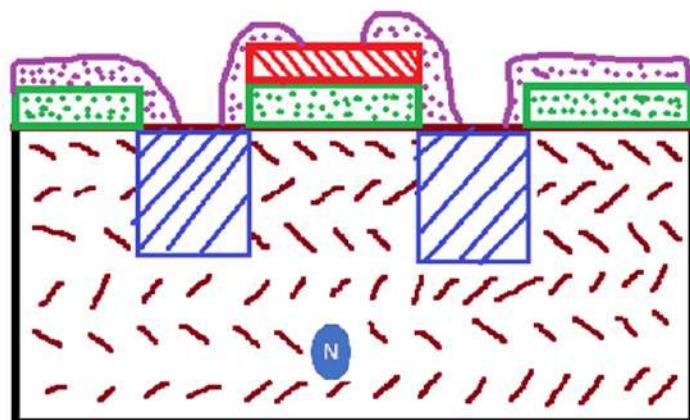
Uses of poly-silicon: Used as gate electrode material and interconnection medium in silicon ICs.



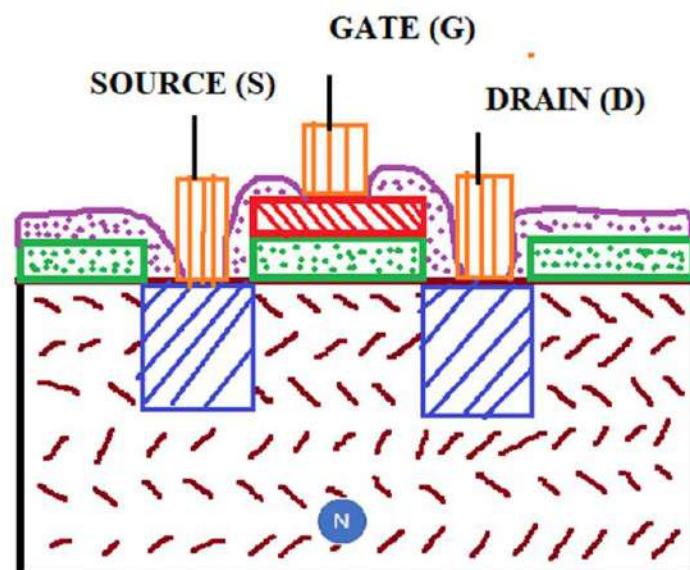
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**CMOS Fabrication**

CMOS can be obtained by integrating both NMOS and PMOS transistors on the same chip substrate. For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs required in which semiconductor type and substrate types are opposite to each other. For less power dissipation requirement CMOS technology is used for implementing transistors. If we require a faster circuit then transistors are implemented over IC using BJT.

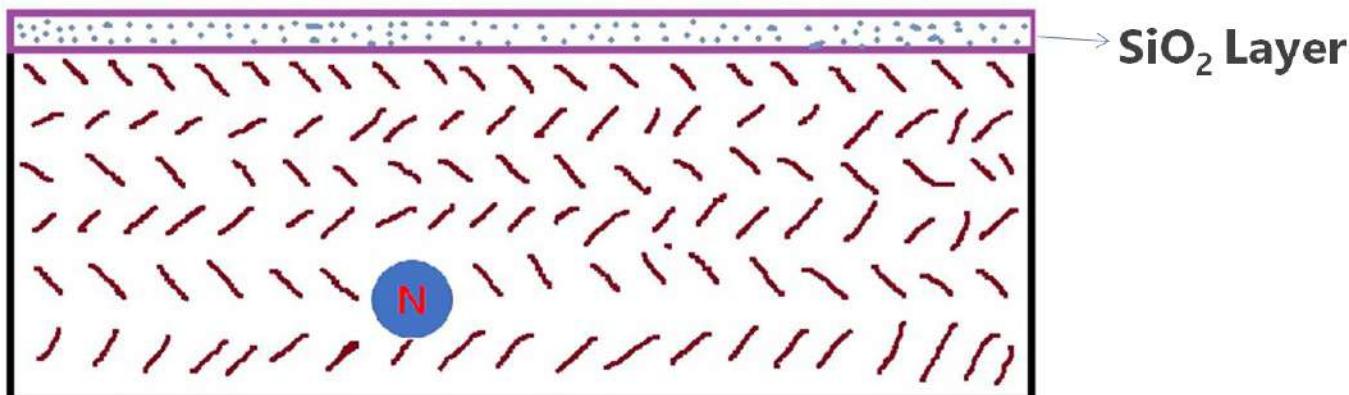
The CMOS can be fabricated using different processes such as

- ❖ The N well/ P well technology, where n-type diffusion is done over a p-type substrate or p-type diffusion is done over n-type substrate respectively.
- ❖ The twin tub technology, where NMOS and PMOS transistors are developed over the wafer by simultaneous diffusion over an epitaxial growth base, rather than substrate.
- ❖ The silicon insulator process, where rather than using silicon as the substrate an insulator material is used to improve speed and latch up susceptibility.

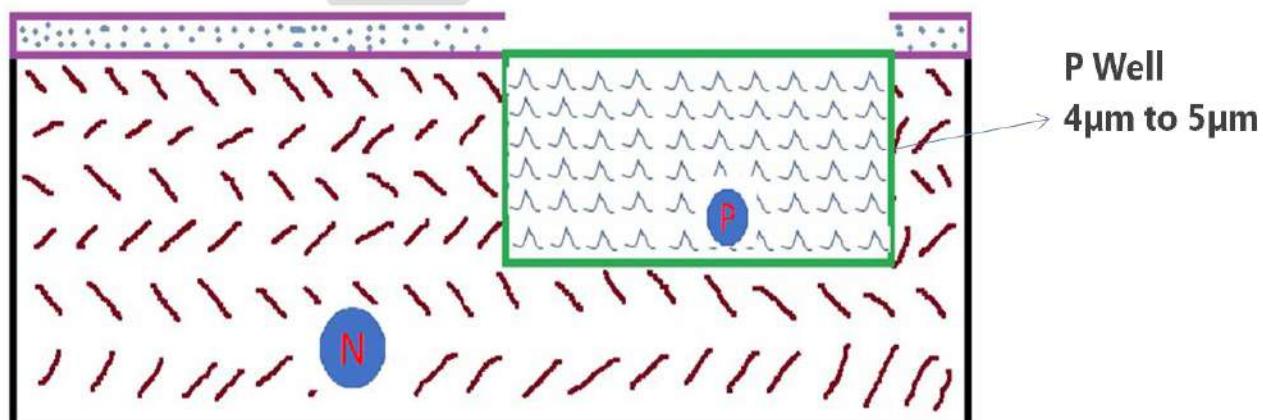
The P-well has to be created on a n-substrate or N-well has to be created on a p-substrate. The fabrication of CMOS is described using the p-substrate, in which the NMOS transistor is fabricated on a p-type substrate and the PMOS transistor is fabricated in N-well.

**CMOS Fabrication using P-well Process**

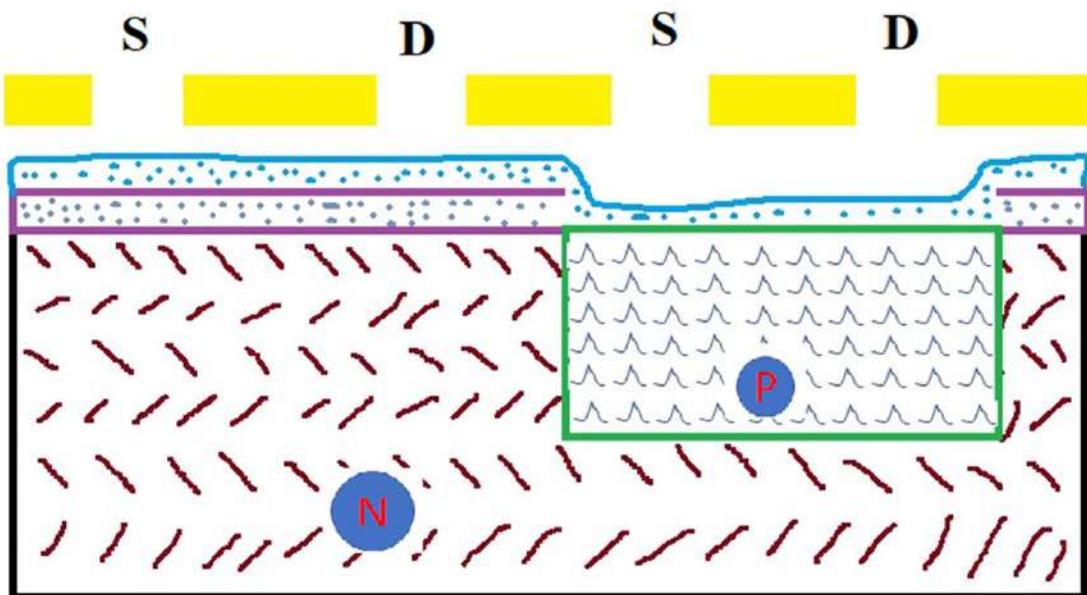
**STEP 1:** This process starts with a n-type silicon substrate with oxide layer grown on the entire surface.



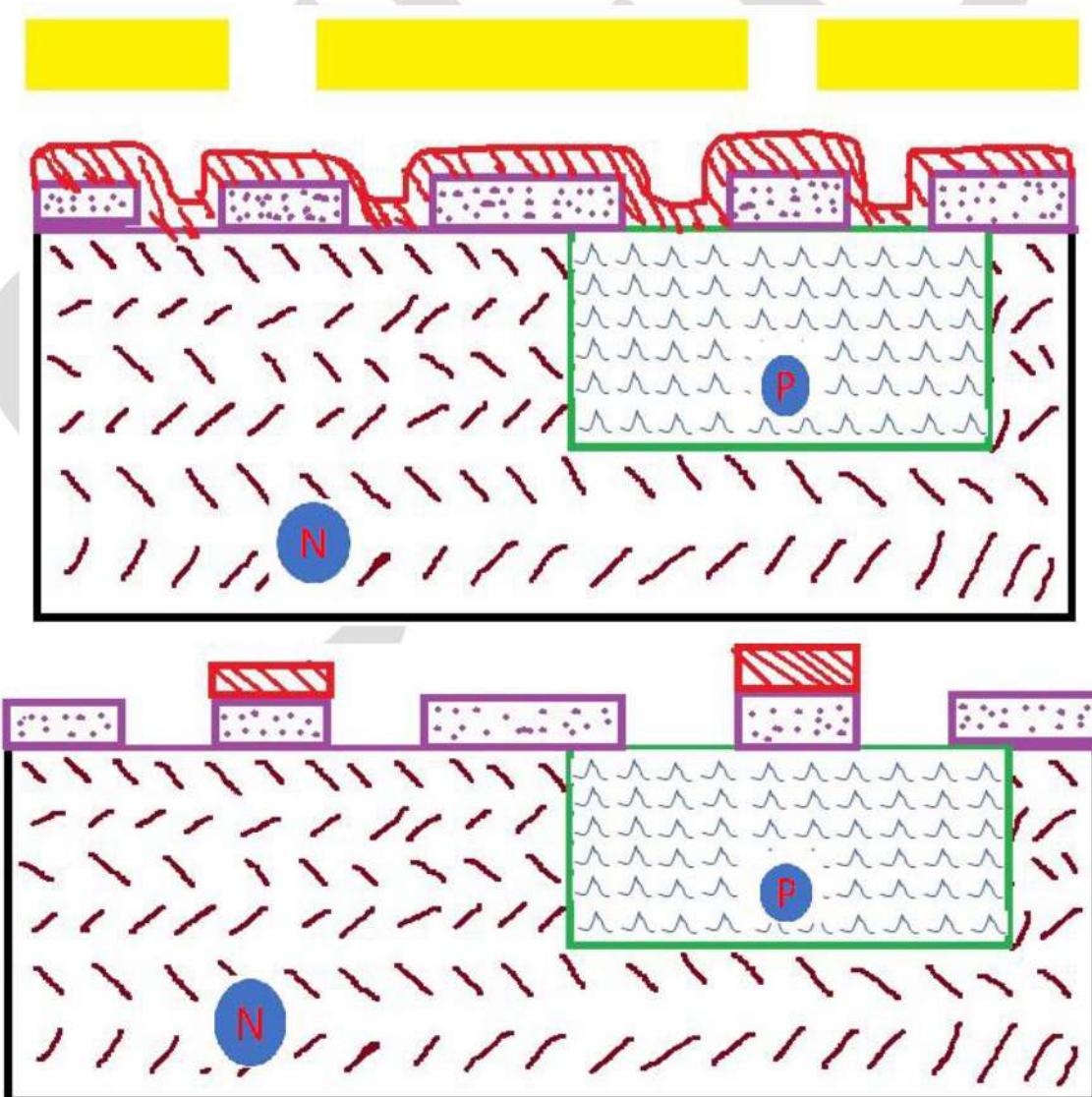
**STEP 2:** Define areas in which the deep P-well diffusions are to take place.



**STEP 3:** Masks for source and drain for both NMOS and PMOS transistors.



**STEP 4:** Formation of Poly-silicon layer using lithography technique



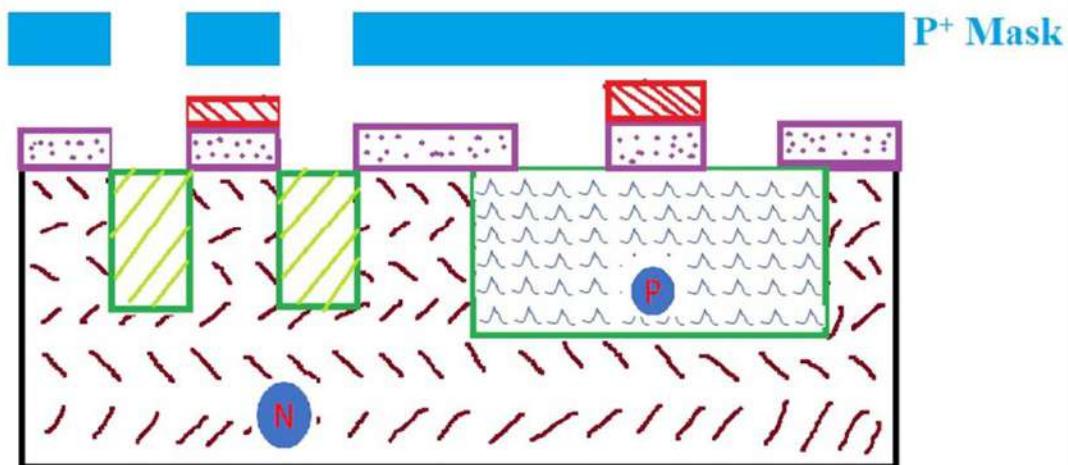
**STEP 5:** Defines where p diffusion is needed.

P<sup>+</sup> mask (+ve)---> Masked area not effected for p diffusion

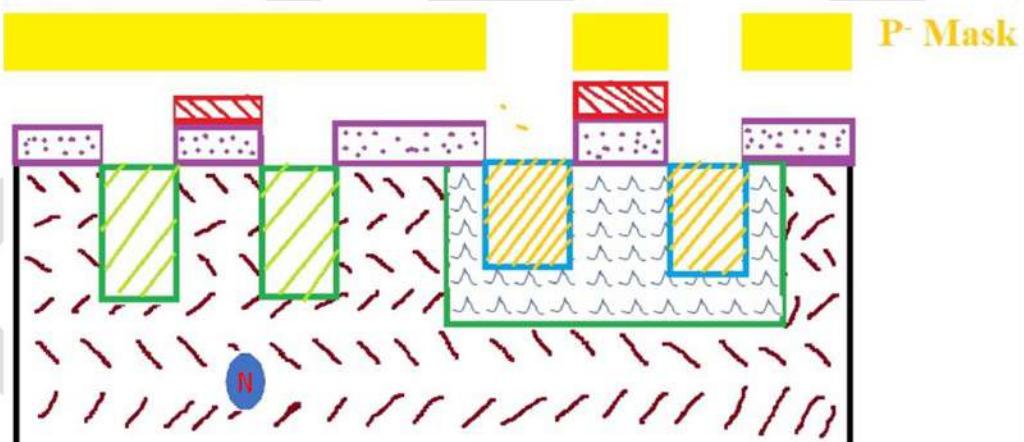
P<sup>+</sup> mask (-ve)---> Masked area not effected for n diffusion

N<sup>+</sup> mask (+ve)---> Masked area not effected for n diffusion

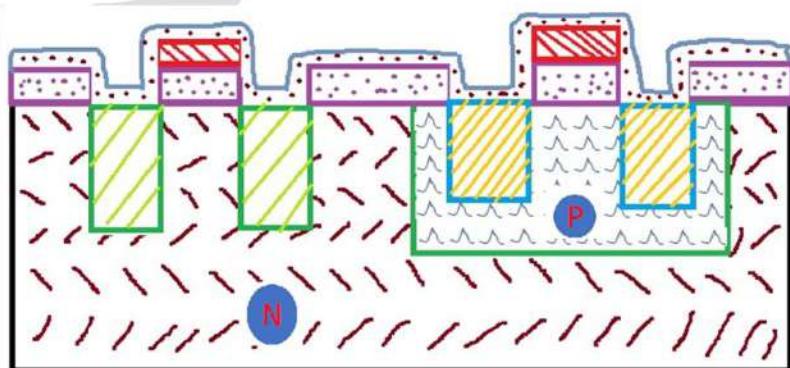
N<sup>+</sup> mask -ve)---> Masked area not effected for p diffusion



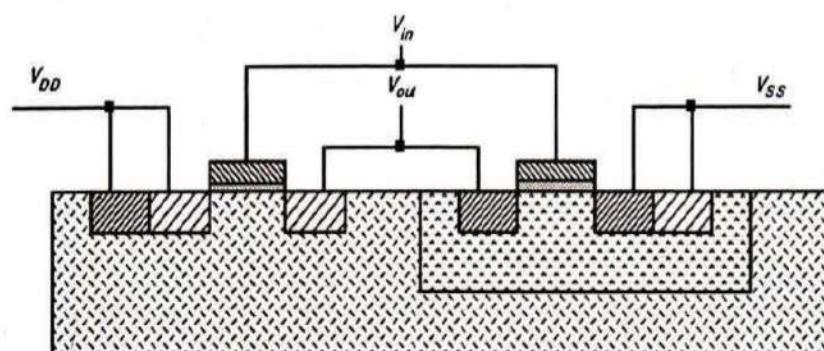
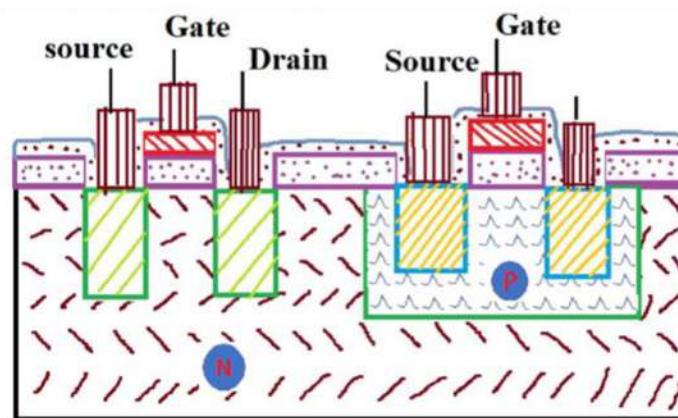
**STEP 6:** Defines where n diffusion is needed.



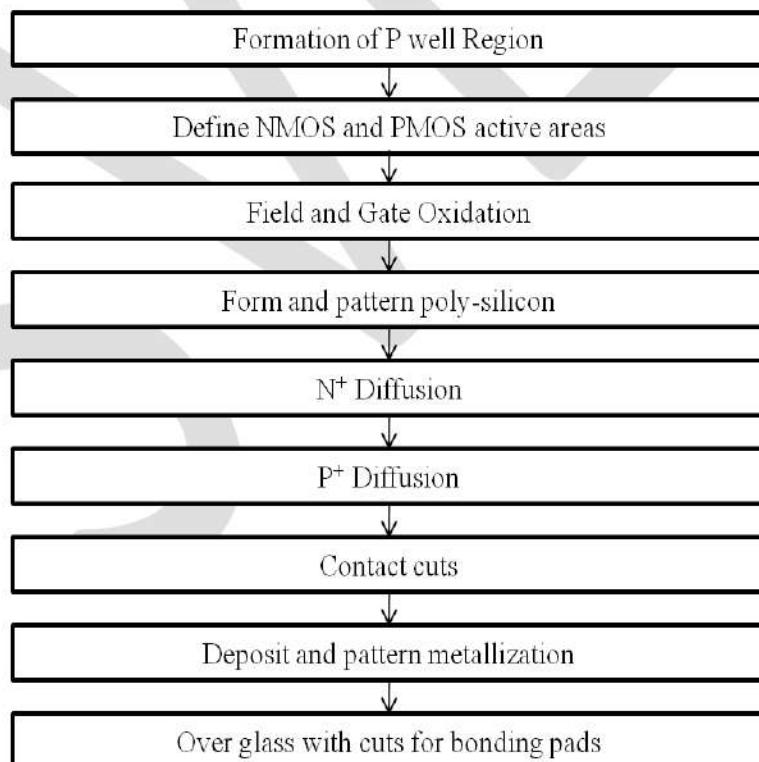
**STEP 7:** Before forming the metal terminals a thin SiO<sub>2</sub> is laid out to form a protective layer for the regions of the wafer where no terminals are required.



**STEP 8:** This step is used for the formation of metal terminals which can provide interconnections.

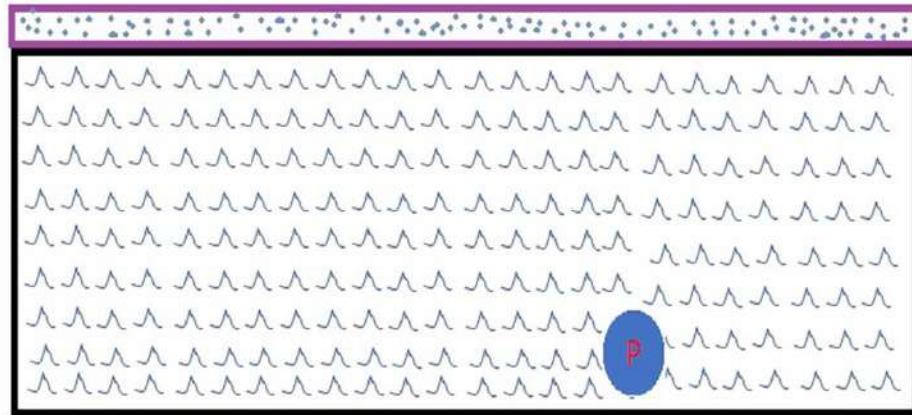


#### Main steps in a typical P-well Process:

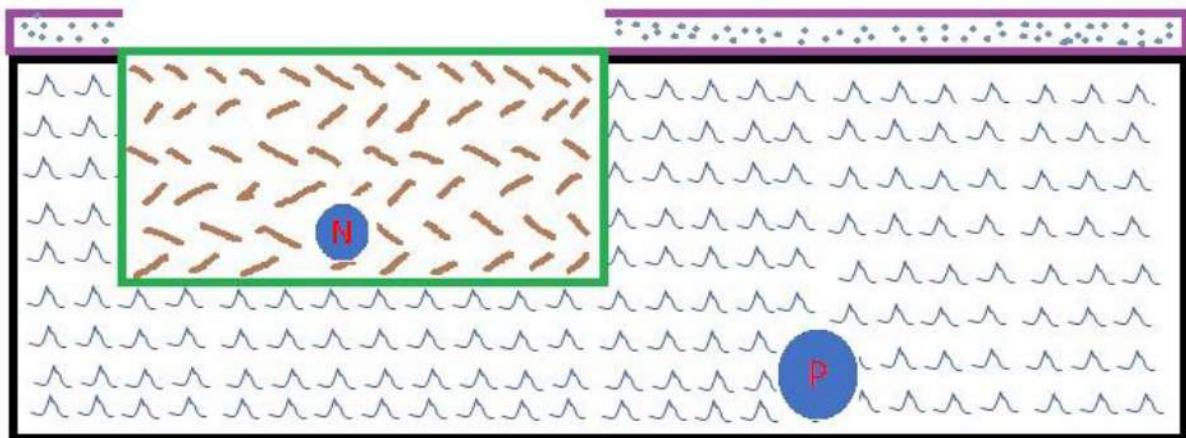


**CMOS Fabrication using N-well Process**

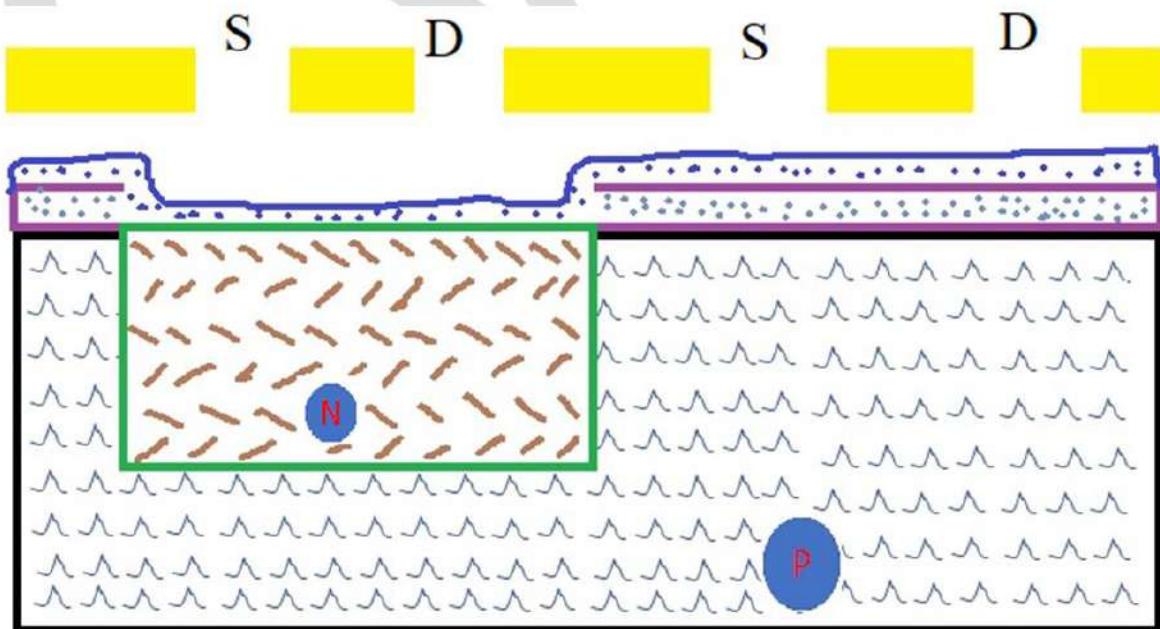
**STEP 1:** This process start with a p-type silicon substrate with oxide layer grown on the entire surface.



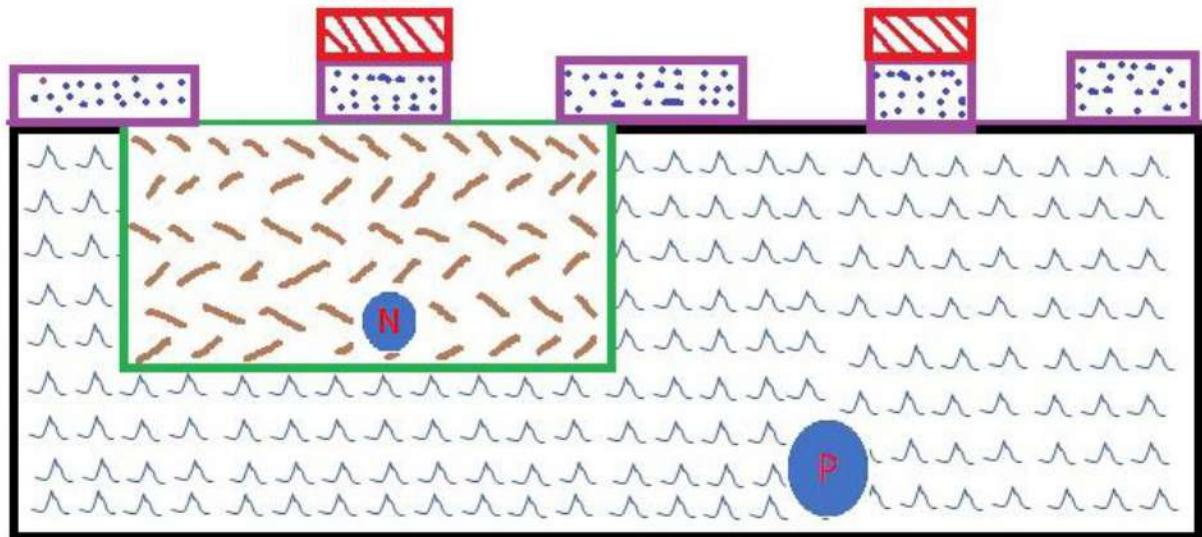
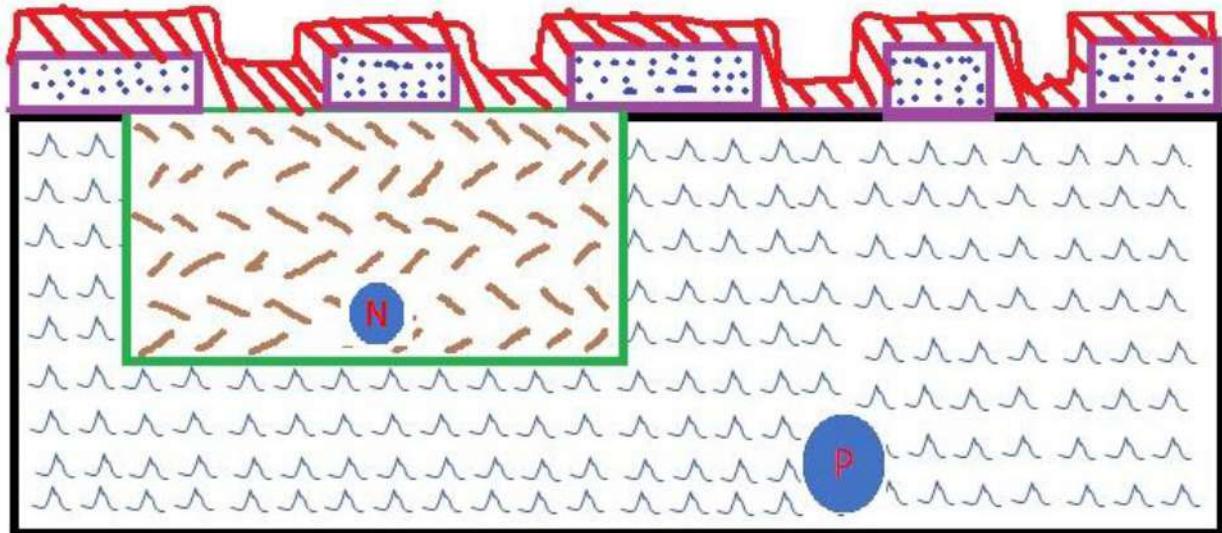
**STEP 2:** Define areas in which the deep N-well diffusions are to take place.



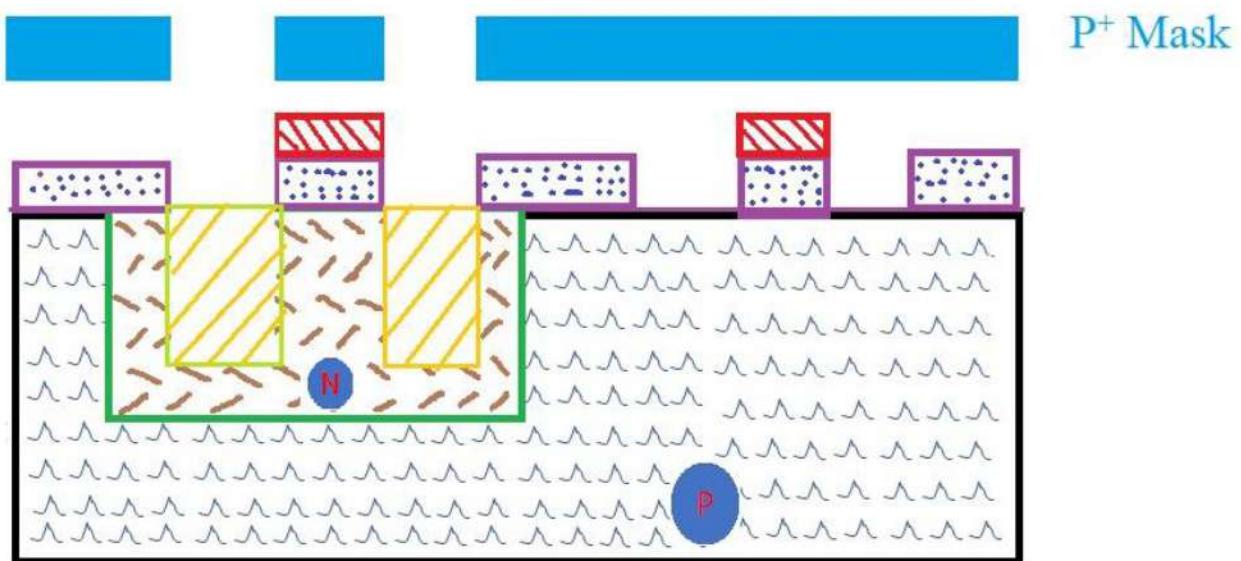
**STEP 3:** Masks for source and drain for both NMOS and PMOS transistors.



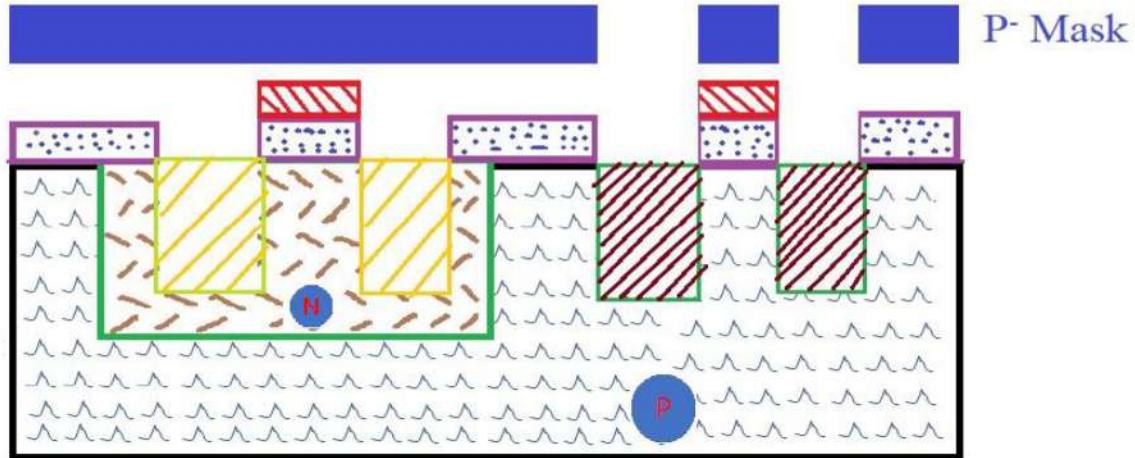
**STEP 4:** Poly-Silicon layer formation for gate electrode



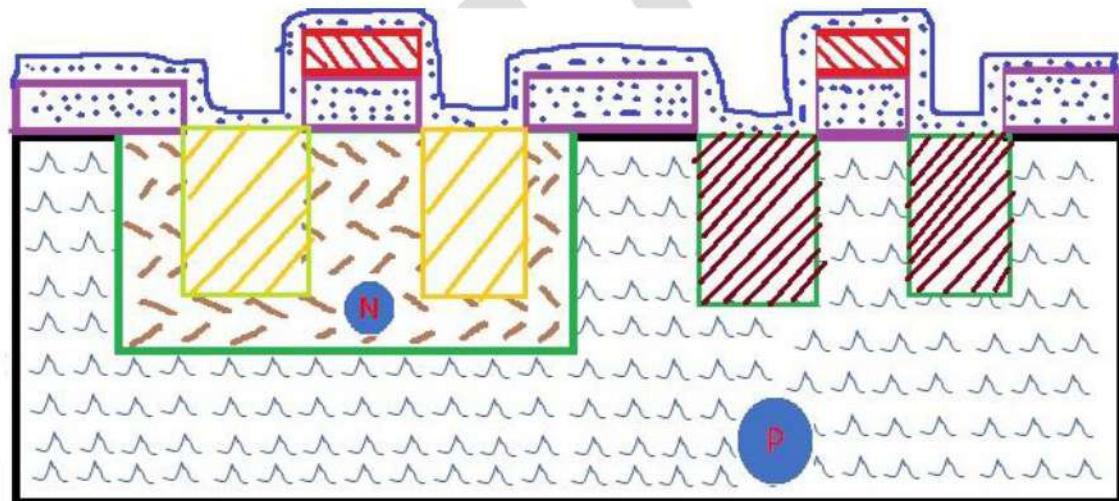
**STEP 5:** Defines where P diffusion is needed.



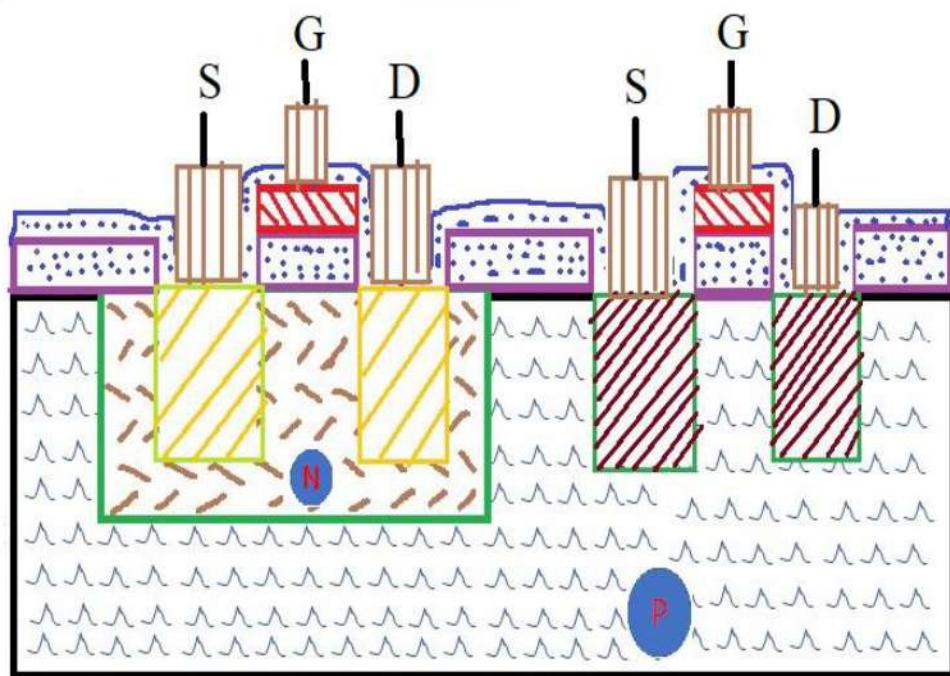
**STEP 6:** Defines where n diffusion is needed.



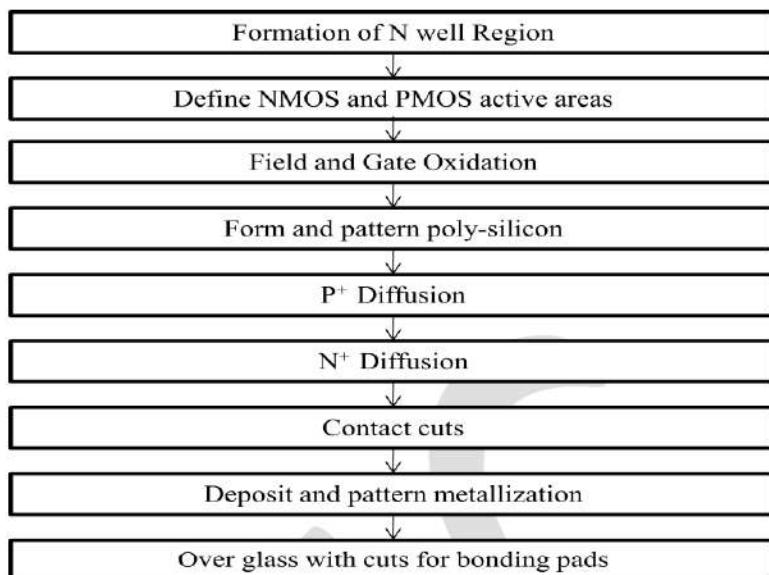
**STEP 7:** Before forming the metal terminals a thin  $\text{SiO}_2$  is laid out to form a protective layer for the regions of the wafer where no terminals are required.



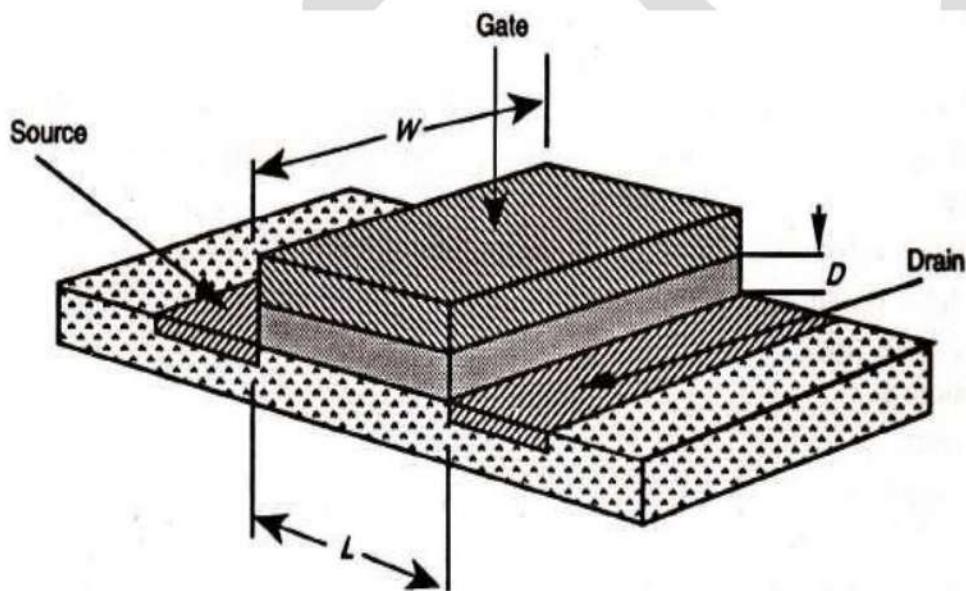
**STEP 8:** This step is used for the formation of metal terminals which can provide interconnections.



### Main steps in a typical N-well Process:



### Drain-to-Source Current $I_{DS}$ versus Voltage $V_{DS}$ Relationships:



The working of a MOS transistor is based on the principle that the use of a voltage on the gate induces a charge in the channel between source and drain, which may then be caused to move from source to drain under the influence of an electric field created by voltage  $V_{ds}$  applied between drain and source. Since the charge induced is dependent on the gate to source voltage  $V_{gs}$  then  $I_{ds}$  is dependent on both  $V_{gs}$  and  $V_{ds}$ . Let us consider the figure in which electrons will flow source to drain. So, the drain current is given by

$$I_{ds} = -I_{sd} = \frac{\text{Charge induced in channel (Qc)}}{\text{Electron transit time (\tau)}}$$

Where the transit time is given by  $\tau_{sd} = \frac{\text{Length of the channel}}{\text{Velocity (V)}}$

But velocity  $v = \mu E_{ds}$

Where  $\mu$  = electron or hole mobility and also,  $E_{ds} = V_{ds}/L$

So,  $v = \mu \cdot V_{ds}/L$  and  $\tau_{ds} = L^2/\mu \cdot V_{ds}$

The typical values of  $\mu$  at room temperature are given below.

$\mu_n \approx 650 \text{ cm}^2/\text{V sec}$  (surface)

$\mu_p \approx 240 \text{ cm}^2/\text{V sec}$  (surface)

### **The Non-saturated Region:**

Let us consider the  $I_d$  vs  $V_d$  relationships in the non-saturated region. The charge induced in the channel due to the voltage difference between the gate and the channel,  $V_{gs}$  (assuming substrate connected to source). The voltage along the channel varies linearly with distance  $X$  from the source due to the IR drop in the channel. In the non-saturated state the average value is  $V_{ds}/2$ . Also the effective gate voltage  $V_g = V_{gs} - V_t$  where  $V_t$  is the threshold voltage needed to invert the charge under the gate and establish the channel. Note that the charge/unit area =  $E_g \epsilon_{ins} \epsilon_0$ .

Hence the induced charge is  $Q_c = E_g \epsilon_{ins} \epsilon_0 W \cdot L$

Where  $E_g$  = average electric field gate to channel

$\epsilon_{ins}$  = relative permittivity of insulation between gate and channel

$\epsilon_0$  = permittivity of free space

So, we can write that

$$E_g = \frac{[(V_{gs} - V_t) - \frac{V_{ds}}{2}]}{D}$$

Here D is the thickness of the oxide layer. Thus

$$Q_c = \frac{WL\epsilon_{ins}\epsilon_0}{D} \left[ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right]$$

So, by combining the above two equations, we get

$$I_{ds} = \frac{\epsilon_{ins}\epsilon_0\mu}{D} \frac{W}{L} \left[ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right] V_{ds}$$

Or the above equation can be written as

$$I_{ds} = K \frac{W}{L} \left[ (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right]$$

In the non-saturated or resistive region where  $V_{ds} < V_{gs} - V_t$  and

$$K = \frac{\epsilon_{ins}\epsilon_0\mu}{D}$$

Generally, a constant  $\beta$  is defined as

$$\beta = K \frac{W}{L}$$

So that, expression for drain-source current will become

$$I_{ds} = \beta \left[ (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right]$$

The gate/channel capacitance is

$$C_g = \frac{WL\epsilon_{ins}\epsilon_0}{D} \text{ (parrel plate)}$$

Hence we can write another alternative form for the drain current as

$$I_{ds} = \frac{\mu C_g}{L^2} \left[ (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Some time it is also convenient to use gate-capacitance per unit area,  $C_g$

So, the drain current is

$$I_{ds} = C_0\mu \frac{W}{L} \left[ (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right]$$

This is the relation between drain current and drain-source voltage in non-saturated region.

### The Saturated Region

Saturation begins when  $V_{ds} = V_{gs} - V_t$ , since at this point the IR drop in the channel equals the effective gate to channel voltage at the drain and we may assume that the current remains fairly constant as  $V_{ds}$  increases further. Thus

$$I_{ds} = \frac{\epsilon_{ins}\epsilon_0\mu}{D} \frac{W}{L} \left[ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right] V_{ds}$$

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

or we can also write that

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

or it can also be written as

$$I_{ds} = \frac{C_g\mu}{2L^2} (V_{gs} - V_t)^2$$

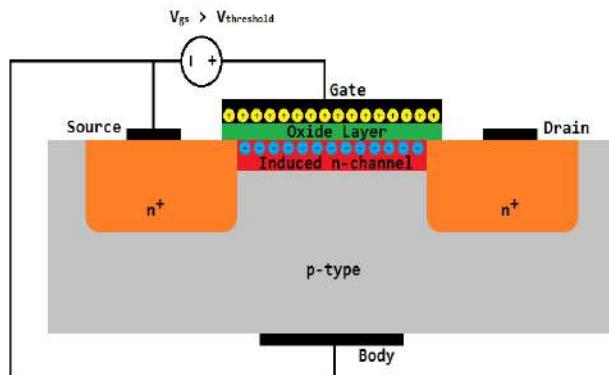
(or)

$$I_{ds} = C_0\mu \frac{W}{2L} (V_{gs} - V_t)^2$$

The expressions derived above for  $I_{ds}$  hold for both enhancement and depletion mode devices. Here the threshold voltage for the nMOS depletion mode device (denoted as  $V_{td}$ ) is negative.

### Threshold Voltage (V<sub>t</sub>)

- The **threshold voltage**, commonly abbreviated as V<sub>th</sub> is required to minimum gate-to-source **voltage** V<sub>GS</sub> i.e the create a conducting path between the source and drain terminals.



- The minimum **voltage** required to ON the transistor is called **Threshold voltage**. It is observed as positive value for NMOS transistor and negative value for PMOS transistor.
- Switching an enhancement mode MOS transistor from the off to the on state consists in applying sufficient gate voltage to neutralize these charges and enable the underlying silicon to undergo an inversion due to the electric field from the gate.
- Switching a depletion mode nMOS transistor from the on to the off state consists in applying enough voltage to the gate to add to the stored charge and invert the 'n' implant region to 'p'.

The threshold voltage V<sub>t</sub> may be expressed as

$$V_t = \phi_{ms} - \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{fN}$$

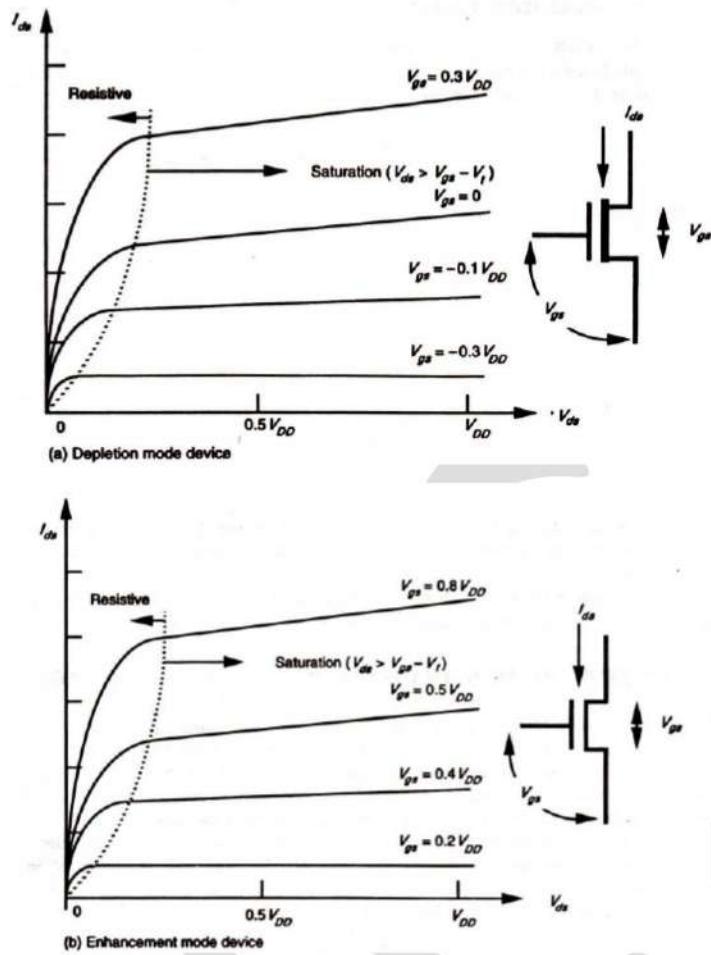
Where Q<sub>B</sub> = the charge per unit area in the depletion layer below the oxide

Q<sub>ss</sub> = charge density at Si: SiO<sub>2</sub> interface

C<sub>0</sub> = Capacitance per unit area.

$\Phi_{ms}$  = work function difference between gate and Si

$\Phi_{fN}$  = Fermi level potential between inverted surface and bulk Si



### Trans-conductance ( $g_m$ )

Trans-conductance expresses the relation between output current  $I_{ds}$  and the input voltage  $V_{gs}$  and is defined as

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \quad \because V_{ds} = \text{constant}$$

To find an expression for  $g_m$  in terms of circuit and transistor parameters, consider that the charge in the channel  $Q_c$  is such that

$$I_{ds} = \frac{Q_c}{\tau}$$

Thus change in current

$$\delta I_{ds} = \frac{\delta Q_c}{\delta \tau}$$

$$\delta I_{ds} = \frac{\delta Q_c \mu V_{ds}}{L^2}$$

But change in charge

$$\delta Q_c = C_g \delta V_{gs}$$

$$\delta I_{ds} = \frac{C_g \delta V_{gs} \mu V_{ds}}{L^2}$$

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

In saturated region  $V_{ds} = V_{gs} - V_t$

$$g_m = \frac{C_g \mu (V_{gs} - V_t)}{L^2}$$

Substituting  $C_g = \frac{WL\varepsilon_{ins}\varepsilon_0}{D}$

$$g_m = \frac{W\varepsilon_{ins}\varepsilon_0}{D} \frac{\mu(V_{gs} - V_t)}{L}$$

$$g_m = \beta(V_{gs} - V_t)$$

It is possible to increase the gm of a MOS device by increasing its width.  $g_m$  also increase the input capacitance and area occupied.

#### **Figure of merit ( $\omega_o$ )**

It is the indication of frequency response. It mathematically defined as

$$\omega_o = \frac{g_m}{C_g} = \frac{C_g \mu V_{ds}}{L^2 C_g} = \frac{\mu}{L^2} V_{ds}$$

For saturated region

$$\omega_o = \frac{\mu}{L^2} (V_{gs} - V_t)$$

#### **Comparison between PMOS and NMOS**

<b>NMOS</b>	<b>PMOS</b>
The majority carriers are electrons	The majority carriers are holes
Positive voltage is applied at the gate terminal	Negative voltage is applied at the gate terminal
NMOS conducts at logic 1	PMOS conducts at logic 0
Mobility of electrons is high	Mobility of electrons is low
Switching speed is high	Switching speed is low

#### **Comparison between CMOS and Bipolar Technology**

<b>CMOS</b>	<b>Bipolar Technology</b>
Low static power dissipation	High power dissipation
High input impedance	Low input impedance
High packing density	Low packing density
High delay sensitivity to load	Low delay sensitivity to load
Low output drive current	Low output drive current
Low gain	High gain
Bi directional capability	Unidirectional

**Two Marks Questions**

1. List out the different steps involved in the IC fabrication process.
2. Define the term threshold voltage of MOSFET.
3. Distinguish between CMOS and BiCMOS.
4. Define the threshold voltage with suitable equation of a MOS device.
5. What is Moore's law? State various IC technologies on the basis of number of transistors on a chip?
6. Describe the different operating regions for an MOS transistor.
7. Differentiate between PMOS and NMOS transistors.
8. Write the basic DC equations of a MOS transistor design in cutoff, saturation and linear region.
9. Mention different MOS layers.
10. Define Latch-up in a MOS circuit. Mention any one of remedial process to reduce latch-up.

**Ten Marks Questions**

1. Explain clearly about NMOS fabrication process flow with neat diagrams.
2. Explain the processing steps in fabrication of PMOS technology with neat sketches.
3. Explain clearly about n-well CMOS fabrication process with neat diagrams.
4. Explain clearly about p-well CMOS fabrication process with neat diagrams.
5. (a) Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region.  
(b) When the gate to source voltage  $V_{GS}$  of a MOSFET with threshold voltage of 400 mv, working in saturation is 900 mv, the drain current is observed to be 1 mA and assuming that the MOSFET is operating at saturation, calculate the drain current for an applied  $V_{GS}$  of 1400 mv.

**ASSIGNMENT QUESTIONS**

1. Explain NMOS fabrication process flow with neat diagrams.
2. Explain clearly about n-well CMOS fabrication process with neat diagrams.
3. Explain clearly about p-well CMOS fabrication process with neat diagrams.
4. Draw V-I characteristics of NMOS transistor. Explain its operation. Derive the drain to source current equation in saturation and resistive region.