### JNTUA B.Tech. R20 Regulations



# JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR B.Tech III-II Sem L T P C 3 0 0 3

# (20A04606) BASIC VLSI DESIGN

# **Course Objectives:**

- Understand the fundamental aspects of circuits in silicon
- Relate to VLSI design processes and design rules

#### **Course Outcomes:**

- Identify the CMOS layout levels, and the design layers used in the process sequence.
- Describe the general steps required for processing of CMOS integrated circuits.
- Design static CMOS combinational and sequential logic at the transistor level.
- Demonstrate different logic styles such as complementary CMOS logic, pass-transistor Logic, dynamic logic, etc.
- Interpret the need for testability and testing methods in VLSI.

#### UNIT I

Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, pwell processes, BiCMOS, Comparison of bipolar and CMOS. Basic Electrical Properties of MOS And BiCMOS Circuits: Drain to source current versus voltage characteristics, threshold voltage, transconductance.

#### **UNIT II**

Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. Basic Circuit Concepts: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers.

### **UNIT III**

MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style Design rules and layout & Scaling of MOS Circuits:  $\lambda$  - based design rules, scaling factors for device parameters

## **UNIT IV**

Subsystem Design and Layout-1: Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates, pseudo nMOS, Dynamic CMOS Examples of structured design: Parity generator, Bus arbitration, multiplexers, logic function block, code converter.

#### UNIT V

Subsystem Design and Layout-2: Clocked sequential circuits, dynamic shift registers, bus lines, General considerations, 4-bit arithmetic processes, 4-bit shifter, RegularityDefinition& Computation Practical aspects and testability: Some thoughts of performance, optimization and CAD tools for design and simulation.

#### **Textbooks:**

1. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3 rd Edition, Prentice Hall of India publication, 2005.

#### **References:**

- 1. "CMOS Digital Integrated Circuits, Analysis And Design", Sung Mo (Steve) Kang, Yusuf Leblebici, Tata McGraw Hill, 3 rd Edition, 2003.
- 2. "VLSI Technology", S.M. Sze, 2nd edition, Tata McGraw Hill, 2003