UNIT-II

Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. Basic Circuit Concepts: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers.

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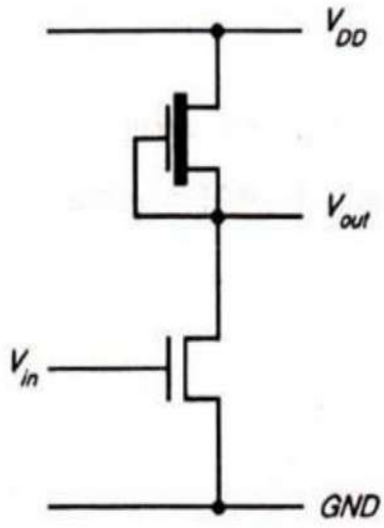
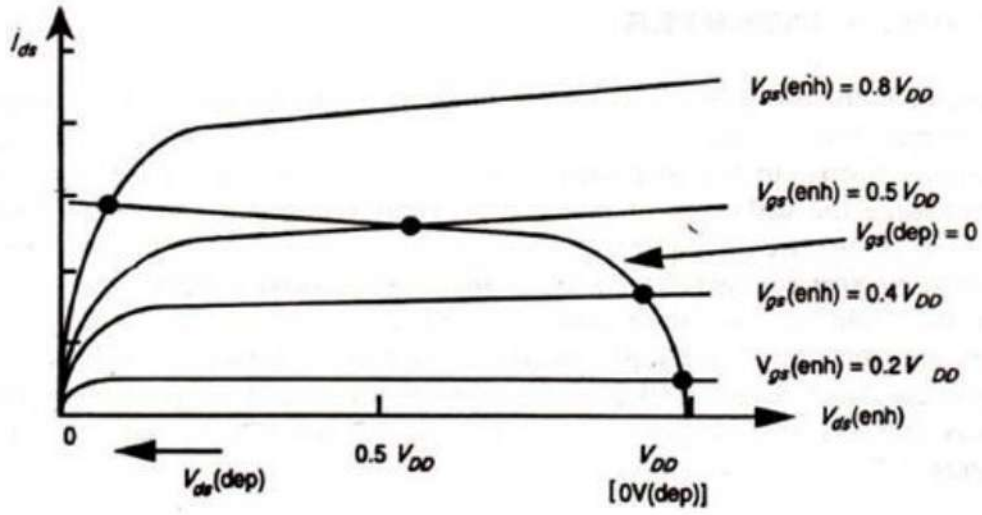
The NMOS INVERTER:

A simple inverter circuit can be constructed using a transistor with source connected to ground and a load resistor of connected from the drain to the positive supply rail V_{DD}. The output is taken from the drain and the input applied between gate and ground.



- With no current drawn from the output, the currents I_{ds} for both transistors must be equal.
- For the depletion mode transistor, the gate is connected to the source so it is always on and only the characteristic curve $V_{gs} = 0$ is relevant.
- In this configuration the depletion mode device is called the pull-up (p.u.) and the enhancement mode device the pull-down (p.d.) transistor.
- To obtain the inverter transfer characteristic we superimpose the $V_{gs} = 0$ depletion mode characteristic curve on the family of curves for the enhancement mode device, nothing that maximum voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor.
- Note that as V_{in} ($=V_{gs}$ p.d. transistor) exceeds the p.d. threshold voltage current begins to flow. The output voltage V_{out} thus decreases and the subsequent increases in V_{in} will cause the p.d. transistor to come out of saturation and become resistive. Note that the p.u. transistor is initially resistive as the p.d. turns on.

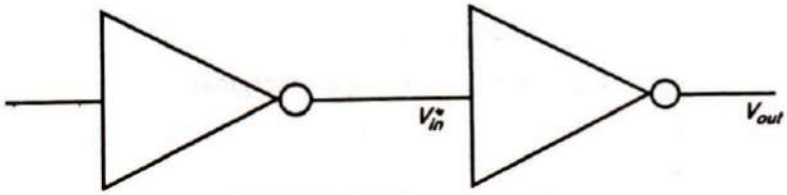
NMOS Inverter transfer characteristic.



PULL-UP TO PULL-DOWN RATIO FOR NMOS INVERTER DRIVEN BY ANOTHER NMOS INVERTER

Consider an inverter is driven from the output of another similar inverter. Consider the depletion mode transistor for which V_{gs} = 0 under all conditions, and further assume that in order to cascade inverters without degradation of levels we are aiming to meet the requirement.

$$V_{in}=V_o=V_{inv}$$



For equal margins around the inverter threshold, we set V_{inv} = 0.5 V_{DD}. At this point both transistors are in saturation.

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$

$$K = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}$$

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$

For the depletion MOSFET

$$V_{gs} = 0 \ \& \ V_t = V_{td}$$

V_{td}= Threshold voltage of depletion MOSFET

$$I_{ds} = K\frac{W_{p.u}}{L_{p.u}}\frac{(0-V_{td})^2}{2} = K\frac{W_{p.u}}{L_{p.u}}\frac{(-V_{td})^2}{2}$$

For NMOS enhancement transistor in saturation region

$$V_{in}=V_{gs}=V_{inv}$$

Therefore

$$I_{ds} = K\frac{W_{p.d}}{L_{p.d}}\frac{(V_{inv}-V_t)^2}{2}$$

From above expressions

$$K\frac{W_{p.d}}{L_{p.d}}\frac{(V_{inv}-V_t)^2}{2} = K\frac{W_{p.u}}{L_{p.u}}\frac{(-V_{td})^2}{2}$$

where *Wp.d,Lp.d., Wp.u.,* and *Lp.u.* are the widths and lengths of the pull-down and pull-up transistors respectively.

$$Z_{p.u} = \frac{L_{p.u}}{W_{p.u}}$$

$$Z_{p.d} = \frac{L_{p.d}}{W_{p.d}}$$

Now write

$$\frac{1}{Z_{p.d}}(V_{inv}-V_t)^2 = \frac{1}{Z_{p.u}}(-V_{td})^2$$

$$\frac{Z_{p.u}}{Z_{p.d}} = \frac{(-V_{td})^2}{(V_{inv}-V_t)^2}$$

Typical values of threshold voltages:

For enhancement MOSFET V_t=0.2 V_{DD}

For Depletion MOSFET V_{td}=-0.6 V_{DD}

In saturation region V_{inv}=0.5 V_{DD}

$$\frac{Z_{p.u}}{Z_{p.d}} = \frac{(-0.6V_{DD})^2}{(0.5V_{DD}-0.2V_{DD})^2} = \left(\frac{0.6V_{DD}}{0.3V_{DD}}\right)^2 = \left(\frac{2}{1}\right)^2 = \frac{4}{1}$$

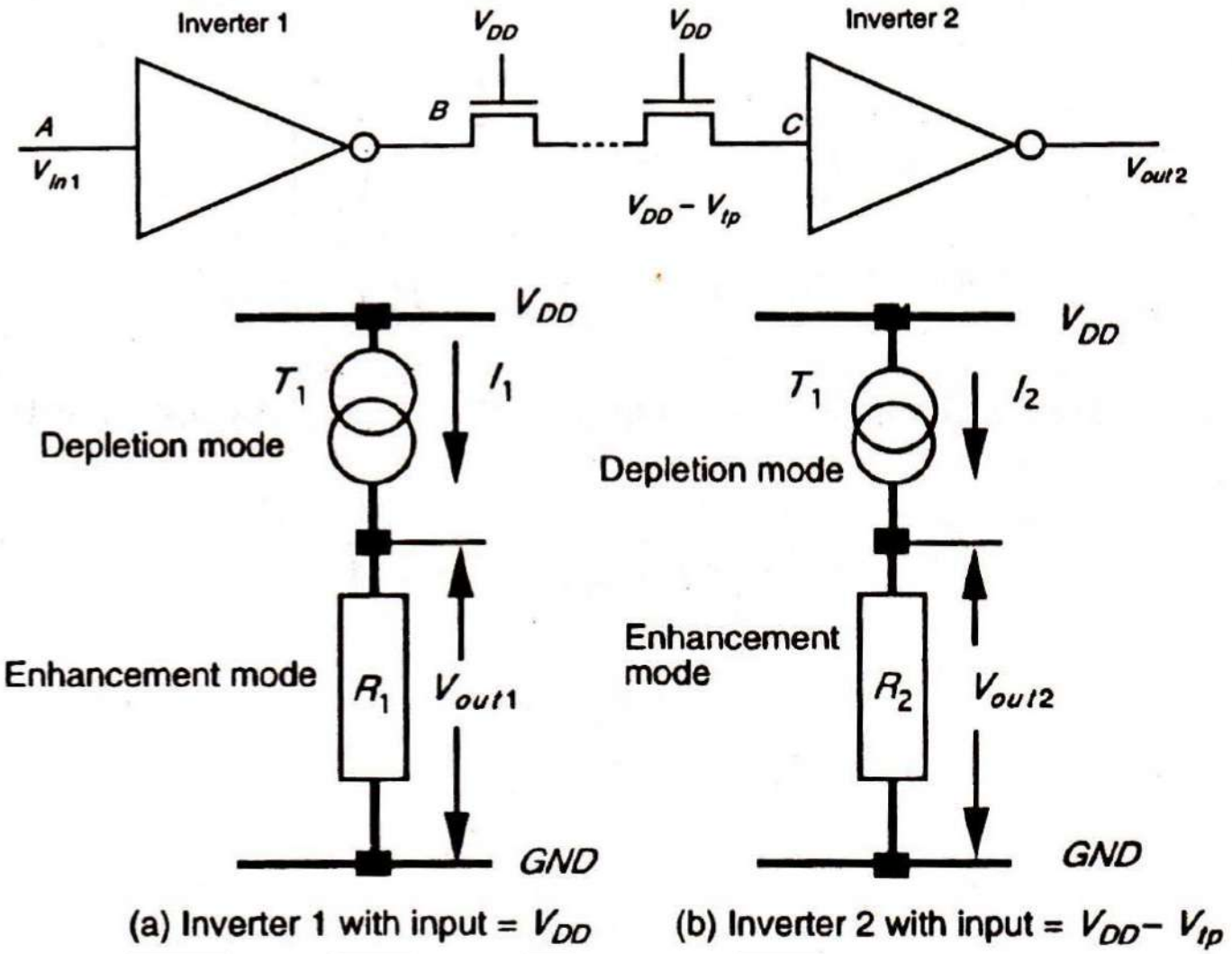
for an inverter directly driven by an inverter.

PULL-UP TO PULL-DOWN RATIO FOR AN nMOS INVERTER DRIVEN THROUGH ONE OR MORE PASS TRANSISTORS

The input to inverter 2 comes from the output of inverter 1 but passes through one or more nMOS transistors used as switches in series (called *pass transistors).*Pass transistors in series will degrade the logic1 level into inverter 2 so that the output will not be a proper logic 0 level. The critical condition is when point *A* is at 0 volts and *B* is thus at V_{DD}. But the voltage into inverter 2 at point *C* is now reduced from V_{DD} by the threshold voltage of the series pass transistor. With all pass transistor gates connected to V_{DD}, there is a loss of V_{tp}, however many are connected in series, since no static current flows through them and there can be no voltage drop in the channels. Therefore, the input voltage to inverter 2 is

$$V_{in2}=V_{DD}-V_{tp}$$

Where, V_{tp} threshold voltage for a pass transistor.



Consider inverter 1 with input = V_{DD}. If the input is at V_{DD}, then the p.d. transistor T1 is conducting but with a low voltage across it; therefore, it is in its resistive region represented by *R1*, the p.u. transistor *T1* is in saturation and is represented as a current source.

For non saturation region of enhancement transistor

$$I_{ds} = K\frac{W}{L}\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]V_{ds}$$

Here $V_{gs}=V_{DD}$ and $V_{ds}=V_{ds1}$(Very small)

$$I_{ds} = K\frac{W_{p.d1}}{L_{p.d1}}\left[(V_{DD} - V_t) - \frac{V_{ds1}}{2}\right]V_{ds1}$$

$$I_{ds} = K\frac{1}{Z_{p.d1}}\left[(V_{DD} - V_t) - \frac{V_{ds1}}{2}\right]V_{ds1}$$

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K\frac{1}{Z_{p.d1}}\left[(V_{DD} - V_t) - \frac{V_{ds1}}{2}\right]}$$

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{Z_{p.d1}}{K}\frac{1}{(V_{DD} - V_t)}$$

Here V_{ds1} is very small so $V_{ds1}/2$ is negligible.

Transistor T_1 is in saturation mode

$$I_{ds1} = K\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$

Here $I_{ds1}=I_1$, $V_{gs}=0$ & $V_t=V_{td}$

$$I_1 = K\frac{W_{p.u1}}{L_{p.u1}}\frac{(-V_{td})^2}{2} = K\frac{1}{Z_{p.u1}}\frac{(-V_{td})^2}{2}$$

Therefore $Vo1=I_1 * R_1$

$$V_{o1} = \frac{Z_{p.d1}}{Z_{p.u1}}\frac{(-V_{td})^2}{2(V_{DD}-V_t)}$$

Similarly, Consider inverter 2 when input = V_{DD}-V_{tp}.

Here $V_{gs}=V_{DD}-V_{tp}$ and $V_{ds}=V_{ds2}$ (Very small)

$$I_{ds} = K\frac{W_{p.d2}}{L_{p.d2}}\left[(V_{DD}-V_{tp}-V_t)-\frac{V_{ds2}}{2}\right]V_{ds2}$$

$$I_{ds} = K\frac{1}{Z_{p.d2}}\left[(V_{DD}-V_{tp}-V_t)-\frac{V_{ds2}}{2}\right]V_{ds2}$$

$$R_2 = \frac{V_{ds2}}{I_{ds}} = \frac{1}{K\frac{1}{Z_{p.d2}}\left[(V_{DD}-V_{tp}-V_t)-\frac{V_{ds2}}{2}\right]}$$

$$R_2 = \frac{V_{ds2}}{I_{ds}} = \frac{Z_{p.d2}}{K}\frac{1}{(V_{DD}-V_{tp}-V_t)}$$

Here V_{ds2} is very small so $V_{ds2}/2$ is negligible.

Transistor T_2 is in saturation mode

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2}$$

Here $I_{ds2}=I_2$, $V_{gs}=0$ & $V_t=V_{td}$

$$I_{ds} = K\frac{W_{p.u2}}{L_{p.u2}}\frac{(-V_{td})^2}{2} = K\frac{1}{Z_{p.u2}}\frac{(-V_{td})^2}{2}$$

Therefore $Vo2=I_2 * R_2$

$$V_{o2} = \frac{Z_{p.d2}}{Z_{p.u2}}\frac{(-V_{td})^2}{2(V_{DD}-V_{tp}-V_t)}$$

If inverter 2 is to have the same output voltage under these conditions then $V_{out1}=V_{out2}$.

That is $I_1R_1=I_2R_2$

$$\frac{Z_{p.d1}}{Z_{p.u1}}\frac{(-V_{td})^2}{2(V_{DD}-V_t)} = \frac{Z_{p.d2}}{Z_{p.u2}}\frac{(-V_{td})^2}{2(V_{DD}-V_{tp}-V_t)}$$

$$\frac{Z_{p.d2}}{Z_{p.u2}} = \frac{Z_{p.d1}}{Z_{p.u1}}\frac{V_{DD}-V_{tp}-V_t}{V_{DD}-V_t}$$

Substitute V_{tp}=0.3 V_{DD} & V_t=0.2 V_{DD}

$$\frac{Z_{p.d2}}{Z_{p.u2}} = \frac{Z_{p.d1}}{Z_{p.u1}} \frac{(V_{DD} - 0.3V_{DD} - 0.2V_{DD})}{(V_{DD} - 0.2V_{DD})}$$

$$\frac{Z_{p.d2}}{Z_{p.u2}} = \frac{Z_{p.d1}}{Z_{p.u1}} \frac{0.5V_{DD}}{0.8V_{DD}}$$

$$\frac{Z_{p.u2}}{Z_{p.d2}} = \frac{Z_{p.u1}}{Z_{p.d1}} \frac{0.8V_{DD}}{0.5V_{DD}} = \frac{Z_{p.u1}}{Z_{p.d1}}\ 2 = \frac{4}{1} * 2 = \frac{8}{1}$$

Summarizing for an NMOS inverter:

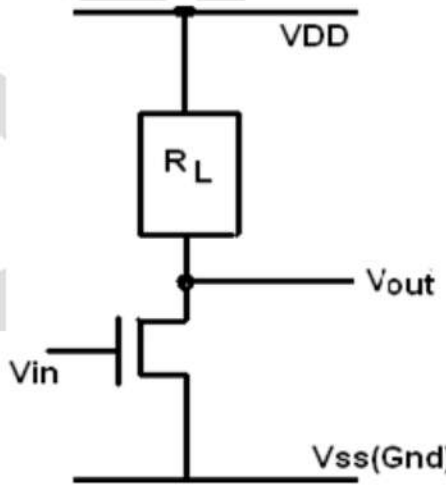
- An inverter driven directly from the output of another should have a $Z_{p.u}/Z_{p.d}$ ratio of ≥4/1.
- An inverter driven through one or more pass transistors should have a $Z_{p.u}/Z_{p.d}$ ratio of ≥8/1.

ALTERMTIVE FORMS OF PULL –UP

Generally the inverter circuit will have a depletion mode pull-up transistor as its load. But there is also other configurations .Let us consider four such arrangements.

(i).Load resistance RL: This arrangement consists of a load resistor as a pull-up as shown in the diagram below. But it is not widely used because of the large space requirements of resistors produced in a silicon substrate.

- If $V_{in} < V_{TN}$, the transistor is in cutoff and $i_D = 0$, there is no voltage drop across R_D, and the output voltage is $V_o = V_{DD} = V_{DS}$.
- If $V_{in} > V_{TN}$, the transistor is **on** and initially is biased in **saturation region**, since $V_{DS} < V_{GS} - V_{TN}$.
- As the input voltage **increases** (V_{GS}), the drain to source voltage (V_{DS}) **decreases** and the transistor inter into the **non-saturation region.**

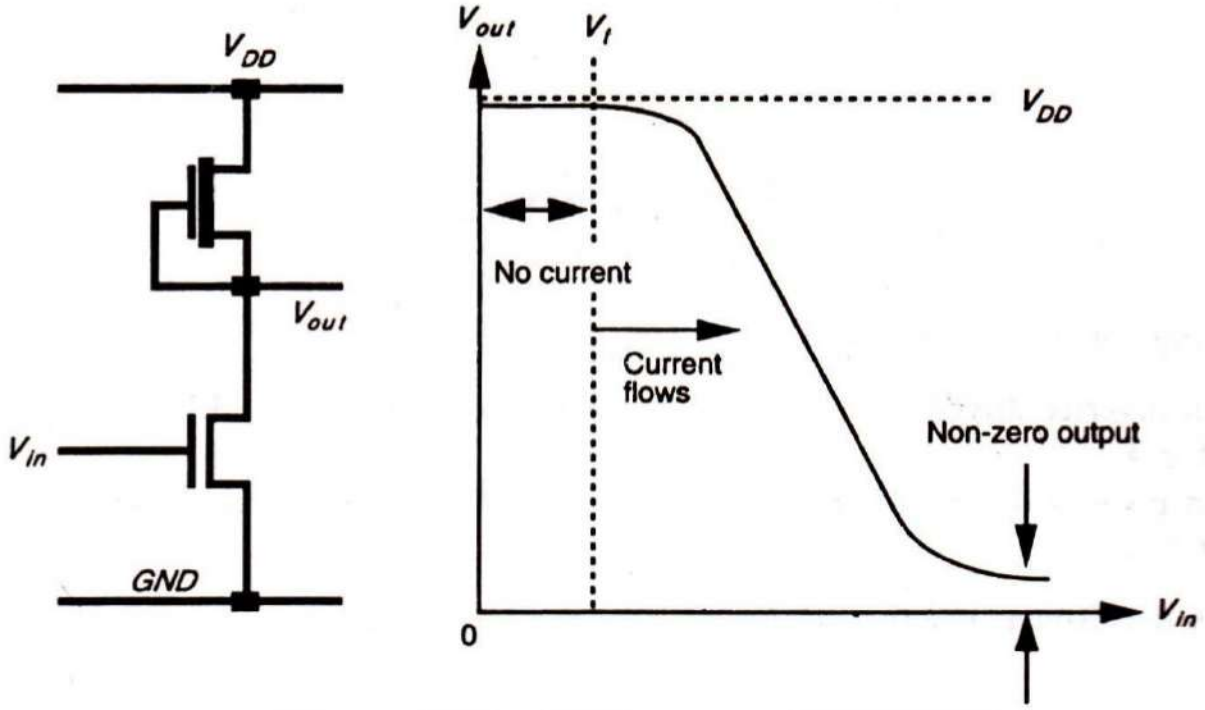


2. **NMOS depletion mode transistor pull-up :** This arrangement consists of a depletion mode transistor as pull-up. The arrangement and the transfer characteristic are shown below. In this type of arrangement we observe

   (a) Dissipation is high, since rail to rail current flows when V_{in} = logical 1.

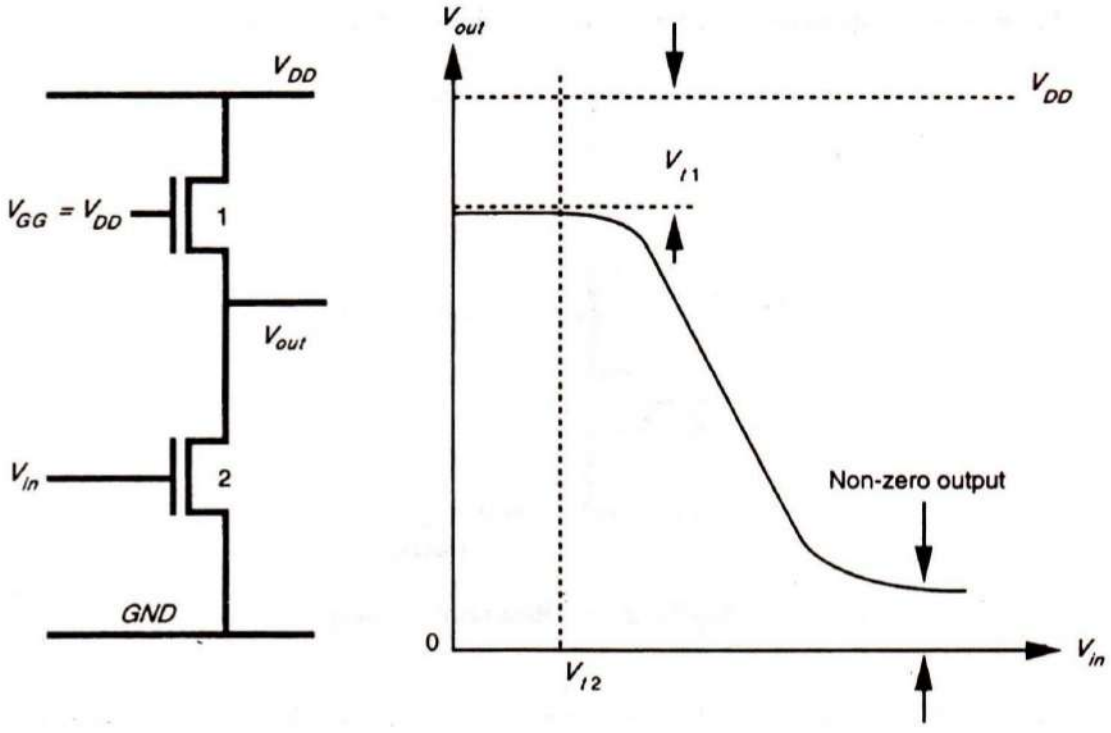
   (b) Switching of output from 1 to 0 begins when V_{in} exceeds V_t, of pull-down device.

(c) When switching the output from 1 to 0, the pull-up device is non-saturated initially and this presents lower resistance through which to charge capacitive loads.



NMOS depletion mode transistor pull-up and transfer characteristic

3. **NMOS enhancement mode pull-up:** This arrangement consists of a n-MOS enhancement mode transistor as pull-up. The arrangement and the transfer characteristic are shown below.



NMOS enhancement mode pull-up and transfer characteristic

The important features of this arrangement are

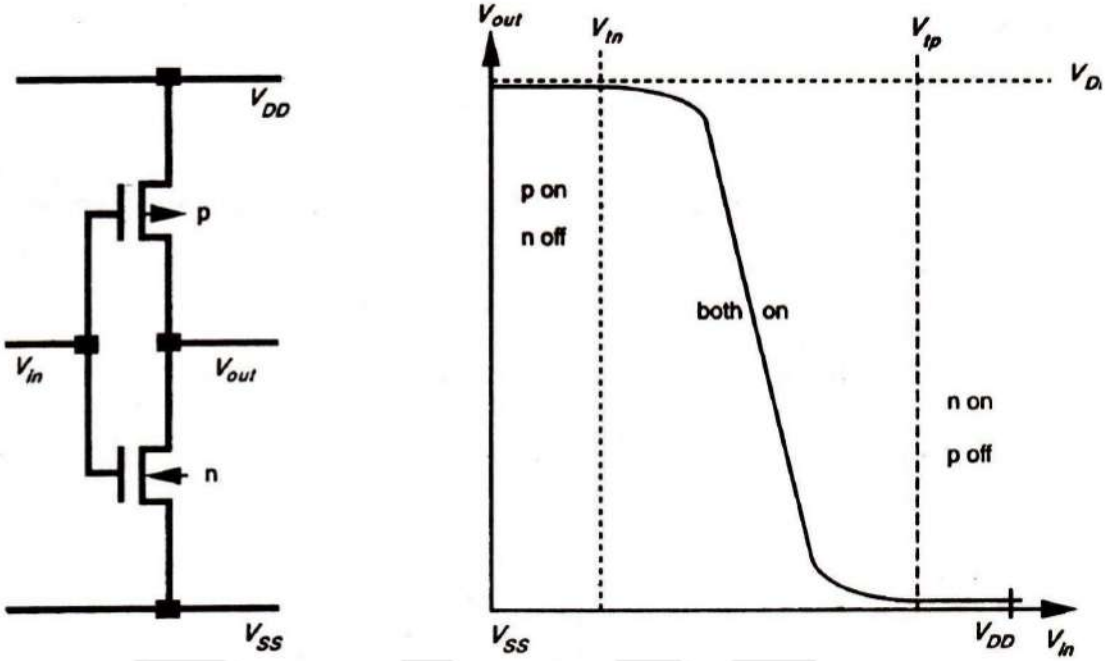
(a) Dissipation is high since current flows when V_{in} =logical 1 (V_{GG} is returned to V_{DD}).

(b) V_{out} can never reach V_{DD} (logical 1) if $V_{GG} = V_{DD}$ as is normally the case.

(c) V_{GG} may be derived from a switching source, for example, one phase of a clock, so that Dissipation can be greatly reduced.

(d) If V_{GG} is higher than V_{DD} then an extra supply rail is required.

4. Complementary transistor pull-up (CMOS): This arrangement consists of a C-MOS arrangement as pull-up. The arrangement and the transfer characteristic are shown below



The salient features of this arrangement are

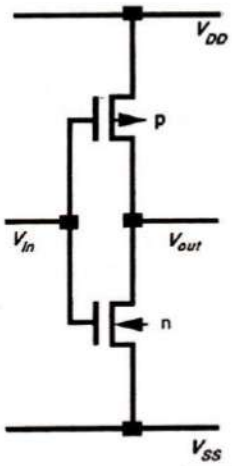
(a) No current flows either for logical 0 or for logical 1 inputs.

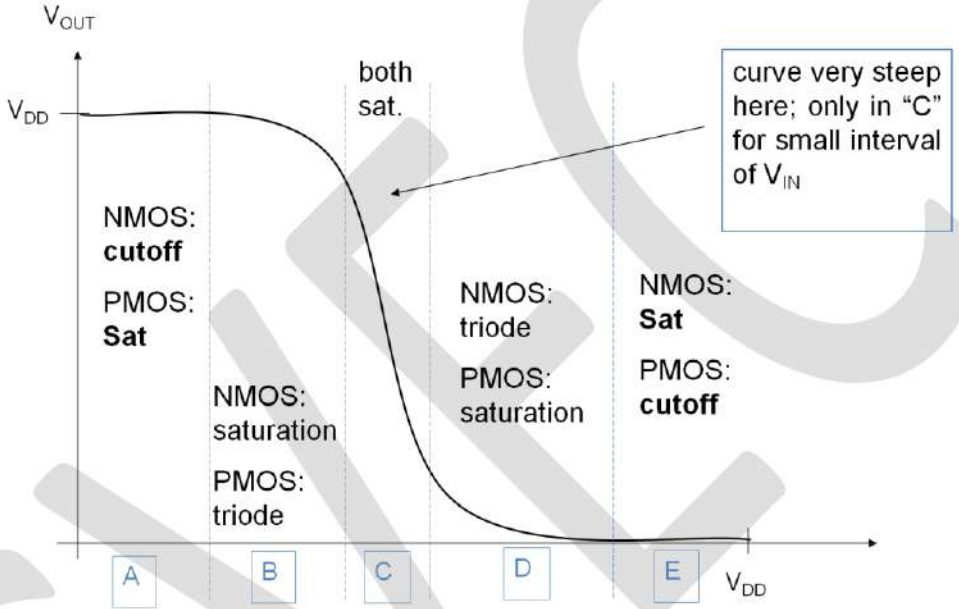
(b) Full logical 1 and 0 levels are presented at the output.

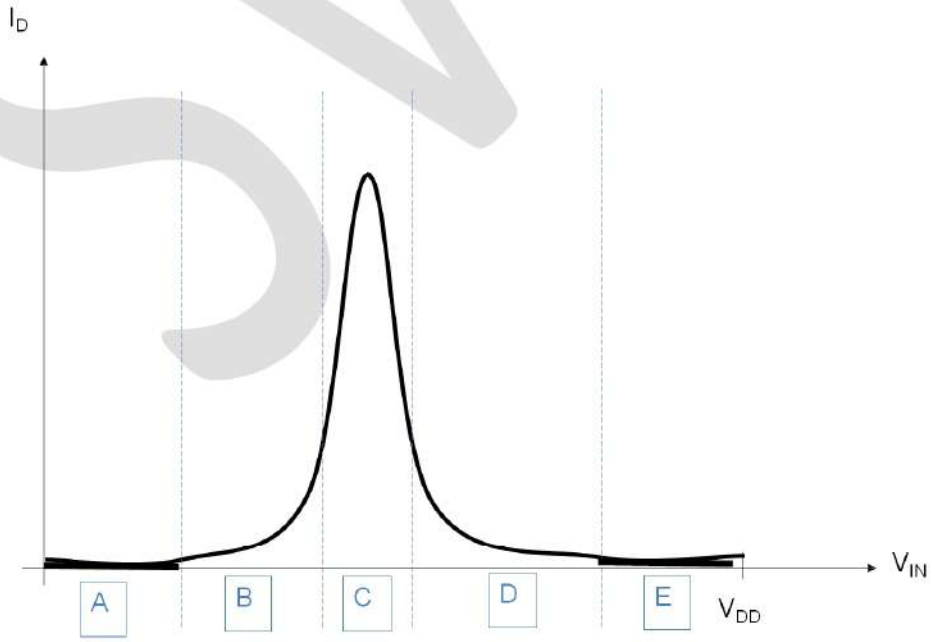
(c) For devices of similar dimensions the p-channel is slower than the n-channel device.

CMOS INVERTER

- An inverter circuit converts a logic high-input such as 1 V to a low logic voltage of 0 V and a logic low-input such as 0 V to a high logic Voltage of 1 V
- The Boolean statement Vout = Vin
- In CMOS technology, both N-type and P-type transistors are used to design logic functions.
- In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground).
- CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).


V_{DD}
p
V_{in}
V_{out}
n
V_{SS}


V_{OUT}
V_{DD}
both sat.
curve very steep here; only in "C" for small interval of V_{IN}
NMOS: **cutoff**
PMOS: **Sat**
NMOS: saturation
PMOS: triode
NMOS: triode
PMOS: saturation
NMOS: **Sat**
PMOS: **cutoff**
A
B
C
D
E
V_{DD}


I_D
V_{IN}
A
B
C
D
E
V_{DD}

Region A: When Vin=0 (Logic 0)

- P Transistor fully turned ON (Saturation)
- N Transistor fully turned OFF (Cutoff)

Thus no current flows through the inverter and the output is directly connected to VDD through the P transistor. A good logic 1 output voltage is thus present at the output.

Region E: When Vin= VDD (Logic 1)

- P Transistor fully turned OFF (Cutoff)
- N Transistor fully turned ON (Saturation)

No current flows through the inverter and a good logic 0 appears at the output.

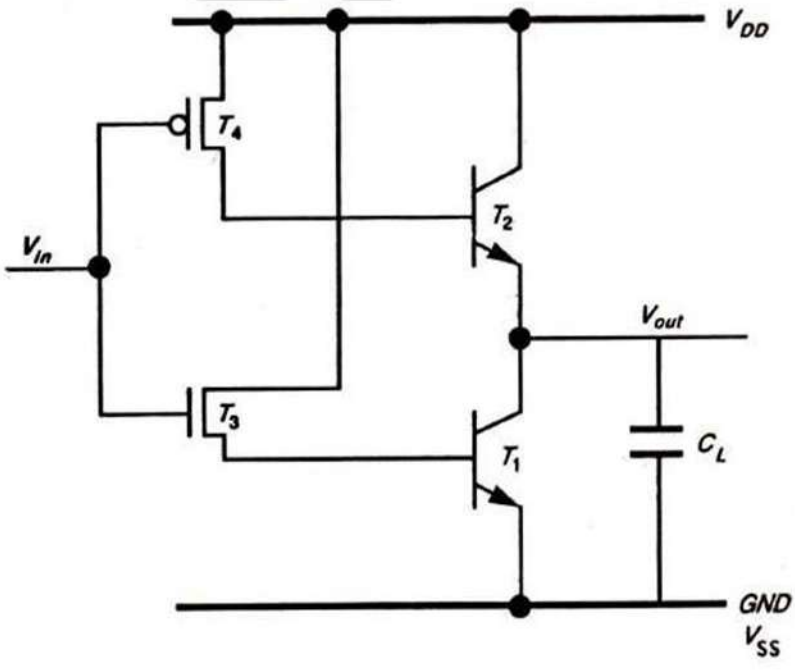
Region B: The input voltage has increased to a level which just exceeds the threshold voltage of the NMOS transistor. The NMOS transistor conducts and has a large voltage between source and drain. So it is in saturation. The P Transistor is also conducting but the only a small voltage across it, it operates in the resistive region. A small current flows through the inverter from V_{DD} to V_{SS}.

Region D: is similar to region B but with roles of the P and N transistors reversed.

Region C: Region C is the region in which the inverter exhibits gain and in which both transistors are in saturation.

Bi-CMOS Inverter

- As in nMOS and CMOS logic circuitry, the basic logic element is the inverter circuit.
- When designing with BiCMOS in mind, the logical approach is to use
  1. MOS switches to perform the logic function and
  2. Transistors to drive the output loads.



It consists of two bipolar transistors *T1* and *T2* with one nMOS transistor *T3,* and one pMOS transistor *T4*.

If Vin =0 Volts

T3=OFF so T1 will be non-conducting

T4 = ON so supplies current to base of T2 which will conduct and act as a current source to charge the load CL towards +5 Volts.

If Vin =+5 Volts

T4=OFF so T2 will be non-conducting

T3= ON so supplies current to base of T1 which will conduct and act as current sink to the load CL discharge it towards '0'.

Advantages:

- C_L will be charged or discharged rapidly.
- The output logic levels will be good.
- The inverter has a high input impedance.
- The inverter has a low output impedance.
- The inverter has a high current drive capability
- The inverter has high noise margins.

Drawback:

- There is a DC path between V_{DD} and GND through T_3 and T_1. Due to these there will significant static current flow when V_{in} = Logic 1.
- When $V_{in} = V_{DD}$, T_4= OFF and no conducting path to the base of T_2 .
- When V_{in}= 0, T_3=OFF and no conducting path to the base of T_1

So it will slow down the action of the circuit.

BASIC CIRCUIT CONCEPTS

The wiring up of circuits takes place through the various conductive layers which are produced by the MOS processing and it is therefore necessary to be aware of the resistive and capacitive of each layer. Sheet resistance and a standard unit capacitance helps greatly in evaluating the effects of wiring and input & output capacitances. The delay associated with wiring, with inverter and with other circuitry may be conveniently evaluated in terms of delay unit **τ.**

SHEET RESISTANCE

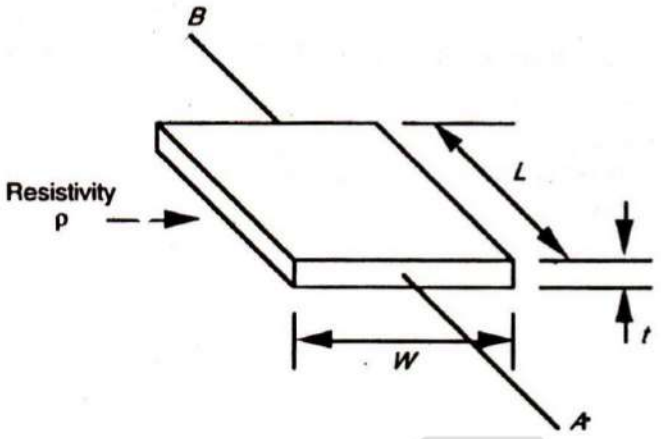
The concept of sheet resistance is being used to know the resistive behavior of the layers that go into formation of the MOS device. Let us consider a uniform slab of conducting material of the following characteristics.

Resistivity- ρ

Width - W

Thickness - t

Length between faces – L



- Resistance is given by $R_{AB} = \frac{\rho L}{A}\ \Omega$
- The area of the slab considered is given by A=Wt.
- Therefore $R_{AB} = \frac{\rho L}{Wt}\ \Omega$.
- If the slab is considered as a square then L=W. therefore $R_{AB}=\rho/t$ which is called as sheet resistance represented by R_s.
- The unit of sheet resistance is ohm per square.

Thus the actual values associated with the layers in a MOS circuit depend on the thickness of the layer and the resistivity of the material forming the layer. For the metal and poly-silicon layers, the thickness of a layer is easily envisaged and the resistivity of the material is known. For the diffusion layer, the depth of the diffusion regions –contributes toward the effective thickness while the impurity concentration (or doping level) profile determines the resistivity.

Typical sheet resistances of MOS layers are tabulated

Layer	**R_S ohm per square**		
	5µm	**Orbit**	**Orbit 1.2µm**
Metal	0.03	0.04	0.04
Diffusion	15 – 100	20-45	20-45
Silicide	2 – 4	---	---
Poly-silicon	15 – 100	15-30	15-30
n- channel	10^4	$2X10^4$	$2X10^4$
p-channel	$2.5\ X\ 10^4$	$4.5\ X\ 10^4$	$4.5\ X\ 10^4$

Sheet resistance concept applied to MOS Transistors

Consider the transistor structures by distinguish the actual diffusion (active) regions from the channel regions. The simple n-type pass transistor has a channel length L = 2λ and a channel width W=2λ.

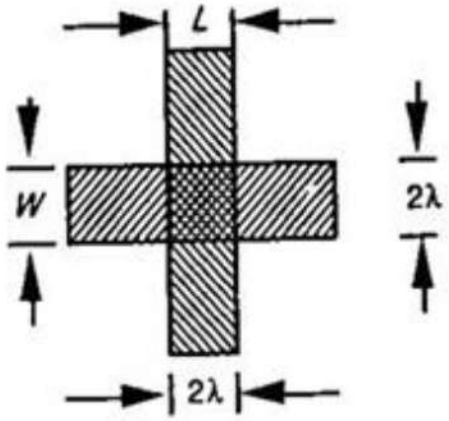
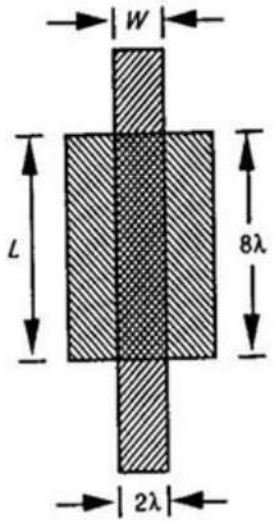


Figure: Resistance calculation for transistor channels

Hence the channel is square and the channel resistance is

$$R = \frac{\rho}{t}\frac{L}{W} = \frac{L}{W}R_s = \frac{2\lambda}{2\lambda}10^4 = 10K\Omega$$

Here the length to width ratio denotes the impedance (Z) and is equal to 1:1.



Consider another transistor has a channel length L = 8λ and width W = 2λ.

Thus, channel resistance

$$R = \frac{\rho}{t}\frac{L}{W} = \frac{L}{W}R_s = \frac{8\lambda}{2\lambda}10^4 = 40K\Omega$$

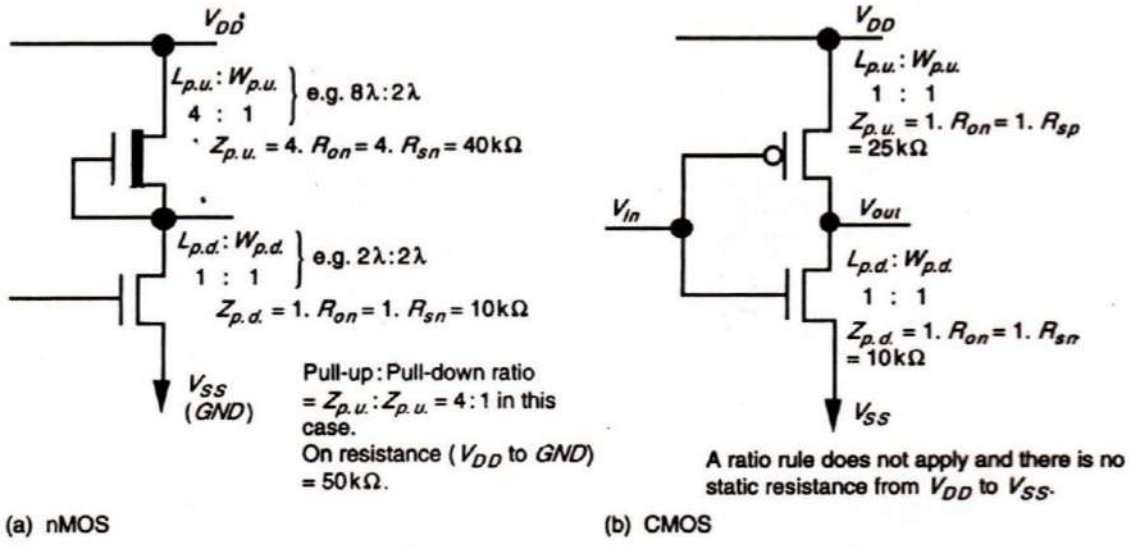
The length to width ratio, denoted Z, is 1:1 in this case. The transistor structure has length L=8 λ and width W=2 λ. Therefore

$$Z = \frac{L}{W} = 4$$

Thus channel resistance

$$R = Z\,Rs = 4 \times 10^4 \text{ ohm}$$

Sheet resistance for Inverters



Note: R_{on} = 'on' resistance; R_{sn} = n-channel sheet resistance; R_{sp} = p-channel sheet resistance.

Consider an nMOS inverter has the channel length 8λ and width 2λ for pull up transistor as shown in figure.

L=8λ;W=2λ

Z=L/W=4

Sheet resistance $R = Z.R_S = 4 \text{ X } 10^4 = 40 \text{ K}\Omega$

For pull down transistor the channel length 2λ and width 2λ, then the sheet resistance is $R = Z.R_S = 1 \text{ X } 10^4 = 10 \text{ K}\Omega$

Hence Zp.u to Zp.d = 4:1 hence the ON resistance between V_{DD} and V_{SS} is the total series resistance i.e.

R_{ON}=40KΩ+10KΩ=50KΩ

Consider the simple CMOS inverter as shown in figure 2.3.

CMOS inverter

Here the pull up transistor is of p-type device with channel length 2λ and width 2λ. Z = L/W =1

Then Sheet resistance $R_{SP} = Z.R_S = 1 \text{ X } 2.5 \text{ X } 10^4 = 25 \text{ K}\Omega$

The pull down transistor is of n-type with channel length 2λ and width 2λ.

Z=L/W=1

Hence, Sheet resistance $R_{SN} = Z.R_S = 1 \text{ X } 10^4 = 10 \text{ K}\Omega$.

In this case, there is no static resistance between V_{DD} and V_{SS} .Since at any point of time only one transistor is ON, but not both.

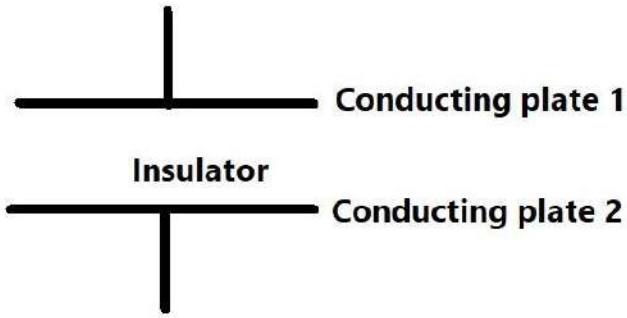
When V_{in} = 1, the ON resistance is 10KΩ

V_{in} = 0, the ON resistance is 25KΩ

MOS DEVICE CAPACITANCES

Area capacitance of layers

From the concept of the transistors, it is apparent that as gate is separated from the channel by gate oxide an insulating layer, it has capacitance. Similarly different interconnects run on the chip and each layer is separated by silicon dioxide.



For any layer by knowing the dielectric thickness, we can calculate the area capacitance as follows

$$C = \frac{\varepsilon_O \varepsilon_{ins} A}{D} \; Farads$$

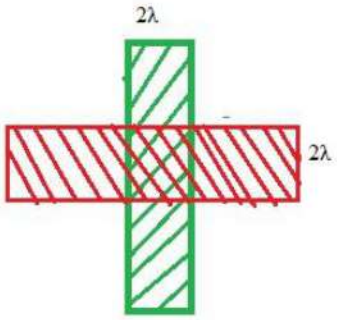
Where, A is area of the plates, D is the thickness of Sio2, Є0 is the permittivity of the free space and $Є_{ins}$ is the relative permittivity of insulator (Sio2).

Typical area capacitance values of MOS circuits

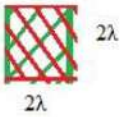
Layer	Value in pF X 10^{-4}/ µm^2 (Relative values in brackets)		
	5µm	Orbit	Orbit 1.2µm
Gate to channel	4	8	16
Diffusion	1	1.75	3.75
Poly-silicon to substrate	0.4	0.6	0.6
Metal 1 to substrate	0.3	0.33	0.33
Metal 2 to substrate	0.2	0.17	0.17
Metal 2 to metal 1	0.4	0.5	0.5
Metal 1 to poly silicon	0.3	0.3	0.3

Standard unit of capacitance □C_g

It is defined as the gate – to – channel capacitance of a MOS transistor having W = L. i.e., Standard Square as shown in figure. The unit is denoted by □C_g. □ C_g may be calculated for any MOS process as follows



Gate to channal capacitance



For 5μm MOS circuits

Area/standard square = 5μm X 5μm = 25 μm^2

Capacitance value = 4 X 10^{-4} pF/ μm^2

Thus standard value □cg = 25 μm^2 X 4 X 10^{-4} pF/ μm^2 = 0.01 pF

For 2μm MOS circuits

Area/standard square = 2μm X 2μm = 4 μm^2

Capacitance value = 8 X 10^{-4} pF/ μm^2

Thus, standard value □cg = 4 μm^2 X 8 X 10^{-4} pF/ μm^2 = 0.0032 pF

For 1.2μm MOS circuits

Area/standard square = 1.2μm X 1.2μm = 1.44 μm^2

Capacitance value = 16 X 10^{-4} pF/ μm^2

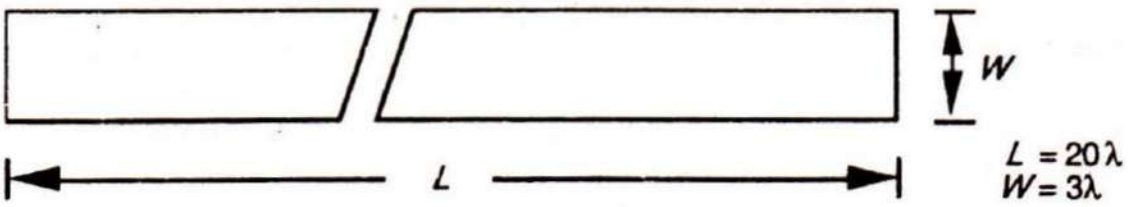
Thus, standard value □Cg = 1.44 μm^2 X 16 X 10^{-4} pF/ μm^2 = 0.0023 pF

SOME AREA CAPACITANCE CALCULATIONS

The approach will be demonstrated using λ based geometry. The calculation of capacitance values may now be undertaken by establishing the ratio between the area of interest and the area of standard (feature size square) gate (2 λ x 2 λ. for λ-based rules) and multiplying this ratio by the appropriate relative *C* value from Table. The product will give the required capacitance in $\square C_g$ units.

Calculate the area relative to that of a standard gate.

$$\text{Relative area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 15$$



1. Consider the area in metal 1.

Capacitance to substrate = relative area x relative *C* value

= 15 X 0.0750□C_g

= 1.125□Cg

That is, the defined area in metal has a capacitance to substrate 1.125 times that of a feature size square gate area.

2. Consider the same area in poly-silicon.

Capacitance to substrate = 15 x 0.1□Cg

= 1.5□Cg

3. Consider the same area in n-type diffusion.

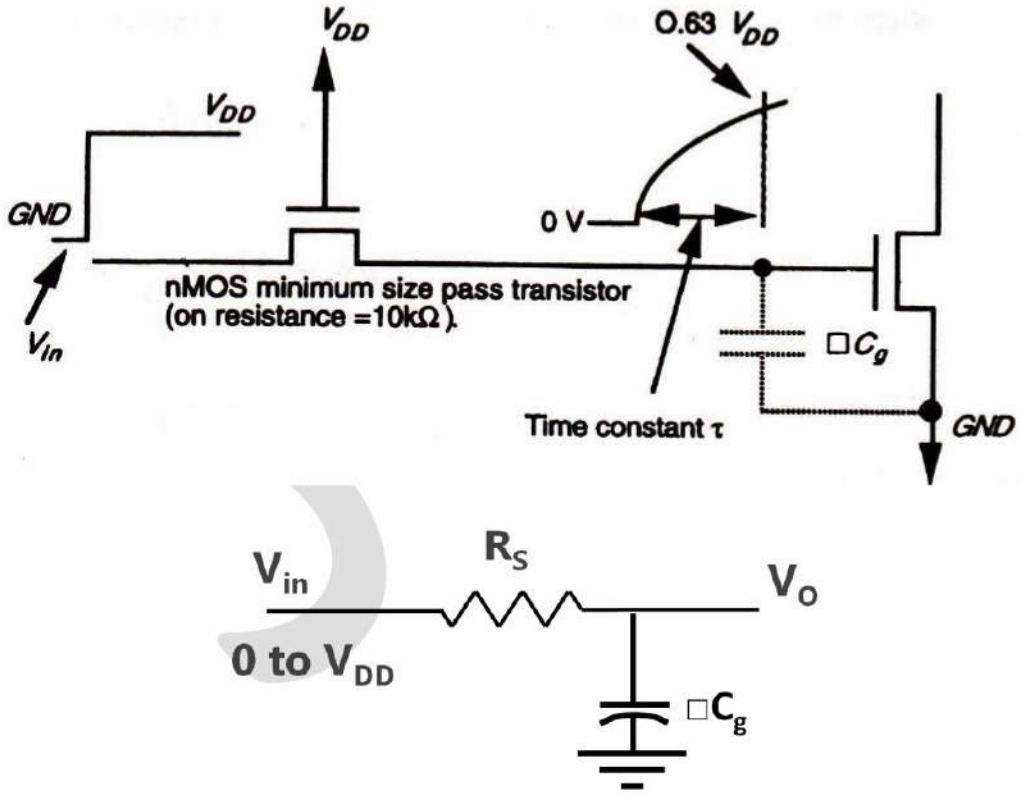
Capacitance to substrate = 15 x 0.25□Cg

= 3.75□Cg

Delay Unit (τ)

It is the time required to charge the capacitor through the resistor by 63% of the difference between initial and final value or discharging the capacitor to 37%.

Time constant **τ** =(1Rs (n channel) x □Cg) seconds



If we increase 0V to 5V at input, it takes some time to represent the same at output called delay time or time constant. Thus, τ is used as the fundamental time unit and all timings in a system can be assessed in relation to τ.

For 5µm MOS technology

$\tau = Rs \times \square C_g$

$= 10K\Omega \times 0.01PF$

$= 0.1$ nsec.

For 2µm MOS technology

$\tau = Rs \times \square C_g$

$= 20K\Omega \times 0.032PF$

$= 0.064$ nsec.

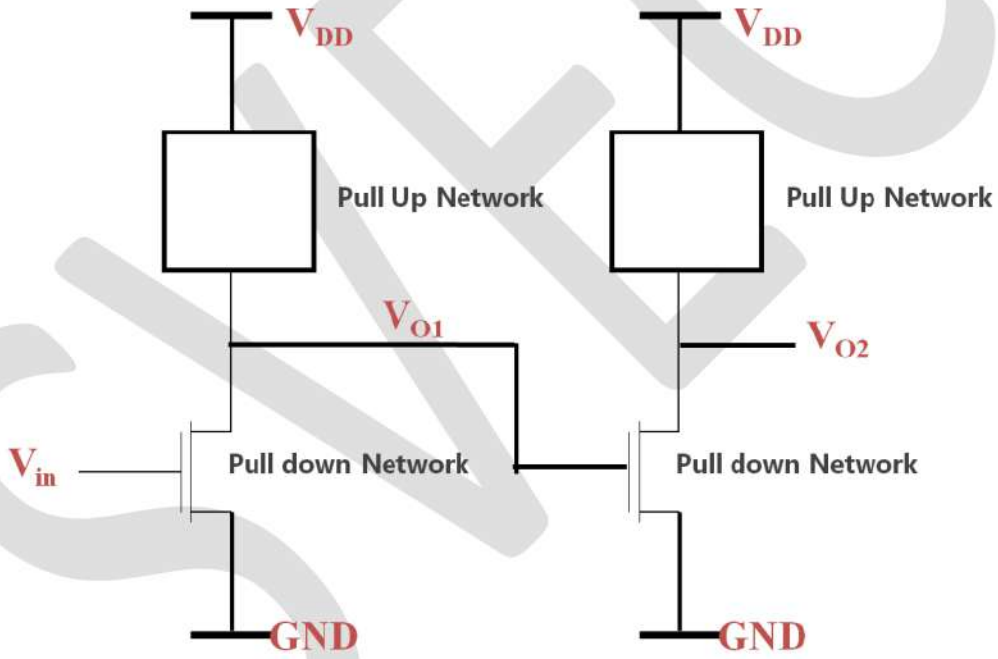
For 1.2µm MOS technology

$\tau = Rs \times \square C_g$

$= 20K\Omega \times 0.023PF$

$= 0.046$ nsec.

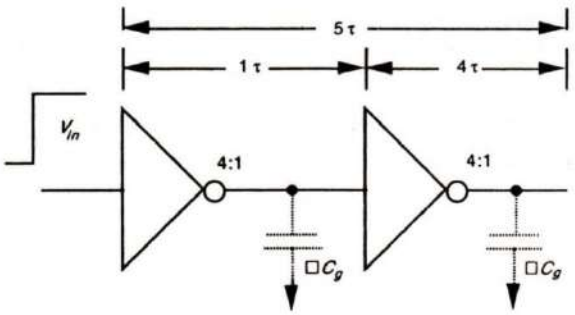
ANALYTIC INVERTER DELAYS



Consider the basic nMOS inverter has the channel length 8λ and width 2λ for pull-up transistor and channel length of 2λ and width 2λ for pull down transistor.

Hence the sheet resistance for pull-up transistor is $R_{p.u} = 4R_S = 40k\Omega$ and sheet resistance for pull-down transistor is $R_{p.d} = 1R_S = 10k\Omega$.

Since ($\tau = RC$) depends upon the values of R & C, the delay associates with the inverter depend up on whether it is being turned on (or) off. Now, consider a pair of cascaded inverters as shown in figure, and then the delay over the pair will be constant irrespective of the sense of the logic level transition of the input to the first.



nMOS Inverter Pair Delay

Note 1: When capacitor is charging, the current will flow to the capacitor to pull up device.

Note 2: When capacitor is discharging, current flows to pull down device.

Inverter 1(discharging) : Time constant $\tau_1=R_{p.d}\times\square C_g$

Inverter 2(charging) : Time constant $\tau_2=R_{p.u}\times\square C_g$

Total delay $\tau_d= \tau_1+ \tau_2$

Consider pull down device is standard NMOS, so it is having sheet resistance $R_{p.d}=R_s$

$$R_{p.u}=4\ R_{p.d}=4\ R_s$$

Total delay $\tau_d= \tau_1+ \tau_2$

$$=R_s\times\square C_g+4\ R_s\times\square C_g=5\ R_s\times\square C_g=5\ \tau$$

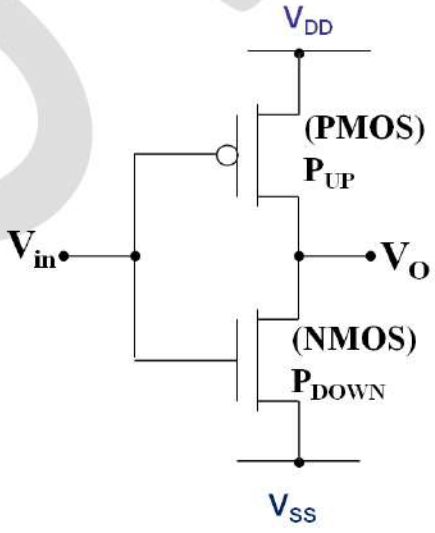
Thus, the inverter pair delay for inverters having 4:1 ration is 5τ.

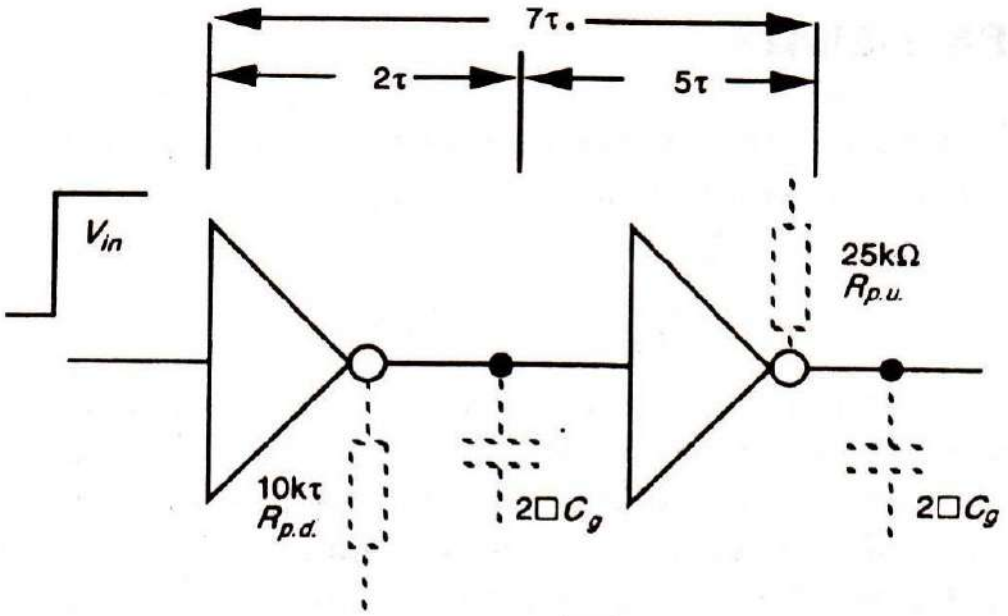
Hence, a single 4:1 inverter exhibits undesirable asymmetric delays, since the delay in turning ON is τ

And delay in turning OFF is 4τ.

CMOS inverter pair delay

When we consider CMOS inverters, the rules for nMOS inverters are not applicable. But we need to consider the natural (R_S) uneven values for equal size pull up p-transistor and the n-type pull down transistors.





Minimum size CMOS inverter Pair Delay

Figure shows the theoretical delay associated with a pair of both n and p transistors lambda based inverters. Here the gate capacitance is double comparable to nMOS inverter since the input to a CMOS inverter is connected to both transistor gate.

Inverter 1(discharging) : Time constant $\tau_1 = R_{p.d} \times 2\square C_g = R_n \times 2\square C_g$

Inverter 2(charging) : Time constant $\tau_2 = R_{p.u} \times 2\square C_g = R_p \times 2\square C_g$

For 5μm technology:

We know, NMOS sheet resistance $R_n = 10k\Omega$

PMOS sheet resistance $R_p = 25k\Omega$

$$R_p = 2.5\ R_n$$

Total delay $\tau_d = \tau_1 + \tau_2$

$= R_n \times 2\square C_g + R_p \times 2\square C_g$

$= R_n \times 2\square C_g + 2.5R_n \times 2\square C_g$

$= R_n \times 2\square C_g + 5R_n \times \square C_g$

$= 7\ R_n \square C_g$

Consider $\tau = R_n \square C_g$

$\tau_d = 7\ \tau$

DRIVING LARGE CAPACITIVE LOADS

When signals are propagated from the chip to off chip destinations we can face problems to drive large capacitive loads. Generally off chip capacitances may be several orders higher than on chip $\square C_g$ values.

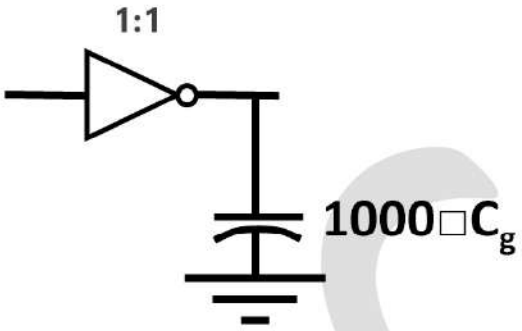
$C_L \geq 10^4\ \square C_g$

Where C_L denotes off-chip load. The capacitances which of this order must be driven through low resistances, otherwise excessively long delays will occur. Large capacitance is presented at the input, which in turn slows down the rate of change of voltage at input.

Cascaded Inverters with varying widths

Inverters to drive large capacitive loads must be present low pull-up and pull down resistance. For MOS circuits low resistance values imply low L:W ratio. Since length L cannot be reduced below the minimum feature size, the channels must be made very wide to reduce resistance value.

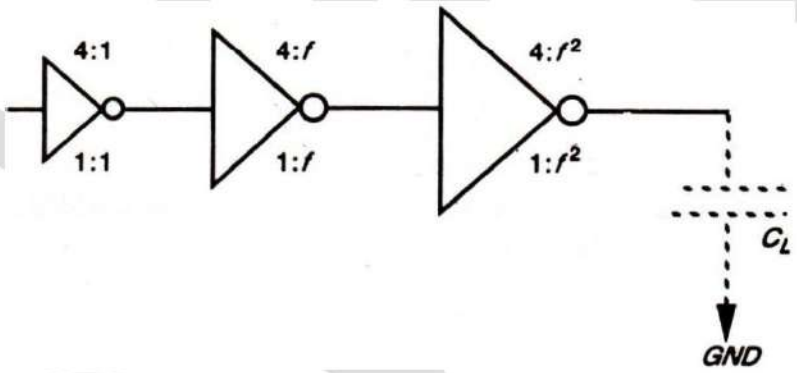
For example consider inverter with load capacitance is $1000\square C_g$



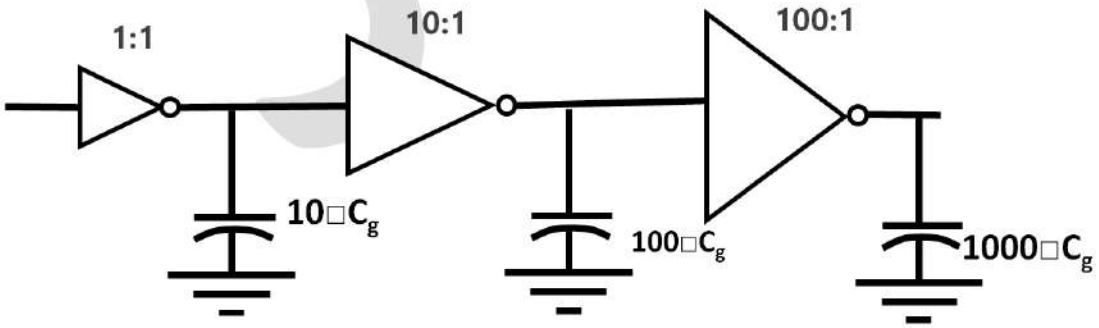
$$\tau_d = R_s \frac{L}{W} 1000\square Cg$$

$$\tau_d = R_s \frac{1}{1} 1000\square Cg = 1000\tau$$

Consider a inverters with varying widths



Driving Large Capacitance Loads



Calculation of delay for first inverter

$$\tau_1 = R_s \frac{L}{W} 10\square Cg$$

$$\tau_1 = R_s \frac{1}{1} 10\square Cg = 10\tau$$

Calculation of delay for second inverter

$$\tau_2 = R_s \frac{L}{W} 100\square Cg$$

$$\tau_2 = R_s \frac{1}{10} 100\square Cg = 10\tau$$

Calculation of delay for third inverter

$$\tau_3 = R_s \frac{L}{W} 1000\square Cg$$

$$\tau_3 = R_s \frac{1}{100} 1000\square Cg = 10\tau$$

Total delay $\tau_d = \tau_1 + \tau_2 + \tau_3 = 10\tau + 10\tau + 10\tau = 30\tau$

Super buffers

Generally the pull-up and the pull down transistors are not equally capable to drive capacitive loads. This asymmetry is avoided in super buffers. Basically, a super buffer is a symmetric inverting or non inverting driver that can supply (or) remove large currents and is nearly symmetrical in its ability to drive capacitive load. It can switch large capacitive loads than an inverter.

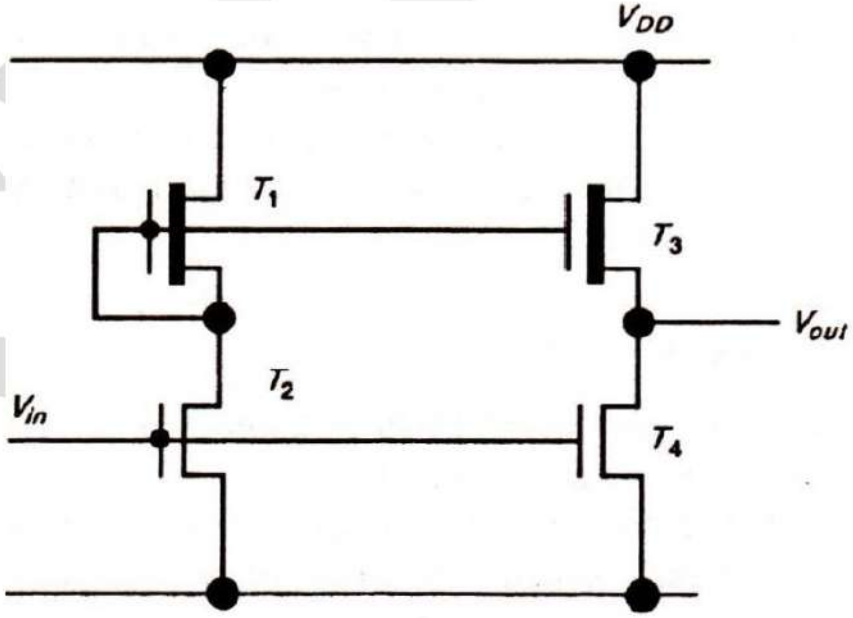
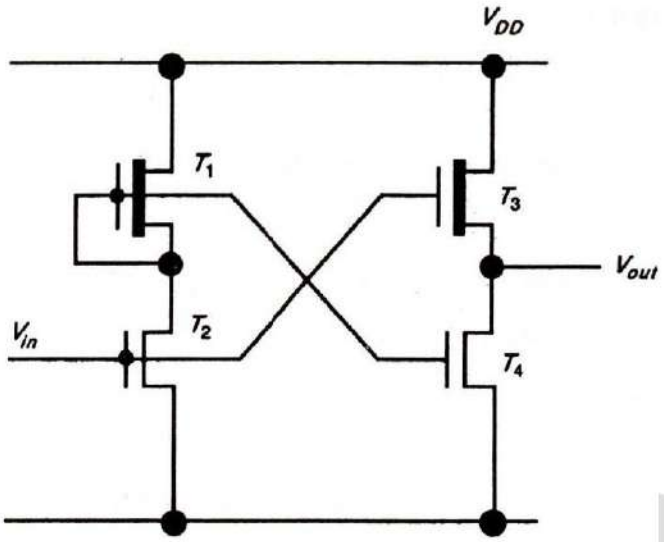


Figure: Inverting type nMOS super buffer

- Consider a positive going (0 to 1) transition at input V_{in} turns ON the inverter formed by T_1 and T_2.
- With a small delay, the gate of T_3 is pulled down to 0 volts. Thus, device T_3 is cut off. Since gate of T_4 is connected to V_{in}, it is turned ON and the output is pulled down very fast.
- For the opposite transition of V_{in} (1 to 0), V_{in} drops to 0 volts. The gate of transistor T_3 is allowed to rise to V_{DD} quickly.

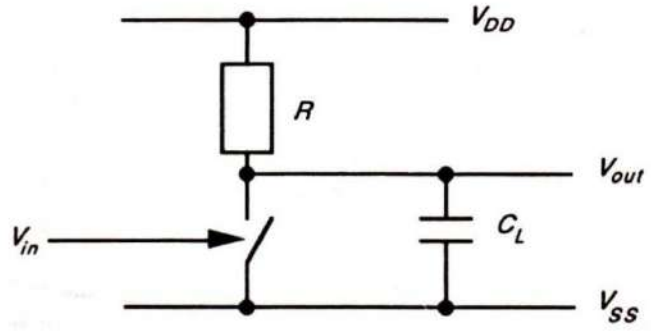
- Simultaneously the low V_{in} turns off T_4 very fast. This makes T_3 to conduct with its gate voltage approximately equal to V_{DD}.
- This gate voltage is twice the average voltage that would appear if the gate was connected to the source as in the conventional nMOS inverter.
- Now as $I_{ds}\alpha\ V_{gs}$, doubling the effective V_{gs} increases the current and there by reduces the delay in charging at the load capacitor of the output. The result is more symmetrical transition.



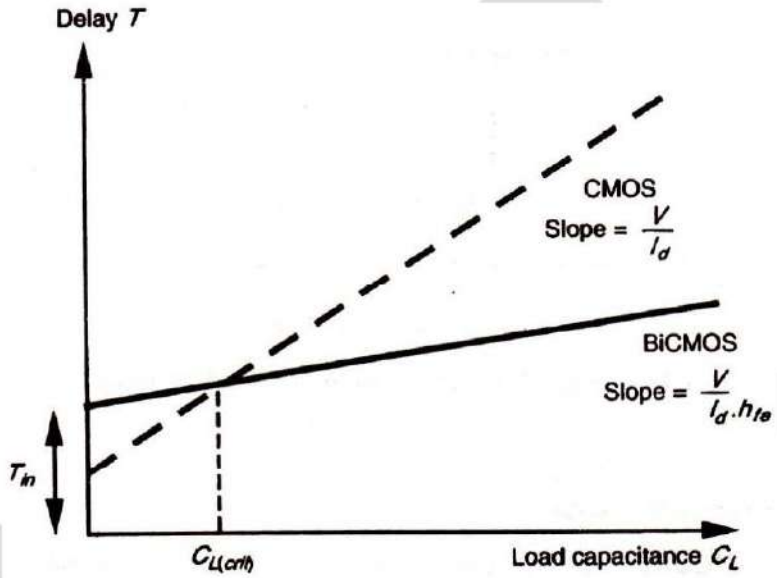
Non-Inverting type nMOS super buffer

Bi-CMOS drivers

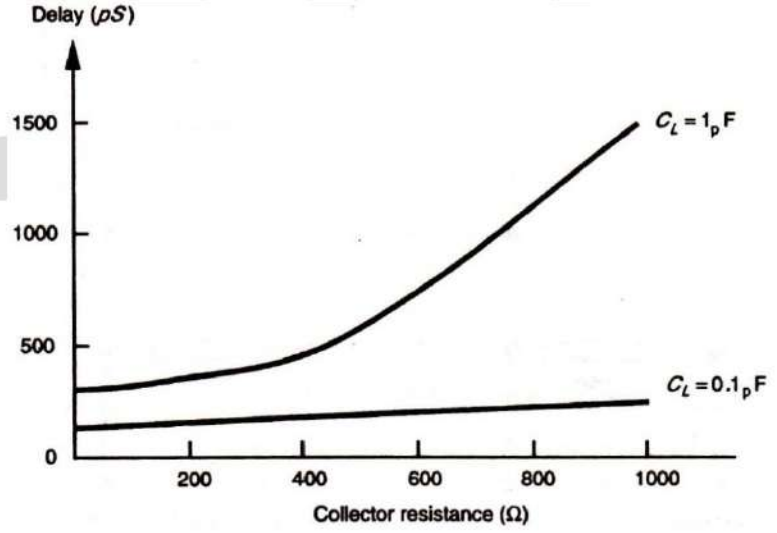
- In Bi-CMOS technology we use bipolar transistor drivers as the output stage of inverter and logic gate circuits.
- In bipolar transistors, there is an exponential dependence of the collector (output) current on the base to emitter (input) voltage V_{be} .
- Hence, the bipolar transistors can be operated with much smaller input voltage swings than MOS transistors and still switch large current.
- Another consideration in bipolar devices is that the temperature effect on input voltage V_{be}.
- In bipolar transistor, V_{be} is logarithmically dependent on collector current I_C and also other parameters such as base width, doping level, electron mobility.
- Now, the temperature differences across an I_C are not very high. Thus the V_{be} values of the bipolar devices spread over the chip remain same and do not differ by more than a few milli volts.
- The switching performance of a bipolar transistor driving a capacitive load can be analysed to begin with the help of equivalent circuit.



Driving ability of bipolar transistor



Delay Estimation



Gate delay as a function of collector resistance