NSCLDAQ-CAEN-DPP Testing results

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DPP-PHA testing results/updaates:

1. RC-CR2 smoothing
- Registers 0x1n54, tested over full range over all channels
- Changed CAENPha::setChannelParameters

2. Input rise time
- Registers 0x1n58, tested over full range over all channels
- Changed CAENPha::setChannelParameters

3. Record length
- Registers 0x1n20, tested over full range
- No changes needed

4. Dynamic range
0x1n28
- Tested for all channels
- No changes needed

5. DC Offset
0x1n98
- CompassProject::convertDCoffset assumes the variable ‘pct’ is signed, it isn’t
- The limit isn’t at 16383 but at 65535
- Also incorporated the change in sign needed when polarity is flipped
- With the changes made above, tested over full range over all channels

6. Channel enable/disable
- Random tests performed on channels being turned OFF/ON seem to work fine

7. NsBaseline
0x1080 : 20-22
- Added option to convertBaselineMeanCode() that included “..._FIXED” in addition to “..._NONE”. Compass uses both these in two different versions.
- Otherwise test over full range for all channels

8. DPP-Pretrigger
0x1n38
Manual says samples N=Ns/4t but what seemed to work was Ns/t

9. Polarity
0x1080 : 16
No change necessary

10. DPP Algo control
0x1080 : 0-5

- Had to be written after writing dppParams for it to work

11. Trigger HoldOff
0x1n74: 0-9
The right value seems to be 2*Trgholdoff_XML/m_nsPerTrigger

12. DPP Algo control
0x1080: 0-5

both shf and finegain had to be adjusted slightly, and are now defined as a case-by-case basis for 1725/30. It's awkward and could use fixing – but otherwise the regisers fully agree at this point.

13. Pole zero
0x1n68
No fix necessary

14. Tflat
0x1n60
No fix necessary

15. Trap rise time
0x1n5c
No fix necessary

16. Peak holdoff
0x1n78
Same fix as trigger holdoff

17. Set 811c's IOLevels from Compass XML

18. Compass writes 0xd0100 to 811c with trgout-trgin-auto

19. Start_Delay
0x8170
Had to change the written value to 2*(delay_XML)/m_nsPerTrigger for it to work

20. Flat Top Delay
0x1n64
No fix necessary

21. In addition, coincidence logic was handled separately from the present design, since the current design seems to use XML definitions from a previous version of Compass/Another CAEN daq

DPP-PSD

1. The per channel parameters were not being read correctly because the hierarchies in the XML file were different for global and per channel parameters as:

(GLOBAL)

parameters → entry
→ key
→ value
→ value

(PER CHANNEL)
channel → values
→ entry
→ key
→ value

This needed fixing in pugiutils.cpp, by defining getAllByName2()

2. In addition, we use the check

```
if(chan != -1)
    valNode = entry
```

so that all the getValue() calls look for the right hierarchy to extract the <values> tag in both global and perchannel cases.

3. Move algoControl register setup to **AFTER** SetDPPParameters()

4. Add polarity-based flipping to the definition of DCOffset
5. Record Length @ 0x1020
→ Tested OK over full range
6. Pre Trigger 0x1038
→ Full range, all channels OK
7. Polarity 0x1080 : 16
→ Full range, all channels OK
8. Ns Baseline 0x1080 : 20-22
→ Full range, all channels OK
9. Fixed baseline 0x1064
→ Had to be moved from before SetDPPParameters() to after
→ Full range + all channels OK
10. DC Offset 1098
→ Full range + all channels
11. InDyn 0x1028
→ OK + OK
12. Trigger thresh 0x1060
→ OK + OK
13. Disc mode 0x1080 bit 6

→ OK + OK

14. Enable/Disable channel ensured to work fine. Default values are written to disabled channels
15. Trigger holdoff 0x1074
    → Full range + all channels OK
16. CFD Delay 0x103c 0-7
    → Full range + all channels OK
17. CFD fraction
    → Full range + all channels OK
18. Change PSDParameters::setChannelCFDSmoothing() to have error condition as value<=0 || value > 16 (not >8)

19. Force 0x200 to 0x1084 so as to get fine timestamp + ext timestamp

20. Charge sensitivity 0x1080
21. Long gate 0x1058
22. Short gate 0x1054
23. Gate delay offset 0x105c

    All four parameters above work full range on all channels

24. Start delay 0x8170 matches

25. Timestamps are messed up, edit CDPpPsdEventSegment::oldestChannel()

Increment ‘adjust’ by 0x80000000 not 0x100000000
Change mask accordingly to get one less bit
i.e. choose lowest 31 bits and highest 33 bits. (Why does it work this way?)

General fixes to have first_trg startmode work:

If(startmode == firstTrigger and trgoutmode==software trigger) //This is how compass now stores trgout_trgin_auto
    send an additional start signal to begin acquisition

Add enums and checks for onboard coincidence mode: implement trgin_veto and trgin_gate

Added accelerator bindings to the tweaker.tcl code for XML file, allowing quicker Open, Save, Save As and Exit using keyboard shortcuts.

Manually set 0x1070 as either ‘c’ or ‘6’ based on board model as checked for using m_nsPerTick.