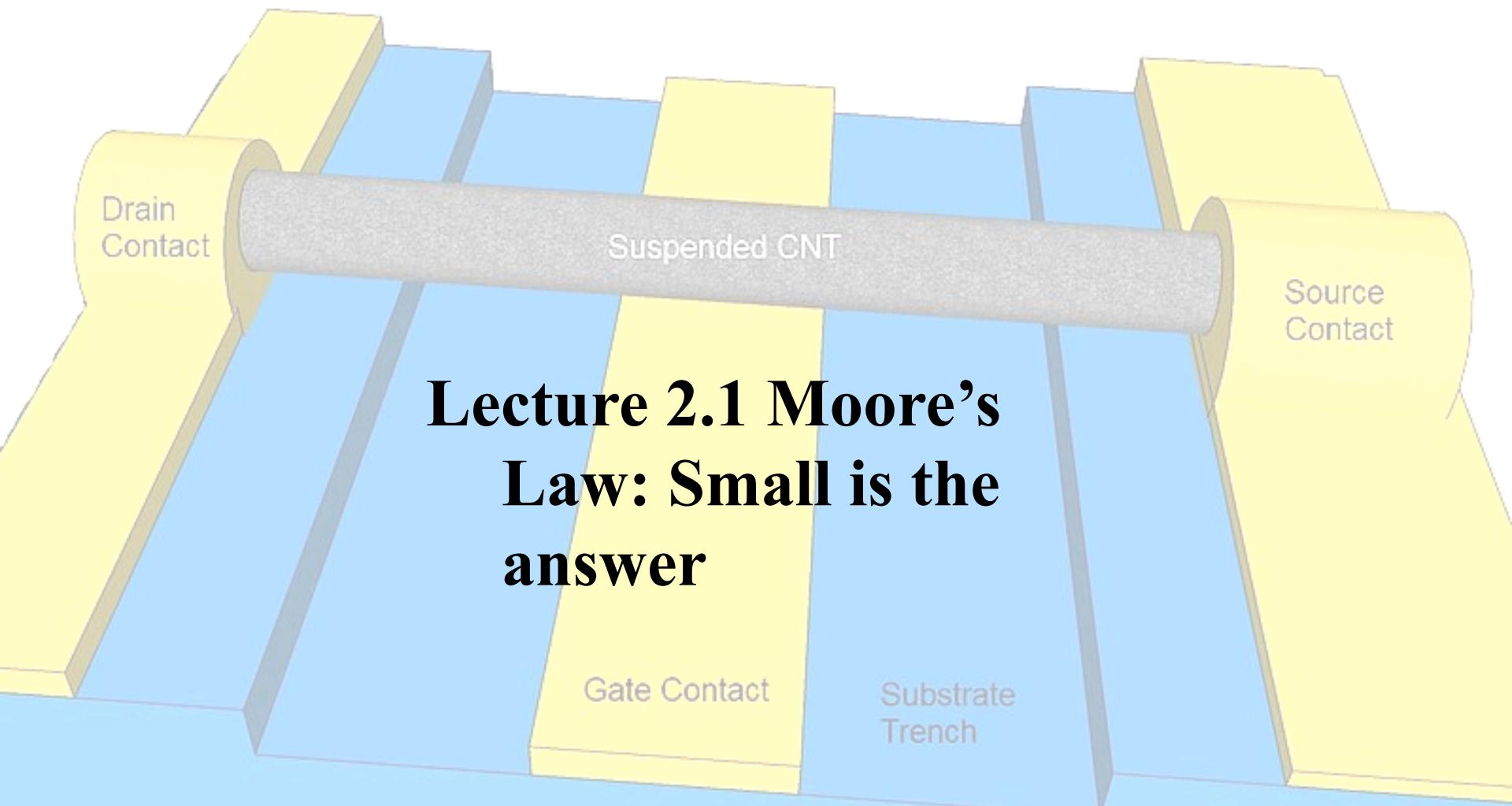
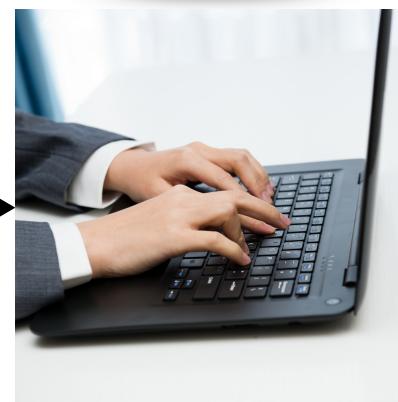


# Nano-Electronics



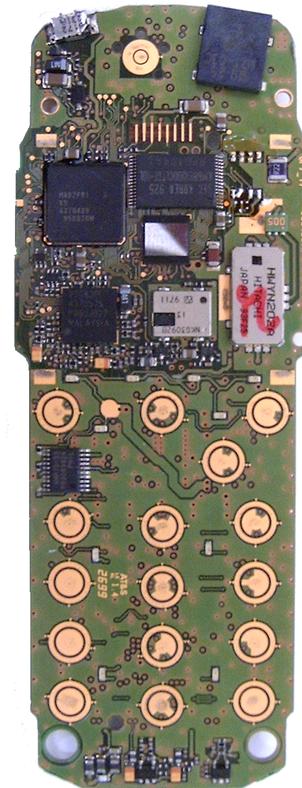
**Lecture 2.1 Moore's  
Law: Small is the  
answer**

# Better Electronics → Better Gadgets



1969 Data General Nova

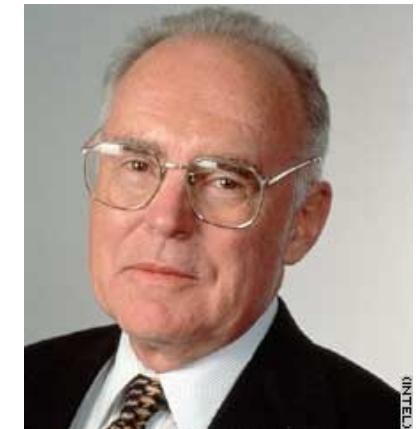
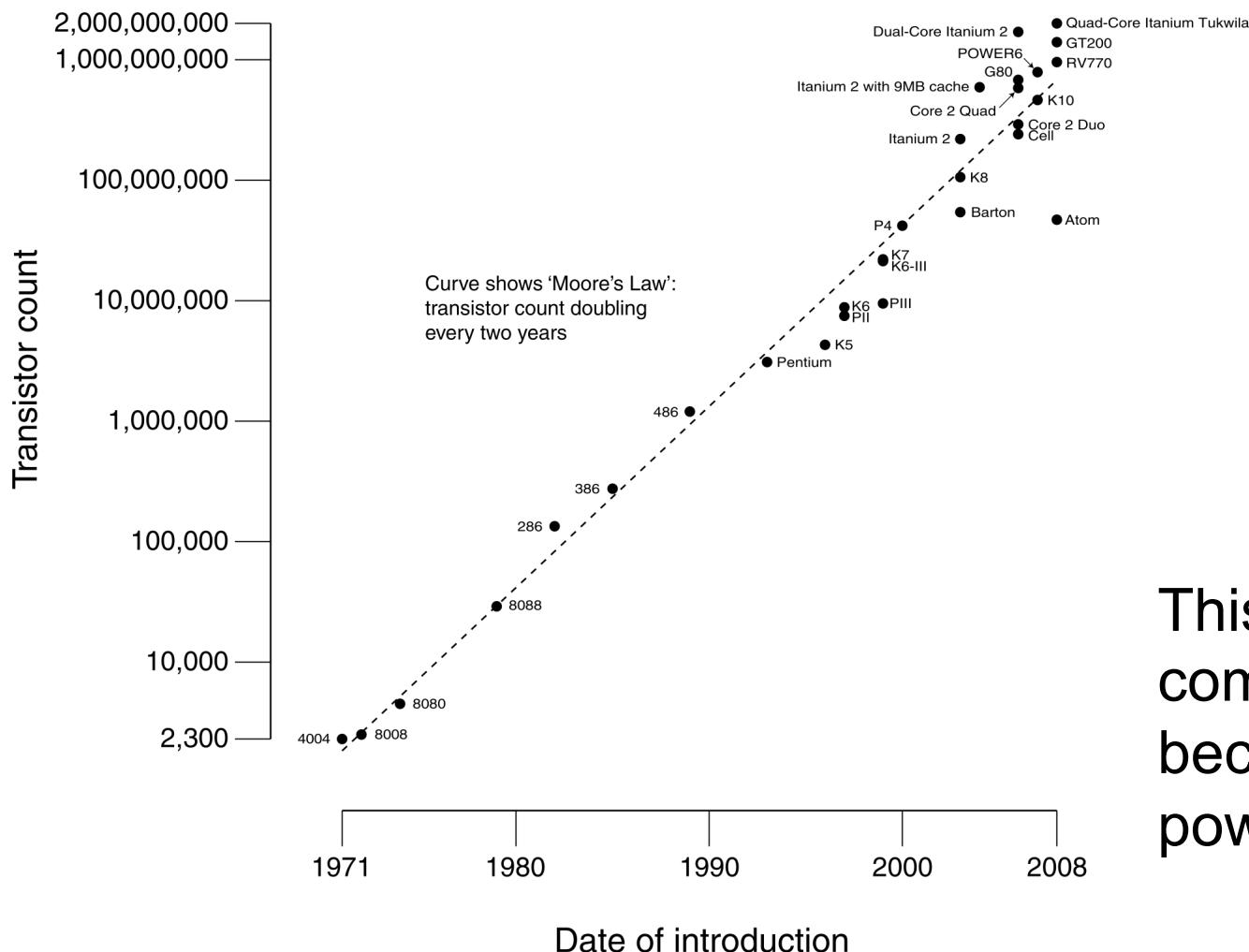
# Consumer Electronics Use Lots of Devices



**Electronic Devices are Inside Everything!**

# Moore's “Law”

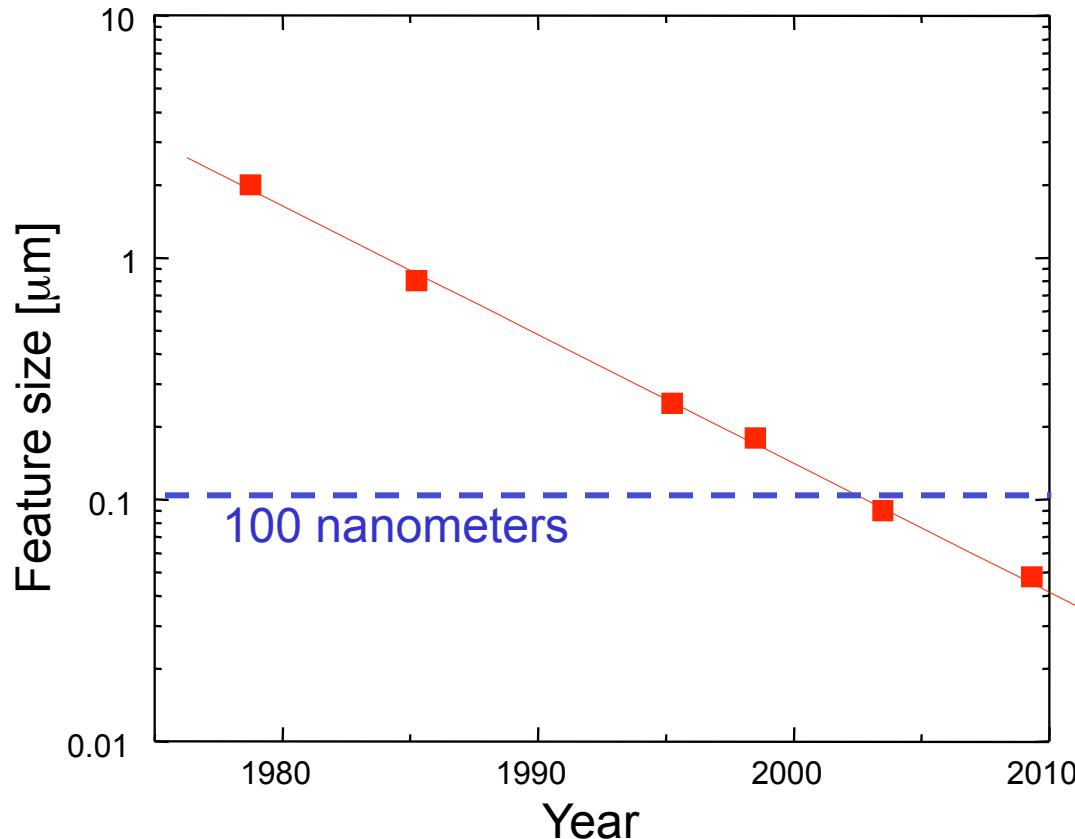
## More Devices in Processors



Gordon Moore

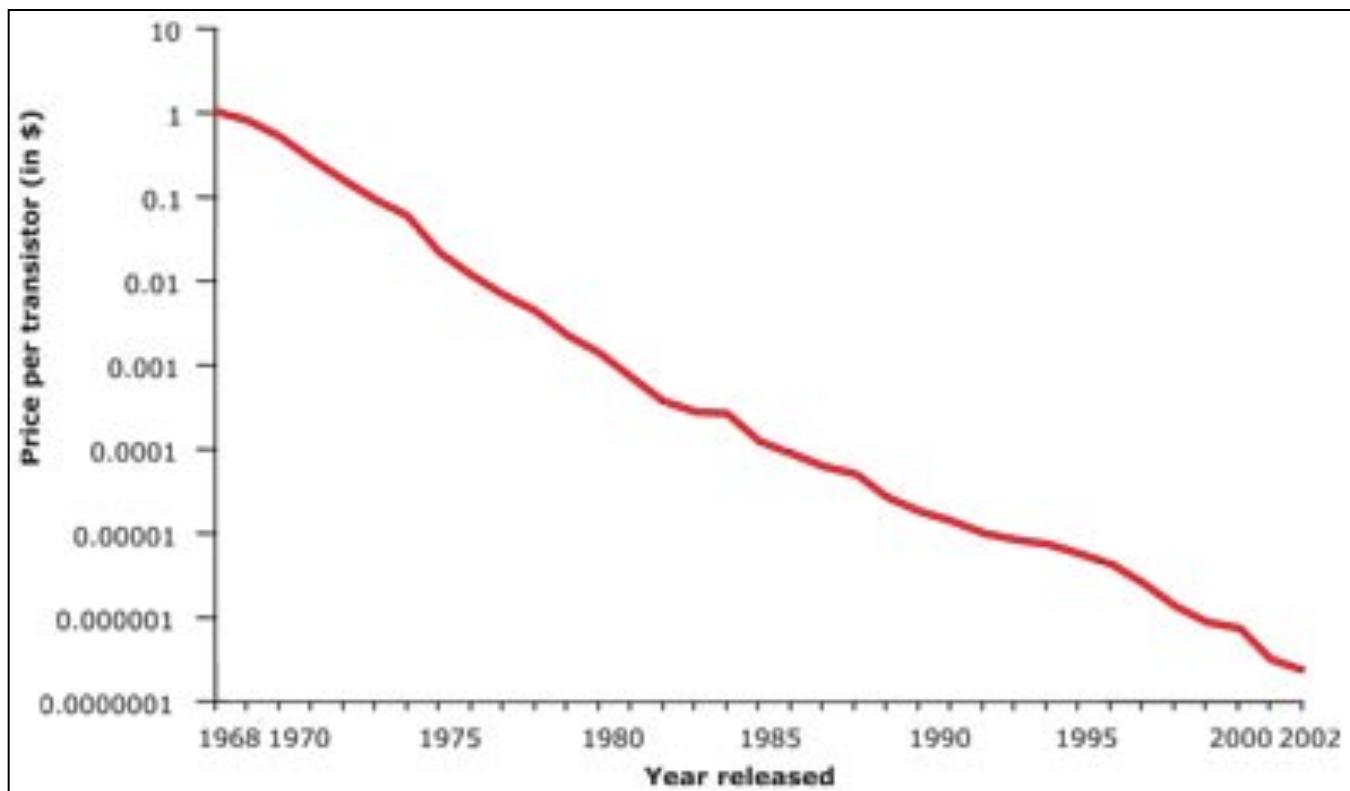
This trend is why computers have become more powerful every year.

# Moore's “Law” Size is Shrinking Too



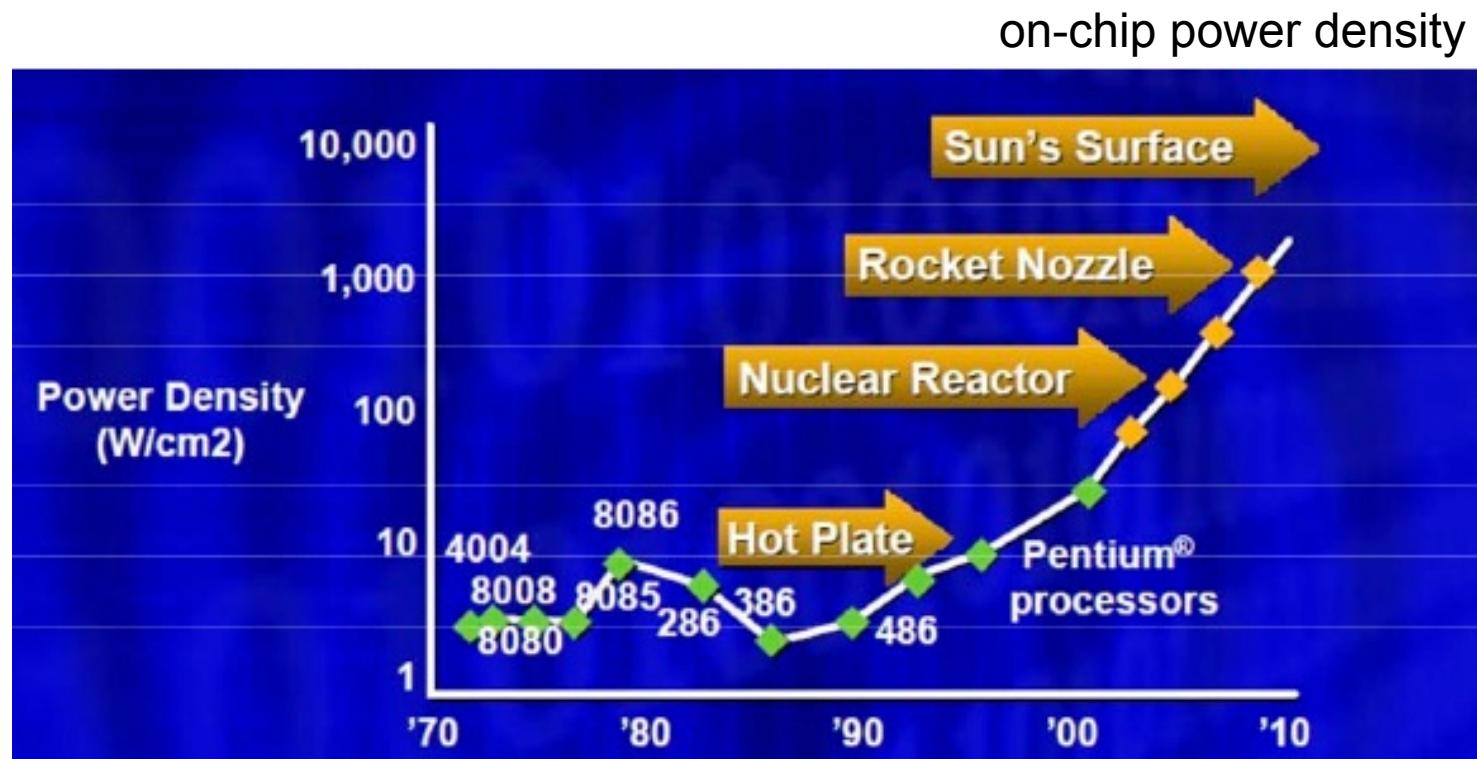
Just like the fruit – if you have more devices, must be smaller

# More of Moore: Small is CHEAP



Almost anything associated with computation  
is on an exponential evolutionary curve.

# More of Moore Small is HOT

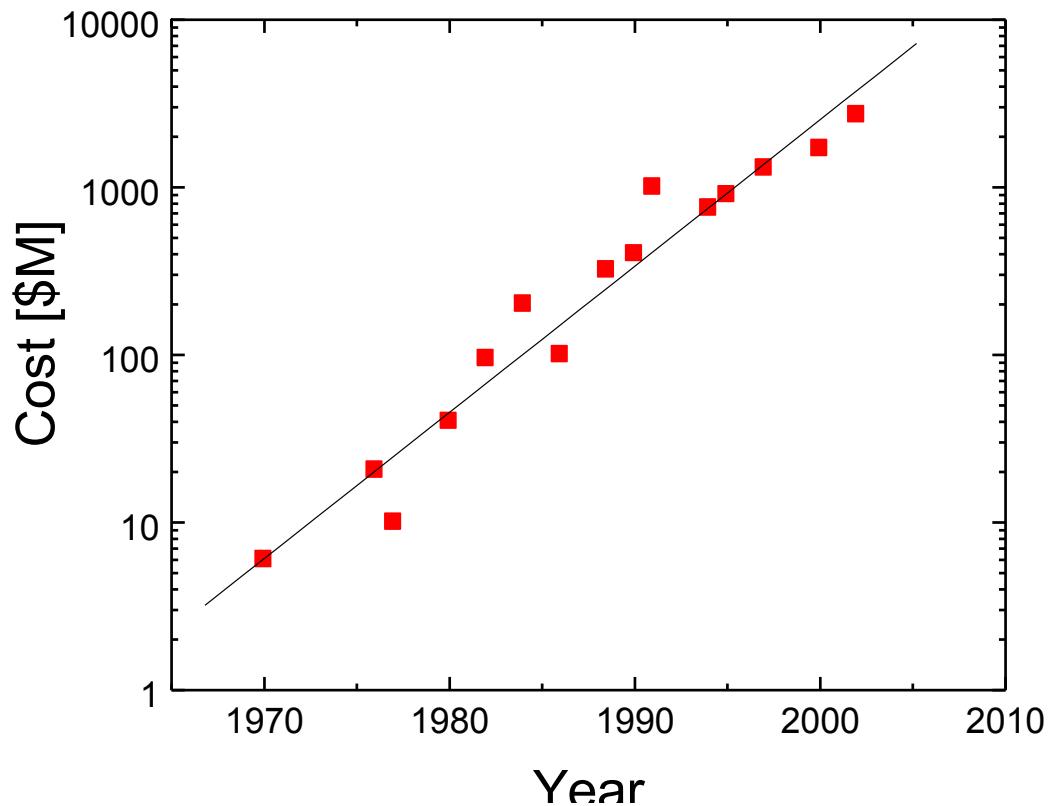


Intel VP Patrick Gelsinger (at ISSCC 2001) made a prediction:  
“If scaling continues at present pace, by 2005, high speed processors would have power density of nuclear reactor, by 2010, a rocket nozzle, and by 2015, surface of sun.”

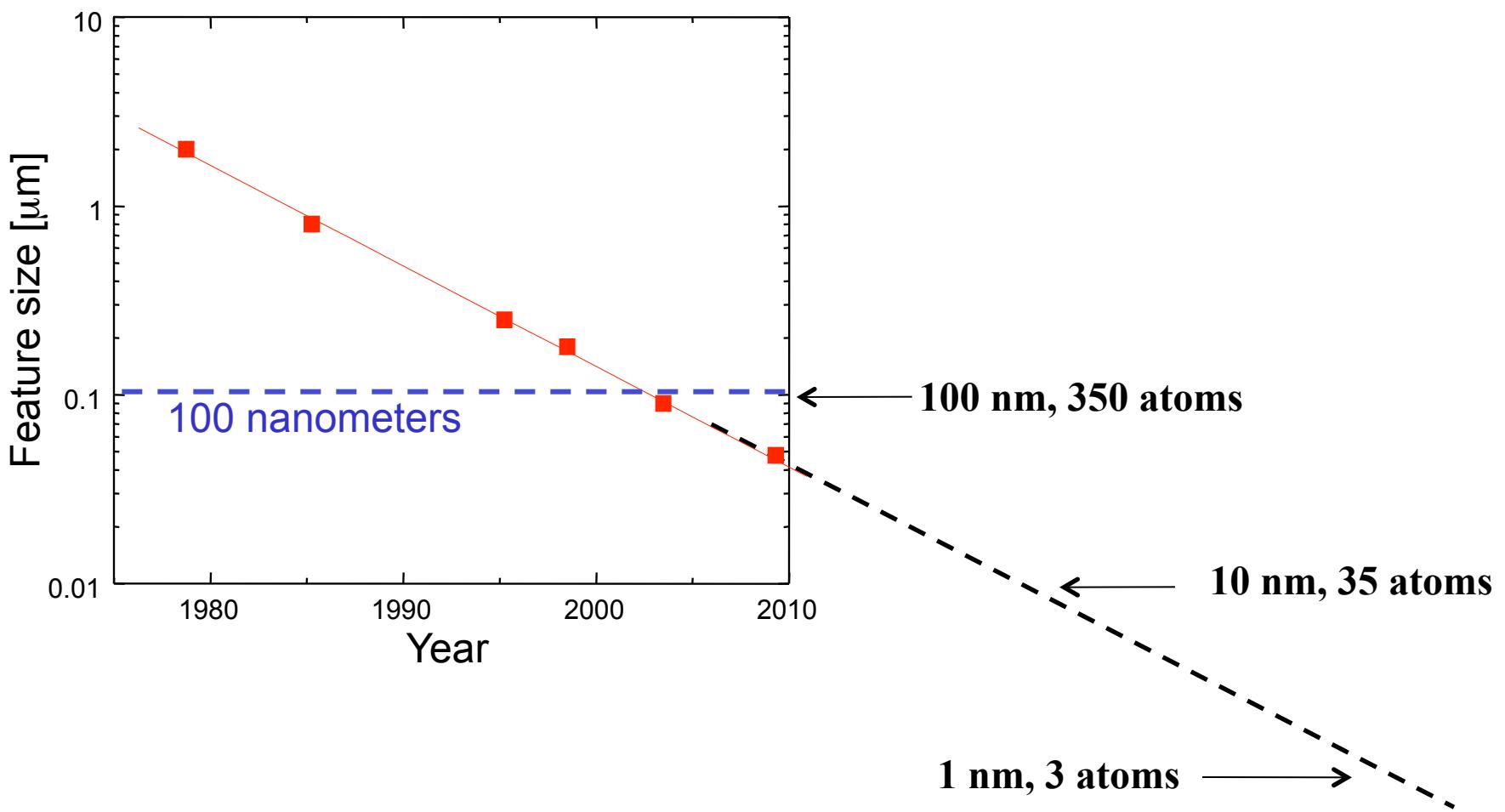
# More of Moore: Nanofactories are Expensive

The cost of a semiconductor production plant also shows an exponential trend.

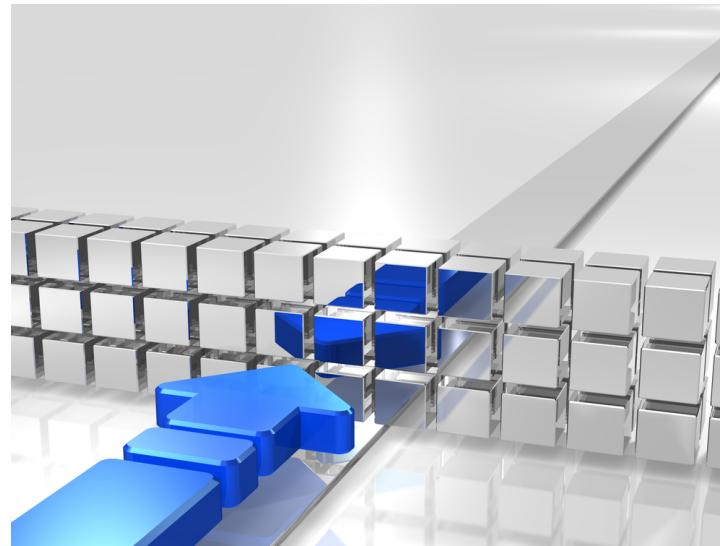
By 2025: \$1 Trillion



# More of Moore: We can't really stay on this trend forever

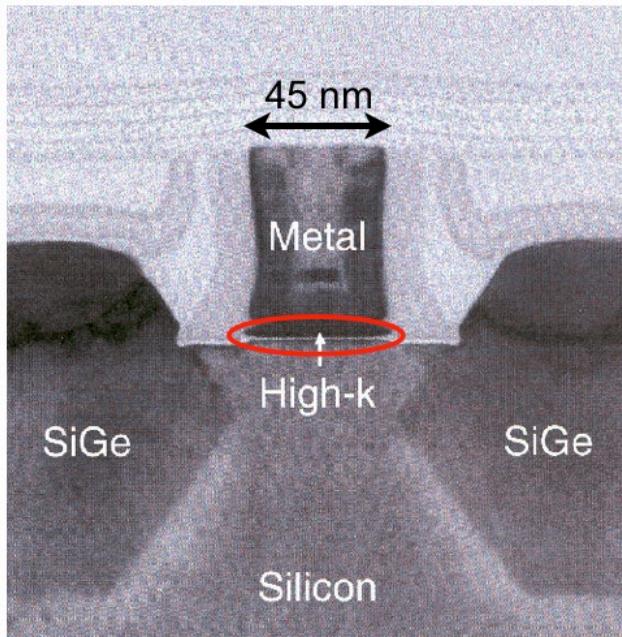


# A few of the Grand Challenges for the electronics industry



- Making nanotransistors smaller, reliably, and economically
- The wire (interconnects) – how to connect
- Managing heat with very dense transistors

# Is Nanotechnology the Answer?



Sohrab Ismail-Beigi, Yale University  
<http://volga.eng.yale.edu>

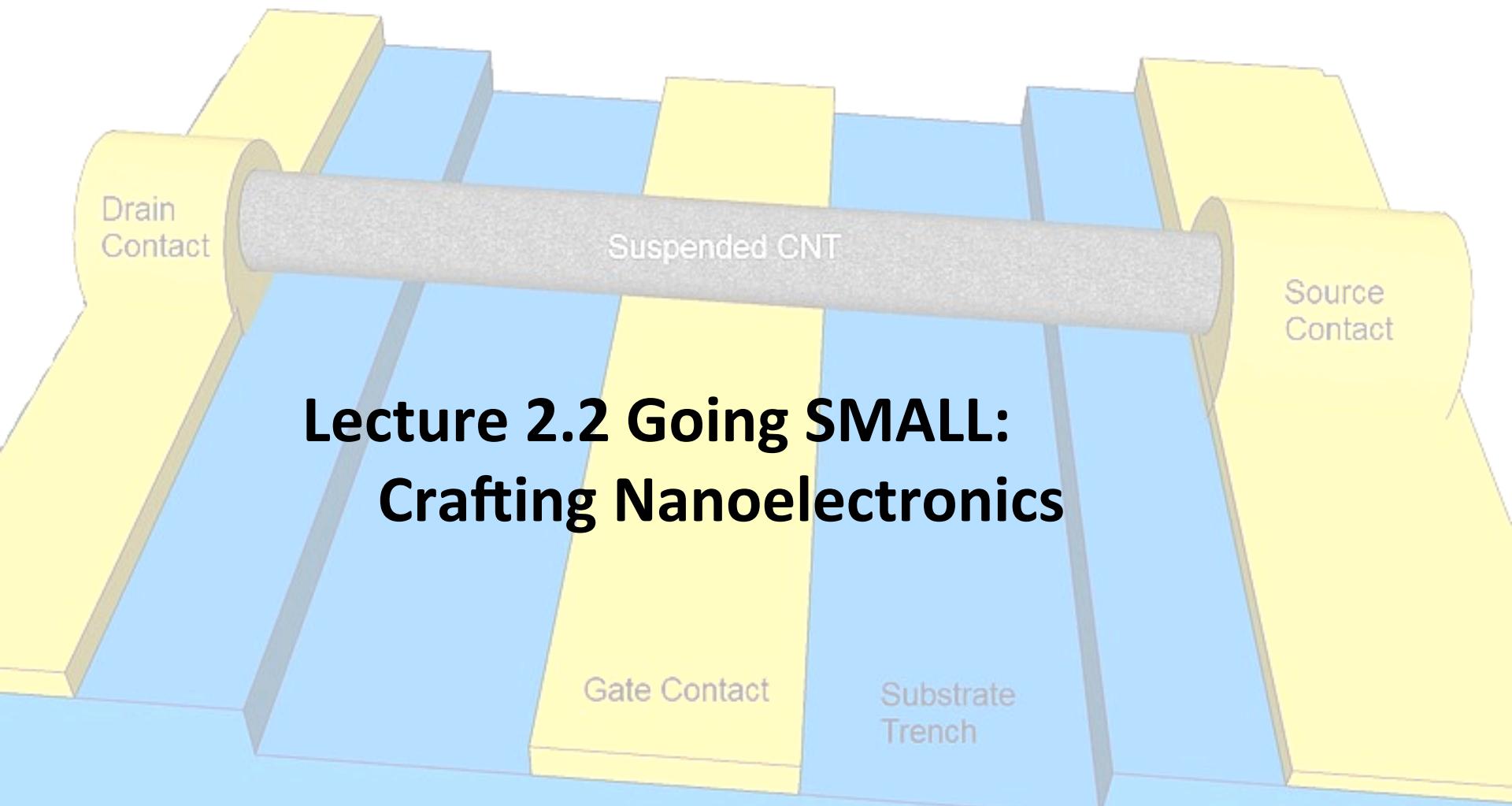


**Watch this week to figure out if it is, and how it might work**

# The ideas

- Electronic components have been getting better AND smaller over time
- Moore's Law – it's not really a law, but it's been true for a long time.
- What comes after Moore's Law?

# Nano-Electronics



## Lecture 2.2 Going SMALL: Crafting Nanoelectronics

# The Problem of the Nanoscale Penny

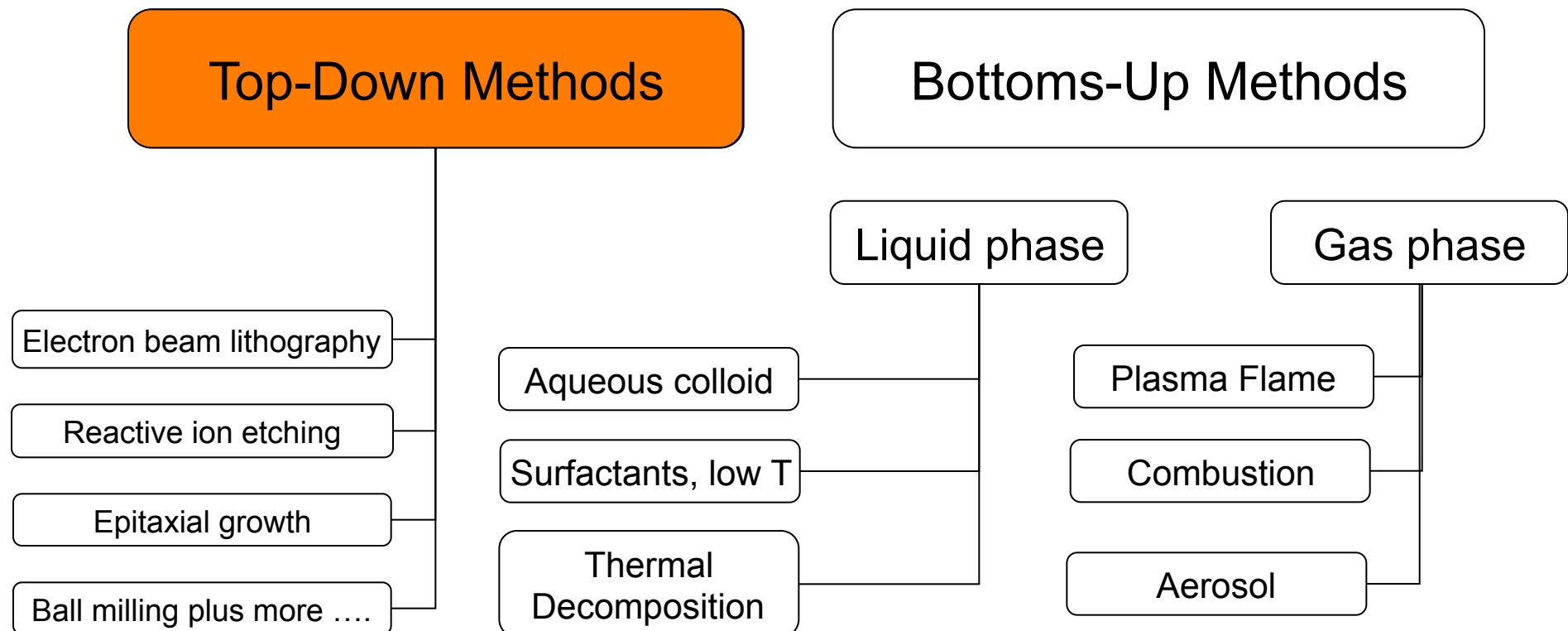


**10,000,000 times  
smaller**



**How would you approach this  
nanomanufacturing problem?**

# The semiconductor industry is all top-down



# A Top-Down Fabricator

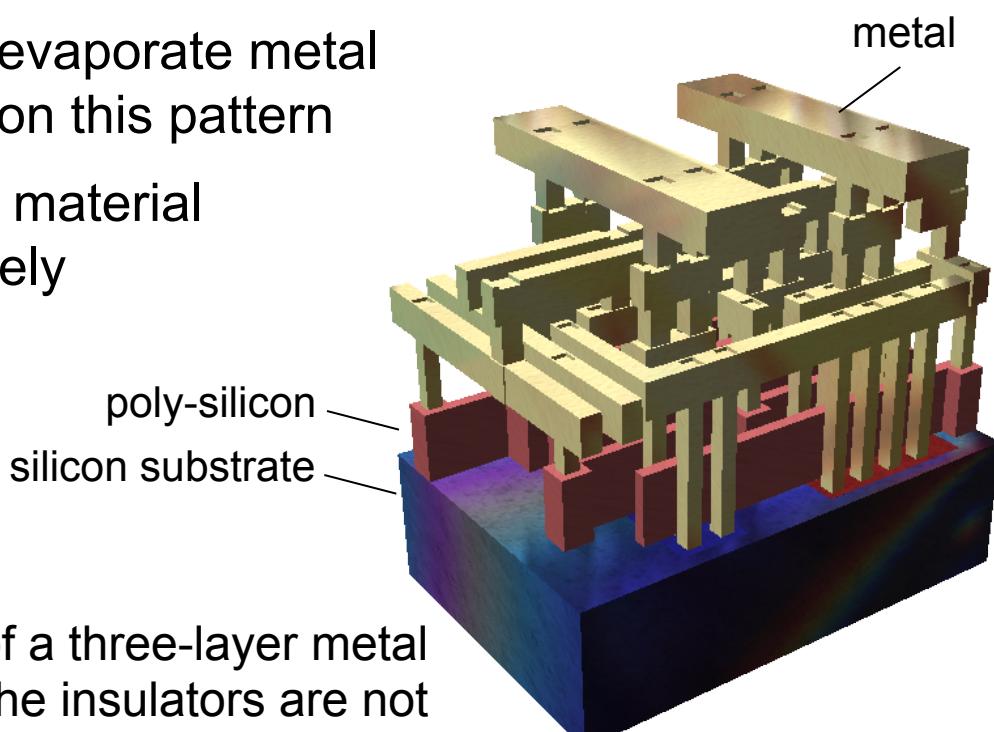


# Top-down fabrication relies on a three-step process

- imaging (i.e., lithography) → create a pattern on a surface, with nanoscale features
- deposition → evaporate metal on this pattern
- etching → remove material selectively

**Repeat as needed**

A 3D rendering of a three-layer metal structure on silicon (the insulators are not shown in this rendering)

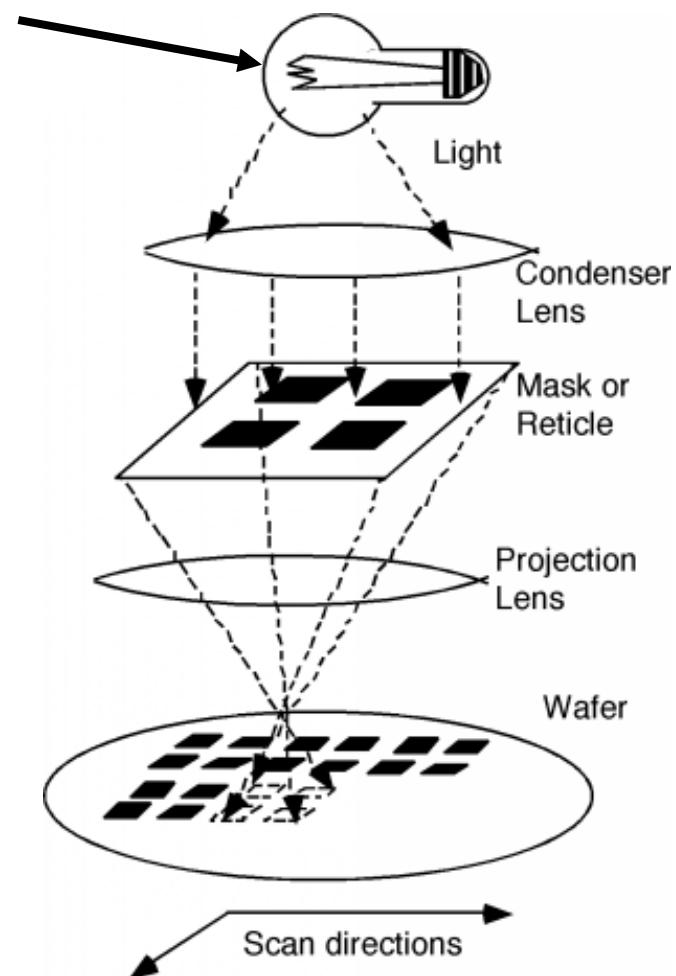


Source: Wikimedia Commons

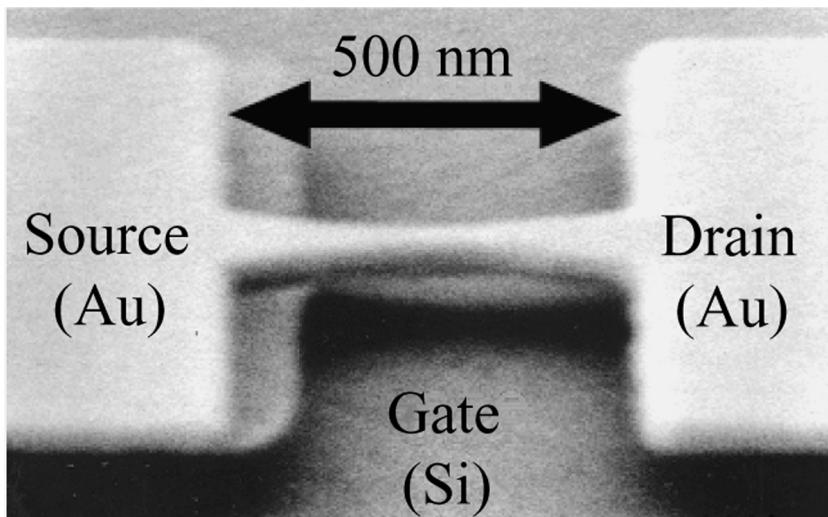
# Photolithography (1796 → Today)

**Key challenge: cannot make feature sizes much smaller than the wavelength of light!**

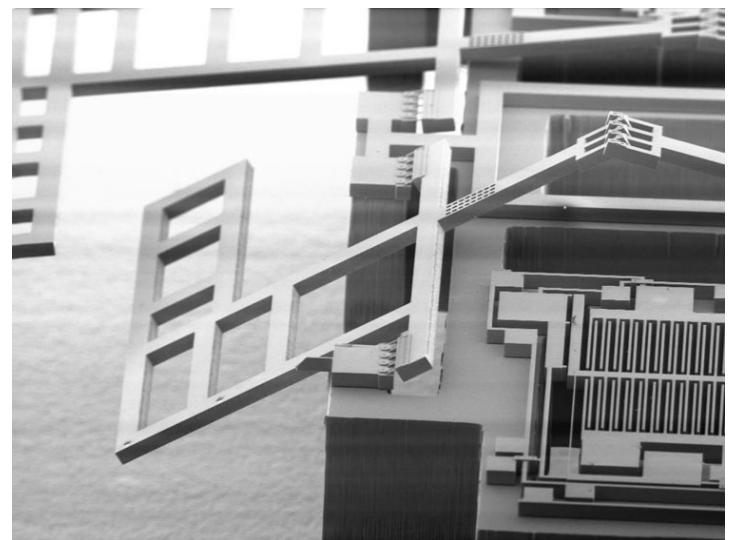
- Industry standard for semiconductor processing
- Currently: 193 nm ultraviolet light source
- With advanced techniques, capable of ~ 50 nm resolution in photoresist.
- Parallel technique, comparatively large areas.
- Limited by optics, properties of materials.



# Photolithography results



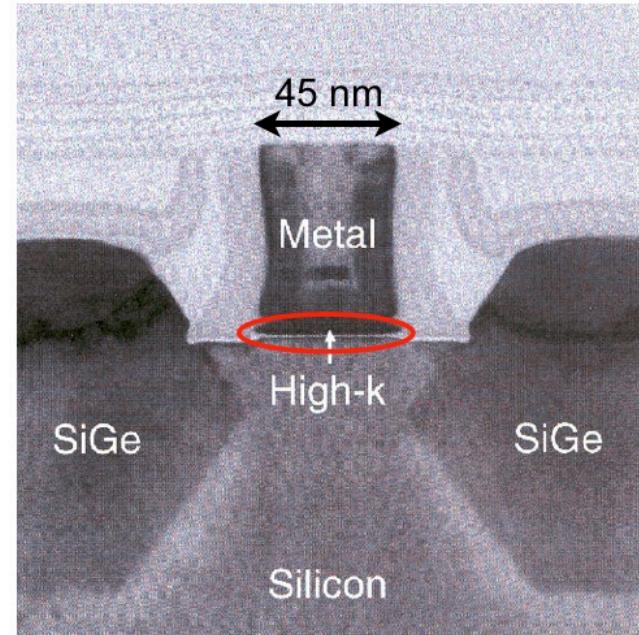
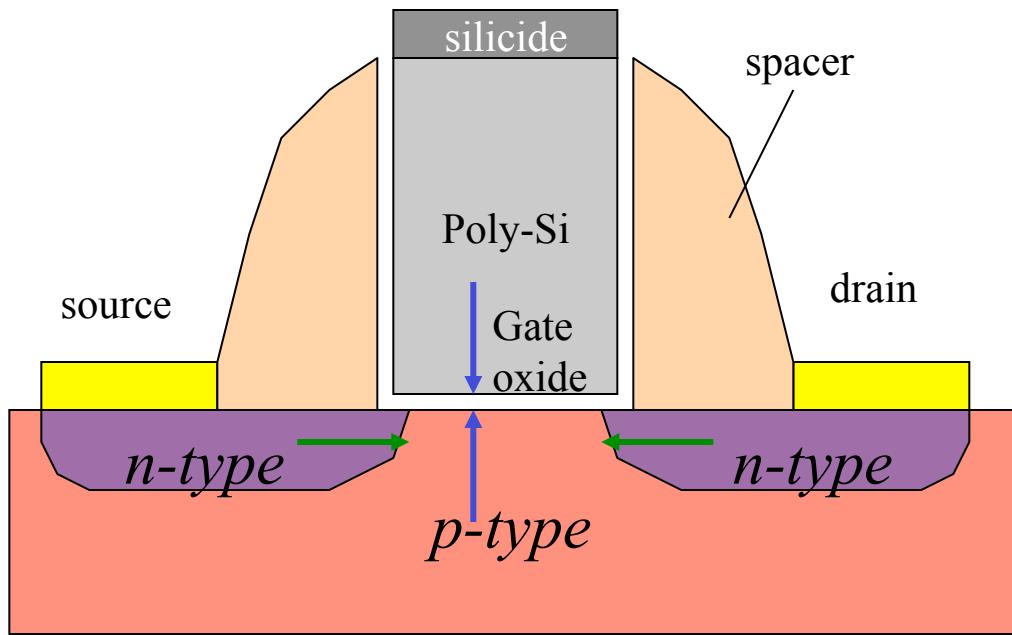
Dan Ralph, Cornell University  
<http://people.ccmr.cornell.edu/~ralph/index.html>



Kristofer Pister, UC Berkeley  
<http://robotics.eecs.berkeley.edu/~pister/>

Many impressive structures can be fabricated.

# State-of-the-art MOSFET



Sohrab Ismail-Beigi, Yale University  
<http://volga.eng.yale.edu>

Oxide thickness:  $\sim 1.8$  nm  
Channel length:  $\sim 65$  nm

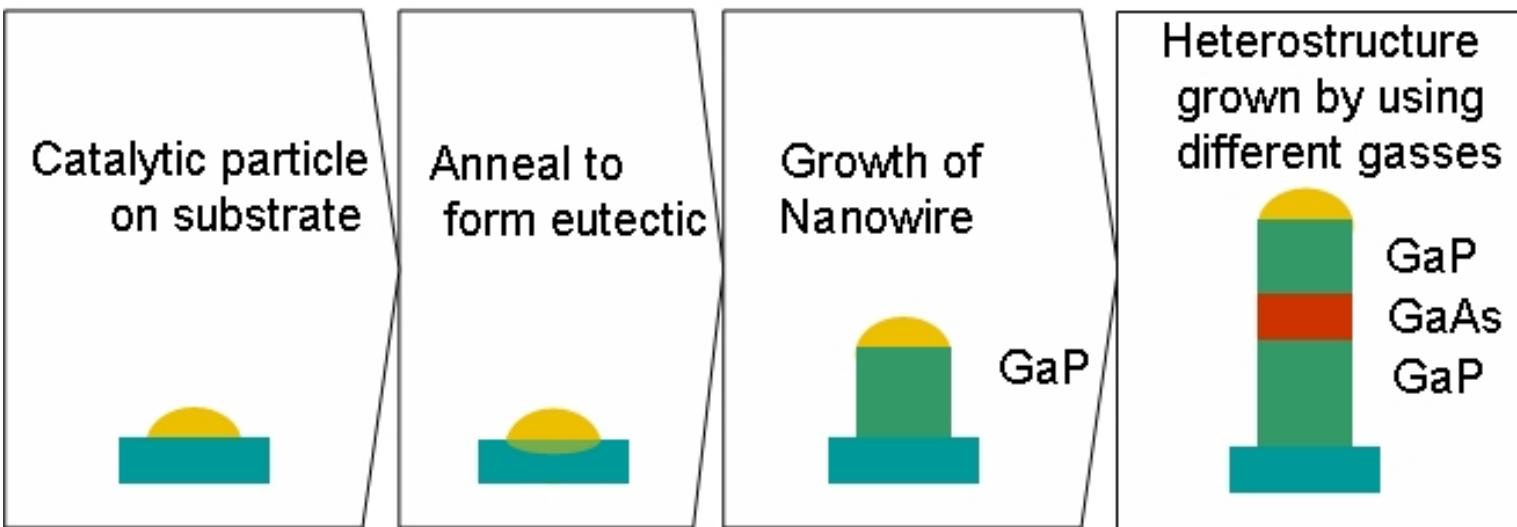
Gate position:  $\sim 6$  nm (!)  
Characteristic time:  $\sim 0.86$  ps

# A Bottoms-Up Synthesis



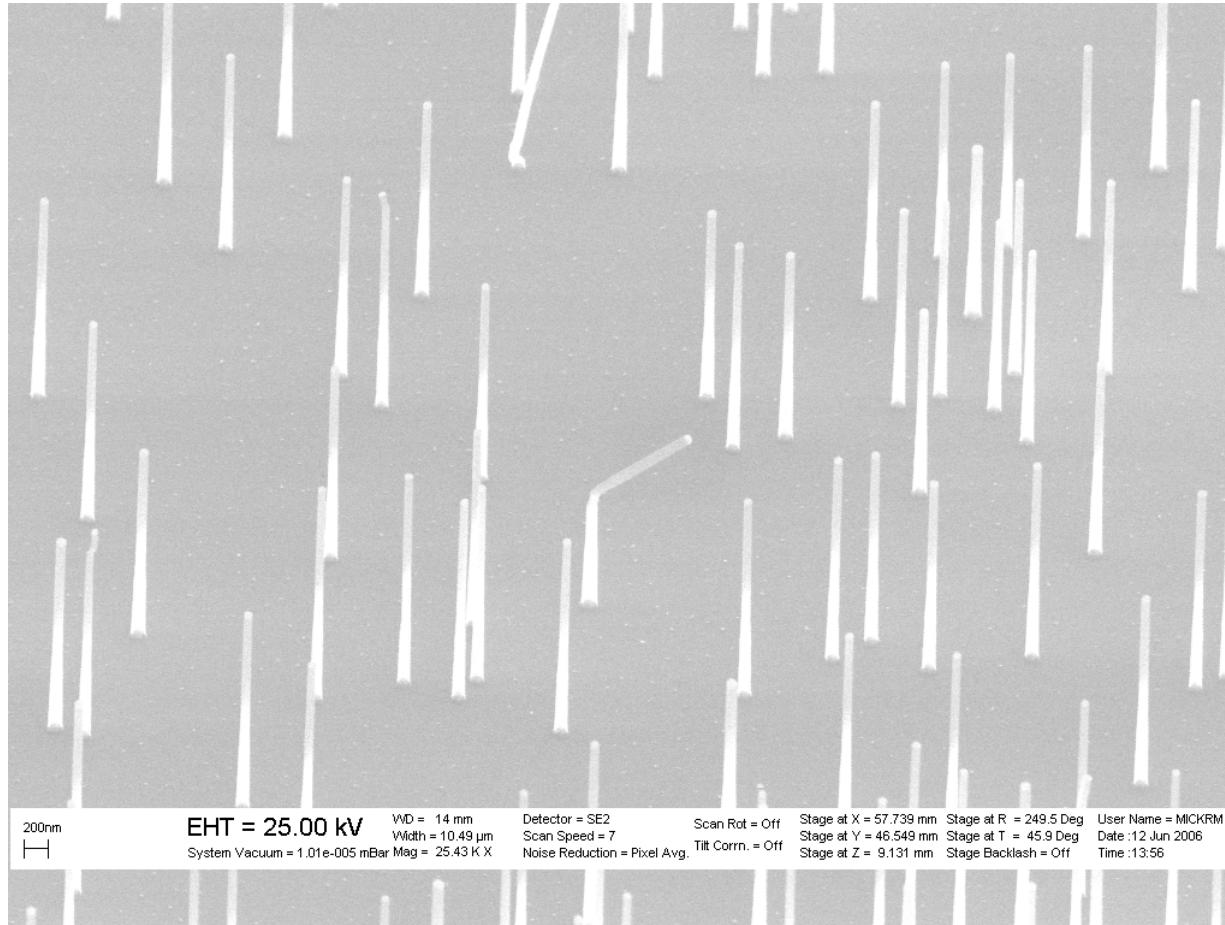
# Gas Phase/Chemical Synthesis

The epitaxial nanowire heterostructure growth process



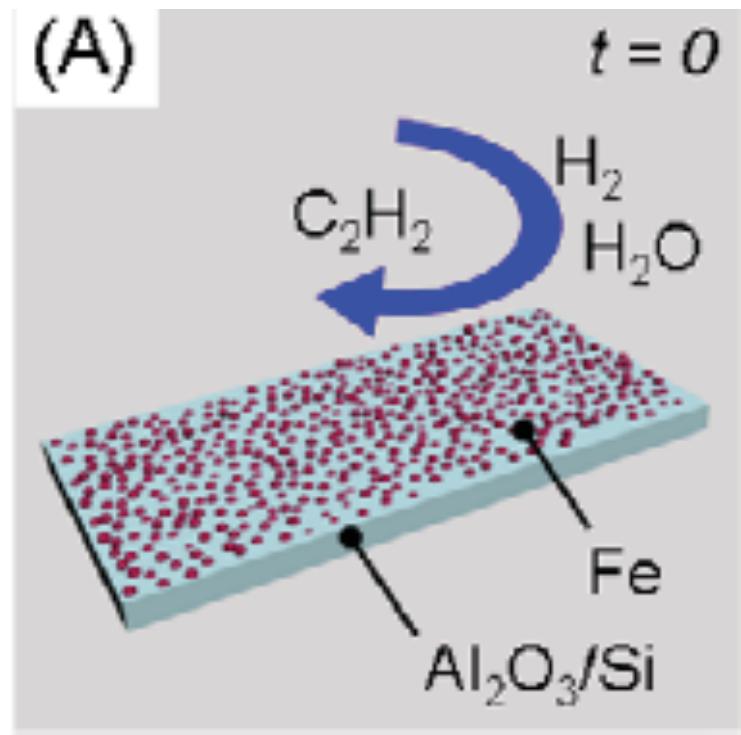
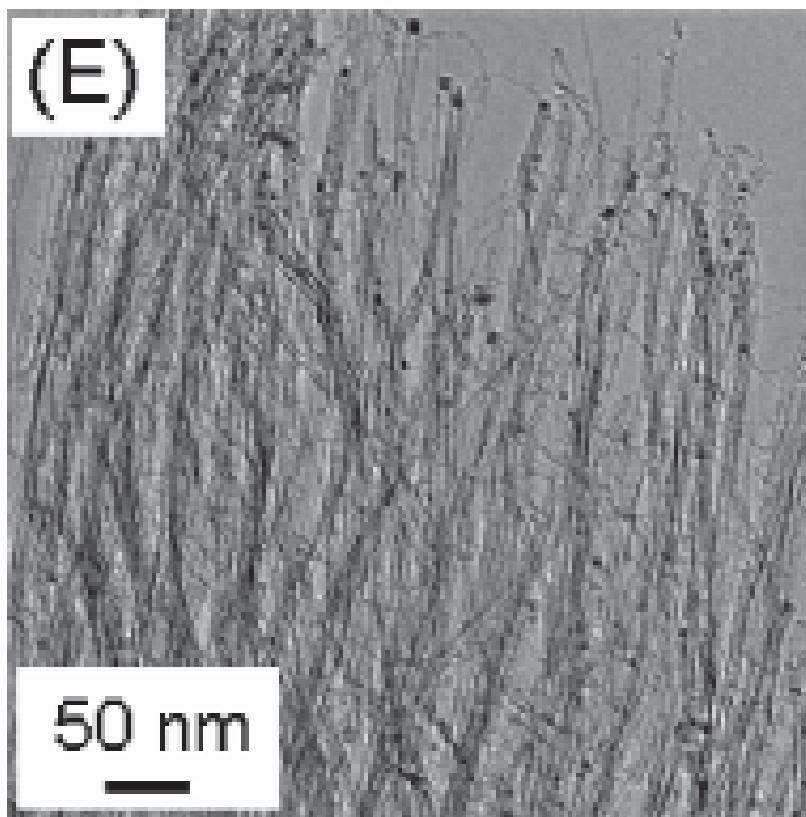
Open Source Handbook of Nanoscience and Nanotechnology, Molhave

# Semiconductor Nanowires



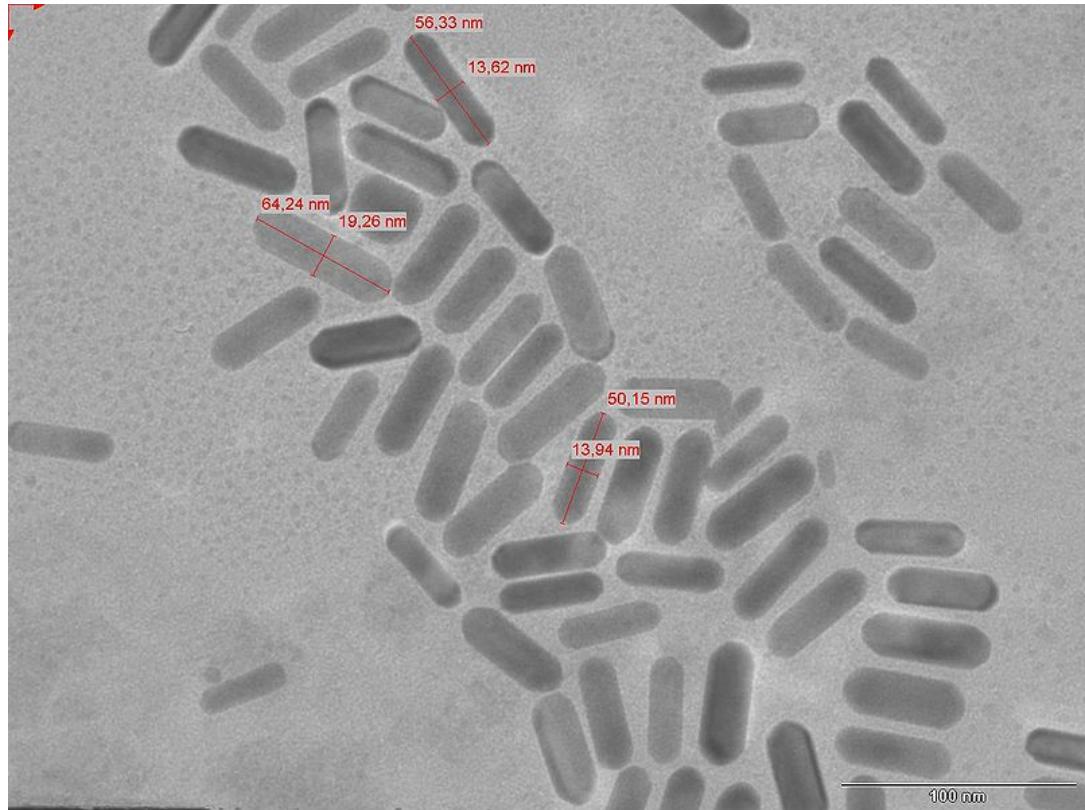
Open Source Handbook of Nanoscience and Nanotechnology, Molhave

# Carbon Nanotube Carpets



■ Courtesy of the Colvin Lab, Seung Soo Lee ■

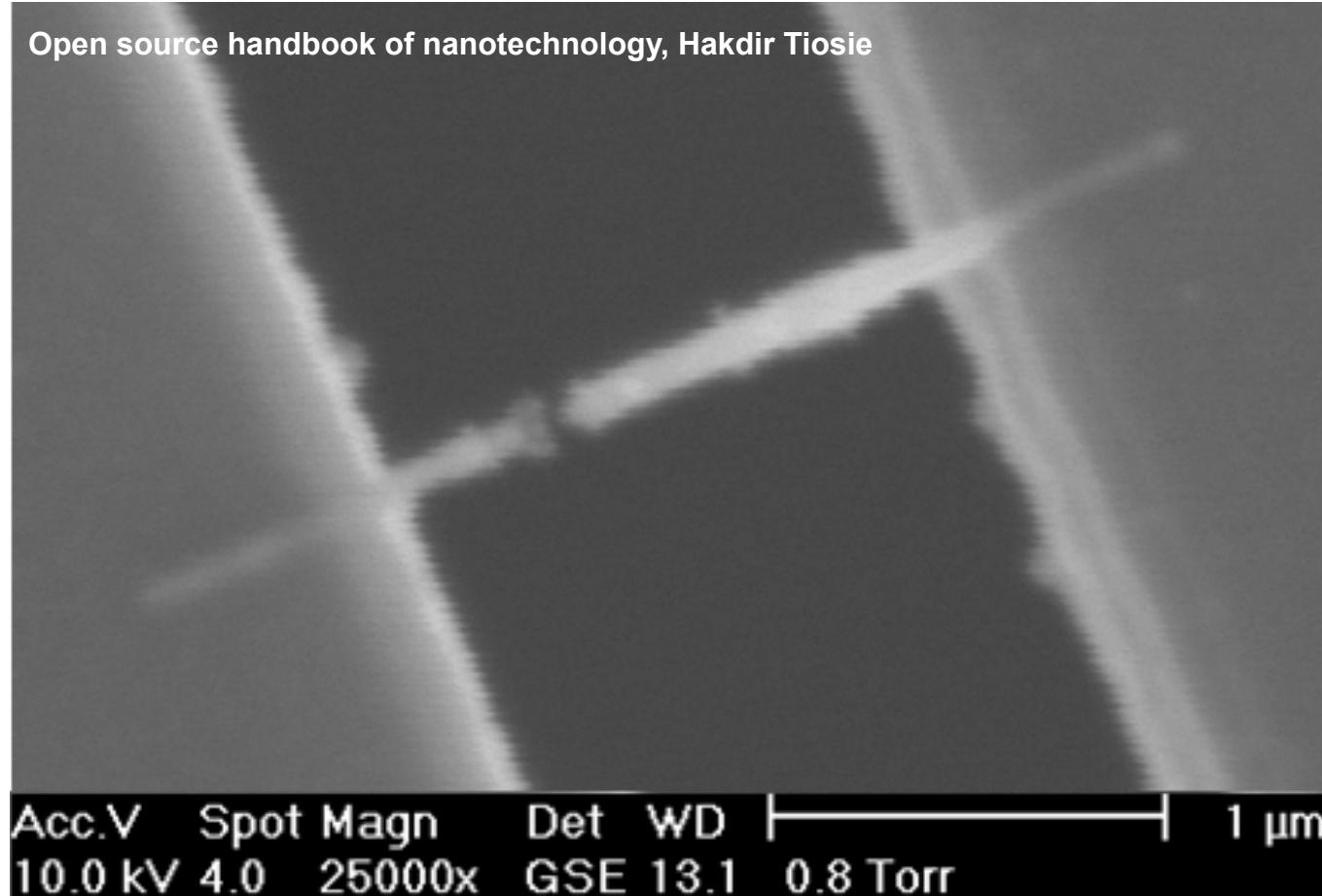
# Metallic Nanowires: All Solution Phase



Creative Commons 3.0 from Grossman, 2006

# The Wiring Problem: A Fried Nanowire

Open source handbook of nanotechnology, Hakdir Tiosie

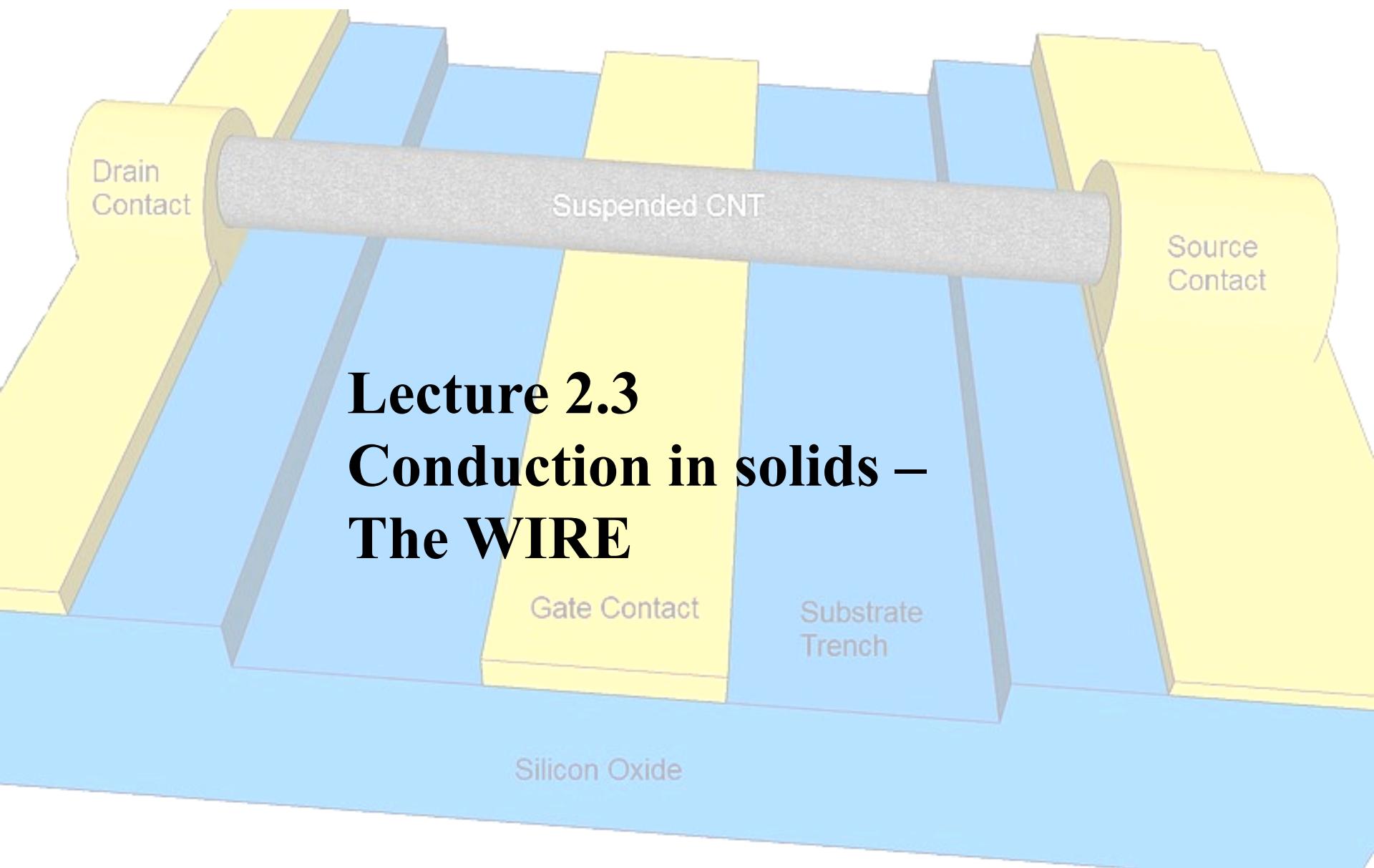


Acc.V   Spot Magn   Det   WD   |————|   1 μm  
10.0 kV 4.0 25000x GSE 13.1 0.8 Torr

# The ideas

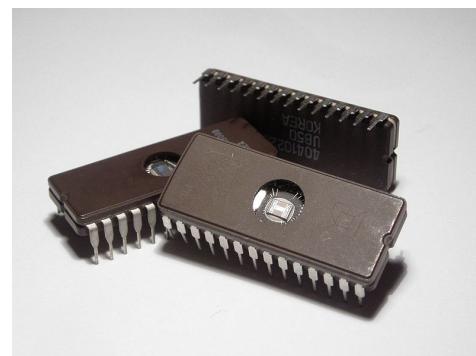
- Lithography: the primary tool for fabricating small (planar) structures → Peters out on nanometer scale
- Chemical Synthesis: naturally good at making small structures, but how do you wire?
- Scalability, cost: key questions for staying on Moore's Law

# Nano-Electronics

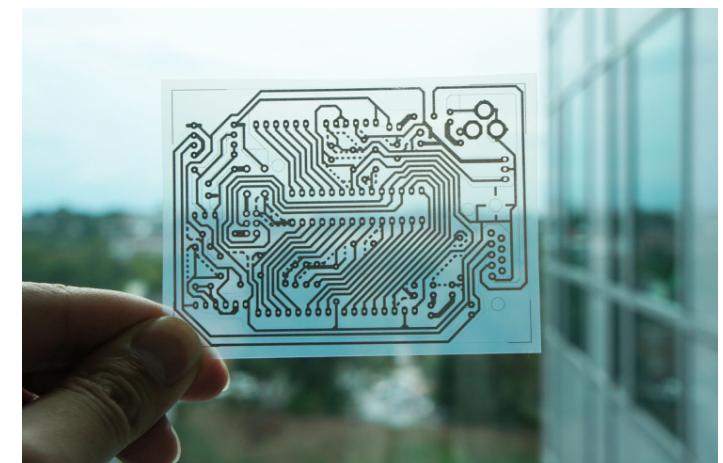


# Consumer electronics rely on integrated circuits

Devices contain chips, which contain circuits.



Wikimedia Commons



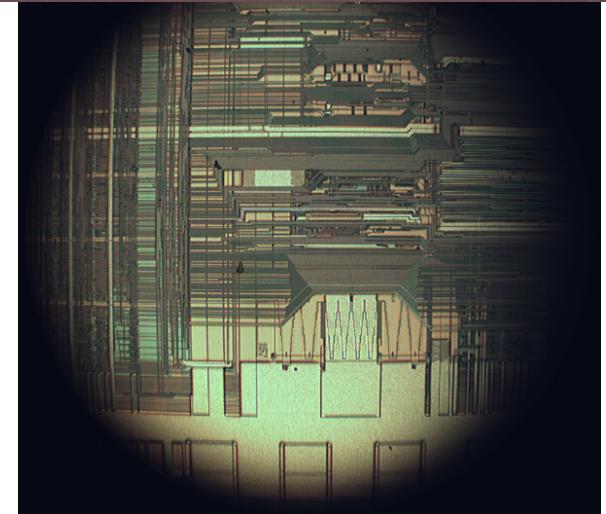
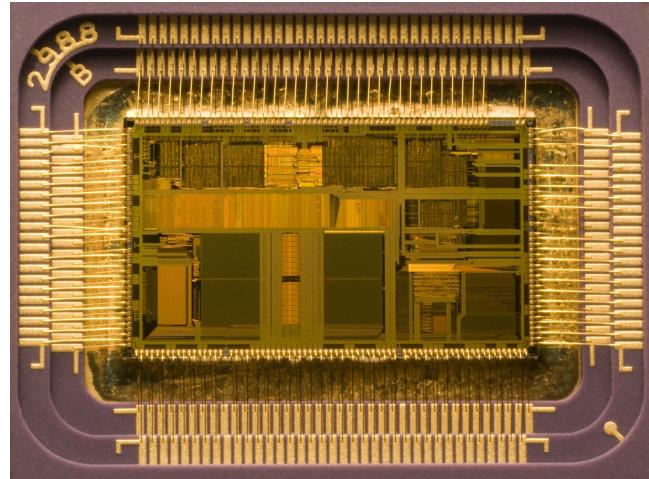
[www.news.gatech.edu](http://www.news.gatech.edu)

# Integrated circuit: what's inside?

A complex network of silicon transistors (and other components too), connected by metal wires.

- invention: Jack Kilby, 1958
- first IC with a million transistors: 1986
- first IC with a billion transistors: 2005
- Today: current record is 6.8 billion (Xilinx)

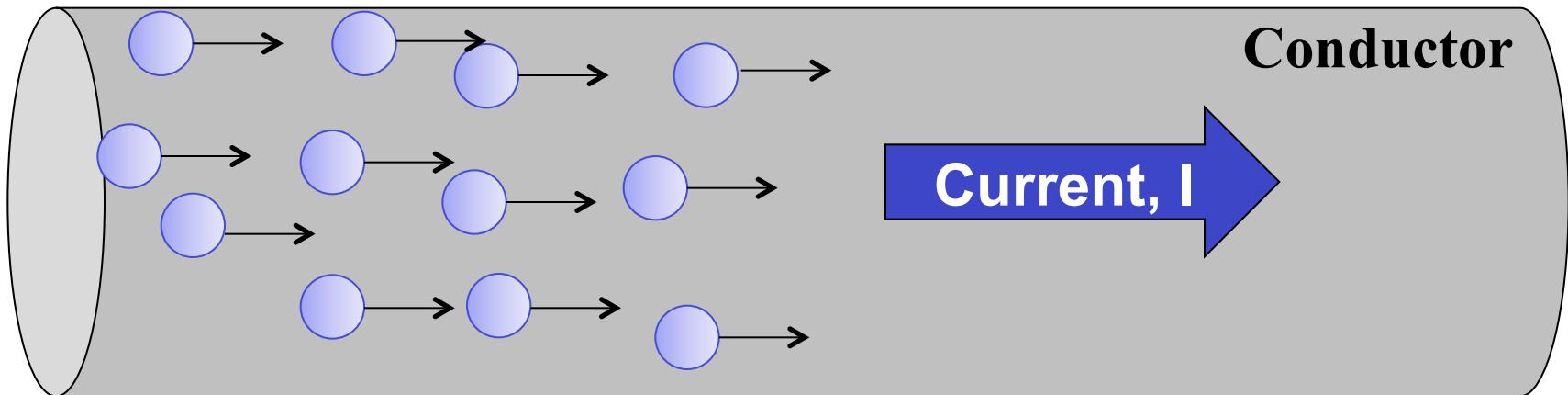
Transistors are only useful if you can connect them to each other!



An exposed 486 chip (manufactured 1993), and a close-up view of its interconnect layer

# Wires and Conductors

## Three Definitions



**Conductors** are materials that can conduct **current** ( $I$ )

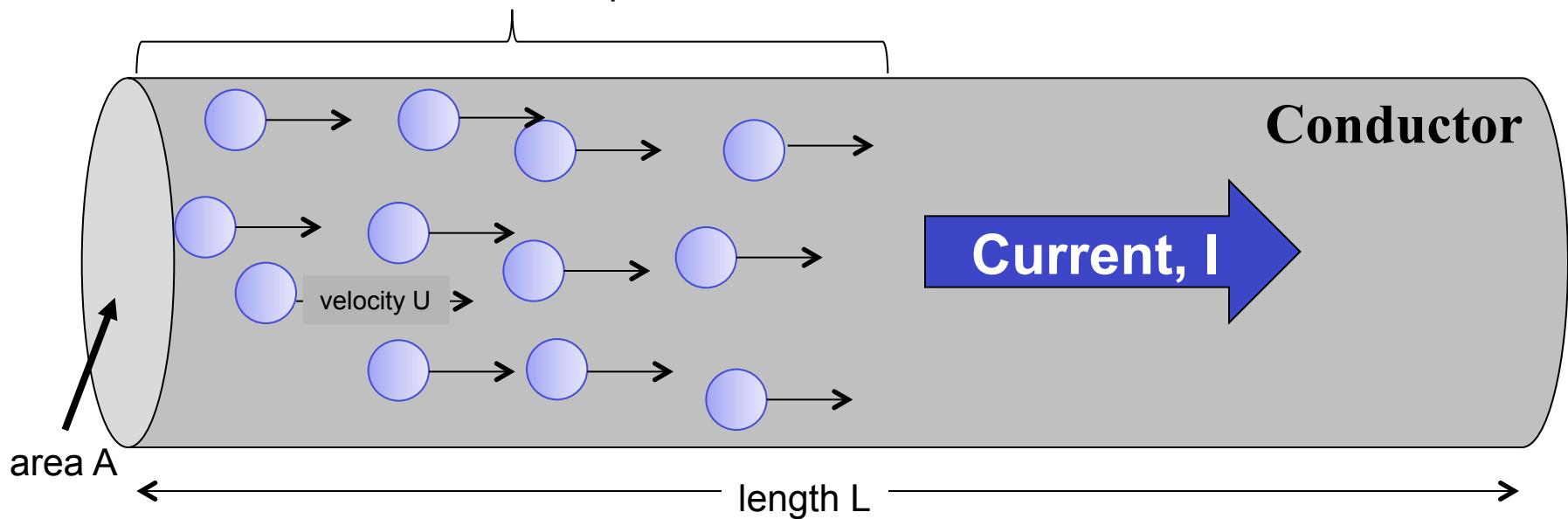
Current is a flow of electric charge (**electrons**,  $e^-$  or **holes**,  $h^+$ )

Current flows due to an applied **voltage** ( $V$ ) over a **distance** ( $d$ ),  
which creates an **electric field**  $E = V/d$

# Wires and Conductors

## Quantitative Description

number of mobile electrons per volume =  $n$



Total charge flowing through the area  $A$  in a time  $T$  is

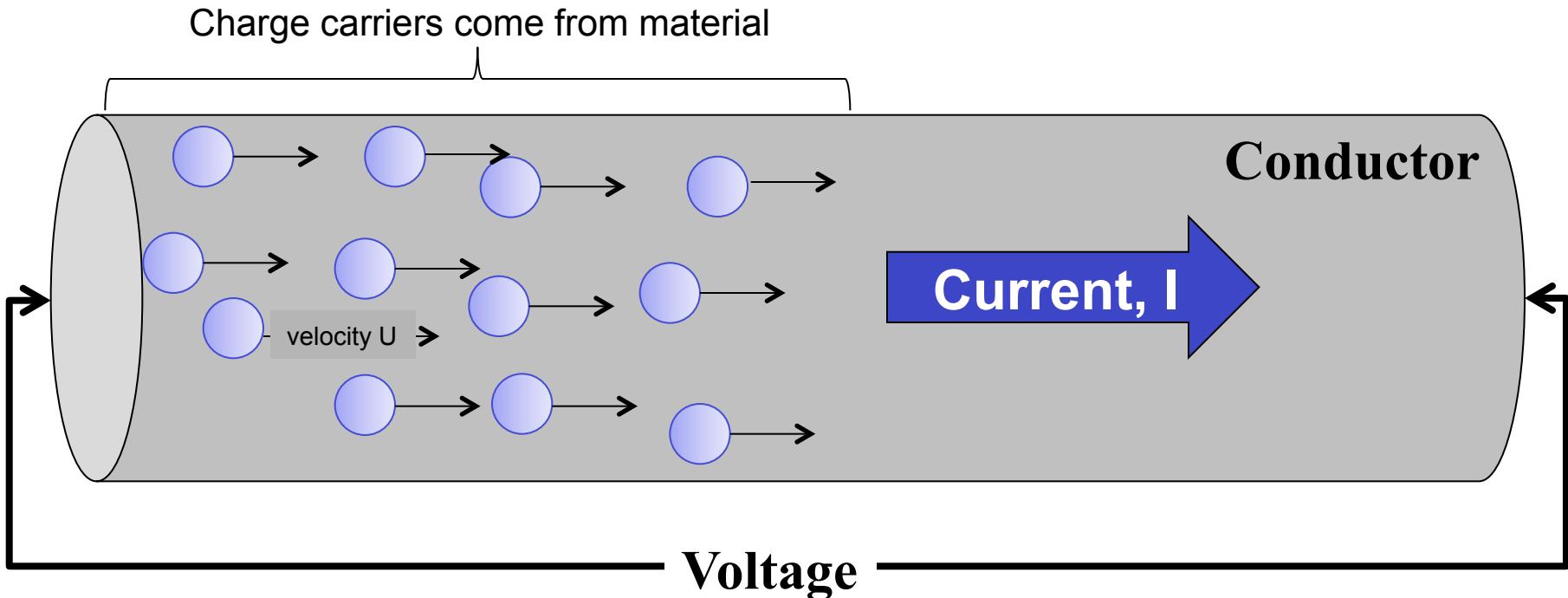
$$Q = e \cdot n \cdot \text{volume} = e n (A \cdot L)$$

To define current  $I$  = charge per unit time =  $Q/T = e n U A$

Current density  $J = I / A = e n U$

# What is needed for conduction?

$$\text{Current density } J = e n U.$$



In order to have current, charges must move ( $n$  cannot be zero)

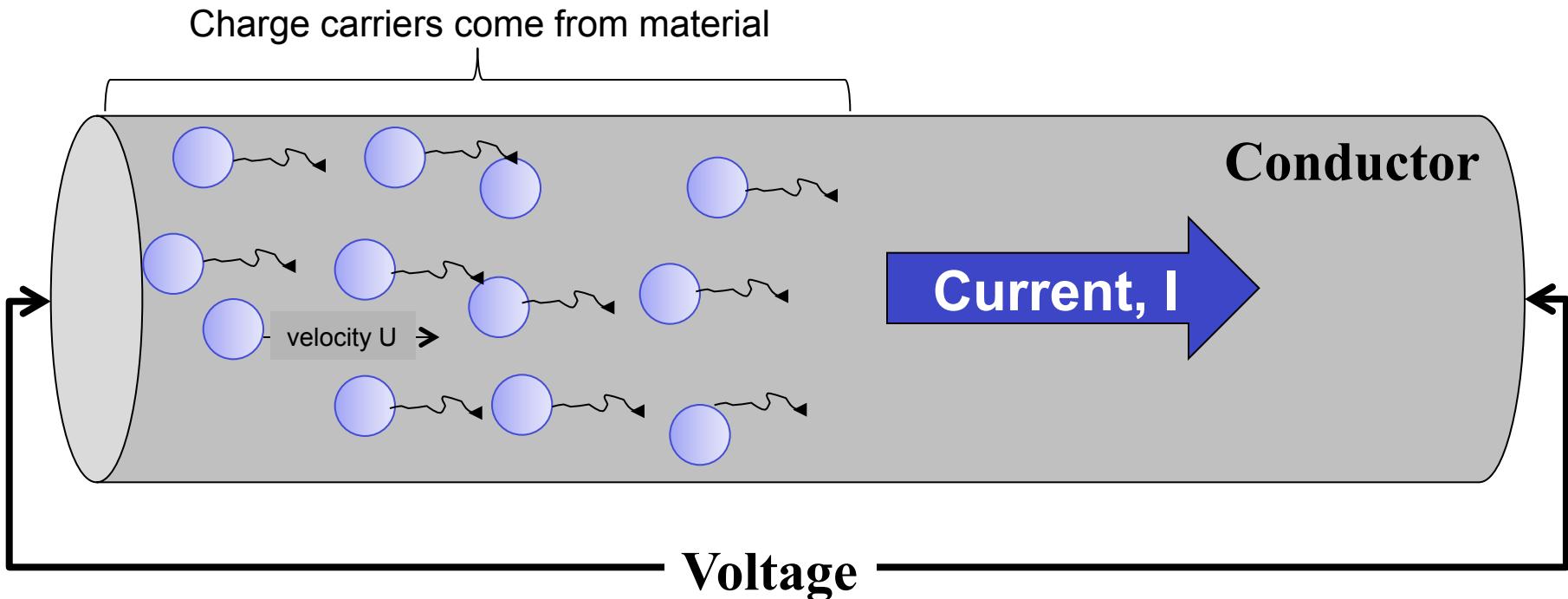
→ So we choose a metal, semiconductor

And, something must cause them to move (so  $U$  is not zero)

→ So we apply a voltage to get  $F=eE$

# Why Wires Are Not PERFECT

## part 1



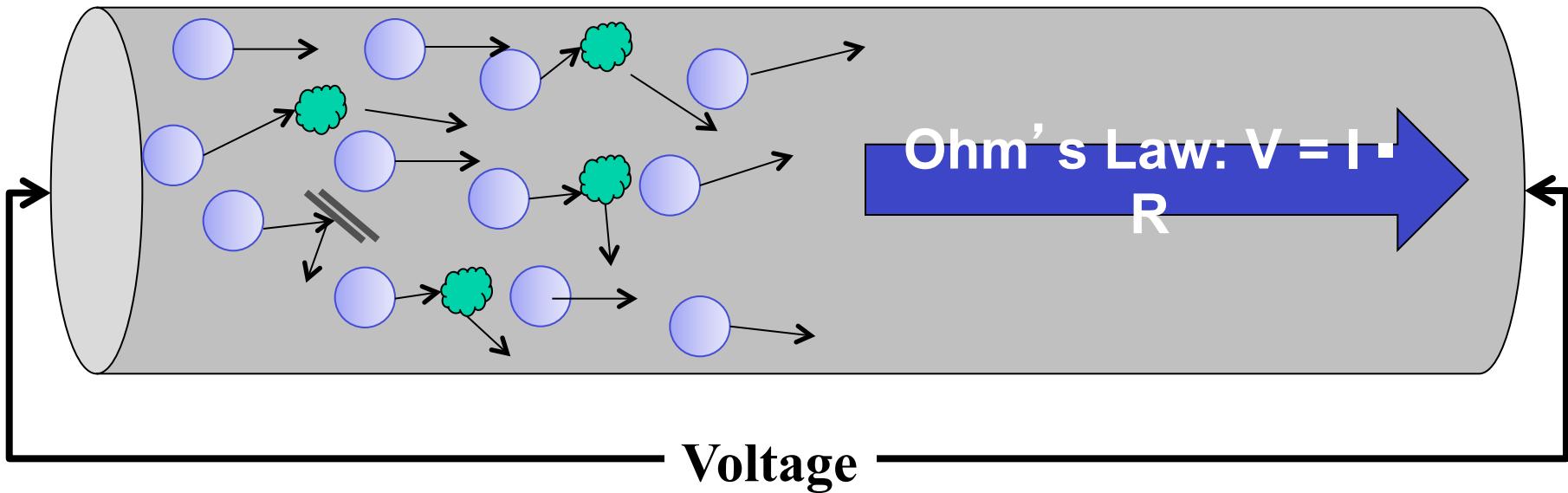
Any lattice vibrates, called phonons

Electrons lose energy by exciting phonons, creating heat

# Why Wires Are Not PERFECT

## part 2

Electrons scatter off of defects 🧬

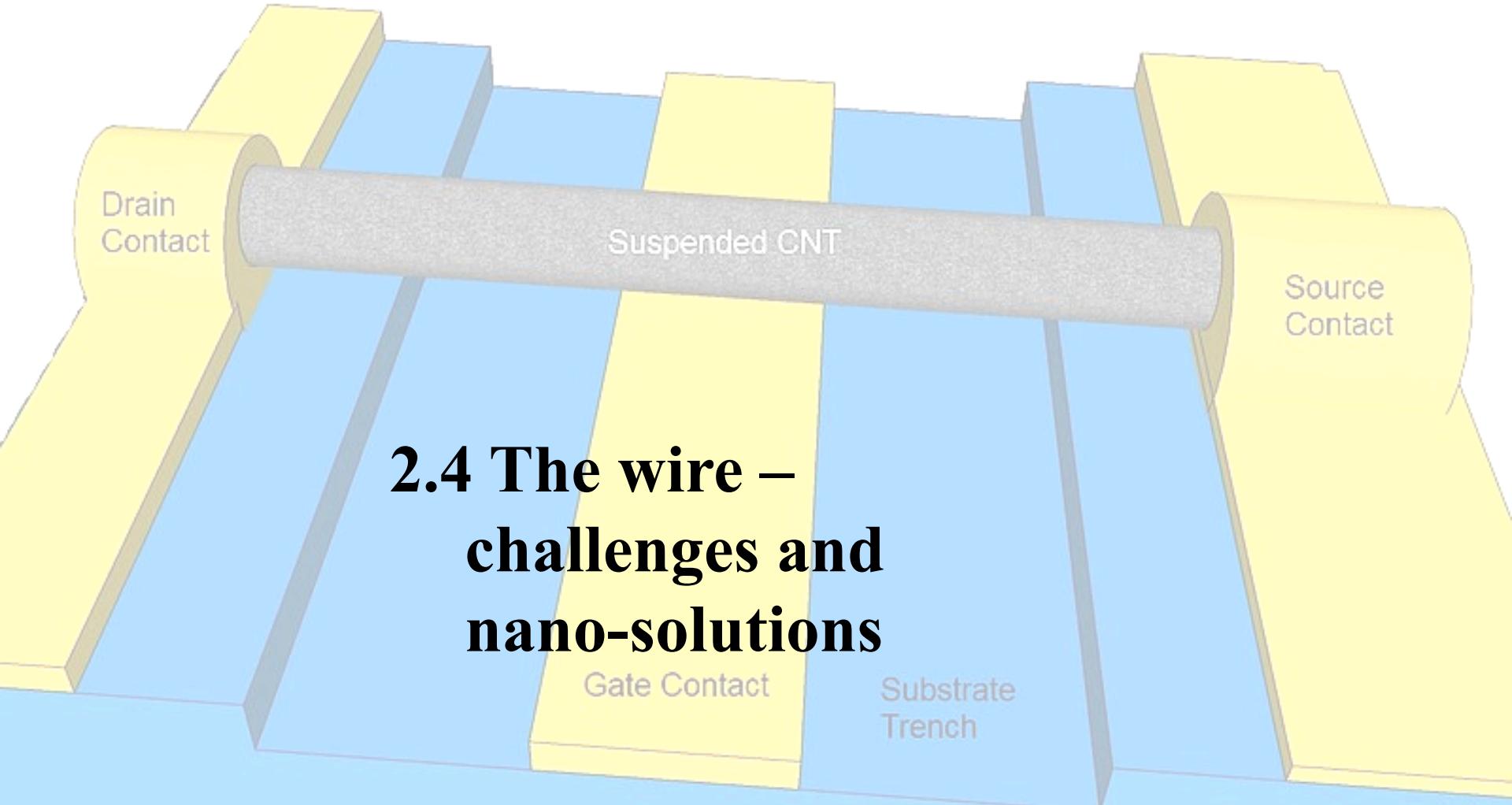


Electron collisions with defects can also cause the wire to heat up.

# The ideas

- The wire: a fundamental building block of any electronic circuit
- Current flows in wires when there are charges that are free to move, and when a voltage pushes them.
- The flow is impeded by the loss of energy to collisions with defects in the material, or to vibrations of the lattice of atoms. This is the origin of resistance.

# Nano-electronics



## 2.4 The wire – challenges and nano-solutions

# The Wire

Standard architectures use **voltage** to represent logic states.

Well-controlled voltages must be applied to electrodes; similarly, currents must flow to charge up or discharge capacitive gates to desired potentials.

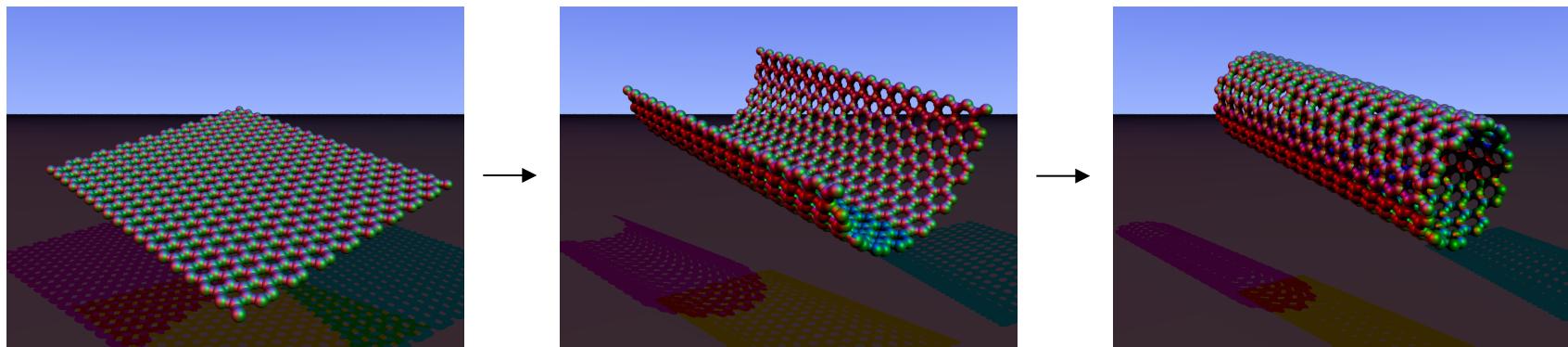
The basic interconnect now: a copper wire

Two problems:

- Shrinking wires lead to poor response at higher frequencies.
- Wires placed in close proximity = parasitic couplings.

# Carbon Nanotubes: Interesting Wires

Rolling a single sheet of carbon into a tube creates a wire of arbitrary length – a carbon nanotube:



Source: Wikimedia commons

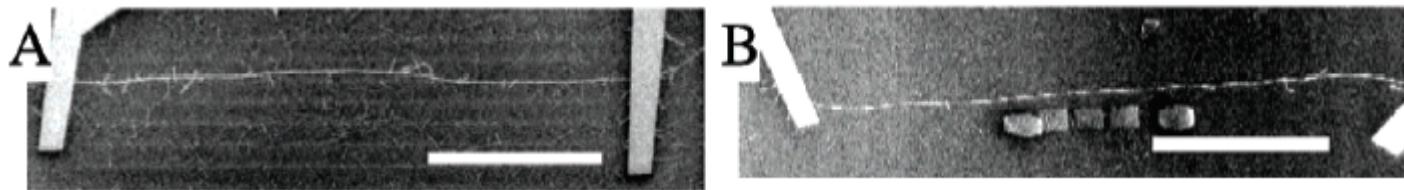
These wires can conduct electricity better than copper. And they are only ~1 nanometer in diameter.

They could be a replacement for lithographically deposited metal wires.

# How to make carbon nanotube circuits

There are three basic methods:

- Put down tubes on top of pre-patterned electrodes.
- Pattern electrodes subsequent to tube deposition.
- Grow tubes directly by CVD between pre-existing electrodes.



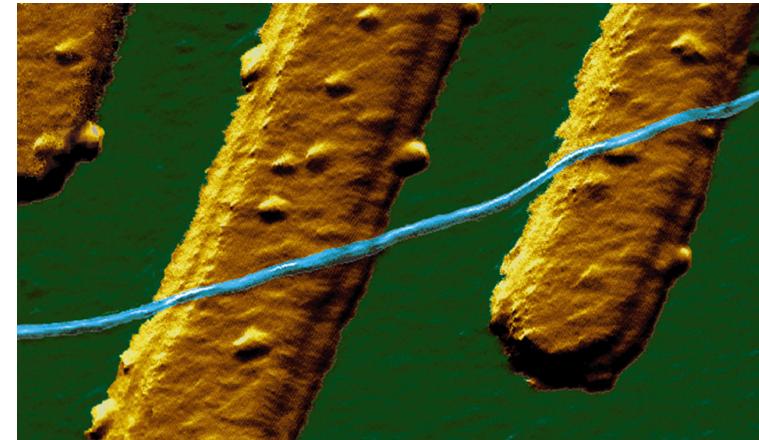
Adapted with permission from Durkop *et al.*, Nano Lett. 4, 35 (2004).  
Copyright 2004 American Chemical Society.

Issues include both scalability and reproducibility.

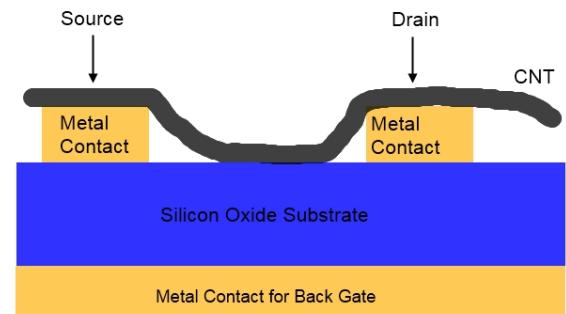
# “The wiring problem”

At right is an integrated circuit involving two SWNT transistors.

- Just because the tubes are small does not mean that the resulting circuits are particularly small
- Wiring up single molecules is extremely tiresome right now.
- This is a sneak-preview of the “wiring problem” for any truly nano circuit element.



Cees Dekker, TU Delft  
<http://ceesdekkerlab.tudelft.nl>



Source: Wikipedia Commons

# Fabrication issues

Three major reproducibility issues:

- Tube type – right now it is not possible to grow a specific tube type deterministically. A semiconducting tube would not be useful as a wire.
- Tube positioning – it is exceedingly difficult to place tubes precisely where they are wanted, in precisely the orientation desired.
- Contacts – device total conductance is limited by contact effects, with nominally identical devices having large variances in conductance.

# Unintended effects

Individual defects can critically effect conduction in SWNT devices!

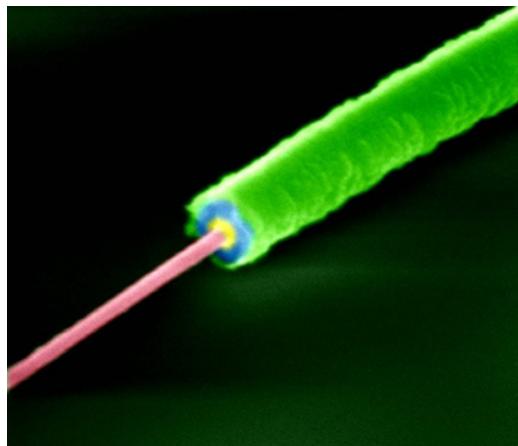
- Screening is poor, so effects of defects extend over long range.
- Conductance is truly 1D – every defect affects every carrier....

Adsorbates can strongly affect electronic properties.

**One person's packaging nightmare is another person's sensor.**

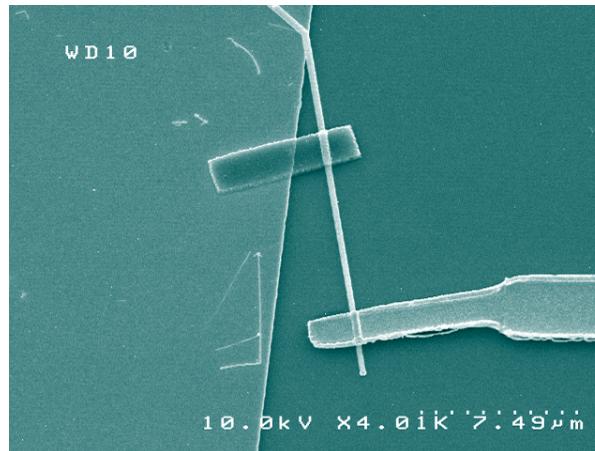
# Semiconductor nanowires

A core-shell  
nanowire



Charles Lieber, Harvard University  
<http://cmliris.harvard.edu/research/image-gallery>

- Methods now exist for growing single-crystal semiconductor nanowires  $\sim 10$  nm in diameter and microns in length.
- These structures have been demonstrated in Si, Ge, SiGe, GaAs, GaN, GaP, InAs, ZnO, etc.
- Controlled dopant distributions are also possible.
- Complicated core-shell structures and “modulation doping” have been demonstrated.

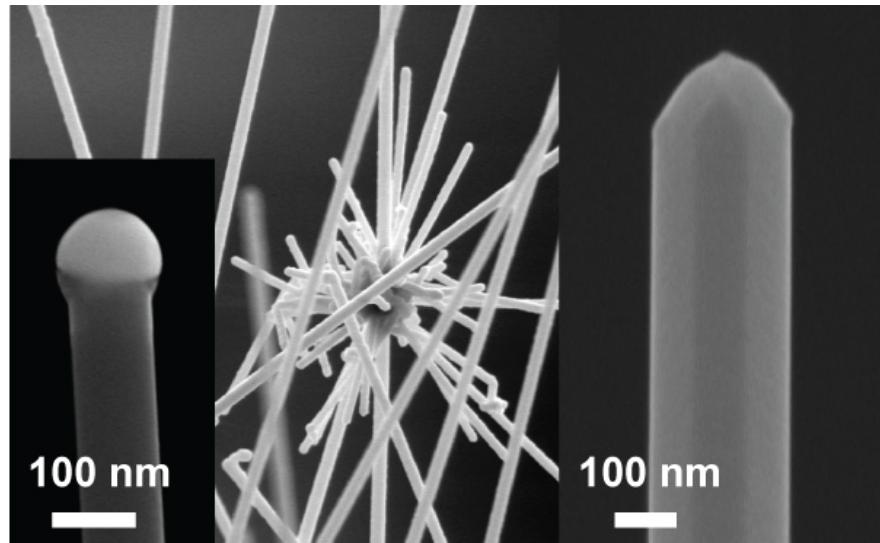


A semiconductor nanowire  
between two metal contacts

Pengyu Fan, Stanford University  
<http://www.stanford.edu/~fanpy839/publication.html>

# Potential Advantages

- Reproducibility much improved relative to carbon nanotubes.
- Similar benefits in terms of mean free path and enhanced mobility.
- Known chemistry for contacts.
- Known passivation techniques for defects, surface states.
- Potentially easier interfacing between different material types.



Jim Cahoon, University of North Carolina  
<http://www.chem.unc.edu/people/faculty/cahoon/group/research.html>

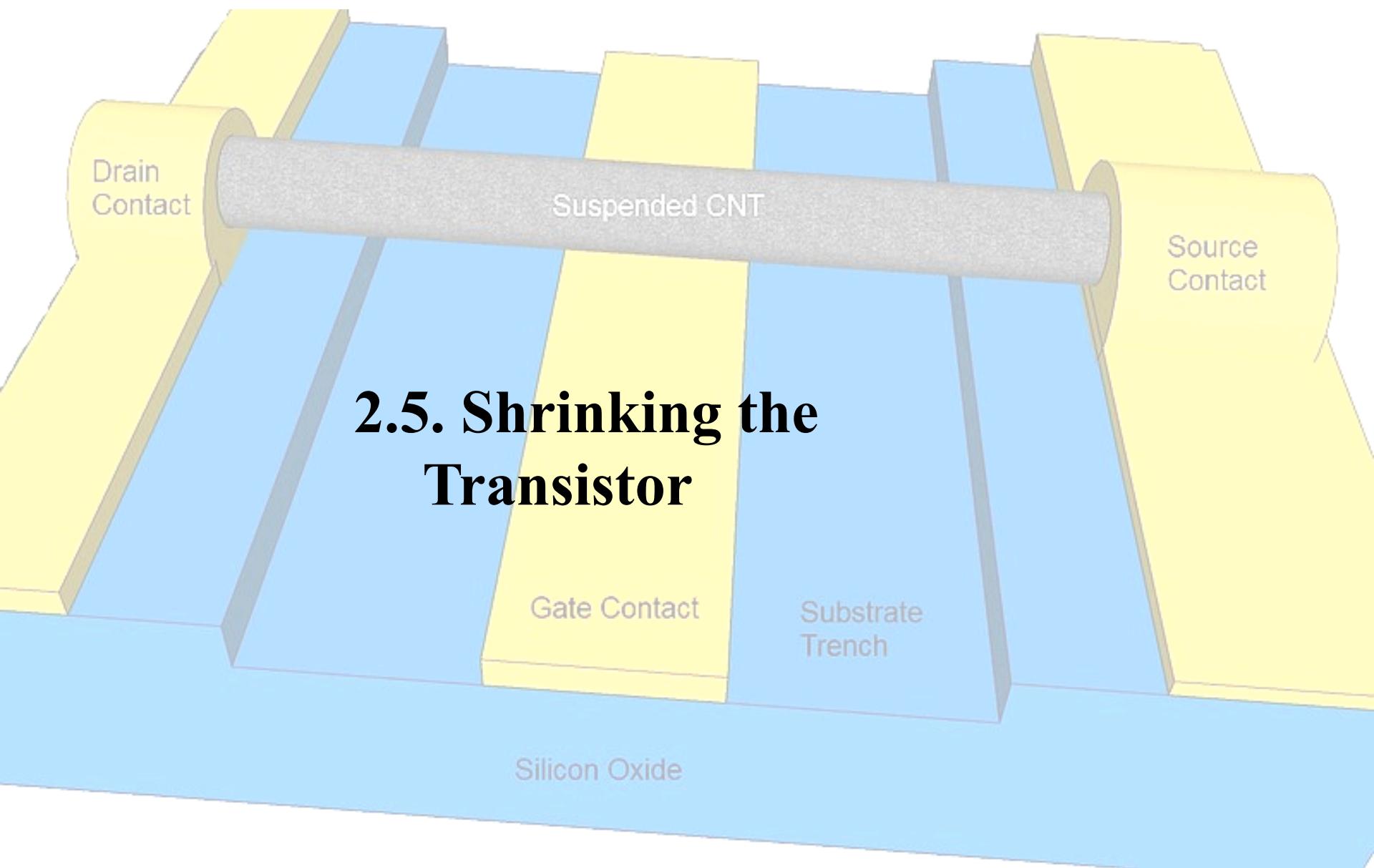
# Potential problems

- Same wiring problems as nanotubes.
- Native oxide problems, unlike in nanotubes.
- Same susceptibility to single defects as nanotubes.
- Same vulnerability to surface modification – again, is it an amazing sensor or a packaging nightmare?

# The ideas

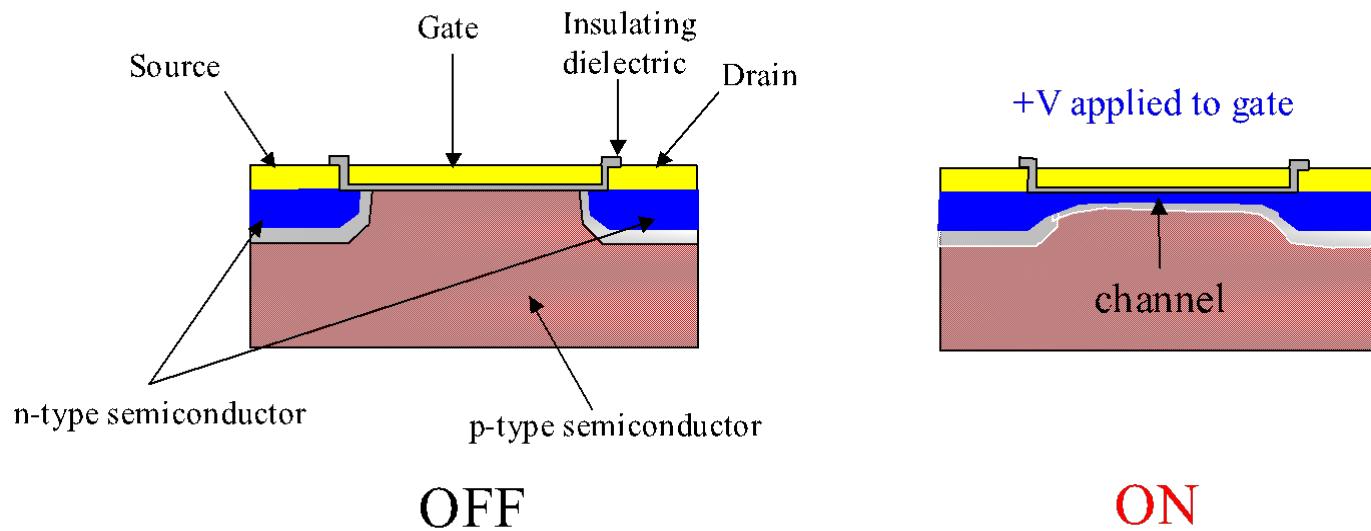
- A key challenge when shrinking circuits down to the nanoscale: the wire
- Possible nano-solutions: carbon nanotubes, semiconductor nano-wires
- Small = highly sensitive to the environment
- The “wiring problem” – how do we hook all this up?

# Nano-electronics



# The transistor

A transistor is a three-terminal device, the electronic analog of a valve.



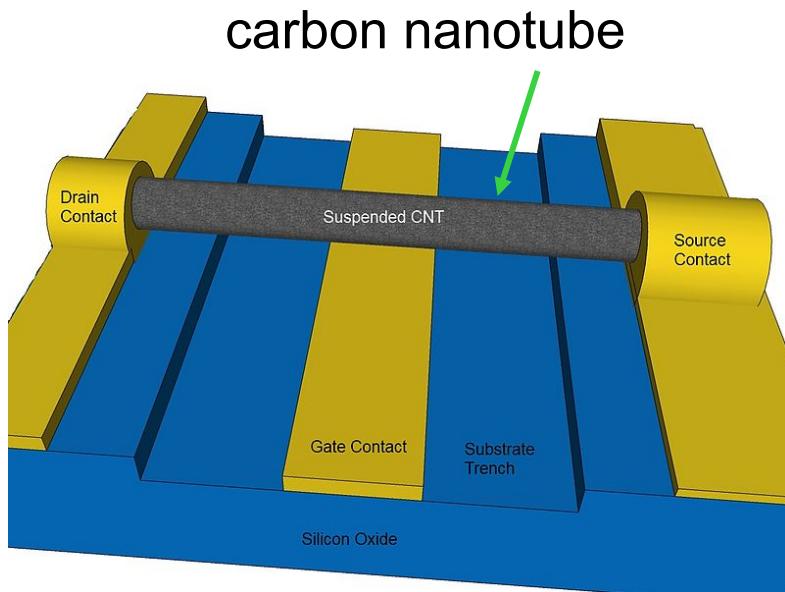
- Normally OFF - the gate must be biased sufficiently to *invert* channel region in order to create a channel for current to flow.
- A very thin insulating barrier (gate oxide) necessary.

# Transistor: issues

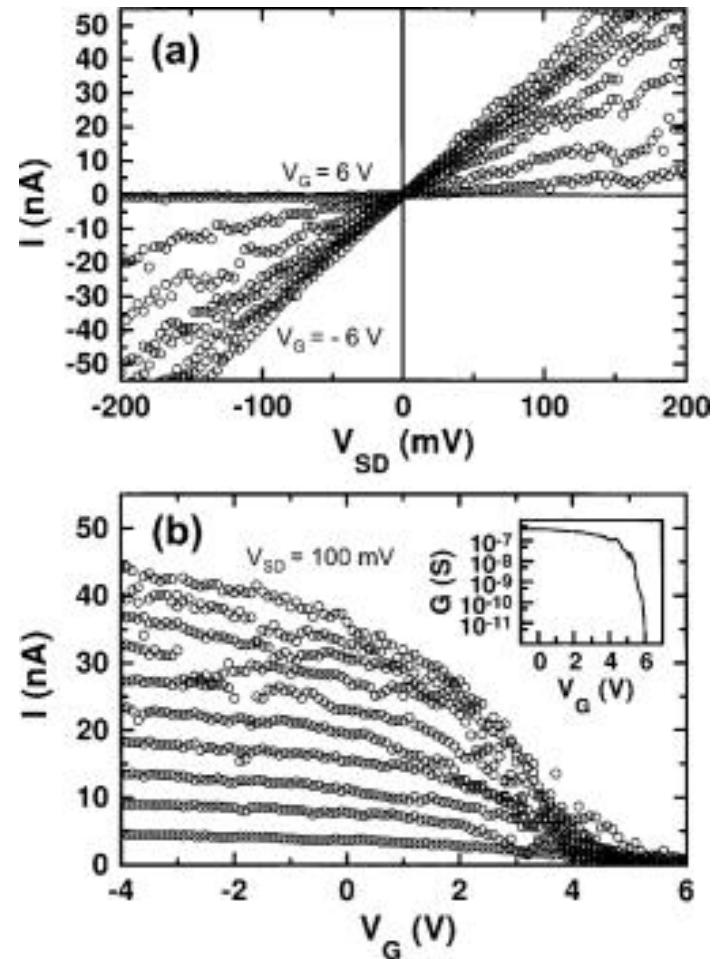
- When the source and drain get very small, the dopants (intentionally added impurities) begin to interact with each other, which increases the resistance of the contacts.
- As the gate oxide gets thinner, issues such as current leakage through the oxide begin to dominate the behavior.
- As the doped regions (e.g., near the source and drain) get small, statistical fluctuations in the number of dopant atoms can strongly influence the conductivity.

# Nanotube Transistors

With low resistance contacts, FETs made from semiconducting tubes can be quite high quality.



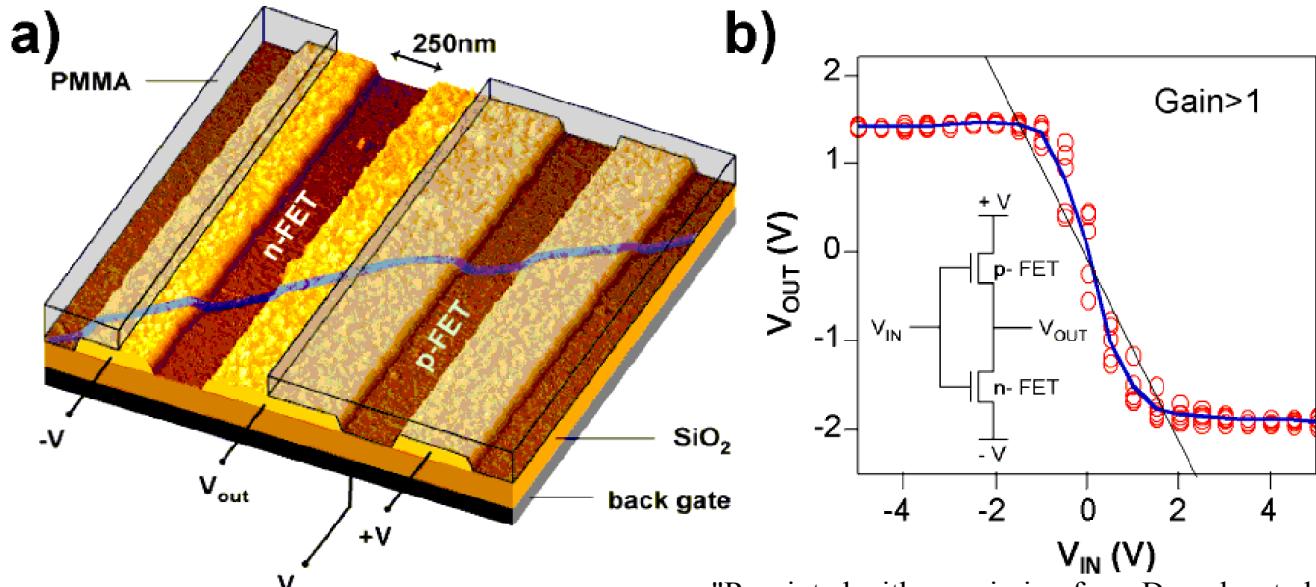
Source: Wikimedia Commons



Martel et al., APL 73, 2447 (1998).

# Potential benefits

- Limited scattering in a 1D structure means incredibly high effective mobilities (greater than  $77000 \text{ cm}^2/\text{Vs}$  at 300 K).
- Per channel width, this means extremely good performance.
- Can be doped by chemical modification to be *p* or *n* type – possible to have a *pn* junction (i.e. a transistor) within a single molecule!



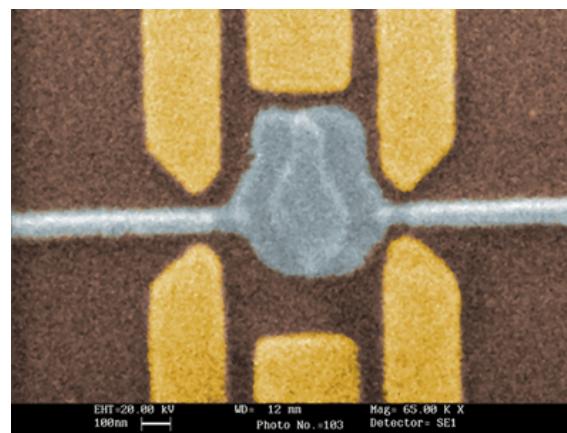
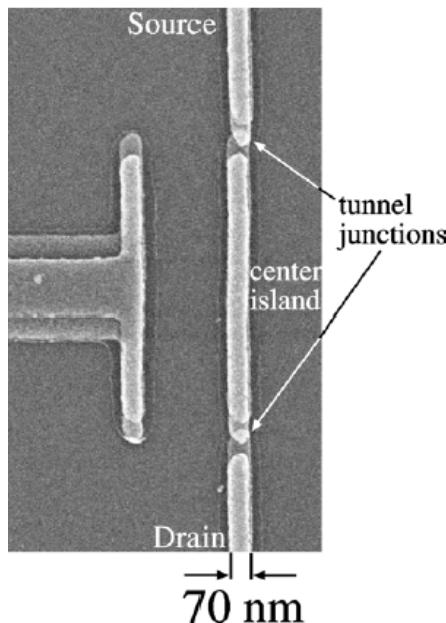
"Reprinted with permission from Derycke et al., Nano Lett. 1, 453 (2001). Copyright (2001) American Chemical Society."

# A transistor which relies on a single electron

Single electron transistor: a possible nano-solution

Various types:

D. Berman, PhD thesis, MIT (1998)

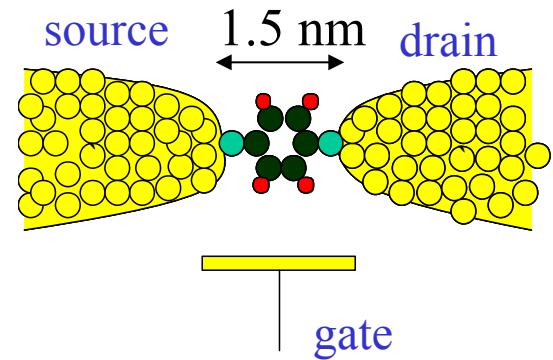


GaAs/AlGaAs SET

Aluminum SET

Alex Rimberg, Dartmouth University  
<http://www.dartmouth.edu/~rimgroup>

Doug Natelson, Rice University  
<http://www.ruf.rice.edu/~natelson/group.html>



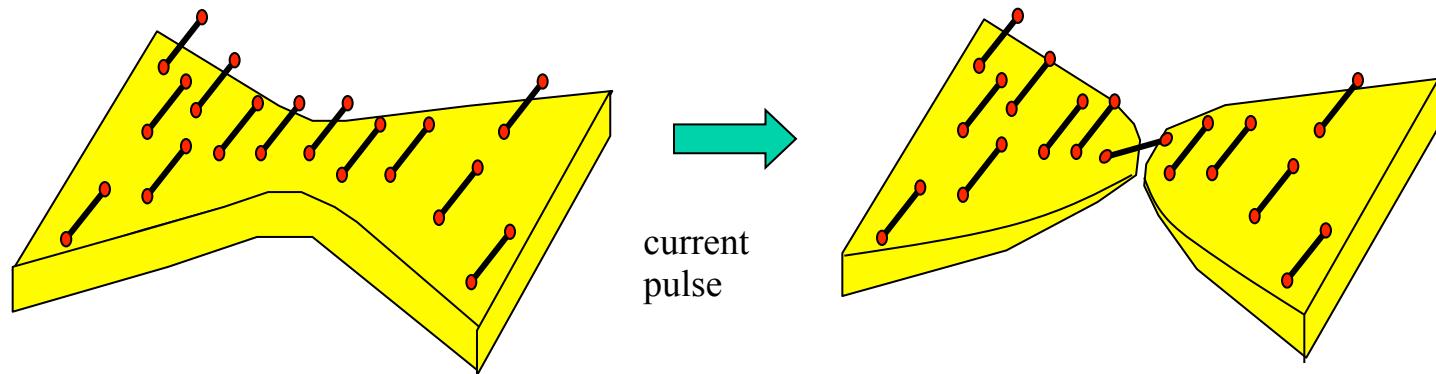
Single-molecule transistor

# Incredible sensitivity to the environment

Any charge near to the SET acts like an effective gate.

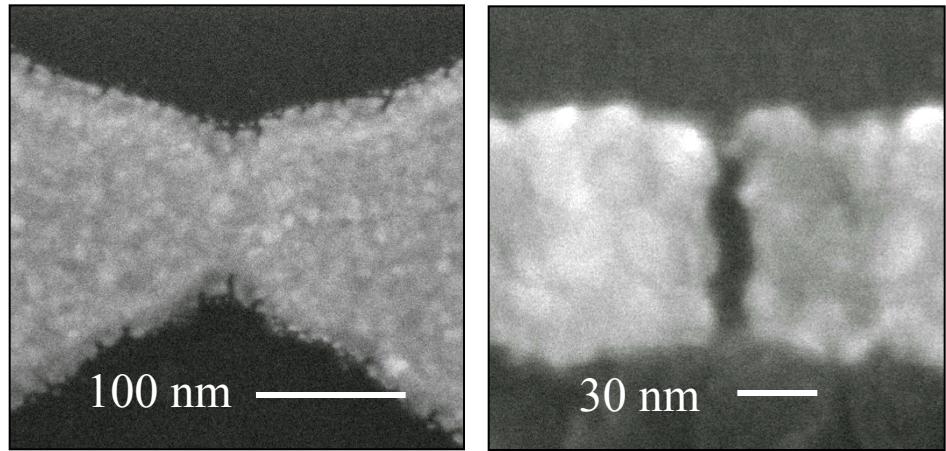
- The good news: SETs are the world's most sensitive electrometers.
- The bad news: switching of any charged trap results in large shifts in conduction properties.

# Molecular electronics?



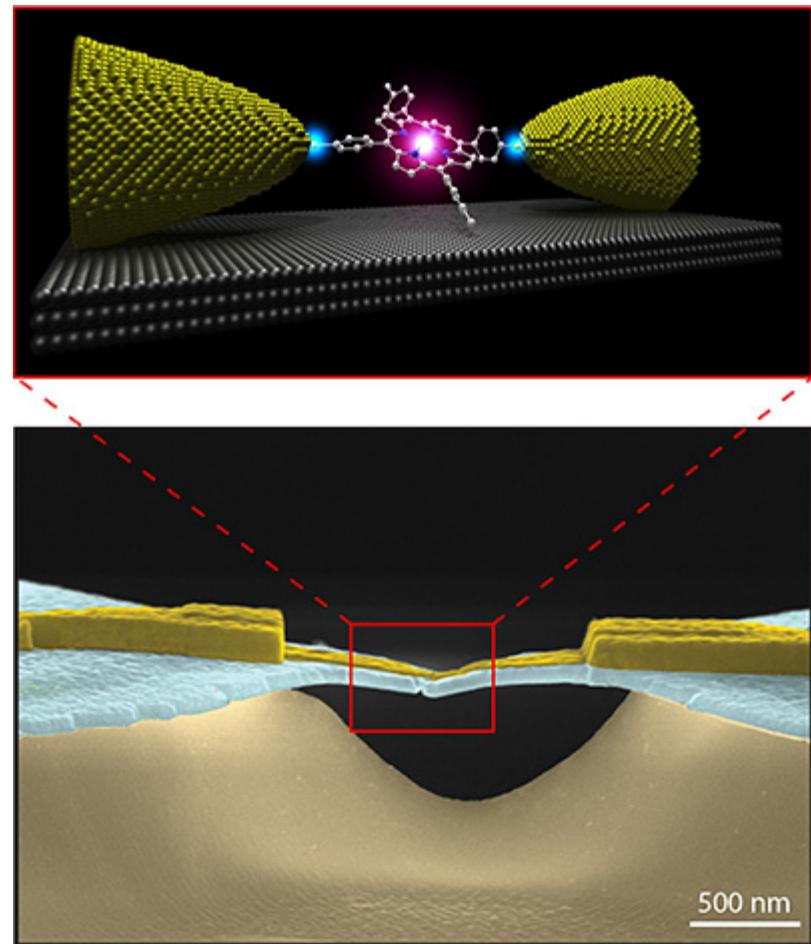
Park *et al.*, *APL* **75**, 301 (1999)

- Rely on chance that some fraction of devices will have a molecule positioned at the source-drain gap.
- Every device is **different!**



# The “wiring problem” again

- Leads and gates are still vastly larger than active device region.
- Device stability is really limited today by atomic-scale geometric stability of electrodes and molecules.
- Possible improvements include more refractory electrode materials and surface passivation of metals by “inert” molecules.



J. Van Ruitenbeek, University of Leiden  
<http://www.research.leiden.edu>

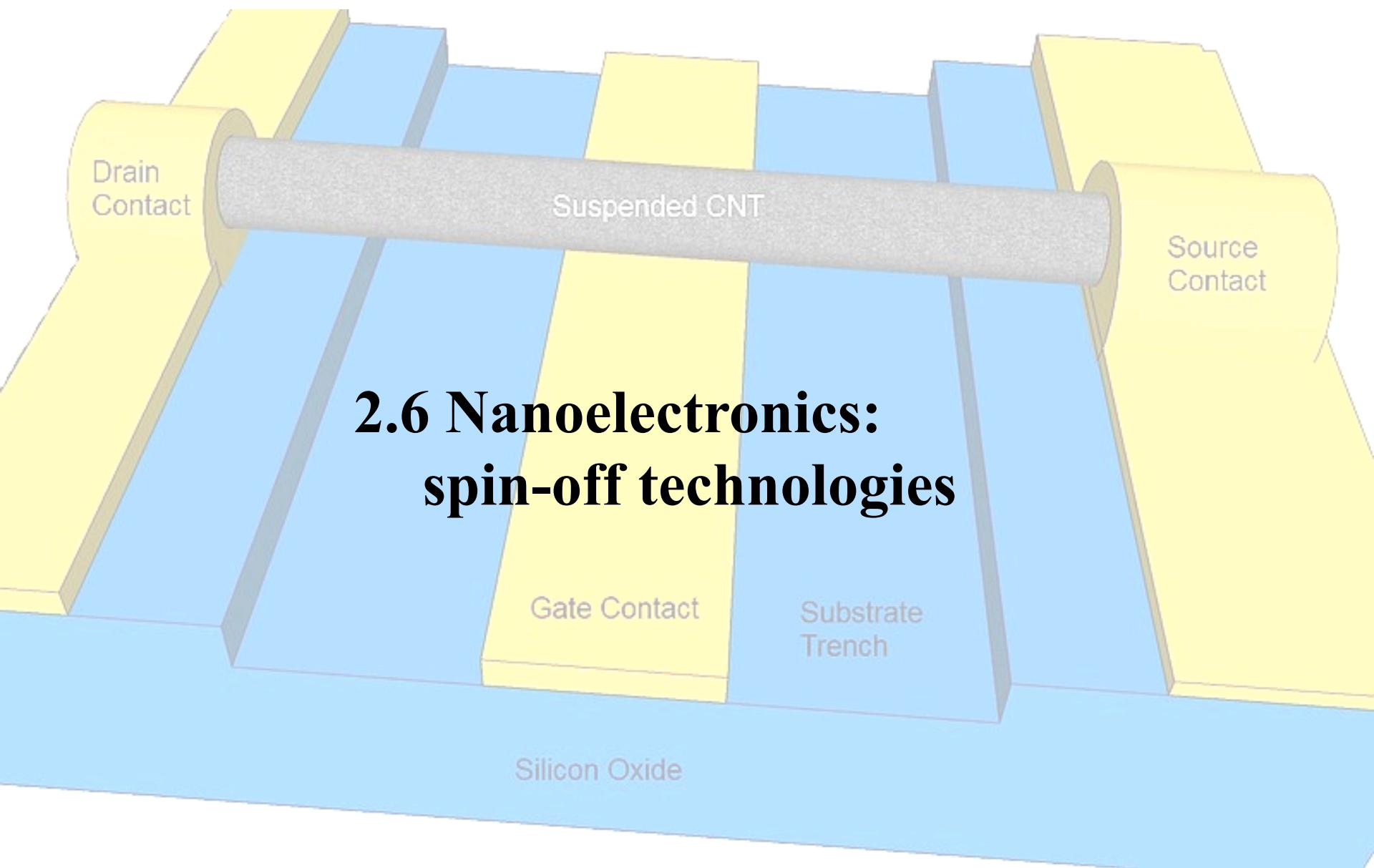
# Many open questions

- Interface energetics between bulk materials remain confounding.
- Charge transfer at the single-molecule level depends critically on ***everything***, including exact details of molecular bonding.
- Where does the “molecule” end and the “leads” begin?
- What are the localized states in SMTs?
- How does screening work?
- What does capacitance mean in such systems?
- How can we treat electronic correlations correctly?
- How do dissipative processes work in these systems?

# The ideas

- A key challenge when shrinking circuits down to the nanoscale: the transistor
- Possible nano-solutions: gated nano-wires, single-molecule electronics
- Fabrication, packaging, repeatability
- The “wiring problem” again

# Nano-electronics



## 2.6 Nanoelectronics: spin-off technologies

# Processing silicon

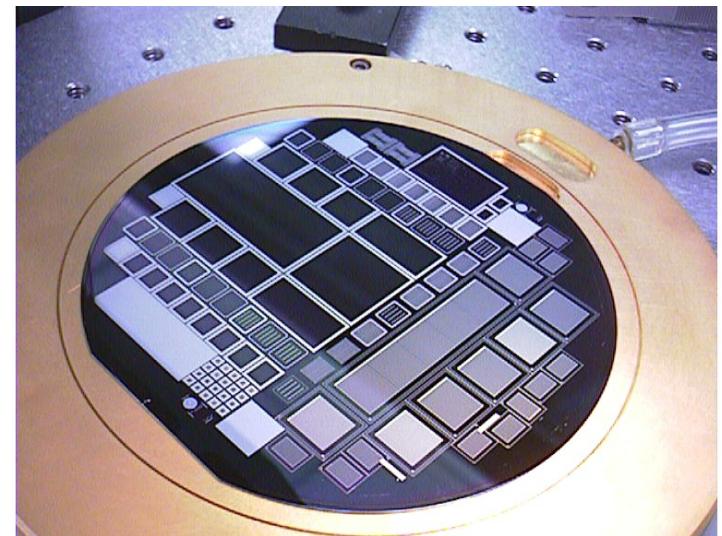
The electronics industry has developed many tools for turning bare silicon wafers into integrated circuits.

A bare, polished Si wafer



Source: University of Vermont, [www.ece.vt.edu](http://www.ece.vt.edu)

A processed Si wafer



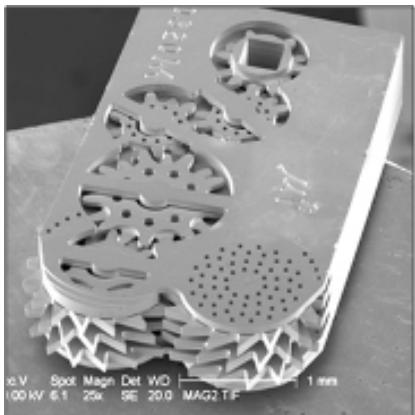
Source: Syracuse University, [www.phys.syr.edu](http://www.phys.syr.edu)

These tools give us amazing abilities to create nanoscale structures.

# Nanoelectronics has many spin-off technologies

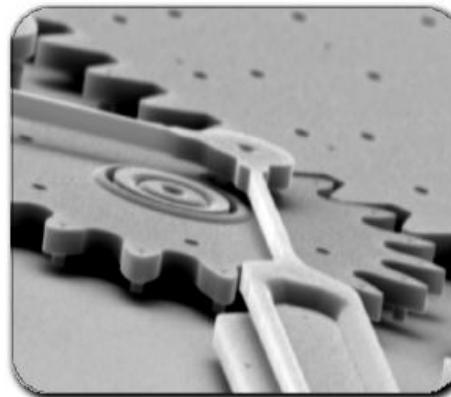
These capabilities have found uses in many areas outside of the electronics industry.

A tool for microsurgery



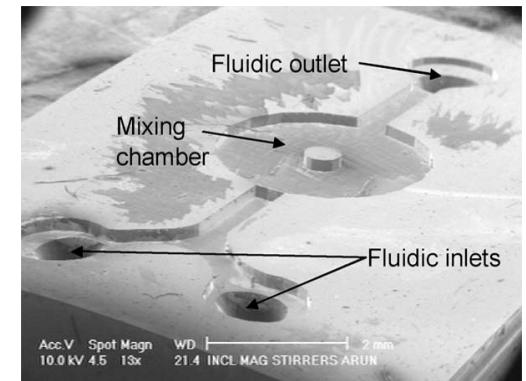
Boston University, [www.bu.edu/biorobotics](http://www.bu.edu/biorobotics)

Micro-gears and machines



Worcester Polytechnic Institute, [chslt.wpi.edu](http://chslt.wpi.edu)

Micro-fluid reaction vessels



University of Texas Dallas, [mems.utdallas.edu](http://mems.utdallas.edu)

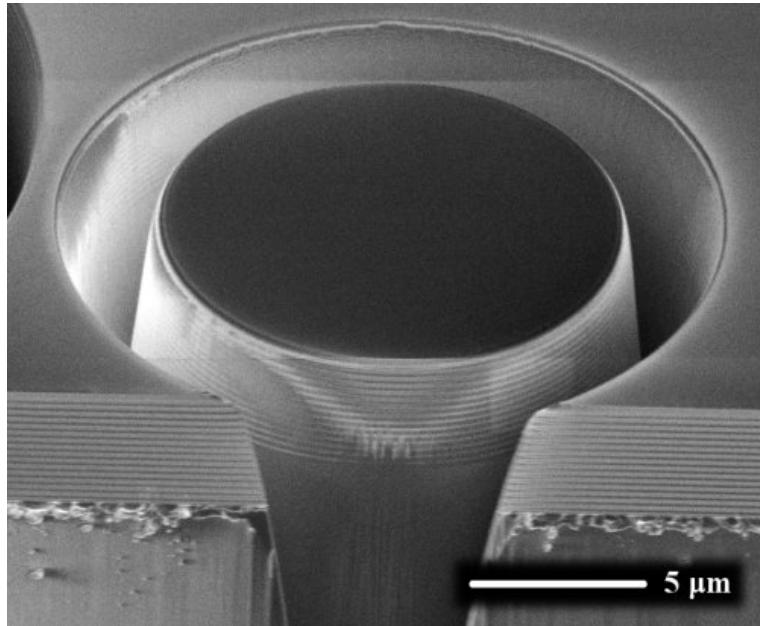
Just a few of the many examples:

- depositing multiple nanometer-thick layers with atomic precision
- carving small channels in substrates
- creating cantilever structures

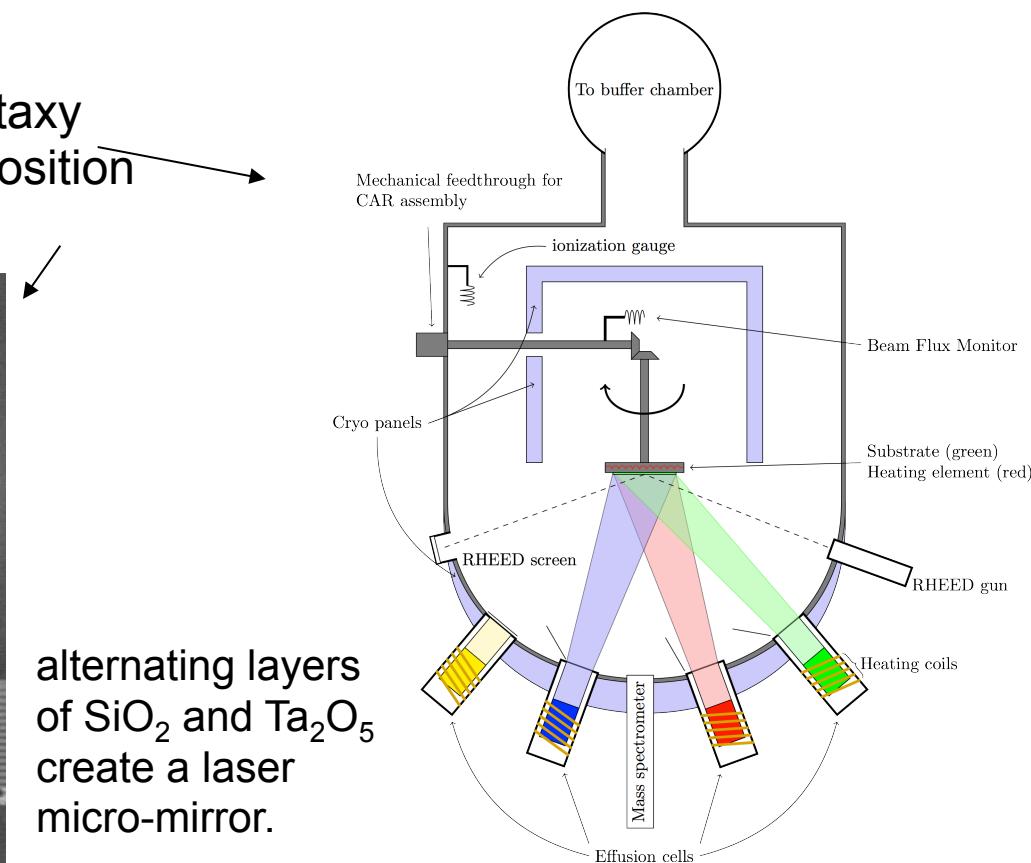
# Making thin perfect layers

Numerous techniques exist for laying down multiple nanometer-thick layers of different materials on a substrate, with thickness control at the atomic level.

Examples: Molecular beam epitaxy  
physical vapor deposition



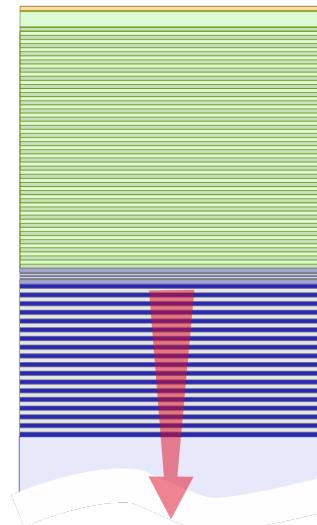
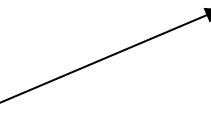
alternating layers  
of  $\text{SiO}_2$  and  $\text{Ta}_2\text{O}_5$   
create a laser  
micro-mirror.



# Making thin perfect layers

Multi-layers of this sort are the basis for many technologies.

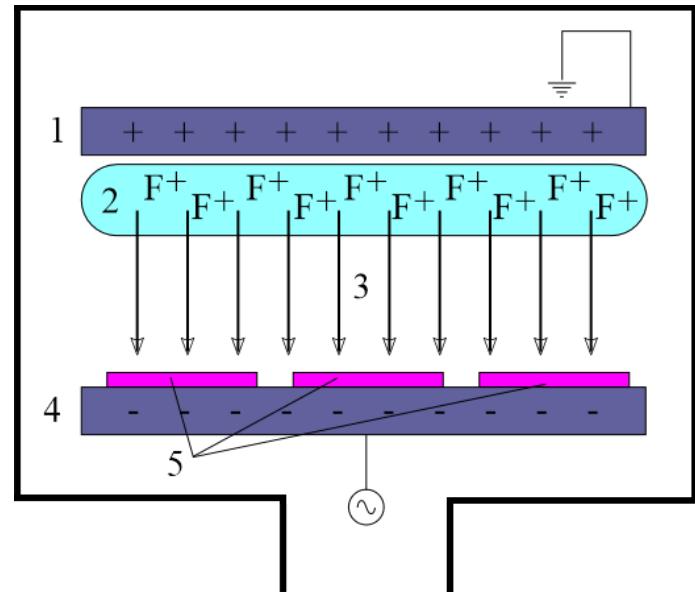
- ❖ optical coatings on your glasses and camera lenses
- ❖ the laser in your DVD player
- ❖ the hard drive in your desktop computer



# It is also useful to remove material selectively

Another important process technology: **reactive ion etching**

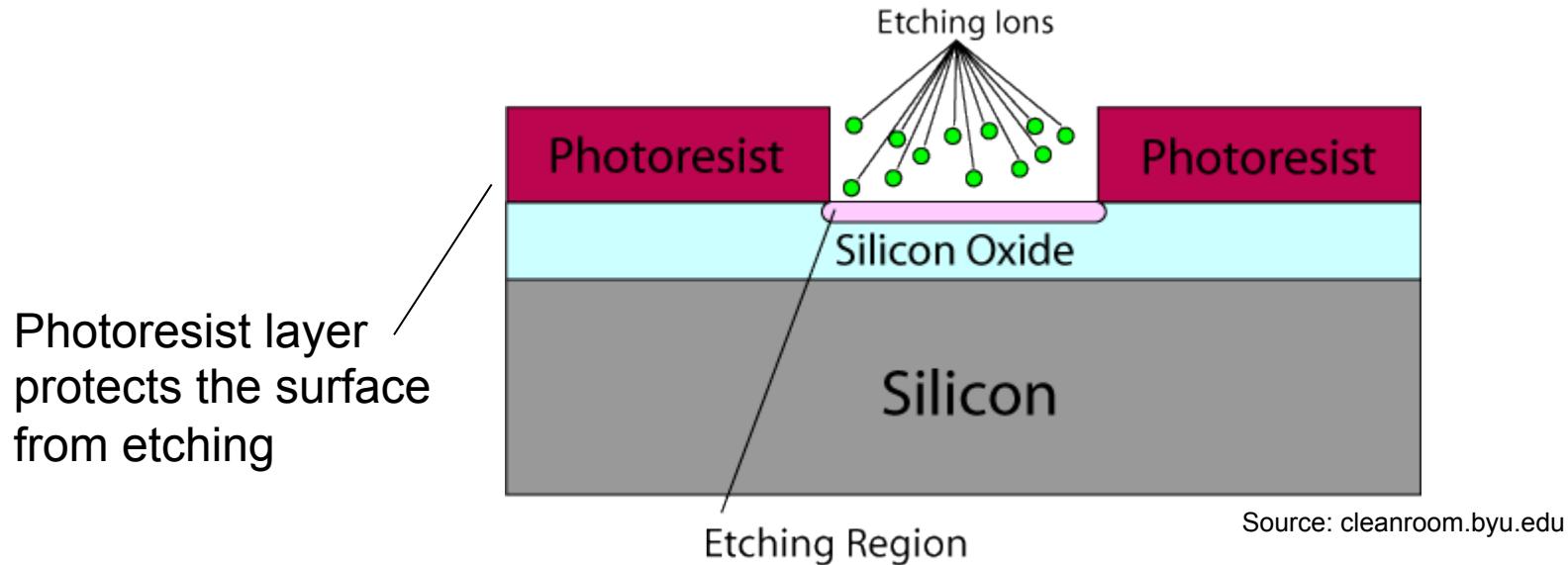
1. Microwave radiation is used to create a plasma, a gas of charged atoms (2), at the top electrode (1).
2. Because these atoms are charged, they are accelerated (3) towards the bottom electrode (5).
3. When they encounter the sample (4), they react with the surface and remove material.



Source: Wikimedia Commons

The removal of material can be very anisotropic: vertical channels

# Controlling where material is removed from



Photolithography can be used to create a pattern of photoresist (basically, plastic) on a surface. This layer protects the surface from the etching process. Thus, etching can be done selectively.

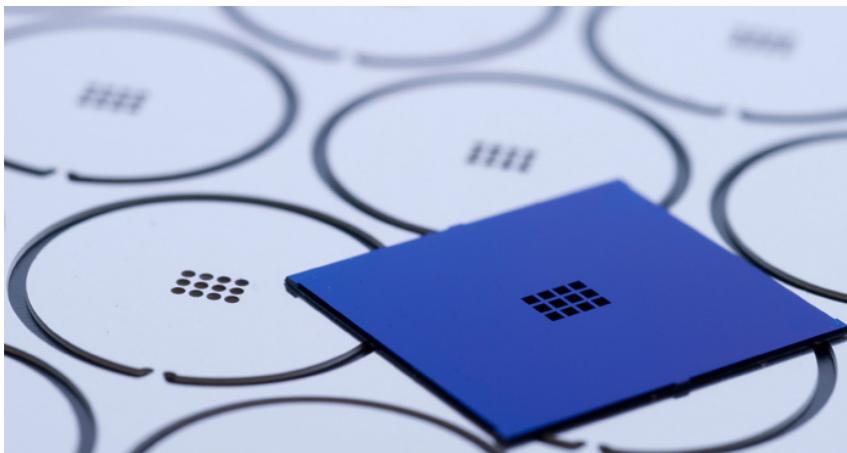
# Microfluidics: small channels

Making tiny channels can be useful for creating a “lab on a chip”

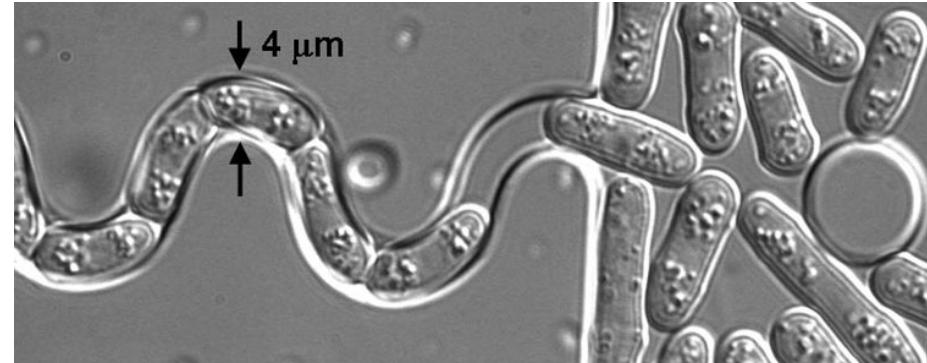
- sensing small quantities of analyte
- cell biology: one cell at a time!
- multiple parallel sensors
- medicine for the Third World

check out Rice 360:

<http://rice360.rice.edu>



Source: McDevitt lab, Rice Univ.

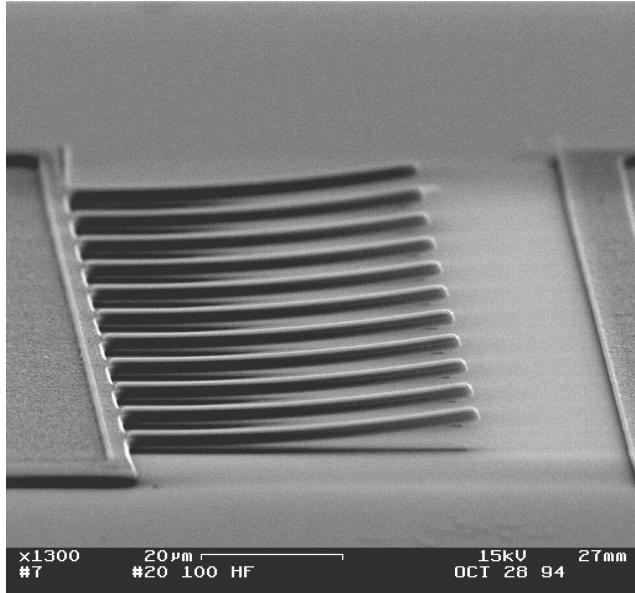


Source: www.uphs.upenn.edu

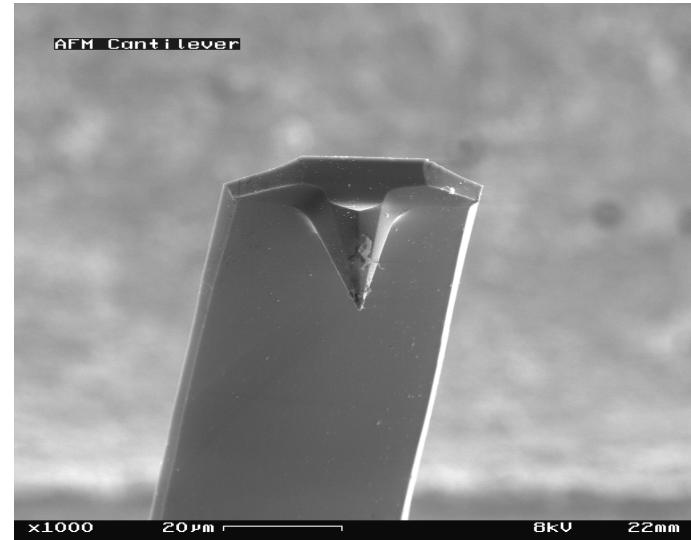
# Cantilevers

These same ideas of depositing and removing material can be used to create more complicated structures, like cantilevers.

An array of micro-cantilevers



A cantilever with a tip on the bottom

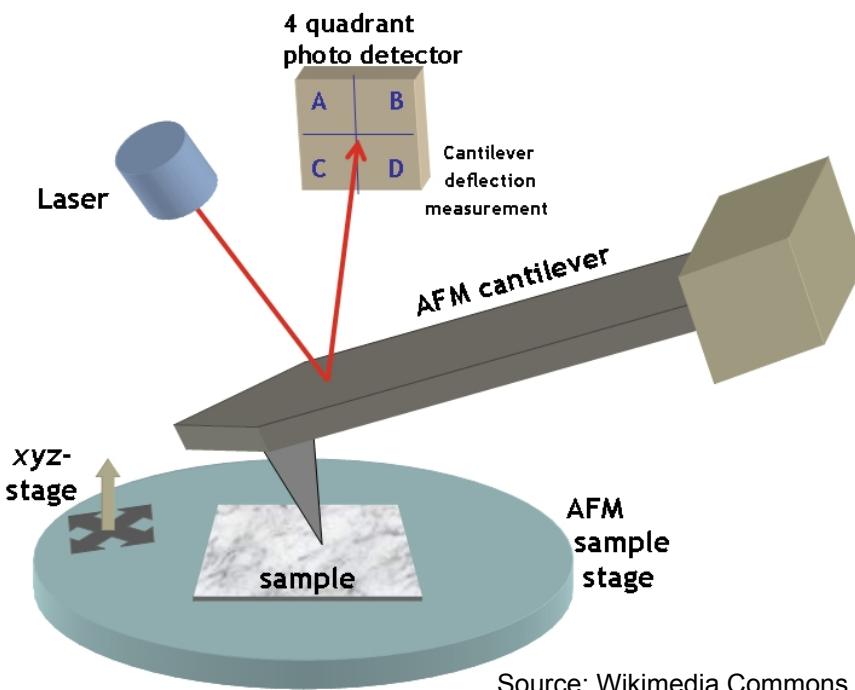


Source: [engineering.dartmouth.edu](http://engineering.dartmouth.edu)

Source: Wikimedia Commons

# Cantilevers for sensing and imaging

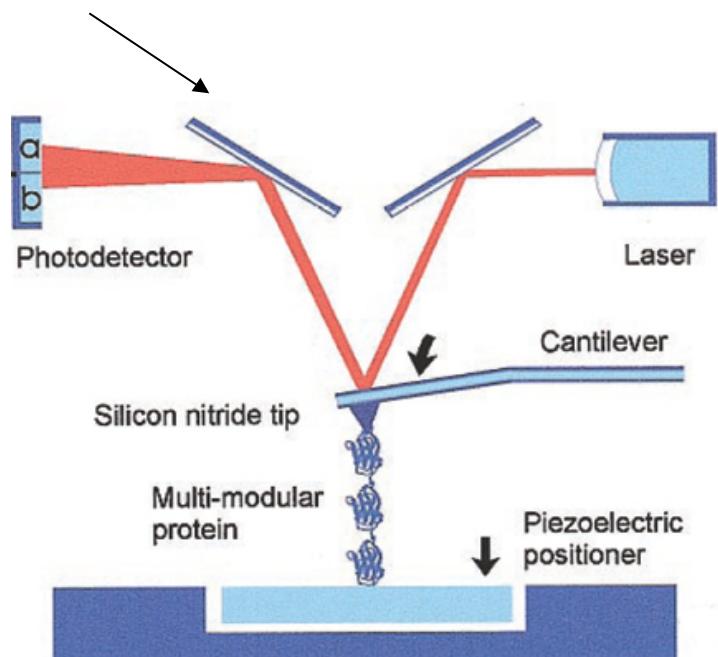
Atomic Force Microscopy:  
measuring the topography of a  
surface with nanometer precision



Source: Wikimedia Commons

Other ideas:

- measuring the binding of a single molecule to the cantilever
- measuring the mechanical properties of a single molecule

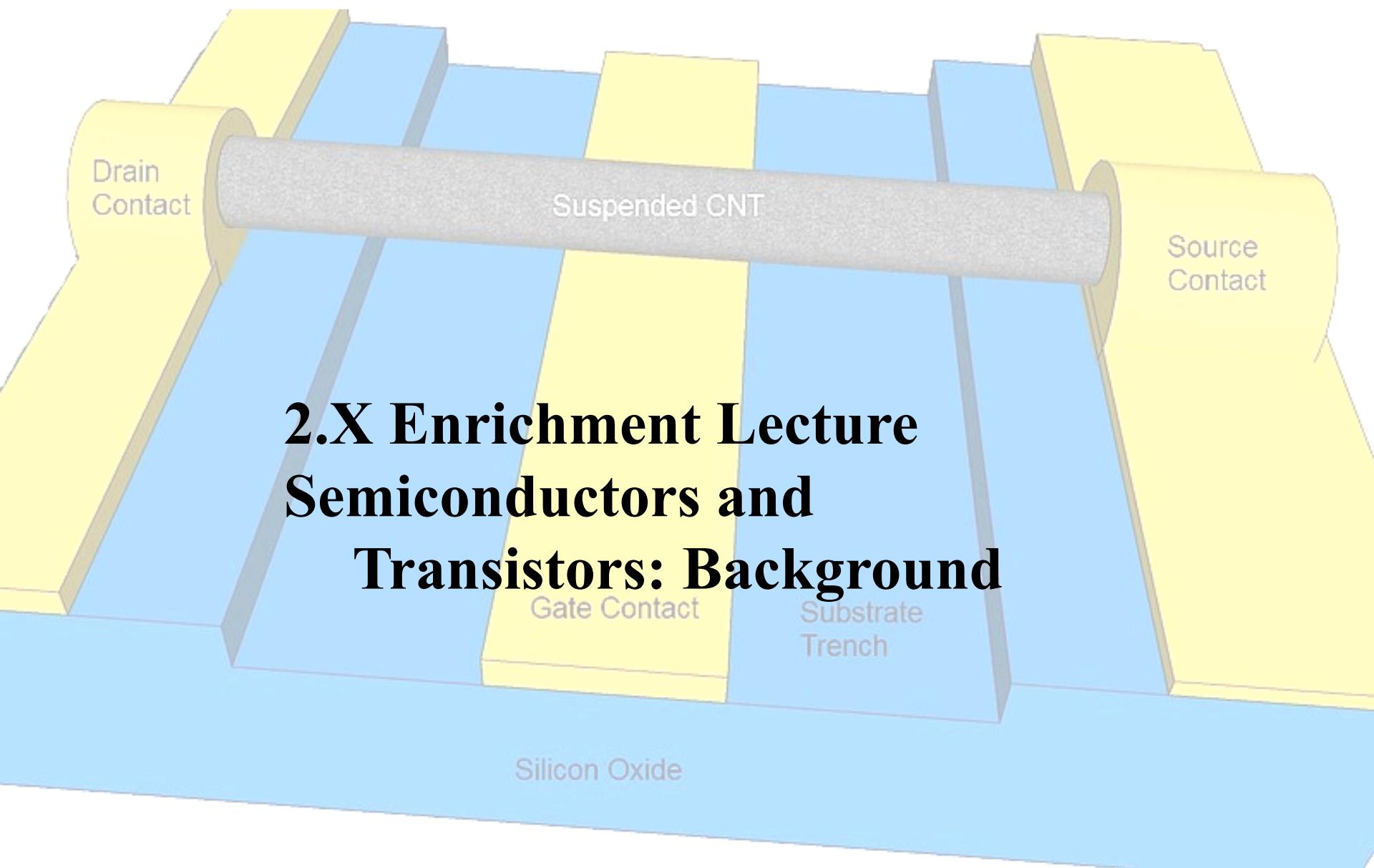


Source: Paul Hansma, hansmalab.physics.ucsb.edu

# The ideas

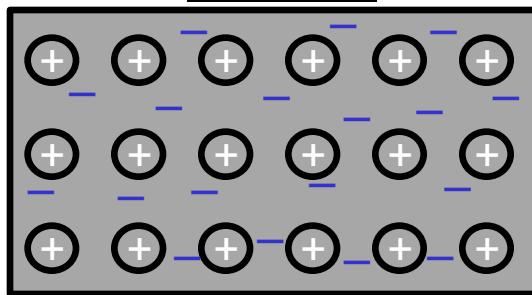
- The need for smaller and smaller electronics has driven a lot of innovation in the processing and fabrication of nanoscale materials and structures.
- These new processes and techniques enable a wealth of spin-off technologies.

# Nano-electronics



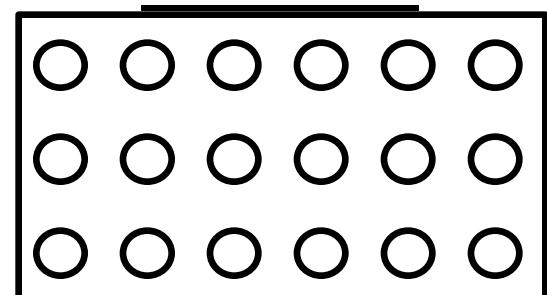
# Metals vs. Insulators

Metals



Is there  
anything in  
between?

Insulators



Positive ions and core electrons do not contribute to conduction, since they are fixed in place

The number of free electrons is equal to valency times number of positive ions, a **VERY** large number.

→  $\sim 10^{23}$  per cm<sup>3</sup>

Free electrons can move around, and therefore contribute to conduction.

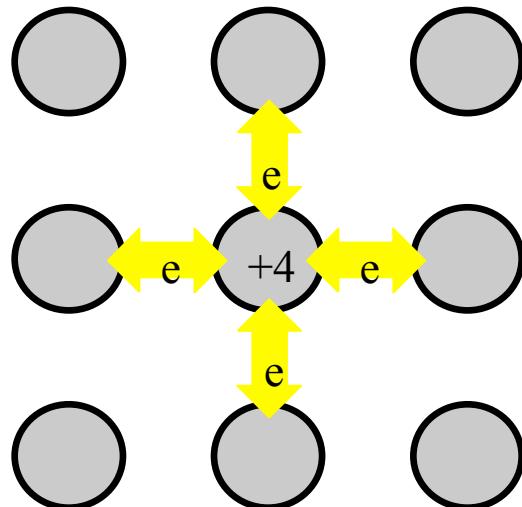
Atomic cores do not give up any valence electrons - all of them are involved in bonds between atoms.

No free electrons means no conduction, even if we apply a voltage.

# Semiconductors

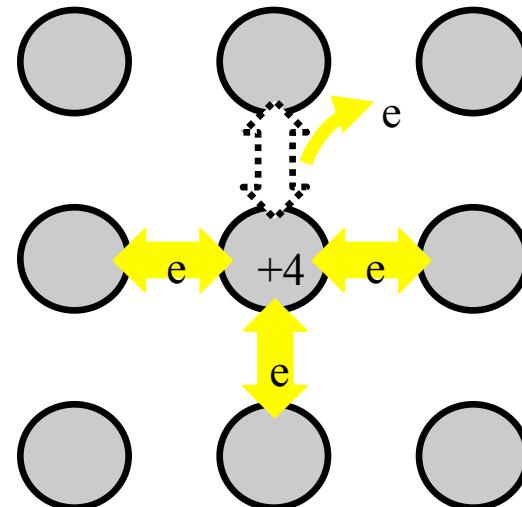
Consider a material where some of the electrons can be liberated from chemical bonds by just a little kick, e.g., a bit of heat.

Low Temperature



all electrons (including valence electrons)  
are bound - NO conduction

High Temperature

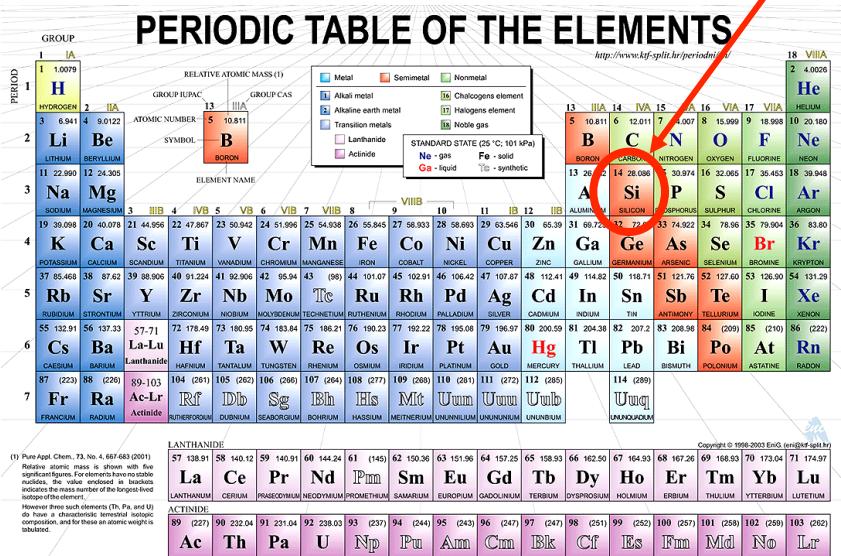


some electrons are able to break  
free and participate in conduction

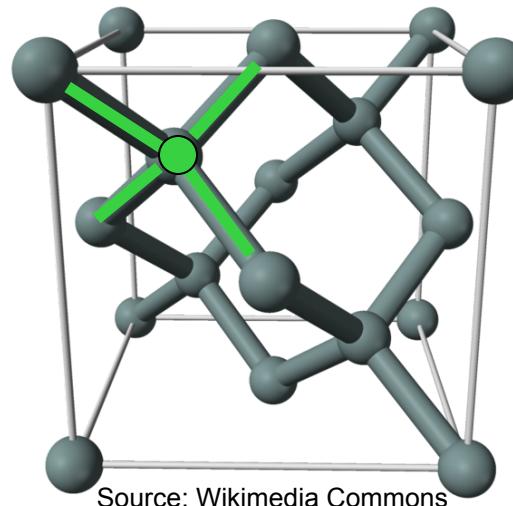
This is a semiconductor. The conduction depends sensitively on the temperature of the material.

# Semiconductors

Silicon is the most important example. It is the base material for all integrated circuits.



Silicon has a valency of 4, which means it has four electrons that can participate in chemical bonds.



Source: Wikimedia Commons

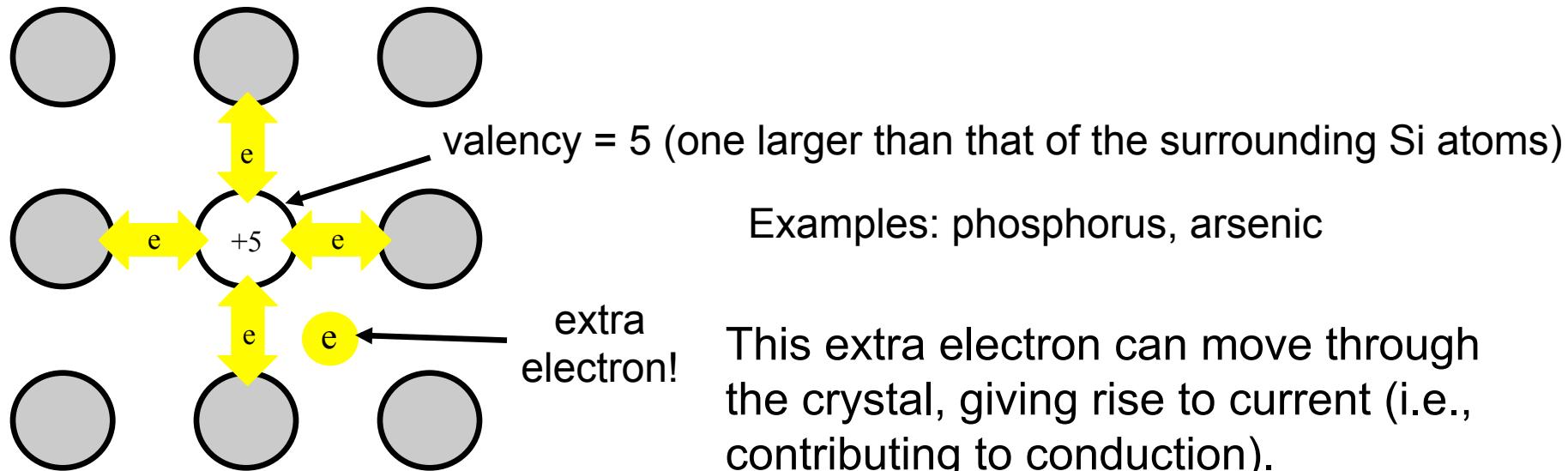


It crystallizes in a structure where each atom has four neighbors. Thus each of the neighbors gets to use one electron in a covalent bond.

# Doping of Semiconductors

Conduction can also be modified by adding impurities.

Doped semiconductor: impurities added on purpose!  
These impurities substitute for a silicon atom.

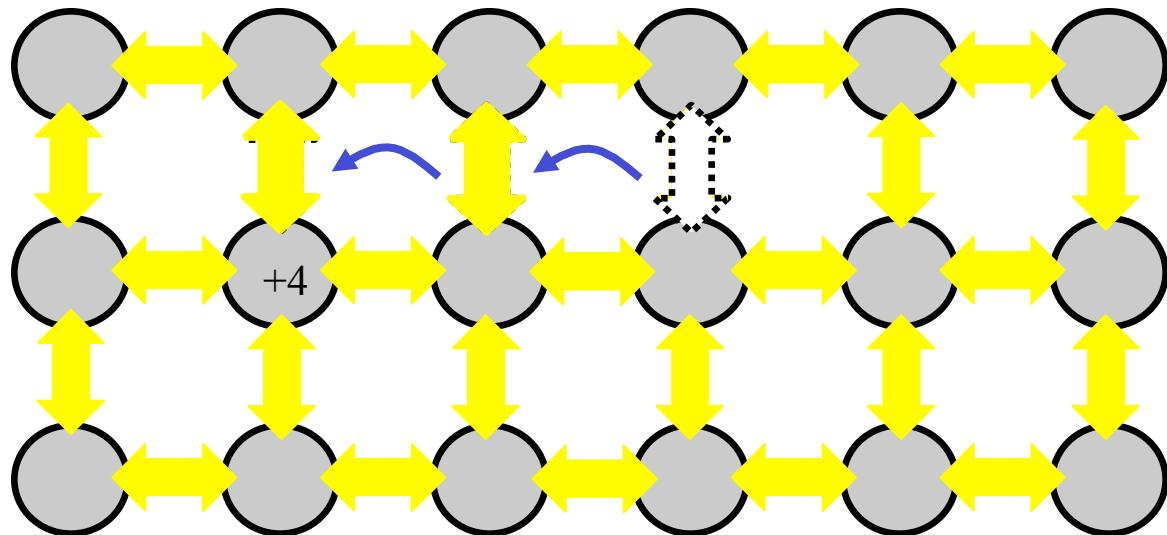


Donor impurity – one that gives up an extra electron.

Note: the crystal is still electrically neutral (no net charge) !!

# Electrons and holes

Consider a lattice where one electron has been freed from its bond, and has moved away, leaving a vacancy.



If electrons cascade from the right to the left, filling the vacancy...

then, effectively, the vacancy (with a + charge) moves from the left to the right...

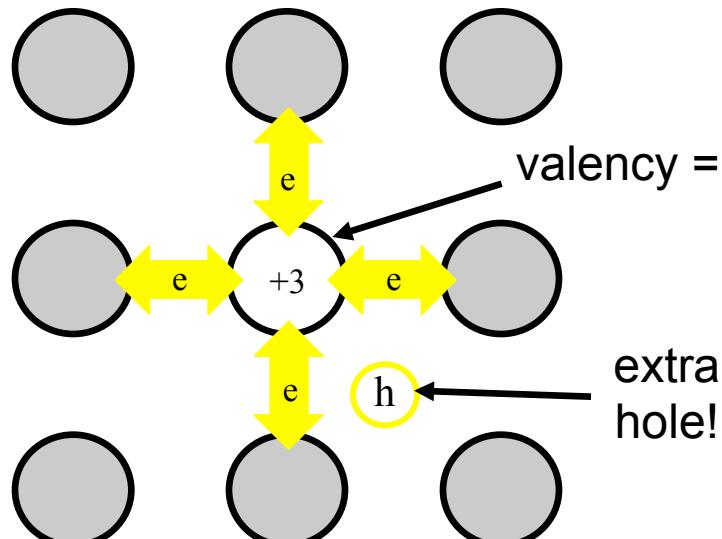
→ POSITIVE CURRENT TO THE RIGHT!!

Conduction in semiconductors can occur via electrons (with negative charge) or holes (with positive charge), or both.

# Acceptor impurities - holes

We saw that adding a valence-5 atom can give us extra electrons.

We can also create extra holes by adding a valence-3 atom.



Acceptor impurity – one less electron.

valency = 3 (one smaller than that of the silicon atoms)

Examples: aluminum, gallium

This extra hole acts just like an extra electron from a donor impurity, except with a positive (instead of negative) charge.

# Donors and acceptors

Intrinsic semiconductor – one with no impurities intentionally added

*n*-type semiconductor: donors added.

$$N_e > 0, N_h \approx 0.$$

*p*-type semiconductor: acceptors added.

$$N_h > 0, N_e \approx 0.$$

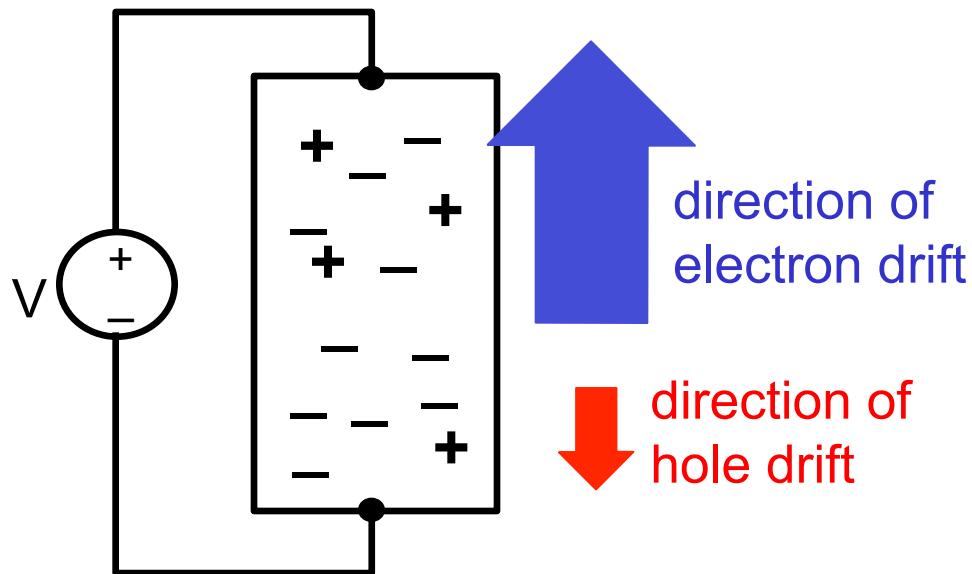
Compensated semiconductor: both donors and acceptors added, in approximately equal amounts.

$$N_e \approx N_h > 0.$$

Partially compensated semiconductor:  $N_e \neq N_h \neq 0$ .

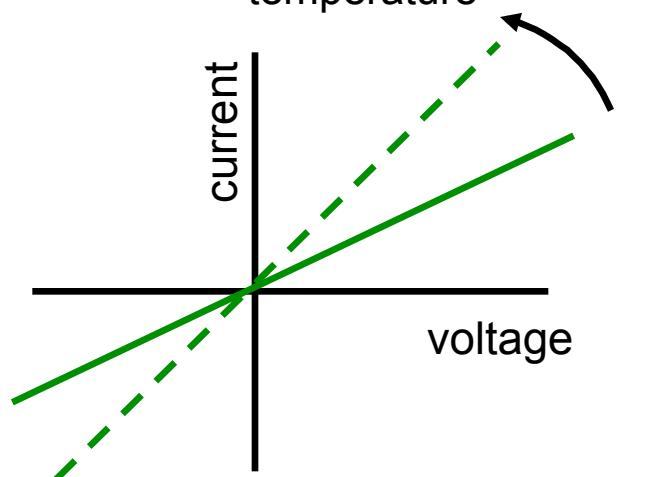
# Ohm's Law and semiconductors

A homogeneous semiconductor is *ohmic*.  
(That is, the plot of current vs. voltage, the I-V curve, is a straight line. Ohm's law,  $V=IR$ , applies.)



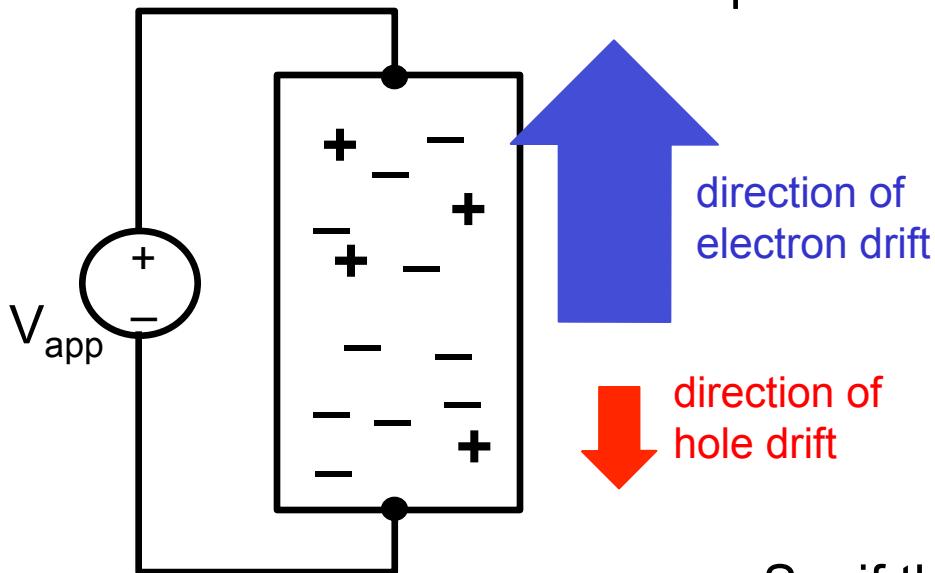
In this illustration, the semiconductor has  $N_e > N_h$ .

slope increases with increasing:  
donor concentration  
acceptor concentration  
temperature



# Drift currents – response to an applied voltage

“Drift current” – the net current that flows as the charge carriers (electrons and holes) respond to a voltage.



In this illustration, the semiconductor has  $N_e > N_h$ .

Recall that current is:  $j = N e v_{ave}$   
where:

$N$  = number of charge carriers (per unit volume)  
 $e$  = the charge on them  
 $v_{ave}$  = their average velocity

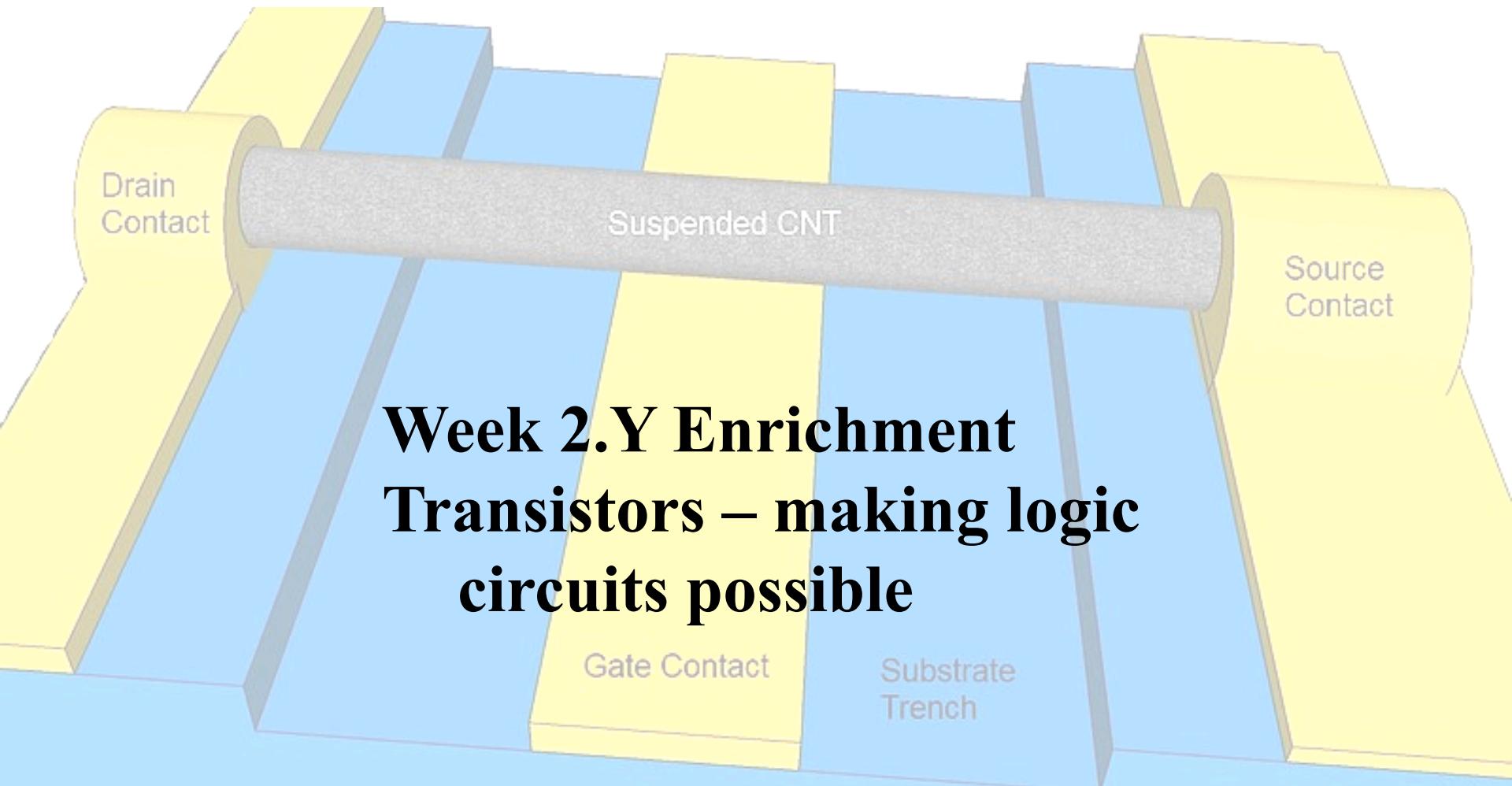
So, if the velocity of the electrons points up, then  $j_{electrons}$  points down, since for electrons,  $e$  is negative.

→ net drift current:  $j_{drift} = j_{electrons} + j_{holes}$   
points down in this picture.

# Your Take-Home Lessons

- Current in semiconductors can be carried either by electrons or holes (which have opposite charges)
- Impurities in semiconductors can be either “donors” – giving up an extra electron – or “acceptors” – creating an extra hole.
- “Drift” currents – the motion of charges in semiconductors when a voltage is applied

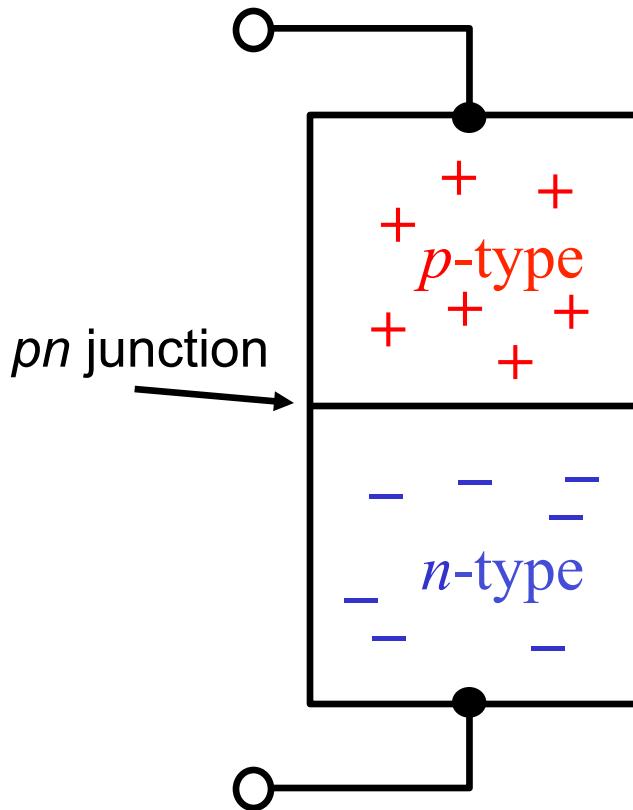
# Nano-Electronics



**Week 2.Y Enrichment  
Transistors – making logic  
circuits possible**

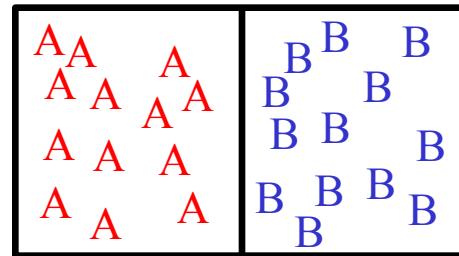
# The *pn* junction

What happens if we put *p*-type silicon next to *n*-type silicon, creating a junction?

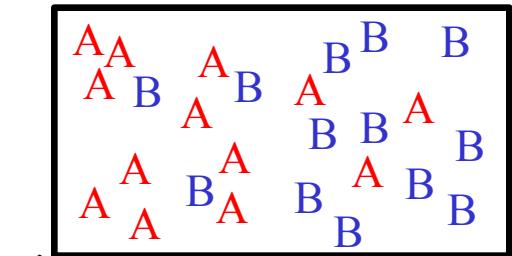


This is exactly analogous to putting containers of two different gases next to each other.

Two different gases in adjacent boxes



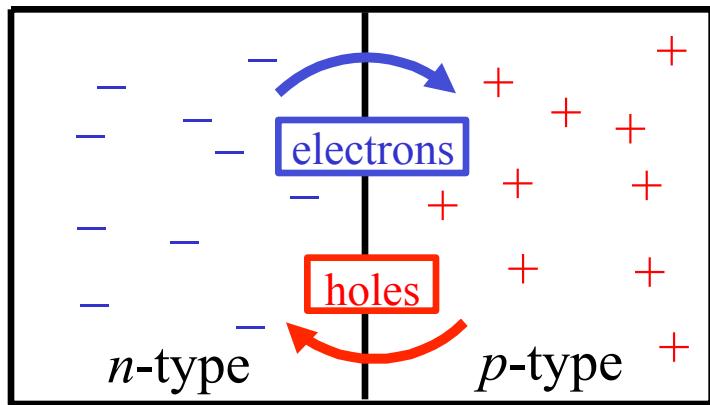
diffusion of A to the right, and B to the left



remove the partition

"Diffusion current" – the net current that flows due to the tendency of charge carrier concentrations to equalize in a volume

# The *pn* junction



Electrons diffuse to the right  
(which corresponds to a current  
flowing to the left)

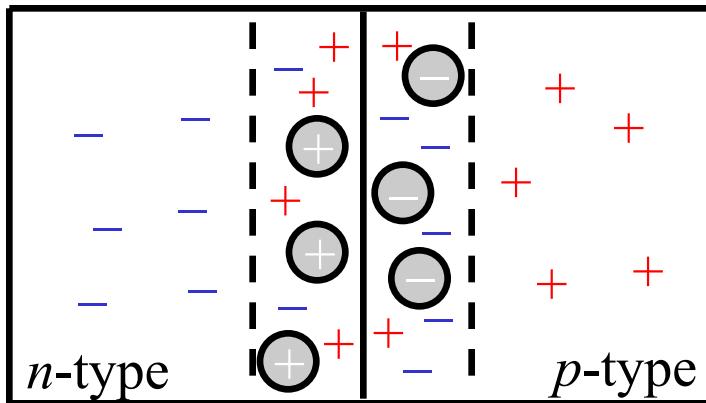
Holes diffuse to the left  
(which also corresponds to a  
current flowing to the left)

net diffusion current:  $j_{\text{diff}} = j_{\text{electrons}} + j_{\text{holes}}$  points to the left.

Note: diffusion current will flow, even if there is no applied voltage,  
until the carrier concentration is constant throughout.

# The depletion region

The region near the junction is interesting.



Diffusing **electrons** leave behind fixed positive charges.

Diffusing **holes** leave behind fixed negative charges.

- Recombination of free electrons with free holes leaves the area very close to the junction *depleted* of mobile charge carriers.
- The left-behind fixed charges give rise to a voltage. In the above diagram, that voltage pushes electrons to the left and holes to the right (i.e., in the opposite direction from the diffusion).
- These new drift currents, which oppose the diffusion currents, grow until they are large enough to cancel the diffusion currents.

# Why does this matter?

The depletion voltage – that is, the voltage that spontaneously appears across the depletion region due to diffusion – is the key to making devices.

A voltage applied from outside can either increase the depletion voltage or oppose (and thereby diminish) it, depending on the sign.

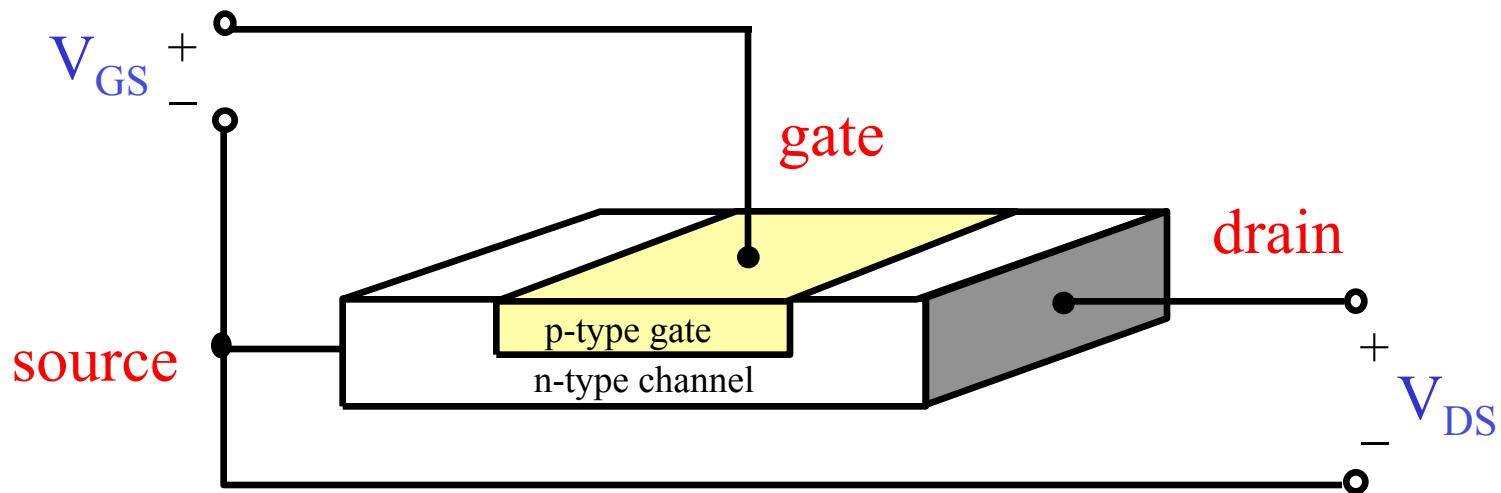
That means: we can control the thickness of the depletion region by applying an external voltage across the *pn* junction.

- if the applied bias reinforces the depletion voltage: the depletion region gets thicker. Since it contains few mobile charges, no current can flow across it.
- if the applied bias opposes the depletion voltage: the depletion region gets thinner. Current can flow across the thin depleted zone.

This is the basis upon which transistors and diodes work.

# A key example: the field-effect transistor (FET)

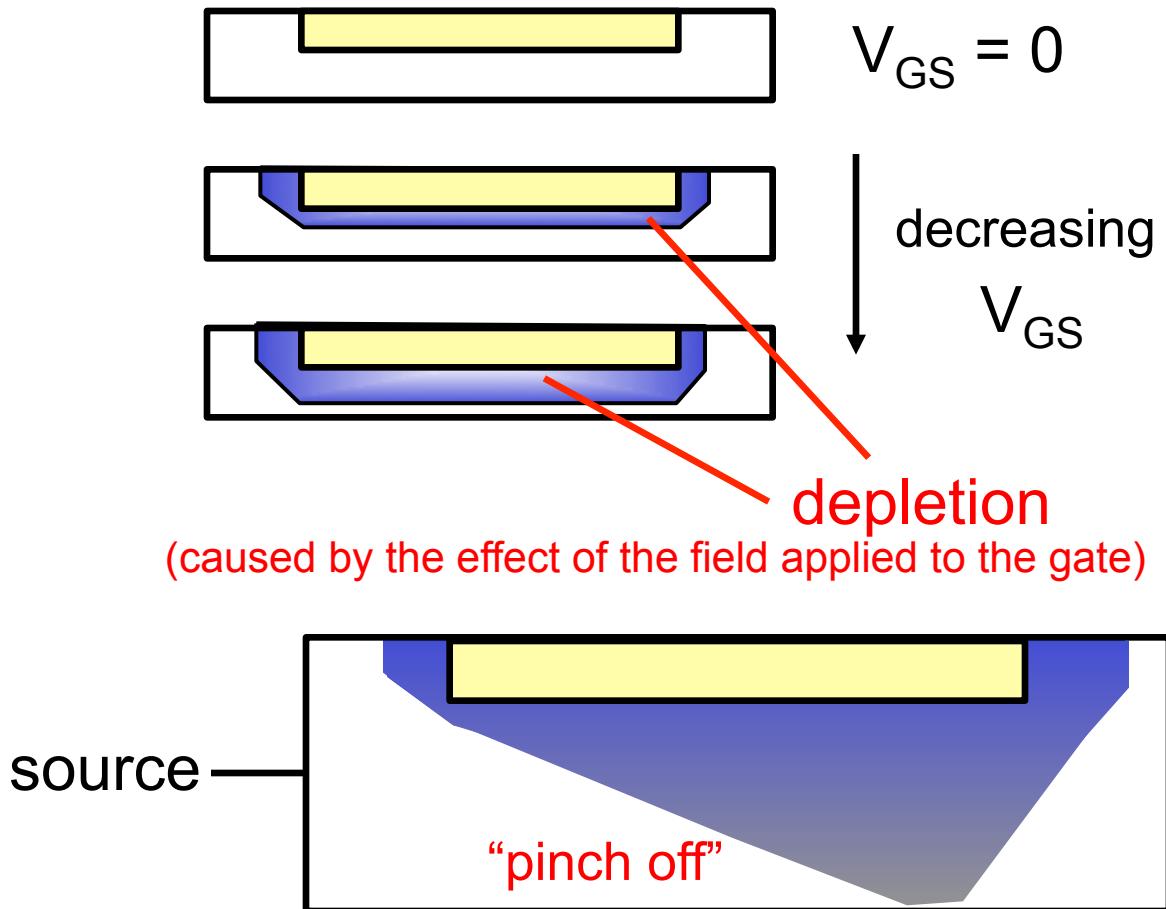
A transistor is a three-terminal device.



In the usual operation, the gate is biased negative, so that there is a large depletion region and no current flows through the gate electrode.

Even though no current flows through the gate, it still controls the amount of current that flows from source to drain.

# FET operation



When  $V_{GS} = 0$ , the channel between source and drain is large.

As  $V_{GS}$  decreases, the depletion region grows, making the channel smaller. Current flows less easily from source to drain.

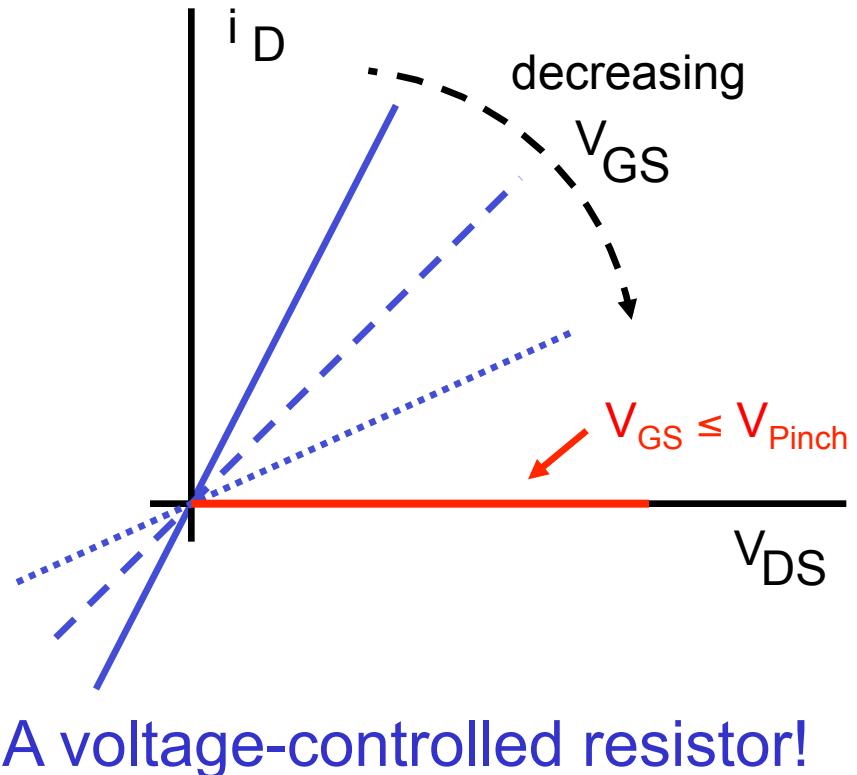
When  $V_{GS}$  is negative enough, the channel is **pinched off**, and no current flows from source to drain.

Pinch-off:  $V_{GS} < V_{Pinch}$

# A FET is a voltage-controlled resistor

For reasonably small values of  $|V_{DS}|$ , the drain current  $i_D$  is proportional to the voltage  $V_{DS}$ ; that is, the device behaves as a resistor between source and drain.

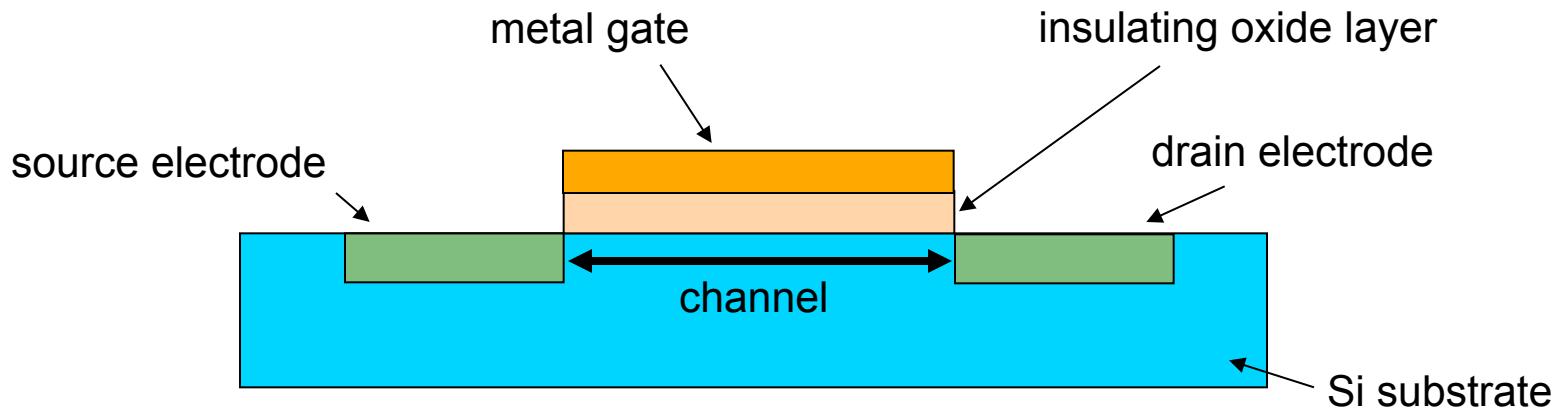
The resistance (the inverse of the slope of the line) is determined by the gate voltage.



This allows us to control the flow of current from source to drain, without dissipating any power in the gate (since the gate current is always zero).

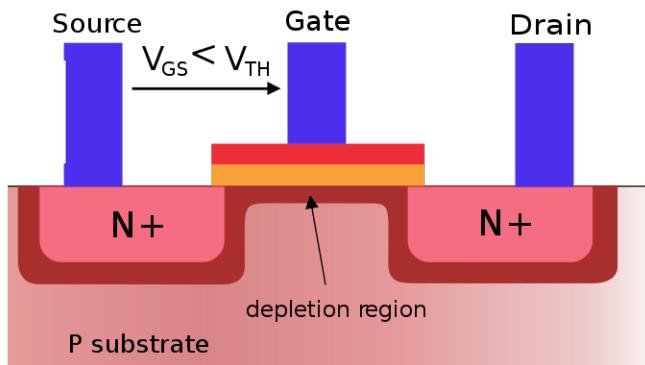
# MOSFETs

MOSFET: Metal-oxide-silicon FET



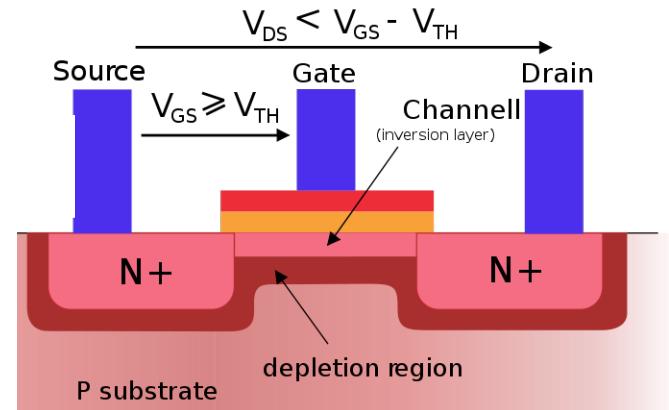
- replaces the doped silicon gate with a metal and a thin insulating layer (oxide)
- operating principle is similar
- MOSFETs are the most commonly used form of transistors

# MOSFET operating regimes



Source: Wikimedia commons

No current flows.



Linear operating region (ohmic mode)

Current flows  
through the channel.

# Your Take-Home Lessons

- Putting a  $p$ -type semiconductor adjacent to an  $n$ -type semiconductor creates a  $pn$  junction.
- The region near the junction becomes depleted of charge carriers.
- We can use a voltage to control the thickness of the depletion region. This is the basis by which transistors and diodes operate.
- MOSFET: the most common transistor architecture