Design of an 8X8 bit SRAM Array with Row Decoder for low-power applications

Sudeep Asundi
Department of Electronics and Communication Engineering
KLE DR. M. S. Sheshgiri College of Engineering and Technology
Belagavi, India
sudeepasundi15@gmail.com

Ruman M Mudenur
Department of Electronics and Communication Engineering
KLE DR. M. S. Sheshgiri College of Engineering and Technology
Belagavi, India
rumanmudenur@gmail.com

Prof. Niranjan Muchandi
Department of Electronics and Communication Engineering
KLE DR. M. S. Sheshgiri College of Engineering and Technology
Belagavi, India
niranjanmuchandi.mss@kletech.ac.in

***Abstract*— Volatile memory, or SRAM, is widely used in embedded systems such as digital signal processing (DSP), video, microcontrollers, silicon-on-a-chip (SoC), field programmable gate arrays (FPGA), and microcontrollers. Because of its many features, including fast read-write access, low power consumption, huge storage density, and stability, it can be used in register, cache, and cache-less applications. By using CMOS SRAM cells, read and write times are shortened and power consumption is greatly reduced. Stability can be improved and these processes are accelerated by increasing cell ratios. One way to reduce power usage is to use PMOS transistors with shorter widths. This paper presents a 6T SRAM cell architecture designed to reduce power consumption, latency, and read/write times. Additionally, an array of 8 X 8 cells has been devised to align with our primary objectives. The paper delineates the design principles of SRAM at the 180nm technology node, elucidating the functionality and operation of peripheral building blocks. Detailed schematics, created using the Cadence Virtuoso design tool, illustrate the peripheral circuitry and SRAM cell design.**

Keywords—CMOS, SRAM, CADENCE, GPDK, nMOS, pMOS, BL, BLB.

1. INTRODUCTION

SRAM circuits are engineered to facilitate both the writing and reading of data bits stored within the memory array. This type of memory is deemed static because it can preserve stored data indefinitely, provided a sufficient power supply voltage is maintained, eliminating the need for periodic refreshing operations.

Here we present the circuit structure and the operation of simple SRAM cells, as well as the peripheral circuits designed to read and write the data. The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states).

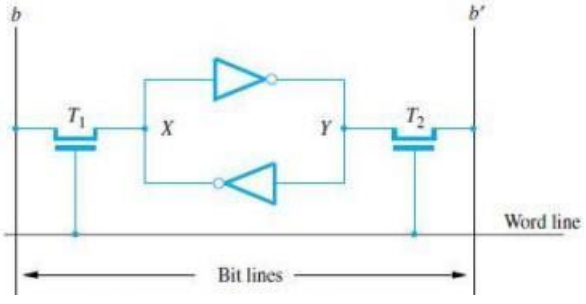

Fig.1. A Static RAM Cell

The two-inverter latch circuit's sustained state determines whether the data stored in the memory cell is interpreted as a logic "0" or a logic "1". At least one switch driven by the appropriate word line (row address selection signal) is needed to provide bit line access to data stored in the memory cell, both for reading and writing. Usually, to connect the 1-bit SRAM cell to the complementary bit lines (columns), two complementary access switches made of nMOS pass transistors are used. This system is comparable to using both hands to steer an automobile in complementary directions.

2. SRAM ARCHITECTURE

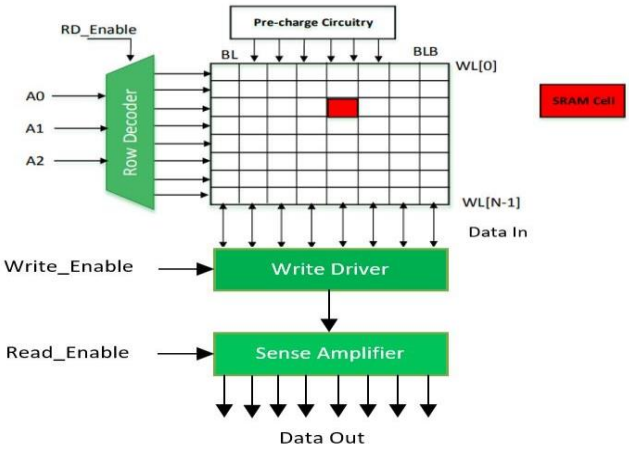

Fig.2. SRAM block diagram

The SRAM building squares are as per the following.

- SRAM cell.
- Pre-Charge Circuit.
- Write Driver Circuit.
- Sense Amplifier.
- Row decoder.

3. 6T SRAM CELL

The 6T SRAM architecture incorporates six transistors, consisting of two PMOS and four NMOS transistors. These components are arranged to form a cross-coupled inverter, with two NMOS transistors connected to the bit lines. These NMOS transistors, termed "access transistors," are regulated by the word line. Compared to the 4T and 5T configurations, the 6T design mitigates many limitations, particularly enhancing noise immunity. Static power dissipation in 6T

SRAM is minimal, as the cell draws power from the supply solely during switching operations. However, in the idle state, leakage current in deep-submicron technology poses challenges, impacting data retention at low operating voltages. In detail, the 6T SRAM comprises two PMOS transistors (M1 and M3) acting as load transistors, two NMOS transistors (M2 and M4) serving as driver transistors, and two NMOS transistors (M5 and M6) functioning as access transistors.

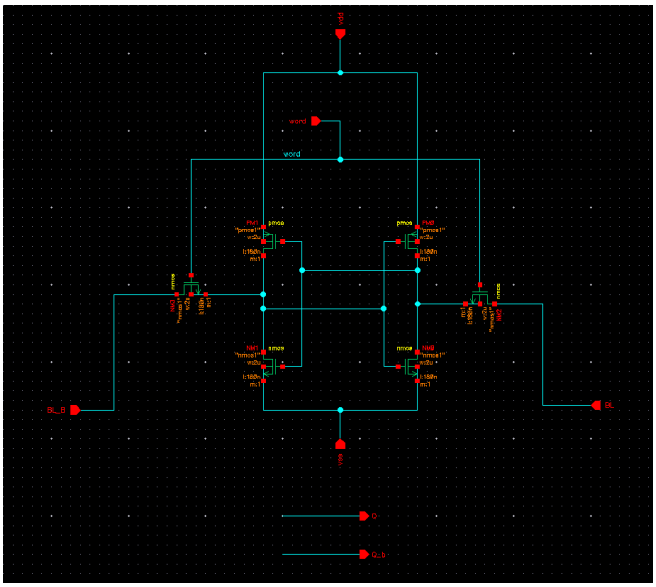

Fig.3.1. Schematic of 6T SRAM cell

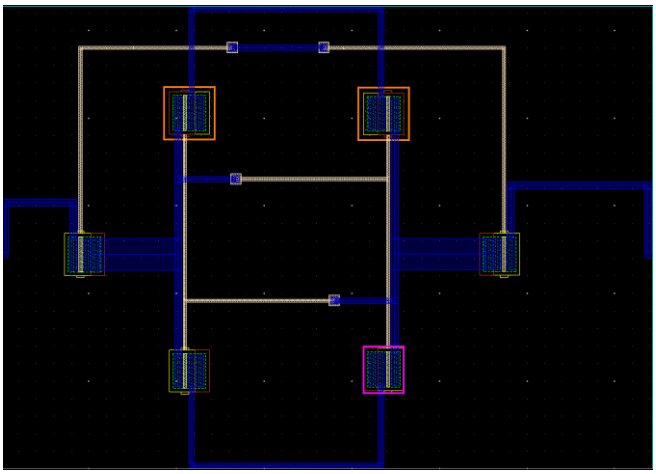

Fig.3.2. SRAM cell Layout

4. PRE-CHARGE CIRCUIT

The pre-charge circuitry charges both bit lines (BL and BLB) to VDD before a read operation. Accurate reading requires exact equalization between the bit lines, which calls for the use of two PMOS transistors, M1 and M2. The equalization transistor, or M1, is essential for removing asymmetrical flaws and guaranteeing accurate read operations. It is crucial for minimizing voltage differences between the bit lines since it shortens the pre-charge period and makes sure that BL and BLB attain almost equal potentials.

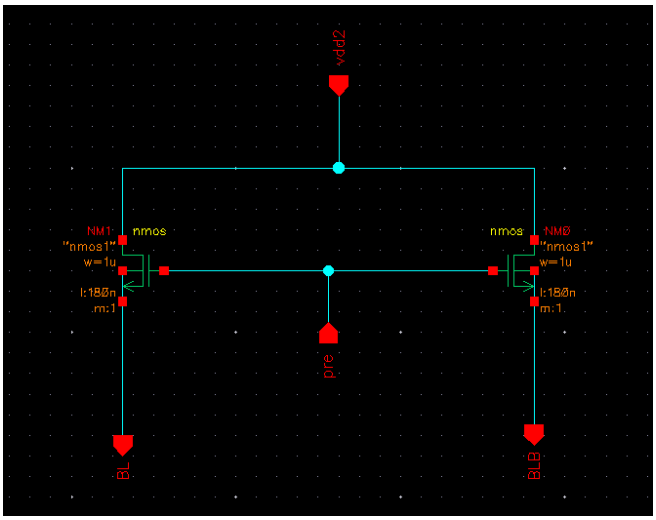

Fig.4.1. Schematic of Pre-charge circuit

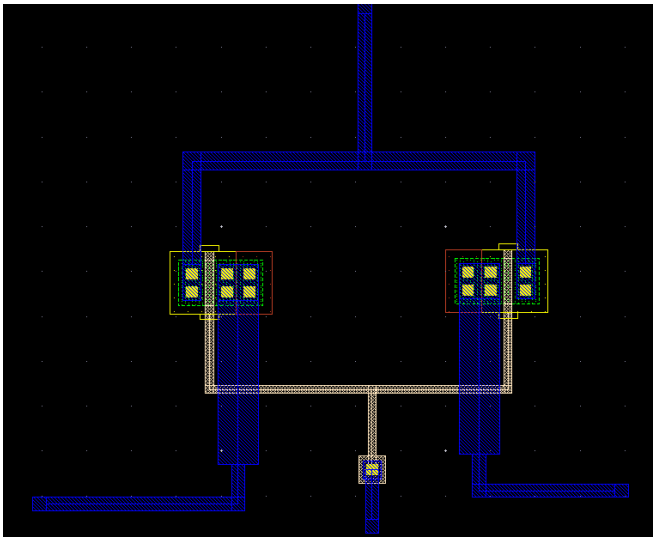

Fig.4.2. Schematic of Pre-charge circuit

5. WRITE DRIVER

The write driver is an essential component that makes it easier for data to be written into the SRAM cell via the access transistors. The write driver modifies the bit lines by the input data. For example, the write driver maintains BLB at VDD and pulls the BL down to GND if the data is 0. On the other hand, if the data is 1, transistor M3 of the write driver pushes BL up to VDD, and transistor M2 pulls BLB down to GND. Data must initially be applied to the data input pin in order to be written into a memory cell. Next, pull the designated address column low, enable the write line (write enable), and activate the word line to choose the cell's matching row and column coordinates. For power-saving purposes, the word line is turned off once the data has been successfully saved in the cell. Moreover, the write driver transistors are intentionally designed to be stronger than the relatively weak transistors of the cell. This design decision guarantees that the data that arrives can successfully overwrite the previously saved state in the memory. Therefore, careful transistor scaling is essential to guarantee the seamless functioning of the complete system.

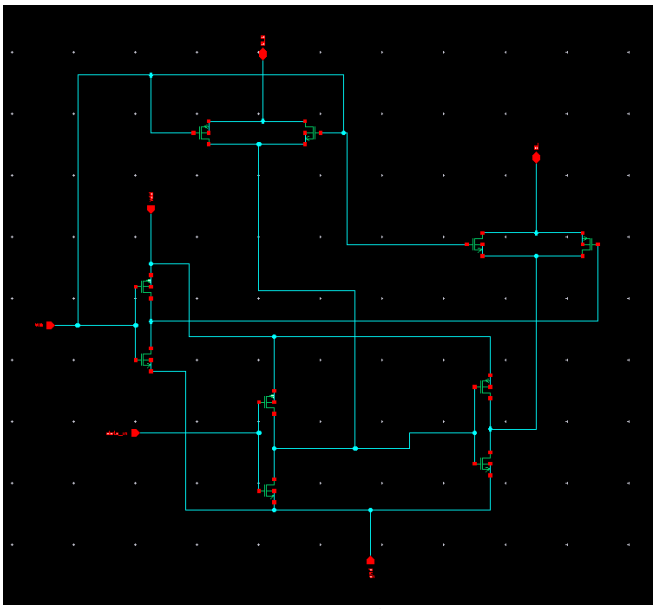

Fig.5.1. Schematic of Write Driver

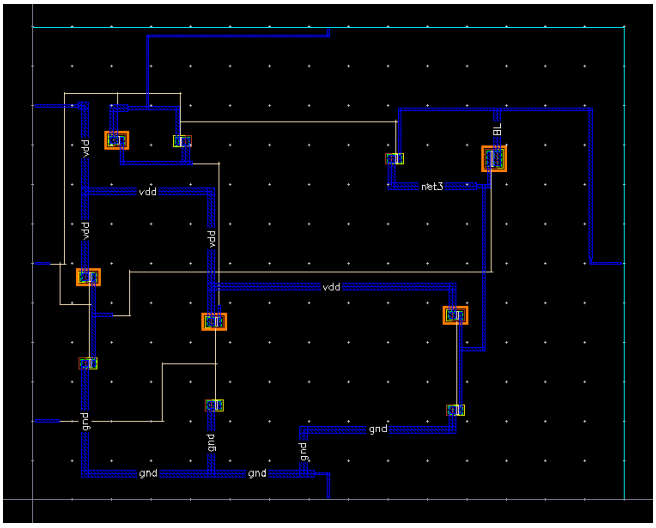

Fig.5.2. Layout of Write Driver

6. Sense Amplifier

The sense amplifier plays a crucial role in the SRAM block, swiftly detecting and amplifying a minute voltage discrepancy in the bit lines during the reading process. This amplification brings the voltage close to VDD, expediting the read operation significantly. Unlike DRAM cells, which necessitate constant refreshing due to their destructive sensing, SRAM's non-destructive sensing ensures efficient operation. Consequently, the robustness of the sense amplifier becomes pivotal. The chosen design profoundly influences various aspects including bit line sensing robustness, read speed, reliability, and power consumption. Sense amplifiers are instrumental in mitigating delays in logic circuits burdened with heavy capacitance.

Within the amplifier circuit, transistors M4 and M8 function as common source differential amplifiers, facilitating the operation of the cross-coupled inverter pair. This configuration triggers regenerative feedback, resulting in one output going low while the other goes high. To conserve power during read operations, it's prudent to deactivate the word lines and sense amplifier once an adequate differential voltage is attained. Additionally, terminating data sensing at the output on the bit lines aids in power conservation. Design considerations for the sense amplifier encompass several factors: ensuring a small input differential voltage, resilience to process variations such as noise, temperature, and voltage fluctuations, critical transistor sizing for symmetry, and minimizing the overall footprint.

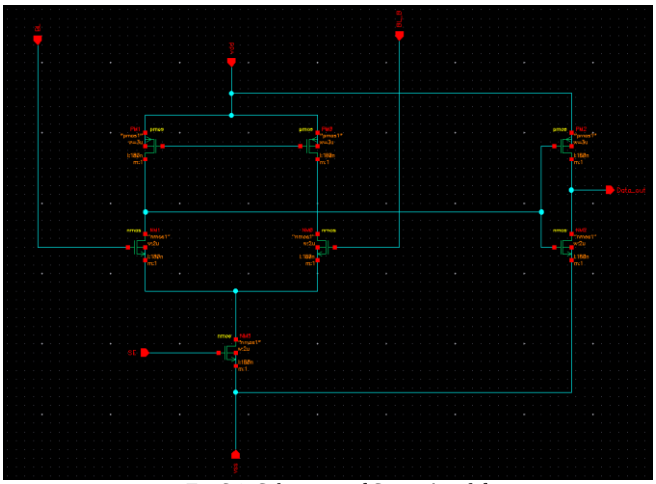

Fig.6.1. Schematic of Sense Amplifier

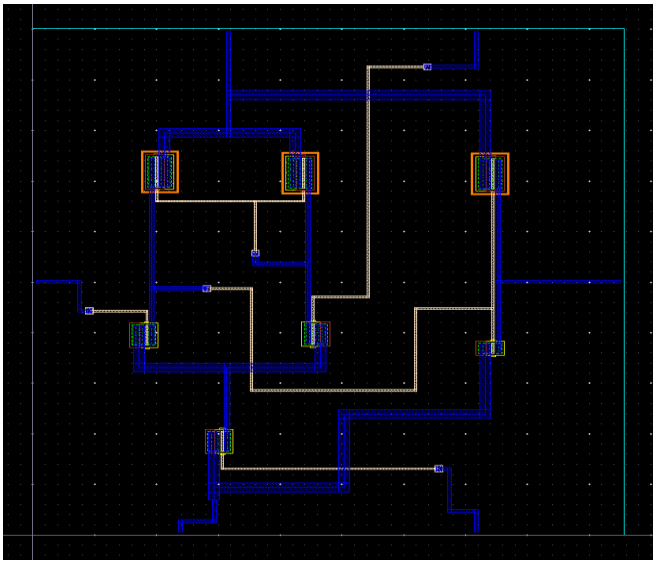

Fig.6.2. Sense Amplifier Layout

7. 3:8 Row Decoder

Each address row is assigned an independent 2N line by the 3:8 decoder. The word row in the SRAM array receives the decoder's output, which indicates which row is active. The row decoder that was employed is shown in Figure 7.

The decoder plays a critical role in SRAM architecture since it pinpoints the precise place inside the memory array that is organized into rows and columns. A sequence of NAND gates make up the row decoder, which accepts N user inputs to decode up to 2N distinct rows. Similar to this, choosing the exact cell in the array depends on the column

decoder. Considering the bit line wire length and the diffusion capacitance of each pass transistor linked across the word line, it is incredibly effective at word design. The column address is decoded bit by bit, with the last bit determining which column is picked. The first few address bits reflect the row address, and the remaining few bits represent the column address. This paper uses a 3:8 row decoder, with the output connected to the array's word line. Address decoders in memory design enable a specific row or column by decoding the specified address. The row and column decoders choose a certain word line (WL) and word enable (WE) from an SRAM array, respectively. Figure 7 displays a decoder with three inputs (a, b, and c) and eight outputs (Y0–Y7). This study uses an AND gate-based decoder.

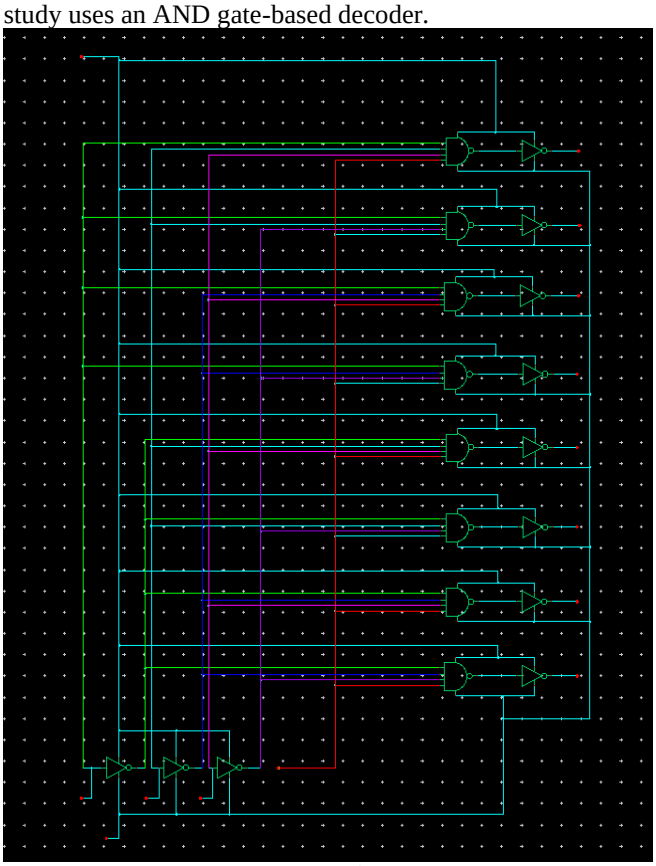

Fig.7.1. Schematic of 3:8 Row Decoder

TABLE 1. 3:8 DECODER AND OUTPUT SELECTION

Inputs			**Output Selection WL/ WE (As selection)**
A	B	C	
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

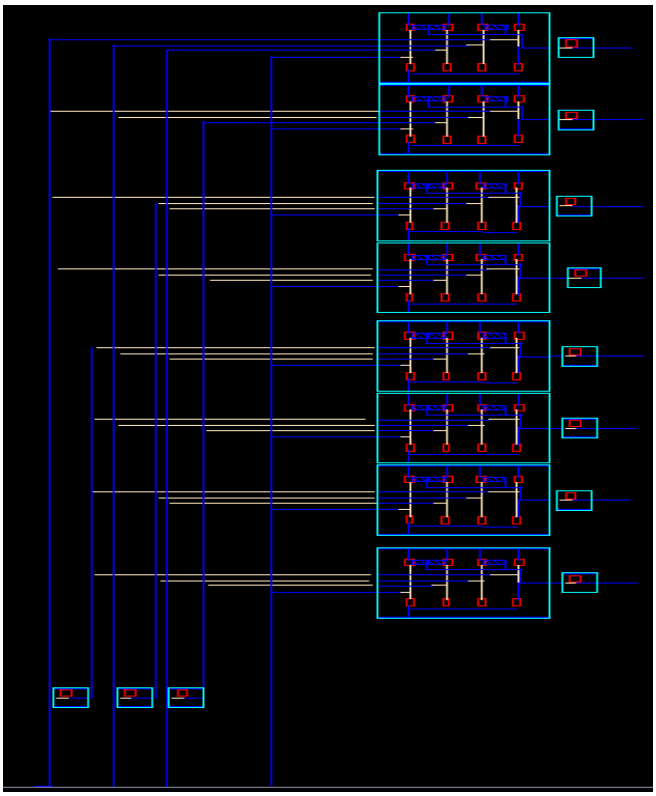

Fig.7.2. 3:8 Row Decoder Layout

8. SRAM ARCHITECTURE DESIGN

The provided figure illustrates the finalized SRAM Architecture, serving as the conclusive segment of the paper. This architecture comprises 64 cells arranged in an 8 x 8 configuration of 6T SRAM units as its primary component. Additionally, it incorporates an array of eight write driver units and pre-charge circuitry situated at the topmost section. Furthermore, a set of sense amplifiers is integrated into the design.

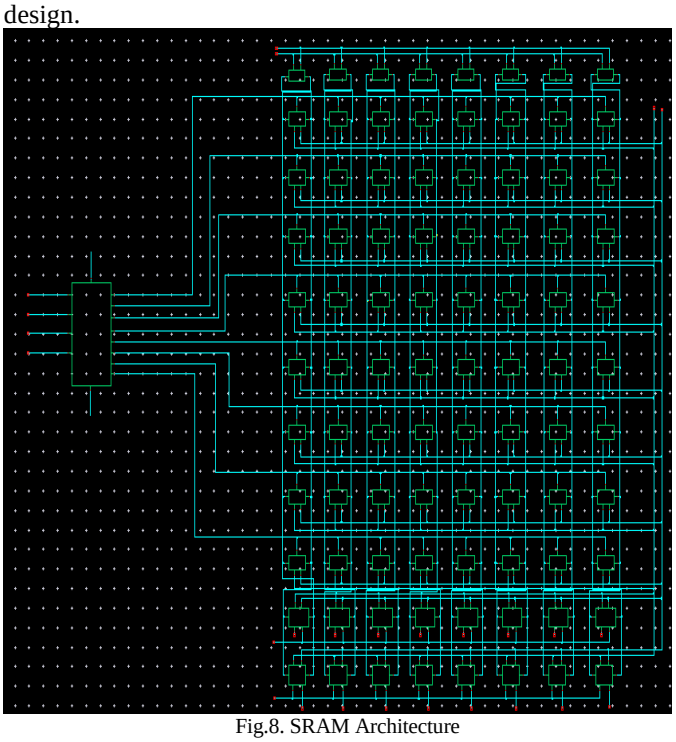

Fig.8. SRAM Architecture

A crucial element preceding the SRAM cells within the architecture is the 3:8 Decoder. This decoder facilitates the selection of a specific row of 8 bits within the SRAM array by utilizing a 3-bit address for read-write operations. Each column of SRAM cells is equipped with dedicated read and write circuitry. The enable pin is consistently maintained at logic high (1), and the necessary VDD and GND connections are correctly established. Moreover, input is supplied to the decoder to designate rows for operation. Finally, an 8-bit input is introduced to the circuit, subsequently read, and written into the SRAM cells.

9. Simulations and Results

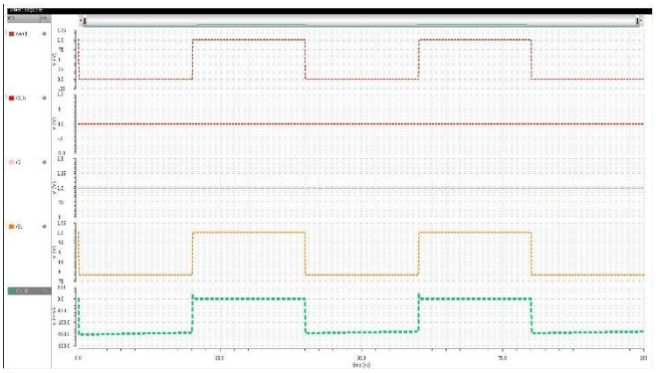

Fig.9.1. SRAM read test simulation

Fig.9.2. SRAM write test simulation

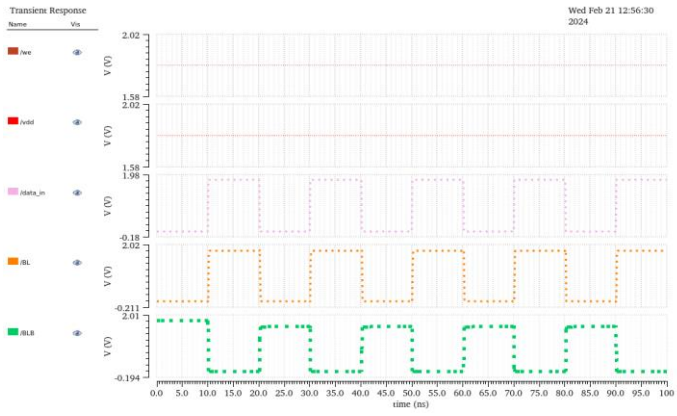

Fig.9.3. Write Driver test simulation

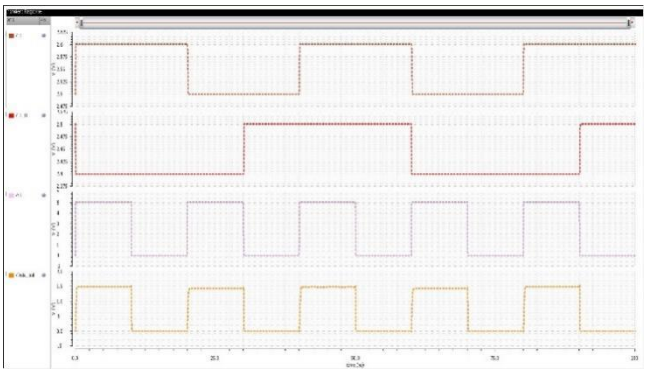

Fig.9.4. Sense Amplifier test simulation

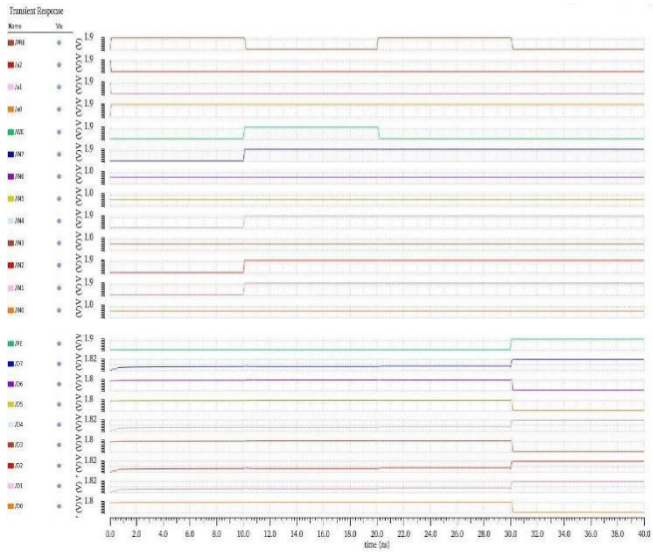

Fig.9.5. SRAM whole system simulation

TABLE 2. OBTAINED RESULTS

Parameters	**Result obtained from Proposed design**
Process Technology	180nm
Power supply voltage	1.8v
Pre-charge voltage	0.9v
Power consumption	3.14mW
Read Delay	196ps
Write Delay	830.5ps

10. Conclusion

In conclusion, the proposed design of an 8x8 bit SRAM array with a row decoder for low power applications demonstrates significant advancements in both performance and power efficiency. Utilizing a 180nm process technology with a power supply voltage of 1.8V and a pre-charge voltage of 0.9V, the design achieves notable reductions in power consumption while maintaining competitive read and write delays. With a power consumption of 3.14mW, read delay of 196ps, and write delay of 830.5ps, the proposed SRAM array showcases its potential for integration into energy-efficient systems where low power consumption is paramount. These results underscore the viability of the design for contemporary applications demanding both performance and

power efficiency, positioning it as a promising solution for future low-power embedded systems and IoT devices.

REFERENCES

[1] Ezeogu Chinonso Apollos – "Design Principles of SRAM Memory in Nano-CMOS Technologies", International Journal of Computer Applications (0975 – 8887) Volume 178 – No. 11, May 2019 J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[2] Ming-Hwa Sheu, S M Salahuddin Morsalin, Chang-Ming Tsai, Cheng-Jie Yang, Shih-Chang Hsia, Ya-Hsin Hsueh, Jin-Fa Lin and Chuan-Yu Chang – "Stable Local Bit-Line 6 T SRAM Architecture Design for Low-Voltage Operation and Access Enhancement", Published: 15 March 2021 K. Elissa, "Title of paper if known," unpublished.

[3] Shivani Yadav, Neha Malik, Ashutosh Gupta and Sachin Rajput – "Low Power SRAM Design with Reduced Read/Write Time", October 2013.

[4] L.Saranya, T.S.Divya, R.Manoranjitham, G.Arun Kumar, R.Karthick Krishnan – "A Survey on Low Power Comparison in SRAM Cell", International Journal of Pure and Applied Mathematics Volume 118 No. 20 2018, 611-616.

[5] M. S. Warde, V. C. S., M. P. Wagh, and S. Parshionikar, "Design and Analysis of 8x8 Static RAM," *International Journal of Scientific & Engineering Research*, vol. 4, no. 5, pp. 1-6, 2013.

[6] Akshay J A, Amith Chavan R, Chethan S P, Dr. S V Sathyanarayana, "Design and VLSI implementation of SRAM memory array using Application-specific Integrated circuits design flow," International Journal of Research in Advent Technology, vol. 2, no. 4, pp. 133-142, 2014.

[7] G. Naga Phanindra et al., "Novel Design and Implementation Of 8 X 8 SRAM Cell Array for Low Power Applications," International Journal of Engineering Research and Technology, 2017.

[8] G. Naga Phanindra et al., "Design and Analysis of Low Power 8x8 SRAM Memory Array," International Journal of Recent Advances in Research (IJRAR), 2016.

[9] V. Kursun et al., "Low-Power CMOS SRAM Cell Design Using Leakage Suppression Techniques," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006.

[10] S. Mukhopadhyay et al., "A Low Power 8T-SRAM Bit-Cell Design with Data Retention Enhancement for Low Voltage Operation," IEEE Transactions on Circuits and Systems I: Regular Papers, 2010.

[11] N. Sinha et al., "Comparative Analysis of Leakage Reduction Techniques in Low Power SRAM Design," International Journal of Computer Applications, 2017.

[12] S. R. Reddy et al., "Design and Analysis of Low Power 7T SRAM 8x8 SRAM Memory Array with Quit Bit Line Technique," Journal of Engineering, Technology, and Innovation, 2023.