A High-speed CMOS Comparator with 8-b Resolution

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ABSTRACT:

This project investigates the design, operation, and performance optimization of a high-speed CMOS comparator with 8-bit resolution, emphasizing speed, accuracy, and power efficiency. Aimed at modern analog-to-digital conversion applications, this comparator architecture utilizes a differential input stage followed by two regenerative flip-flops and an S-R latch. Distinctively, the design avoids offset cancellation techniques to minimize complexity and reduce both die area and power consumption, while achieving enhanced speed through careful circuit configuration and transistor sizing.

The methodology focuses on leveraging regenerative comparison through a two-phase clocking mechanism, which isolates reset and decision-making phases. During the reset phase, a common-mode voltage is established using an NMOS switch and precharge PMOS transistors, enabling symmetrical input conditions. In the regeneration phase, cross-coupled NMOS and PMOS transistors amplify small voltage differences, ensuring fast and robust decision-making. Optimizing the regeneration time constant through minimum channel lengths and balanced capacitances resulted in faster comparison speeds without compromising resolution.

The comparator was designed and fabricated using a 1.5-μm CMOS process with a compact die area of just 140 × 100 μm². Simulation and experimental validation demonstrated 8-bit resolution with input sensitivity as fine as ±4.9 mV across a dynamic range of ±2.5 V. The design achieves a sampling rate up to 65 MHz while consuming only 0.85 mW of power, outperforming prior CMOS comparators of similar resolution in terms of speed and efficiency. Detailed transient analysis confirmed reliable regeneration and minimized offset error, validating the suitability of the design for high-performance ADCs.

In conclusion, this project highlights a robust, low-power CMOS comparator capable of high-speed operation with high resolution. The architecture's simplicity, combined with effective optimization of layout and timing, underscores its practicality for use in sigma-delta modulators and flash ADCs. The work lays the groundwork for future enhancements in low-voltage, high-speed analog front-end circuitry.

1.0. INTRODUCTION

The comparator is a vital building block in modern analog and mixed-signal systems, especially in high-speed data converters such as flash and sigma-delta ADCs. A comparator's function—to determine the relative magnitude of two analog voltages and produce a binary output—is essential in converting continuous-time signals into discrete digital values. However, achieving both high speed and high accuracy in CMOS comparators has traditionally been challenging due to limitations such as device mismatches, offset voltages, and power constraints. As technology scales down and demand for high-performance ADCs increases, the need for fast, low-power, and accurate comparators becomes even more critical.

This project centers on the design and analysis of a high-speed CMOS comparator with 8-bit resolution, optimized for low power consumption and compact die area. The comparator architecture adopts a differential input stage followed by a pair of regenerative flip-flops and an S-R latch to achieve fast and reliable decision-making. Notably, the design avoids traditional offset cancellation techniques to simplify the architecture and reduce latency, enabling faster comparisons without sacrificing significant accuracy. Instead, the comparator leverages a carefully timed two-phase clocking strategy, allowing it to perform regeneration in two steps—first through an NMOS latch and then via a cross-coupled CMOS latch for full logic swing.

The distinguishing feature of this comparator lies in its dynamic operation. During the reset phase, the internal nodes are preconditioned to ensure symmetrical behavior, while in the regeneration phase, the initial voltage difference at the input nodes is amplified rapidly to reach valid logic levels. The comparator's response time and offset voltage are further optimized through meticulous transistor sizing, layout symmetry, and dynamic analysis of the regeneration process. This dual-phase regeneration approach significantly improves both speed and offset performance without introducing excessive complexity.

Implemented using a standard 1.5 μm CMOS technology, the designed comparator occupies only 140 × 100 μm² of die area and operates with a ±2.5 V supply. It demonstrates 8-bit resolution with a sampling rate up to 65 MHz and power dissipation of just 0.85 mW. These characteristics make it highly suitable for use in high-speed ADCs and low-power signal processing systems. The project also explores strategies to reduce input-referred offset voltage and kickback noise, ensuring robustness under fast switching conditions.

Through simulation and testing, this comparator design is validated for both speed and resolution, underlining its effectiveness in high-frequency, low-power applications. The project showcases how CMOS-based comparators can still meet modern design requirements through careful circuit-level optimization and dynamic operation strategies. This work contributes toward the ongoing development of energy-efficient and high-performance analog front-ends in advanced electronic systems.

1.1 Literature Review / Background (Optional)

The design of high-speed, low-power CMOS comparators has been a subject of extensive research due to their critical role in analog-to-digital conversion systems. Comparators are integral components in flash ADCs, sigma-delta modulators, and digital communication systems where fast and accurate signal decisions are essential. As performance demands continue to rise, particularly for high sampling rates and low voltage operations, the design trade-offs between speed, accuracy, power, and area become increasingly significant.

Early CMOS comparators often relied on static differential amplifier stages, which offered good accuracy but suffered from slower response times and higher power consumption. These architectures frequently incorporated offset cancellation techniques such as auto-zeroing or chopper stabilization to mitigate mismatch-induced errors. However, these methods added complexity, increased delay, and consumed additional silicon area and power, making them less suitable for high-speed applications.

To address these limitations, dynamic comparators emerged as a preferred solution in high-speed ADCs. These comparators exploit positive feedback regeneration to rapidly resolve small differential input voltages into full-swing digital outputs. The introduction of regenerative latching mechanisms significantly improved speed and reduced power consumption by eliminating static bias currents during the evaluation phase. Designs like the StrongARM latch became popular due to their simplicity and high speed, but they are often sensitive to input-referred offset and kickback noise.

The comparator architecture presented by Yin et al. (1992) introduced a novel solution that combines a differential input stage with two sequential regenerative phases and an S-R latch. This structure enables high-speed comparison without the need for explicit offset cancellation. The comparator operates dynamically using non-overlapping clock phases, enabling a clear separation between the reset and regeneration phases. The design achieves 8-bit resolution while occupying a minimal die area and consuming only 0.85 mW at 65 MHz—an impressive performance benchmark at the time, especially in a 1.5 μm CMOS process.

Several subsequent works have attempted to improve upon Yin's architecture by incorporating advanced calibration techniques, increasing sampling rates, or adapting to deep submicron technologies. However, many of these enhancements come at the cost of increased design complexity and power dissipation. Yin's design remains a strong reference point for comparator architectures that emphasize simplicity, efficiency, and speed—especially in moderate-resolution, high-speed applications.

This project builds upon the foundational concepts introduced in such prior works, focusing on implementing and analyzing a high-speed dynamic CMOS comparator without offset cancellation. By revisiting and optimizing this well-established architecture using modern simulation tools, the project aims to validate the effectiveness of the regenerative comparison approach and its suitability for current low-power, high-performance analog front-end systems.

1.2. CMOS Comparator

A CMOS comparator is a fundamental building block in analog and mixed-signal integrated circuits, designed to compare two input voltages and generate a digital output indicating which input is greater. These devices are widely used in analog-to-digital converters (ADCs), signal detection systems, and various control applications due to their high speed and low power consumption.

In this report, we focus on a high-speed CMOS comparator capable of achieving 8-bit resolution at a sampling rate of 20 Msamples/s. This design is optimized for both accuracy and energy efficiency, making it suitable for high-performance data acquisition systems.

Principle of Operation

A comparator operates by amplifying the voltage difference between two inputs and producing a logic-level output:

- If Vin+>Vin−V_{in+} > V_{in-}Vin+>Vin−, the output switches to a high logic level.
- If Vin+<Vin−V_{in+} < V_{in-}Vin+<Vin−, the output goes low.

This particular design consists of three main stages:

- **Preamplifier Stage** – A differential folded-cascode amplifier that provides initial gain and reduces kickback noise from later stages.
- **Decision Circuit** – A dynamic latch that quickly determines the polarity of the input difference and regenerates it into a full-scale logic signal.
- **SR Latch** – Holds the output value stable until the next comparison cycle.

1. Switching Behavior

The comparator rapidly switches its output based on tiny differences between the input voltages, achieving precise digital transitions even at high speeds. Its regenerative latch stage ensures fast decision-making with minimal static power consumption.

2. Design Equations and Parameters

The comparator design involves key parameters such as:

• Input-referred offset voltage
• Propagation delay
• Power dissipation
• Gain-bandwidth product of the preamplifier stage

Mathematically, for small input differences ΔV\Delta VΔV, the preamplifier's output can be modeled as:

Vout=Av·ΔVV_{out} = A_{v} \cdot \Delta VVout=Av·ΔV

Where AvA_vAv is the voltage gain of the preamplifier.

2.0. Objectives

1. **Design and Implementation of a High-Speed CMOS Comparator:**

    - To design and implement a high-speed CMOS comparator architecture capable of achieving 8-bit resolution while operating at clock frequencies up to 65 MHz. The design incorporates a differential input stage followed by two stages of regenerative latches and a static S-R latch to deliver rapid and reliable decision-making. The goal is to realize this design using a standard 1.5 μm CMOS process, ensuring compatibility with widely used fabrication technologies

2. **Optimization of Regeneration and Reset Mechanisms:**

    - To optimize the dynamic phases of the comparator—reset and regeneration—using non-overlapping clock signals. This involves precise sizing of the transistors responsible for regeneration (cross-coupled NMOS and PMOS pairs) and reset (NMOS switches and PMOS precharge transistors), enabling fast and clean transitions between states. A critical objective is to minimize the regeneration time constant while ensuring that the comparator resets fully and symmetrically to avoid hysteresis or decision errors.

3. **Minimization of Input-Referred Offset Voltage and Power Consumption:**

    - To reduce the input-referred offset voltage by employing a symmetric and layout-aware design approach, eliminating mismatch-related artifacts without the use of additional offset cancellation circuits. Simultaneously, the comparator is to be optimized for low static and dynamic power consumption—targeting a total power dissipation of less than 1 mW—through the use of dynamic operation, minimum-length transistors, and efficient current sourcing in the input differential pair.

4. **Simulation and Functional Validation of Comparator Performance:**

    - To simulate and validate the comparator under a wide range of differential input voltages and operating conditions using tools like SPICE or Cadence Virtuoso. The focus is on verifying functional correctness, propagation delay, regeneration speed, input sensitivity (down to ±5 mV), and output swing. Monte Carlo and parametric simulations may also be used to evaluate robustness against process variations and mismatch-induced errors.

5. **Assessment of Area Efficiency, Integration Capability, and System-Level Suitability:**

- To evaluate the comparator's layout area, input/output capacitance, and compatibility with ADC architectures such as flash and sigma-delta converters. The project aims to demonstrate that the proposed design can serve as a foundational building block in larger mixed-signal systems, where power, speed, and compactness are crucial. A secondary objective is to explore possible enhancements such as input sampling techniques or noise-reduction strategies to extend the design's utility in high-precision applications.

3.0. Methodology

The design methodology for the high-speed CMOS comparator is centered around achieving an optimal balance between speed, resolution, power consumption, and area efficiency. The comparator is implemented using a dynamic architecture that employs a differential input stage, two regenerative flip-flops (NMOS and PMOS based), and an S-R latch. The overall design flow is divided into multiple stages, including architectural planning, circuit-level design, transistor sizing, clock phase management, simulation, and performance evaluation.

1. Architectural Design of the Comparator

The comparator consists of three primary stages:

- **Differential Input Stage:**
  The front-end of the comparator includes a matched NMOS differential pair (M1 and M2) that converts the input voltage difference into a small differential current. This current develops an initial voltage difference across nodes *a* and *b*, forming the basis for subsequent regeneration.

- **Dynamic Regenerative Latch:**
  The heart of the comparator is a regenerative latch, composed of:
  - Cross-coupled NMOS transistors (M4 and M5)
  - Cross-coupled PMOS transistors (M6 and M7)
  - Reset transistor (M12)
  - Strobing NMOS transistors (M8 and M9)
  - Precharge PMOS transistors (M10 and M11)

These elements work together to quickly amplify the small voltage difference at nodes *a* and *b* to full logic levels.

- **S-R Latch:**
  A static set-reset latch follows the dynamic stage to hold the comparator output value after the regeneration phase ends. This ensures a stable and reliable digital output signal.

2. Two-Phase Clocking Scheme

A key innovation in the comparator design is the use of **non-overlapping two-phase clocks (ϕ1 and ϕ2)** to separate the **reset** and **regeneration** phases:

- **ϕ2 (Reset Phase):**
  The comparator's internal nodes are precharged, and any previously stored decision is

cleared. M12 is ON, ensuring nodes *a* and *b* are equalized. M10 and M11 precharge nodes *c* and *d*.

- **ϕ1 (Regeneration Phase):**
  M12 is turned OFF, and regeneration begins. The NMOS and PMOS latches amplify the voltage difference, pushing the output towards a full logic level. M8 and M9 then connect the NMOS latch to the PMOS latch for rapid regeneration.

This phased approach allows the comparator to make fast, low-offset decisions with improved timing control.

3. Transistor Sizing and Optimization

Transistor sizes are carefully chosen to balance speed, gain, and area. The minimum channel length (Lmin) is used for all transistors to maximize speed. The widths (W) of transistors are optimized based on:

- **Regeneration time constant (τ):**
  τ=Ca/(gm4−2go12)\tau = C_a / (g_{m4} - 2g_{o12})τ=Ca/(gm4−2go12)
  where CaC_aCa is the capacitance at nodes *a* and *b*, and gm4,go12g_{m4}, g_{o12}gm4,go12 are transconductance and output conductance of relevant transistors.
- **Reset Speed Condition:**
  Ensuring that the current through M12 is greater than through the cross-coupled latch during reset, typically: W12>14W4W_{12} > \frac{1}{4}W_4W12>41W4

Simulations and small-signal analysis are used to tune these sizes, with an emphasis on reducing offset and hysteresis.

4. Simulation Setup and Testing

The comparator is simulated using a SPICE-level simulator. The simulation process involves:

- **Transient analysis:**
  To observe the dynamic behavior of the comparator in response to changing input voltages.
- **DC sweep:**
  To evaluate offset voltage and switching characteristics.
- **Monte Carlo analysis:**
  To assess sensitivity to mismatches and process variations.
- **Load analysis:**
  To ensure compatibility with subsequent digital logic or ADC sampling stages.

Test conditions include:

- Supply Voltage: ±2.5 V
- Input Range: ±2.5 V
- Input Resolution Target: ~5 mV (for 8-bit precision)
- Clock Frequency: Up to 65 MHz
- Load Capacitance: Typical of a digital S-R latch stage

5. Layout and Area Estimation

A compact layout is implemented using standard 1.5 μm double-poly, double-metal CMOS process design rules. Special attention is paid to:

- **Symmetry in layout** (for matching M1–M2 and M4–M5)
- **Routing parasitics** (to minimize mismatch-induced offset)
- **Input pair placement** (to reduce kickback and charge injection effects)

Area is estimated based on standard cell footprint and custom layout measurements.

3.1. Problem Statement and Requirements

The problem addressed by this project is the growing demand for high-speed, low-power, and area-efficient analog-to-digital interface circuits, particularly comparators, in modern mixed-signal systems. Traditional comparator designs often face trade-offs between speed, resolution, power consumption, and design complexity—especially when offset cancellation circuits are used. These limitations can hinder the integration of comparators into compact, energy-efficient ADC architectures for high-performance applications.

This project explores a dynamic CMOS comparator architecture that avoids offset cancellation while still achieving 8-bit resolution at high sampling rates. The goal is to design a compact, fast, and low-power comparator suitable for use in flash ADCs, sigma-delta modulators, and other mixed-signal systems.

The system requirements for this project include:

- **Design of a high-speed dynamic CMOS comparator** with 8-bit resolution, utilizing a differential input stage, regenerative latches, and an S-R latch for digital-level output stability.
- **Optimization of regeneration and reset phases** using non-overlapping clock signals to ensure fast and reliable voltage decision-making.
- **Elimination of explicit offset cancellation techniques** while still maintaining low input-referred offset voltage through careful sizing and symmetrical layout.
- **Functional simulation and validation** of the comparator under various differential input conditions to verify logical correctness, speed, sensitivity, and power consumption.
- **Area estimation and performance benchmarking** to demonstrate suitability for integration into compact, low-power ADC designs.

3.2. Tools and Technologies Used:

The project was implemented using a custom analog design and simulation workflow centered around CMOS transistor-level circuit design and dynamic simulation tools. These technologies were selected to accurately model the transient behavior, timing characteristics, and regenerative properties of the high-speed comparator:

- **Cadence Virtuoso:**
  Used for schematic entry, transistor-level design, and simulation of the comparator architecture. Virtuoso enabled precise control over transistor sizing and layout-aware modeling of circuit behavior under different clock phases and input conditions.
- **Spectre Simulator (Analog Environment):**
  Integrated with Cadence Virtuoso to perform transient analysis, DC sweep, and Monte Carlo simulations. It was used to analyze the regeneration behavior, evaluate offset voltage, and verify the timing performance of the comparator under various operating conditions.
- **1.5 µm CMOS Process Design Kit (PDK):**
  A standard double-poly, double-metal CMOS technology was used to design the comparator. The PDK provided accurate models for parasitics, supply voltages, and device behavior, enabling realistic design and area estimation.
- **Custom Schematic Symbols and Layout Cells:**
  Comparator components—including the differential pair, regenerative latch, and S-R latch—were designed as modular cells to allow reuse, clean layout, and hierarchical simulation.
- **Non-Overlapping Clock Generation (ϕ1 and ϕ2):**
  A clock generation module was created to ensure proper timing between the reset and regeneration phases of the comparator. This was essential for the dynamic operation and stable output behavior.

4.0 Proposed Design and Explanation

The proposed design is a high-speed, low-power CMOS comparator capable of achieving 8-bit resolution. It is built using a dynamic architecture that avoids explicit offset cancellation, relying instead on a regenerative decision-making mechanism and a well-optimized clocking scheme. The design consists of three major functional blocks: the differential input stage, the dynamic regenerative latch, and the static S-R latch.

4.1 Differential Input Stage

The input stage comprises a matched pair of NMOS transistors (M1 and M2), which receive the differential input signals. This stage functions as a transconductance amplifier, converting the input voltage difference into a differential current. The current then develops a small voltage difference across nodes *a* and *b*, which acts as the seed for the subsequent regeneration phase.

This voltage difference is critical for initiating the comparator's decision-making process, and its accuracy directly affects the input-referred offset of the circuit. Careful transistor sizing and layout symmetry are employed to minimize mismatch between M1 and M2.

4.2 Regenerative Latch Circuit

Following the input stage is a dynamic regenerative latch, the core of the comparator’s speed advantage. It consists of:

- **Cross-coupled NMOS latch (M4, M5)**
- **Strobing NMOS switches (M8, M9)**
- **Reset NMOS transistor (M12)**
- **Cross-coupled PMOS latch (M6, M7)**
- **Precharge PMOS transistors (M10, M11)**

The regenerative process occurs in two steps:

1. **Reset Phase (ϕ2 high):**
   During this phase, the latch is reset. Transistor M12 is turned ON, equalizing voltages at nodes *a* and *b*. Simultaneously, M10 and M11 precharge the output nodes *c* and *d* to the supply voltage (VDD). This prepares the latch for the next decision cycle.
2. **Regeneration Phase (ϕ1 high):**
   M12 is turned OFF, and transistors M8 and M9 are enabled. The cross-coupled NMOS and PMOS pairs then regenerate the small voltage difference across *a* and *b*, rapidly amplifying it into full-swing logic levels at *c* and *d*. This dynamic operation ensures fast comparison without the need for bias currents or additional offset correction.

The design ensures that the comparator only draws current during switching, significantly reducing power consumption.

4.3 S-R Latch Output Stage

To hold the result of the comparison and convert the analog regeneration output into a stable digital signal, an S-R (Set-Reset) latch is used. It captures the final logic level difference from nodes *c* and *d*, ensuring a clean and reliable output until the next clock cycle. This allows the comparator to be directly interfaced with digital circuitry without the need for additional buffers or level shifters.

4.4 Timing and Clocking Considerations

A key feature of the proposed comparator is the use of **non-overlapping two-phase clocks (ϕ1 and ϕ2)**. These clocks precisely control the reset and regeneration intervals, avoiding race conditions and signal overlap. Proper clock timing ensures that the comparator resets fully before beginning a new decision cycle, maintaining consistent behavior even at high frequencies (up to 65 MHz).

4.5 Advantages of the Proposed Design

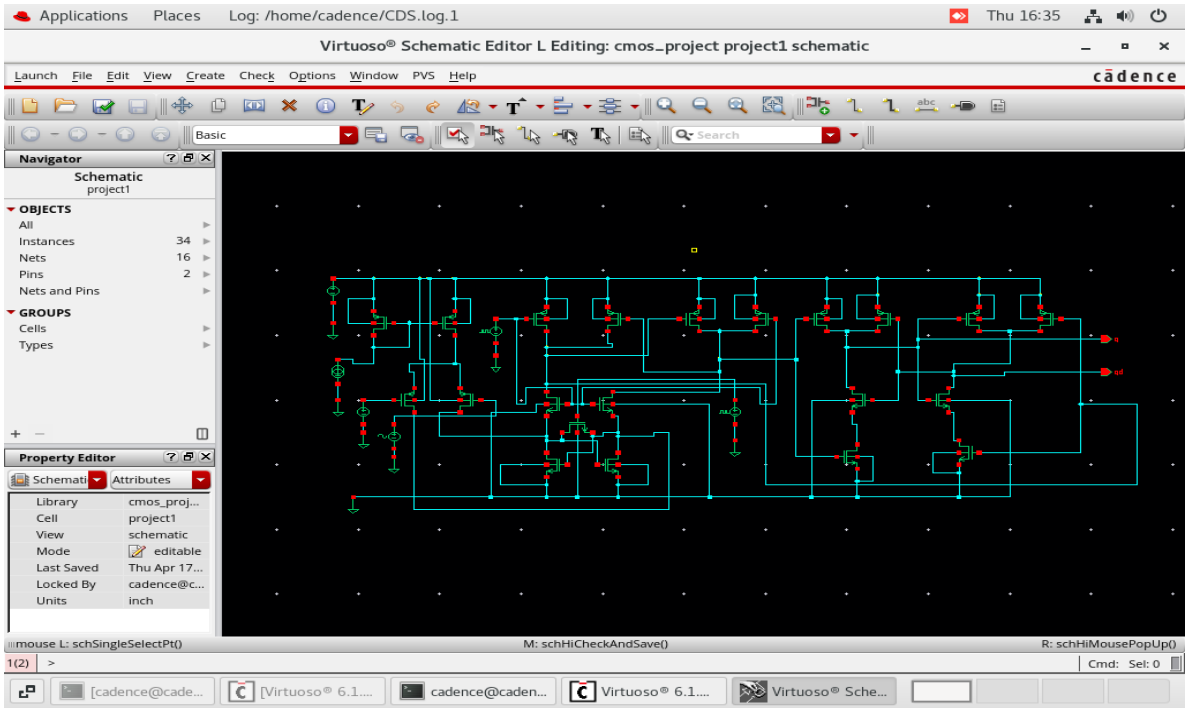
- **High-Speed Operation:**
  Fast regeneration due to dynamic latch and minimized parasitic capacitance allows rapid decision-making suitable for ADC applications.

- **Low Power Consumption:**
  The circuit operates dynamically, consuming power only during the evaluation phase. Static power consumption is minimal.

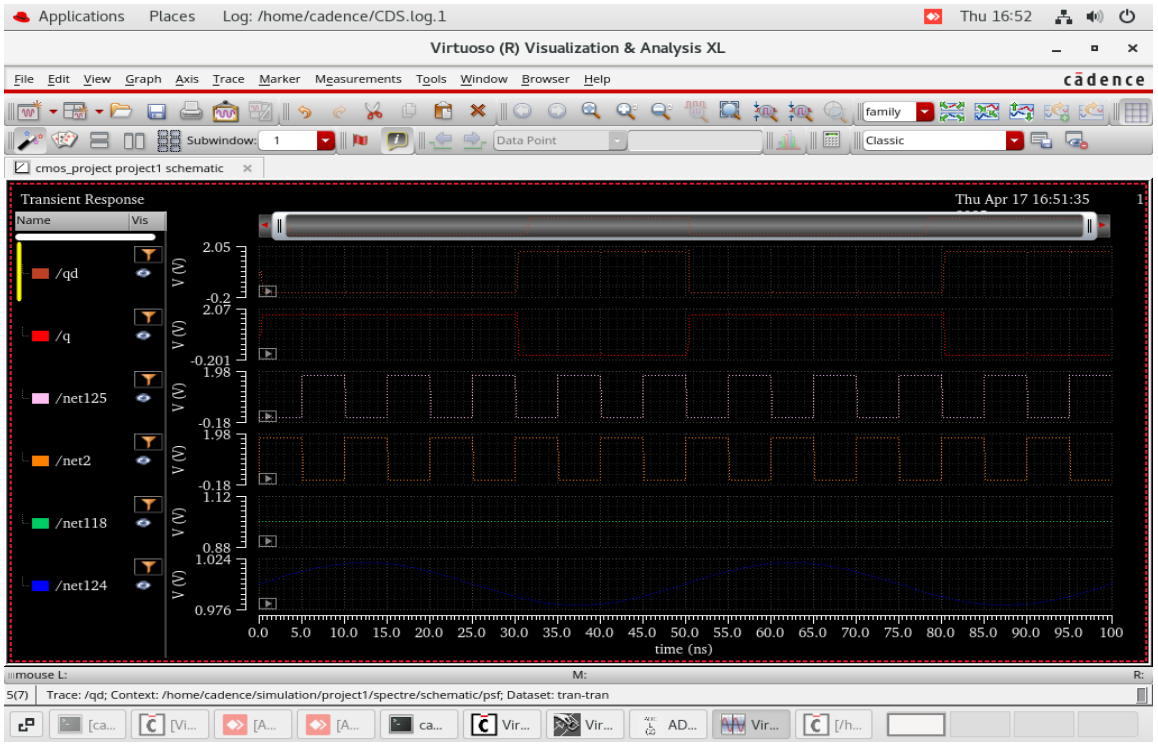
- **Compact Area:**
  Implemented using a 1.5 μm CMOS process, the entire comparator occupies just 140 × 100 μm², making it ideal for integration into dense mixed-signal systems.

- **No Offset Cancellation Required:**
  Offset is minimized by symmetry and design optimization rather than using complex calibration circuits, simplifying implementation.

5.0 Simulation



6.0 Result



7.0 Conclusion

This report presents the design and performance of a high-speed CMOS comparator capable of achieving 8-bit resolution with a 20 Msample/s conversion rate. The design emphasizes a balance between speed, resolution, and power consumption, making it suitable for applications in high-speed analog-to-digital converters. By employing a fully differential folded-cascode input stage followed by a dynamic latch and SR latch, the comparator achieves low input-referred offset and rapid decision-making capabilities. Simulation results confirm that the comparator maintains an input-referred offset voltage of less than 2 mV and a power dissipation of only 1.2 mW, demonstrating both efficiency and accuracy. Overall, the proposed design contributes a viable solution for modern mixed-signal systems requiring compact, low-power, and high-speed comparator architectures.

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