CENG311

PROGRAMMING ASSIGNMENT 4 REPORT

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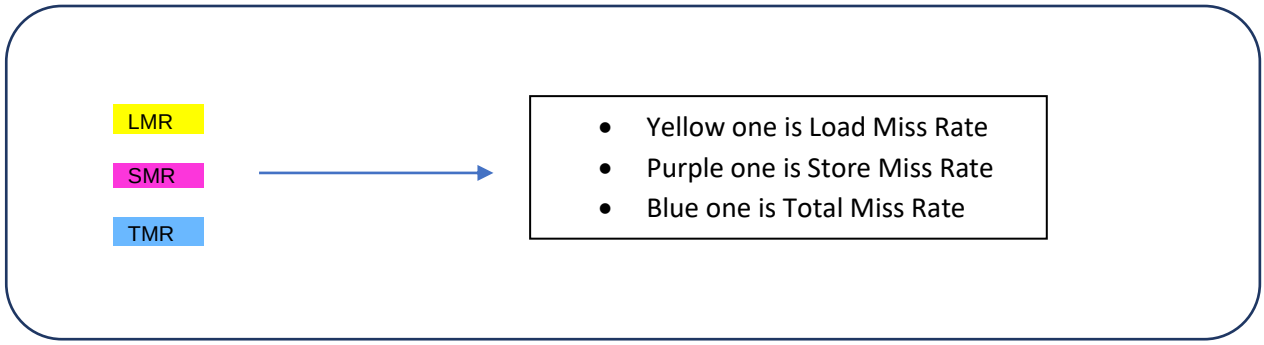
NOT:



1- N = 10

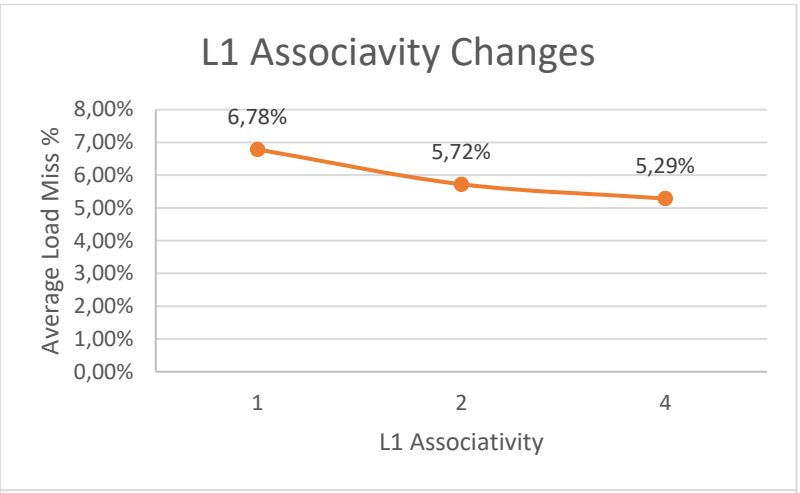
L1 Size [KB]	Block Size [B]	L1 Associativity	First Try			Second Try			Third Try			Fourth Try			Fifth Try			Average		
8	32	1	6,76%	9,32%	7,33%	6,33%	9,32%	6,99%	6,93%	9,89%	7,58%	7,37%	10,99%	8,18%	6,53%	8,86%	7,04%	6,78%	9,68%	7,42%
8	32	2	5,82%	8,52%	6,42%	5,56%	8,73%	6,26%	5,98%	8,35%	6,51%	5,82%	8,25%	6,36%	5,43%	8,52%	6,12%	5,72%	8,47%	6,33%
8	32	4	5,28%	8,31%	5,95%	5,31%	8,47%	6,01%	5,27%	8,33%	5,95%	5,30%	8,32%	5,97%	5,27%	8,33%	5,95%	5,29%	8,35%	5,97%
16	16	1	7,89%	13,78%	9,20%	8,88%	14,86%	10,20%	9,59%	17,27%	11,30%	8,02%	14,12%	9,37%	8,05%	14,29%	9,43%	8,49%	14,86%	9,90%
16	32	1	5,54%	8,24%	6,14%	5,19%	8,15%	5,85%	6,06%	8,71%	6,65%	5,21%	8,18%	5,87%	5,11%	8,07%	5,76%	5,42%	8,27%	6,05%
16	64	1	3,78%	4,63%	3,97%	4,22%	5,06%	4,41%	4,44%	4,86%	4,54%	4,57%	6,37%	4,97%	5,74%	5,67%	5,72%	4,55%	5,32%	4,72%
16	16	2	7,64%	14,20%	9,10%	7,66%	14,08%	9,08%	7,59%	13,79%	8,97%	7,66%	13,98%	9,07%	7,65%	13,85%	9,03%	7,64%	13,98%	9,05%
16	32	2	4,81%	7,92%	5,50%	4,81%	7,93%	5,50%	4,78%	7,91%	5,48%	4,81%	8,02%	5,52%	4,75%	7,76%	5,42%	4,79%	7,91%	5,48%
16	64	2	3,24%	4,31%	3,48%	3,32%	4,52%	3,59%	3,37%	4,37%	3,59%	3,33%	4,44%	3,57%	3,41%	4,57%	3,67%	3,33%	4,44%	3,58%
16	16	4	7,48%	13,62%	8,84%	7,49%	13,64%	8,85%	7,45%	13,59%	8,81%	7,49%	13,72%	8,87%	7,49%	13,64%	8,85%	7,48%	13,64%	8,84%
16	32	4	4,67%	7,71%	5,35%	4,68%	7,73%	5,36%	4,66%	7,77%	5,35%	4,69%	7,69%	5,36%	4,69%	7,83%	5,38%	4,68%	7,75%	5,36%
16	64	4	3,29%	4,30%	3,51%	3,29%	4,40%	3,53%	3,29%	4,37%	3,53%	3,26%	4,30%	3,49%	3,27%	4,31%	3,50%	3,28%	4,34%	3,51%
32	32	1	7,14%	13,04%	8,45%	4,59%	7,60%	5,26%	5,25%	8,07%	5,87%	5,99%	8,96%	6,65%	4,94%	7,64%	5,54%	5,58%	9,06%	6,35%
32	32	2	4,41%	7,54%	5,10%	4,43%	7,58%	5,13%	4,42%	7,56%	5,12%	4,49%	7,66%	5,19%	4,40%	7,54%	5,09%	4,43%	7,58%	5,13%
32	32	4	4,37%	7,51%	5,06%	4,35%	7,54%	5,06%	4,33%	7,54%	5,04%	4,34%	7,53%	5,05%	4,34%	7,51%	5,04%	4,35%	7,53%	5,05%

2- N=1000

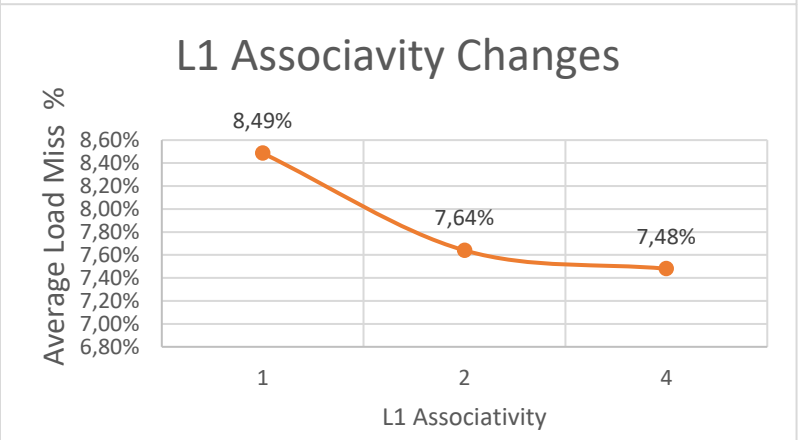
L1 Size [KB]	Block Size [B]	L1 Associativity	LMR	SMR	TMS
8	32	1	7,90%	1,39%	7,33%
8	32	2	7,27%	0,37%	6,67%
8	32	4	7,25%	0,33%	6,65%
16	16	1	8,77%	0,51%	8,05%
16	32	1	7,50%	0,81%	6,92%
16	64	1	6,76%	1,55%	6,31%
16	16	2	9,54%	0,18%	8,72%
16	32	2	7,20%	0,19%	6,59%
16	64	2	6,04%	0,29%	5,54%
16	16	4	9,56%	0,17%	8,74%
16	32	4	7,20%	0,18%	6,59%
16	64	4	6,03%	0,27%	5,52%
32	32	1	5,55%	0,32%	5,09%
32	32	2	5,96%	0,13%	5,45%
32	32	4	6,77%	0,11%	6,19%

CHANGE GRAPHS WHEN N = 10:

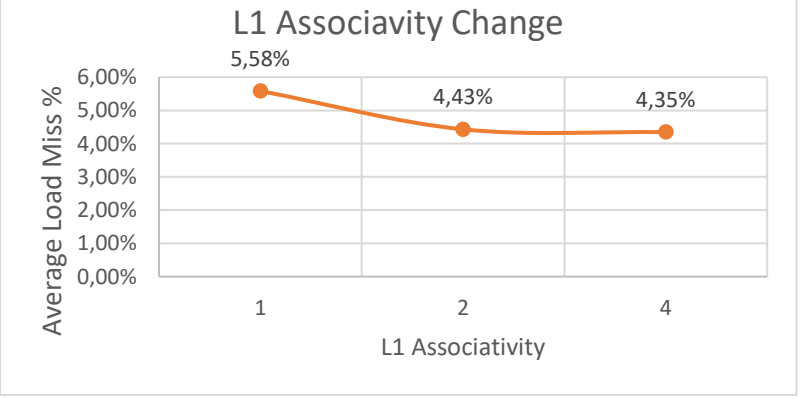
3- Effect of changing L1 Associativity on Load Miss (L1 Associativity Values: 1, 2, 4)



L1 Size [KB] =8
Block Size [K] = 32

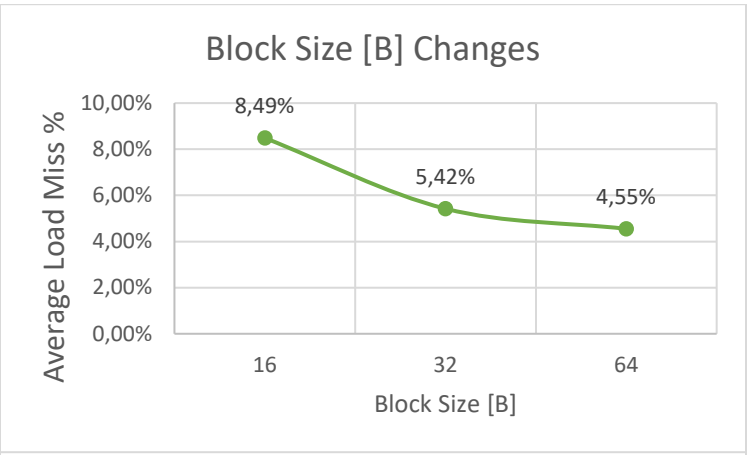


L1 Size [KB] =16
Block Size [K] = 16

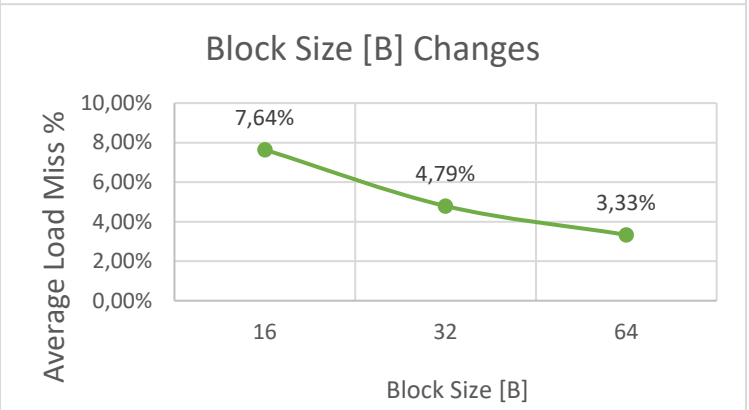


L1 Size [KB] =32
Block Size [K] = 32

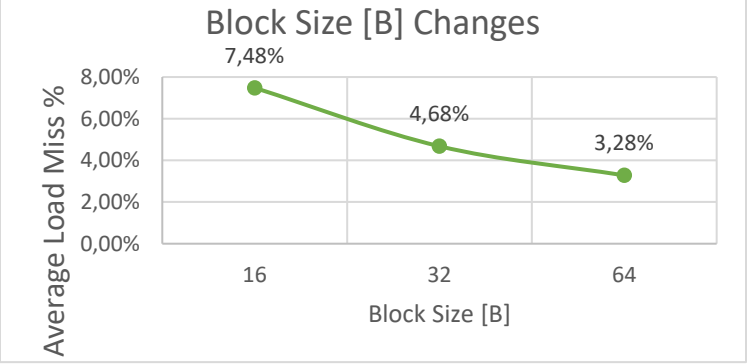
4- Effect of changing Block Size on Load Miss (Block Size Values: 16, 32, 64)



L1 Size [KB] =16
L1 Associativity = 1

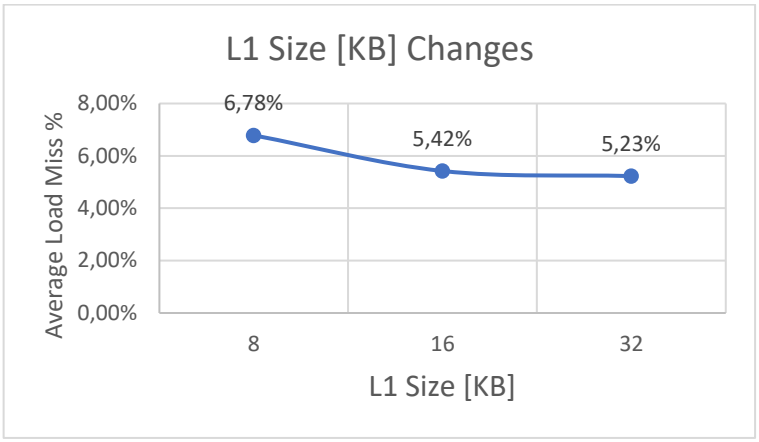


L1 Size [KB] =16
L1 Associativity = 2

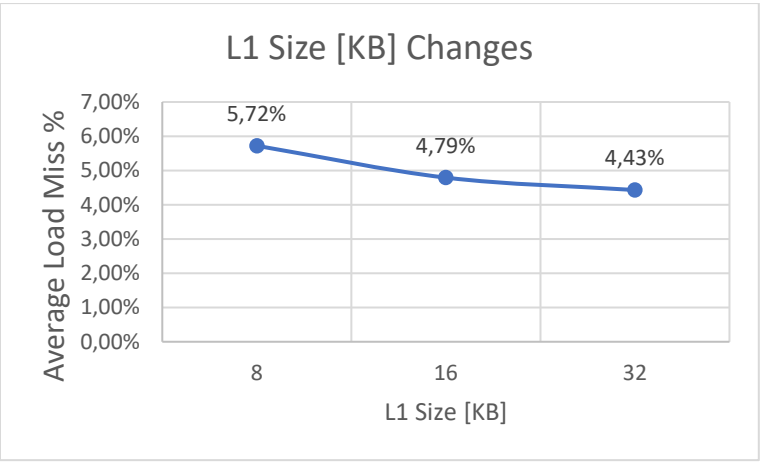


L1 Size [KB] =16
L1 Associativity = 4

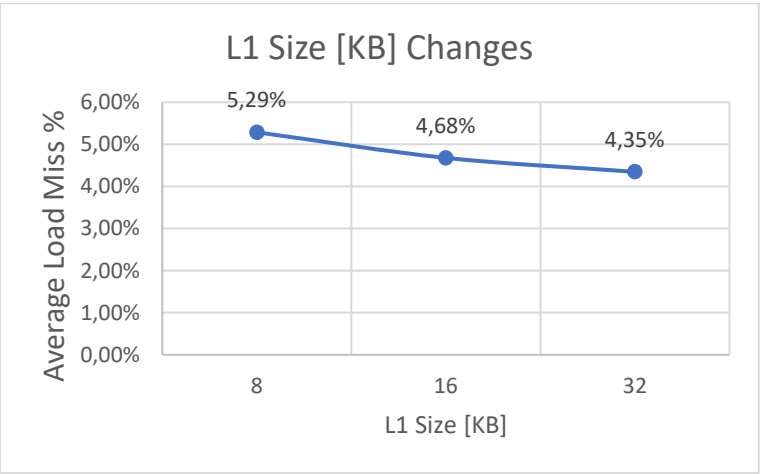
5- Effect of changing L1 Size on Load Miss (L1 Size Values: 8, 16, 32)



Block Size [K] =32
L1 Associativity = 1



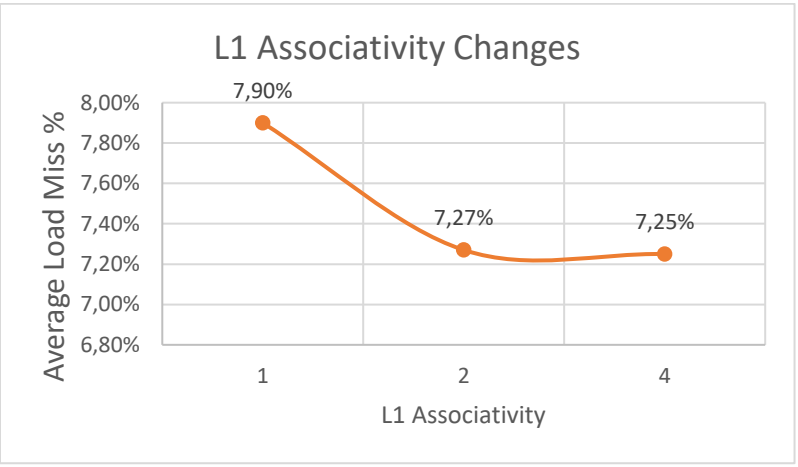
L1 Size [KB] =32
L1 Associativity = 2



L1 Size [KB] =32
L1 Associativity = 4

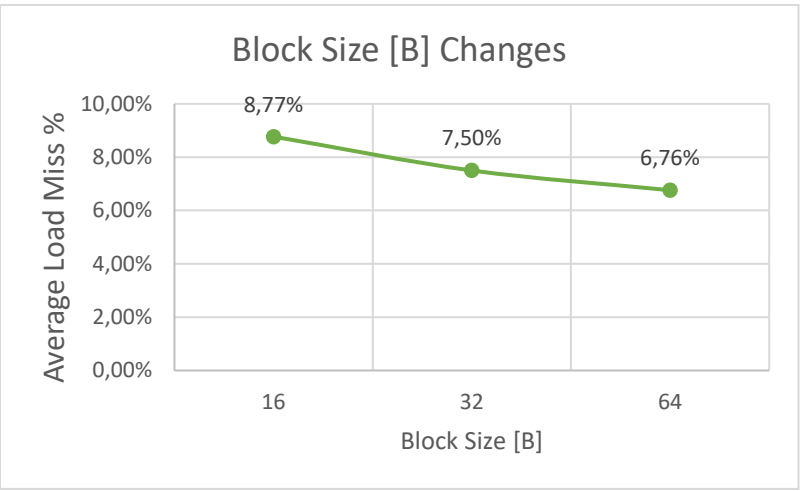
CHANGE GRAPHS WHEN N = 1000:

6- Effect of changing L1 Associativity on Load Miss (L1 Associativity Values: 1, 2, 4)



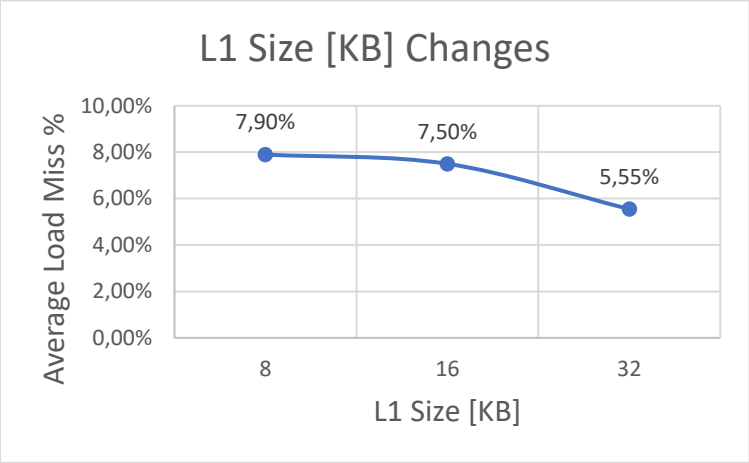
L1 Size [KB] =8
Block Size [K] = 32

7- Effect of changing Block Size on Load Miss (Block Size Values: 16, 32, 64)



L1 Size [KB] =16
L1 Associativity = 1

8- Effect of changing L1 Size on Load Miss (L1 Size Values: 8, 16, 32)



L1 Associativity = 1
Block Size [K] = 32

COMMENTS ABOUT THE EXPERIMENTS:

1- Change in L1 Associativity: The number of ways that a cache block may be mapped to cache sets is the cache's associativity. Higher associativity indicates that there are more possible ways to map a block to a cache set, which might result in fewer cache conflicts (mentioned on lectures) and a lower miss rate. Contrarily, a cache with lower associativity has fewer possible ways to map a block to a cache set, which might result in more cache conflicts and a greater miss rate.

2- Change in Block Size: When there is a smaller block size, the miss rate is higher since it uses spatial locality. This is because the impact of spatial locality in decreasing cache misses is diminished by smaller block sizes, which might result in a greater miss rate in cache performance since they are less likely to contain the data that a program requires.

3- Change in L1 Size (Cache Size): A decrease in L1 size reduces the load miss rate since the L1 cache is the closest cache to the CPU, so if it is small, it has less space convenient to store data that is wanted to be recently accessed, which leads to a higher miss rate. Temporal locality refers to the reuse of specific data and/or resources within a relatively short period. Since it uses temporal locality, increasing the size of the L1 cache causes a decrease in cache misses.

4- Comparison of when N=1000 and N=10: Because the L1 cache is relatively bigger in comparison to matrix size, the impact of the L1 associativity on the load miss rate may be less obvious as the matrix size increases. The block size and L1 cache size may in this scenario have a higher influence on the load miss rate. However, in general their effect on load miss is relatively smoother when we have a large matrix.

5- A different situation:

L1 Size [KB]	Block Size [B]	L1 Associativity	LMR	SMR	TMS
32	32	1	5,55%	0,32%	5,09%
32	32	2	5,96%	0,13%	5,45%
32	32	4	6,77%	0,11%	6,19%

In that case load miss increases dependent on L1 associativity rise since L1 cache size is large and sufficient to store data. At some point L1 associativity does not affect load miss too much due to the L1 size and block size.