Digital Electronics – 18EC3DCDEC.

Module-1

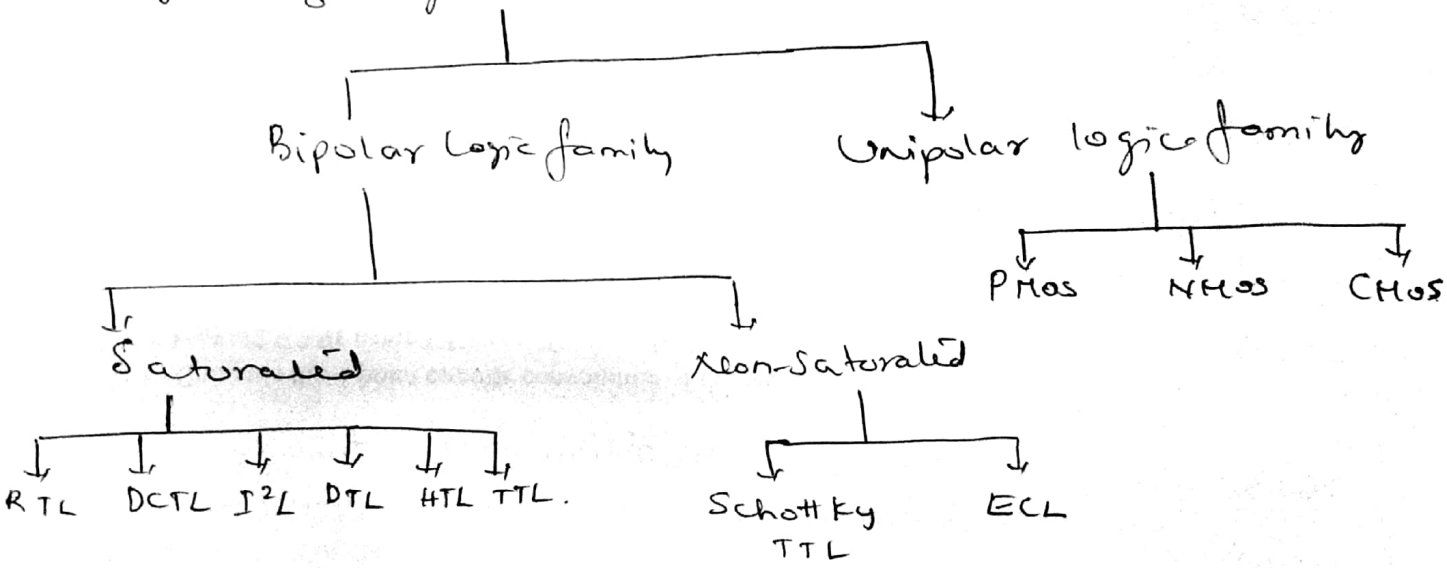
Introduction to logic families:

* Logic Family: Logic families indicate the type of logic circuit used in the IC.
* Basically there are two types of Semiconductor devices: Bipolar and Unipolar.

  Bipolar devices: Resistors, Diodes & Transistors.

  Unipolar devices: MOSFET.

* Types of logic Families

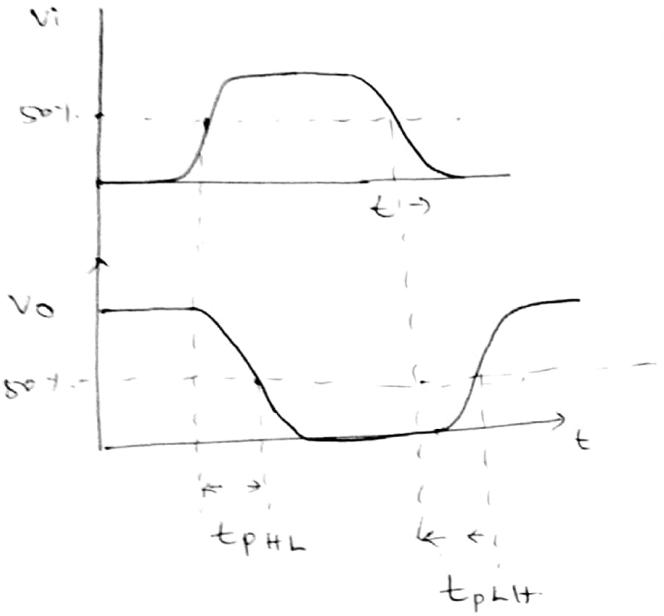


* Characteristics of Digital ICs
  1. Speed of operation.
  2. power dissipation
  3. Figure of Merit.
  4. Current and voltage parameters.
  5. Noise Immunity.
  6. Fan-out
  7. Fan-in
  8. power-supply requirements
  9. operating temperature.

1. Speed of operation (propagation Delays)

The speed of digital circuit is specified in terms of propagation delay time.

propagation delay of gate is the average transition delay time for the signal to propagate from input to output. It is measured in nanoseconds.



t_{pHL} → o/p goes from High to Low

t_{pLH} → o/p goes from Low to High.

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2}$$

2. Power Dissipation: This is the amount of power dissipated in the IC.

Every Ic needs a certain amount of electrical power to operate. V_{cc} (TTL) and V_{DDC} (MOS).

Power dissipation = $V_{cc} \times I_{cc}$ (avg)

$$I_{cc}(avg) = \frac{(I_{ccH} + I_{ccL})}{2}$$

It is measured in miliwatts.

3. Figure of merit: It is defined as the product of speed and power.

Fom = propagation delay × power dissipation

= (ns) × (mw)

= PJ (picojoules).

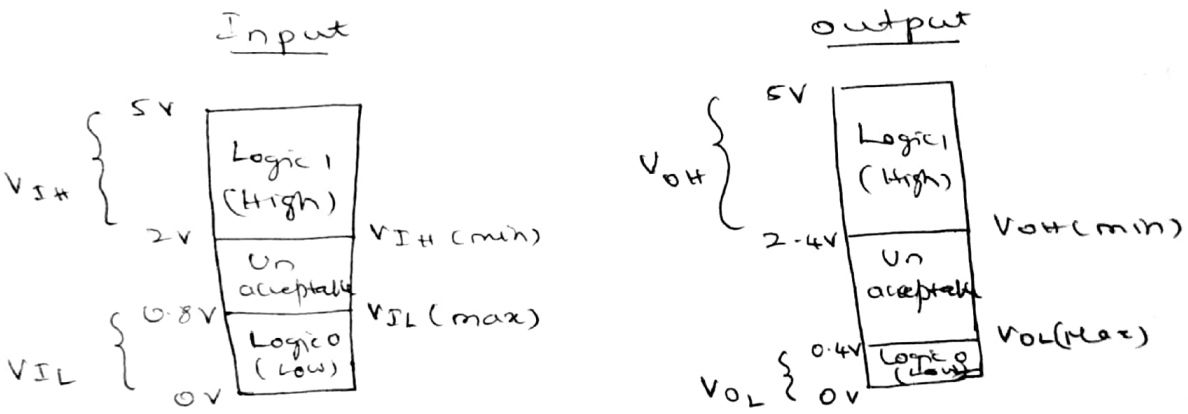
4. current and voltage parameters.

$V_{IH(min)}$: High level i/p voltage: This is the minimum i/p voltage which is recognised by the gate as logic 1.

$V_{IL(max)}$: Low-level i/p voltage: This is the maximum i/p voltage which is recognised by the gate as logic 0.

V_{OH} : High level o/p voltage: This is the minimum voltage available at the output corresponding to logic 1.

V_{OL} : low level o/p voltage: This is maximum voltage available at the output corresponding to logic 0.



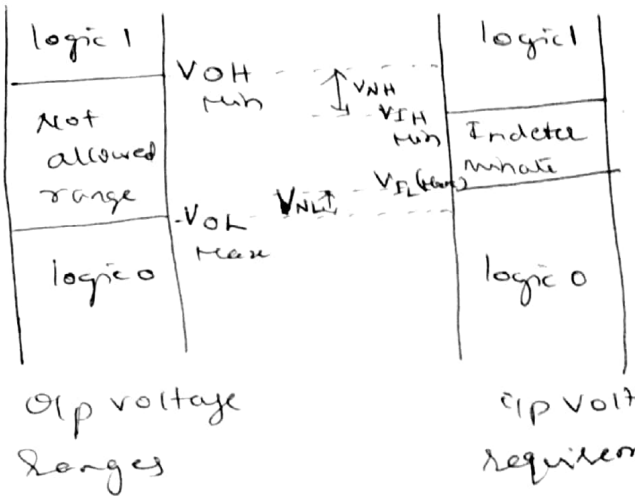
I_{IH} : High level i/p current : This is the minimum current which must be supplied by a driving source corresponding to logic '1' level voltage.

I_{IL} : Low-level i/p current : This is the minimum current which must be supplied by a driving source corresponding to logic '0' level voltage.

I_{OH} : High level o/p current: This is maximum current which the gate can sink in logic '1' level.

I_{OL} : low level o/p current: This is the maximum current which the gate can sink in logic '0' level.

5. Noise Immunity: The i/p and o/p voltage levels gets affected by stray electric and magnetic fields Stray electric and magnetic fields may induce unwanted voltages known as noise, on the connecting wires between logic circuits. This may cause the voltage at the i/p to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the noise immunity, a quantative measure of which is called noise margin.



V_{NH} = High state Noise Margin
$= V_{OH(min)} - V_{IH(min)}$

V_{NL} = low state Noise margin
$= V_{IL(max)} - V_{OL(max)}$

6. Fan-out: It is defined as maximum number of standard logic input that an output can drive reliably. Fan out is also called as Loading factor.

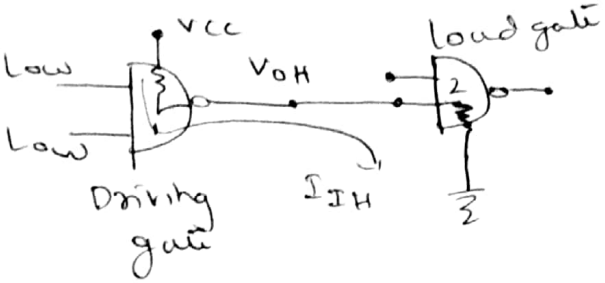
7. Fan-In: It represents the number of inputs the logic gate can handle.

8. power supply Requirements: The supply voltages and the amount of power required by an IC are important characteristics required to choose the power supply.

9. operating Temperature: The temp range for consumer → 0 to +70°C & industrial applications and for military −55°C to +25°C.

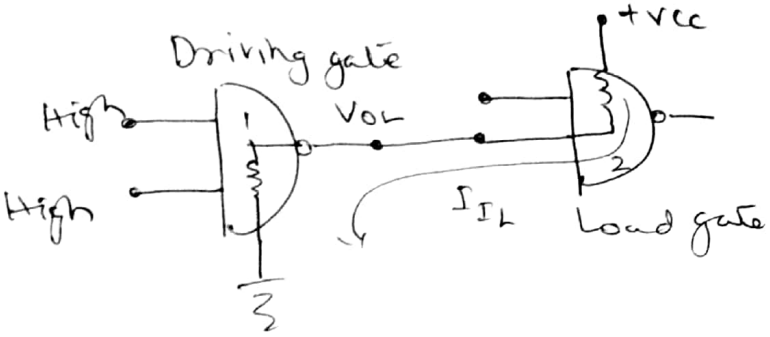
Current Source and current Sink.

Logic families can be described according to how current flows between the output of one logic circuit and the input of another.



current sink

Driving gate supplies (sources) current to load gate in High state

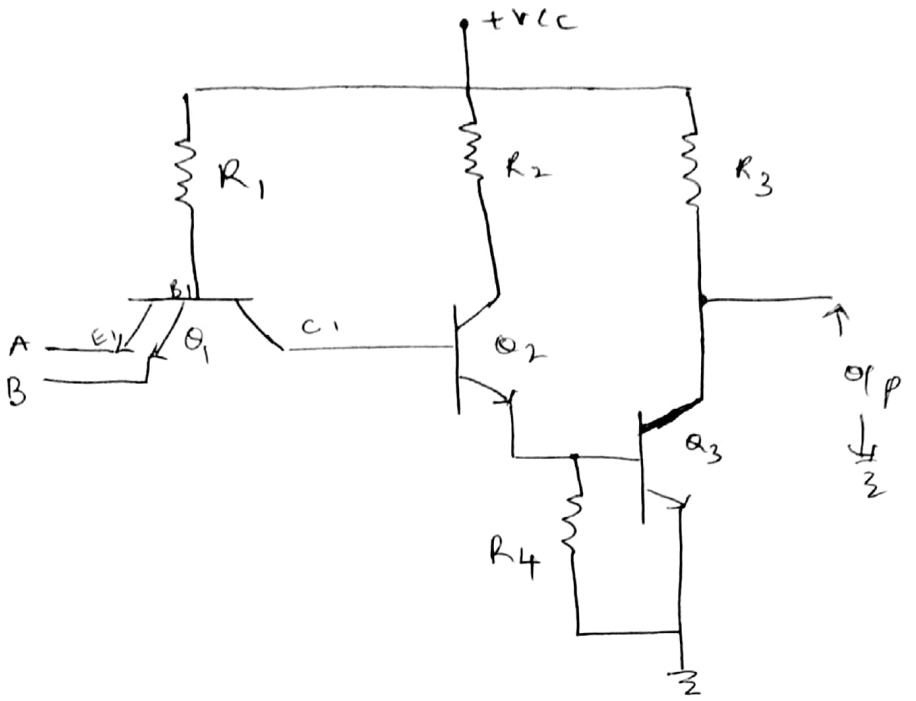


Driving gate receives (sinks) current from load gate in Low state.

TTL - Transistor - Transistor Logic Families

* First Introduced in 1964 (TI)
* power dissipation is 10 mW
* Fan in of 6 and fan-out of 10
* propagation delay of 5-15 ns.
* It can perform many digital function and have achieved the most popularity.
* TTL ICs are given numerical designation as 5400 and 7400 series.
* The basic circuit of TTL with totem pole output stage is NAND gate
* Less noise immunity.

* A Basic two-i/p TTL NAND gate:



* The basic two i/p TTL nand gate is as shown above, consists of multiemitter npn transistor(Q_1) as the i/p stage.

* The base collector junction of Q_1 and base-emitter jn of Q_2 forms diode AND gate.

* The final stage consists of a transistor inverter Q_3.

* It is assumed that,

Transistor

$V_{BE(on)} = V_{BE(sat)} = 0.7\,V$,

$V_{BC(on)} = V_{BC(sat)} = 0.5\,V = V_\gamma$

$V_{CE(sat)} = 0.2\,V$.

Diode

V_γ = cut in voltage = 0.6V

Voltage across conducting diode = 0.7V.

* Condition 1: At least one input is Low. The emitter base junction of Q_1 corresponding to the i/p in the LOW state is forward biased making the voltage at B_1, $V_{B_1} = 0.2 + 0.7 = 0.9\,V$. For base collector junction of Q_1 to be Forward biased, and for Q_2 & Q_3 to be conducting, V_{B_1} is required to be at least $0.6 + 0.5 + 0.5 = 1.6\,V$. Hence Q_2 & Q_3 are off.

Since Q_3 is OFF, $\therefore Y = V(1) = V_{cc}$.

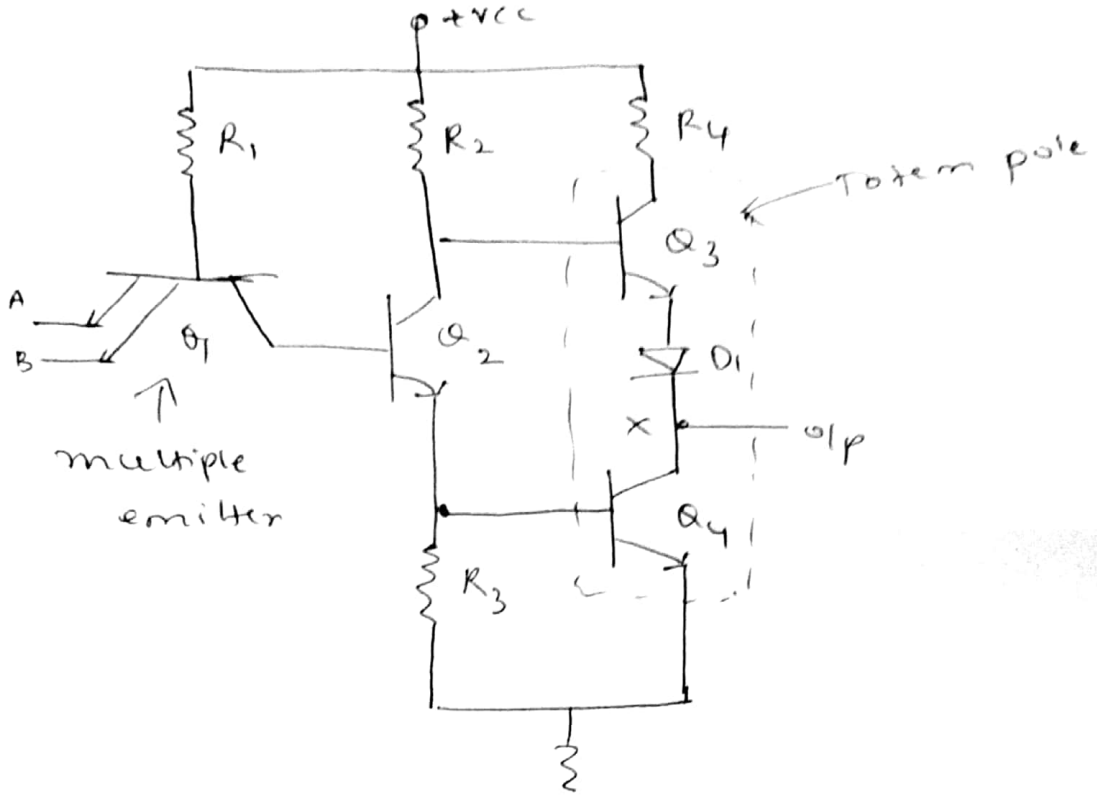
Condition ii: All i/p are HIGH. The emitter-base junction of Q_1 are reverse biased. If we assume that Q_2 & Q_3 are ON, then $V_{B_2} = V_{C_1} = 0.8 + 0.8 = 1.6V$. Since B_1 is connected to +5V (V_{cc}) through R_1, the collector-base junction of Q_1 is forward-biased. The transistor Q_1 is operating in active inverse mode, making I_{C_1} flow in the reverse direction. This current flows into the base of Q_2 driving Q_2 and Q_3 into saturation.

$\therefore Y = V(0) = 0.2V$.

* The speed of operation of a logic gate is also dependent upon the parasitic o/p capacitance & is associated with the wiring capacitance, the i/p diode capacitance of the load gates, and the collector-emitter capacitance of transistor Q_3. The rate at which this parasitic capacitor is charged and discharged affects the switching time of the driving gate.

* It is desirable to have R_3 be as small as possible while the o/p is switching from its low to high value in order to have a small RC time constant, and have R_3 be as large as possible when the gate is in its steady state with a low output in order to have low power dissipation. This is achieved by active pull up circuit known as totem-pole output.

* TTL gate with Totem-pole output



* A two i/p TTL nand-gate with a totem-pole output is as shown above.

* when both the i/ps are high, the base emitter junction of Q_1 is reverse biased and Base-collector junction of Q_1 is forward biased. Hence Q_2 and Q_4 are forced into saturation and transistor Q_1 is in inverted active mode. Since Q_2 is in saturation, the voltage at its collector is $V_{CE_2(sat)} + V_{BE_4(sat)} = 0.2 + 0.7 = 0.9V$. This is also the voltage at the base of transistor Q_3. Since transistor Q_4 is also in saturation, the voltage at the cathode of diode D_1 is $V_{CE_4(sat)} = 0.2V$. With a voltage difference of $0.9 - 0.2 = 0.7$ V between the base of tr Q_3 & o/p, there is insufficient force to support the base-emitter drop of Q_3

and the diode drop of D_1 to allow current to flow through these two elements. Thus, tr Q_3 and diode D_1 are in cut off. with tr Q_4 in cut off, no current flow through the low-valued resistor R_3. As a result, the objective of having no power dissipation is achieved when the o/p of the gate is low. However, tr Q_4 is still sinking current due to loads.

* when either or both inputs are low, base emitter junction is forward biased & Base collector junction is reverse biased. ∴ transistor Q_2 is OFF. with Q_2 OFF, there is no base current for Q_4 and it turns OFF. Since there is no Q_2 collector current, the voltage at Q_3's base will be large enough to forward-bias Q_3 and D_1, so that Q_3 will conduct. ∴ o/p at X is high (3.4 to 3.8 V).