FET Biasing.

Graphical analysis is chosen to get accuracy as DC Analysis by mathematical approach turns out to be complicated because of non linear relationship between I_D & V_{GS}.

General relationships applied to dc analysis of FET amplifier are.

$I_G \simeq 0A$.

& $I_D = I_S$

For JFET's and depletion type MOSFETs Shockley's equation is applied.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2.$$

For Enhancement type MOSFET,

$I_D = k(V_{GS} - V_T)^2$ is applicable.

Fixed Bias Configuration

* Both approaches are included for this Biasing arrangements for n-channel JFET.

1. Coupling capacitors are open circuited for DC Analysis.

∴ For DC analysis

$I_G \cong 0A$.

$\therefore V_{R_G} = I_G R_G = 0V$.

The 0V drop across R_G permits replacing R_G by short circuit.

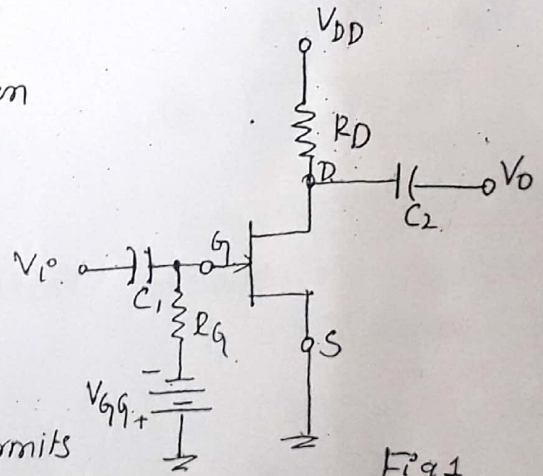


Fig 1.

A circuit is redrawn considering above 2 points as shown in Fig 2.

Apply KVL to the loop indicated in Fig2.

$$-V_{GG} - V_{GS} = 0.$$

$$V_{GS} = -V_{GG} \quad -(1)$$

Since V_{GS} is fixed by battery V_{GG} it is called "Fixed Bias Configuration"

& I_D is given by shockley's eqn as.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad -(2)$$

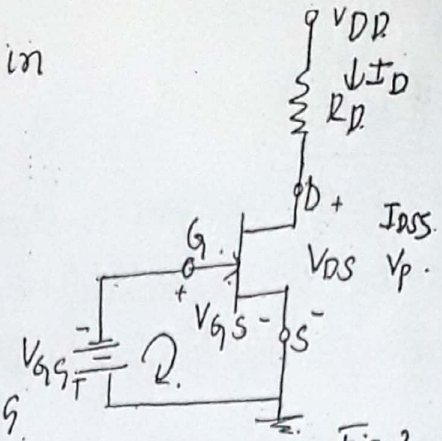


Fig 2.

The drain to source voltage of o/p can be determined by applying KVL as follows.

$$+V_{DS} + I_D R_D - V_{DD} = 0.$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \quad -(3)$$

$V_S = 0V$

$$\therefore V_{DS} = V_D - V_S$$

$$\therefore \boxed{V_D = V_{DS}} \quad -(4)$$

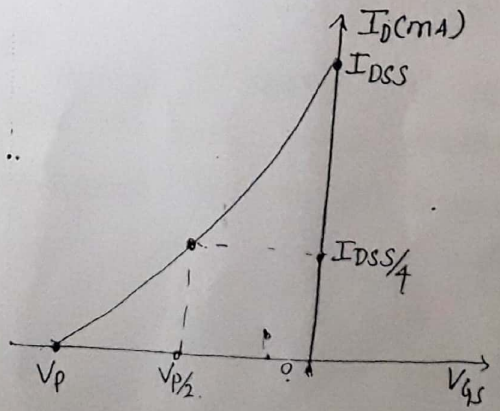
$$V_{GS} = V_G - V_S$$

$$\therefore \boxed{V_G = V_{GS}} \quad -(5)$$

Graphical Approach

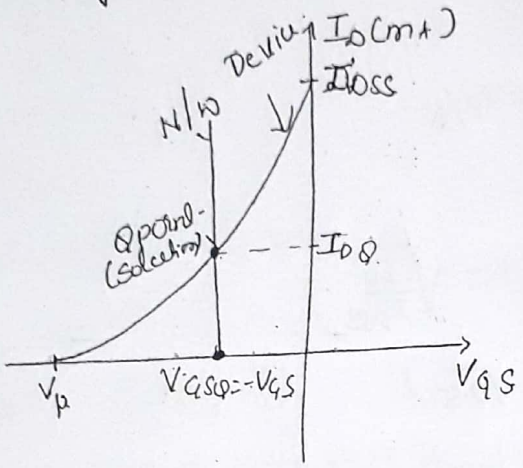
From shockley's Equation Transfer curve can be plot for 4 points i.e.

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$\frac{I_{DSS}}{2}$
$0.5V_P$	$\frac{I_{DSS}}{4}$
V_P	0mA



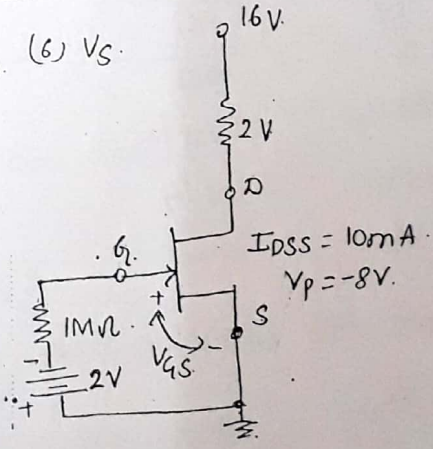
To find Q-point on the fixed Bias configuration.

Draw a vertical line for $V_{GS} = -V_{GG}$ (fixed) wherever it intersects the curve, the I_{DQ} point is taken which is found by drawing a horizontal line from Q-point to vertical I_D axis



* Determine the following for the n/w.

(1) V_{GSQ} (2) I_{DQ} (3) V_{DS} (4) V_D (5) V_G (6) V_S



1. $V_{GSQ} = -V_{GG} = -2V$

2. $I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10mA\left(1 - \frac{(-2V)}{-8V}\right)^2$

$= 5.625\,mA$

3. $V_{DS} = V_{DD} - I_D R_D$

$= 4.75V$

4. $V_D = V_{DS} = 4.75V$

5. $V_G = V_{GS} = -2V$

6. $V_S = 0V$

Method to draw Transfer Curve

1. $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= I_{DSS}\left(1 - \frac{V_P/2}{V_P}\right)^2 = I_{DSS}\cdot(1-1/2)^2$ [Putting $V_{GS} = \frac{V_P}{2}$]

$I_D = I_{DSS}(0.25)$

$I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS}=V_P/2}$.

2. Choose $I_D = I_{DSS}/2$.

then $V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$

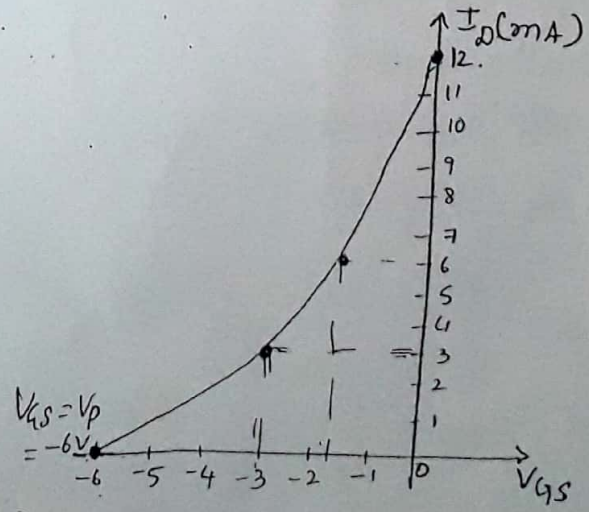
$= V_P.(1-\sqrt{0.5})$

$V_{GS} = 0.3V_P\Big|_{I_D = I_{DSS}/2}$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

1. Sketch the Transfer curve defined by $I_{DSS} = 12mA$ & $V_P = -6V$.

V_{GS}	I_D
0	$I_{DSS} = 12mA$
$V_P = -6V$	0mA
$0.3V_P = -1.8V$	6mA
$0.5V_P = -3V$	3mA



This is for n-channel JFET.

Self-Bias Configuration

1. For DC Analysis, capacitors are open ckted & $I_G = 0A$ so R_G is replaced by short circuit.
The resulting n/w is shown in Fig ②.

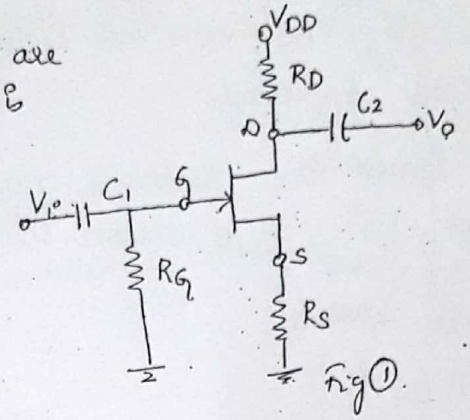


Fig ①.

2. $I_S = I_D$ &
$V_{RS} = I_D R_S$.

3. Applying KVL to i/p loop.
$-V_{GS} - V_{RS} = 0$.
$V_{GS} = -I_D R_S$ ---①.

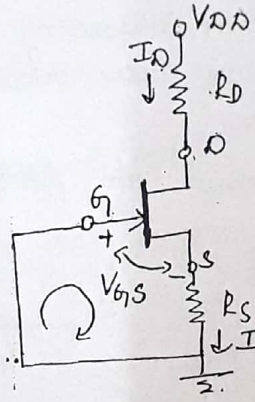


Fig ②

So from Eqn ① it is clear that V_{GS} is a function of o/p current I_D & is not fixed as for fixed bias configuration.

4. Now I_D is given by Schokley Eqn as
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$
$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By expanding & rearranging terms, we obtain an Eqn of following form $I_D^2 + k_1 I_D + k_2 = 0$ - ②

This Quadratic Eqn can be solved to get appropriate solution for I_D.

5. Now apply KVL to o/p circuit, we get
$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$
$$V_{DS} = V_{DD} - I_S R_S - I_D R_D$$
$$V_{DS} = V_{DD} - I_D(R_S + R_D) \quad [\because I_S = I_D]$$
---③.

& $V_S = I_D R_S$ - (4)

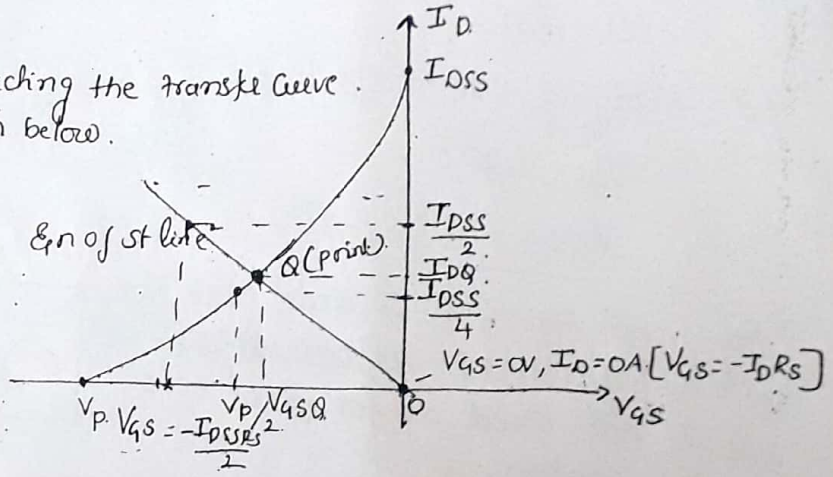
$V_G = 0V$ - (5)

$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$ - (6).

Graphical Approach.

Step 1: Draw the transfer characteristics for below table & is shown in fig (3).

V_{GS}	I_D
0	I_{DSS}
$V_P/2$	$I_{DSS}/4$
V_P	0



Step 2: Draw a line intersecting the transfer curve. & analysis is as shown below.

$V_{GS} = -I_D R_S$

Can be transformed into Eqn of st line as. $I_D = \left(\frac{-1}{R_S}\right) V_{GS}$.

$y = m \quad x + c$

[Note: $x = V_{GS}$, $y = I_D$, $c = 0$. Slope $= -1/R_S$.

When $c = 0$, Eqn starts through the origin.]

If $V_{GS} = 0V$ then $I_D = 0A$ (origin)

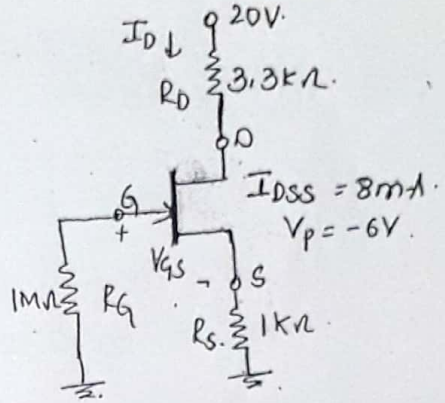
If $I_D = \frac{I_{DSS}}{2}$ then $V_{GS} = -\frac{I_{DSS} R_S}{2}$. Fixed.

Thus 2 points are obtained & a st line is drawn through the origin.].

→ Wherever the straight line and the Transfer curve intersects give the Q-point [V_{GSQ}, I_{DQ}].

1. Determine the following for the network.

a. V_{GSQ} b. I_{DQ} c. V_{DS} d. V_S e. V_G f. V_D.



1. $V_{GS} = -I_D R_S$.

To find (V_{GSQ} I_{DQ}) from Graph.

Steps:

1. Choose $I_D = \frac{I_{DSS}}{2} = \frac{8mA}{2} = 4mA$.

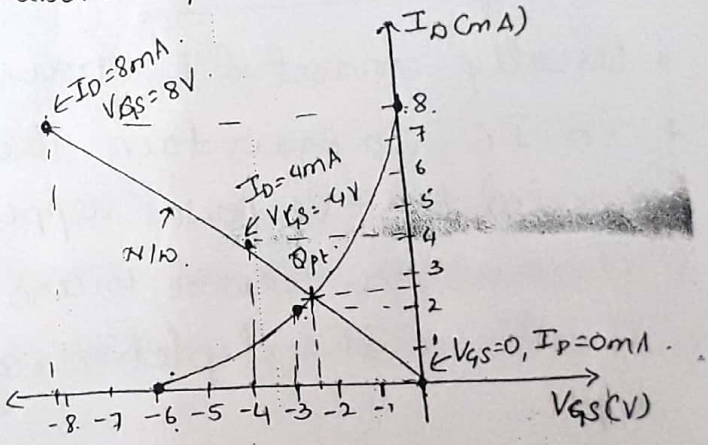
$V_{GS} = -4V$.

2. Choose $I_D = 0A \Rightarrow V_{GS} = 0V$.

3. Choosing $I_D = I_{DSS} = 8mA$.

$V_{GS} = 8V$.

St line is drawn with above 3 points.



Step2: To draw Transfer curve

V_{GS}	I_D
0	8mA
−3	2mA
−6	0

Points to be drawn on Graph.

From Graph Q-pt = V_{GSQ} = −2.6V & I_{DQ} = −2.6mA

1. $V_{GSQ} = -2.6V$

2. $I_{DQ} = -2.6mA$

3. $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$= 8.82V$

4. $V_S = I_D R_S$

$= 2.6V$.

5 $V_G = 0V$ ..

6. $V_D = V_{DS} + V_S = 8.82 + 2.6 = 11.42V$

or $= V_{DD} - I_D R_D = 11.42V$.

2. Find the Q.pt for same above n/w for (i) $R_S = 100\Omega$ & $R_S = 10k\Omega$

Role of substrate.

- usually connected to ground & ignored.
- In IC, to maintain the cutoff conditions usually connected to -Ve power supply (NMOS) & +ve in PMOS.
- It results in reverse bias & effects the device operation.
- It widens the depletion region, reduces the channel depth.
- effect of V_{SB} will result in change of V_t.

$$V_t = V_{to} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

$V_{to} = V_t$ at $V_{SB} = 0$, $\phi_f \rightarrow$ a physical parameter with $2\phi_f$ typically $= 0.6V$, γ - fabrication process parameter

$$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}$$

q - electron charg $= 1.6 \times 10^{-19} C$.

N_A - doping concentration of P-substrate

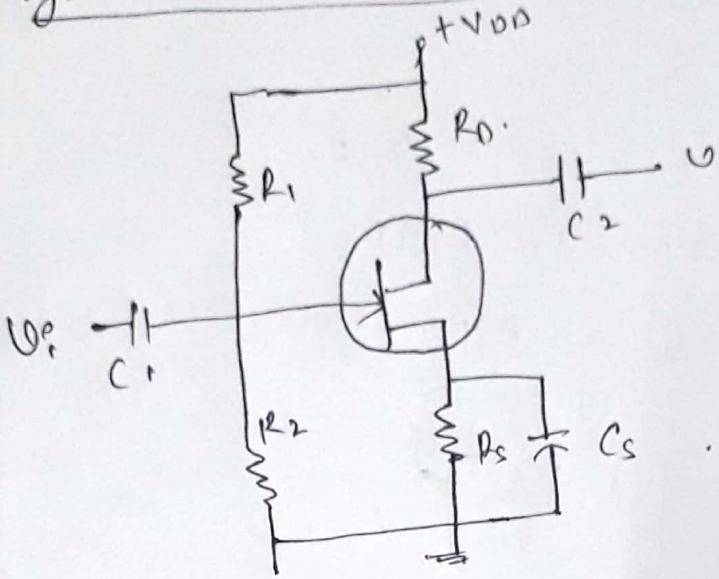
ε_s - permitivity of silicon $= 11.7\varepsilon_0 = 1.04 \times 10^{-12}$ F/cm

$\gamma = 0.4\sqrt{V}$

change in $V_{SB} \rightarrow$ change $V_t \rightarrow$ change in I_D .: Body Vtg controls I_D.
This phenomenon is called as body effect.
$\gamma \rightarrow$ body effect parameter.

Q no.	Description	Marks

Voltage Divider Bias Ckt



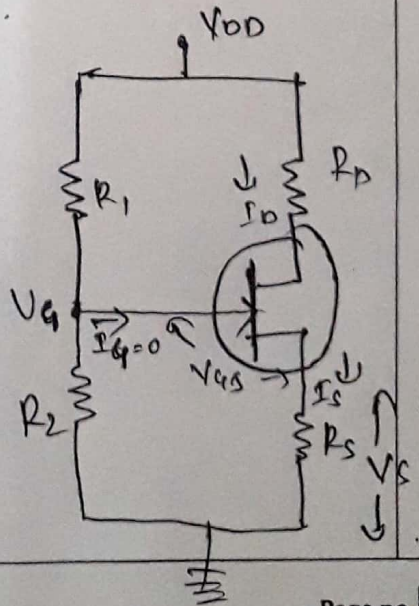
The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source function reverse biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 & R_2 as expressed by the following eqn using the voltage divider formula.

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

DC Analysis.



Applying KVL to the input ckt we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S$$

$$= V_G - I_D R_S$$

Page no

Q no.	Description	Marks

Applying KVL to the o/p ckt we get

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S)$$

The Q point of a Amplifier using the voltage divider is given by.

$$I_{DQ} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

I_{DSS} → (Referred as the drain current for zero bias) is the maximum current that flows through a FET transistor, which is when the gate voltage, V_G, supplied to the FET is 0V.