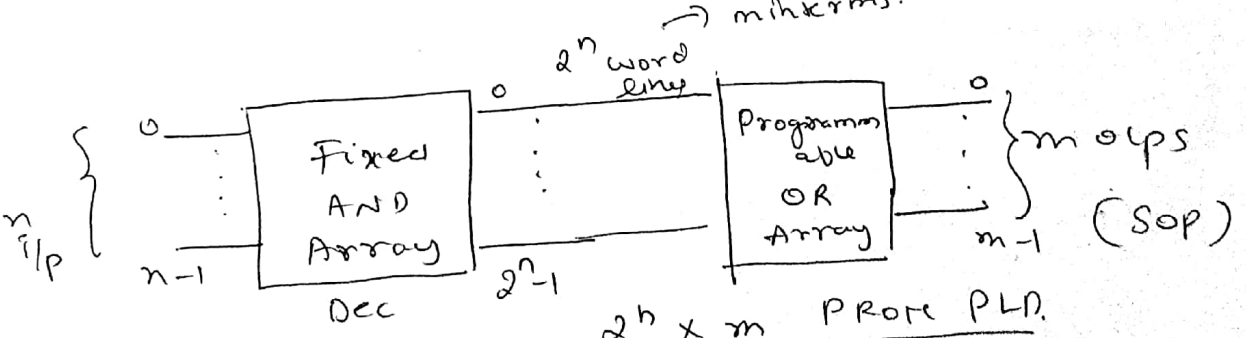
Programmable Logic Devices (PLD)

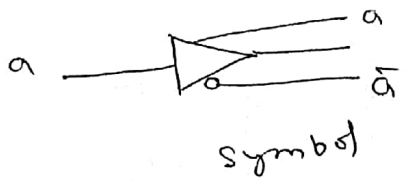
* PLD's consists of an array of AND gates and an array of OR gates.
* Unlike Integrated circuits (IC) which consists of logic gates and have a fixed function.
* A PLD has an undefined function at the time of manufacture.
* Before the PLD can be used in a circuit, it must be programmed (reconfigured) by using a specialized program.
* There are three types of PLD's.
  * PROM → programmable Read only memory
  * PAL → programmable Array Logic.
  * PLA → programmable Logic Array.

* The process of entering the information into these devices is known as programming. (It is reprogrammable)

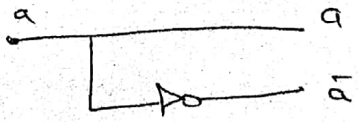


$2^n \times m$ PROM PLD.

* Buffer inverter

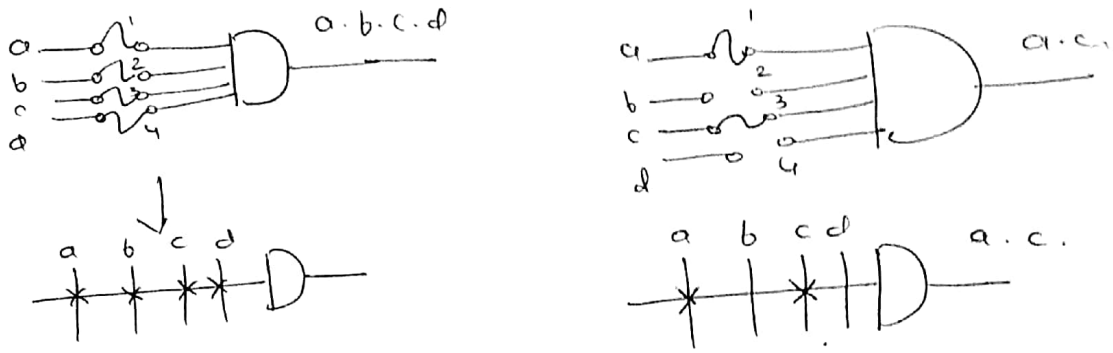


Symbol



Implementation.

* Fusable i/ps.



* Non-fusable

Problem

① Implement the following fn using PROM PLD.

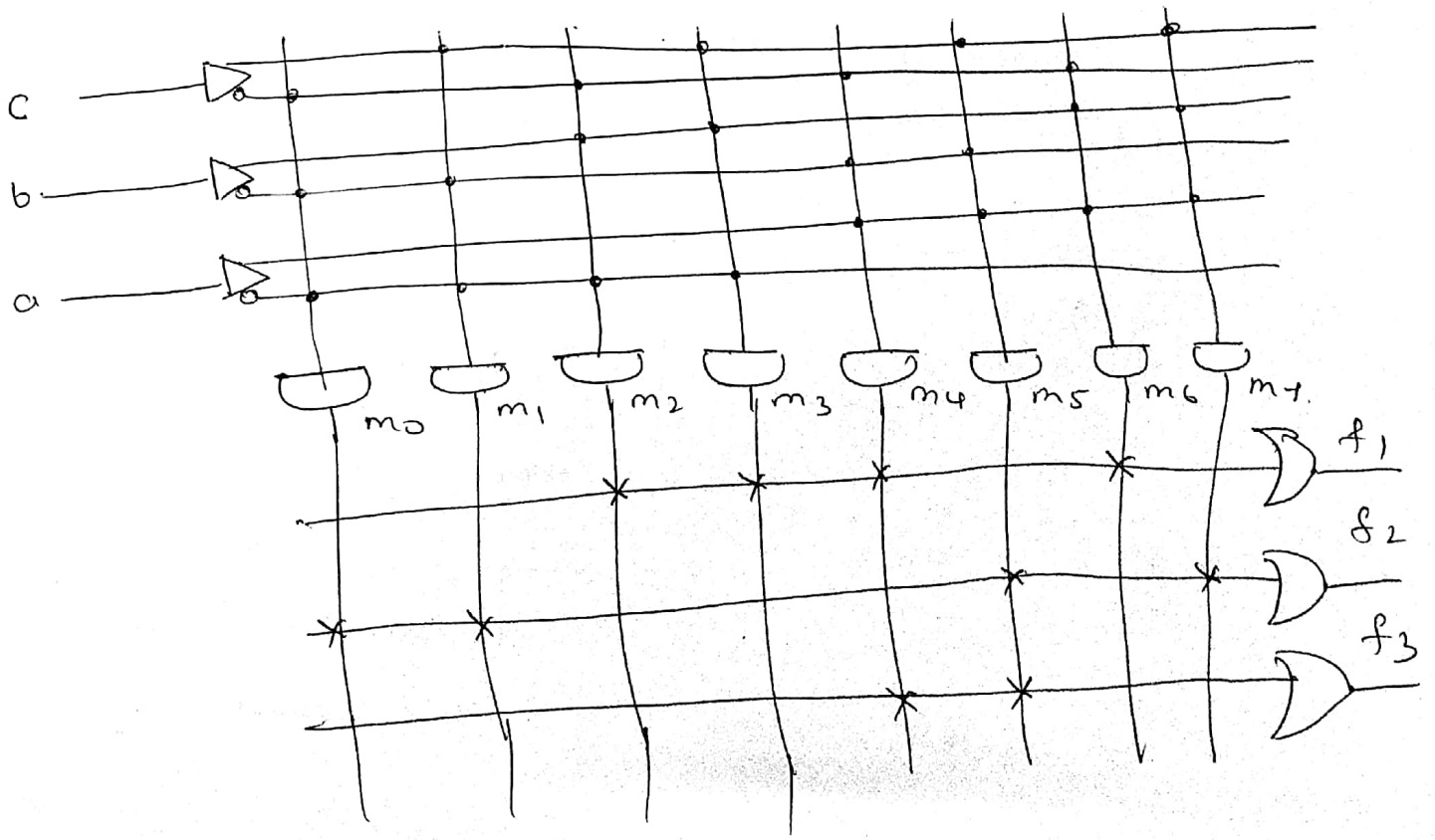
3 × 8 × 3

$f_1(a,b,c) = \Sigma m(2,3,4,6)$

$f_2(a,b,c) = \Sigma m(0,1,5,7)$

$f_3(a,b,c) = \Sigma m(4,5)$.

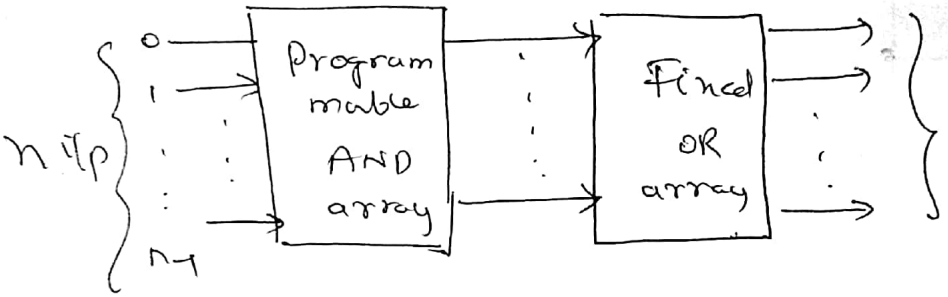
→ This can be implemented on $2^n \times m$ ie is $2^3 \times 3$ PROM as shown



② Programmable Array Logic [PAL]

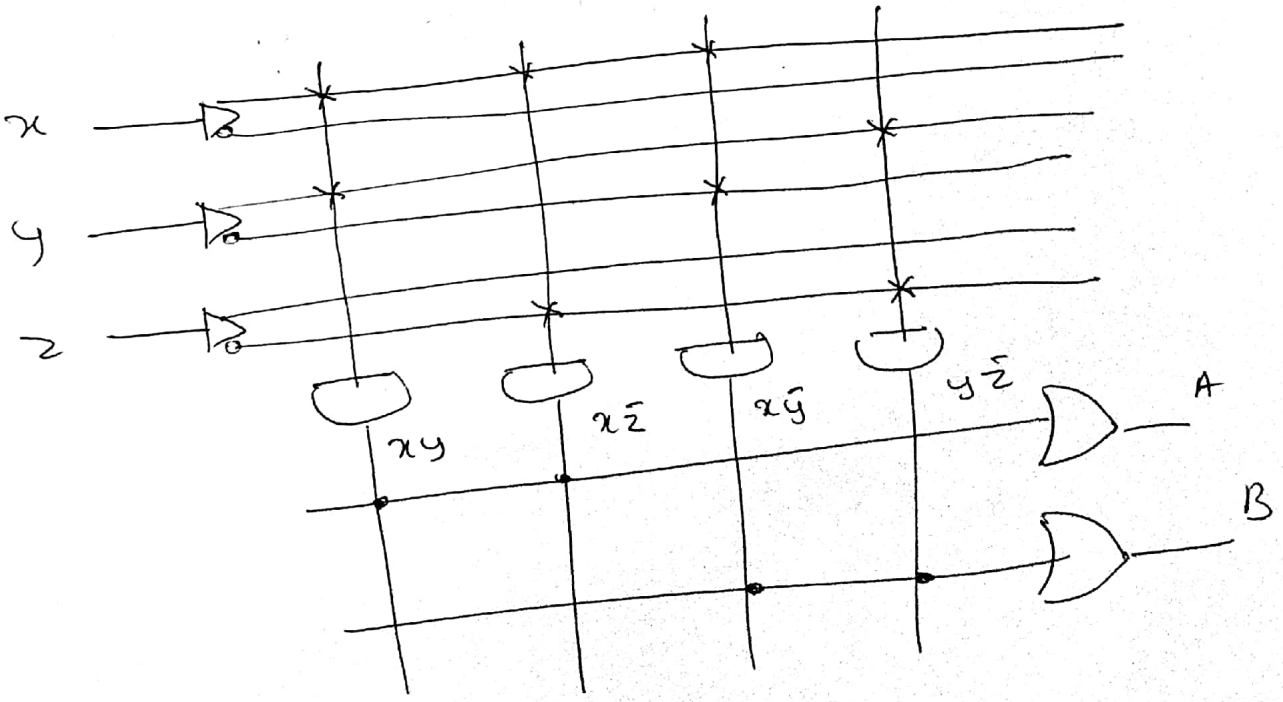
PAL is a programmable logic device that has programmable AND array and fixed OR array.

Advantage : PAL is that only the required product terms of boolean fn can be generated instead of generating all the minterms by using programmable AND gates.



Prob. Implement the following Boolean fn using PAL 3×4×2

$A = xy + x\bar{z}$, $B = x\bar{y} + y\bar{z}$

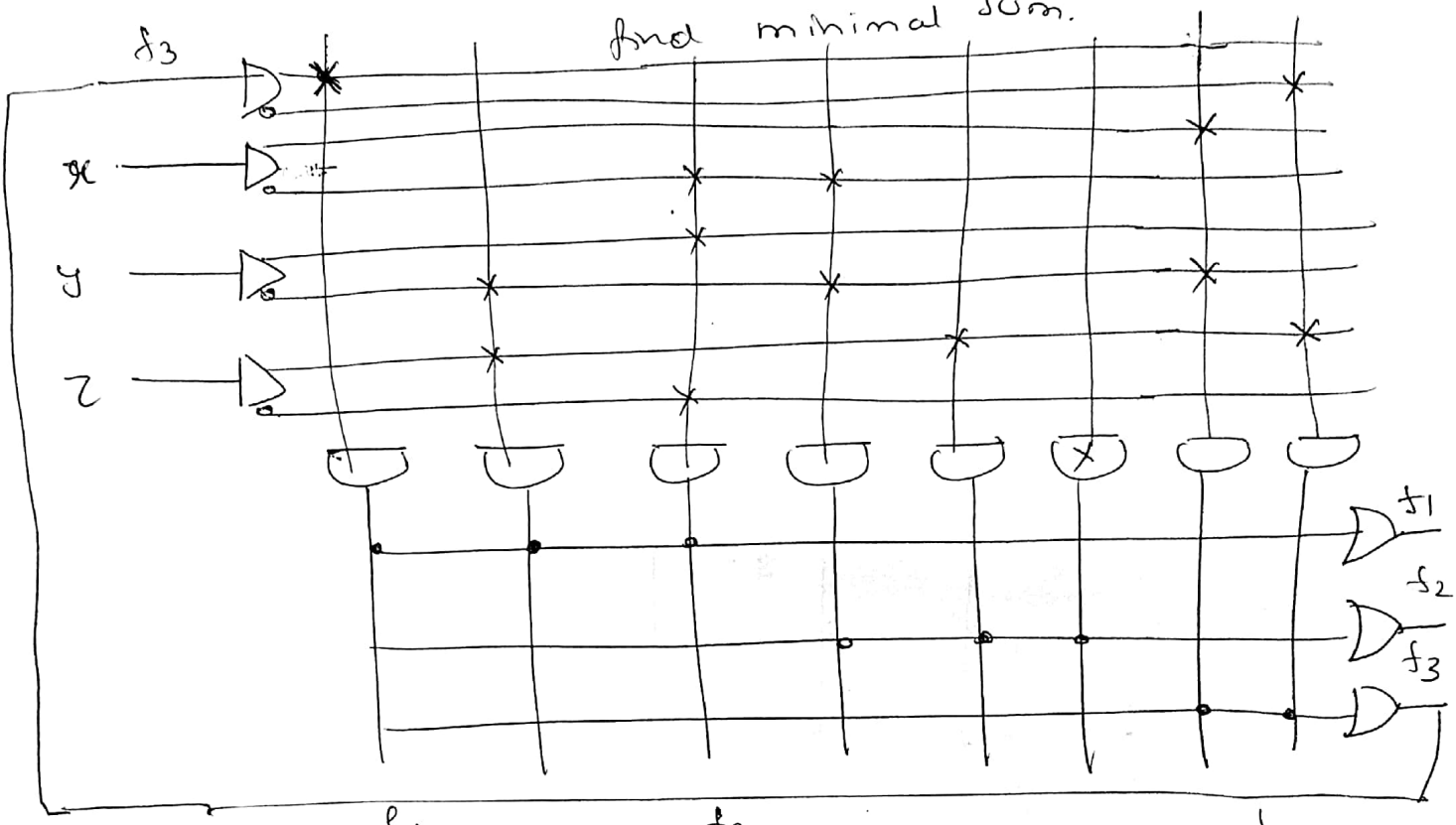


prob Implement the following function to realise the following for using PAL. (3 × 8 × 3)

$f_1(x, y, z) = \Sigma m(1, 2, 4, 5, 7)$

$f_2(x, y, z) = \Sigma m(0, 1, 3, 5, 7)$

find minimal sum.



K-map

f_1

z \ xy	00	01	11	10
0	0 (0)	1 (2)	0 (6)	1 (4)
1	1 (1)	0 (3)	1 (7)	1 (5)

f_2

z \ xy	00	01	11	10
0	1 (0)	0 (2)	0 (6)	0 (4)
1	1 (1)	1 (3)	1 (7)	1 (5)

$f_1 = x\bar{y} + xz + \bar{y}z + \bar{x}y\bar{z}$

$f_2 = \bar{x}\bar{y} + z.$

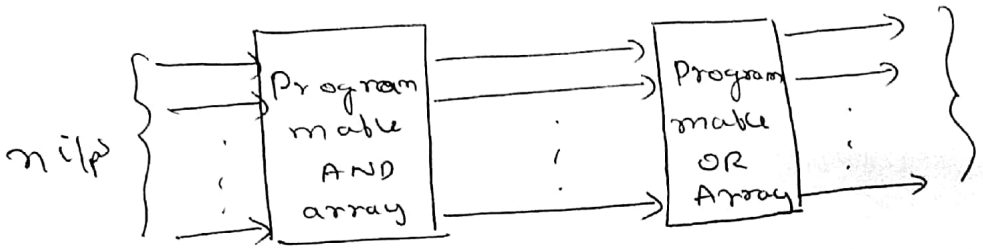
Let $f_3 = x\bar{y} + xz$

$\therefore f_1 = f_3 + \bar{y}z + \bar{x}y\bar{z}$

$f_2 = \bar{x}\bar{y} + z.$

(3) Programable Logic Arrays (PLA's)

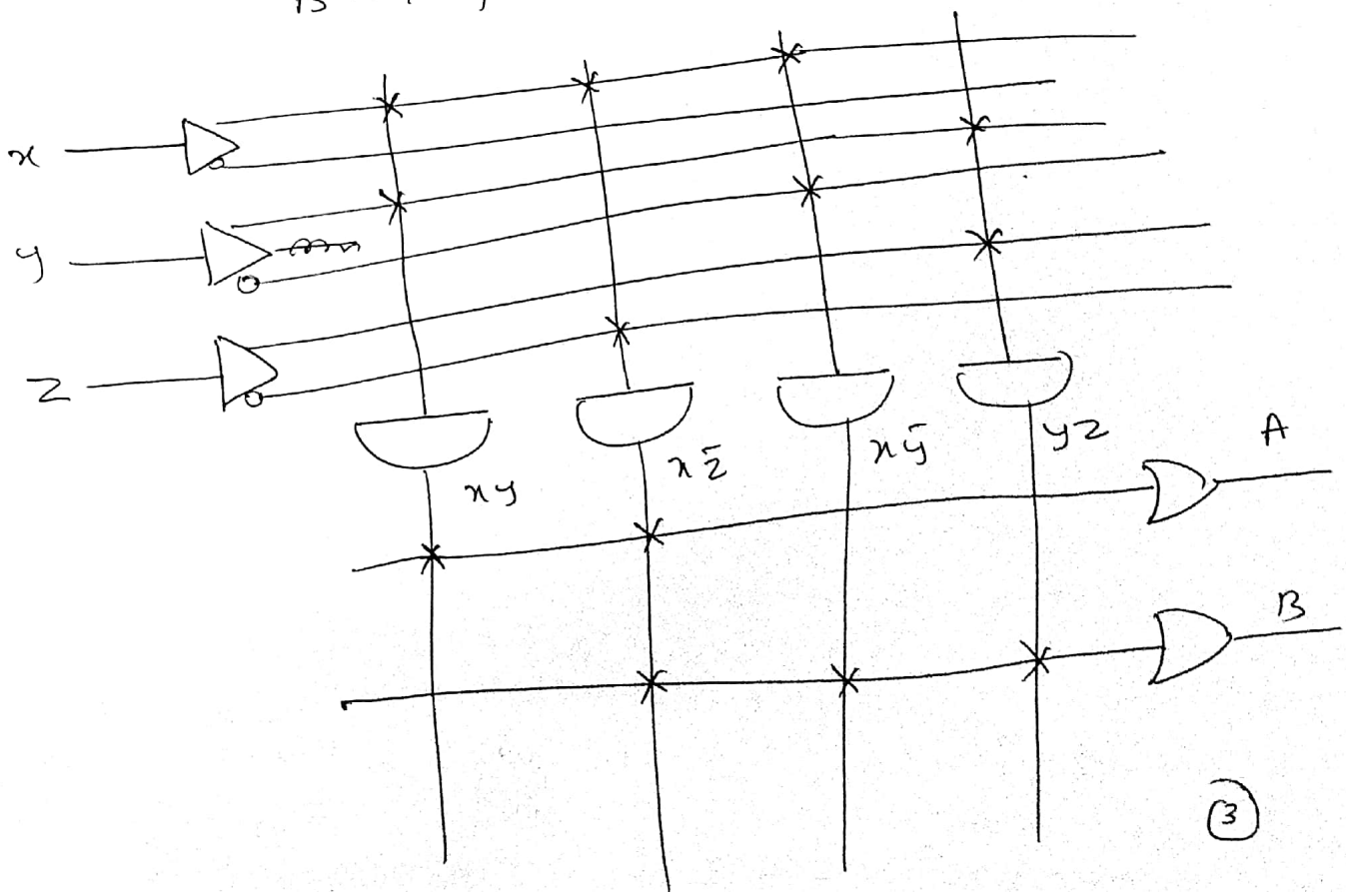
* In PLA both AND Array and OR array are programmable.
* It should be noted that open input terminals to an AND gate is logic-1, while open input terminals to an OR gate is logic 0.



* prob: Implement the following Boolean function using PLA.

$$A = XY + X\bar{Z}$$

$$B = X\bar{Y} + YZ + X\bar{Z}$$



Prob 2 Implement the following function

$f_1(x, y, z) = \Sigma m(0, 1, 3, 4)$

$f_2(x, y, z) = \Sigma m(1, 2, 3, 4, 5)$

using $3 \times 4 \times 2$ PLA.

f_1

z \ xy	00	01	11	10
0	1	0	0	1
1	1	1	0	0

$f_1 = \bar{x}z + \bar{y}\bar{z}$

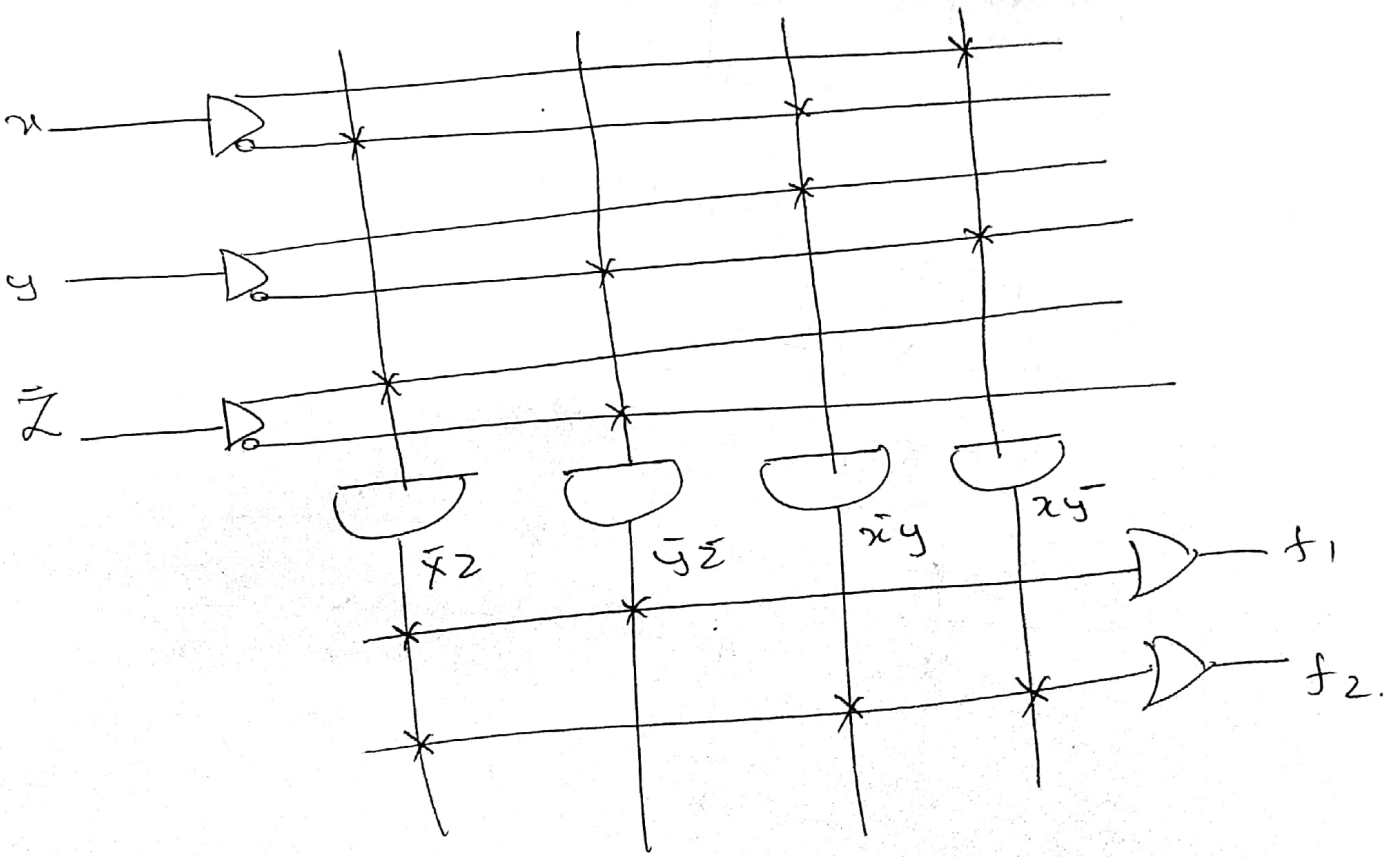
1 2

f_2

z \ xy	00	01	11	10
0	0	1	0	1
1	1	1	0	1

$f_2 = \bar{x}y + x\bar{y} + \bar{x}\bar{z}$

3 4 1



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