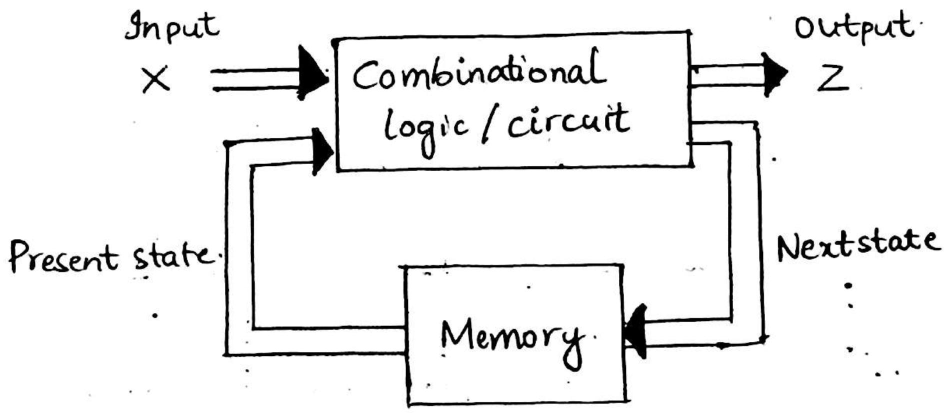
# Module 5 :- Sequential design

**Topics**

Introduction, Mealy and Moore models, State machine notation, synchronous sequential circuit analysis and design.

## Sequential design

- Includes systematic analysis of simple sequential machine.
- The clocked synchronous sequential circuits have master clock which is connected simultaneously to the controlled clock input of all the flip flops in the memory block of the circuit.
- The figure below shows the general configuration of a clocked synchronous sequential circuit input.

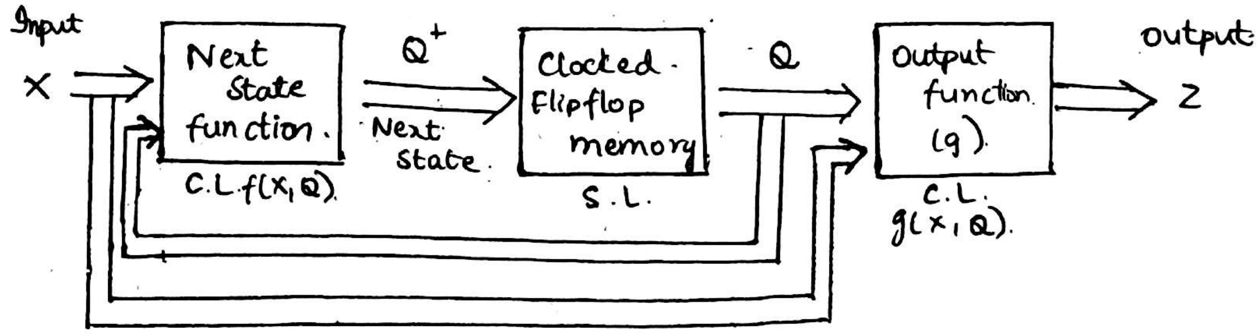



There are two sequential models called.

1) Melay model.
2) Moore model.

1) Melay model.

C.L - combinational logic
S.L - sequential logic.



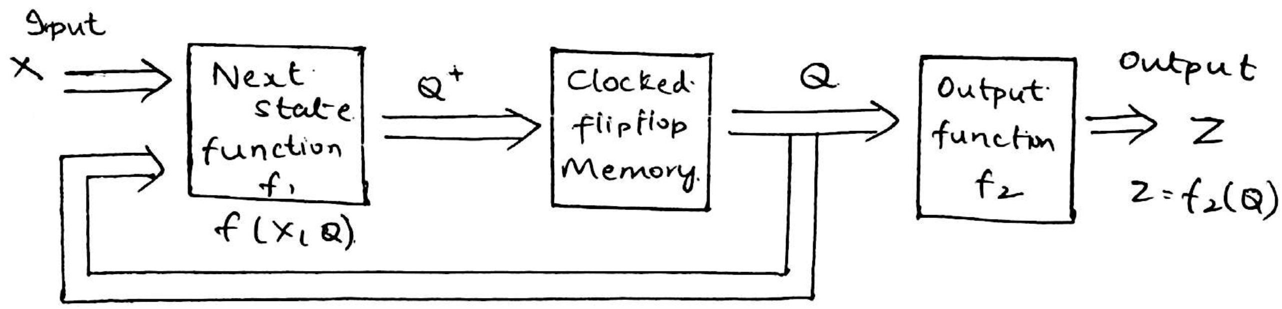
If $x$ denoted the collective external input signal and $Q$ the collective present state of the flipflop then the next state of the network denoted by -

$Q^+ = f(x, Q)$.

similarly. if $z$ is regarded as the collective output signals of the network then under the assumption that the output are the function of both input and present state.

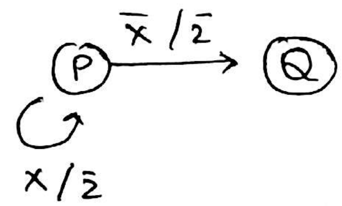
$$z = g(x, Q).$$

(2) Moore model.




Identify the type of machine [Melay / Moore]

(1)




$Q^+ = f(x, Q)$.

$z = f(x, Q)$

$x \rightarrow$ input.

$z \rightarrow$ output.

Numerator $\rightarrow$ Input

Denominator $\rightarrow$ output

$Q \rightarrow$ present state

$Q^+ \rightarrow$ Next state.

Melay model.

- There are two states 'P' and 'Q'
- When at state P

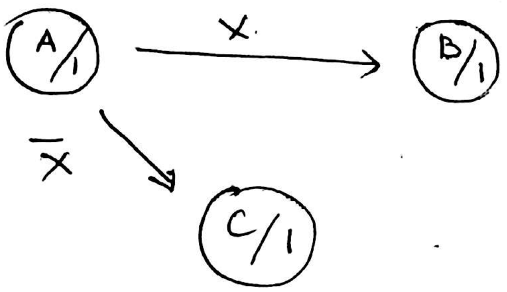
$\rightarrow$ If the input is 1, it remains at state P and output is zero

→ If the input is '0', it makes a transition to the state Q and the output is '0'. Therefore transition to the state Q and the output is '0'. Therefore

$$Q^+ = f(x, Q)$$
$$Z = f(x, Q)$$

This is a melay model.

(2)




$$Q^+ = f(x, Q)$$
$$Z = f(Q)$$

Moore model.

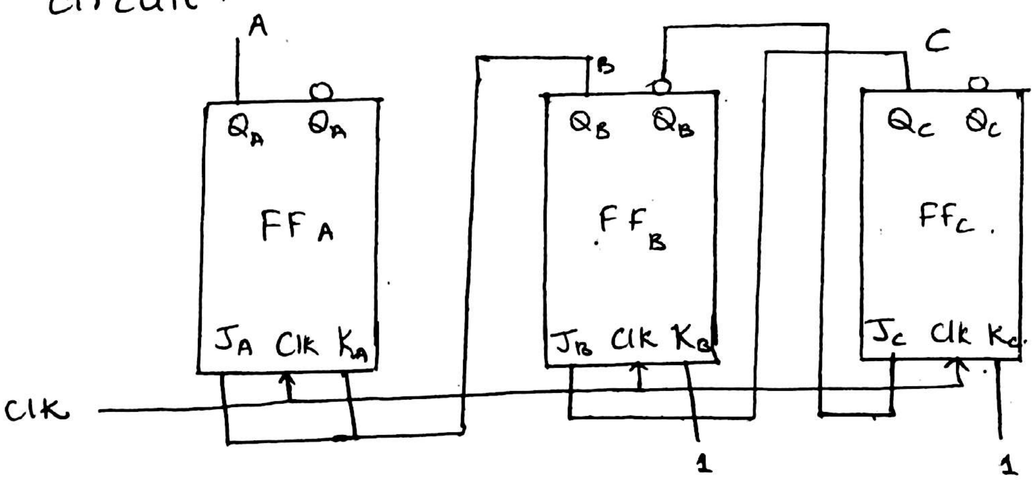
Analysis of sequential circuits.

- Combinational circuits are easy to analyse, we need to write boolean expression for the outputs and write the truth table.
- The operation of sequential circuit is not quite apparent from the diagram
- We need to write the state diagram in order to understand the sequence of state for every clock pulse applied.

The procedure to analyse synchronous circuit is as follows:-

- Identify the state variables. [Flip flop o/p]
- Identify the flip flop type.
- Write the flipflop input equations.
- Construct k-map using flip flop equation.
- Write the state diagram from state transition table.

Analyse the following synchronous sequential circuit.




Soln ① There are 3 state variable A, B, C.

② All are JK flip flop.

③ $J_A = Q_B$, $K_A = \bar{Q}_B$

$J_B = Q_C$, $K_B = 1$

$J_C = \bar{Q}_B$, $K_C = 1$.

④ K-map.

$J_A$ & $K_A$

| $Q_C$ \ $Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |

$J_B$

| $Q_C$ \ $Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

$K_B$ & $K_C$

| $Q_C$ \ $Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $1_0$ | $1_2$ | $1_6$ | $1_4$ |
| 1 | $1_1$ | $1_3$ | $1_7$ | $1_5$ |

$J_C$.

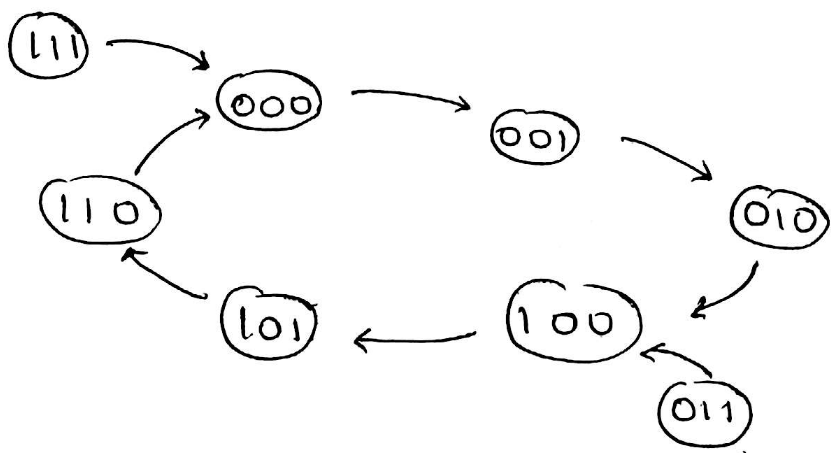
| $Q_C$ \ $Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $1_0$ | $0_2$ | $0_6$ | $1_4$ |
| 1 | $1_1$ | $0_3$ | $0_7$ | $1_5$ |

State transition table.

Decided from P.S & J K

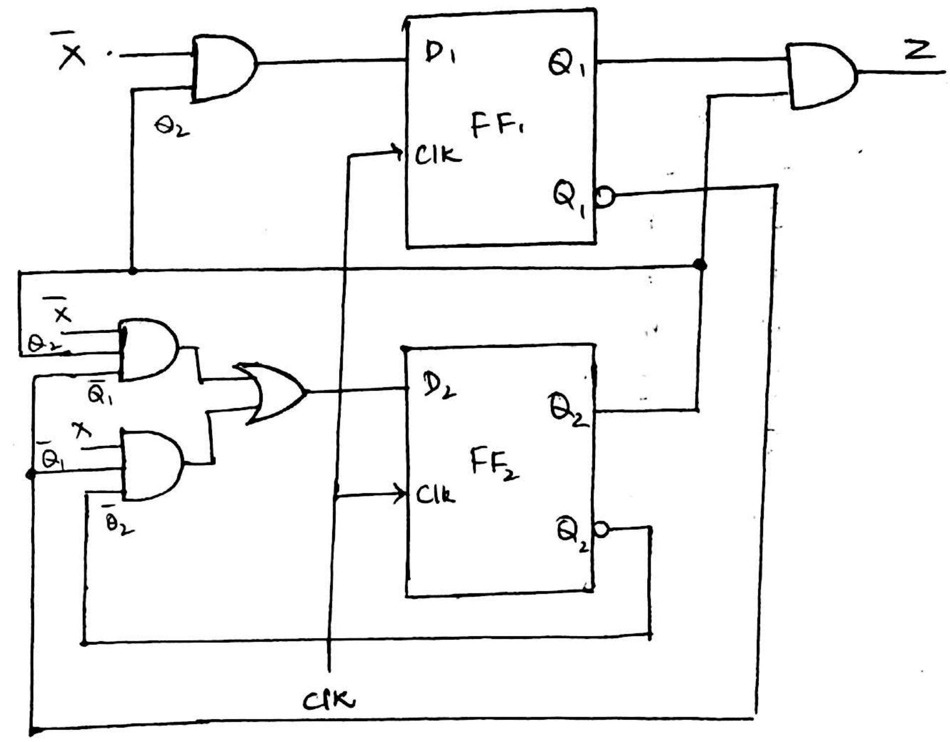
| P.S | | | N.S | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_A$ | $Q_B$ | $Q_C$ | $Q_A^+$ | $Q_B^+$ | $Q_C^+$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

State diagram




Scanned by CamScanner

Analyze synchronous sequential circuit.




Soln ① There are 2 state variable

$Q_1$ , $Q_2$

② Both are D flip flop

③ $D_1 = Q_2 \bar{x}$

$D_2 = \bar{x} Q_2 \bar{Q_1} + \bar{Q}_1 \bar{Q}_2 x$

$= \bar{Q}_1 (\bar{x} Q_2 + \bar{Q}_2 x)$

$= \bar{Q}_1 ( Q_2 \oplus x ]$

$Z = Q_2 Q_1 = Q_1 Q_2$

K-map.

$D_1$

| x \ $Q_1 Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $1_2$ | $1_6$ | $0_4$ |
| 1 | $0_1$ | $0_3$ | $0_7$ | $0_5$ |

$D_2$

| x \ $Q_1 Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $1_2$ | $0_6$ | $0_4$ |
| 1 | $1_1$ | $0_3$ | $0_7$ | $0_5$ |

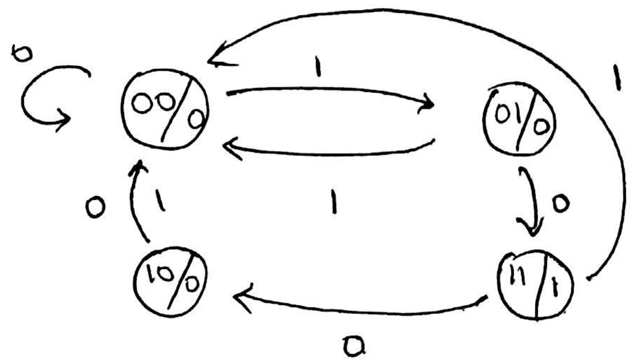
Z

| x \ $Q_1 Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $0_2$ | $1_6$ | $0_4$ |
| 1 | $0_1$ | $0_3$ | $1_7$ | $0_5$ |

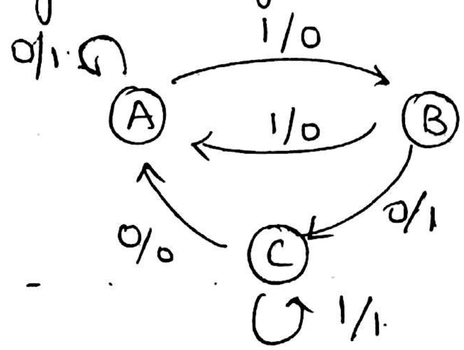
state transition.

| P.S | | | N.S | | $D_1$ | $D_2$ | Z |
|---|---|---|---|---|---|---|---|
| $Q_1$ | $Q_2$ | X | $Q_1^+$ | $Q_2^+$ | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

Moore model.




Realise the system represented by the following State diagram using D-FF




Soln

In order to generate 3 states, we require 2 flipflops..

State assignment.

Assuming $A = 00$, $B = 01$, $C = 10$

| P.S. | | | N.S. | | | | |
|---|---|---|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $X$ | $Q_1^+$ | $Q_2^+$ | $D_1$ | $D_2$ | $Z$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | X | X | X | X | X |
| 1 | 1 | 1 | X | X | X | X | X |

K-map

$D_1$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $1_2$ | $X_6$ | $0_4$ |
| 1 | $0_1$ | $0_3$ | $X_7$ | $1_5$ |

$D_1 = Q_2\overline{X} + Q_1X$

$D_2$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $0_2$ | $X_6$ | $0_4$ |
| 1 | $1_1$ | $0_3$ | $X_7$ | $0_5$ |

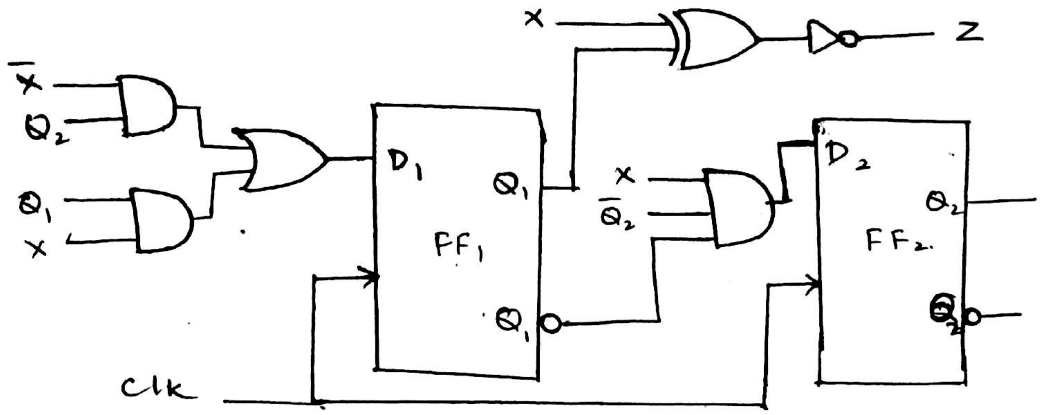
$D_2 = \overline{Q}_1\overline{Q}_2X$

$Z$

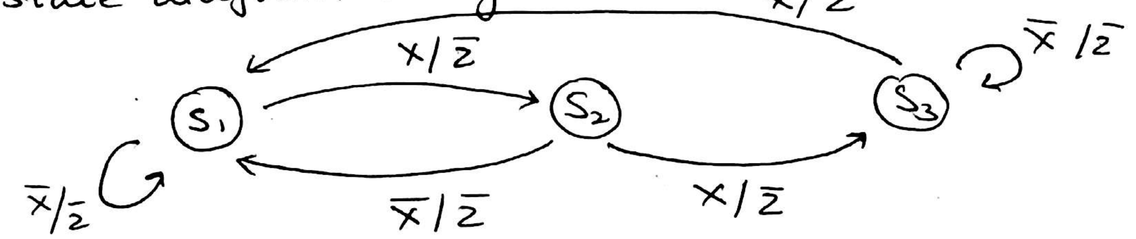
| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $1_0$ | $1_2$ | $X_6$ | $0_4$ |
| 1 | $0_1$ | $0_3$ | $X_7$ | $1_5$ |

$Z = \overline{Q}_1\overline{X} + Q_1X$

$= \overline{Q_1 \oplus X}$




Realise the system represented by the following state diagram using T-FF



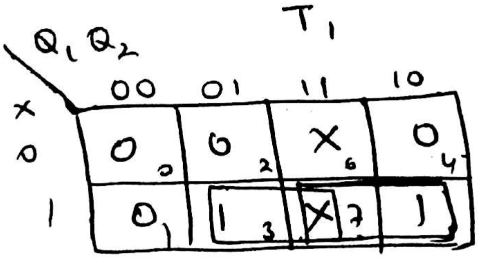

<u>Soln</u> we use 2 flip flops for 3 states.

Assume $S_1 = 00$
$S_2 = 01$
$S_3 = 10$

| P.S. $Q_1$ | $Q_2$ | $X$ | N.S. $Q_1^+$ | $Q_2^+$ | $T_1$ | $T_2$ | $Z$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

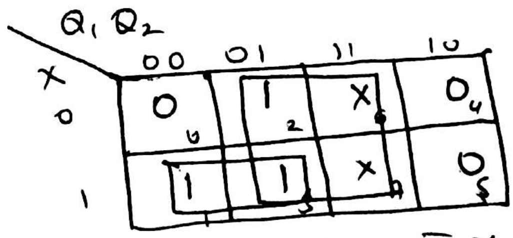
K-map.

$T_1$




$T_1 = Q_2 X + Q_1 X$

$T_2$

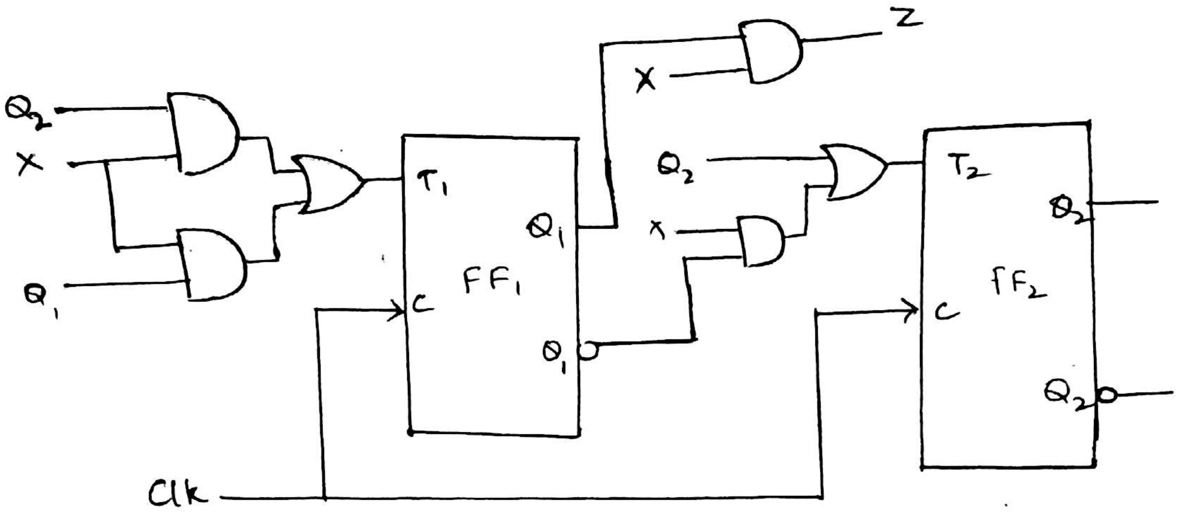



$T_2 = Q_2 + \bar{Q}_1 X$

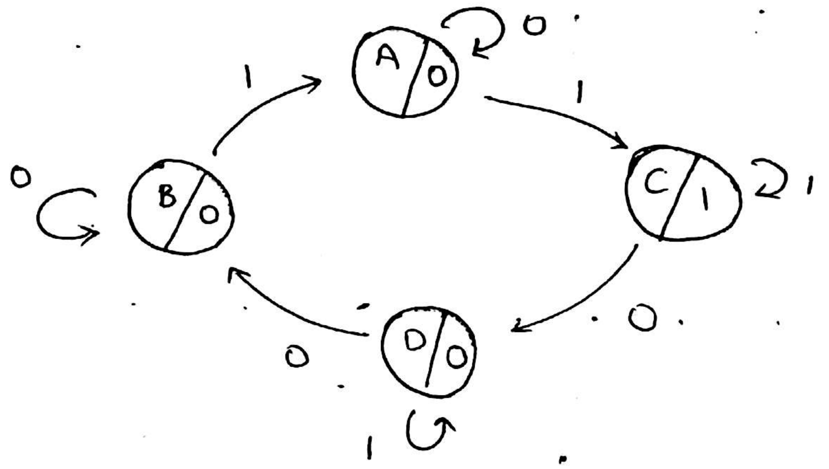
Z

| $x \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | X | 0 |
| 1 | 0 | 0 | X | 1 |

$$Z = Q_1 X$$




Realise the circuit diagram using JK flip flop




Soln We use 2 flip flops for 4 states.

Assume :-

A = 0 0

B = 0 1

C = 1 0

D = 1 1

| P.S | | | N.S. | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $X$ | $Q_1^+$ | $Q_2^+$ | $J_1$ | $K_1$ | $J_2$ | $K_2$ | $Z$ |
| 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | X | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | X | 0 | X | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | X | X | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | X | X | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | X | 0 | 1 | X | 1 |
| 1 | 0 | 1 | 1 | 0 | X | 0 | 0 | X | 1 |
| 1 | 1 | 0 | 0 | 1 | X | 1 | X | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | X | 0 | X | 0 | 0 |

Kmap.

$J_1$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $0_2$ | $X_6$ | $X_4$ |
| 1 | $\boxed{1}_1$ | $0_3$ | $X_7$ | $\boxed{X}_5$ |

$J_1 = \bar{Q}_2 X$

$K_1$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $X_0$ | $X_2$ | $1_6$ | $0_4$ |
| 1 | $X_1$ | $X_3$ | $0_7$ | $0_5$ |

$K_1 = Q_2 \bar{X}$

$J_2$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $X_2$ | $X_6$ | $1_4$ |
| 1 | $0_1$ | $X_3$ | $X_7$ | $0_5$ |

$J_2 = Q_1 \bar{X}$

$K_2$

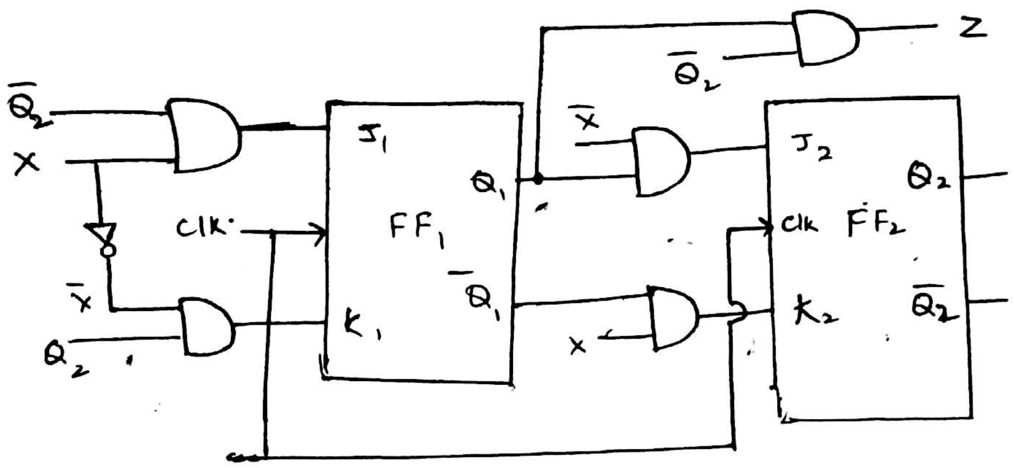
| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $X_0$ | $0_2$ | $0_6$ | $X_4$ |
| 1 | $X_1$ | $1_3$ | $0_7$ | $X_5$ |

$K_2 = \bar{Q}_1 X$

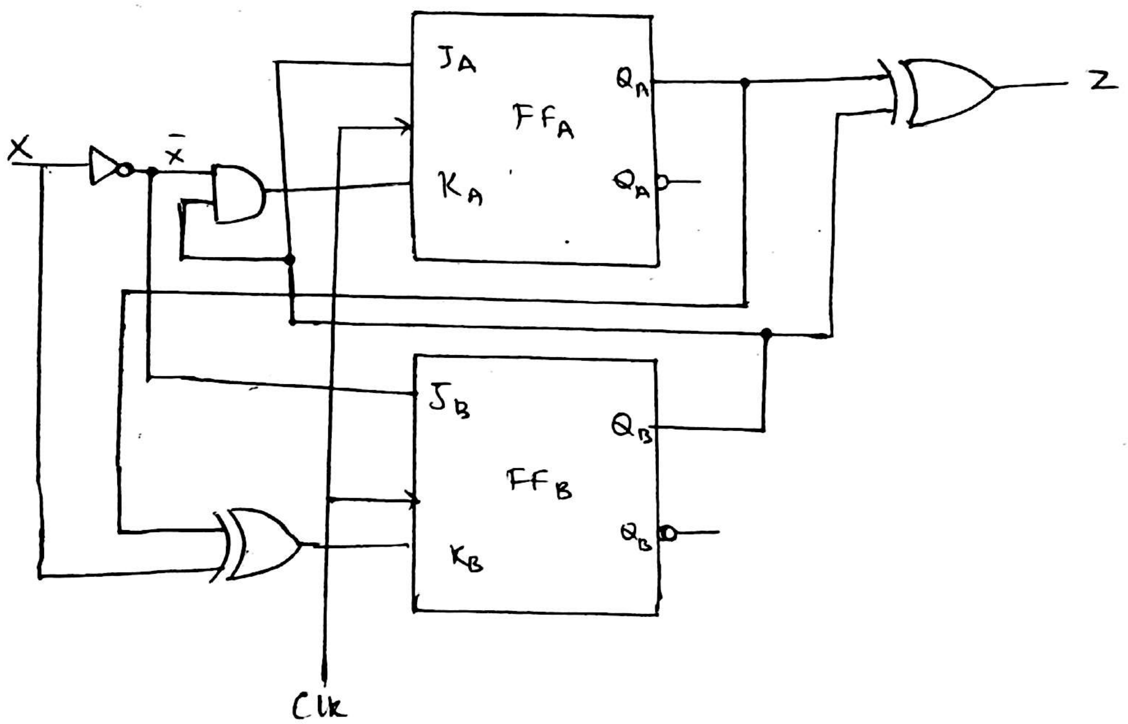
$Z$

| $X \backslash Q_1Q_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $0_0$ | $0_2$ | $0_6$ | $1_4$ |
| 1 | $0_1$ | $0_3$ | $0_7$ | $1_5$ |

$Z = Q_1 \bar{Q}_2$




Analyse synchronous sequential circuit -




<u>Soln</u>

- We have used 2 flipflop.
- All are JK flipflops.

$J_A = Q_B$ $\quad\quad K_A = \bar{x}\, Q_B$

$J_B = \bar{x}$ $\quad\quad K_B = Q_A \bar{x} + x \overline{Q_A}$

$$Z = Q_B \overline{Q_A} + Q_A \overline{Q_B}$$

K-map

$J_A$

| $X \backslash Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |

$K_A$

| $X \backslash Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |

$J_B$

| $X \backslash Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |

$K_B$

| $X \backslash Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

Z

| $X \backslash Q_AQ_B$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |

| P.S. | | | N.S. | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $Q_A$ | $Q_B$ | $X$ | $Q_A^+$ | $Q_B^+$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ | Z |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |