DEPARTMENT
OF
ELECTRONICS & COMMUNICATION ENGINEERING

DIGITAL ELECTRONICS LABORATORY MANUAL

III Semester (18EC3DLDEL)

Autonomous Course

Lab In-Charges: Prof. Shashi Raj K
Dr. K N Pushpalatha
Dr. Thenmozhi S

Lab Instructors: Mr. Shivaswamy
Mr. Ramamurthy N

HOD: Dr. T.C. Manjunath

Name of the Student	:	
Semester /Section	:	
USN	:	
Batch	:	

Dayananda Sagar College of Engineering
Shavige Malleshwara Hills, Kumaraswamy Layout,
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Web - http://www.dayanandasagar.edu Email : hod-ece@dayanandasagar.edu
(An Autonomous Institute Affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)
(Accredited by NBA, National Assessment & Accreditation Council (NAAC) with 'A' grade)

Dayananda Sagar College of Engineering

Dept. of E & C Engineering

Name of the Laboratory	**:**	DIGITAL ELECTRONICS LAB
Semester/Academic Year	**:**	III / 2019-20
No. of Students/Batch	**:**	20
No. of Equipment's	**:**	20
Major Equipment's	**:**	CRO's Sine/Square/Wave Generator Function Generator IC Tester Digital IC Trainer Kit
Area in square meters	**:**	109 Sq Mts
Location	**:**	Level – 2
Total Cost of Lab	**:**	Rs. 37, 77,535/-
Lab In charge/s	**:**	Prof. Shashi Raj K Dr. K N Pushpalatha Dr. Thenmozhi S
Instructors	**:**	Mr. Shivaswamy Mr. Ramamurthy N
HOD	**:**	Dr. T.C. Manjunath, Ph.D. (IIT Bombay)

About the College & the Department

The Dayananda Sagar College of Engineering was established in 1979, was founded by Sri R. Dayananda Sagar and is run by the Mahatma Gandhi Vidya Peetha Trust (MGVP). The college offers undergraduate, post-graduates and doctoral programmes under Visvesvaraya Technological University & is currently autonomous institution. MGVP Trust is an educational trust and was promoted by Late. Shri. R. Dayananda Sagar in 1960. The Trust manages 28 educational institutions in the name of "Dayananda Sagar Institutions" (DSI) and multi – Specialty hospitals in the name of Sagar Hospitals - Bangalore, India. Dayananda Sagar College of Engineering is approved by All India Council for Technical Education (AICTE), Govt. of India and affiliated to Visvesvaraya Technological University. It has widest choice of engineering branches having 16 Under Graduate courses & 17 Post Graduate courses. In addition, it has 21 Research Centres in different branches of Engineering catering to research scholars for obtaining Ph.D under VTU. Various courses are accredited by NBA & the college has a NAAC with ISO certification. One of the vibrant & oldest dept is the ECE dept. & is the biggest in the DSI group with 70 staffs & 1200+ students with 10 Ph.D.'s & 30^{+} staffs pursuing their research in various universities. At present, the department runs a UG course (BE) with an intake of 240 & 2 PG courses (M.Tech.), viz., VLSI Design Embedded Systems & Digital Electronics & Communications with an intake of 18 students each. The department has got an excellent infrastructure of 10 sophisticated labs & dozen class room, R & D centre, etc…

Vision of the College:

To impart quality technical education with a focus on Research and Innovation emphasising on Development of Sustainable and Inclusive Technology for the benefit of society.

Mission of the College:

- To provide an environment that enhances creativity and Innovation in pursuit of Excellence.
- To nurture teamwork in order to transform individuals as responsible leaders and entrepreneurs.
- To train the students to the changing technical scenario and make them to understand the importance of Sustainable and Inclusive technologies.

Vision of the Department

To achieve continuous improvement in quality technical education for global competence with focus on industry, societal needs, research and professional success.

Mission of the Department

- Offering quality education in Electronics and Communication Engineering with effective teaching learning process in multidisciplinary environment.
- Training the students to take-up projects in emerging technologies and work with team spirit.
- To imbibe professional ethics, development of skills and research culture for better placement opportunities.

Programme Educational Objectives [PEOs]

The Graduate students must be able to:

PEO-1: Ready to apply the state-of-art technology in industry and meeting the societal needs with knowledge of Electronics and Communication Engineering due to strong academic culture.

PEO-2: Competent in technical and soft skills to be employed with capability of working in multidisciplinary domains.

PEO-3: Professionals, capable of pursuing higher studies in technical, research or management programs.

Programme Specific Outcomes [PSOs]

PSO-1: Design, develop and integrate electronic circuits and systems using current practices and Standards.

PSO-2: Apply knowledge of hardware and software in designing Embedded and Communication Systems.

DIGITAL ELECTRONICS LAB

Course code: 18EC3DLDEL **Credits: 02**
L: P: T: S: 0: 2: 1: 0 **CIE Marks: 50**
Exam Hours: 03 **SEE Marks: 50**

Course Objectives:
This laboratory course enables students to get practical experience in design, realisation and verification of

1. SOP and POS forms.
2. Half/Full adder and Half/Full Subtractors using logic gates
3. Parallel adder and code converters.
4. Multiplexer using logic gate and IC
5. Demultiplexer /Decoder using logic gate and IC
6. Flip Flops, Counters and Shift register.

Syllabus:

Experiment. No.	Contents of the Experiment	Hours	COs
1	Simplification, realization of Boolean expressions using logic gates/Universal gates.	03	CO1 CO2
2	Realization of Half/Full adder and Half/Full Subtractors using logic gates.	03	CO2
3	Using 7483 chip (i) Realization of parallel adder/Subtractors (ii) BCD to Excess-3 code conversion and vice versa.	02	CO2
4	Realization of Binary to Gray code conversion and vice versa	02	CO4
5	MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.	02	CO5
6	Realization of One/Two bit comparator and study of 7485 magnitude comparator.	02	CO4
7	Use of a) Decoder chip to drive LED display, b) Priority encoder.	02	CO2
8	Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.	02	CO3
9	Design and Realization of 3 bit counters as a sequential circuit and MOD– N counter (7476, 7490, 74192, 74193).	02	CO3 CO5
10	Shift left, Shift right, SIPO, SISO, PISO, PIPO operations using 74LS95	02	CO3
11	Wiring and testing of Ring counter/Johnson counter	02	CO6
12	Wiring and testing of Sequence generator.	02	CO6

Course Outcomes:

At the end of the course, student will be able to:

CO1	Demonstrate the truth table of various expressions and Combinational circuits using logic gates.
CO2	Construct, realize and test combinational circuits
CO3	Construct, realize and test sequential circuits
CO4	Design and evaluate combinational circuits
CO5	Design and evaluate sequential circuits like counters using ICs
CO6	Apply the knowledge of shift registers into applications like Ring counter, Johnson counter and Sequence generator.

Mapping of Course outcomes to Program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	-	-	-	-	-	-	2	-	-	-	-	-
CO2	2	2	1	-	-	-	-	-	2	-	-	-	1	1
CO3	2	2	1	-	-	-	-	-	2	-	-	-	1	1
CO4	2	2	2	-	-	-	-	-	2	-	-	-	2	2
CO5	2	2	2	-	-	-	-	-	2	-	-	-	2	2
CO6	2	2	2	-	-	-	-	-	2	-	-	-	2	2

DIGITAL ELECTRONICS LABORATORY (18EC3DLDEL)

I - CYCLE

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.

2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.

3. Using 7483 chip i) Realization of parallel adder/Subtractor.
   ii) BCD to Excess-3 code conversion and vice versa.

4. Realization of Binary to Gray code conversion and vice versa.

5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits.

6. Realization of One bit comparator and study of 7485 magnitude comparator.

7. Use of a) Decoder chip to drive LED display
   b) Priority encoder.

II – CYCLE

8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.

9. Design and Realization of 3 bit counters as a sequential circuit and MOD– N counter (7476, 7490, 74192, 74193).

10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74LS95.

11. Wiring and testing Ring counter/Johnson counter.

12. Wiring and testing of Sequence generator.

DAYANANDA SAGAR COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING
BENGALURU – 560078

DO's

- All the students should come to LAB on time with proper dress code and identity cards.
- Keep your belongings in the corner of laboratory.
- Students have to enter their name, USN, time-in/out and signature in the log register maintained in the laboratory.
- All the students should submit their records before the commencement of Laboratory experiments.
- Students should come to the lab well prepared for the experiments which are to be performed in that particular session.
- Students are asked to do the experiments on their own and should not waste their precious time by talking, roaming and sitting idle in the labs.
- Observation book and record book should be complete in all respects and it should be corrected by the staff member.
- Before leaving the laboratory students should arrange their chairs and leave in orderly manner after completion of their scheduled time.
- Prior permission to be taken, if for some reasons, they cannot attend lab.
- Immediately report any sparks/ accidents/ injuries/ any other untoward incident to the faculty /instructor.
- In case of an emergency or accident, follow the safety procedure.
- Switch OFF the power supply after completion of experiment.

DONT's

- The use of mobile/ any other personal electronic gadgets is prohibited in the laboratory.
- Do not make noise in the Laboratory & do not sit on experiment table.
- Do not make loose connections and avoid overlapping of wires
- Don't switch on power supply without prior permission from the concerned staff.
- Never leave the experiments while in progress.
- Do not leave the Laboratory without the signature of the concerned staff in observation book.

Experiment No: 1 Date:

Logic Gates

Aim: Simplification, realization of Boolean expression using logic gates/universal gates

a) Verification of Logic gates.

b) Realization of logical expressions Using Logic gates and Universal gates.

i) SOP form ii) POS form

Components required:-

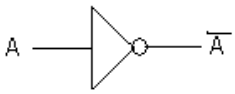
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	AND gate	7408
2	OR gate	7432
3	Not gate	7404
4	EXOR gate	7486
5	NAND gate	7400
6	NOR gate	7402
8	Patch chords	
9	Trainer Kit	

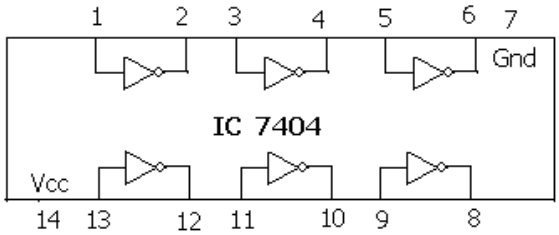
a) Verification of Logic gates.

NOT GATE

TRUTH TABLE SYMBOL IC7404

I/P (A)	O/P $\overline{(A)}$
0	1
1	0



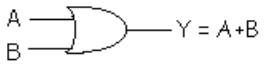


OR GATE

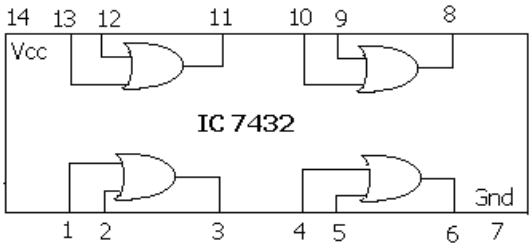
TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

SYMBOL



IC7432

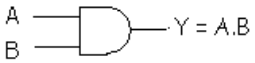


AND GATE

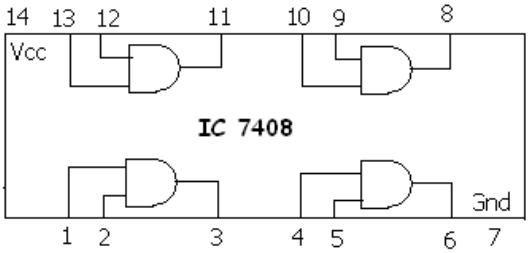
TRUTH TABLE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

SYMBOL



IC7408

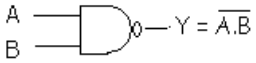


NAND GATE

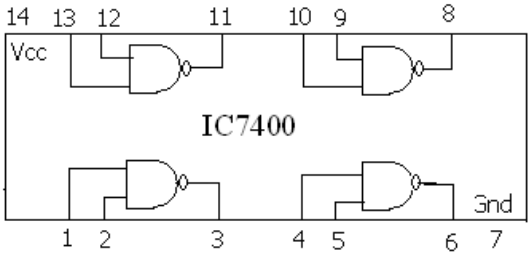
TRUTH TABLE

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

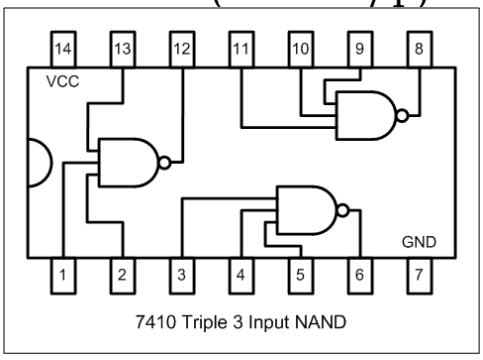
SYMBOL



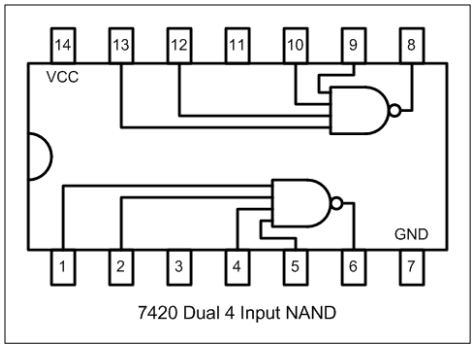
IC7400(Two i/p)



IC 7410(Three i/p)



IC 7420(Four i/p)

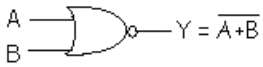


NOR GATE

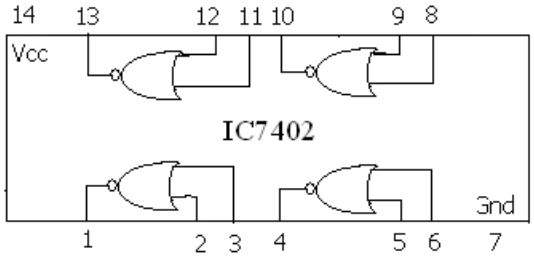
TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

SYMBOL



IC7402

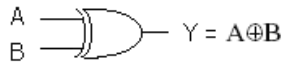


XOR GATE

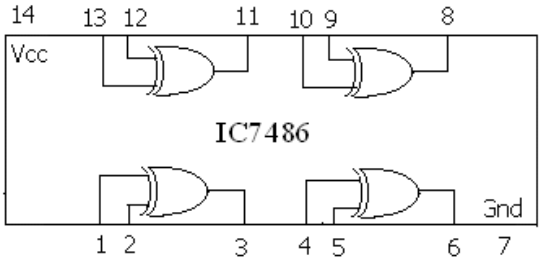
TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

SYMBOL



IC7486



NOT gate	
A	$\overline{A}$
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Procedure:

1. Place the IC in the socket of the trainer kit.
2. Make the connections for the gate as shown in the circuit diagram.
3. Verify the Truth Table.
4. Repeat the above steps for other gates in the different IC chips.

b) Realization of logical expressions Using Logic gates and Universal gates.
i) SOP form ii) POS form

Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	AND gate	7408
2	OR gate	7432
3	Not gate	7404
4	EXOR gate	7486
5	NAND gate	7400
6	NOR gate	7402
7	Patch chords	
8	Trainer Kit	

THEORY : To minimize a boolean expression we can employ any one of the following techniques:

i) Boolean Algebra
ii) Karnaugh maps.

Before we proceed to simplification techniques, two forms of the Boolean expression must be noted

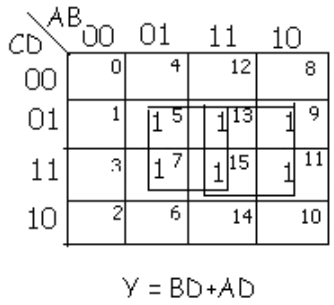
1) Sum of product (SOP):
Ex: ABC+AB+AC

2) Product of Sum (POS) :
Ex: (A+B+C)(A+B)+(A+C)

i) SUM OF PRODUCT (SOP):

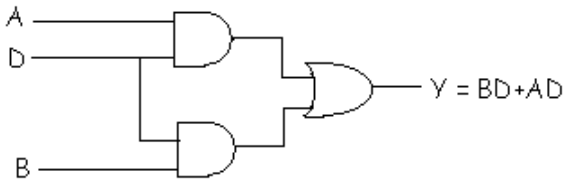
$$F(A,B,C,D) = \sum(5,7,9,11,13,15)$$

Simplification- SOP form

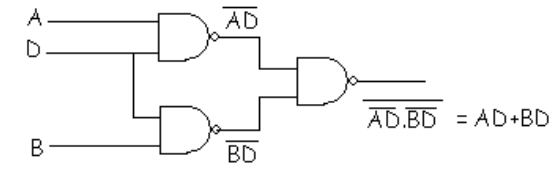


Y = BD+AD

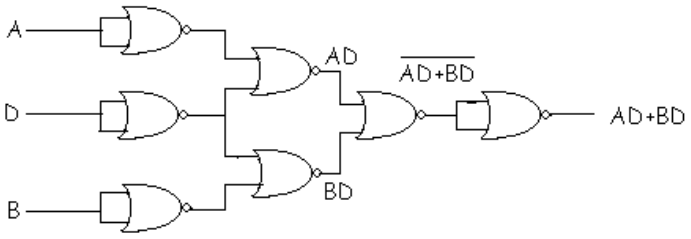
Using Basic Gates



Using NAND gates

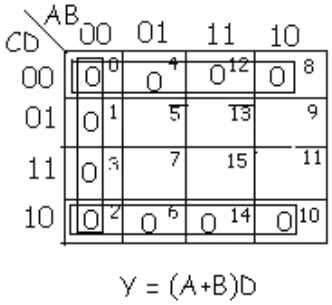


Using NOR Gates



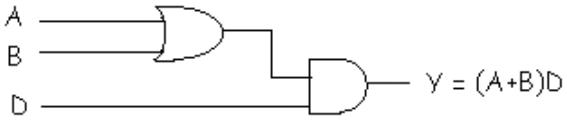
ii)PRODUCT OF SUM : F(A,B,C,D) = ∏(0,1,2,3,4,6,8,10,12,14)

Simplification- POS form

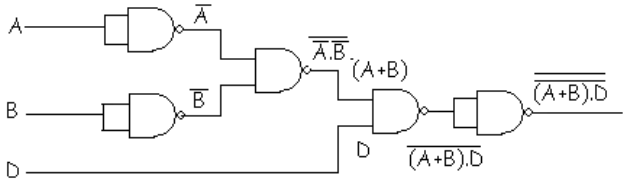


Y = (A+B)D

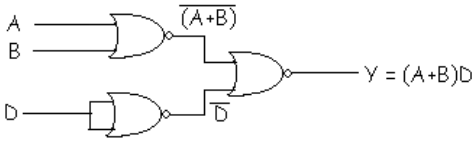
Using Basic Gates



Using NAND gates



Using NOR gates



TRUTH TABLE:

A	B	D	Y=(A+B)D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

PROCEDURE:

1. Place the IC in the socket of the trainer kit.
2. Make the connections as shown in the circuit diagram.
3. Apply diff combinations of i/ps according to the truth table and Verify the o/p.
4. Repeat the above procedure for all the circuit diagrams.

***NOTE: The Truth Table is common for Both SOP and POS form.**

Results:

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No: 2 Date:

HALF ADDER & FULL ADDER

AIM: Realization of (a) Half /Full adder
(b)Half/Full subtractor
using logic gates

COMPONENTS REQUIRED :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	AND gate	7408
2	OR gate	7432
3	Not gate	7404
4	EXOR gate	7486
5	NAND gate	7400
6	NOR gate	7402
7	Patch chords	
8	Trainer Kit	

THEORY: The basic rules of binary addition are

0+0 = 0
0+1 = 1
1+0 = 1
1+1 = $(10)_2$

Column by column addition, similar to decimal addition is performed a logic circuit known as half adder adds two 1 bit signals. In octual addition there is often a thiral bit, the carry bit that must be added. Hence to add 3 bits at a time a logic circuit known as a Full adder is used.

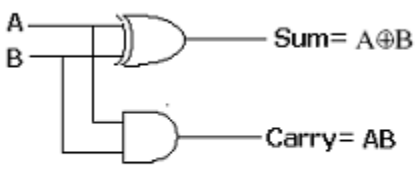
a) Verify the truth table for half adder and full adder circuits using basic and universal gates

i) HALF ADDER USING BASIC GATES

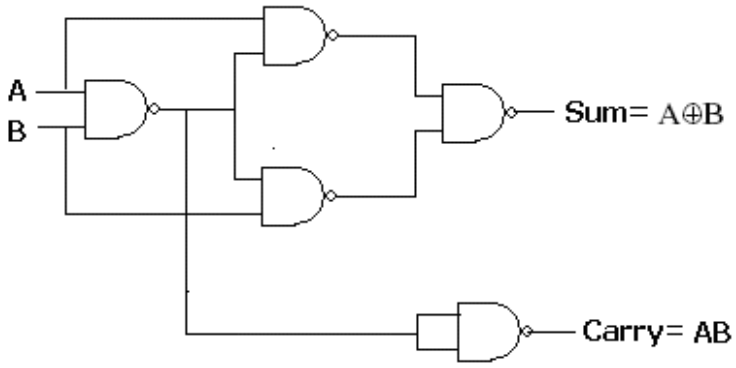
A	B	Sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$Sum=\overline{A}B+A\overline{B}$

Carry =AB



HALF ADDER USING NAND GATES



ii) FULL ADDER:

Truth table (Full adder)

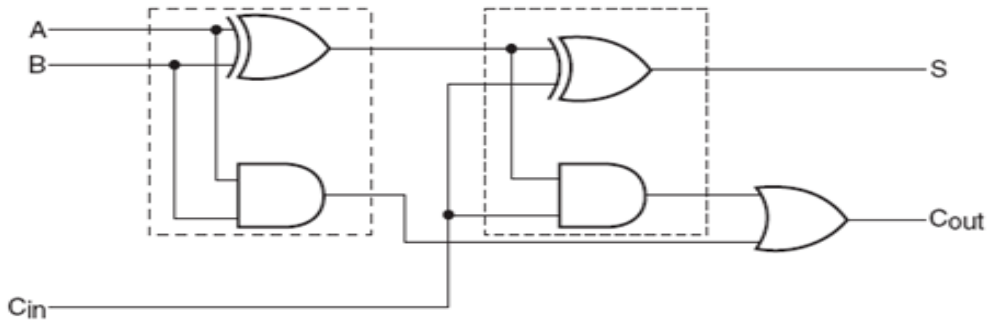
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$SUM = \overline{A}\,\overline{B}\,Cin + \overline{A}\,B\,\overline{Cin} + A\,\overline{B}\,\overline{Cin} + A\,B\,Cin$

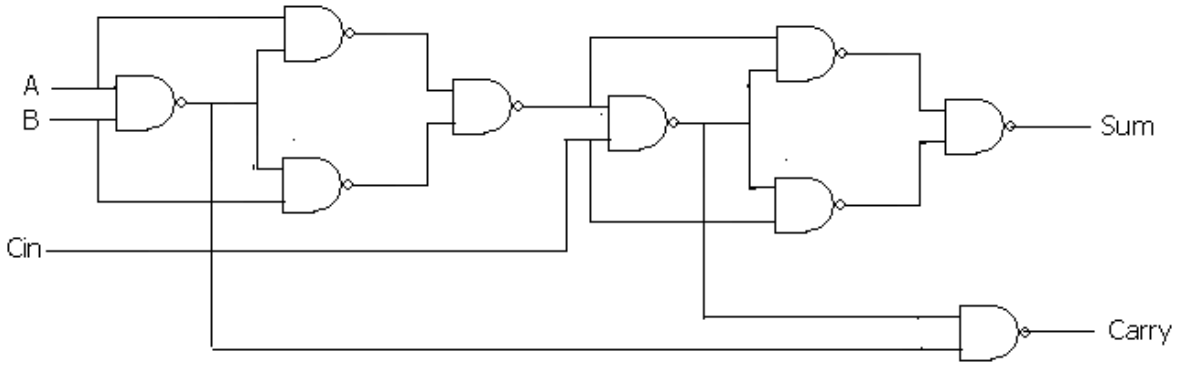
$= (\overline{A}\,\overline{B} + AB)Cin + (\overline{A}\,B + A\,\overline{B})\overline{Cin}$

$SUM = \overline{(A \oplus B)}Cin + (A \oplus B)Cin$ $\qquad carry = (A \oplus B)\,Cin + A\,B$

FULL ADDER USING BASIC GATES



FULL ADDER USING NAND GATES



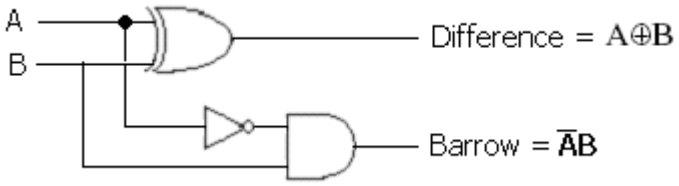
b) Verify the truth table for half subtractor and full subtractor circuits using basic and universal gates

i) HALF SUBTRACTOR

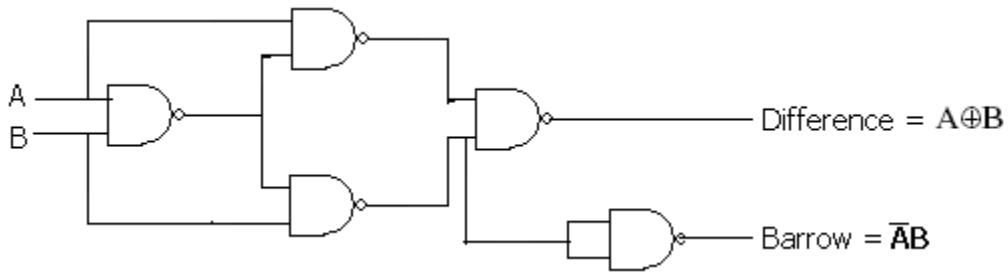
Truth Table

A	B	Diff	Barrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Half Subtractor Basic gates



Half Subtractor Using NAND gates



ii) FULL SUBTRACTOR:

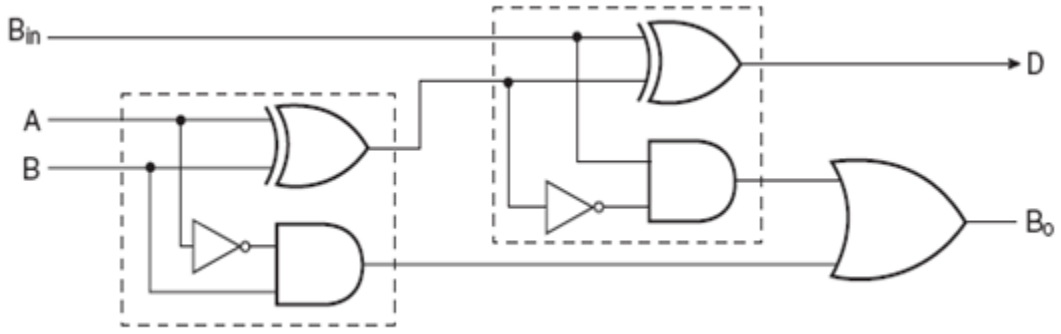
Truth Table

Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

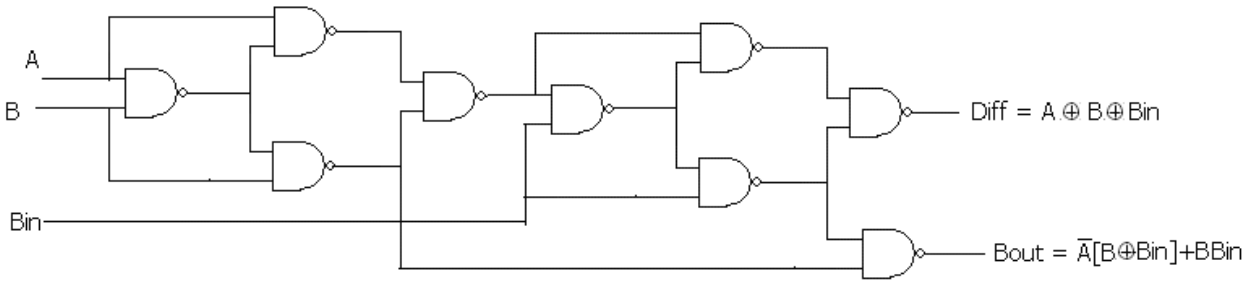
$$D = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B}_{in} + A.\overline{B}.\overline{B}_{in} + A.B.B_{in}$$

$$B_o = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B}_{in} + \overline{A}.B.B_{in} + A.B.B_{in}$$

Full Subtractor using Basic gates



Full Subtractor using NAND gates



PROCEDURE:

1. Place the IC in the socket of the trainer kit.
2. Make the connections as shown in the circuit diagram.
3. Apply diff combinations of i/ps according to the truth table and Verify the o/p.
4. Repeat the above procedure for all the circuit diagrams.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 3 Date:

Parallel Adder/Subtractor using IC 7483

AIM: i) Realization of Parallel adder/subtractor using 7483 chip.

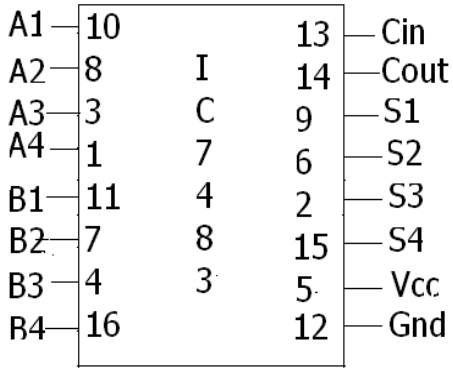
Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	EXOR gate	7486
2	Patch chords	
3	Trainer Kit	
4	4 bit parallel adder/subtractor	7483

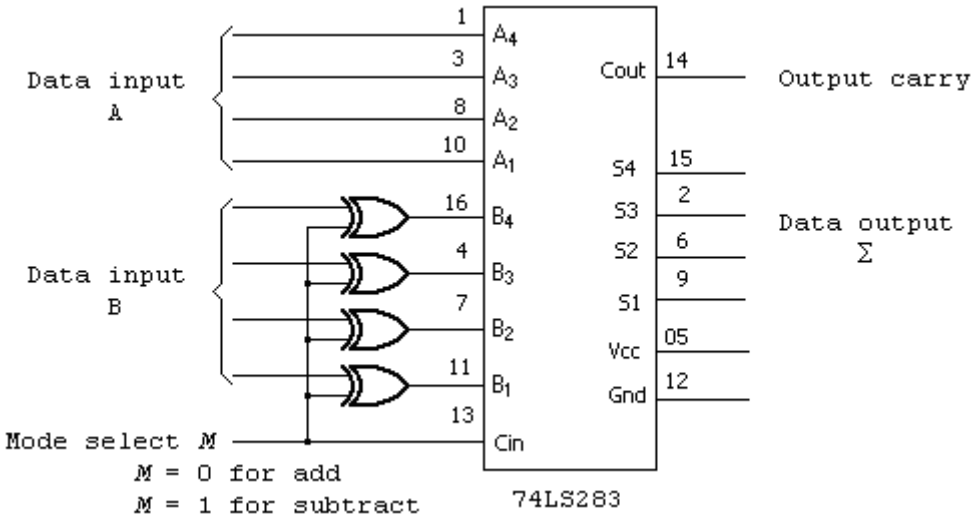
THEORY:

The IC 7483 is a 4- bit parallel adder IC that contains four inter connected FAs high speed operation.The inputs to this IC are two 4-bit numbers A3,A2,A1,A0 & B3,B2,B1,B0 and the carry Cin in to the LSB position.The outputs are the sum bits ∑3, ∑2,∑1,∑0. and the Cout of the b position.

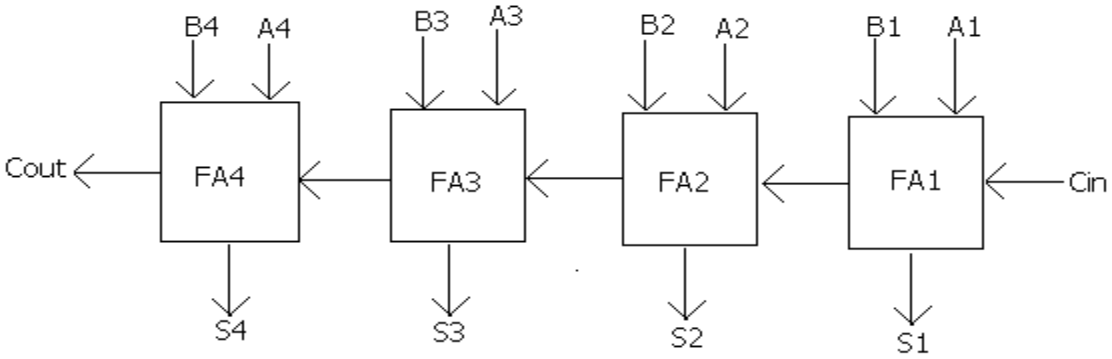
Pin diagram:



REALISATION of Parallel adder/subtractor using 7483chip



Block Diagram



Cin	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Cout	S_3	S_2	S_1	S_0

Procedure:

1. Make the connections as shown.
2. For addition, make Cin=0 and apply the 4 bits as i/p for A and apply another set of 4 bits to B. Observe the o/p at S_3, S_2 S_1 S_0 and carry generated at Cout. Repeat the above steps for different inputs and tabulate the result.
3. For subtration make Cin=1 and A-B format is used. By Xoring the i/p bits of 'B' by 1, complement of 'B' is obtained. Further Cin which is 1 is added to the LSB of the XORed bits. This generates 2's complement of B.
4. Verify the difference and polarity of differences at S0, S_1, S_2, and S3 and Cout. If Cout is 0, diff is –ve and diff is in 2's complement form. If Cout is 1, diff is +ve. Repeat the above steps for different inputs and tabulate the result.

(2) BCD to XS3 code conversion and vice versa

Truth Table

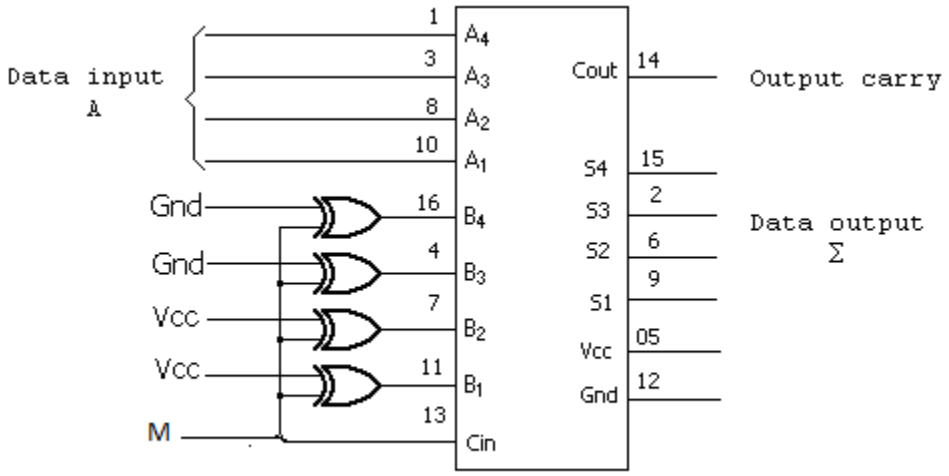
BCD to Ex-3

BCD				**XS3**			
B4	B3	B2	B1	X4	X3	X2	X1
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Ex-3 to BCD

XS3				BCD			
X4	X3	X2	X1	B4	B3	B2	B1
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	0	0	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Circuit Diagram



BCD to XS-3 code conversion and vice-versa can be implemented using IC 7483 along with 7486 Xor gates. The four i/p bits of 'B' ie B_3, B_2, B_1, B_0, are fixed as 0011. Cin =0, performs addition and Cin =1 performs subtraction.

- For BCD to xs –3 code conversion 3 has to be added to i/p bits of A therefore Cin =0.
- For Xs-3 to BCD code conversion '3' has to be subtarcated from the i/p of A therefore Cin =1.
- Verify the truth table.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 4 Date:

Realisation of Binary to Gray Code Conversion Vice & Versa

AIM: To Design and set up

(i) 4-bit Binary to Gray code converter circuit and
(ii) 4-bit Gray to binary code circuit using logic gates.

Components required:-

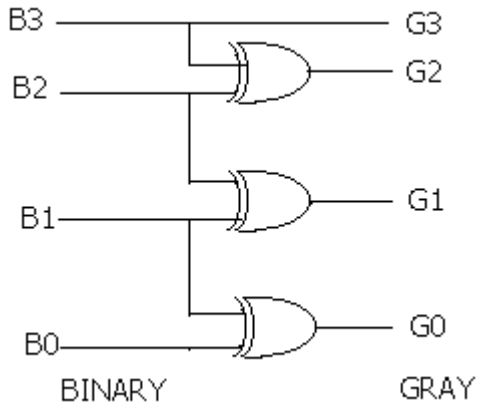
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	EXOR gate	7486
2	NAND gate	7400
3	Patch chords	
4	Trainer Kit	

Binary to Gray code converter

BINARY				GRAY CODE			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

- **Draw K-Map for each output and design the equations**.

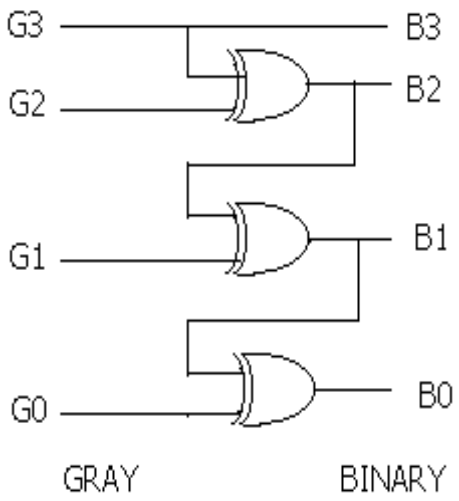
Using Xor Gates Only



Gray to Binary code converter

GRAY CODE				BINARY CODE			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

- **Draw K-Map for each output and write the equation**.



LOGIC DIAGRAM

PROCEDURE:

1. Place the IC in the socket of the trainer kit.
2. Make the connections as shown in the circuit diagram.
3. Apply diff combinations of i/ps according to the truth table and Verify the o/p.
4. Repeat the above procedure for all the circuit diagrams.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 5 Date:

Realisatiion of 1-Bit Comparator and Study of 7485 Magnitude Comparator

AIM:

To Realise 1-bit digital comparater & 2-bit digital compatater with the following outputs

(i) a > b
(ii) a = b
(iii) a < b

Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	AND gate	7408
2	OR gate	7432
3	Not gate	7404
4	EXOR gate	7486
5	Magnitude	
6	comparator	7485
7	Patch chords	
8	Trainer Kit	

THEORY:

A Magnatitude comparater is a combinational circuit that compares two numbers, A and B , and determines their relative magnitudes. The out come of the comparision is specified by three binary variables that indicates wheather

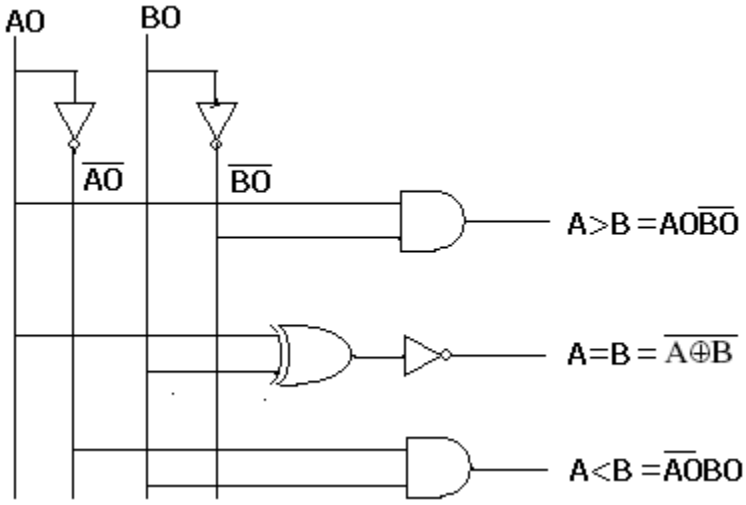
A > B
A = B
A < B

a) 1-Bit Comparator

TRUTH TABLE

A0	B0	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

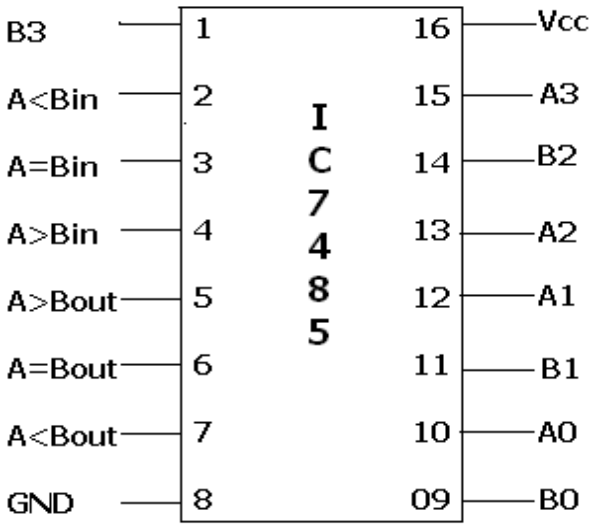
Logic Diagram Using Basic Gates



b) 4 Bit Magnitude Comparator

IC 7485: The IC 7485 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4 bit binary and producess three magnitude results.

IC 7485 PIN DETAILS

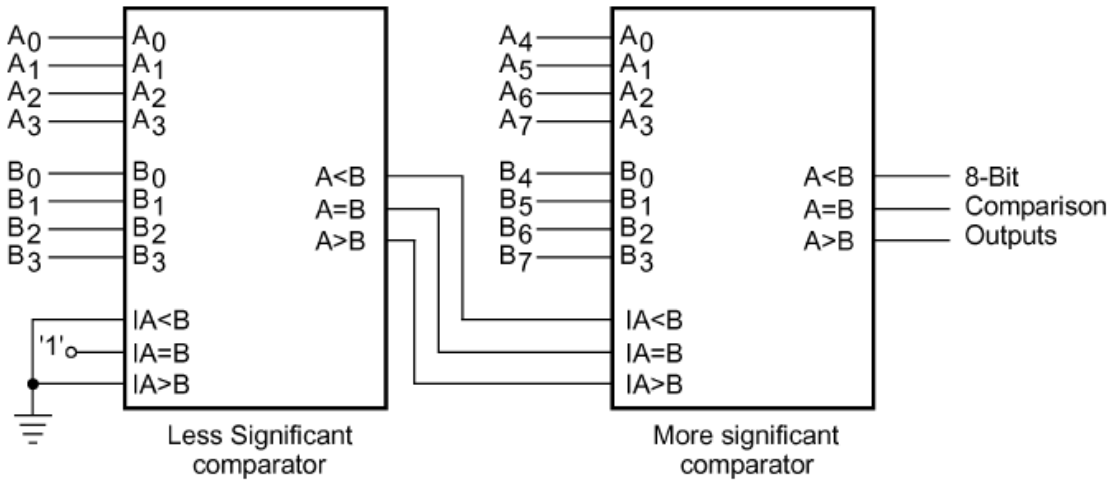


CASCADIG INPUTS				CASCADIG OUTPUT					
A3 B3	A2 B2	A1 B1	A0 B0	A>B	A=B	A<B	A>B	A=B	A<B
A3>B3	X	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	0	0	1
A3=B3	A2>B2	X	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	AO=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	AO=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	AO=B0	X	1	X	0	1	0
A3=B3	A2=B2	A1=B1	AO=B0	0	0	0	1	0	1
A3=B3	A2=B2	A1=B1	AO=B0	1	0	1	0	0	0

4 Bit Comparator Truth Table

A3	A2	A1	A0	B3	B2	B1	B0	A>B	A=B	A<B

- **Circuit Diagram for 8 Bit Comparator**



Procedure:

1) Rig up the circuit for one bit comparator as shown in the figure.
2) Verify the Truth Table of values. The output obtained should match the required result.
3) Using IC 7485 magnitude comparator Verify the truthtable for 4 Bit and 8 Bit.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 6 Date:

Study of MUX/DEMUX and Use of 74153, 74139 For Arithmetic Circuits.

AIM: To Realise 4:1 MUX using (i) NAND gates and (ii) IC 74153

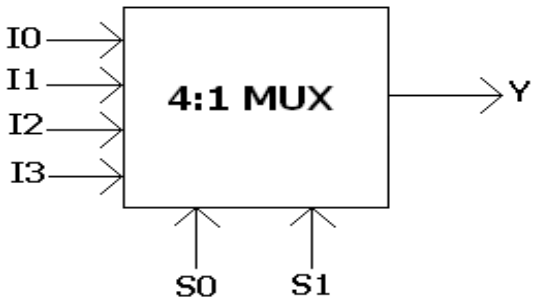
Components required :-

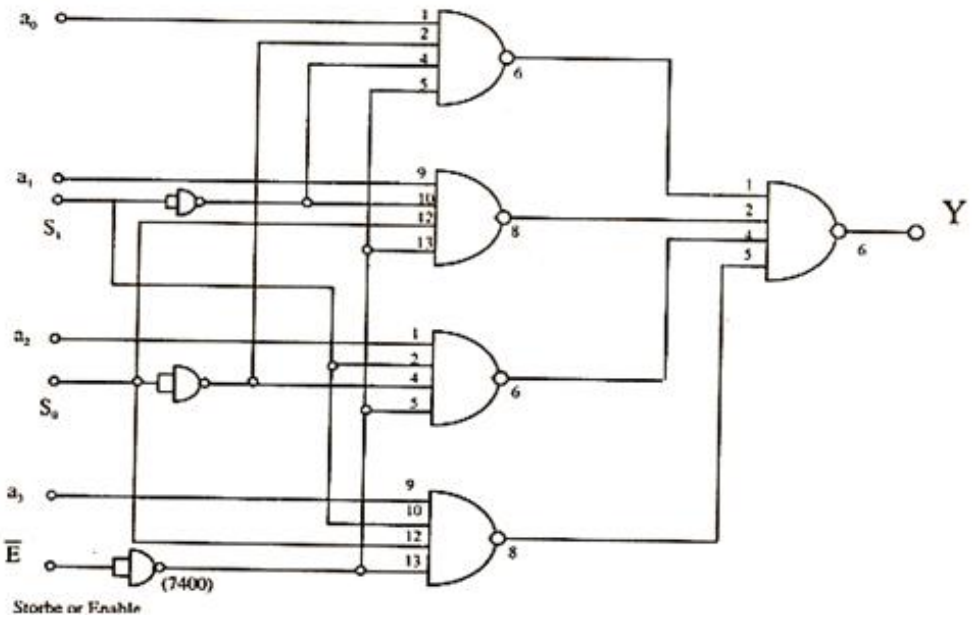
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	NANDgate(2	7400
2	pin)	
3	NANDgate(4	74153
4	pin)	74139
5	MUX	7404
6	DEMUX	
7	Not gate	
	Patch chords	
	Trainer Kit	

a) MUX

Truth table (4:1 MUX) SYMBOL

S1	S0	I0	I1	I2	I3	Y
0	0	I0	X	X	X	I0
0	1	X	I1	X	X	I1
1	0	X	X	I2	X	I2
1	1	X	X	X	I3	I3



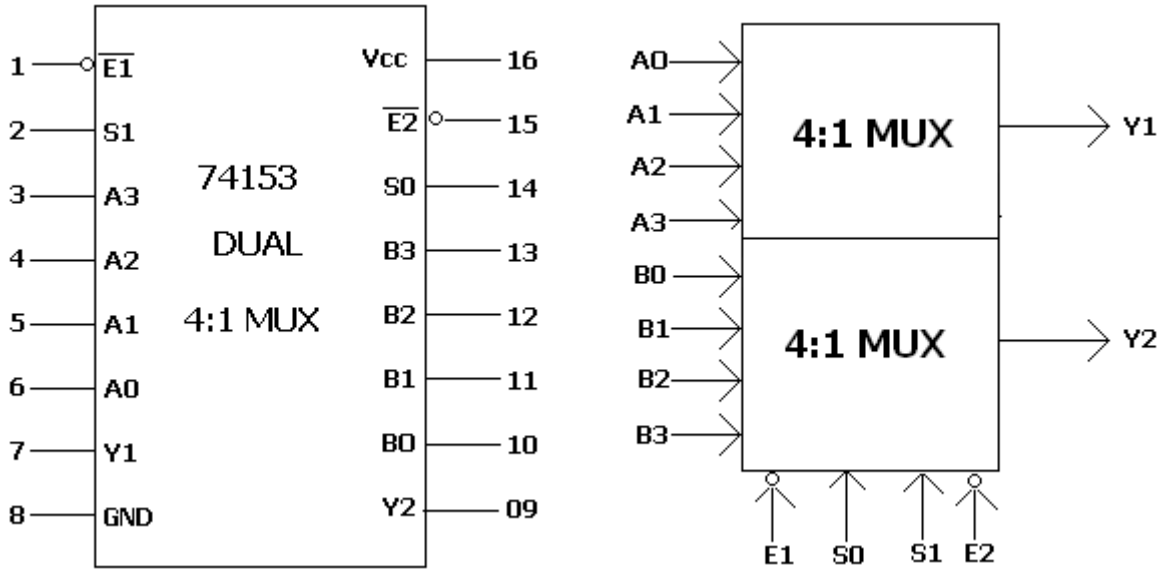


Enable input E	Select inputs S_1	S_0	Datainputs a_0	a_1	a_2	a_3	Output Y	Comments
0	0	0	0	X	X	X	0	'a_0' selected
	0	0	1	X	X	X	1	
	0	1	X	0	X	X	0	'a_1' selected
	0	1	X	1	X	X	1	
	1	0	X	X	0	X	0	'a_2' selected
	1	0	X	X	1	X	1	
	1	1	X	X	X	0	0	'a_3' selected
	1	1	X	X	X	1	1	

Procedure:

1. Set up the circuit as shown in figure
2. Verify the truth table of 4:1 MUX.

PIN DETAILS OF 74153



IC 74153 : the IC 74153 is a dual 4-i/p mux that can select 2 bits of data from up to eight sources under the control of the common select inputs (S0,S1). The two 4- i/p Mux circuits have individual active low enables (E1,E2) which can be used to strobe the outputs independently outputs (Y1,Y2) are forced low when the correspondinf enables (E1,E2) are high.

TRUTH TABLE FOR MUX 74153(DUAL 4:1 MUX)

E	S1	S0	Yn
1	X	X	0
0	0	0	An
0	0	1	Bn
0	1	0	Cn
0	1	1	Dn

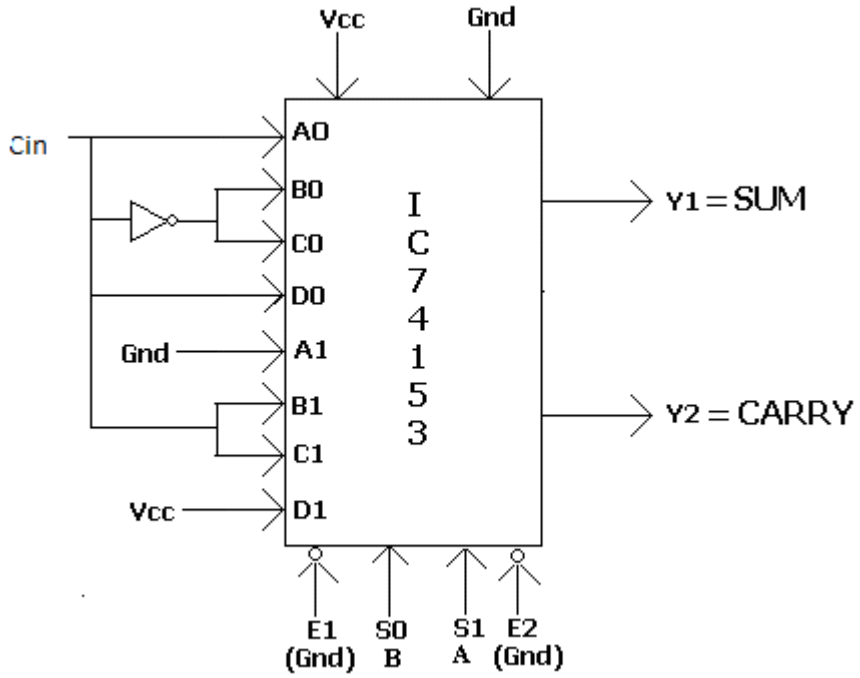
When E1 and E2 =1, device is not enabled and outputs are zero.

Realisation of Full Adder Using IC 74153

Here the outputs sum and carry out are represented in Terms of input cin

A	B	SUM	Cout
0	0	Cin	0
0	1	$\overline{Cin}$	Cin
1	0	$\overline{Cin}$	Cin
1	1	Cin	1

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



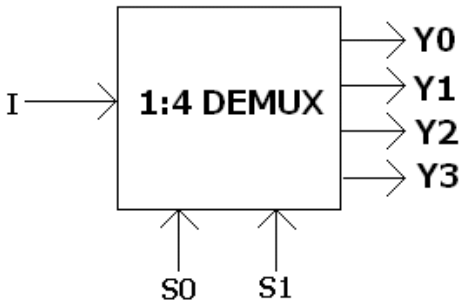
- **Realise Full-Subtractor using IC 74153.**

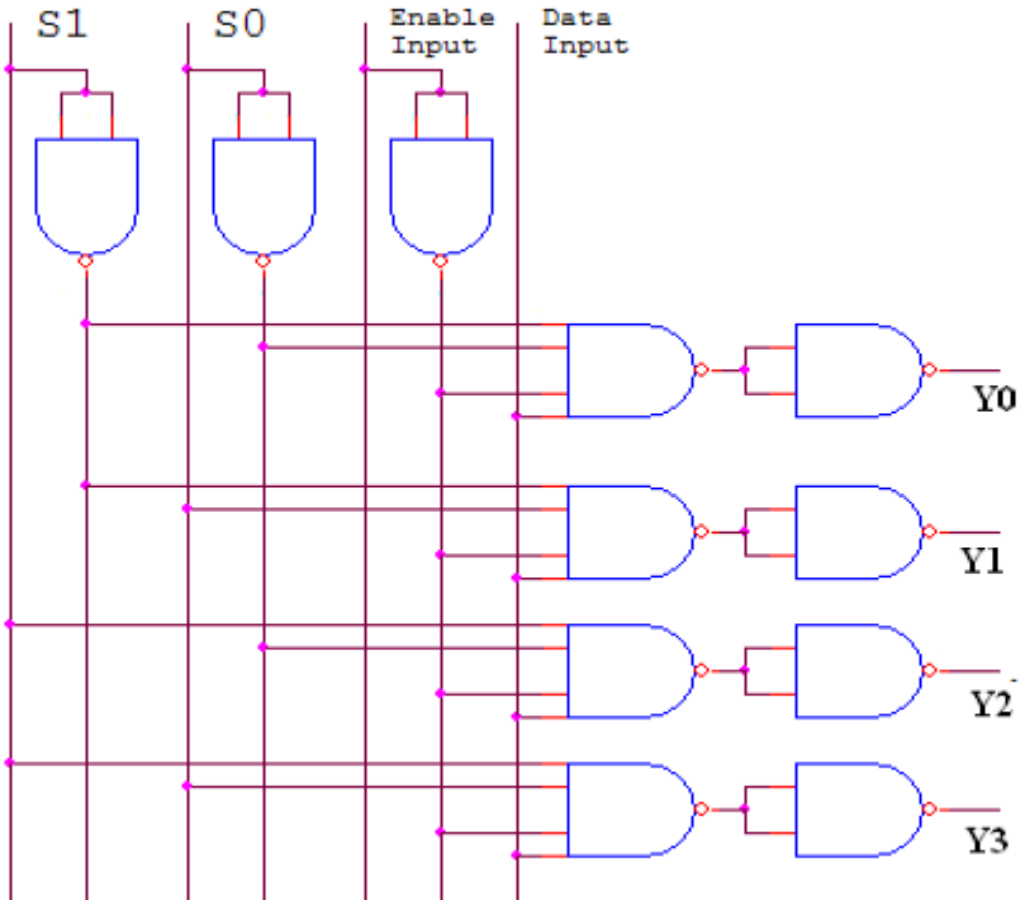
b) DEMULTIPLEXER

FUNCTIONAL TABLE

S1	S0	Ii	Y0	Y1	Y2	Y3
0	0	I	I	0	0	0
0	1	I	0	I	0	0
1	0	I	0	0	I	0
1	1	I	0	0	0	I

SYMBOL

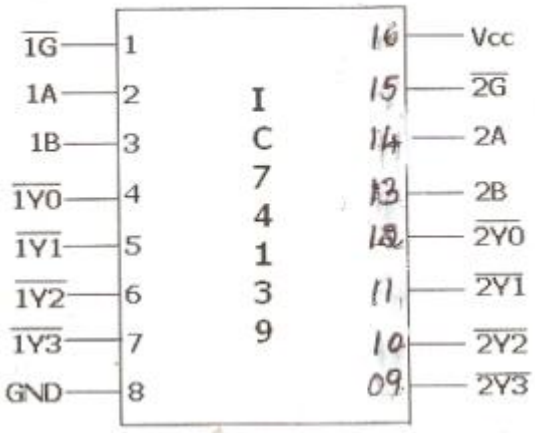




IC74139 DEMUX/ FUNCTIONAL TABLE

$\overline{1G}$	B(S1)	A(S0)	Y3	Y2	Y1	Y0
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

IC 74139 DEMUX/ DECODER



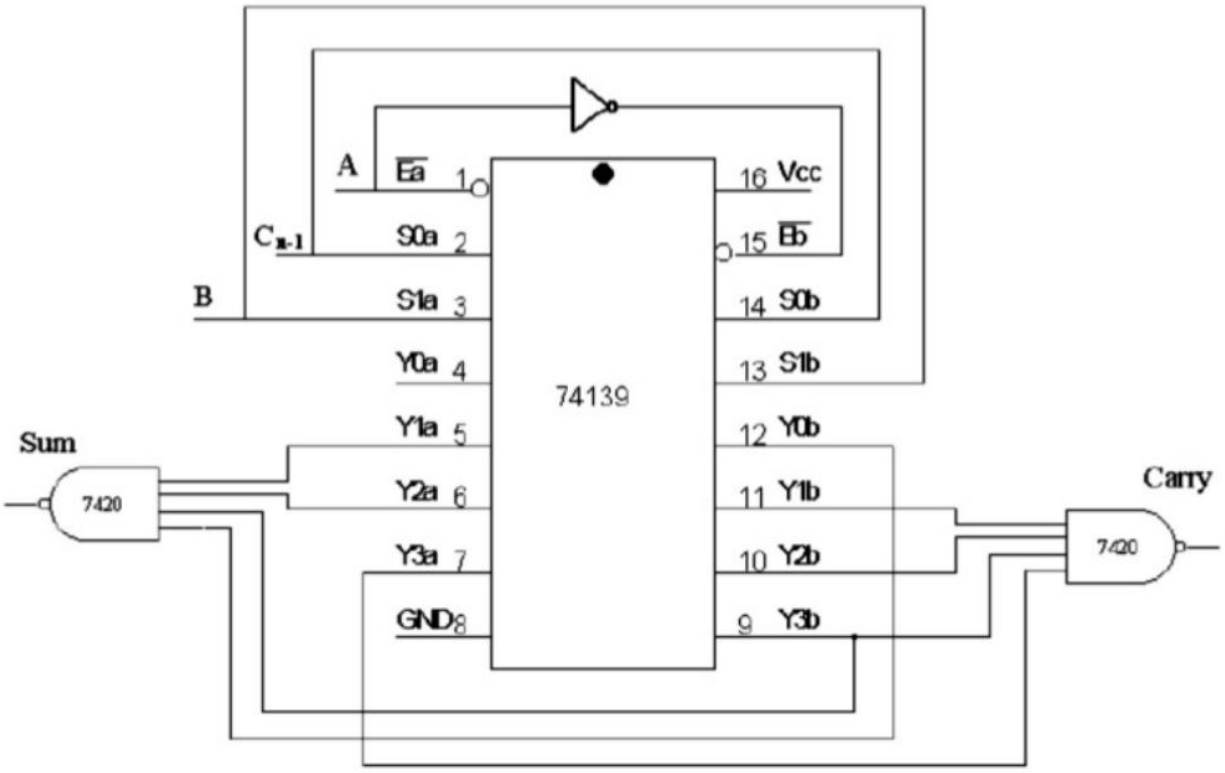
IC 74139: The ic 74139 is a high speed dual 1 of 4 decoder/ demultiplexer. this device has two independent decoders each accepting two binary weighted inputs (a, b) and providing four mutually exclusive active low o/ps(Y0-Y3).each decoder has an active low enable (E) when E=1 every o/p is forced high. The enable can be uysed as the data input for a 1 of 4 DEMUX application

- **FULL ADDER using IC 74139**

TRUTH TABLE

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum =∑1,2,4,7
Carry =∑3,5,6,7



- **Realise Full-Subtractor using IC 74139.**

Procedure:

1) Rig up the circuit using NAND gates and then with IC74139 and 74153 as shown in figure.
2) Verify the output with the truth table Values.
3) The output obtained practically should match the required result.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 7 Date:

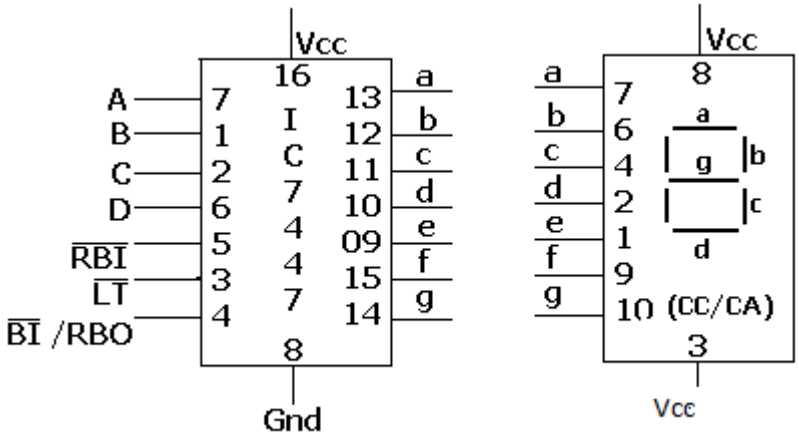
LED Display and Priority Encoder

AIM : Use of
(a) Decoder Chip to Drive Led
(b) Priority Encoder

Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	LED(CA)	7447
2	LED(CC)	7448
3	LCD	7448
4	Priority	74147
5	Encoder	
6	Patch chords	
	Trainer Kit	

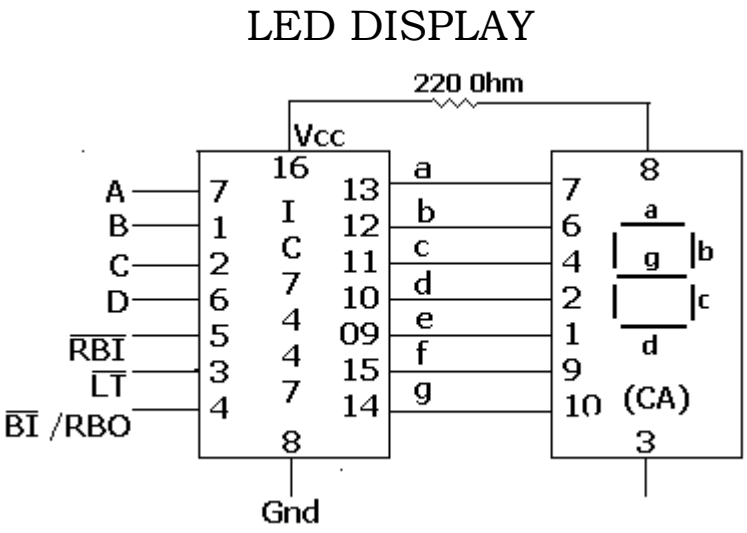
PIN DAIGRAM OF IC7447/8 AND LED(CC/CA)



TRUTH TABLE

INPUTS D C B A	OUTPUTS (7 SEG LED DISP)
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9

CIRCUIT DIAGRAM



Procedure:

1) Set up the circuit as shown in figure.
2) Apply logic '0' to LT (pin 3) and observe the seven segments of the LED. All the segments must be ON.
3) Apply logic '1' to LT (pin 3) and logic '0' to RBI(pin 5) and BI/RBO (pin 4) and observe the BI/RBO output and the numver displayed on the LED for all the inputs 0000 through. This is the normal decodeing mode with zero blinking

PRIORITY ENCODER

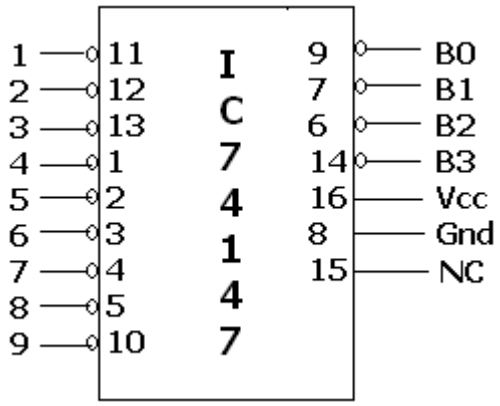
A priority Encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time the input having the highest priority will takes precedence.

(1) To convert decimal to BCD using IC 74147

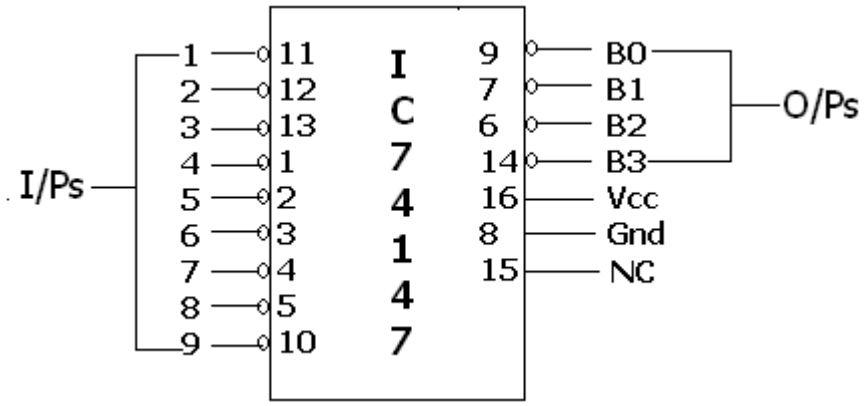
TRUTH TABLE

1	2	3	4	5	6	7	8	9	B3	B2	B1	B0
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
X	0	1	1	1	1	1	1	1	1	1	0	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	X	X	0	0	1	1	0

PIN DIAGRAM



CIRCUIT DIAGRAM



Procedure:

1. Rig up the ckt as shown in the figure.
2. Apply logic zero to LT signal and observe 7 segments of LED i.e all the lines must be ON.
3. Apply zero to blank i/p of BI and observe all the lines to be off.
4. Aplly logic 1 to LT and RBI and observe the number displayed on LED/LCD versus i/p combinations 0000 to 1001 , this is normal decoding mode.
5. Apply logic 1 to LT and Zero to RBI and observe RBO o/p and number displayed on LED/LCD versus i/p combinations . This is normal decoding mode with zero blanking.Verify the truth table.

Observation:-

LT =0, all the segment are ON

$\overline{BI}$ and $\overline{RBI}$=1

LT=0/1 , $\overline{BI}$=0 $\overline{RBI}$=1 all the segments are OFF

LT=1 , $\overline{RBI}$=0 , RBO to Output.

Zero is not displayed

PROCEDURE:

1. Place the IC in the socket of the trainer kit.
2. Make the connections as shown in the circuit diagram.
3. Apply diff combinations of i/ps according to the truth table and Verify the o/p.
4. Repeat the above procedure for all the circuit diagrams.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 8 Date:

Flip-Flops

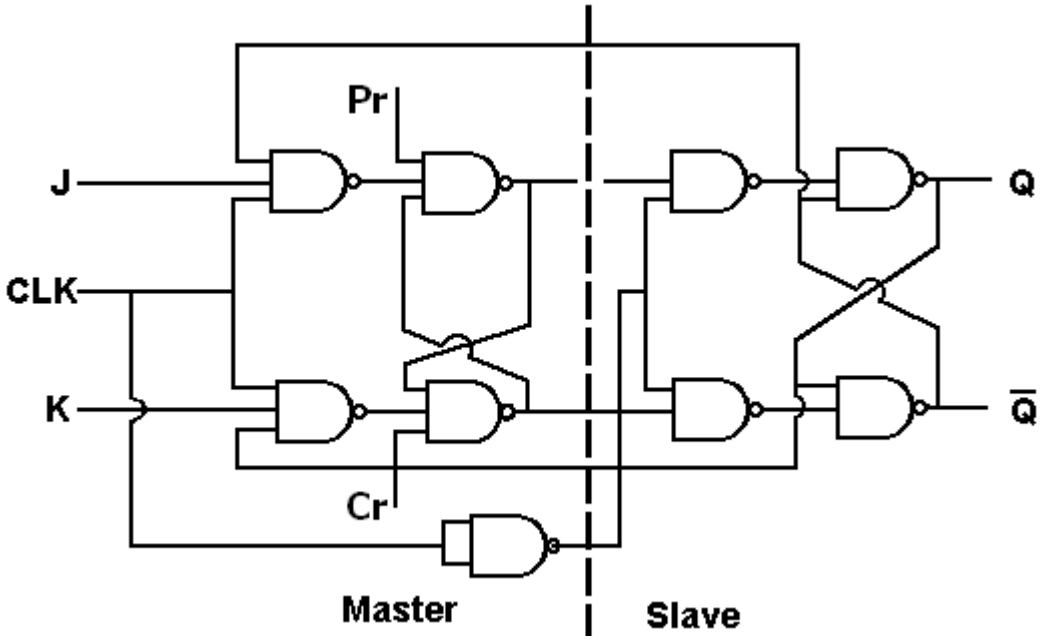
AIM:- Truth Table verification of flipflops:

(i) JK Master slave
(ii) T type
(iii) D –type.

Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	Dual J.K	7476
2	FlipFlop	7400
3	NAND gate	7404
4	NOT gate	
5	Patch chords	
	Trainer Kit	

THEORY: The flip-flops can be mode to respond to trailing edge of a pluse by employing two flip-flop circuits, one to hold the output state on the trailing edge and the other to sample the i/p information on the leading edge. Such a combination is called a master- slave flip-flop. The MS combination can be constructed for any type of FF. In case of JK MS FF the information present at the J and K inputs is transmitted to the master FF on the leading edge of the clk pluse and held there until the trailing edge of clock pluse occurs offer which if is allowd to pass through to the slave FF.



TRUTH TABLE

Table 1

Inputs Clk	Cr	pr	Output Q	Operation Performed
1	1	1	Qn+1	Normal FF(Table-2) (F.F. enabled)
0	0	1	0	F.F. Cleared(Reset)
0	1	0	1	F.F. Preset(Set)

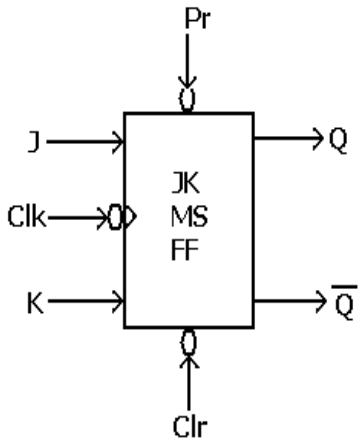
Note: - Keep Pr= Cr=1 for verifying the truth tables JK MS F.F, T and D type FF.

Procedure:

1)Rig up the circuit as shown in the diagarm.

2)Apply the i/ps to these flipflops as per the Truth table and observe the o/p Verify with the truth table.

SYMBOL OF MS-JK FF



PIN DIAGRAM

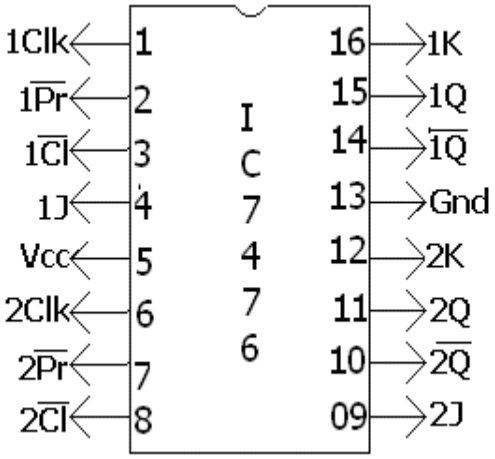
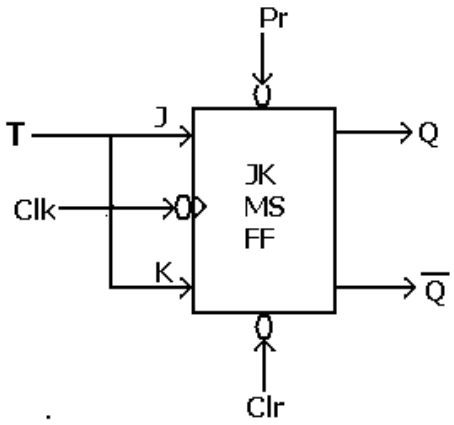


Table 2

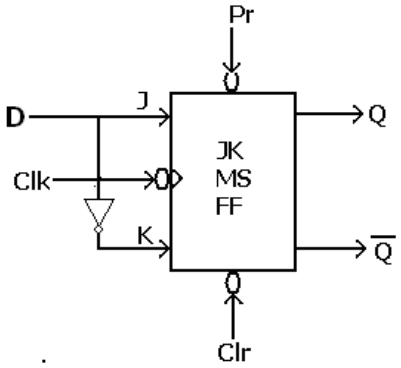
Clk	Inputs J	K	Output Qn+1	COMMENTS
⎍↓	X	X	Qn	No Change
⎍↓	0	0	Qn	No change
⎍↓	0	1	0	Reset
⎍↓	1	0	Qn	Set
⎍↓	1	1	$\overline{Qn}$	F.F. Preset(Set)

T- Type FF using MS JK FF



Inputs CLK	Tn	Output Qn+1	Comments
0	X	Qn	No change
↓	0	Qn	No change
↓	1	$\overline{Qn}$	Toggles

D - Type FF using MS JK FF



Inputs CLK	Dn	Output Qn+1	Comments
0	X	Qn	No change
↓	0	0	Data tarnsfered
↓	1	1	Data tarnsfered

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 9 Date:

COUNTERS

AIM -Realization of 3-bit counters as a sequential circuit and mod-N counter design using 7476, 7490, 74192, 74193.

Components required :-

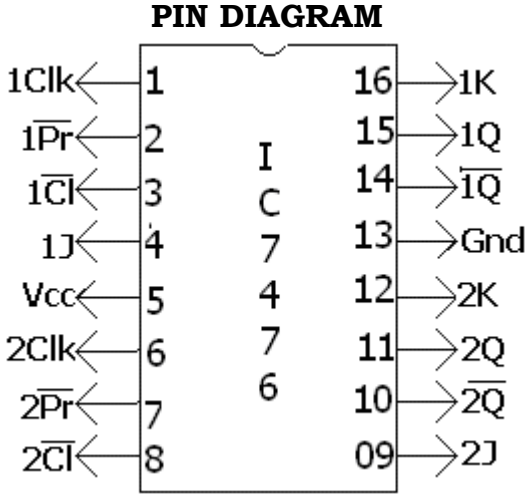
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	JK flip flop	7476
2	NAND gate	7400
3	AND gate	7408
4	OR gate	7432
5	Decade Counter	7490
6	Decade Up/down Counter	74192
	MOD 16 counter	74193
	Patch chords	
	Trainer Kit	

ASYNCRONOUS COUNTERS

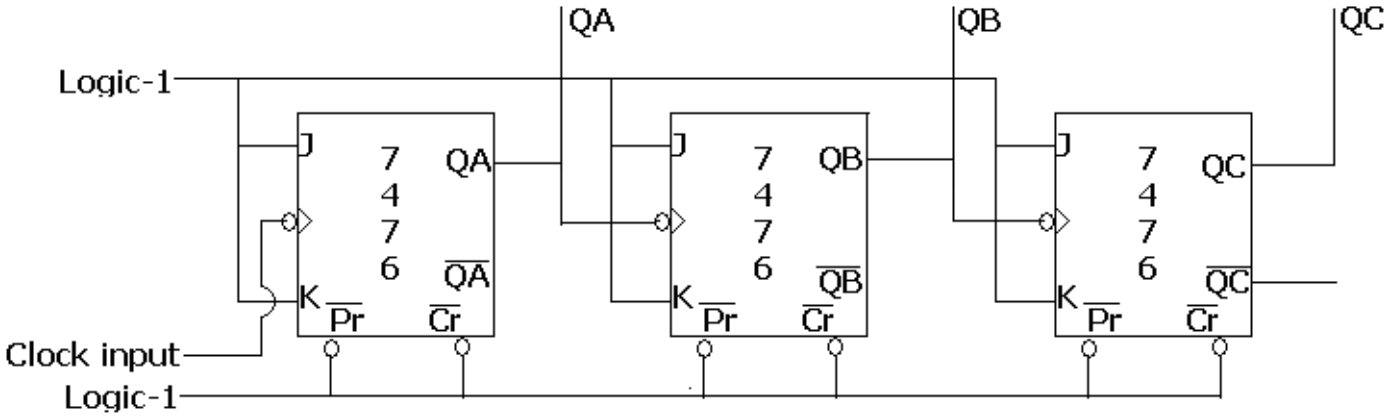
A binary ripple (Asynchrounous) counter consists of a series connections of T- flip-flops without any logic gates. Each FF is triggered by the output of it's preceding FF goes from 1 to 0.

Realization of 3-bit binary counters using IC7476

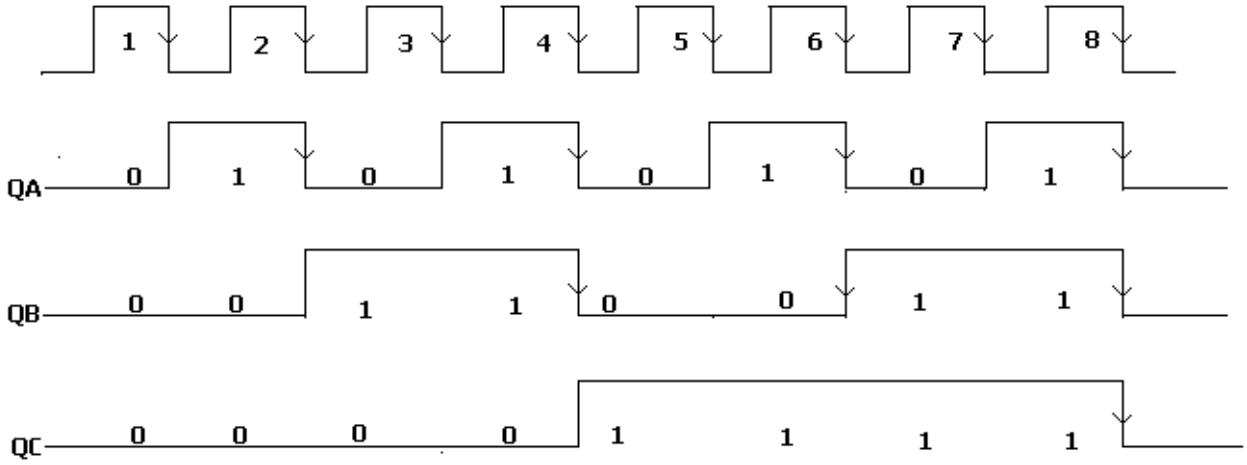
PIN DIAGRAM



Aynchrounous UP Counter (MOD-8)



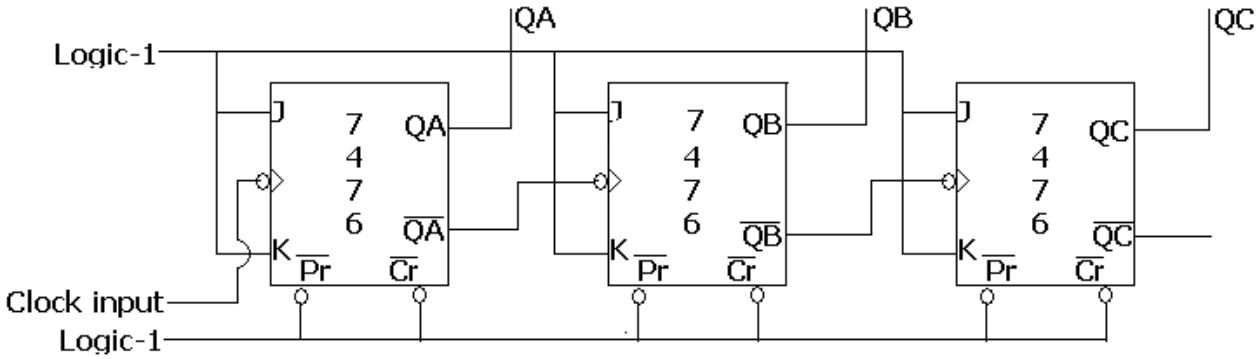
WAVE FORMS



TRUTH TABLE

Number of clock pulses	Flip Flop outputs Qc	Qb	Qa
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

3 Bit Asynchrounous DOWN Counter



TRUTH TABLE

Number of clock pulses	Flip Flop outputs Qc	Qb	Qa
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1

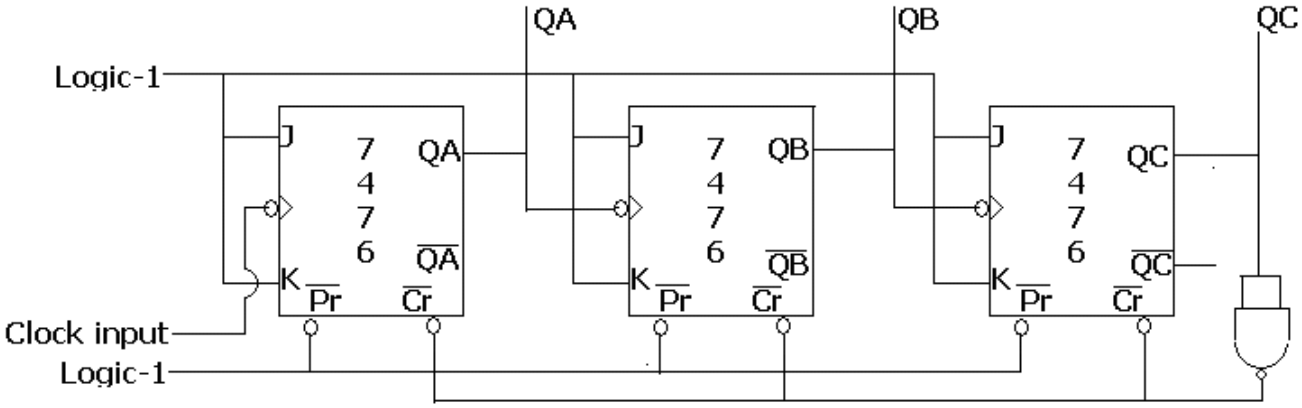
Asynchrounous MOD-N Counter (UP Counter)

MOD-4 COUNTER

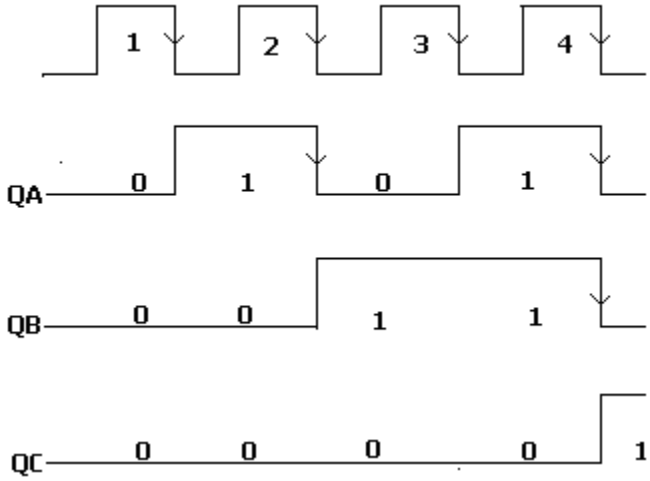
In MOD-4 counter 1 0 0 (Qa, Qb, Qc) is Invalid state

TRUTH TABLE

Number of clock pulses	Flip Flop outputs Qc	Qb	Qa
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1



WAVE FORMS

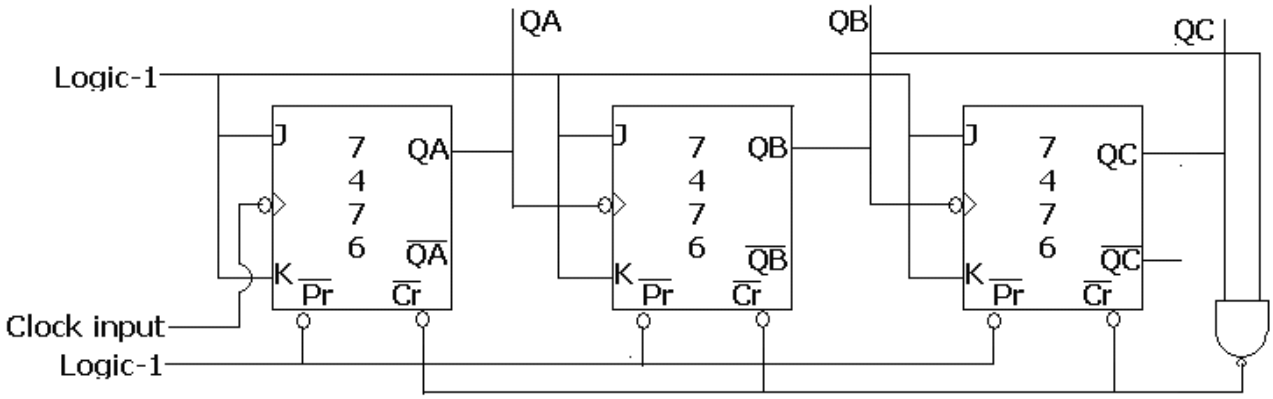


MOD-6 COUNTER

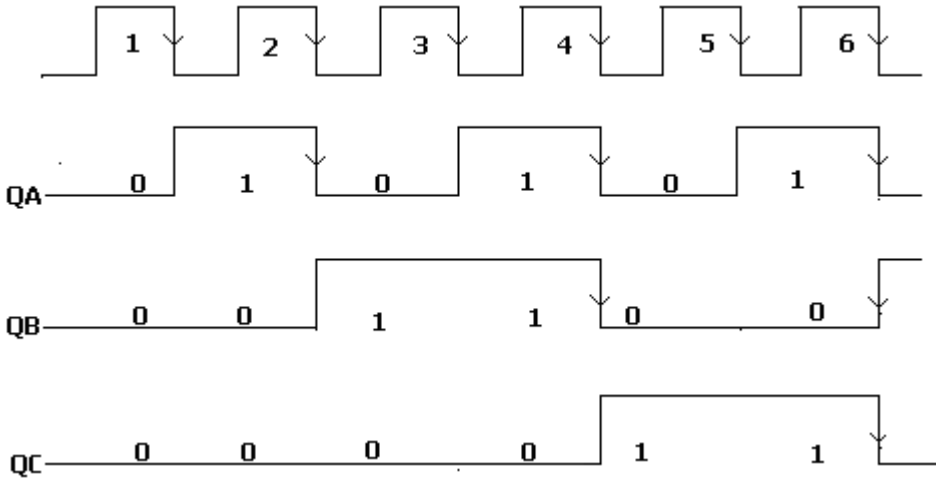
TRUTH TABLE

In MOD-6 counter 1 1 0 (Q_C, Qb, Qa) invalid state

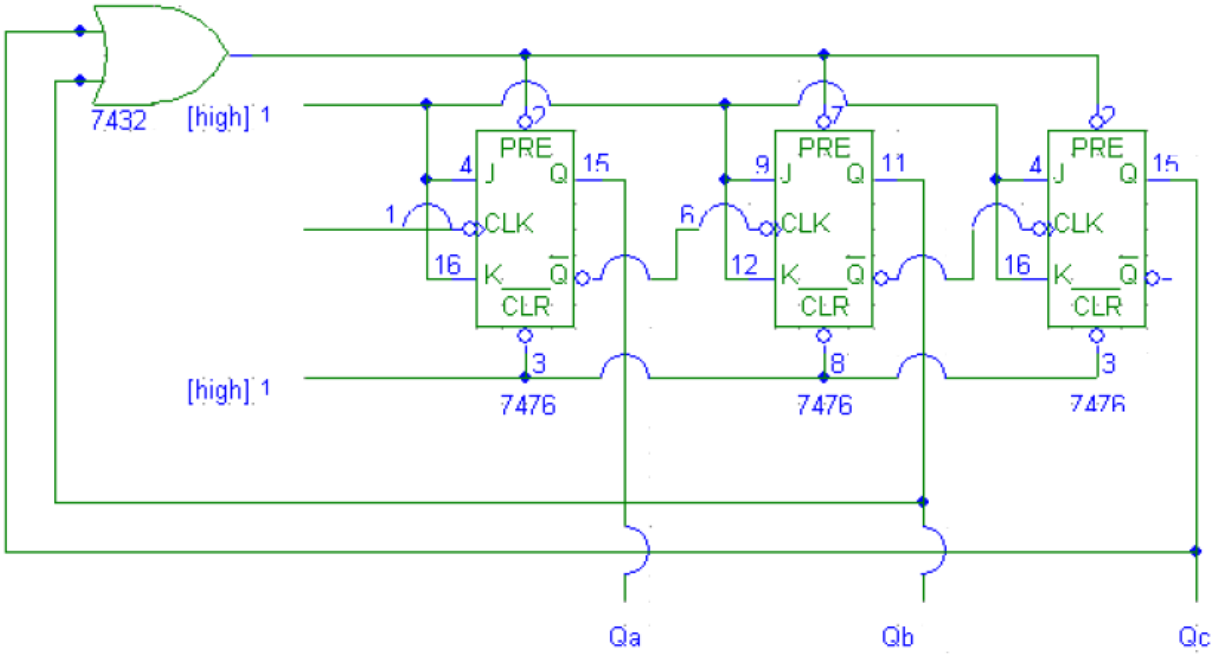
Number of clock pulses	Flip Flop outputs Qc	Qb	Qa
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	0	0	0



WAVE FORMS



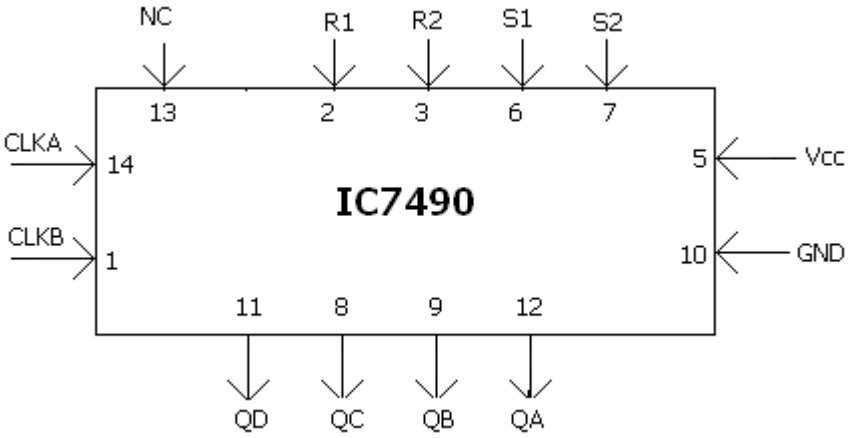
Asynchrounous MOD-6 Down Counter



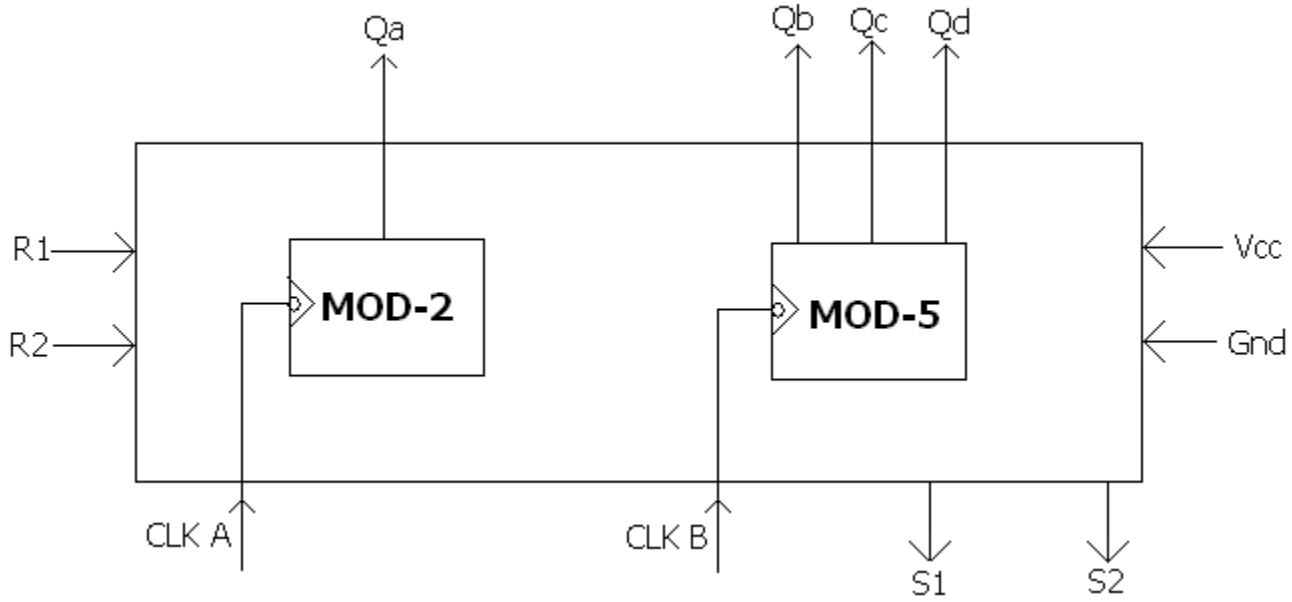
MOD-N COUNTERS

To realize a MOD-N counter using IC-7490

Pin Diagram



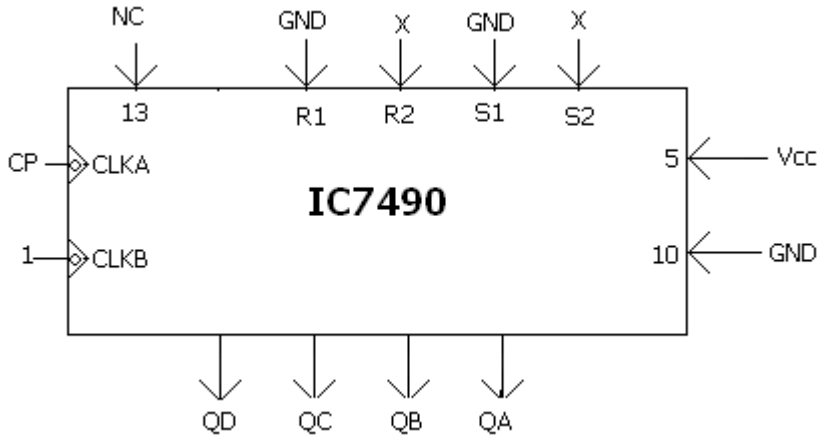
Internal Diagram



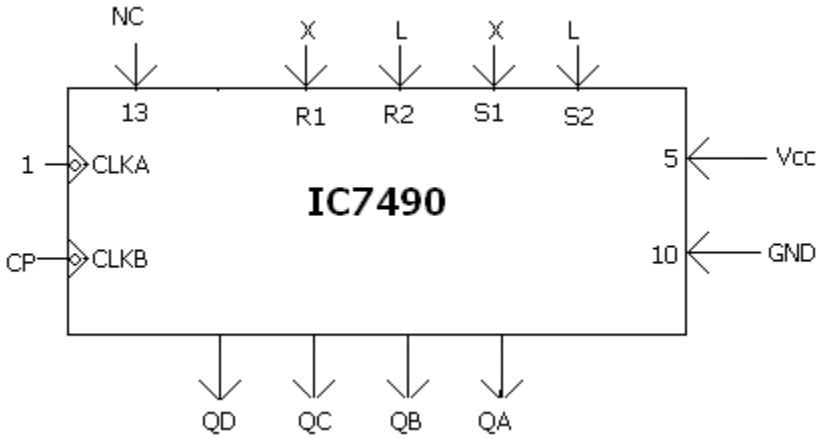
Conditional Table

R1	R2	S1	S2	Qa	Qb	Qc	Qd
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	L	H	H	1	0	•	1
L	X	L	X	MOD-2 COUNTER			
X	L	X	L	MOD-5 COUNTER			

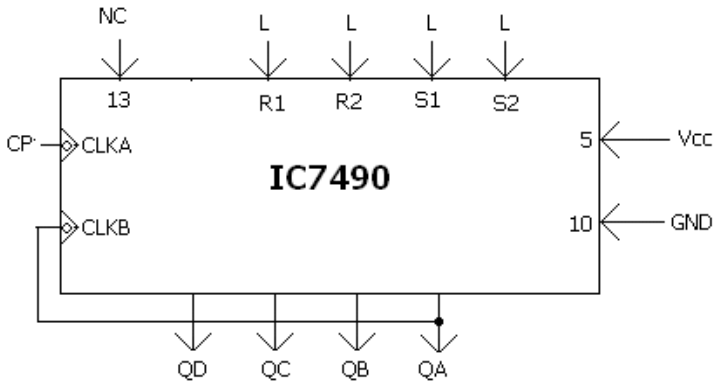
7490 As Mod-2 Counter



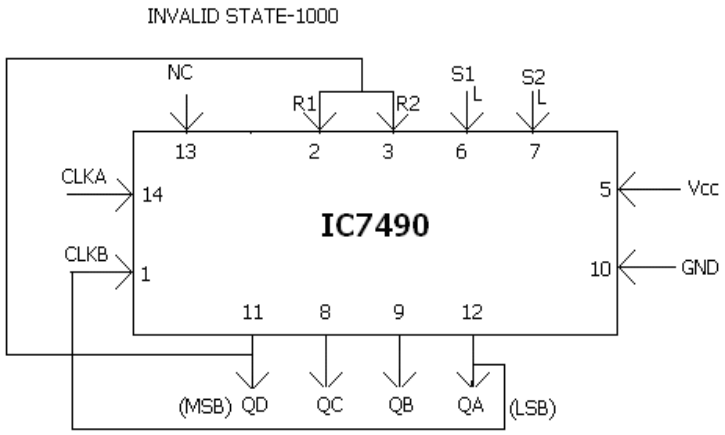
7490 As Mod-5 Counter



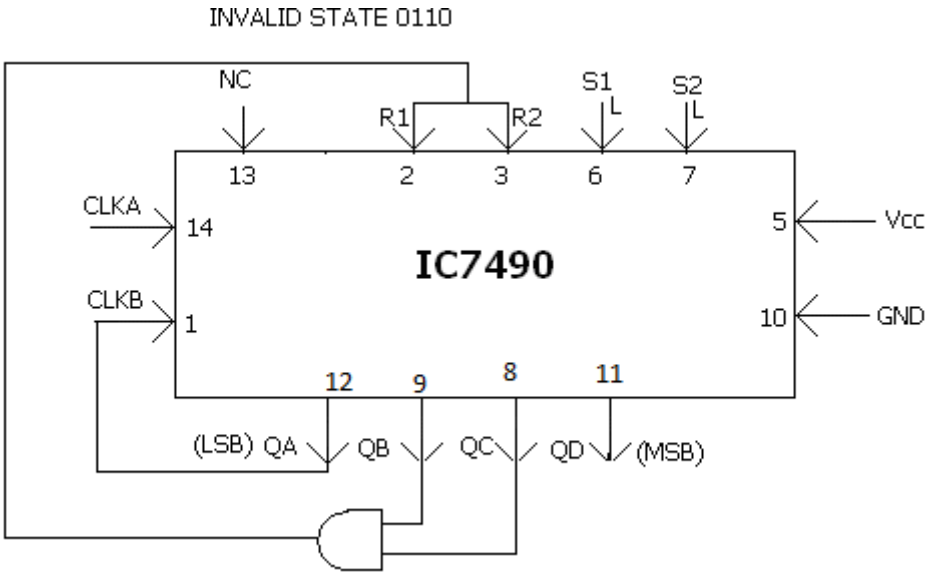
7490 As Mod-10 Counter



7490 As Mod-8 Counter



7490 As Mod-6 Counter

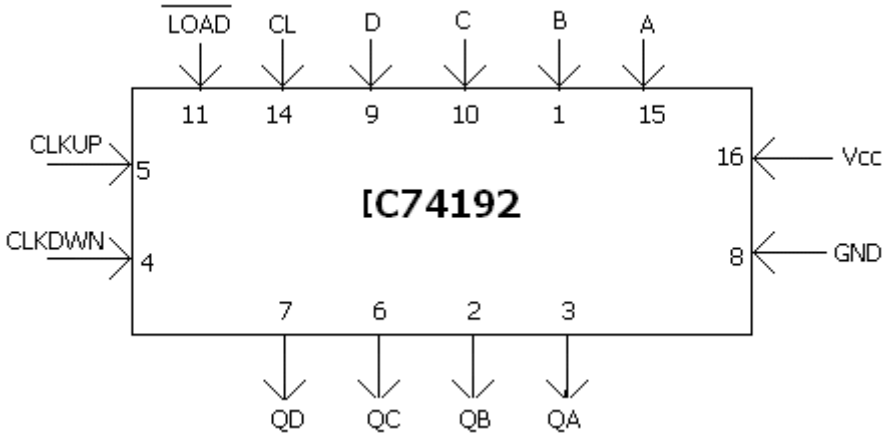


To realize a MOD-N counter using IC74192

To realize a MOD-N counter using IC74192 with given preset value, write down the expected function table

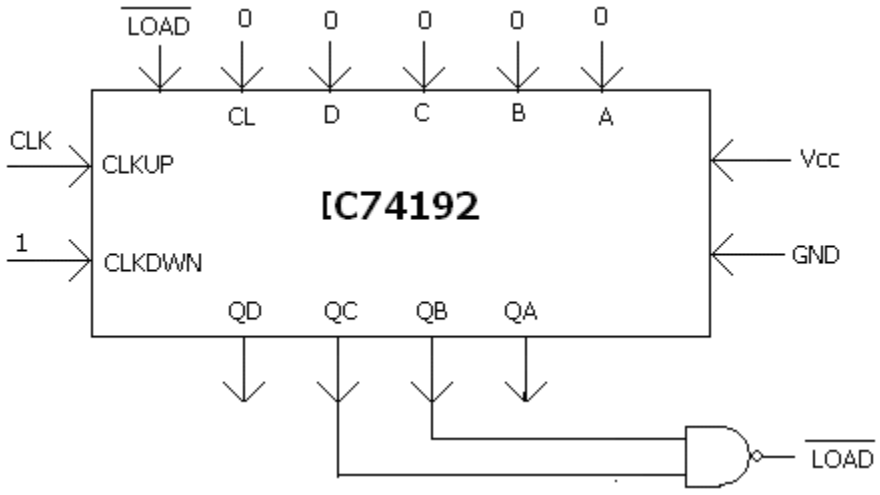
Synchronous Counter

PIN DETAILS OF IC-74192[MOD-10 UP/DOWN COUNTER]

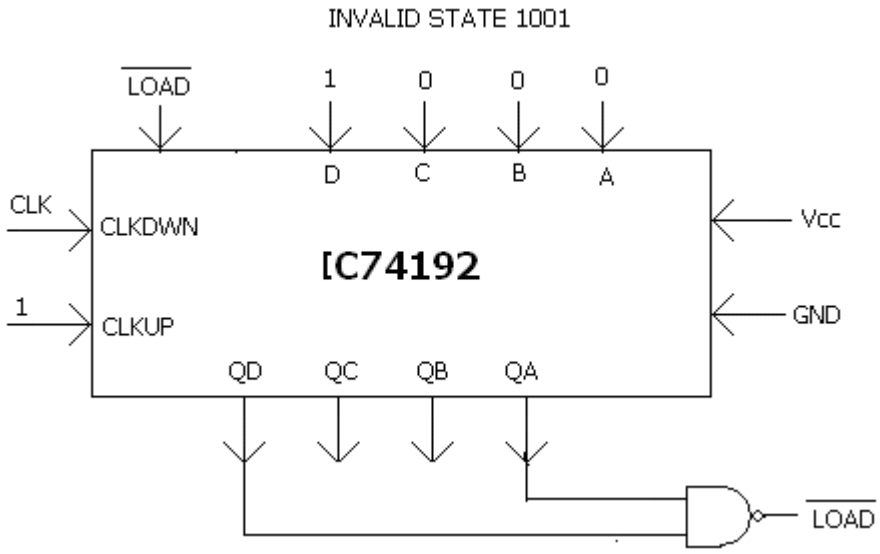


Mod-6 Up Counter

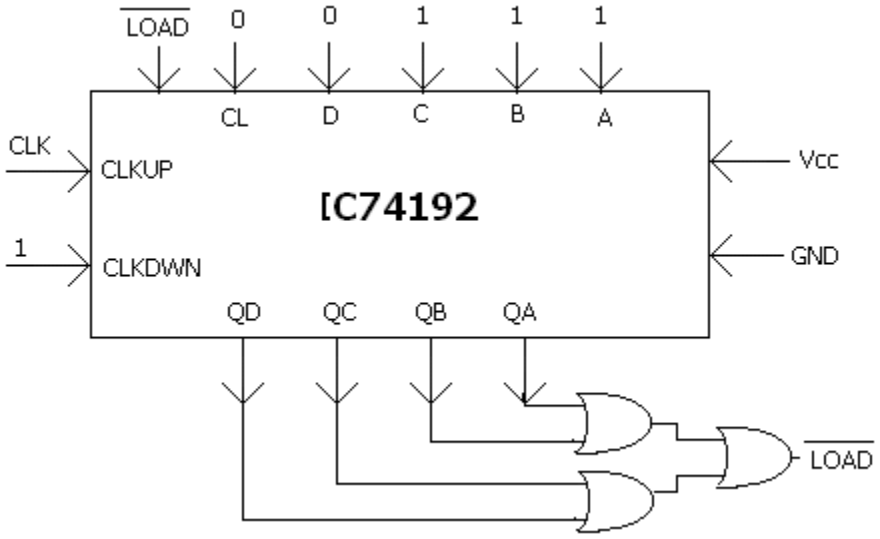
Invalid state-0110



Mod-9 Down Counter



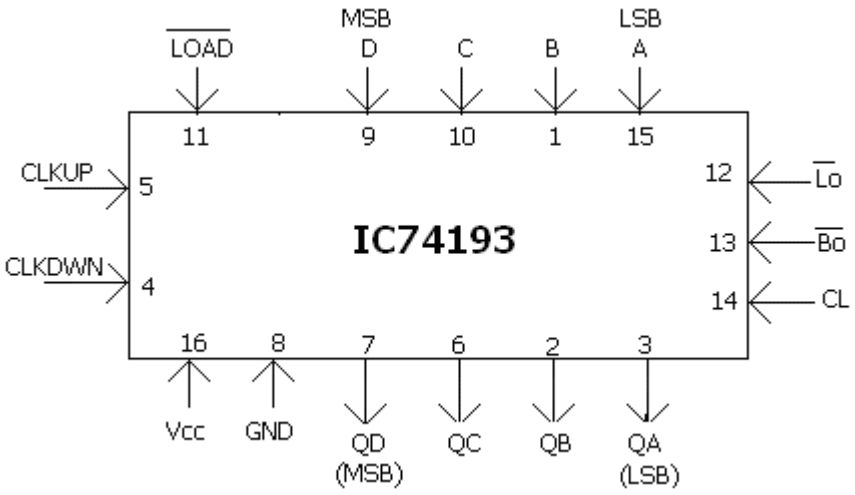
Design A Counter Which Can Count From 7 To 9



NOTE After 1001, out put becomes 0000

To realize a MOD-N counter using IC-74193 with a given preset value, write down the expected function table.

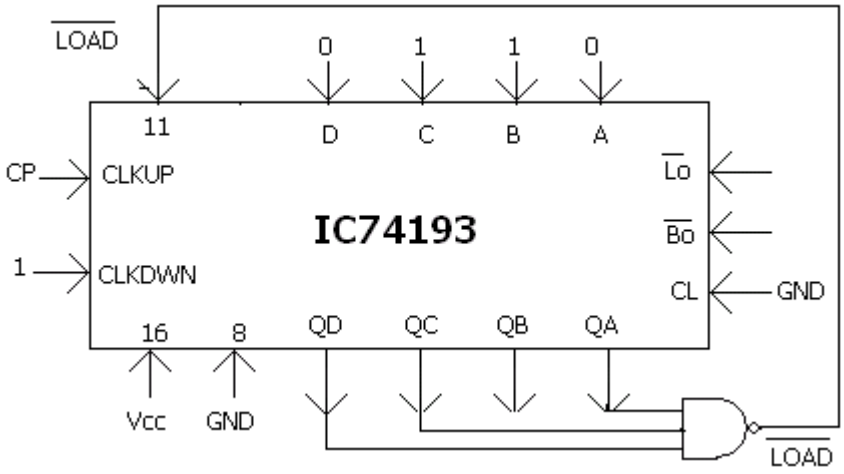
Pin details of IC 74193(Synchronous counter)
[MOD-16 UP/DOWN COUNTER]



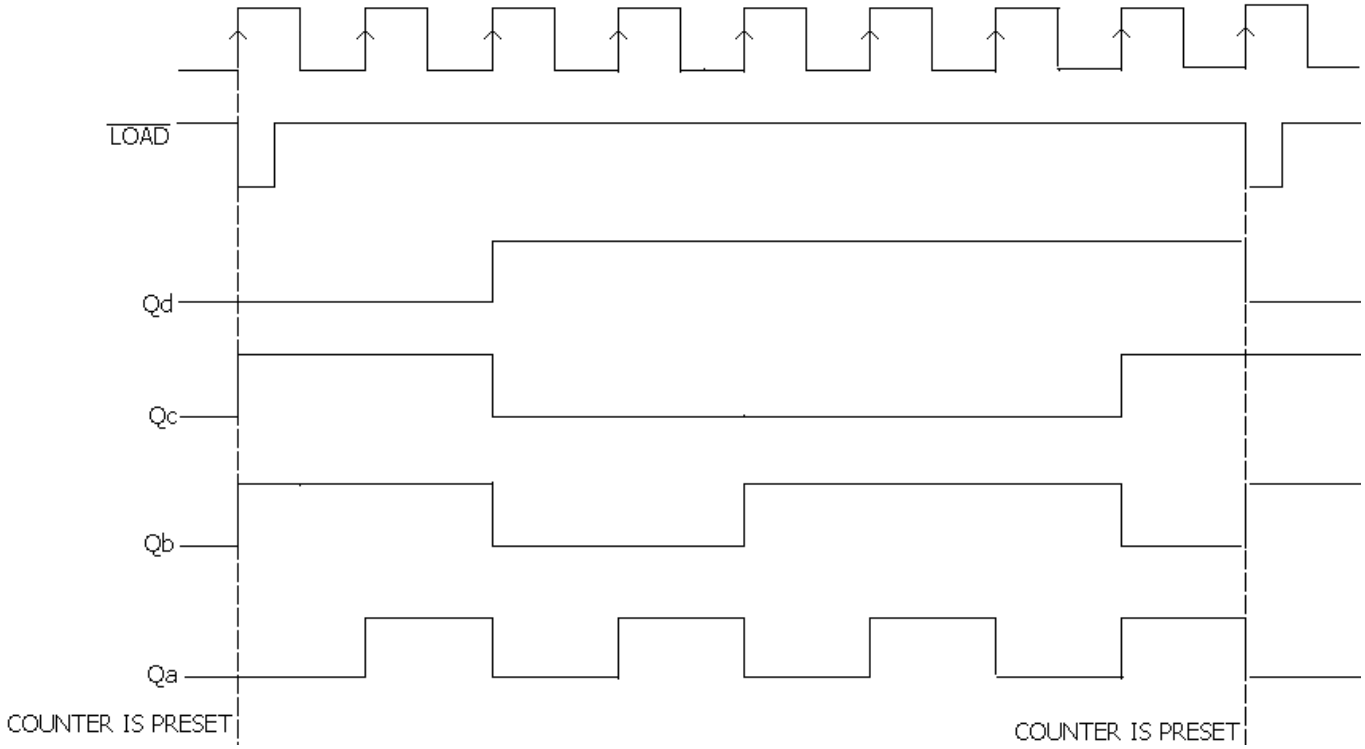
FUNCTION TABLE

$\overline{Clr}$	Load	Up	Down	Qd	Qc	Qb	Qa
H	X	X	X	0	0	0	0
L	L	X	X	D	C	B	A
L	H	Cp	H	COUNT UP			
L	H	H	Cp	COUNT DOWN			
L	H	H	H	NO CHANGE			

Design a counter which counts from (6-12)

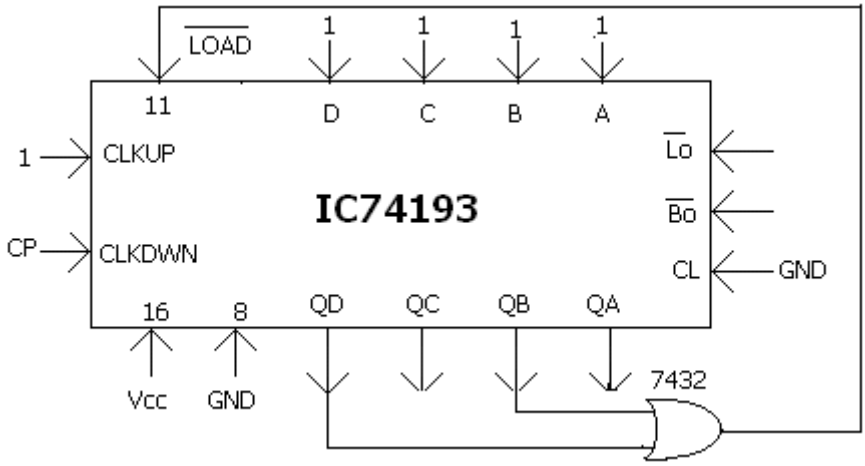


Invalid state 1101



WAVE FORMS

Realize A (15-6) Counter Using Ic 74193



Invalid state---0101
Note:-Lo and Bo are used basically for cascading the counters

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No:10 Date:

SHIFT REGISTERS

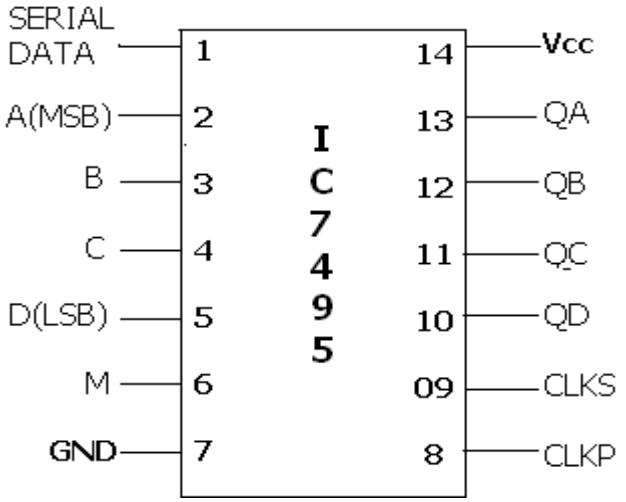
Aim- To demonstrate Shift lift shift right, SIPO, SISO, PISO, PIPO operations using IC 7495

Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1 2	Shift register Trainer kit Patch Chords	7495

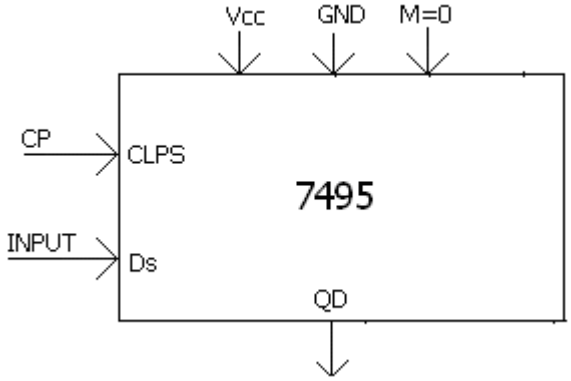
The IC 7495 is a 4-bit shift register ,allowing
Serial in serial out(SISO)
Serial in parallel out(SIPO)
parallel in serial out(PISO)
parallel in parallel out(PIPO)
above all four are shift right operation and also to do Shift left operation.

PIN DIAGRAM OF IC 7495



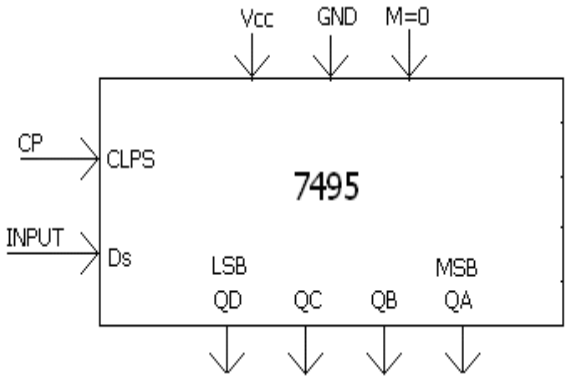
M=1 for parallel operation
M=0 for serial operation

Serial In Serial Out (SISO)-shift right



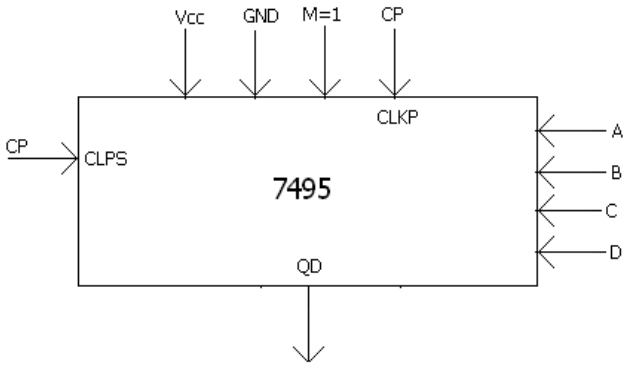
Clk	TIME	Qa	Qb	Qc	Qd
clks	T0 1	1			
	T1 0	0	1		
	T2 1	1	0	1	
	T3 1	1	1	0	1
	T4	x	1	1	0
	T5	x	x	1	1
	T6	x	x	x	1

Serial in Parallel out (SIPO)



Time	Serial data	Qa	Qb	Qc	Qd
T0	1	1			
T1	0	0	1		
T2	1	1	0	1	
T3	1	1	1	0	1

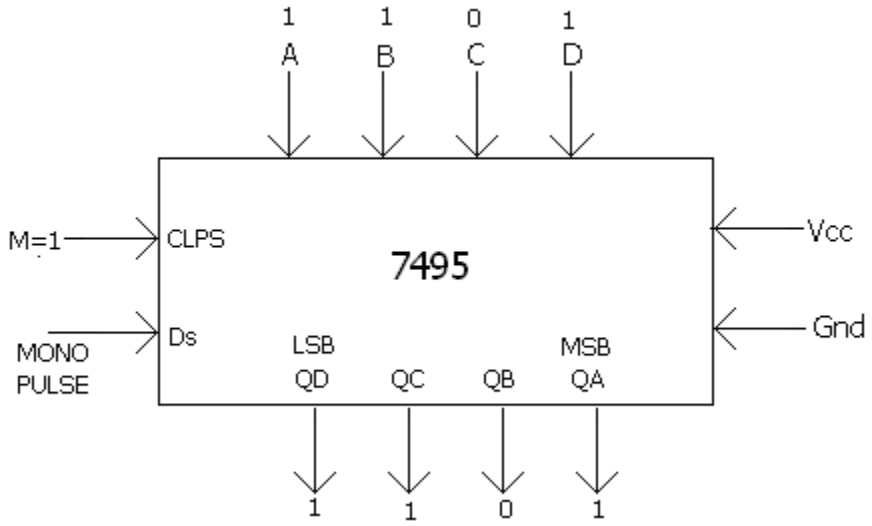
Parallel in serial out (PISO)



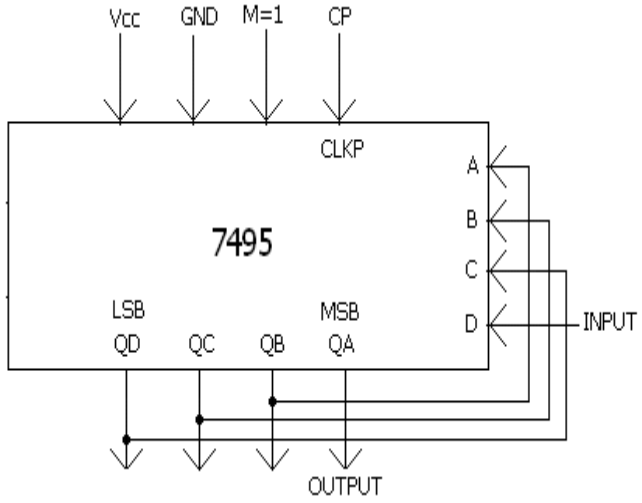
Clk	TIME	Qa	Qb	Qc	Qd
Clks	T0	1	1	0	1
	T1	x	1	1	0
	T2	x	x	1	1
	T3	x	x	x	1

To check the serial out, M is made to 0 and clk is given clock pulse

Parallel in Parallel out (PIPO)



Shift Left (serial)



Clk	TIME	I/P	Qa	Qb	Qc	Qd
clks	T0	1				1
	T1	0			1	0
	T2	1		1	0	1
	T3	1	1	0	1	1
	T4		0	1	1	X
	T5		1	1	X	X
	T6		1	X	X	X

Parallel clk to be given When mode M=0, i/p is given to A
A-Qa, Qa-B, Qb-C,Qc-D,Qd-LSB

Procedure:

Serial In Serial Out (SISO)-shift right

(i)connect mode control(pin no 6) to '0' and apply serial data at serial input at pin no 1 terminal storing from lsb.
(ii) apply clock pulses at clock one in (pin no 9) ,terminal after each data bit and observe outputs.
(iii)verify its operation as a right shift register.

Parallel in serial out (PISO)

(i) To load the parallel input data in to the shift register (ie to make Qa Qb Qc Qd = parallell input data)
(ii) Connect mode control pin no 6 to '1' state the parallel inputs A B C D to be loaded in to shift register are given to pin no 2,3,4,5 respectively.
(iii) Clck 2 (pin no 8) is pulsed once now A B C D parallel inputs appeares in the respective out puts.
(iv) To convert this parallel input data in to serial out put data on Qd line first connect mode control (pin no 6) to '0' state ,apply clk pulse at clock '1' pin no 9 and observe the outputs.

SHIFT LEFT (SERIAL)

(i) connect mode control pin no 6 to logic '1' and apply the serial data at D input starting from MSB.
(ii) Appply clk pulse at clk 2 ie pin no 8 terminal and observe the outputs Qa Qb Qc Qd,record out put states and verify its operation as a left shift register.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No:11 Date:

Ring counter/Johnson counter

AIM –Design and testing of Ring counter/Johnson counter using IC-7495

Components required :-

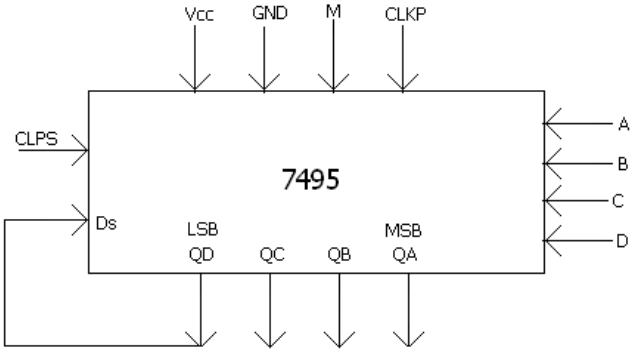
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1 2	Ring Counter Patch chords Trainer Kit	7495

RING COUNTER USING IC-7495

TRUTH TABLE

CP	QA	QB	QC	QD
t0	1	0	0	0
t1	0	1	0	0
t2	0	0	1	0
t3	0	0	0	1
t4	1	0	0	0

CIRCUIT DIAGRAM



Procedure:

(i) Connect the circuit as in the figure

(ii) To circulate logic '1' -- mode control pin no 6=0, apply data '1' at the serial input pin no 1 and apply clk pulses at clk 1 pin no 9, and observe the outputs.

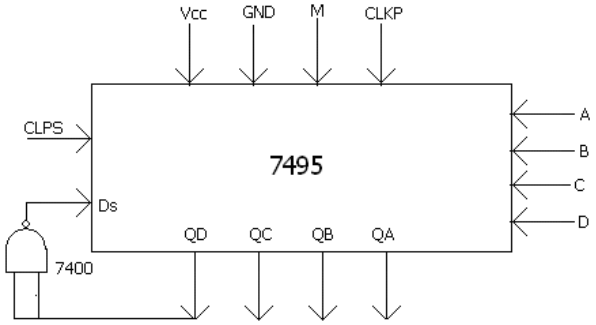
(iii) Apply a clock pulse of 1 khz at the clk 1 input observe the outputs Qa Qb Qc Qd.

JOHNSON COUNTER

TRUTH TABLE

CP	QA	QB	QC	QD
t0	1	0	0	0
t1	1	1	0	0
t2	1	1	1	0
t3	1	1	1	1
t4	0	1	1	1
t5	0	0	1	1
t6	0	0	1	1
t7	0	0	0	1
t8	1	0	0	0

CIRCUIT DIAGRAM



Procedure:

(i) Connect the circuit as in the figure

(ii) To circulate logic '1' -- mode control pin no 6=0, apply data '1' at the serilal input pin no 1 and apply clk pulses at clk 1 pin no 9, and observe the outputs.

(iii) Apply a clock pulse of 1 khz at the clk 1 input observe the outputs Qa Qb Qc Qd.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

Experiment No: 12 Date:

Sequence Generator

Aim: Design a Sequence Generator
Sequence: i) 100010011010111 ii) 1101011

Design: There are 15 bits, so there will be 15 states s=15. So at least 4 flip-flops are required.
Components required :-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1		7495
2	ExOR	7486
3	Trainer Kit	
4	Patch Chords	

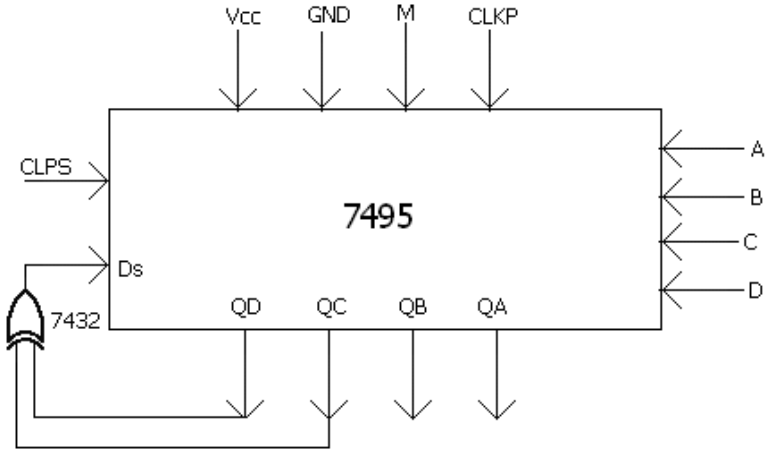
Sequence generator which generates a prescribed sequence of bits in synchronous with a clock is referred to as a Sequence generator. Shift register with feedback can be used as sequence generator on waveform generator.

Sequence: i)100010011010111

TRUTH TABLE

QA	QB	QC	QD	f
1	1	1	1	0
0	1	1	1	0
0	0	1	1	0
0	0	0	1	1
1	0	0	0	0
0	1	0	0	0
0	0	1	0	1
1	0	0	1	1
1	1	0	0	0
0	1	1	0	1
1	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

CIRCUIT DIAGRAM

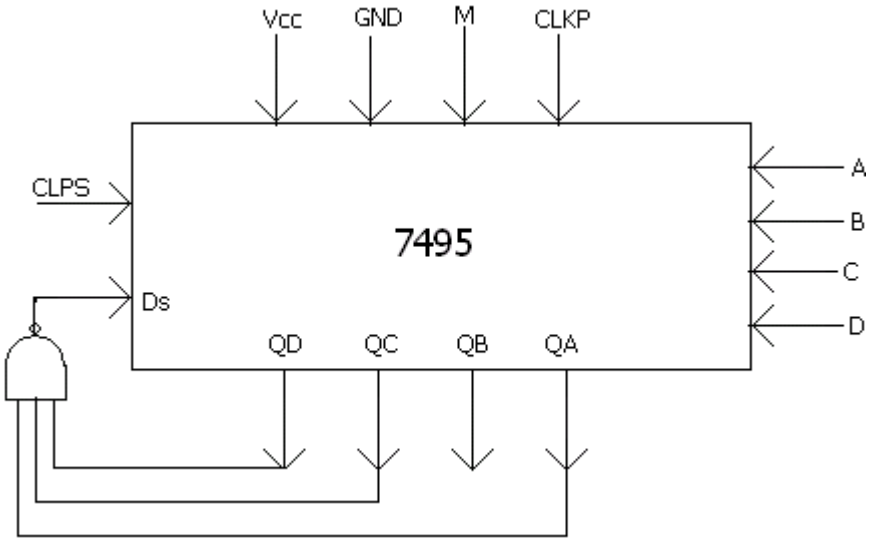


ii)1101011

TRUTH TABLE

QA	QB	QC	QD	f
1	1	1	0	1
1	1	1	1	0
0	1	1	1	1
1	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	0	1	1

CIRCUIT DIAGRAM



Procedure:

(i) Set up the circuit as shown in figure

(ii) Load the initial state by keeping mode control pin in HIGH state.

(iii) Set mode control = '0' and apply clock pulses and record all observations.

Results:

Applications:

Remarks :

Signature of Staff Incharge with date

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QUESTION BANK

1) a) Simplify and realize the given Boolean expression using Basic gates / Universal gates.
   f (a,b,c,d) = ∑(5,7,9,11,13,15)
   b) Realize Full Adder using two Half adder and OR gate.

2) a) Realize& verify the T.T. of Full Adder using EX-OR & Basic Gates.
   b) Design a counter which counts 6-12 using IC 74193.

3) a) Realize& verify the T.T. of Full Adder using Nand Gates.
   b) Design a Ring counter & Johnson counter using IC 7495

4) a) Realize& verify the T.T. of Full subtractor using EX-OR & Basic Gates.
   b) Design a mod-10 counter using IC 7490.

5) a) Realize& verify the T.T. of Full subtractor using Nand Gates.
   b) Using IC 7495 design a sequence generator for a given sequence 1101011.

6) a) Realize 4-bit i)Addition ii) Subtraction using IC 7483.
   b) Design Mod N UP counter using IC 74192.

7) a) Realize Binary to Gray using EX-OR Gates.
   b) Design Mod N down counter using IC 74192.

8) a) Realize Gray to Binary using EX-OR Gates.
   b) Design a counter which counts from 3 to 9 using IC 74192.

9) a) Realize& verify the T.T. of 4:1 MUX using only Nand Gates.
   b) Design Mod N down counter using IC 74193.

10) a) Realize& verify the T.T. of 1:4 DEMUX using only Nand Gates .
    b) Design Mod N up counter using IC 74193.

11) a) Design a mod-N counter using IC 7490.
    b) Realize& verify the T.T. of Full subtractor using IC 74139.

12) a) Design a mod-N counter using IC 7490.
    b) Realize& verify the T.T. of Full subtractor using IC 74153.

13) a) Realize& verify the T.T. of Full Adder using IC 74153
    b) Realize & verify the T.T. of priority Encoder using IC 74147.

14) a) Realize& verify the T.T. of one Bit digital comparator and demonstrate its working.
b) Design a counter which counts from 15-6 using IC 74193.

15) a) Realize& verify the T.T. of Two Bit digital comparator and demonstrate its working.
b) Conduct a suitable experiment to compare the given 4 bit data using IC7485.

16) a) Conduct a suitable to convert decimal to BCD using IC 74147.
b) Realize 3 bit MOD-N Asynchronous UP/DOWN counter using IC 7476. Write the State table.

17) a) Realize& verify the T.T. of MSJK FF using NAND Gates only.
b) Realize& verify the T.T. of T FF& D FF using NAND Gates only.

18) Realize 3 bit MOD-N Synchronous UP/DOWN counter using IC 7476. Write the state table & draw the waveforms.

19) a) Conduct a suitable experiment to compare the given 4 bit data using IC7485.
b) Realize the following operations using IC 7495.
i) SIPO i) SISO iii) PISO iv) PIPO v) shift left.

DIGITAL ELECTRONICS LABORATORY (17EC3DLLOD)

PROBABLE/SUGGESTED QUESTION BANK

1. What do you mean by Logic Gates?
2. What are the applications of Logic Gates?
3. What is Truth Table?
4. Why we use basic logic gates?
5. Write down the truth table of all logic gates?
6. What do you mean by universal gate?
7. Write truth table for 2 I/P OR, NOR, AND and NAND gate?
8. Implement all logic gate by using Universal gate?
9. Why is they called Universal Gates?
10. Give the name of universal gate?
11. Draw circuit diagram of Half Adder circuit?
12. Draw circuit diagram of Full Adder circuit?
13. Draw Full Adder circuit by using Half Adder circuit and minimum no. of logic gate?
14. Write Boolean function for half adder? Q.5 Write Boolean function for Fulladder?
15. Design the half Adder & Full Adder using NAND-NAND Logic.
16. Draw circuit diagram of Half Subtractor circuit?
17. Draw circuit diagram of Full Subtractor circuit?
18. Draw Full Subtractor circuit by using Half Subtractor circuit and minimum no. of logic gate?
19. Write Boolean function for half Subtractor?
20. Write Boolean function for Full Subtractor?
21. What is Excess-3 code? Why it is called Excess-3 code?
22. What is the application of Excess-3 Code?
23. What is ASCII code?
24. Excess-3 code is Weighted or Unweighted?
25. Out of the possible 16 code combination? How many numbers used in Excess-3 code?
26. What is Demorgan's Law?
27. Show the truth table for Demorgan's Theorem?

28. What is Minterm & Maxterm?
29. How Minterm can be converted in Max term?
30. What is Hybrid function?
31. Explain the principle of Multiplexer?
32. Draw a circuit diagram of 4: 1 Multiplexer?
33. What are the advantages of Multiplexer?
34. What are the disadvantages of Multiplexer?
35. Make the Truth-table of Multiplexer?
36. Explain about Demultiplexer?
37. Draw a circuit diagram of 1: 4 Demultiplexer?
38. Make a logic diagram of 1: 4 Demultiplexer?
39. What is the application of Demultiplexer?
40. What is the difference between Multiplexer and Demultiplexer?
41. What is Flip-Flop?
42. What is Latch circuit?
43. Draw a truth –tables of S-R, J-K, D and T?
44. What are the disadvantages of S-R Flip-Flop?
45. How can you remove the problem of S-R Flip –Flop?
46. Make circuit diagram of S-R, J-K, D and T Flip-Flop?
47. What do you understand by Race Aground condition? How it is over come in J-K Flip Flop?

References:

1. Donald D Givone, **"Digital Principles and Design",** Tata McGraw Hill Edition, 2002.
2. R.P. Jain, **"Modern Digital Electronics",** Tata McGraw-Hill Education, 3rd edition.
3. M Morris Mono, **"Digital Logic and computer design",** Prentice Hall.
4. Charles H Roth, Jr., **"Fundamentals of logic design",** Thomson Learning, 2004.
5. Mono and Kim, **"Logic and computer design Fundamentals",** Pearson, Second Edition, 2001.
6. Ronald J Tocci, Neal S. Wildmer, and Gregory L. Moss, **"Digital Systems: Principles and Applications",** Pearson, 9th Edition.
7. William I. Fletcher, **"An Engineering Approach to Digital Design"**, Prentice-Hall, 1980.