DEPARTMENT
OF
ELECTRONICS & COMMUNICATION ENGINEERING
ANALOG ELECTRONCIS CIRCUITS LABORATORY MANUAL

AEC LAB MANUAL
III Semester (ECL37)
2018
Autonomous Course

HOD-Dr. T.C. Manjunath

Lab In-Charge/s : N. Rajanish, A. Rajagopal
Anuradha Kasangottuwar, Priyanka N

Lab Instructors : Padma G.& Puttaraju M.S.

Name of the Student	:	
Semester /Section	:	
USN	:	
Batch	:	

Dayananda Sagar College of Engineering
Shavige Malleshwara Hills, Kumaraswamy Layout,
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(An Autonomous Institute Affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)
(Accredited by NBA, National Assessment & Accreditation Council (NAAC) with 'A' grade)

Dayananda Sagar College of Engineering

Dept. of E & C Engg

Name of the Laboratory-1	:	Analog Electronic Circuits lab **Padma G. (Lab instructor)**
Name of the Laboratory-2	:	Analog Electronic Circuits lab **Puttaraju M.S. (Lab instructor)**
Semester/Year	:	III/2017 & 2018 (Autonomous)
No. of Students/Batch	:	20 for each lab
No. of equipment's	:	20 for each lab
Major Equipment's for each lab	:	Power supply CRO's Signal Generator Function Generator Digital Multi Meter Rheostat Decade Resistance Box Decade Inductance Box Storage Oscilloscope Voltage Stabilizer Analog Multimeter
Area in square meters	:	104 Sq mts & 72.9 Sq mts
Location	:	Level – 3 (17214 & 17215)
Total Cost of Lab	:	Rs. 15 lakhs
Lab Incharge/s	:	N. Rajanish, A. Rajagopal Anuradha AK, Priyanka N

Instructor : Mrs. G. Padma & Mr. Puttaraju M.S

HOD : Dr. T.C. Manjunath, Ph.D. (IIT Bombay)

About the college & the department

The Dayananda Sagar College of Engineering was established in 1979, was founded by Sri R. Dayananda Sagar and is run by the Mahatma Gandhi Vidya Peetha Trust (MGVP). The college offers undergraduate, post-graduates and doctoral programmes under Visvesvaraya Technological University & is currently autonomous institution. MGVP Trust is an educational trust and was promoted by Late. Shri. R. Dayananda Sagar in 1960. The Trust manages 28 educational institutions in the name of "Dayananda Sagar Institutions" (DSI) and multi – Specialty hospitals in the name of Sagar Hospitals - Bangalore, India. Dayananda Sagar College of Engineering is approved by All India Council for Technical Education (AICTE), Govt. of India and affiliated to Visvesvaraya Technological University. It has widest choice of engineering branches having 16 Under Graduate courses & 17 Post Graduate courses. In addition, it has 21 Research Centres in different branches of Engineering catering to research scholars for obtaining Ph.D under VTU. Various courses are accredited by NBA & the college has a NAAC with ISO certification. One of the vibrant & oldest dept is the ECE dept. & is the biggest in the DSI group with 70 staffs & 1200+ students with 10 Ph.D.'s & 30^{+} staffs pursuing their research in various universities. At present, the department runs a UG course (BE) with an intake of 240 & 2 PG courses (M.Tech.), viz., VLSI Design Embedded Systems & Digital Electronics & Communications with an intake of 18 students each. The department has got an excellent infrastructure of 10 sophisticated labs & dozen class room, R & D centre, etc…

Vision & Mission of the Institute

Vision of the Institute

- To impart quality technical education with a focus on Research and Innovation emphasizing on Development of Sustainable and Inclusive Technology for the benefit of society.

Mission of the Institute

- To provide an environment that enhances creativity and Innovation in pursuit of Excellence.
- To nurture teamwork in order to transform individuals as responsible leaders and entrepreneurs.
- To train the students to the changing technical scenario and make them to understand the importance of Sustainable and Inclusive technologies.

Vision & Mission of the Department

Vision of the department

To prepare the students for the global competence, with core knowledge in ECE having focus on research to meet the needs of the industry & society.

Mission of the department

- To provide in-depth knowledge of ECE, ensuring the effective teaching learning process.
- To train the students to take up innovate projects in group with sustainable and inclusive technology relevant to the industry standards.

Program Education Objectives

PEO-1: Graduates trained with the core knowledge of ECE will be ready to apply the state of art technology to solve engineering and socially relevant problem.

PEO-2: Engineers who can engage in team work with professional ethics, technical knowledge and effective communication skills to address the practical issues in industry and society.

PEO-3: Technologists who can analyze and design innovative projects through research and sustainable technology.

PEO-4: Professionals with lifelong learning capabilities pursuing higher studies in technical/managerial courses.

Program Specific Outcomes

PSO-1: Design and develop embedded system (Microcontroller, DSP, FPGA based) applications, related to industry, social and Environmental Problems.

PSO-2: To design various types of electronic systems for applications in signal processing and communication.

Course Outcomes

Students will be able to Design

1. Half wave, full wave and center tapped rectifier circuits and to measure the amount of ripples present in each output.
2. Clipping Circuits to know the different types of distortions that are incurred in the received signal.
3. Clamping circuits to study the effect of addition of DC signal to AC.
4. Thevenin's and Maximum Power Transfer circuits
5. Resonance circuits to know the condition at which max frequency is obtained at the output
6. RC Coupled amplifier to measure the amplified signals voltage, current, frequency, equivalent input, output impedance of the circuit and the frequency band to which the circuit responds.
7. To generate signals of desired frequency using Oscillator circuits.
8. A circuit for the current amplification, voltage follower and analyze the input and output impedances using Darlington Emitter follower.

9. Two stage Voltage series feedback amplifier and to know the various parameters such as resistance, frequency etc.

CO1	Design rectifiers, clippers and clamper circuits.
CO2	Verification of Thevenin's and Maximum Power Transfer Theorems and Resonance circuits.
CO3	To design BJT and FET based RC Coupled amplifier to measure the amplified signals voltage, current, frequency, equivalent input, output impedance of the circuit and the frequency band to which the circuit responds.
CO4	Ability to analyze the working operation of voltage follower with current amplification.
CO5	To generate signals of desired frequency using Oscillator circuits.
CO6	To design Power Amplifiers and verify the characteristics of MOSFET

Mapping of Course outcomes to Program outcomes

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	2	2	2	1	-	-	1	-	-	1
CO2	3	2	2	2	2	1	-	-	1	-	-	1
CO3	3	2	2	1	2	1	-	-	1	-	-	1
CO4	2	1	1	1	2	1	-	-	1	-	-	1
CO5	3	2	2	2	2	1	-	-	1	-	-	1
CO6	3	2	1	2	2	1	-	-	1	-	-	1

DO's

- Students should follow the dress code of the laboratory compulsorily.
- Keep your belongings in the corner of the laboratory.
- Students have to enter their name, USN, time in/out and signature in the log register maintained in the laboratory.
- Students are required to enter components in the components register related to the experiment and handle the equipment's smoothly.
- Check the components, range and polarities of the meters before connecting to the circuit.
- Come prepare for the experiment and background theory.
- Before connecting to the circuit refer the designed circuit diagram properly. Debug the circuit for proper output.
- Students should maintain discipline in the laboratory and keep the laboratory clean and tidy.
- Observation book and Record book should be complete in all respects and get it corrected by the staff members.
- Clarify the doubts with staff members and instructors.
- Experiment once conducted, in the next lab, the entire record should be complete in all respects, else the student will lose the marks.
- For programming lab, show the output to the concerned faculty.
- All the students should come to LAB on time with proper dress code and identity cards
- Keep your belongings in the corner of laboratory.
- Students have to enter their name, USN, time-in/out and signature in the log register maintained in the laboratory.
- All the students should submit their records before the commencement of Laboratory experiments.
- Students should come to the lab well prepared for the experiments which are to be performed in that particular session.
- Students are asked to do the experiments on their own and should not waste their precious time by talking, roaming and sitting idle in the labs.

- Observation book and record book should be complete in all respects and it should be corrected by the staff member.
- Before leaving the laboratory students should arrange their chairs and leave in orderly manner after completion of their scheduled time.
- Prior permission to be taken, if for some reasons, they cannot attend lab.
- Immediately report any sparks/ accidents/ injuries/ any other untoward incident to the faculty /instructor.
- In case of an emergency or accident, follow the safety procedure.
- Switch OFF the power supply after completion of experiment.

DONT's

- Do not switch on the power supply before verification of the connected circuits by concerned staff.
- Do not feed higher voltages than rated to the device.
- Do not upload, delete or alter any software on the laboratory PC's.
- Do not write or mark on the equipment's.
- Usage of mobile phone is strictly prohibited.
- Ragging is punishable.
- If student damages the equipment or any of the component in the lab, then he / she is solely responsible for replacing that entire amount of the equipment or else, replace the equipment.
- The use of mobile/ any other personal electronic gadgets is prohibited in the laboratory.
- Do not make noise in the Laboratory & do not sit on experiment table.
- Do not make loose connections and avoid overlapping of wires.
- Don't switch on power supply without prior permission from the concerned staff.
- Never point/touch the CRO/Monitor screen with the tip of the open.

ANALOG ELECTRONIC CIRCUITS LAB
AUTONOMOUS COURSE
2018

Course code : ESL37 Credits: 2 & 3 hrs per lab

L : P : T : S : 1 : 2 : 0 : 0 CIE Marks: 50

Exam Hours : 3 SEE Marks: 50

EXPT	Course Content	Hours	COs
1	Diode Clipping Circuits	03	CO1
2	Diode Clamping Circuits	03	CO1
3	Half-wave, Full-wave and Bridge Rectifier Circuits	03	CO1
4	Verification of Theorems (Thevenin's & Maximum Power Transfer) for DC Circuits	03	CO2
5	Resonant Circuits –Series and Parallel circuits	03	CO2
6	RC Coupled Single Stage BJT Amplifier	03	CO3
7	RC Coupled Single Stage FET Amplifier	03	CO3
8	BJT Darlington Emitter follower with and without bootstrapping	03	CO4
9	BJT RC Phase-shift Oscillator	03	CO3 CO5
10	BJT Colpitt's & Hartley Oscillator	03	CO3 CO5
11	BJT Crystal Oscillator	03	CO3 CO5
12	Two stage BJT Voltage series feedback amplifier	03	CO3
13	Class B push pull Amplifier.	03	CO6
14	Characteristics of MOSFET.	03	CO6

Cycle of experiments

DO's

- All the students should come to LAB on time with proper dress code and identity cards. Keep your belongings in the corner of laboratory.
- Students have to enter their name, USN, time-in/out and signature in the log register maintained in the laboratory.
- All the students should submit their records before the commencement of Laboratory experiments.
- Students should come to the lab well prepared for the experiments which are to be performed in that particular session.
- Students are asked to do the experiments on their own and should not waste their precious time by talking, roaming and sitting idle in the labs.
- Observation book and record book should be complete in all respects and it should be corrected by the staff member.
- Before leaving the laboratory students should arrange their chairs and leave in orderly manner after completion of their scheduled time.
- Prior permission to be taken, if for some reasons, they cannot attend lab.
- Immediately report any sparks/ accidents/ injuries/ any other untoward incident to the faculty /instructor.
- In case of an emergency or accident, follow the safety procedure.
- Switch OFF the power supply after completion of experiment.

DONT's

The use of mobile/ any other personal electronic gadgets is prohibited in the laboratory.

- Do not make noise in the Laboratory & do not sit on experiment table.
- Do not make loose connections and avoid overlapping of wires
- Don't switch on power supply without prior permission from the concerned staff.
- Never leave the experiments while in progress.
- Do not leave the Laboratory without the signature of the concerned staff in observation book.

Experiment No. : 1 Date : / / .

Rectifiers and Filters

Aim: To design and verify the performance of half wave rectifier, center tap full wave rectifier and bridge rectifier with and without 'C' filter

Apparatus/Components required:

Sl. No.	Particulars	Range	Quantity
1.	Transformer	As per design	01
2.	Diode (BY 127 / 1N4007)	-	04
3.	Resistors & Capacitors	As per design	-
4.	Multimeter	-	01
5.	CRO Probes	-	2 Set
6.	Spring board and connecting wires	-	-

Theory:

Rectifier is a circuit which converts AC to pulsating DC. Rectifiers are used in construction of DC power supplies. There are three types of rectifiers namely Half wave rectifier, Center tap full wave rectifier and bridge rectifier.

In half wave rectification, either the positive or negative half of the AC wave is passed, while the other half is blocked. Because only one half of the input waveform reaches the output, it is very inefficient if used for power transfer.

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient. Fullwave rectification can be obtained either by using center tap transformer or by using bridge rectifier.

The output of a rectifier is not a smooth DC it consistes of ac ripples there fore to convert this pulsating DC in to smooth DC we use a circuit called filter. There are many types of filters like C filter, L filter, LC filter, multiple LC filter, π filter etcc.. of all these C filter is the most fundamental filter.

Design Procedure :

a) Half Wave Rectifier Without filter

$V_{DC} = Vm / \pi$

For the given V_{DC} calculate Vm and Vrms = Vm / 2

Choose the transformer of rating, 0 – Vrms / ≥ I_{DC}

The value of load resistance, $R_L = V_{DC} / I_{DC}$, $P_{RL} = V_{DC}^2 / R_L$

b) Center Tap Full Wave Rectifier / Bridge Rectifier Without filter

$V_{DC} = 2Vm / \pi$ for FWR (both center tap and bridge rectifier)

For the given V_{DC} calculate Vm and Vrms = $Vm / \sqrt{2}$

Choose the transformer of rating Vrms – 0 – Vrms / ≥ I_{DC} for Center tap full wave rectifier and

0 – Vrms / ≥ I_{DC} for Bridge rectifier

The value of load resistance, $R_L = V_{DC} / I_{DC}$, $P_{RL} = V_{DC}^2 / R_L$

c) Half Wave Rectifier with 'C' filter

$\gamma = 1 / (2\sqrt{3} fCR_L)$ (f = 50 Hz)

For the given value of V_{DC} and I_{DC} Calculate $R_L = V_{DC} / I_{DC}$, $P_{RL} = V_{DC}^2 / R_L$

For the given γ Calculate the value of capacitor 'C'

For the given value of V_{DC} and I_{DC} Calculate Vm and Vrms = Vm / 2

Choose the transformer of rating, 0 – Vrms / ≥ I_{DC}

Choose the capacitor of value C / ≥ Vm

d) Full Wave Rectifier / Bridge Rectifier with 'C' filter

$\gamma = 1 / (4\sqrt{3} fCR_L)$ (f = 50 Hz)

For the given value of V_{DC} and I_{DC} Calculate $R_L = V_{DC} / I_{DC}$, $P_{RL} = V_{DC}^2 / R_L$

For the given γ Calculate the value of capacitor 'C'

For the given value of V_{DC} and I_{DC} Calculate Vm and Vrms = $Vm / \sqrt{2}$

Choose the transformer of rating,

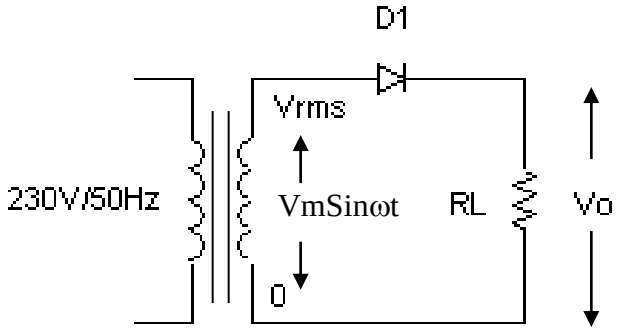
Vrms – 0 – Vrms / ≥ I_{DC} for Center tap full wave rectifier and 0 – Vrms / ≥ I_{DC} for Bridge rectifier Choose the capacitor of value C / ≥ Vm

Procedure:

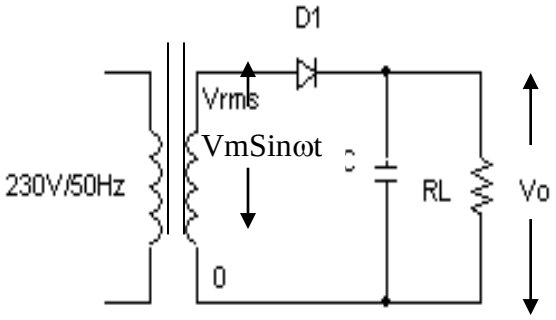
1. Components / Equipment are tested for their good working condition
2. Connections are made as shown in the circuit diagram
3. Observe different waveforms on CRO
4. Measure V_{DC} using multimeter in dc mode and Vm on CRO
5. Calculate Vrms from Vm using formula Vrms = Vm / 2 for Half wave rectifier Vrms = Vm / √2 for full wave rectifier
6. Calculate the efficiency, ripple factor and regulation. Compare the results with the theoretic values.

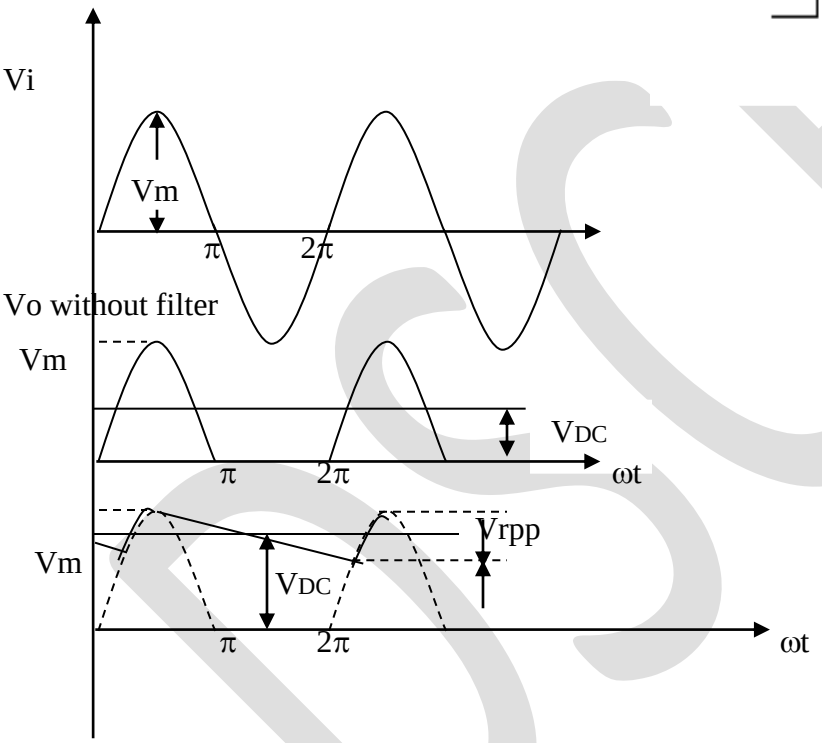
Circuit Diagram:

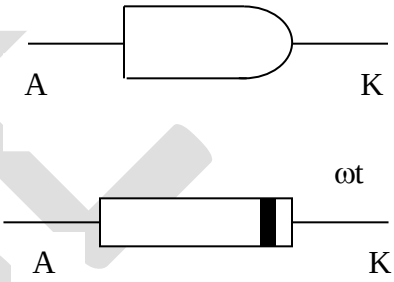
a) Half wave rectifier without filter



b) Half wave rectifier with 'C' filter

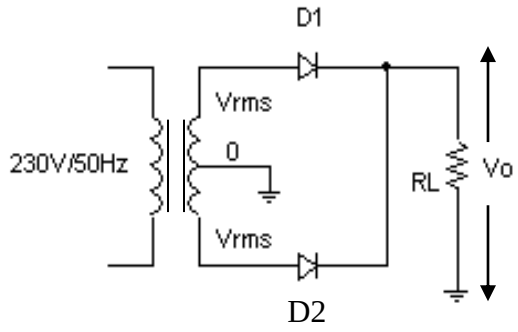




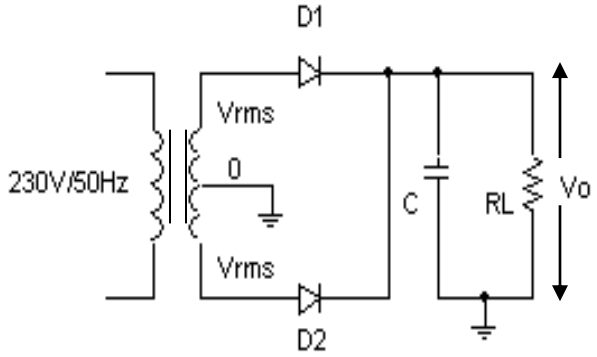


Full wave rectifier

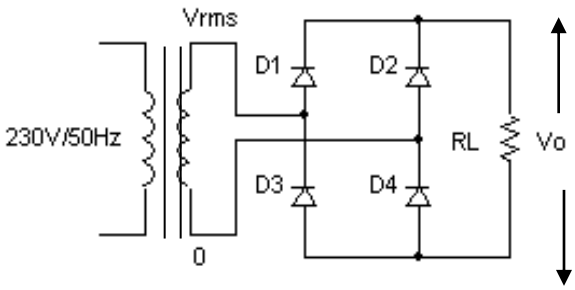
a) Center tap FWR without filter



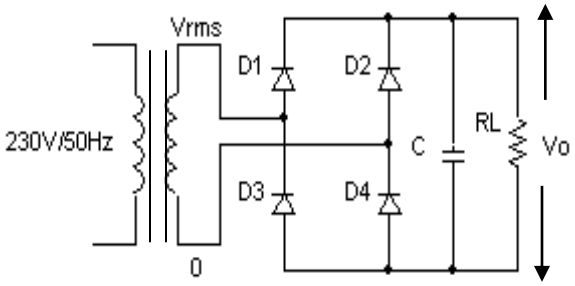
b) Center tap FWR with 'C' filter

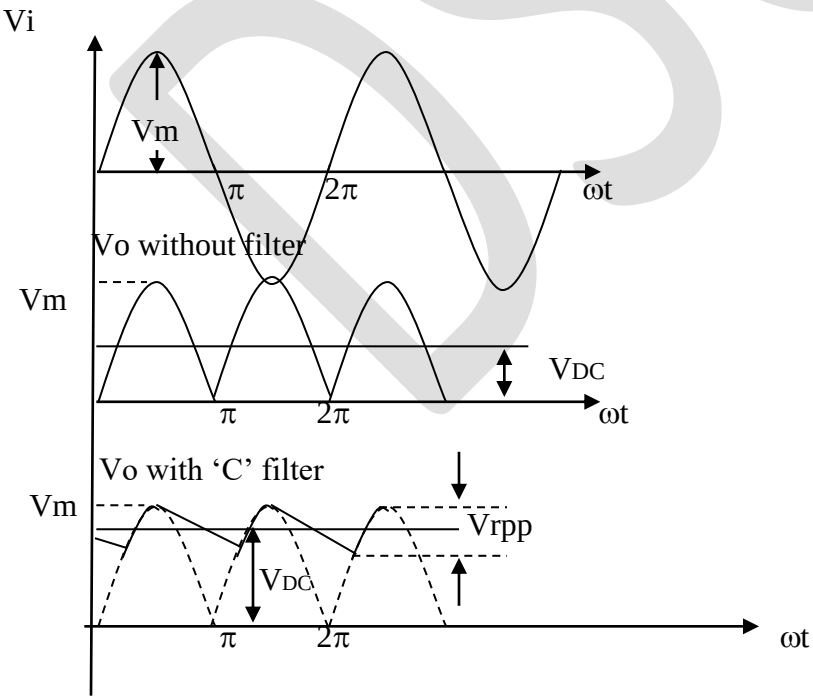


a) Bridge Rectifier without filter



b) Bridge Rectifier with 'C' filter





Without filter

Circuit	V_{DC}	Vm	Vrms	$\eta = V_{DC}^2 / Vrms^2$	$\gamma = \sqrt{(Vrms^2 / V_{DC}^2) - 1}$
Half wave rectifier					
Center tap full wave rectifier					
Bridge Rectifier					

Note : Vrms = Vm / 2 for Half wave rectifier Vrms = Vm / $\sqrt{2}$ for full wave rectifier

With filter :

Circuit	V_{DC} full load	Vrpp	Vrrms	V_{DC} *no load*	% Regulation	γ = Vrrms / V_{DC}
Half wave rectifier						
Center tap full wave rectifier						
Bridge rectifier						

Note : Vrrms = Vrpp / $2\sqrt{3}$

% Regulation = (V_{DC} no load – V_{DC} full load) / V_{DC} full load

Without filter:

Type of rectifier	γ - theoretical	γ - practical	η - theoretical	η - practical
Half wave rectifier	1.21		40.6 %	
Center tap full wave rectifier	0.48		81.2 %	
Bridge Rectifier	0.48		81.2 %	

With filter:

Type of rectifier	γ theoretical	γ practical	% Regulation
Half wave rectifier	0.012		
Center tap full wave rectifier	0.006		
Bridge Rectifier	0.006		

Results:

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 2 Date : / / .

Clipping Circuits

Aim: To design and study the series and shunt clipping circuits using diodes.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	Diode (1N4007 / BY 127)	-	02
2.	Resistor	As per design	-
3.	Multimeter	-	01
4.	CRO Probes	-	3 set
5.	Spring Board and Connecting wires	-	-

Theory :

A clipper is a circuit that removes either positive or negative portion of a waveform. This kind of processing is useful for signal shaping, circuit protection and communications. The clippers are usually constructed by using diodes and resistors and some times to adjust the clipping level DC power supplies are also used. There are two types of clippers namely series clippers and shunt clippers. If the clipping element (diode) is in series with the source then we call it as series clippers and if the clipping device is in parallel with the source then we call such circuit as shunt clippers. Further based on the portion of a waveform clipped the clippers can be classified as positive clippers, negative clippers and two level clippers (combination clippers).

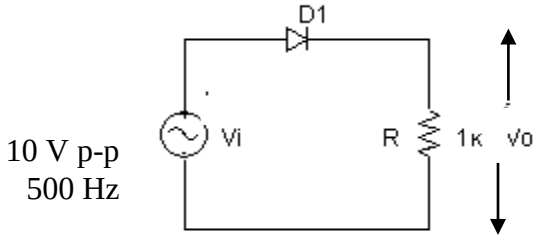
Procedure :

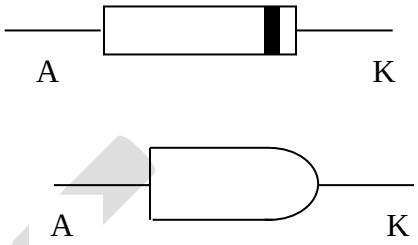
1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram
3. Apply a sine wave of amplitude greater than the designed clipping level with frequency 500 Hz.
4. Observe the output wave form on the CRO
5. Observe the transfer characteristic curve on CRO by applying input waveform to channel – X and output waveform to channel – Y.
6. Measure the clipped voltage and compare with the designed value.

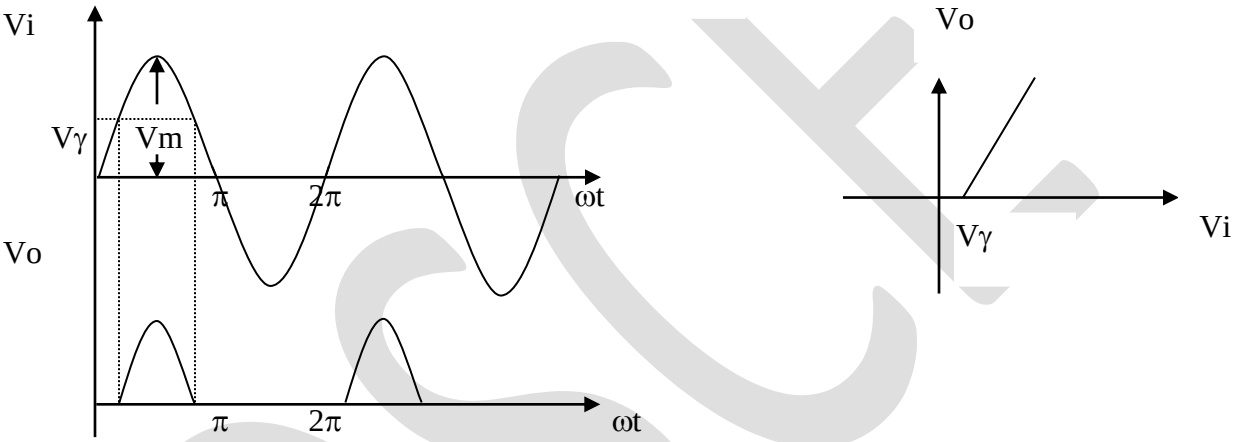
Circuit Diagram:

A. Series Clippers:

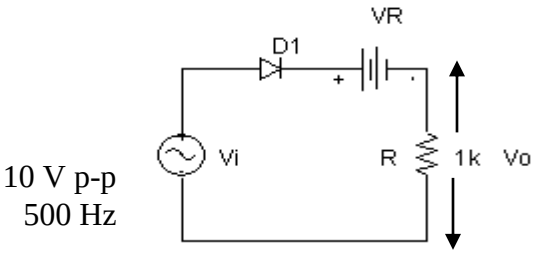
1. To pass positive peak above Vγ level

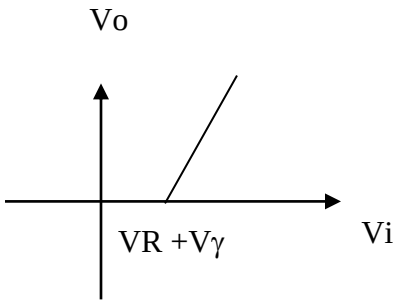


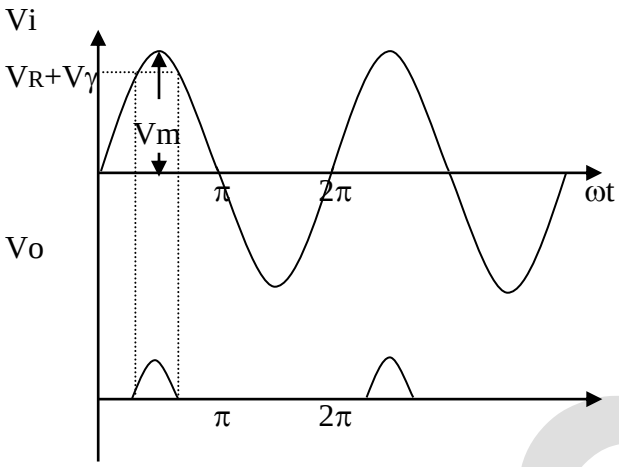




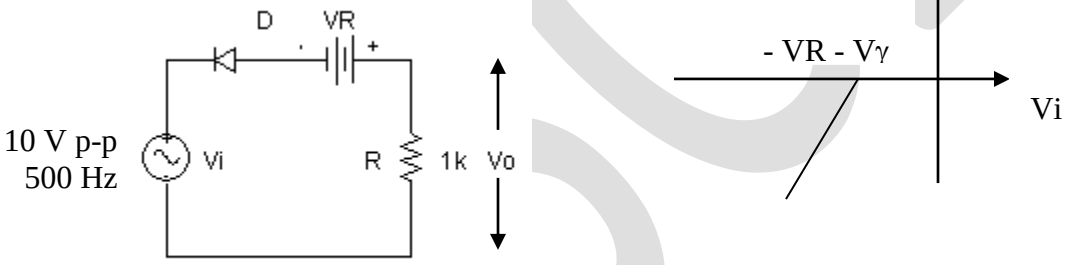
2. To pass positive peak above some reference level (VR +Vγ)

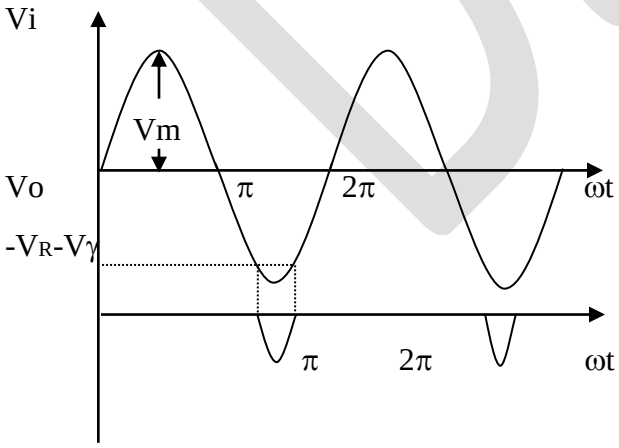






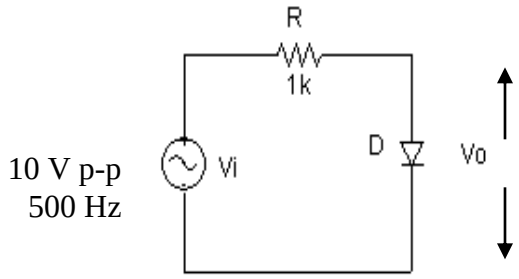
3. To pass negative peak above some reference level (-VR - Vγ)

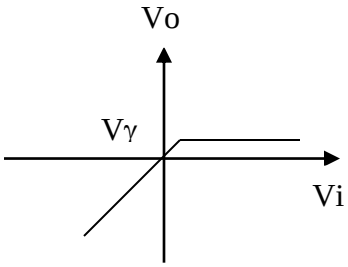


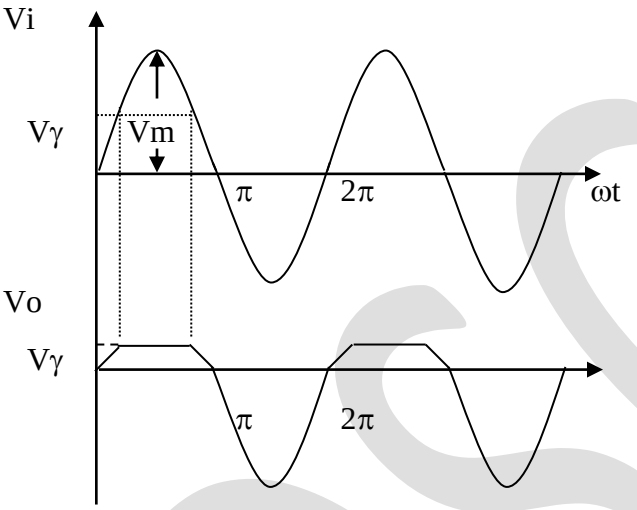


B. Shunt Clippers

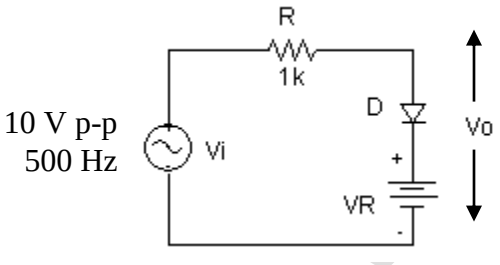
4. To remove positive peak above Vγ level

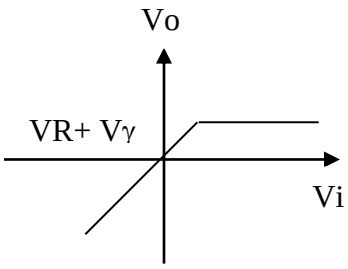


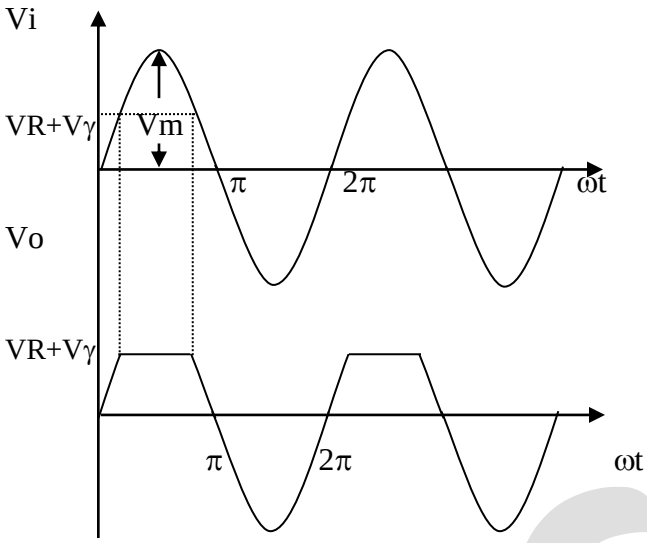




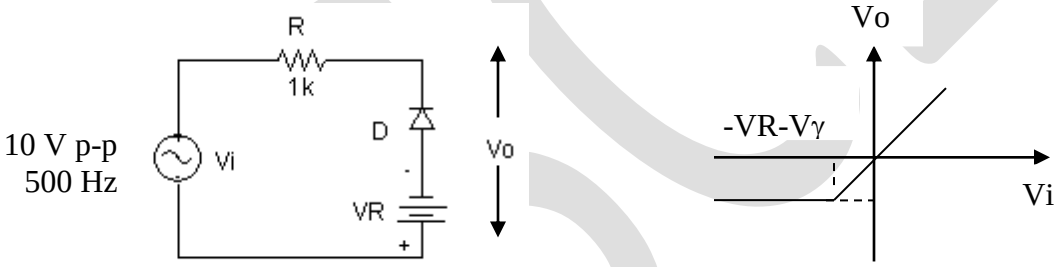
5. To remove positive peak above some reference level (VR +Vγ)

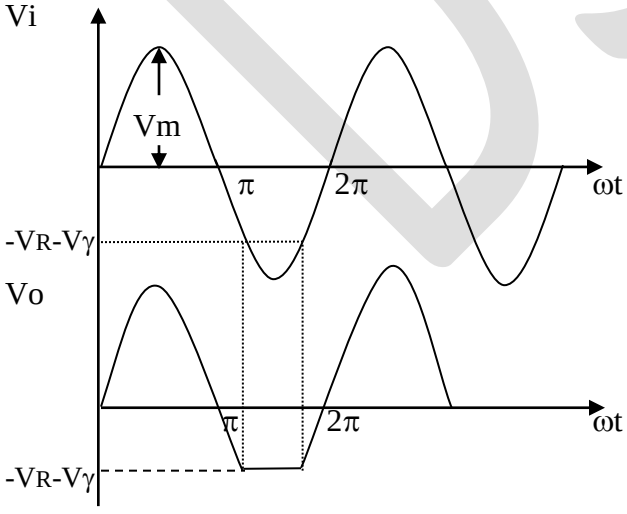




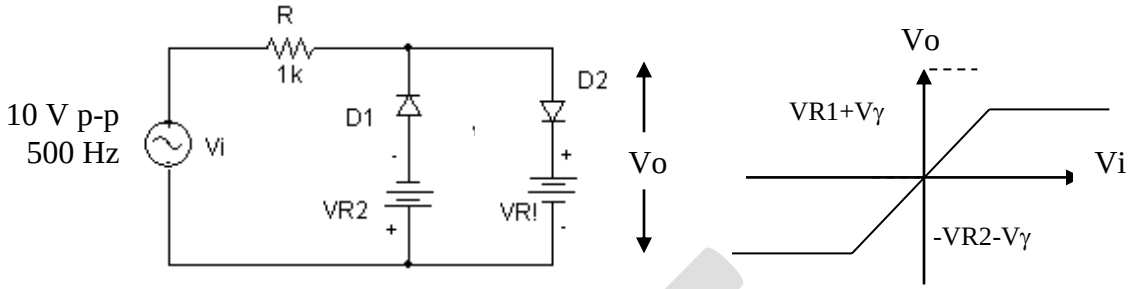


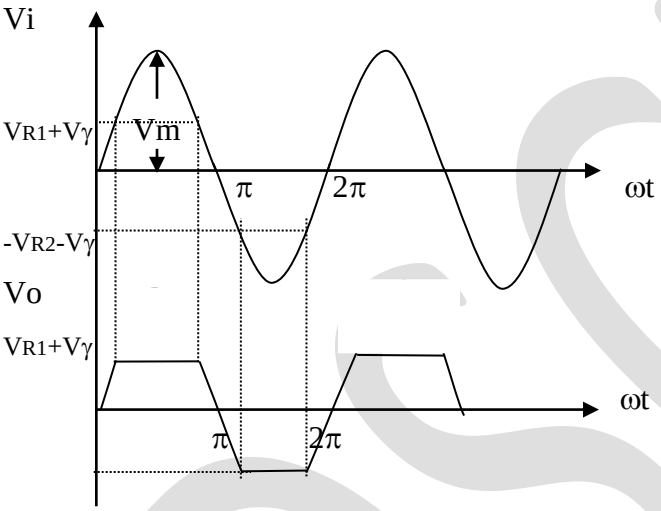
6. To remove negative peak above some reference level (-VR-Vγ)





7. To remove positive peak above some reference level (VR1+Vγ) and negative peak above some reference level (-VR2-Vγ)





Results:

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 3 Date : / / .

Clamping Circuits

Aim : To design a clamping circuit for the given specification.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Diode (1N4007 / BY 127)	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 set
4.	Spring board and connecting wires		

Theory :

Clamper is a circuit which adds DC level to an AC waveform. There are two types of clampers namely positive clampers and negative clampers. In positive clampers positive DC level will be added to the AC waveform or the negative peak will be clamped to some other level. In Negative peak clampers negative DC level will be added to the AC waveform or the positive peak will be clamped to some other level.

Clampers are very much used in communication systems for example clampers are used in analog television receivers for the purpose of restoring the dc component of the video signal prior to its being fed to the picture tube.

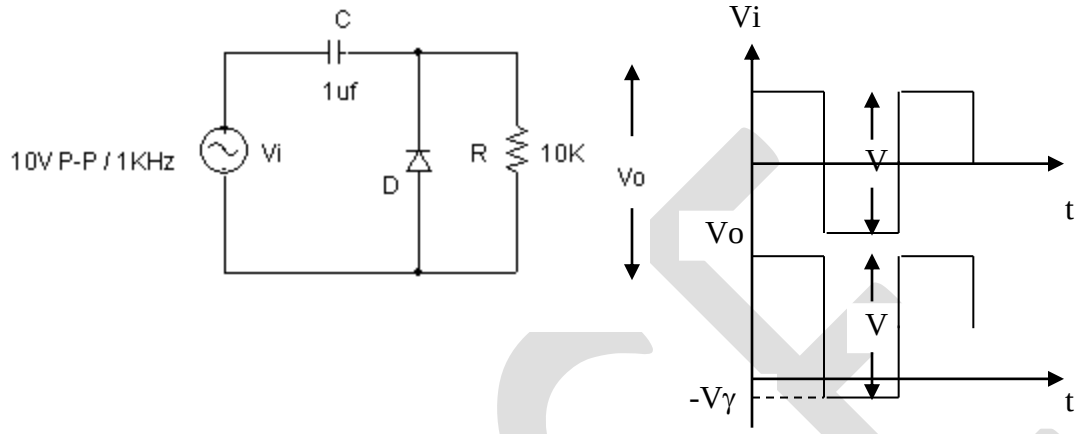
Procedure :

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram
3. Apply a square wave / triangular wave / sine wave input of amplitude 10 V peak to peak and frequency of 1 kHz
4. Observe the input and output waveform keeping CRO in DC position
5. Measure the clamping level and compare with the designed value

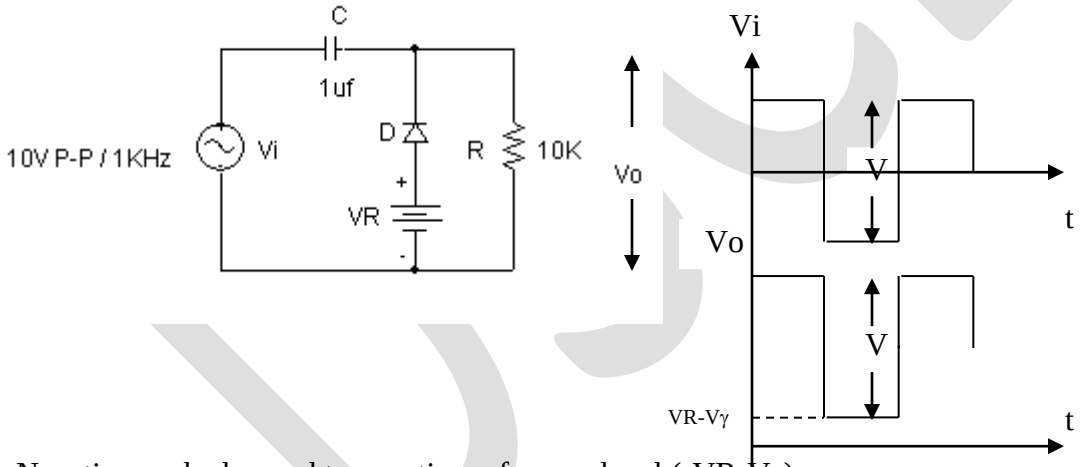
Circuit Diagram :

Positive Clampers :

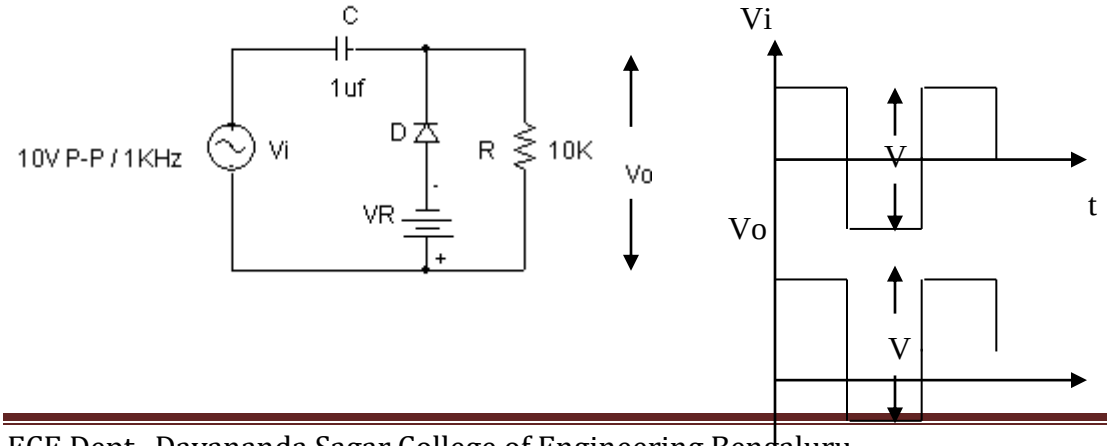
1. Negative peak clamped to -Vγ level



2. Negative peak clamped to positive reference level (VR-Vγ)



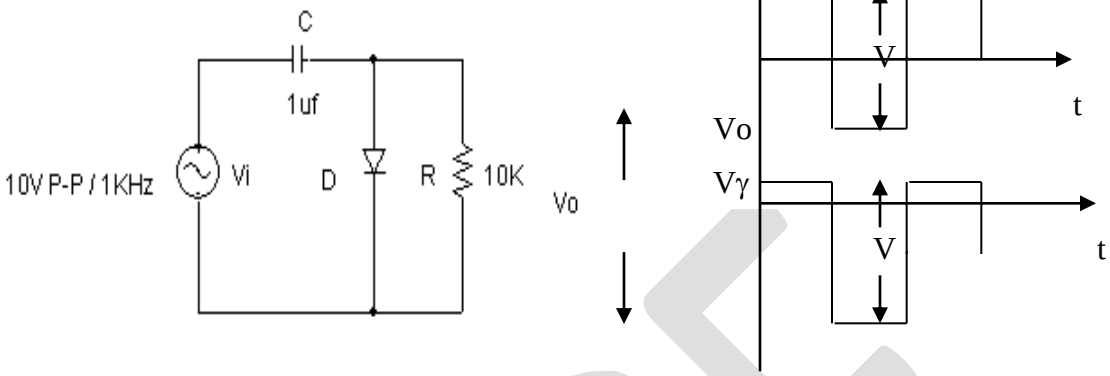
3. Negative peak clamped to negative reference level (-VR-Vγ)



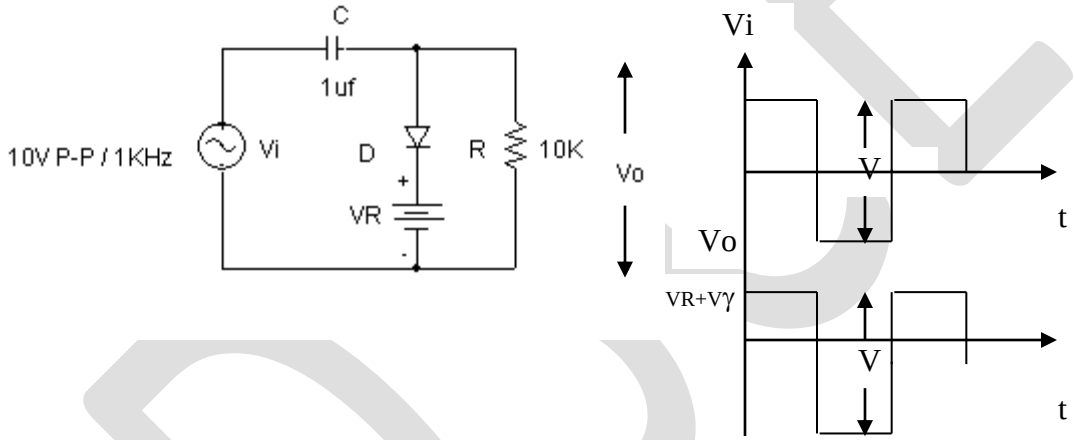
-VR-Vγ ------ t

Negative Clampers :

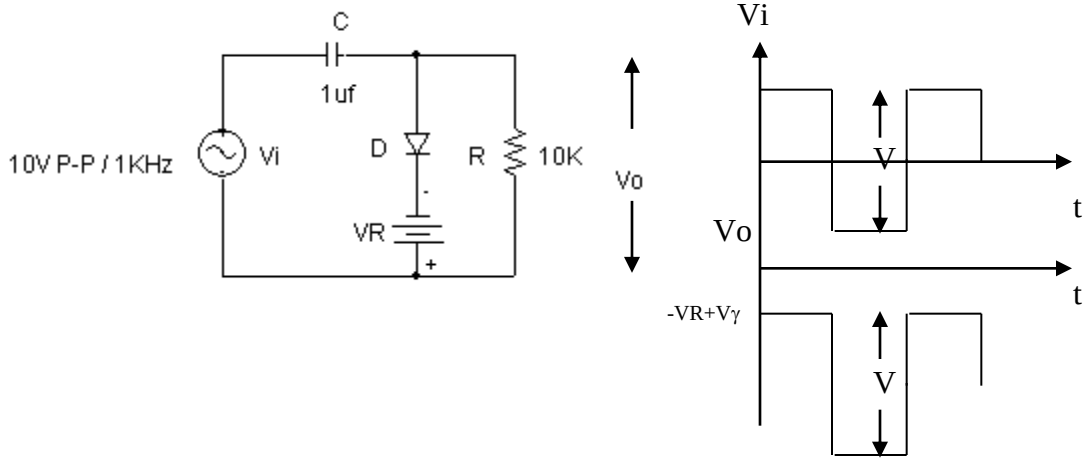
4. Positive peak clamped to Vγ level



5. Positive peak clamped to positive reference level (VR+Vγ)



6. Positive peak clamped to negative reference level (-VR+Vγ)



Results:

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 4 Date : / / .

Verification of Theorems

Aim : To verify Thevenin's and Maximum power transfer theorem for DC circuits.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Resistors	As per design	-
2.	Mili ammeter	0 - 20mA	01
3.	Multimeter	-	01
4.	DRB	-	01
5.	Spring board and connecting wires	-	-

Theory :

Thevenin's Theorem :

Thevenin's theorem states that any linear two-terminal circuit, as in figure - 1, may be replaced by a Thevenin voltage source of voltage V_{Th} in series with a Thevenin resistance R_{Th}, as shown in figure 1d. This equivalent circuit will produce the same voltages and currents in any external circuit as does the original linear circuit.

Maximum Power Transfer Theorem :

The maximum power transfer theorem states that the maximum power will be transferred from a source with a finite internal resistance to the load only when the load resistance is equal to the source internal resistance. When RL = RS the maximum power will be transferred to the load.

Procedure :

1. Thevenin's Theorem

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in figure 1a, and the load current IL is recorded
3. Disconnect the load resistance between A & B and determine Vth (Figure 1b).
4. By doing connections as shown in figure 1c Rth is calculated (Apply V = 10V).

5. Rig up the Thevinin's equivalent circuit as shown in figure 1d and observe IL′, where IL′ = IL

2. Maximum Power Transfer Theorem

1. Connections are made as shown in figure 2a.
2. Vary RL from 100Ω to 2 KΩ in convenient steps (say 100Ω) and note down corresponding Io and Vo.
3. Calculate Po and plot a graph of RL versus Po.
4. Determine the maximum power and corresponding load resistance.

Circuit Diagram :

Thevenin's Theorem

Figure 1. Given circuit

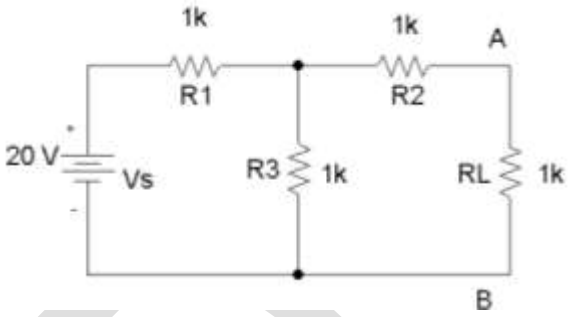
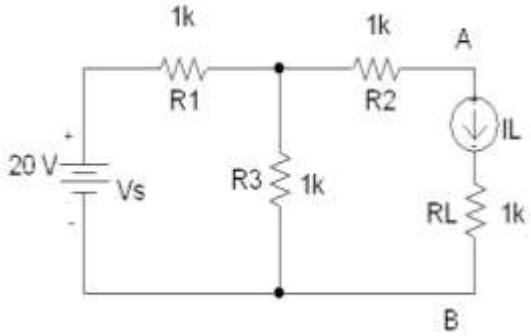
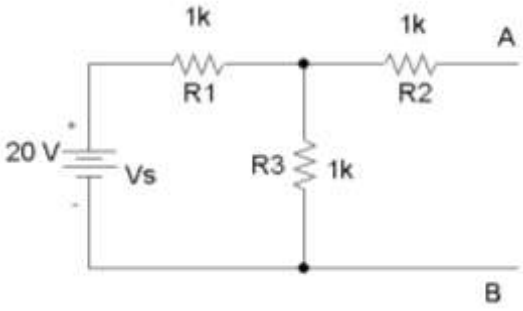


Figure 1a To measure load current



IL = ____mA

Figure 1b To measure Vth



Vth = _____ V

Figure 1c To determine Rth

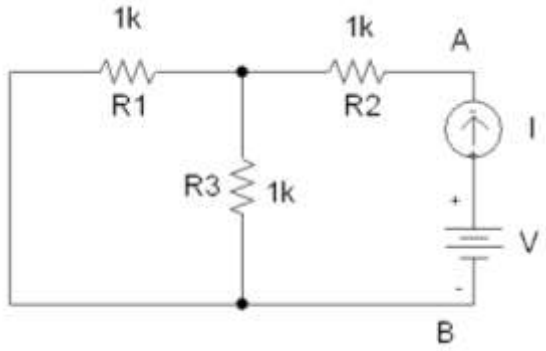
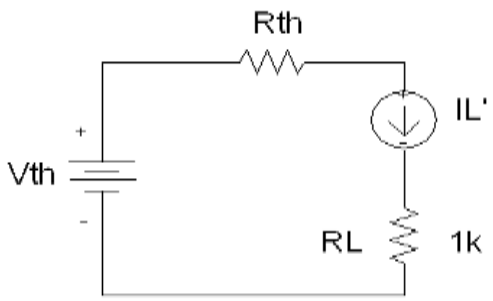


Figure 1d Thevinin's equivalent circuit



V = _____, I = _____

IL′ = _____ mA

Rth = V / I = _____ Ω

Note : IL = IL′

Maximum Power Transfer Theorem :

Figure 2 Given Circuit

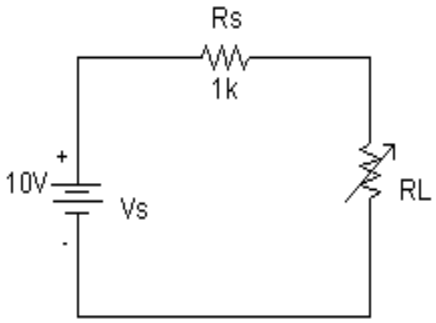
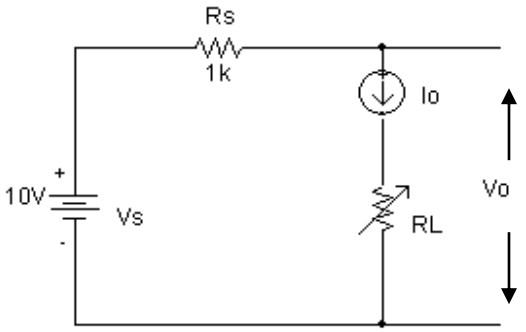


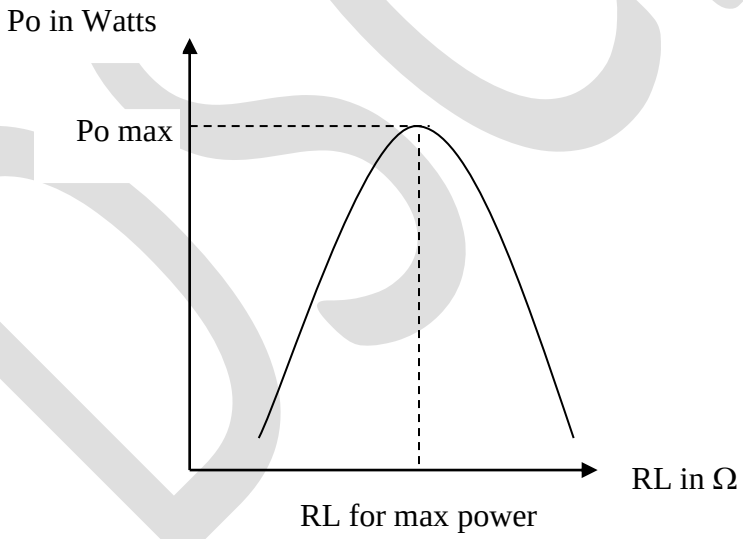
Figure 2a Practical circuit



Tabular Column :

Sl. No.	R_L in Ω	Vo in Volt	Io in mA	Power Po = Vo X Io

Ideal Graph :



Result :

1.IL = _____, IL'=____ (Since IL=IL' Thevenin's theorem is verified)

2.Po Max =_____ , RL(at Po Max)= _____ (at RL=RS, Maximum power will be transferred to the load)

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 5 Date : / / .

Series and Parallel Resonance Circuits

Aim : To design and study the series and parallel resonance circuits and to determine the bandwidth and quality factor of the circuit.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	DCB and DIB	-	1 each
2.	Resistors	1 KΩ 680Ω	1 each
2.	CRO probes	-	2 set
3.	Spring board and connecting wires	-	-

Theory :

A resonant circuit, also called a tuned circuit consists of an inductor and a capacitor together with a voltage or current source. It is one of the most important circuits used in electronics. For example, a resonant circuit, in one of its many forms, allows us to select a desired radio or television signal from the vast number of signals that are around us at any time. A network is in resonance when the voltage and current at the network input terminals are in phase and the input impedance of the network is purely resistive.

A condition of resonance will be experienced in a tank circuit when the reactance of the capacitor and inductor are equal to each other. Because inductive reactance increases with increasing frequency and capacitive reactance decreases with increasing frequency, there will only be one frequency where these two reactance will be equal. The reactance of inductor is given by $X_L = 2 \pi f L$ and the reactance of capacitor is given by $X_C = 1 / (2 \pi f C)$

In basic series-resonant circuit the steady state amplitude and the phase angle of the current vary with the frequency of the sinusoidal voltage source. As the frequency of the source changes, the maximum amplitude of the source voltage (Vm) is held constant. The frequency at which the reactance of the inductance and the capacitance cancel each other is the resonant frequency (or the unity power factor frequency) of this circuit hence at this frequency the

amplitude across the LC network becomes minimum and at other frequencies the total reactance of inductor and capacitor will be more than that at resonant frequency hence the amplitude will be more.

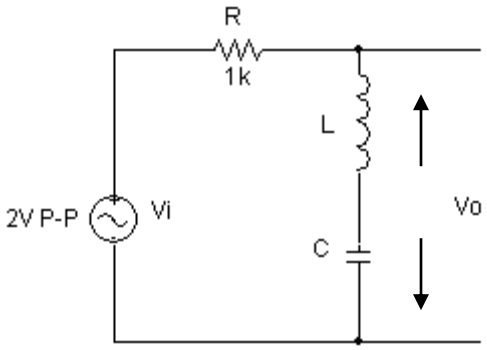
In parallel resonant circuit at resonance the reactance of the inductance and the capacitance will become equal and the output voltage will be maximum where at other frequencies any one of the reactance will be less than other so that the output voltage will be less.

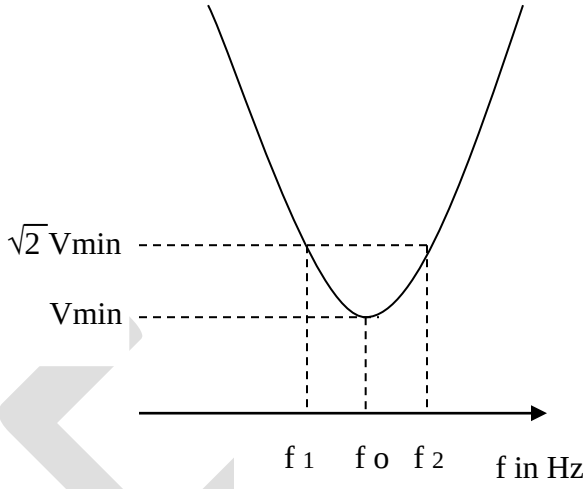
Resonance was discovered by Galileo Galilei with his investigations of pendulums beginning in 1602.

Procedure :

1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram
3. Set the signal generator to to 2V p-p and vary the frequency from 100Hz to 10KHz and corresponding output amplitude is measured using multimeter in ac mode
4. Plot a graph of frequency in Hz versus Vo
5. Calculate BW and quality factor.

Circuit Diagram : Series Resonance





Design :

Given fo = 5 KHz

f o = 1 / ($2\pi\sqrt{LC}$)

assume C = 0.1 uf

L = 10.13 mH, Choose L = 10 mH

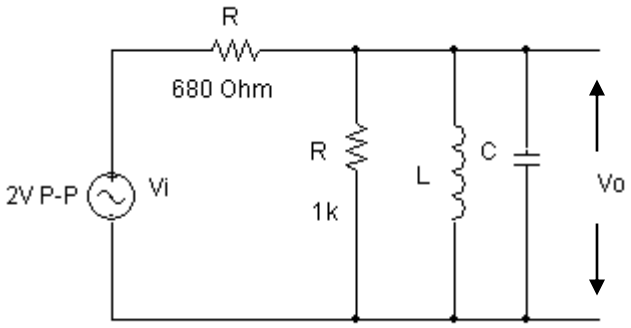
Tabular Column :

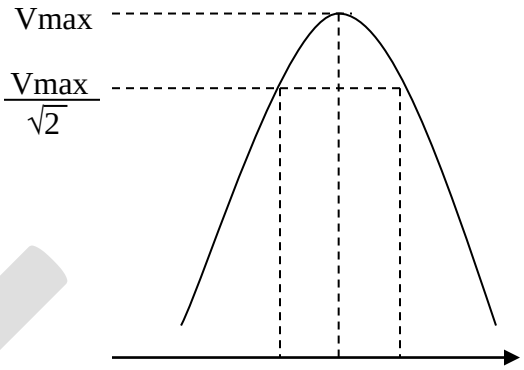
Vi* = _____ *V

6.

Frequency in Hz	Vo in volt

Parallel Resonance :





Design :

Given fo = 5 KHz

$f_o = 1 / (2\pi\sqrt{LC})$

assume C = 0.1 uf

L = 10.13 mH, Choose L = 10 mH

Tabular Column :

Vi = _____ V

Frequency in Hz	Vo in volt

Result :

Series Resonance: Qo = _____, BW = _____ Hz

Parallel Resonance: Qo = _____, BW = _____ Hz

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 6 Date : / / .

RC Coupled Single Stage BJT Amplifier

Aim : To conduct an experiment to plot the frequency response of an RC coupled amplifier and to find the input impedance, output impedance and the voltage gain.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL100	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory :

An amplifier is a circuit which increases the voltage, current or power level of i/p signal where the frequency is maintained constant from o/p to i/p signal. The common emitter amplifier is basically a current amplifier (IC = β IB) where IB is input current and IC is output current and β is a non unity value, in turn it provides voltage amplification. The ratio of collector current to base current is noted as the current amplification factor and is denoted as 'β'i.e.[$\beta = I_C/I_B$], β is very large.

In RC coupled CE amplifier R1, R2 and RC are selected in such a way that transistor operates in active region and the operating point will be in the middle of active region. RE is used for stabilization of operating point. Coupling capacitors CC1 and CC2 are used to block dc current flow through load and the source. The emitter by-pass capacitor CE is connected to avoid negative feedback. Input signal increases base current and the collector current increases by a factor β. [i.e. Ic = βIb]. Hence output voltage is large compared to input voltage which is known as amplification

An amplifier in which resistance-capacitance coupling is employed between stages and at the input and an output point of the circuit is known as RC coupled amplifier. A capacitor provides a path for signal currents between stages, with resistors connected from each side of the capacitor to the power supply or to ground.

Procedure :

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (V_{CE} and $I_C = V_{RC} / R_C$)

To find frequency response :

1. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
3. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width.
4. Calculate figure of merit.

To find the input impedance (Zi) :

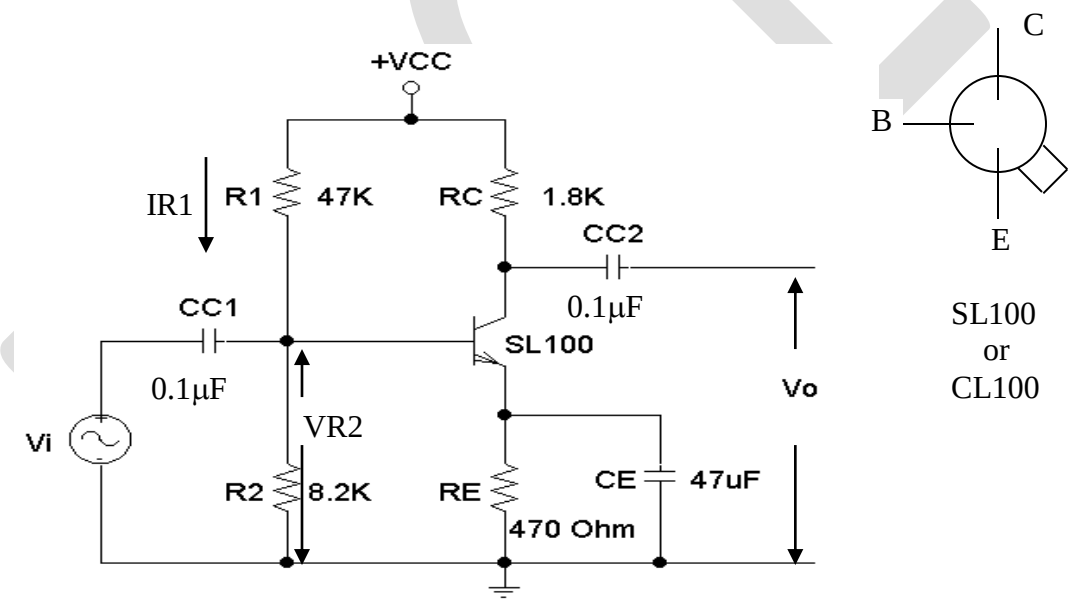
1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

Circuit Diagram :

RC coupled Single stage BJT amplifier :



Design :

Given, **V_{CE} = 5 V** and **I_C = 2 mA** Assume β = 100

$V_{CC} = 2V_{CE} = 2 \times 5 =$ **10 V**

Let V_{RE} = 10% V_{CC} = 1 V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 2mA / 100 = 20\ \mu A$

$R_E = 1 / (2m + 20\mu) = 495\Omega$

Choose **$R_E = 470\ \Omega$**

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (10 – 5 – 1) / 2\ m$

$R_C = 2\ K\Omega$ Choose **$R_C = 1.8\ K\Omega$**

Let $I_{R1} = 10\ I_B = 10 \text{ X } 20\ \mu A = 200\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 1 = 1.6\ V$ (Since transistor is silicon make $V_{BE} = 0.6\ V$)

$R2 = V_{R2} / (I_{R1} – I_B) = 1.6 / (200\ \mu A - 20\ \mu A)$

$R2 = 8.8\ K\Omega$ Choose **$R2 = 8.2\ K\Omega$**

$R1 = (V_{CC} – V_{R2}) / I_{R1} = (10 – 1.6) / 200\ \mu A$

$R1 = 42\ K\Omega$ Choose **$R1 = 47\ K\Omega$**

$X_{CE} << R_E$

$X_{CE} = R_E / 10$

$1 / (2\ \pi\ f\ C_E) = 470 / 10$ Let $f = 100\ Hz$

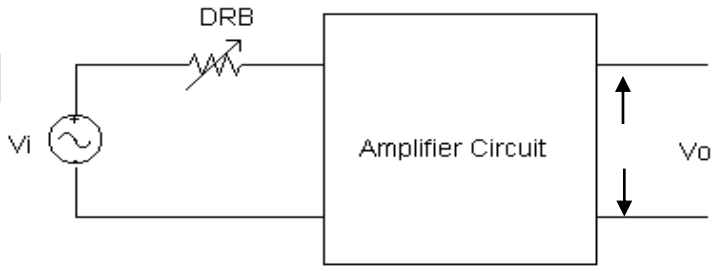
$C_E = 33\ \mu F$ Choose **$C_E = 47\ \mu F$**

Choose **$C_{C1} = C_{C2} = 0.1\ \mu F$**

Tabular Column : Vi = _____ V

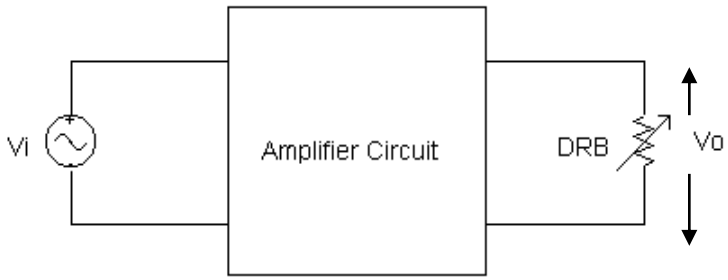
F in Hz	Vo in Volt	AV = Vo / Vi	Gain in dB = 20*log AV

Circuit to find input impedance (Zi) :

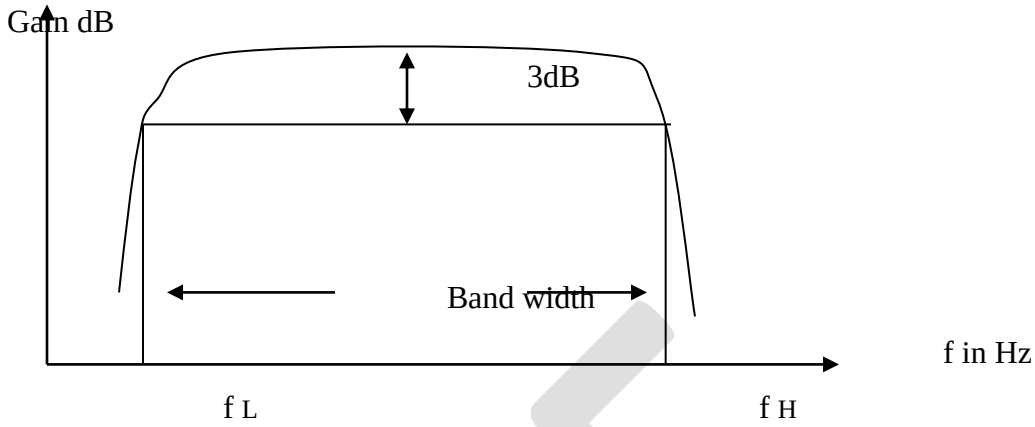


4.

Circuit to find output impedance (Zo) :



Ideal Graph :



f L = Lower cutoff frequency f H = Higher cutoff frequency

Result :

1. Quiescent point : V_{CE} = ____ V, I_C = _____ mA
2. Voltage Gain (AV) = _____ (in mid band region)
3. Bandwidth (BW) = _____ Hz
4. figure of merit (FM = AV * BW) = _____ Hz

Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 7 Date : / / .

RC Coupled Single Stage FET Amplifier

Aim : To conduct an experiment to plot the frequency response of an RC coupled amplifier and to find the input impedance, output impedance and the voltage gain.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	FET BFW 10	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory :

An amplifier is a circuit which increases the voltage, current or power level of i/p signal where the frequency is maintained constant from o/p to i/p signal. In FET amplifier the output current (ID) is a function of input voltage VGS. That is as VGS varies the drain current varies. VGS varies as input signal varies in turn the drain current varies hence amplification takes place.

In RC coupled FET amplifier RD and RS are selected in such a way that FET operates in active region and the operating point will be in the middle of active region. Coupling capacitors CC1 and CC2 are used to block dc current flow through load and the source. The source by-pass capacitor CS is connected to avoid negative feedback.

An amplifier in which resistance-capacitance coupling is employed between stages and at the input and output point of the circuit is known as RC coupled amplifier. A capacitor provides a path for signal currents between stages, with resistors connected from each side of the capacitor to the power supply or to ground.

Procedure :

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (V_{DS} and $I_D = V_{RD} / R_D$)

To find frequency response :

5. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
6. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
7. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width.
8. Calculate figure of merit.

To find the input impedance (Zi) :

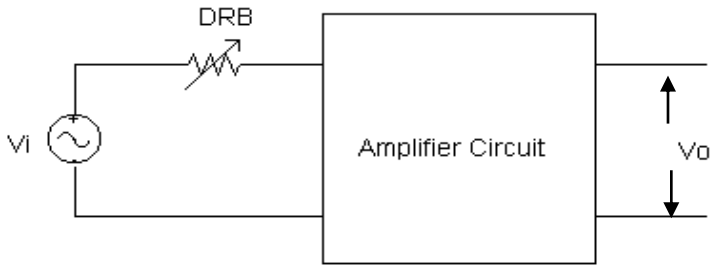
1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

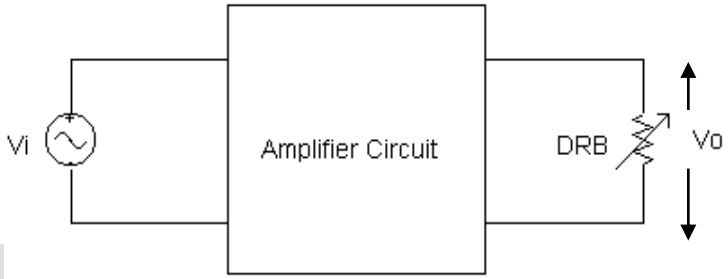
5. Connections are made as shown in the diagram.
6. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.

7. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

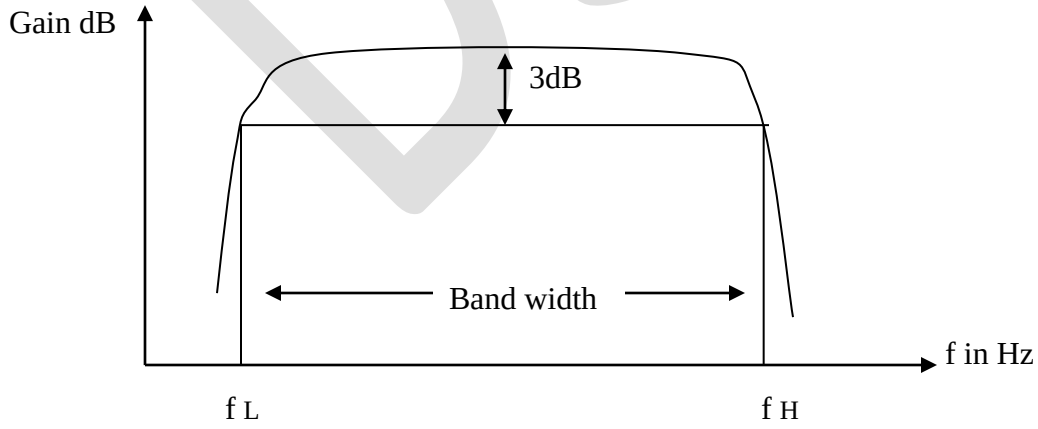
Circuit to find input impedance (Zi) :



Circuit to find output impedance (Zo) :

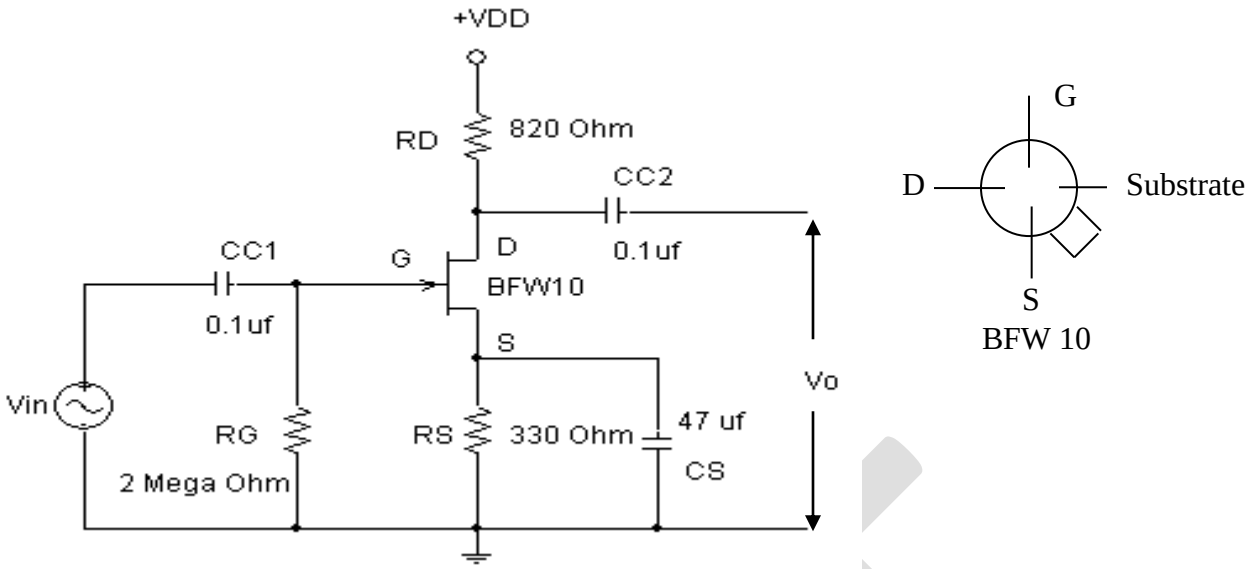


Ideal Graph :



f L = Lower cutoff frequency f H = Higher cutoff frequency

Circuit Diagram :



Design :

Given V_{DD} = 10V, V_{GS}(off) = -4V I_{DSS} (max) = 12mA R_G = 2 MΩ

Formulae

$I_D = I_{DSS}.(1 – V_{GS} / V_{GS}(off))^2$ ----------(1)

When V_G = 0, Then $V_S = -V_{GS}$

But $V_S = I_D . R_S$

When V_G = 0, $I_D = I_{DSS}$

$V_S = I_{DSS}.R_S$

$I_{DSS}.R_S = -V_{GS}$ (off)

R_S = -(-4) / 12mA = 333 Ω

Choose **R_S = 330 Ω**

From (1)

$I_D = I_{DSS}.(1 – I_D.R_S / V_{GS}(off))^2$

$I_D = I_{DSS}.(1 + I_D^2.R_S^2 / 16 - I_D.R_S/2)$

$I_D = 12 \times 10^{-3} \times (1 + I_D^2.330^2 / 16 - I_D.330/2)$

$81.675I_D^2 - 2.98I_D + 12 \times 10^{-3} = 0$

I_D = 4.6 mA or I_D = 31.9 mA

Since I_D cannot be greater than I_{DSS}, Choose I_D = 4.6 mA Assume V_{DS} = 50 % V_{DD}

V_{DS} = 5V

Applying KVL to output circuit

$V_{DD} = I_D . R_D + V_{DS} + I_D . R_S$

$R_D = (10 – 5 – 4.6 \times 10^{-3} \times 330) / 4.6 \times 10^{-3}$

$R_D = 756\ \Omega$

Choose **R_D = 820 Ω**

$X_{CS} << R_S$

$X_{CS} = R_S / 10$

$1 / (2 \pi f C_S) = 470 / 10$ Let f = 100 Hz

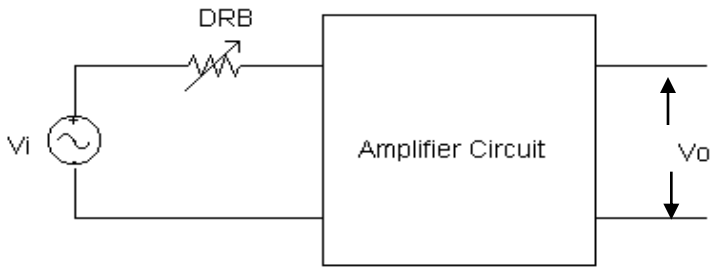
C_S = 33 μF Choose **C_S = 47 μF**

Choose **$C_{C1} = C_{C2}$ = 0.1 μF**

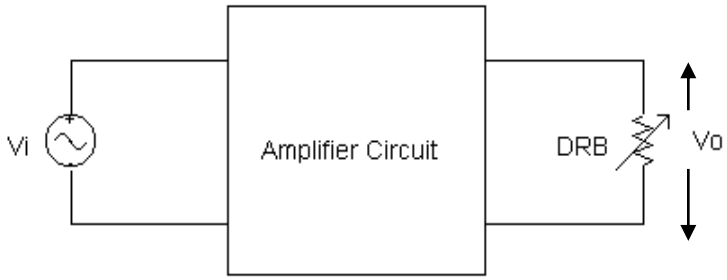
Tabular Column : Vi = _____ V

F in Hz	Vo in Volt	AV = Vo / Vi	Gain in dB = 20*log AV

Circuit to find input impedance (Zi) :



Circuit to find output impedance (Zo) :



Result :

1. Quiescent point : V_{DS} = ____ V, I_D = _____ mA, V_{GS} = _____ V
2. Voltage Gain (AV) = _____ (in mid band region)
3. Bandwidth (BW) = _____ Hz
4. figure of merit (FM = AV * BW) = _____ Hz
5. Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 8 Date : / / .

Darlington Emitter Follower

Aim : To conduct an experiment to plot the frequency response of an Darlington emitter follower amplifier with and without bootstrapping and to find the input impedance, output impedance and the voltage gain.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL 100 and 2N3055	-	1 each
2.	Resistors & Capacitors	As per design	-
3.	Multi meter	-	01
4.	CRO probes	-	3 set
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory :

When high input impedance and low output impedance requirements are to be met the natural choice is common collector configuration the common collector configuration of transistor has high input impedance, low output impedance and high current gain although no phase inversion. The common collector transistor amplifies is termed as emitter follower for the simple reason that the o/p voltage follows the input voltage (AV ≈ 1). The important application of emitter follower is as buffer amplifier for impedance matching. A single stage emitter follower provides an i/p impedance of 500 KΩ. But for the requirement of i/p impedance beyond 500 KΩ we employ Darlington emitter follower. The voltage gain of Darlington Emitter Follower is less than but very nearly equal to unity. The coupling of the two stages of emitter follower amplifier, this cascaded connection of two emitter follower is called Darlington connections. In this connection, since two stages of transistor are connected it improves the current gain and input resistance of the circuit. In Darlington connections of two transistor emitter of the first transistor is directly connected to the base of the second transistor. The

leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high which is not desired. For further high i/p impedance requirement we employ bootstrapping. Bootstrap circuit is an arrangement of components used to boost the input impedance of a circuit by using a small amount of positive feedback, usually over two stages

Procedure : (With and without bootstrapping)

1. Check all the components and equipments for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (VEC2 and IE2 = VRE / RE)

To find frequency response :

1. Connect the AC source. Keeping the frequency of the Ac source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
3. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f L, f H and band width.
4. Calculate figure of merit.

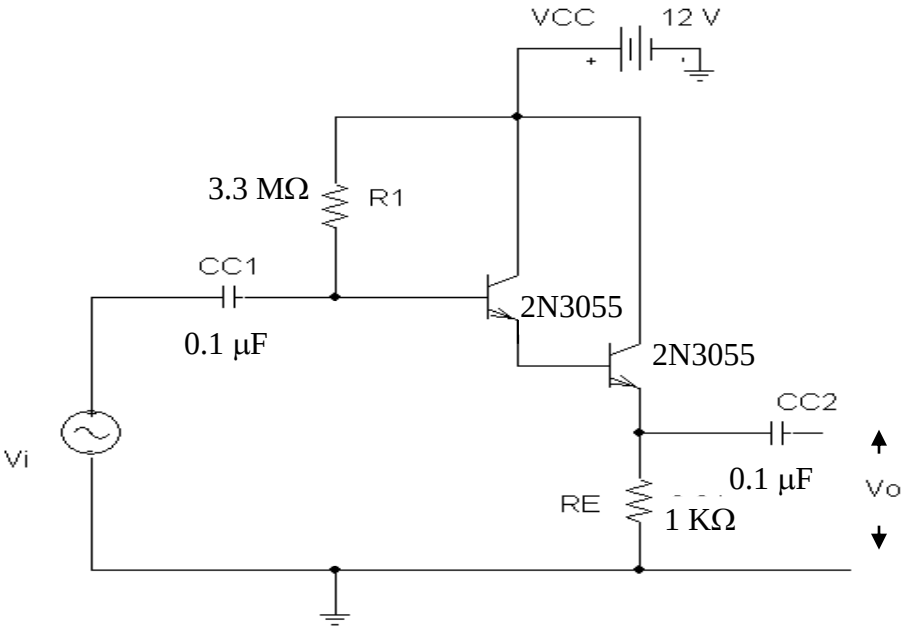
To find the input impedance (Zi) :

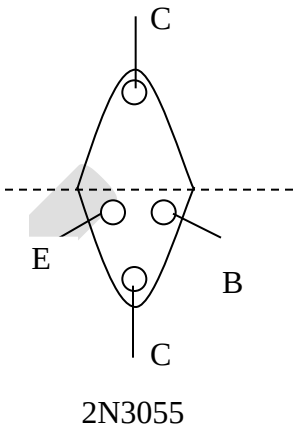
1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

Circuit Diagram : Without boot strapping





Design:

Given V_{CC} = 12 V, I_{E2} = 6mA, $\beta_1 = \beta_2 = 60$

Assume V_{CE} = 50% V_{CC} = 12 / 2 = 6V

$V_E = I_E R_E = V_{CC} - V_{CE} = 6V$

$R_E = 6 / I_E$, $R_E = 1\ k\Omega$,

Choose $\mathbf{R_E = 1\ k\Omega}$

$I_{B2} = I_{E2} / (1 + \beta_2) = 98.36\ \mu A$

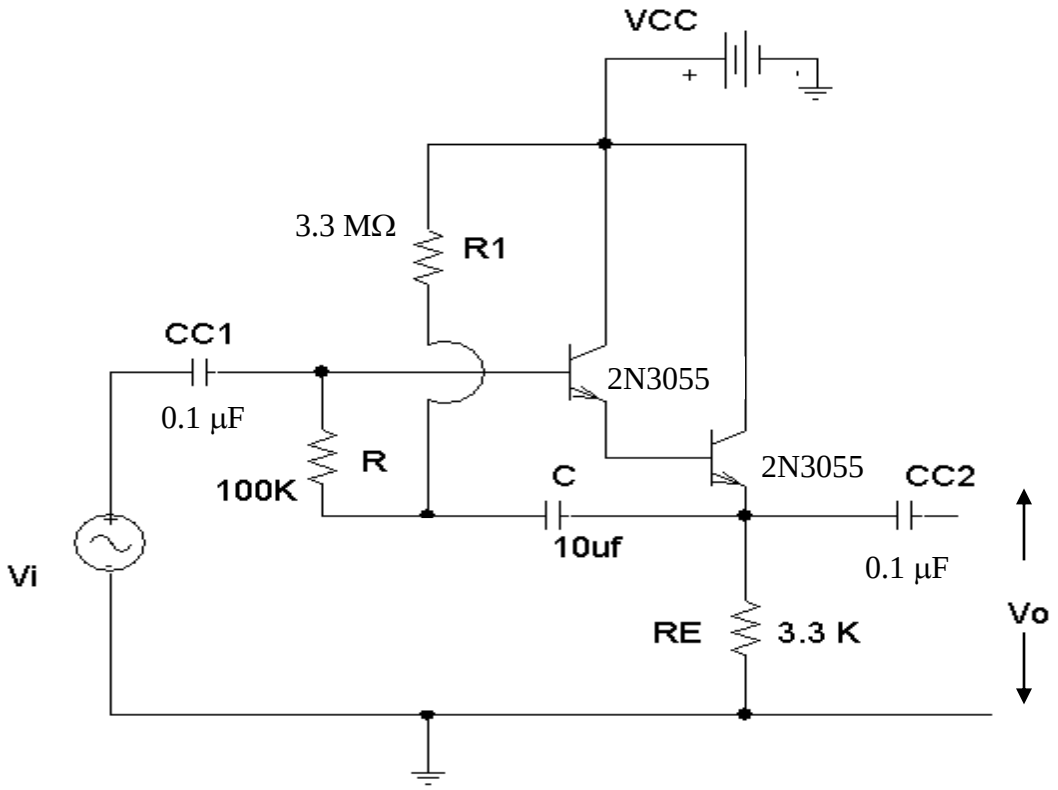
$I_{B1} = I_{E1} / (1 + \beta_1) = I_{B2} / (1 + \beta_1) = 1.61\ \mu A$

$R_B = (V_{cc} - V_{BE1} - V_{BE2} - V_E) / I_{B1}$

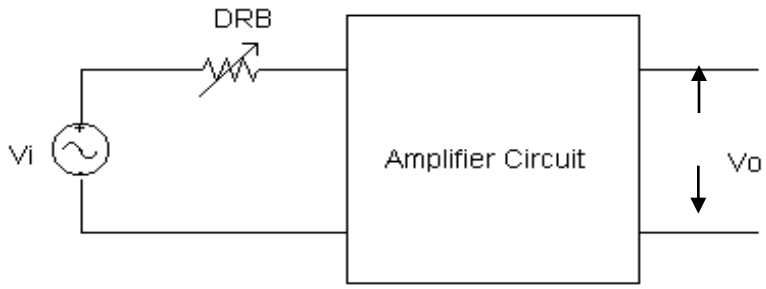
R_B = 2.98 MΩ , Choose **R_B = 3.3 MΩ**

Assume **C_{C1} = C_{C2} = 0.1 µF**

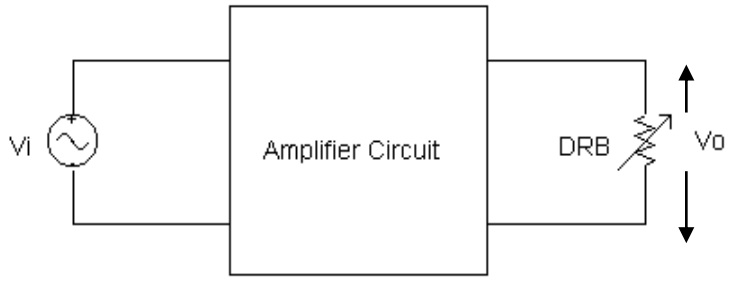
Circuit Diagram : With boot strapping



Circuit to find input impedance (Zi) :



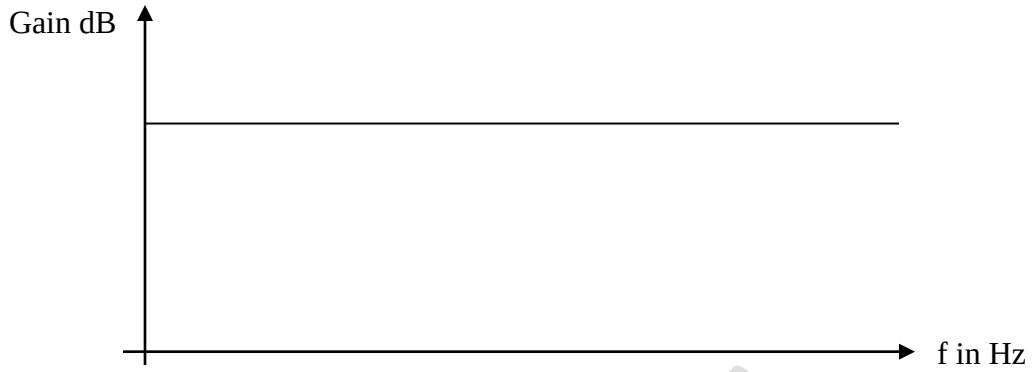
Circuit to find output impedance (Zo) :



Tabular Column : Vi = _____ V

F in Hz	Vo in Volt	AV = Vo / Vi	Gain in dB = 20*log AV

Ideal Graph :



Result :

Without bootstrapping

1. Quiescent point : V_{EC2} = ____ V, I_E = _____ mA,
2. Voltage Gain (AV) = _____ (in mid band region)
3. Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

With bootstrapping

1. Quiescent point : V_{EC2} = ____ V, I_E = _____ mA,
2. Voltage Gain (AV) = _____ (in mid band region)
3. Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 9 Date : / / .

RC Phase Shift Oscillator

Aim : To design and test an RC phase shift oscillator for the given frequency of oscillations.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL 100	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory :

An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave. RC-phase shift oscillator is used generally at low frequencies (Audio frequency). It consists of a CE amplifier as basic amplifier circuit and three identical RC networks for feedback, each section of RC network introduces a phase shift of 60° and the total phase shift by feedback network is 180°. The CE amplifier introduces 180° phase shift hence the overall phase shift is 360°. The feedback factor for an RC phase shift oscillator is 1/29, hence the gain of amplifier (A) should be ≥ 29 to satisfy Barkhausen criteria.

The Barkhausen criteria states that in a positive feedback amplifier to obtain sustained oscillations, the overall loop gain must be unity (1) and the overall phase shift must be 0° or 360°.

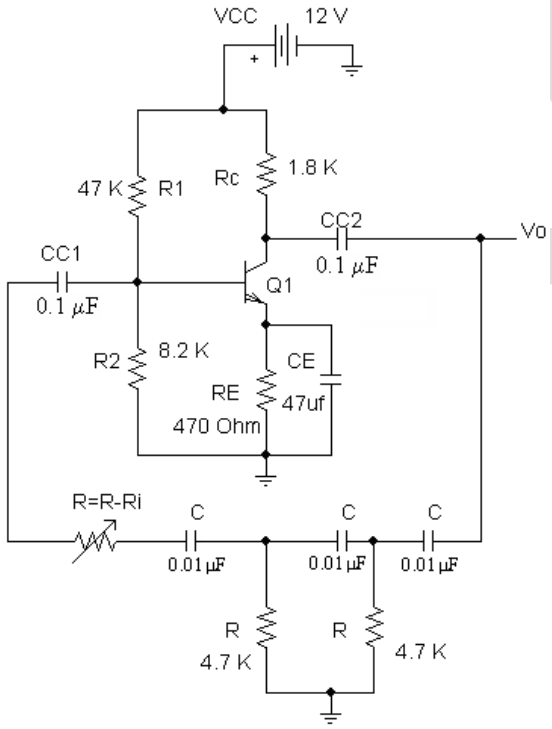
When the power supply is switched on, due to random motion of electrons in passive components like resistor, capacitor a noise voltage of different frequencies will be developed at the collector terminal of transistor, out of these the designed frequency signal is fed back to the

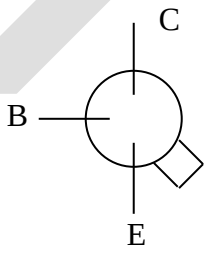
amplifier by the feed back network and the process repeats to give suitable oscillation at output terminal

Procedure :

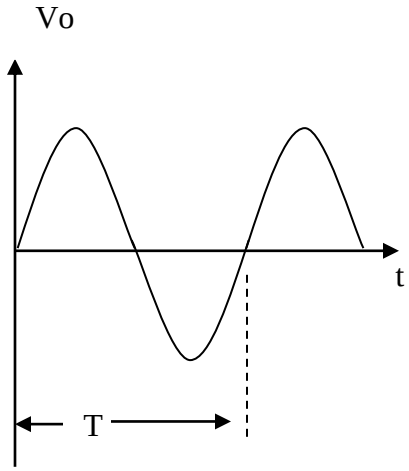
1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the diagram
3. The quiescent point of the amplifier is verified for the designed value.
4. Observe the output wave form on CRO and measure the frequency.
5. Verify the frequency with the designed value.

Circuit Diagram :





SL100
or
CL100



Design :

Given, **V_{CE} = 5 V, I_C = 2 mA** and (Assume β = 100)

$V_{CC} = 2V_{CE} = 2 \times 5 =$ **10 V**

Let V_{RE} = 10% V_{CC} = 1 V

$R_E = V_{RE} / (I_C + I_B)$

fo = 1 / T Hz

$I_B = I_C / \beta = 2mA / 100 = 20\ \mu A$

$R_E = 1 / (2m + 20\mu) = 495\Omega$

Choose **$R_E = 470\ \Omega$**

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (10 – 5 – 1) / 2\ m$

$R_C = 2\ K\Omega$ Choose **$R_C = 1.8\ K\Omega$**

Let $I_{R1} = 10\ I_B = 10 \text{ X } 20\ \mu A = 200\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 1 = 1.6\ V$ (Since transistor is silicon make $V_{BE} = 0.6$ V)

$R2 = V_{R1} / (I_{R1} – I_B) = 1.6 / (200\ \mu A - 20\ \mu A)$

$R2 = 8.8\ K\Omega$ Choose **R2 = 8.2 KΩ**

$R1 = (V_{CC} – V_{R2}) / I_{R1} = (10 – 1.6) / 200\ \mu A$

$R1 = 42\ K\Omega$ Choose **R1 = 47 KΩ**

$X_{CE} << R_E$

$X_{CE} = R_E / 10$

$1 / (2 \pi f C_E) = 470 / 10$ Let f = 100 Hz

$C_E = 33\ \mu F$ Choose **$C_E = 47\ \mu F$**

Choose **$C_{C1} = C_{C2} = 0.1\ \mu F$**

Tank Circuit : Assume fo = 1 kHz

$f_o = 1/[(2 \times \pi \times R \times C (6+4k)^{0.5}]$

where $k = R_c / R$, and $R_i = R_1 \parallel R_2 \parallel h_{ie}$

$4k+23+29/k \leq h_{fe}$

Assume $h_{fe} = \beta = 100$

Therefore $4k+23+29/k = 100$

$4k^2+23k+29 = 100$

$4k^2 – 77k + 29 = 0$

$k = 18.865$ or 0.385

if $k = 18.865$, $R_c / R = 18.865$

R is very small. Therefore proper oscillations are not obtained

Choosing $k = 0.385$

R_c = 1.8 k Ω

R = 4.675 k Ω

Choose R = 4.7 k Ω

C =1/[2 x π x f_o x R (6+4 x 0.385)$^{0.5}$]

C = 0.012 µF

Choose C = 0.01 µF

R_i = 8.2K || 47K || 1.1K

R_i = 0.9 k Ω

R_3 = R – R_i

R_3 = 3.8 k Ω

Result :

Q Point : V_{CE} = _____ V, Ic = _____ MA

fo Theoretical = _____ Hz

fo Practical = _____ Hz

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 10 Date : / / .

Crystal Oscillator

Aim : To design and test a crystal oscillator.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL 100,	-	01
2.	Crystal	1MHz	01
3.	Resistors & Capacitors	As per design	-
4.	CRO Probes	-	3 Set
5.	Multi meter	-	01
6.	DCB	-	02
7.	Spring board and connecting wires	-	-

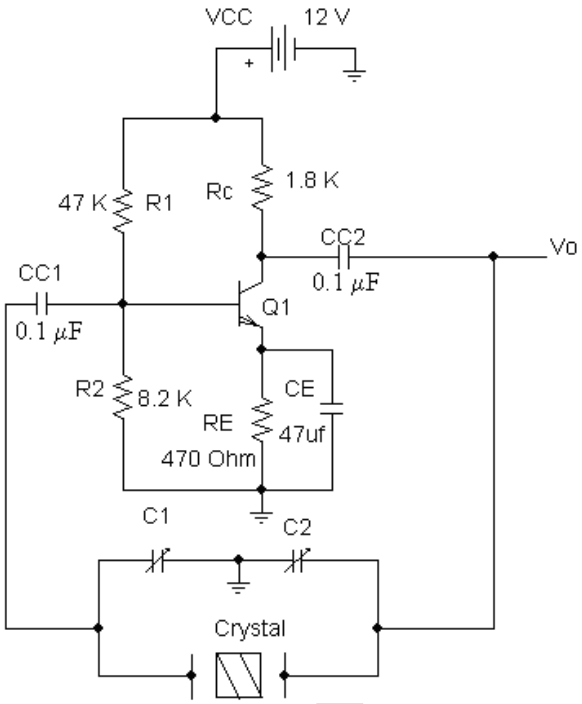
Theory :

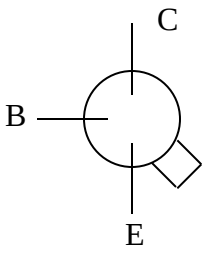
An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave. A **crystal oscillator** is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called "crystal oscillators".

Procedure :

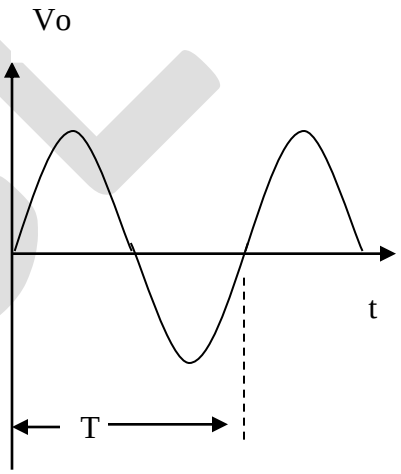
1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the diagram
3. The quiescent point of the amplifier is verified for the designed value.
4. Observe the output wave form on CRO and measure the frequency.
5. Verify the frequency with the crystal frequency.

Circuit Diagram :





SL100
or
CL100



fo = 1 / T Hz

Design :

Given, **V_{CE} = 5 V** and **I_C = 2 mA** Assume β = 100

$V_{CC} = 2V_{CE} = 2 \times 5 =$ **10 V**

Let $V_{RE} = 10\% V_{CC} = 1$ V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 2mA / 100 = 20\ \mu A$

$R_E = 1 / (2m + 20\mu) = 495\Omega$, Choose **$R_E$ = 470 Ω**

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (10 – 5 – 1) / 2\ m$

$R_C = 2\ K\Omega$ Choose **R_C = 1.8 KΩ**

Let $I_{R1} = 10\ I_B = 10 \times 20\ \mu A = 200\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 1 = 1.6$ V (Since transistor is silicon make $V_{BE} = 0.6$ V)

$R2 = V_{R1} / (I_{R1} – I_B) = 1.6 / (200\ \mu A - 20\ \mu A) = 8.8\ K\Omega$ Choose **R2 = 8.2 KΩ**

$R1 = (V_{CC} – V_{R2}) / I_{R1} = (10 – 1.6) / 200\ \mu A = 42\ K\Omega$ Choose **R1 = 47 KΩ**

$X_{CE} << R_E$, $X_{CE} = R_E / 10$

$1 / (2 \pi f C_E) = 470 / 10$

Let f = 1MHz; C_E = 33 µF Choose **C_E = 47 µF**

Choose **$C_{C1} = C_{C2} = 0.1$ µF; C1=C2=0.001µF**

Result :

Q Point : V_{CE} = _____ V, Ic = _____ mA

fo Crystal = _____ Hz

fo Practical = _____ Hz

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 11 Date : / / .

Hartley and Colpitt's Oscillator

Aim : To design and test Hartley and Colpitt's oscillator for the given frequency of oscillations

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	BJT SL 100	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DCB, DIB	-	2 each
6.	Spring board and connecting wires	-	-

Theory :

An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave. The **Hartley oscillator** is an LC electronic oscillator that derives its feedback from a tapped coil in parallel with a capacitor (the tank circuit). A Hartley oscillator is essentially any configuration that uses a pair of series-connected coils and a single capacitor. It was invented by Ralph Hartley.

A **Colpitts oscillator**, named after its inventor Edwin H. Colpitts, is one of a number of designs for electronic oscillator circuits using the combination of an inductance (L) with a capacitor (C) for frequency determination, thus also called LC oscillator. One of the key features of this type of oscillator is its simplicity (needs only a single inductor) and robustness. A Colpitts oscillator is the electrical dual of a Hartley oscillator. Fig. 1 shows the basic Colpitts circuit, where two capacitors and one inductor determine the frequency of oscillation. The feedback needed for oscillation is taken from a voltage divider made by the two capacitors, where in the Hartley oscillator the feedback is taken from a voltage divider made by two inductors (or a tapped single inductor).

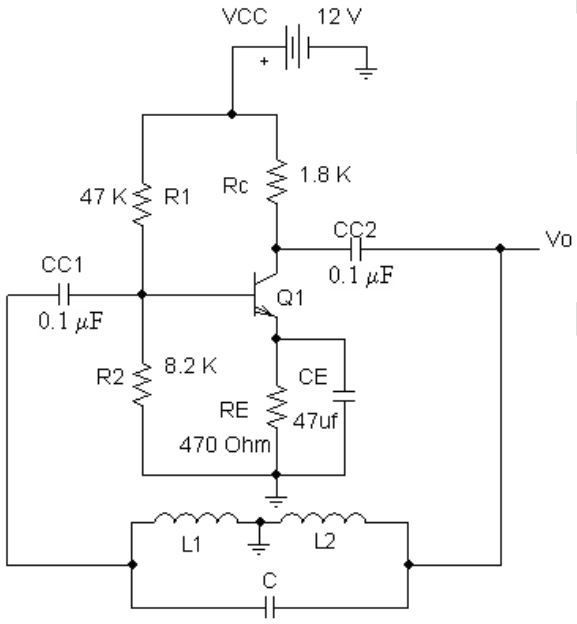
The basic CE amplifier provides 180° phase shift and the feedback network provides the remaining 180° phase shift so that the overall phase shift is 360° to satisfy the Barkhausen criteria. The Barkhausen criteria states that in a positive feedback amplifier to obtain sustained

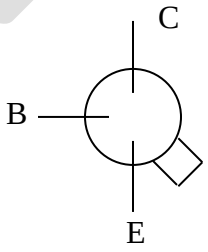
oscillations, the overall loop gain must be unity (1) and the overall phase shift must be 0° or 360°. When the power supply is switched on, due to random motion of electrons in passive components like resistor, capacitor a noise voltage of different frequencies will be developed at the collector terminal of transistor, out of these the designed frequency signal is fed back to

Procedure :

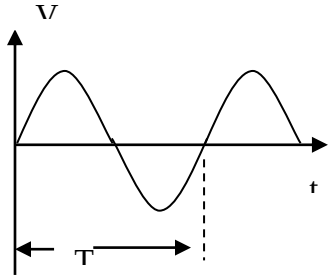
1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the diagram
3. The quiescent point of the amplifier is verified for the designed value.
4. Observe the output wave form on CRO and measure the frequency.
5. Verify the frequency with the crystal frequency.

Circuit Diagram : Hartley Oscillator



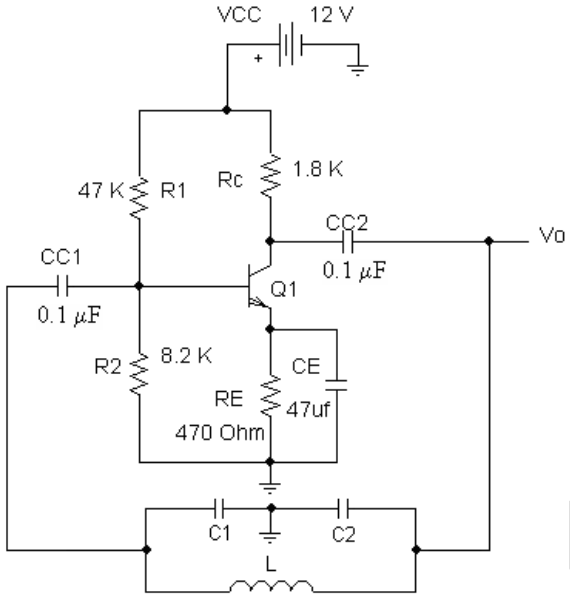


SL100
or
CL100



$f_0 = 1 / T$

Colpitt's Oscillator



Design :

Given, **V_{CE} = 5 V** and **I_C = 2 mA** Assume β = 100

$V_{CC} = 2V_{CE} = 2 \times 5 =$ **10 V**

Let $V_{RE} = 10\% V_{CC} = 1$ V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 2mA / 100 = 20\ \mu A$

$R_E = 1 / (2m + 20\mu) = 495\Omega$, Choose **$R_E$ = 470 Ω**

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (10 – 5 – 1) / 2$ m

$R_C = 2$ KΩ Choose **R_C = 1.8 KΩ**

Let $I_{R1} = 10\ I_B = 10 \times 20\ \mu A = 200\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 1 = 1.6$ V (Since transistor is silicon make $V_{BE} = 0.6$ V)

$R2 = V_{R1} / (I_{R1} – I_B) = 1.6 / (200\ \mu A - 20\ \mu A) = 8.8$ KΩ Choose **R2 = 8.2 KΩ**

$R1 = (V_{CC} – V_{R2}) / I_{R1} = (10 – 1.6) / 200\ \mu A = 42$ KΩ Choose **R1 = 47 KΩ**

$X_{CE} << R_E$, $X_{CE} = R_E / 10$

$1 / (2 \pi f C_E) = 470 / 10$ Let f = 100 Hz

C_E = 33 µF Choose **C_E = 47 µF**

Choose **$C_{C1} = C_{C2} = 0.1$ µF**

Hartley oscillator: Design of tank circuit: Assume fo = 100 kHz

Formula $f_o = 1 / 2\pi \sqrt{(L_T . C)}$

Where $L_T = L_1 + L_2$

Barkhausen's criterion is $A.\beta = 1$

Therefore $\beta = 1/A = L_1 / L_2$

Assume C = 7.45 nF then L=340 µH, Let L_1 = 100 µH and L_2 = 240 µH

Colpitt's oscillator: Design of tank circuit: Assume fo = 100 kHz

Formula $f_o = 1 / 2\pi \sqrt{(C_T . L)}$

Where $C_T = C_1 . C_2 / (C_1 + C_2)$

Barkhausen's criterion is $A.\beta = 1$

Therefore $\beta = 1/A = C_2 / C_1$

Assume L = 358.8 µH , then C= 7.05nf ,Assume C_2 = 0.01 µF , therefore C_1 = 0.024 µF, then the amplifier by the feed back network and the process repeats to give suitable oscillation at output terminal.

Result :

Hartley Oscillator :

Q Point : V_{CE} = _____ V, I_C = _____ mA,

fo Theoretical = _____ Hz, fo Practical = _____ Hz

Colpitt's Oscillator :

Q Point : V_{CE} = _____ V, I_C = _____ mA,

fo Theoretical = _____ Hz, fo Practical = _____ Hz

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 12 Date : / / .

Two Stage Voltage Series Feedback Amplifier

Aim : To conduct an experiment to plot the frequency response of an two stage amplifier with and without feedback and to find the input impedance, output impedance and the voltage gain.

Apparatus Required:

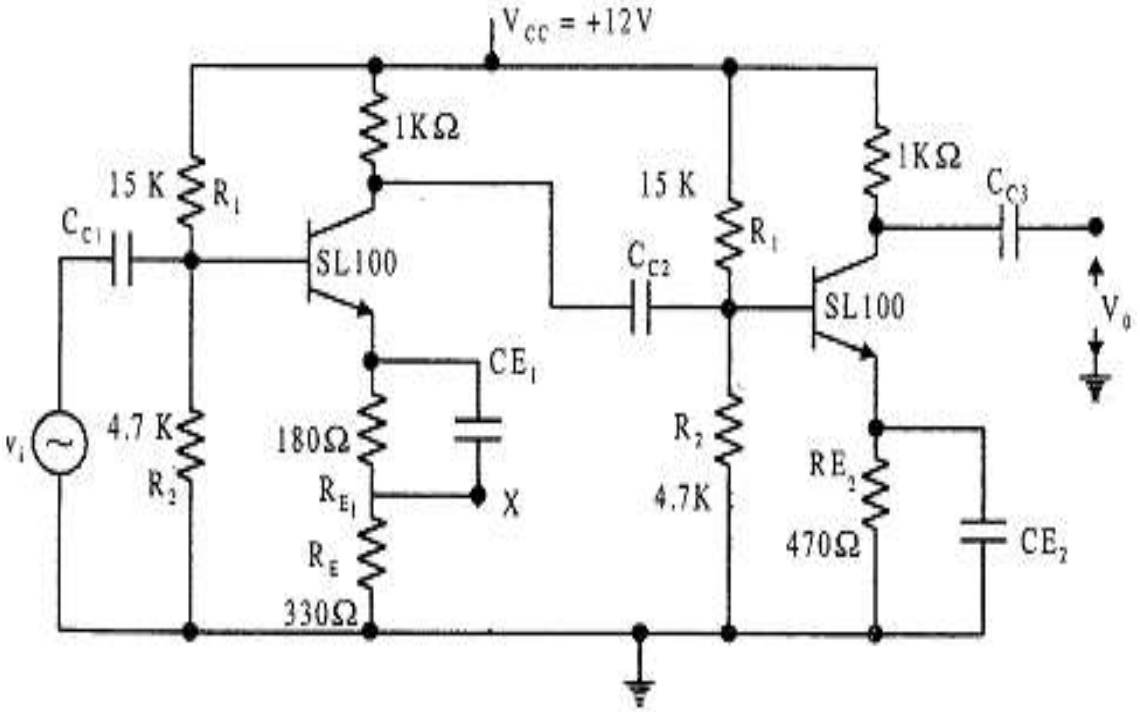
Sl. No.	Particulars	Range	Quantity
1.	SL 100	-	02
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory:

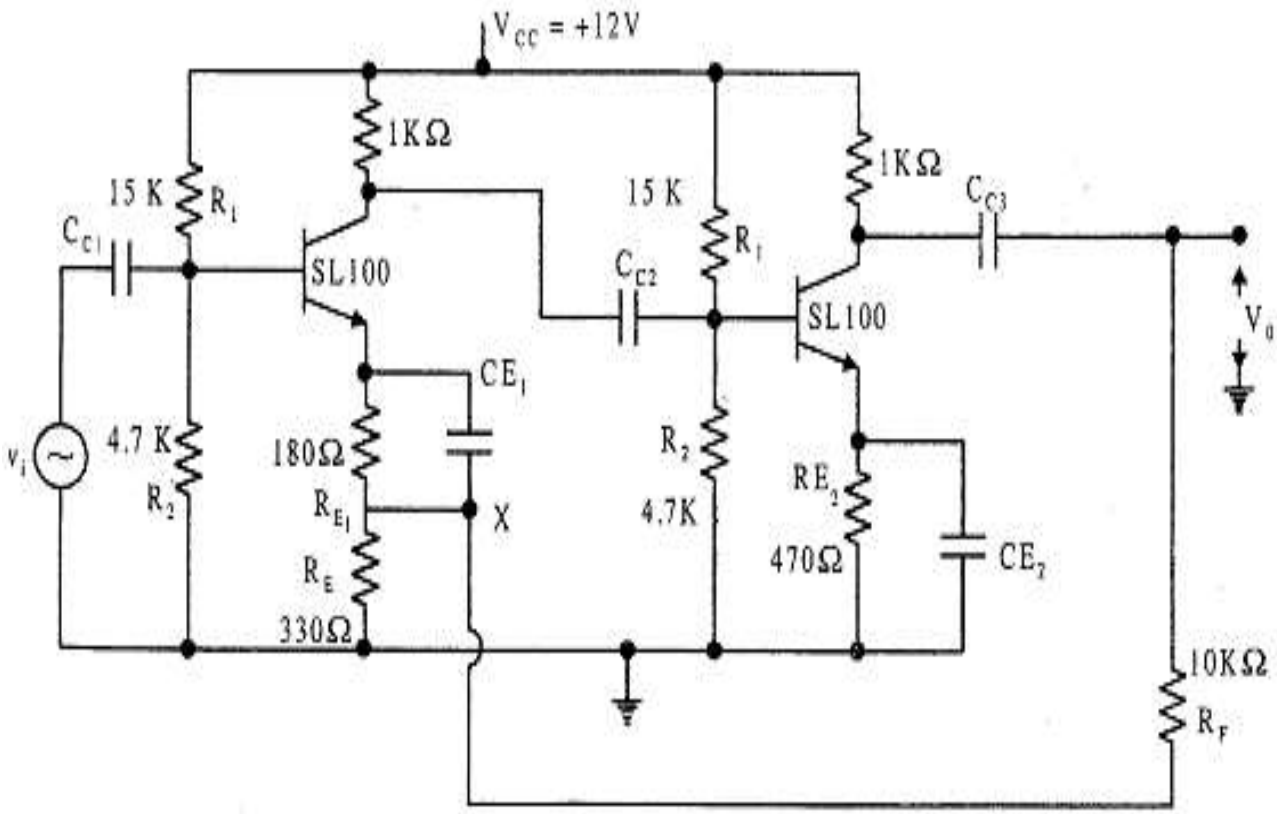
Feedback is the process of combining a portion of output signal with input signal. There are two types of feedback namely positive feedback and negative feedback. If the signal fed back is in phase with the input signal we call it as positive feedback and if the fed back signal is out of phase with the input signal we call it as negative feedback.

Positive feedback is used in oscillators to develop oscillations, whereas negative feedback is used in amplifiers to improve the characteristics of amplifiers. There are four types of feedback concepts name voltage series feedback, current series feedback, voltage shunt feedback and current shunt feedback. In this experiment we discuss voltage series feedback. In voltage series feedback the input impedance will increase, output impedance will decrease, bandwidth increases and distortion decreases which are all advantages but the voltage gain decreases which is a disadvantage which can be improved by cascading with other amplifier

Circuit Diagram : Without feedback



Circuit Diagram : With feedback


V_{CC} = +12V
1KΩ
15 K
R_1
C_{C1}
SL100
C_{C2}
15 K
R_1
1KΩ
C_{C3}
SL100
V_0
CE_1
V_i
4.7 K
R_2
180Ω
R_{E1}
X
R_E
330Ω
R_2
4.7K
RE_2
470Ω
CE_2
10KΩ
R_F

V_i : Signal Generator, V_0 : Measured using CRO,

$R_1 = 15K\Omega$, $R_2 = 4.7K\Omega$, $R_C = 1K\Omega$,

$R_E = 330\Omega$, $R_{E1} = 180\Omega$, $R_{E2} = 470\Omega$,

$R_F = 10K\Omega$, $C_1 = C_2 = 0.47\mu F$, $C_3 = 0.47\mu F$,

$C_{E1} = C_{E2} = 47\mu F$

Design:

Let $V_{CC} = 12V$, $I_C = 4mA$, $V_{CE} = 6V$

Assuming $V_E = \frac{V_{CC}}{6} = \frac{12}{6} = 2V$

Let $C_1 = C_2 = C_3 = 0.47\mu F$ and $C_{E1} = C_{E2} = 47\mu F$

We know that

$$V_E = I_E \times R_E$$

$$R_E = \frac{V_E}{I_E} = \frac{2}{4mA} = 0.500K \quad \text{Since } I_C = I_E$$

Therefore $R_E = 500\Omega$ (Use 470 ohms)

For first stage of the amplifier split R_E into two parts

Therefore $R_E = 330\Omega + 180\Omega(R_{E1})$

Applying KVL to the collector emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

Therefore $$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$R_C = \frac{12-6-2}{4\times10^{-3}} = \frac{4}{4\times10^{-3}} = 1K\Omega$$

Use $R_C = 1K\Omega$

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + 2 = 2.7V$$

Procedure : (Without Feedback)

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (V_{DS} and $I_D = V_{RD} / R_D$)

To find frequency response :

5. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
6. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
7. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width.
8. Calculate figure of merit.
9. Components / Equipment are tested for their good working condition.
10. Connections are made as shown in the circuit diagram.
11. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
12. By disconnecting the AC source measure the quiescent point (V_{DS} and $I_D = V_{RD} / R_D$)

To find frequency response :

13. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
14. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
15. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width.
16. Calculate figure of merit.

To find the input impedance (Zi) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

4. Connections are made as shown in the diagram.
5. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
6. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

$$\frac{2.7}{12} = \frac{R_2}{R_1 + R_2}$$

$$0.225 = \frac{R_2}{R_1 + R_2}$$

$$R_2 = 0.225R_1 + 0.225R_2$$

$$0.775R_2 = 0.225R_1$$

$$R_2 = 0.29R_1$$

$$R_1 = 3.44R_2$$

Let $R_2 = 4.7K\Omega$ therefore $R_1 = 16.18K\Omega$

Use $R_1 = 15K\Omega$

Design of second stage of the amplifier is same as that of the first stage.

Use $R_E = 470\Omega$ (standard value).

Let $C_E = 47\mu F$ (bypass capacitor) for both the sates.

Coupling capacitors $C_1 = C_2 = C_3 = 0.47\mu F$ or $0.1\mu F$.

The feedback factor $\beta = \frac{R'_E}{R_F + R'_E}$

$$R'_E = 330\Omega$$

The feedback resistor R_F should be much greater than R_C. β should be between 0.01 to 0.1.

Let $R_F = 10K\Omega$

$$\beta = \frac{330}{330 + 10,000} = 0.032$$

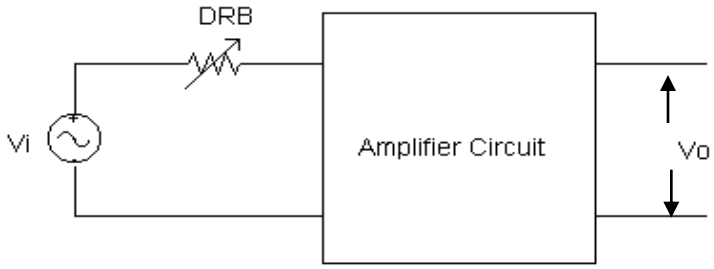
Hence β is within the usual value chosen values of 0.01 to 0.1

Calculations:

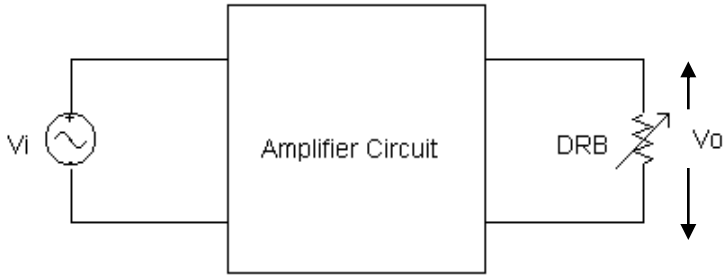
Tabular Column : Vi = _____ V

F in Hz	Without Feedback			With Feedback		
	Vo in Volt	AV = Vo / Vi	Gain in dB = 20*log AV	Vo in Volt	AVf = Vo / Vi	Gain in dB = 20*log AVf

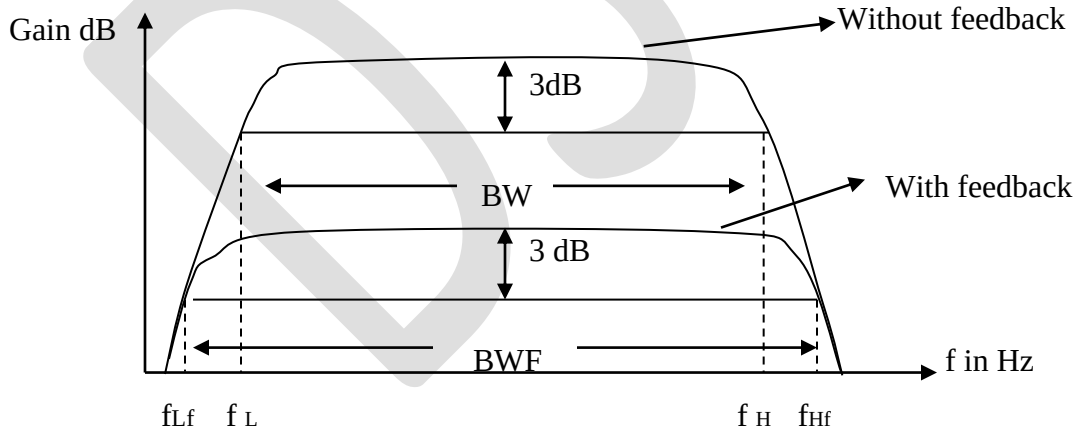
Circuit to find input impedance (Zi) :



Circuit to find output impedance (Zo) :



Ideal Graph :



f L = Lower cutoff frequency f H = Higher cutoff frequency

f Lf = Lower cutoff frequency with feedback f Hf = Higher cutoff frequency with feedback

Result :

With Feedback

1. Quiescent point : V_{DS} = ____ V, I_D = _____ mA, V_{GS} = _____ V
2. Voltage Gain (AV) = _____ (in mid band region)
3. Bandwidth (BW) = _____ Hz
4. figure of merit (FM = AV * BW) = _____ Hz
5. Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

Without Feedback

1. Voltage Gain (AV) = _____ (in mid band region)
2. Bandwidth (BW) = _____ Hz
3. figure of merit (FM = AV * BW) = _____ Hz
4. Input impedance (Zi) = _____Ω, Output Impedance (Zo) = _____Ω

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 13 Date : / / .

Class B Push Pull Power Amplifier

Aim : To determine the efficiency of class B push pull amplifier and to find the optimum load.

Apparatus Required :

Sl. No.	Particulars	Range	Quantity
1.	Transistor AD149 and 2N3055	-	1 each
2.	Resistors as per design	-	-
3.	Mili ammeter	0-20 mA	01
4.	Multimeter	-	01
5.	CRO Probes	-	3 Set
6.	Spring Board and Connecting wires	-	-

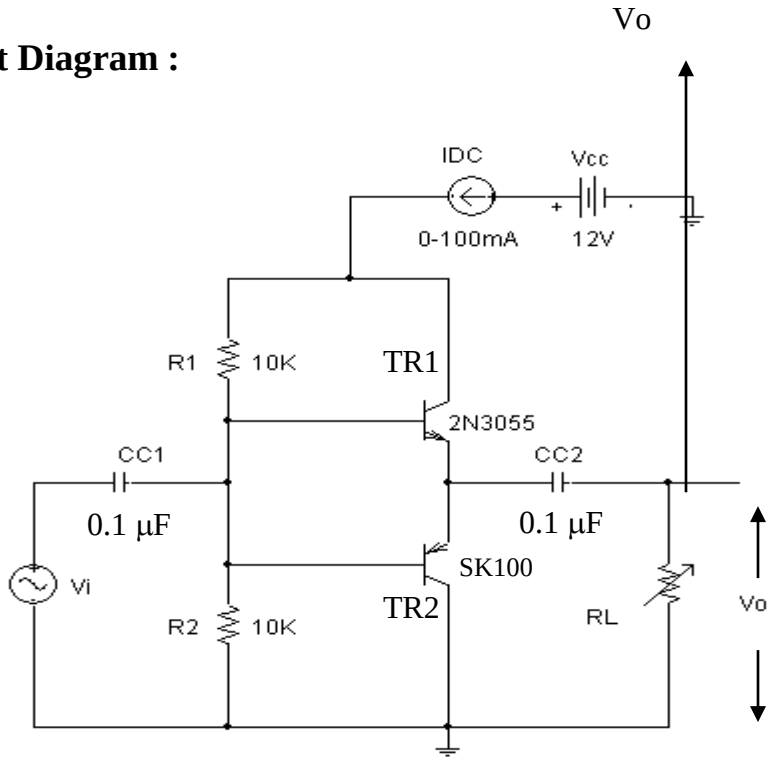
Theory :

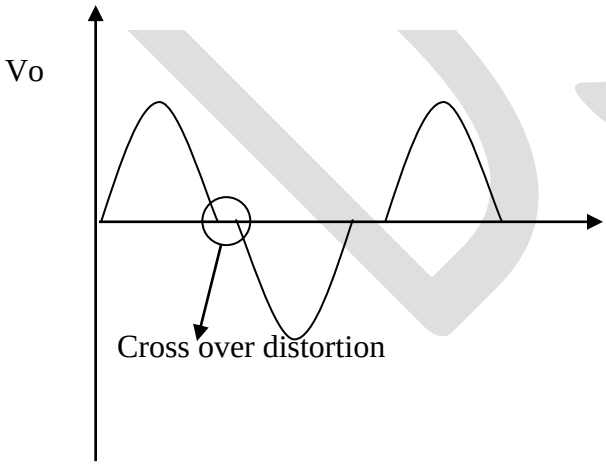
To improve the full power efficiency of the Class A type amplifier it is possible to design the amplifier circuit with two transistors in its output stage producing a "**push-pull**" type amplifier configuration. Push-pull operation uses two "complementary" transistors, one an NPN-type and the other a PNP-type with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or 180^0 of the input waveform while the other transistor amplifies the other half or remaining 180^0 of the waveform with the resulting "two-halves" being put back together at the output terminal. This pushing and pulling of the alternating half cycles by the transistors gives this type of circuit its name but they are more commonly known as **Class B Amplifiers**

The transistor base inputs are in "anti-phase" to each other as shown in circuit diagram, thus if TR1 base goes positive driving the transistor into heavy conduction, its collector current will increase but at the same time the base current of TR2 will go negative further into cut-off and the collector current of this transistor decreases by an equal amount and vice versa. Hence negative halves are amplified by one transistor and positive halves by the other transistor giving this push-pull effect. Unlike the DC condition, these AC currents are **ADDITIVE** resulting in the two output half-cycles being combined to reform the sine-wave which then appears across the

load. **Class B Amplifiers** have the advantage over Class A amplifier so that no current flows through the transistors when they are in their quiescent state (ie, with no input signal), therefore no power is dissipated in the output transistors when there is no signal present

Circuit Diagram :



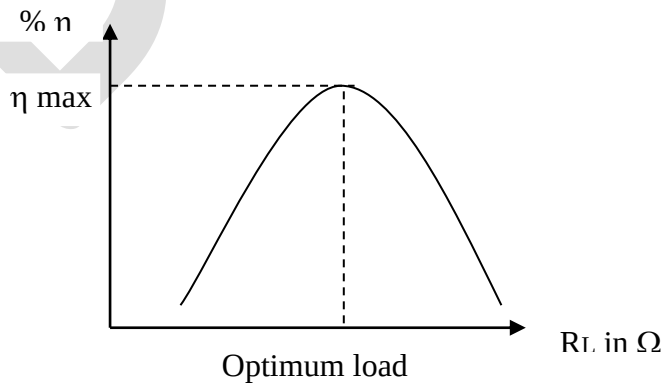


Tabular Column :

Vi = _____ V, V_{CC} = _____ V

Sl. No.	R_L in Ω	Ic in mA	Vo in Volt	Pdc = V_{CC}. I_C	Pac=Vo^2 / 8R_L	% η=Pac / P_{DC}

Ideal Graph :



unlike Class A amplifier stages that require significant base bias thereby dissipating lots of heat - even with no input signal. So the overall conversion efficiency (η) of the amplifier is greater than that of the equivalent Class A with efficiencies reaching as high as 75% possible resulting in nearly all modern types of push-pull amplifiers operated in this Class B mode.

While Class B amplifiers have a much high gain than the Class A types, one of the main disadvantages of class B type push-pull amplifiers is that they suffer from an effect known commonly as Crossover Distortion. This occurs during the transition when the transistors are switching over from one to the other as each transistor does not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs. This is because the output transistors require a base-emitter voltage greater than 0.7v for the bipolar transistor to start conducting which results in both transistors being "OFF" at the same time. One way to eliminate this crossover distortion effect would be to bias both the transistors at a point slightly above their cut-off point. This then would give us what is commonly called an Class AB Amplifier circuit.

Procedure :

1. Connections are made as shown in circuit diagram
2. Keep R_L = 1KΩ, and adjust the amplitude of input signal for distortion less output waveform.
3. RL is varied in convenient steps and corresponding Vo and I_C are recorded.
4. Calculate P_{DC} and Pac and calculate efficiency
5. Plot a graph of %η versus R_L and obtain the optimum load.

Result :

Maximum efficiency = _____ %, Optimum load, R_L opt = _____ Ω

Applications:

Remarks :

Signature of Staff Incharge with date:

Experiment No. : 14 Date : / / .

MOSFET

Aim: To study and plot the MOSFET Characteristics

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	Transistor BS170	-	1
2.	Resistors	as per design	2
3.	Mili ammeter	0-20 mA	01
4.	Multimeter	-	01
5.	CRO Probes	-	3 Set
6.	Spring Board and Connecting wires	-	-

Theory :

MOSFETs are three terminal devices having a source gate and a drain. MOSFET is the abbreviation of Metal Oxide Semiconductor Field Effect Transistor. It uses a thin layer of silicon dioxide as an insulator between the gate and the channel. It is also known as Insulated Gate Field Effect Transistor (IGFET). There are two types of MOSFET, depletion and enhancement types. Consider the N- Channel depletion type MOSFET. Heavily doped two N-Type regions are diffused on a lightly doped P-Type substrate to form source and drain. Between these two N Type wells a lightly doped N-Type material forms a channel. A thin layer of SiO2 which is an insulating material is fabricated on the surface above the channel and the gate terminal is attached to it. Source and Drain terminals are attached to the heavily doped N-Type material with metal contacts. A positive voltage VDS is applied at the drain with respect to source to establish drain current. When a negative voltage VGS Is applied at the gate with respect to the source, positive charges get induced in the channel resulting the channel becoming effectively thinner. This reduces the current flow through the channel. If the magnitude of VGS is increased, the drain current decreases. If a positive voltage is applied at the gate, drain current increases.

Enhancement type MOSFET does not have a channel fabricated in it. The applied positive voltage induces negative charges between the source and drain and a channel forms. BS170 is a

low power enhancement type MOSFET. Some MOSFETS are able to function in Enhancement and Depletion modes.

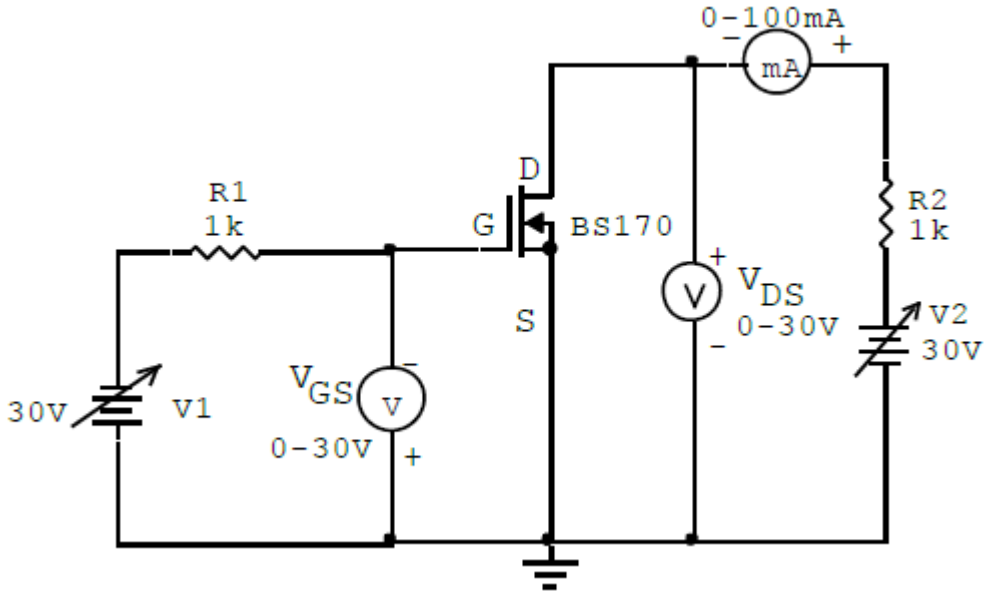
Procedure (Drain Characteristics):

1. Setup the circuit
2. Keep VGS at 0v. Vary VDS in equal steps and note down ID. Repeat it for values of VGS, 2V and 4V.
3. Reverse the polarity of VGS and the voltmeter measuring it. Note down ID for negative values of VDS, -2V and -4V. Plot a graph with VDS along x axis and ID along y axis.

Procedure (Mutual Characteristics):

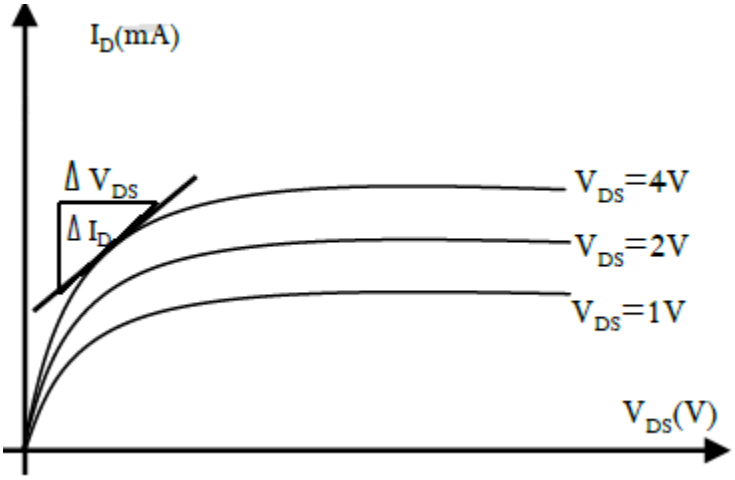
Fix VDS at 10V. Note down drain current ID for various values of VGS. Plot a graph with VGS along x axis and ID along y axis.

Circuit Diagram:



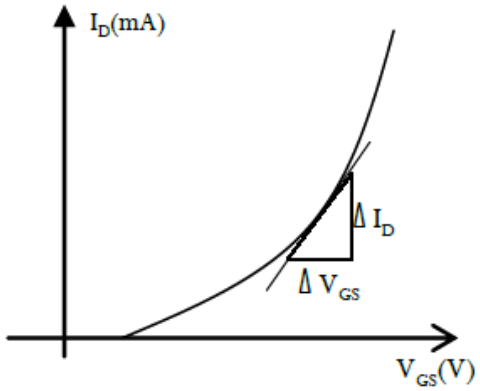
Drain characteristics:

V_{GS} = 1V		V_{GS} = 2V		V_{GS} = 4V	
V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D



Mutual Characteristics:

V_{DS} = 5V		V_{DS} = 10V	
V_{GS}	I_D	V_{GS}	I_D



Result :

Applications:

Remarks :

Signature of Staff Incharge with date:

Viva Questions

Clipping circuits:

1. List the types of clipping circuits?
2. What are the uses of clipping circuits?
3. What is transfer function?
4. Why the shapes of the transfer function and dynamic characteristics of a diode circuit same?
5. What is the piecewise linear diode model? What is its significance?
6. Explain the equivalent circuits of an ideal diode and practical diode.
7. What determines the slope in any part of the transfer function?

Clamping circuits:

1. What are clamping circuits? What are its uses?
2. What are the different types of clamping circuits?

Rectifiers and Filters

1. Define rectifier.
2. Compare different type of rectifiers.
3. What is PIV of diode.
4. What are the different types of filters.

Verification of Theorems

1. Define Thevinin's theorem.
2. Define maximum power transfer theorem.
3. State and prove Thevenin's and maximum power transfer theorem

Series and parallel resonance circuits

1. Compare series and parallel resonance circuits.

RC Coupled amplifier:

1. Define gain of the amplifier
2. What are the functions of the three resistances R_1 , R_2 , R_e?

3. What are the functions of the capacitances C_E and C_C ?
4. Explain the Thevenin's model of the voltage divider bias network
5. How can a transistor be operated as a switch?
6. Which configuration of a transistor is preferred when a transistor is used as a switch.
7. What is quiescent point?
8. What is load line?
9. Why is the Q – point always at the centre of the load line?
10. Why are the coupling capacitors used?
11. Why are there 2 circuits namely the biasing circuit and amplifier circuit?
12. Explain why the frequency response is as it is shown?
13. Explain why only a 3dB bandwidth is chosen?
14. What is early effect?
15. Compare FET with BJT.

FET RC Coupled amplifier:

1. What is a FET?
2. How the FET is a voltage controlled device?
3. Why the FET is called so?
4. What is Gate - Source Cutoff voltage?
5. What are the types of FET?
6. Which type of FET is BFW 10?
7. What are the advantages of FET over BJT?
8. What is pinch off voltage?

Darlington emitter follower:

1. Why the Darlington emitter follower is called so?
2. What are the advantages of the Darlington emitter follower?
3. Where is the Darlington emitter follower used?
4. Why is the emitter follower said to be in the common collector configuration?
5. What are the features of the emitter follower
6. Explain the advantage bootstrapping.

RC phase shift oscillator:

1. Explain the function of the tank circuit.
2. What is the magnitude of the phase change due to the tank circuit?
3. What is Barkhausen's criterion and how is it satisfied?
4. How can the frequency of oscillations be altered?

Hartley and Colpitts oscillator

1. Explain how oscillations are obtained by the tank circuit.
2. Explain how barkhausen's criterion is satisfied.
3. Application of Tuned Circuits
4. Explain the working of tuned circuits.

Voltage Series feedback amplifier:

1. What are the different types of feedback amplifiers?
2. What are the advantages of feedback?
3. What type of amplifier is used in voltage series feedback amplifier?
4. What are the different types of feedback?
5. How is the gain affected when feedback is used?
6. How is the stability of a system affected when used with feedback?
7. What is desensitivity factor?
8. Why is there an increase in the immunity to noise and sensitivity of the amplifier when feedback is used?

Class B Push Pull Amplifier

1. Define different types of amplifiers based on selection of operating point.
2. What are the advantages and disadvantages of Class B push pull amplifier.

MOSFET

1. Explain the construction of MOSFET
2. What is the difference between Enhancement and Depletion type MOSFET
3. Explain the Mutual and transfer characteristics of MOSFET.

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