Example 1.16.1 *Sketch the output for the given circuit assuming ideal diode.*

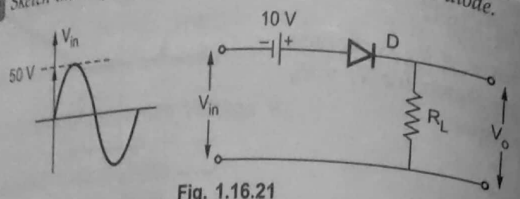


Fig. 1.16.21

Solution : Due to 10 V battery, the diode is forward biased when $V_{in} = 0$. Not only this but as long as $V_{in} > -10$ V, the diode D is forward biased and the circuit is as shown in the Fig. 1.16.21 (a). Applying KVL to loop.

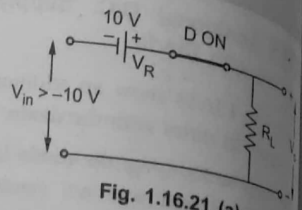


Fig. 1.16.21 (a)

$$+10 - V_o + V_{in} = 0 \quad \text{i.e.} \quad V_o = V_{in} + 10$$

Hence when $V_{in} = 0$ V, $V_o = 10$ V and when $V_{in} = 50$ V, $V_o = 60$ V.

When $V_{in} < -10$ V, the diode D is reverse biased and circuit becomes open. Hence $V_o = 0$ V. Hence the input and output waveforms are shown in the Fig. 1.16.21(b).

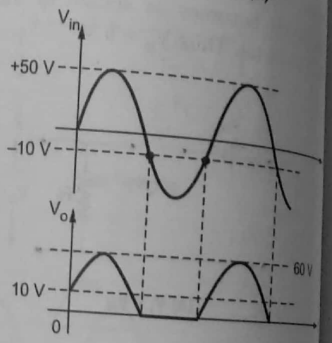


Fig. 1.16.21 (b)

Example 1.16.2 *Sketch the waveform of V_o for the circuit shown in the Fig. 1.16.22.*

Feb.-09, Marks 8

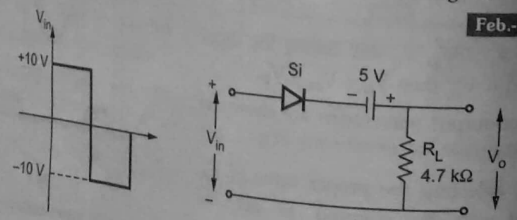


Fig. 1.16.22

Solution : For $V_{in} = +10$ V, the diode is forward biased and circuit reduces as shown in the Fig. 1.16.23.

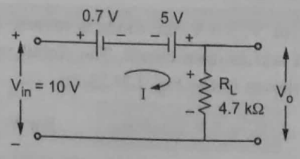


Fig. 1.16.23

$$-0.7 + 5 - V_o + 10 = 0$$

$$\therefore \quad V_o = 14.3 \text{ V}$$

For $V_{in} < -5$ V, the diode will become reverse biased and the output will be zero as no current flows through diode.

Hence the output waveform is shown in the Fig. 1.16.24.

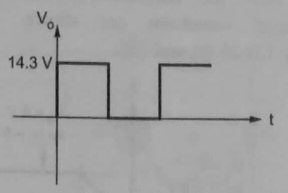
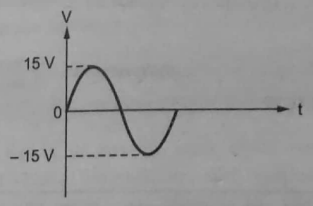


Fig. 1.16.24

Example 1.16.3 *Analyse the clipper circuit of Fig. 1.16.25 and draw its output waveform and transfer characteristic curve.*

Aug.-06



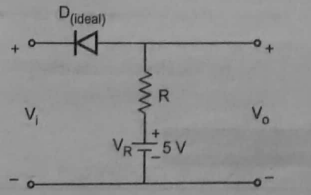


Fig. 1.16.25

Solution : When $V_i < V_R = 5$ V, the diode becomes forward biased and acts as short circuit. The circuit reduces as shown in the Fig. 1.16.25 (a).

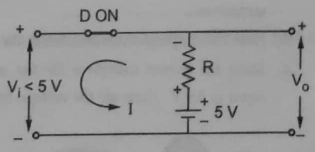


Fig. 1.16.25 (a)

Applying KVL

$$-IR - V_i + 5 = 0$$

$$\therefore \quad I = \frac{5 - V_i}{R}$$

$$\therefore \quad V_o = 5 - I \times R = 5 - \frac{(5 - V_i)}{R} \times R$$

$$\therefore \quad \boxed{V_o = V_i} \qquad \text{... For } V_i < 5 \text{ V}$$

For $V_i > 5$ V, the diode is reverse biased and acts as open circuit. The circuit reduces as shown in the Fig. 1.16.25 (b).

$\therefore$ $V_o = 5$ V Constant ... For $V_i < 5$ V

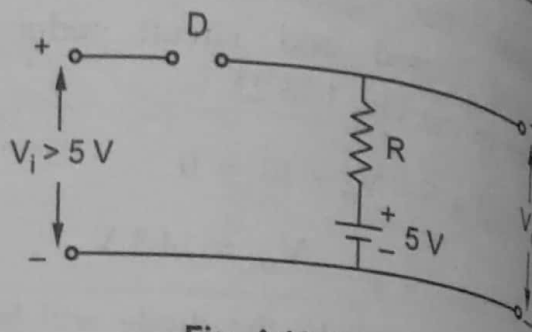
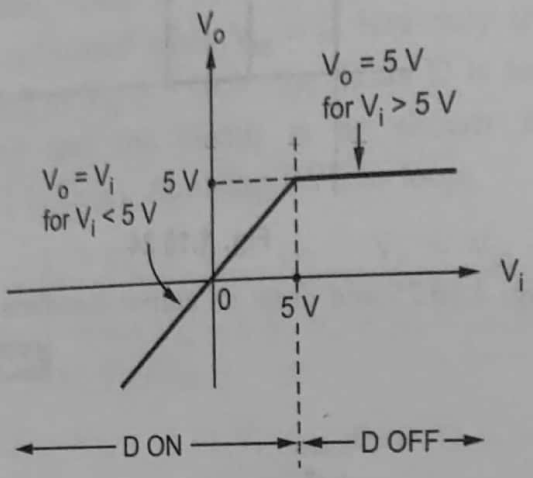
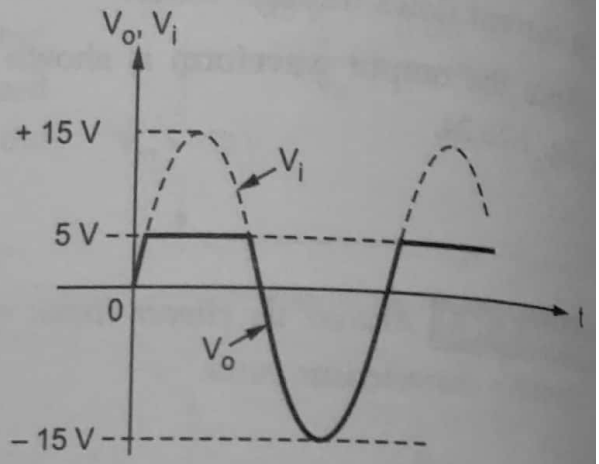


Fig. 1.16.25 (b)

Thus the transfer characteristics and output waveform are shown in the Fig. 1.16.25 (c) and (d).



(c) Transfer Characteristics



(d) Waveforms

Fig. 1.16.25

Review Questions

1. *Draw the circuit of series negative clipper and explain its operation with the help of relevant waveforms.*
2. *Draw the circuit of series positive clipper and explain its operation with the help of relevant waveforms.*
3. *How the clipping above and below the reference level is achieved in series clippers ?*
4. *Show the output waveform for the network shown in the Fig. 1.16.26, if the peak value of a.c. input is 15 V. Show all the voltage levels in the output.*

[Ans. :

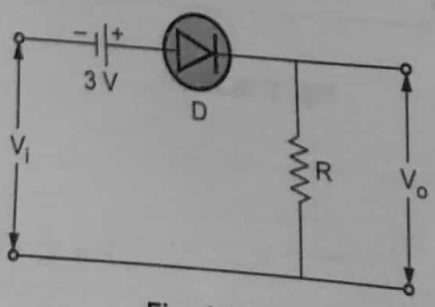


Fig. 1.16.26

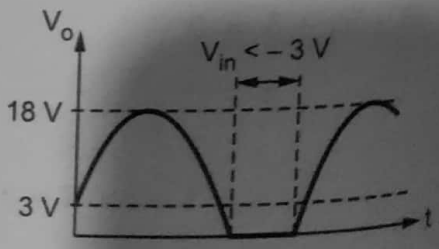


Fig. 1.16.26 (a)

Example 1.17.2 *The Fig. 1.17.26 shows the circuit diagram of a parallel clipper, in which V_R is added in such a way that it opposes the diode drop V_D. Assuming $V_D = 0.7\,V$ analyse the circuit and sketch output waveform and transfer characteristics.*

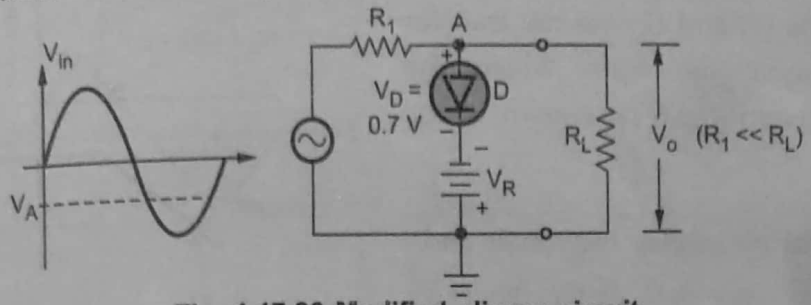


Fig. 1.17.26 Modified clipper circuit

Solution : The drop across the diode is 0.7 V in the forward biased state.

Now $V_A = -V_R + 0.7$

And as $-V_R$ is more negative than 0.7, the overall reference clipping level V_A becomes negative.

So as long as $V_{in} > -V_R + 0.7$, the diode is forward biased and the output voltage $V_o = V_A$.

$$\therefore \quad V_o = V_A = -V_R + 0.7 \quad \ldots V_{in} \geq V_A \qquad \ldots (1)$$

When V_{in} is less than V_A, the diode becomes reverse biased and acts as an open circuit. And output is same as input assuming $R_1 << R_L$.

$$\therefore \quad V_o = V_{in} \ldots V_{in} < V_A \qquad \ldots (2)$$

Key Point *As $(-V_R + 0.7)$ is negative, not only the positive half cycle of the input gets clipped but part of negative half cycle up to level of V_A gets clipped.*

This is shown in the Fig. 1.17.27.

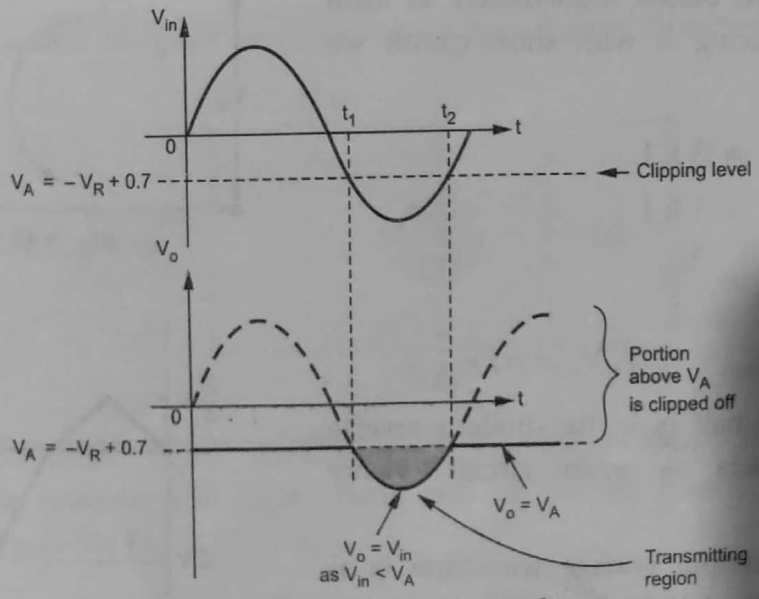


Fig. 1.17.27 Input-output waveforms

The shaded portion is the transmitting region.

The equations (1) and (2) are the transfer characteristic equations, from which the transfer characteristics can be shown in the Fig. 1.17.28.

Key Point *Thus by varying magnitude and direction of V_R, any part of the input is clipped off as per the requirement.*

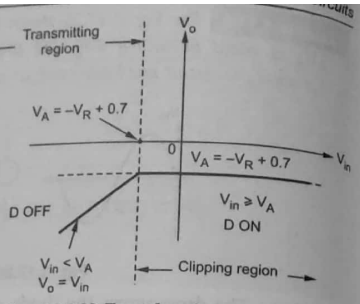


Fig. 1.17.28 Transfer characteristics

Example 1.17.3 *Assuming ideal diode in the circuit shown in the Fig. 1.17.29, draw the output voltage for the given input signal.* **March-01, Jan.-07, Marks 8**

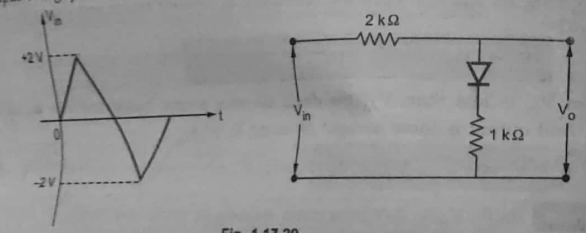


Fig. 1.17.29

Solution : *For positive half cycle, the diode becomes forward biased immediately as ideal diode. So replacing it with short circuit we get,*

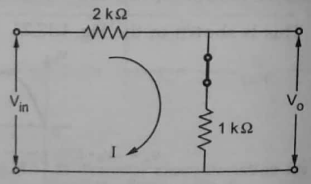


Fig. 1.17.29 (a)

$\therefore \quad V_{in} = 3\ k\ I$

and $\quad V_o = 1\ k\ I$

$\therefore \quad V_o = \frac{V_{in}}{3}$

Hence for $(V_{in})_{max} = +2$ V, $V_o(max) = \frac{2}{3}$ V.

For negative half cycle, the diode is reverse biased and acts as open circuit. Hence $V_o = V_{in}$.

Hence the output voltage waveform is as shown in the Fig. 1.17.29 (b).

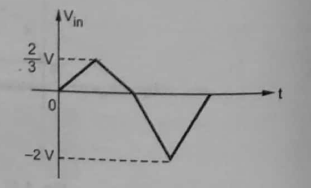


Fig. 1.17.29 (b)

Example 1.17.4 *Sketch the output waveform V_o for the circuit shown in the Fig. 1.17.30. Assume ideal diode.*

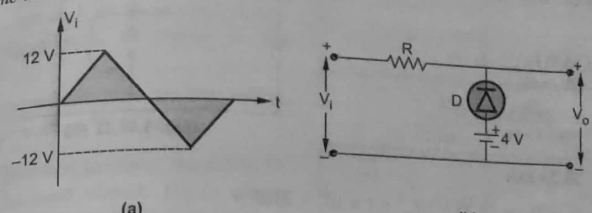


Fig. 1.17.30

Solution : This is a shunt clipper. Now the reference voltage V_{BIAS} is 4 V. When V_i is greater than 4 V, the diode is reverse biased and the output is equal to V_i. But when V_i is less than 4 V, the diode is forward biased and the output is equal to V_R to 4 V. Hence the output waveform can be shown as in Fig. 1.17.31.

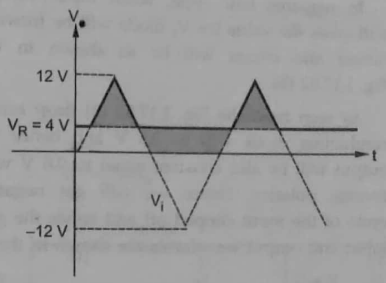


Fig. 1.17.31

Example 1.17.5 *Analyze the given circuit and sketch the nature of its output voltage.*

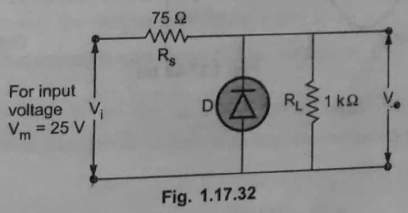


Fig. 1.17.32

Assume silicon diode with cut-in voltage of 0.6 V.

Solution : In the positive half cycle, diode will be reverse biased. And circuit will become as shown in the Fig. 1.17.32 (a).

So, output will follow the input waveform.

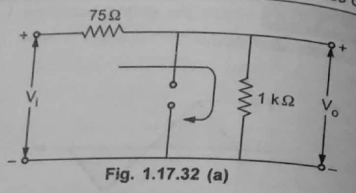


Fig. 1.17.32 (a)

$$I_m = \frac{(V_i)_m}{(R_s + R_L)} = \frac{25}{(75+1\times10^3)}$$

$$= 23.25 \text{ mA}$$

$$\therefore (V_o)_m = I_m \times R_L = 23.25 \times 10^{-3} \times 1 \times 10^3 = 23.25 \text{ V}.$$

$\therefore$ Peak value of output voltage will be 23.25 V.

In negative half cycle, when input voltage will cross the value 0.6 V, diode will be forward biased and circuit will be as shown in the Fig. 1.17.32 (b).

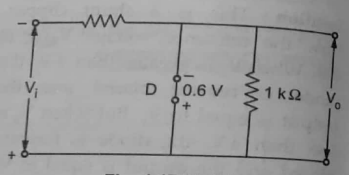


Fig. 1.17.32 (b)

As seen from the Fig. 1.17.32 (b) drop across conducting diode will be 0.6 V and hence the output will be also constant equal to 0.6 V with reverse polarity. Hence we will get negative cycle of the input clipped off and hence the given circuit is negative clipper circuit. The input and output waveforms are shown in the Fig. 1.17.32 (c).

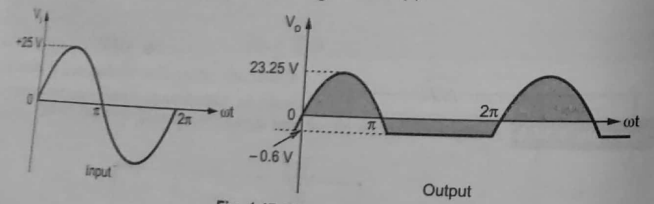


Fig. 1.17.32 (c)

Example 1.17.6 *For the clipper circuit shown in the Fig. 1.17.33, the input is 50 sin ωt. Draw the transfer characteristics and input-output waveforms, assuming ideal diodes.*

Feb.-10, Marks 10

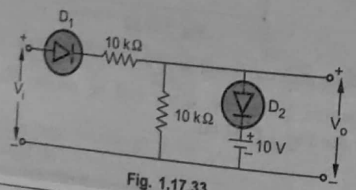


Fig. 1.17.33

Solution : When V_i is less than 0 i.e. negative, both the diodes D_1 and D_2 are reverse biased and act as an open circuit. The circuit reduces as shown in the Fig. 1.17.33 (a).

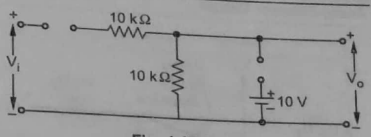


Fig. 1.17.33 (a)

No current can flow in the circuit. The output voltage V_o is zero.

As V_i becomes positive, the diode D_1 becomes forward biased. Hence circuit becomes as shown in Fig. 1.17.33 (b).

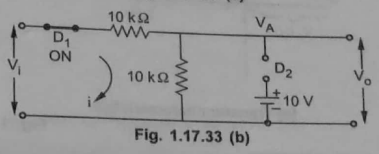


Fig. 1.17.33 (b)

But for D_2 to be ON, V_A must be greater than 10 V. But $V_A = V_o$ i.e. for D_2 ON V_o must be greater than 10 V.

Now under this condition,

$$i = \frac{V_i}{(10+10)\times 10^3}$$

$$\therefore \quad V_o = 10\times10^3 \times \frac{V_i}{20\times 10^3} = \frac{V_i}{2} \quad \therefore \quad V_i = 2\,V_o$$

When V_o = 10 V, D_2 is forward biased i.e. when V_i is 2 V_o i.e. 20 V D_2 is forward biased. Thus both D_1 and D_2 are forward biased for V_i greater than 20 V. The circuit becomes as shown in Fig. 1.17.33 (c).

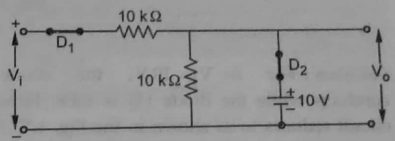


Fig. 1.17.33 (c)

It can be seen that when both the diodes are forward biased, the output is constant equal to 10 V.

Thus the transfer characteristic equations can be written as,

$$V_o = 0, \qquad \text{for } V_i < 0$$

$$V_o = \frac{V_i}{2}, \qquad \text{for } 0 < V_i < 20 \text{ V}$$

$$V_o = 10 \text{ V}, \qquad \text{for } V_i > 20 \text{ V}$$

The transfer characteristics can be shown as in the Fig. 1.17.34 (a) while the input-output waveforms can be shown as in the Fig. 1.17.34 (b).

1.20.5 Clamper Application

The clamper circuits are often used in the television receivers as d.c. restorer. The video signal in television is processed through capacitively coupled amplifiers hence the signal losts its d.c. component which effectively loses black and white reference levels and the blanking level. Hence it is necessary to restore these levels back before applying signal to the picture tube. This is done by a clamper circuit acting as a d.c. restorer. This is shown in the Fig. 1.20.14.

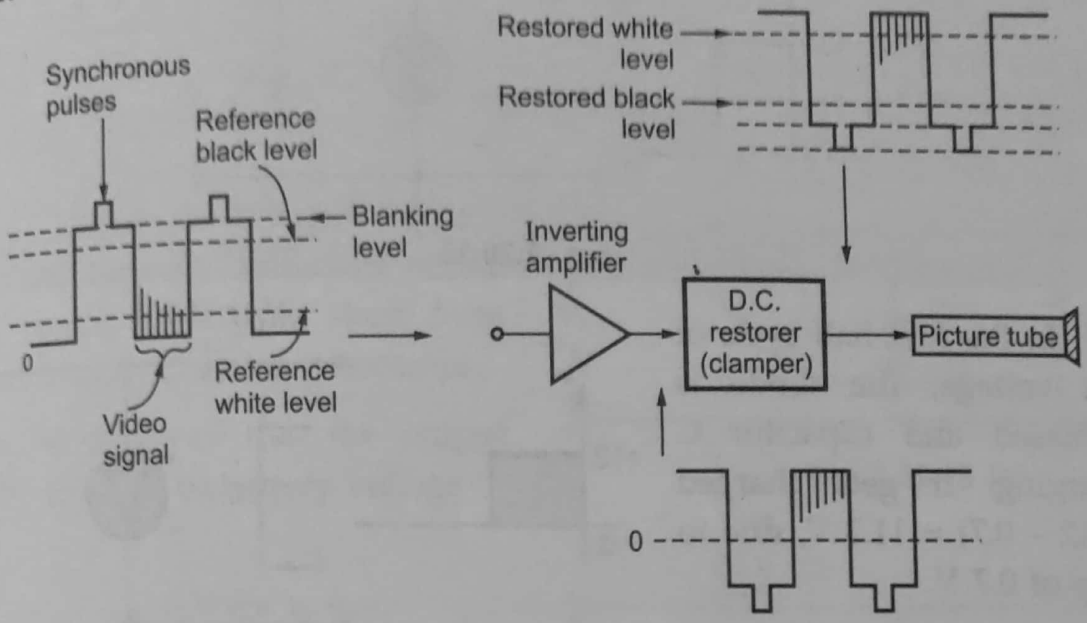


Fig. 1.20.14 Use of clamper circuit in television receiver

Example 1.20.1 *Using ideal diode, design a clamping circuit to perform the function as in Fig. 1.20.15.*

Feb.-02, Aug.-2000

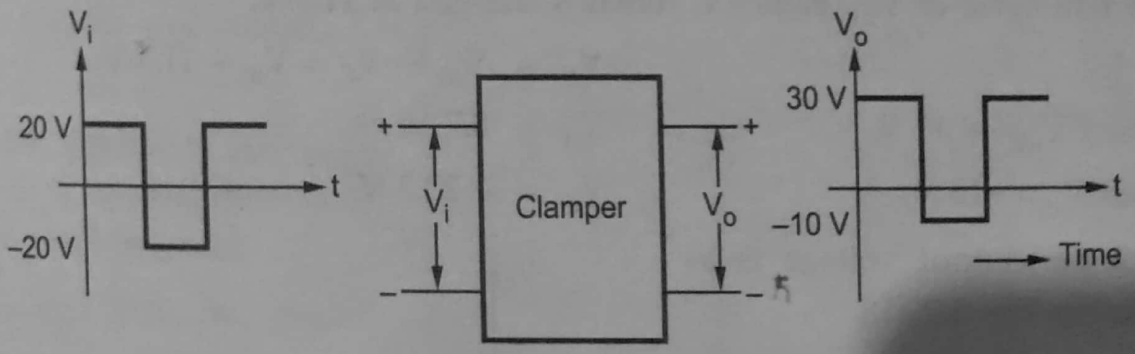


Fig. 1.20.15

Solution : It can be seen that the output swing is same as input swing but a d.c. level of +10 V is added to V_i to produce V_o. So circuit required is positive clamper as shown in the Fig. 1.20.15 (a).

For first negative half cycle of input, D conducts and capacitor gets charged to,

$$V_C = 20 - 10 = 10 \text{ V}$$

The polarities are as shown in the Fig. 1.20.15 (a).

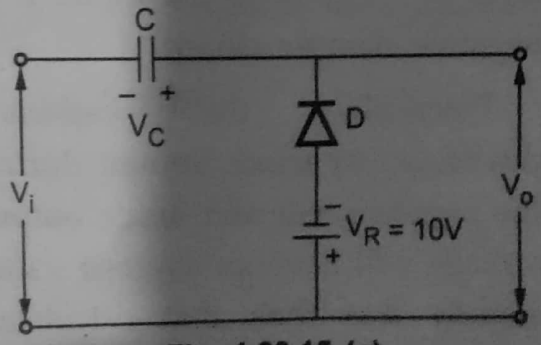


Fig. 1.20.15 (a)

∴ When $V_i = +20$ V, $V_o = V_i + V_C = 20 + 10 = \mathbf{30\ V}$

When $V_i = -20$ V, $V_o = V_i + V_C = -20 + 10 = \mathbf{-10\ V}$

Example 1.20.2 *Sketch the output voltage waveform for the circuit shown in the Fig. 1.20.16. Assume large time constant R_LC. Assume silicon diode with $V_\gamma = 0.7$ V.*

June-12, Marks 6

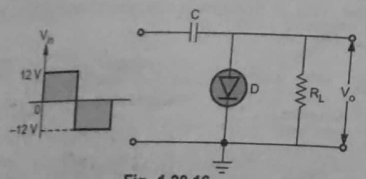


Fig. 1.20.16

Solution : In the first half cycle of the input voltage, the diode is forward biased and capacitor C starts charging. It gets charged equal to (12 – 0.7) = 11.3 V, due to diode drop of 0.7 V.

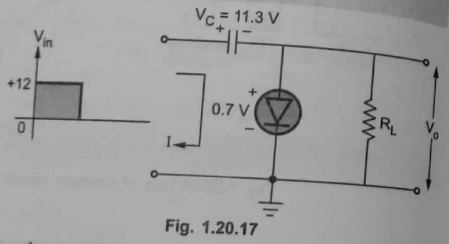


Fig. 1.20.17

When V_{in} becomes negative, the diode is reverse biased and acts as an open circuit. And C remains charged at 11.3 V, with the polarities as shown in the Fig. 1.20.17.

Due to large time constant, there is hardly any loss of capacitor charge during negative half cycle of V_{in}. Hence C remains charged at 11.3 V.

Hence $V_o = V_{in} - V_C = V_{in} - 11.3$ V

Thus when $V_{in} = +12$ V, $V_o = 0.7$ V

and when $V_{in} = -12$ V, $V_o = -23.3$ V

Hence the output voltage is as shown in the Fig. 1.20.18.

Thus the circuit adds a d.c. level of – 11.3 V to the input. It is negative clamper circuit.

Practically the capacitor discharges by small amount during the negative half and hence output voltage will have an average value slightly less than that calculated above.

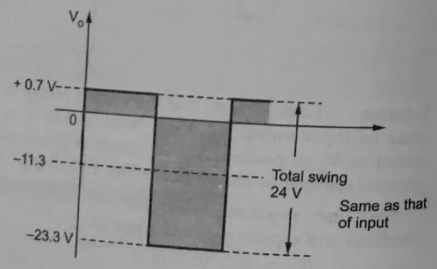


Fig. 1.20.18

Example 1.20.3 *Determine the output voltage V_o for the clamper circuit shown in the Fig. 1.20.19.*

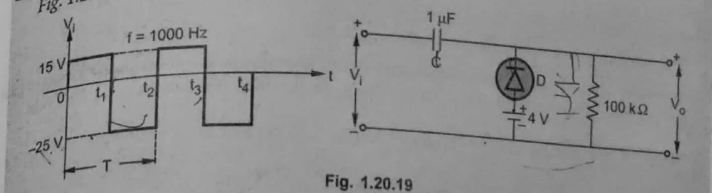


Fig. 1.20.19

Solution : The diode will get forward biased in the negative half cycle of the input V_i. Hence the analysis starts from the period t_1 to t_2. The circuit becomes,

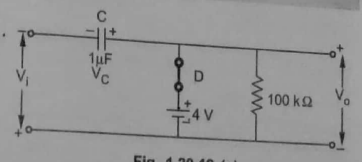


Fig. 1.20.19 (a)

It can be observed that the output voltage V_o is equal to battery voltage of 4 V.

∴ $V_o = 4$ V for t_1 to t_2

Applying KVL to the loop of capacitor and battery,

$+4 - V_C + V_i = 0$

∴ $V_C = 4 + 25 = 29$ V

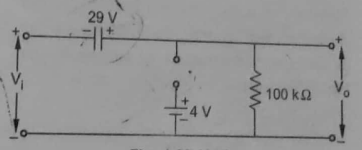


Fig. 1.20.19 (b)

The capacitor will charge upto 29 V.

For the period t_2 to t_3, the diode is reverse biased and the circuit becomes,

Applying KVL to the loop,

$-V_o + V_i + 29 = 0$

∴ $V_o = V_i + 29$

$= 15 + 29 = 44$ V

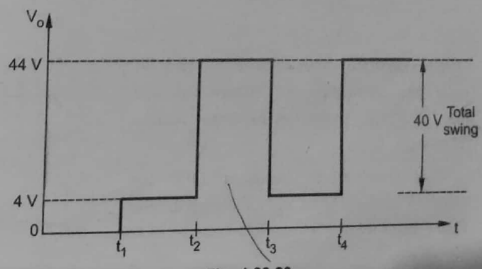


Fig. 1.20.20

The discharge time constant is,

$T_d = RC = 100\ k\Omega \times 1\ \mu F = 0.1$ sec

∴ Total discharge time $= 5\ T_d = 0.5$ sec = 500 msec

While the interval t_2 to t_3 lasts for half of the period i.e. $\frac{T}{2} = \frac{1}{2\times1000} = 0.5$ m sec.

Thus capacitor holds its entire charge and remains charged at 29 V.

The output waveform is shown in the Fig. 1.20.20.

It can be observed that the total output swing is equal to the total input swing equal to 40 V. The circuit adds 29 V d.c. to the input, to produce the output.

Example 1.20.4 *Analyze the circuit shown in Fig. 1.20.21, and draw the output waveform. Assume $V_\gamma = 0.7$ V.*

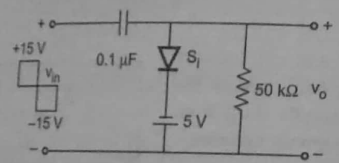


Fig. 1.20.21

Solution : For the positive half cycle, the capacitor will charge instantaneously as diode is forward biased as shown in the Fig. 1.20.21 (a).

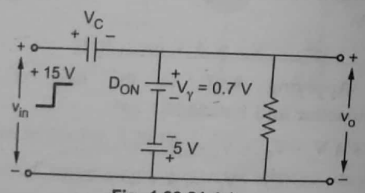


Fig. 1.20.21 (a)

Applying KVL,

$$-V_C - 0.7 + 5 + 15 = 0$$

$$\therefore \quad V_C = 19.3 \text{ V}$$

$$\therefore \quad V_o = -5 + 0.7 = -4.3 \text{ V}$$

The capacitor will charge to 19.3 V, with the polarities as shown in the Fig. 1.20.21 (a). Thereafter capacitor retains its charge.

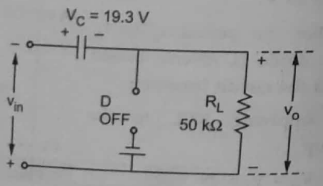


Fig. 1.20.21 (b)

Then the diode becomes OFF for negative half cycle of v_{in} as shown in the Fig. 1.20.21 (b)

Appying KVL,

$$-V_C - V_o - V_{in} = 0$$

$$\therefore \quad V_o = -V_C - V_{in}$$

$$= -19.3 - 15 = -34.3 \text{ V}$$

Hence the output waveform is as shown in the Fig. 1.20.21 (c)

It can be observed that the total output swing is same as total input swing of 30 V.

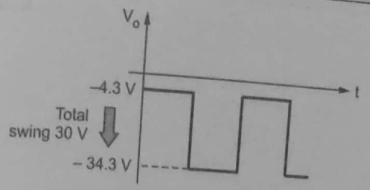


Fig. 1.20.21 (c)

Example 1.20.5 *Determine v_o for the network shown in Fig. 1.20.22 Also sketch v_o.*

Dec.-11, Marks 6

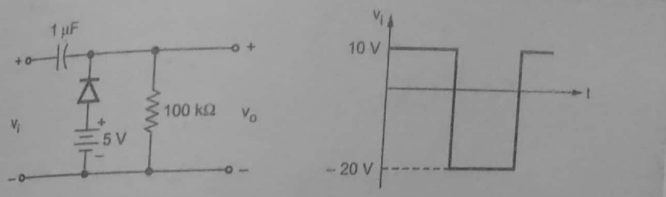


Fig. 1.20.22

Solution : Refer example 1.20.3 for the procedure and verify the answer as :

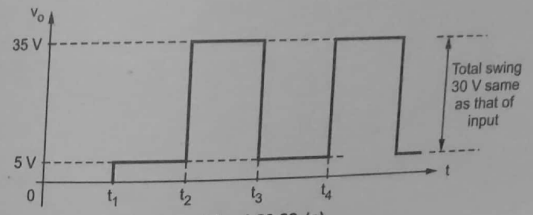


Fig. 1.20.22 (a)

Review Questions

1. *Draw a simple clamping circuit and explain its operation.* **July-04, Marks 6**
2. *Draw and explain the working of the clamper circuit which clamps the positive peak of a signal to zero.* **Jan.-08, Marks 5**

□□□