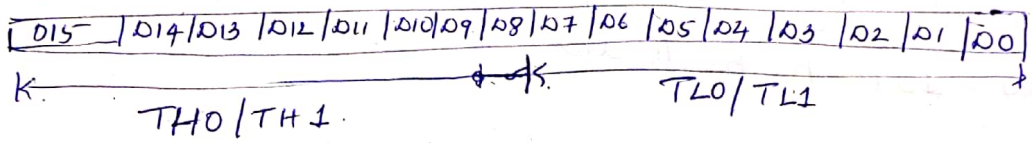
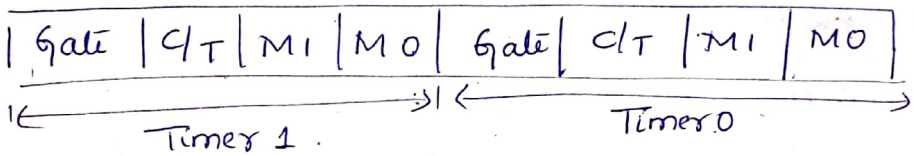
8051 Timers

→ has 2 timers Timer 0 & Timer 1. They can be used either as timers or as event counters.

→ Both are 16 bits wide. treated as low byte and high byte. The low byte register is called TL0/TL1 & higher byte register is called TH0/TH1.



TMOD register



Gate: Gating control when set, the timer/counter is enabled only while INTx pin is high and TRx control pin is set. When cleared, the timer is enabled whenever TRx control bit set. (H/w control) (S/w control)

C/T: Timer/counter selected.
C/T = 0 ⇒ Timer operation.
C/T = 1 ⇒ counter operation

M1 & M0: Mode selection for timers.

M1	M0	Mode	operating mode
0	0	0	→ 13 bit timer mode 8bit timer/counter. THx with TLx as 5 bit prescaler.
0	1	1	→ 16 bit timer mode 16 bit timer/counters THx & TLx are cascaded.
1	0	2	→ no prescaler. 8 bit autoreload (THx holds a value that is reloaded into TLx each time it overflows.
1	1	3	→ Split timer mode.

* Find the values of TMOD to operate as timers in following modes.

(1) Mode 1 Timer 1

(2) Mode 2 Timer 0, Mode 2 Timer 1

(3) Mode 0 Timer 1

(1)

	Timer 1				Timer 0.			
	Gate	C/T	M1	M0	Gate	C/T	M1	M0
	0	0	0	1	0	0	0	0
				1				0

∴ TMOD = 10 H to be loaded

(2)

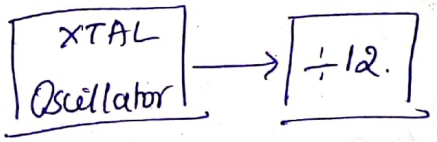
	0	0	1	0	0	0	1	0

TMOD = 22 H

(3) TMOD = 00 H

* Timer clock frequency [Clock source for timer]

Timers use $1/12^{th}$ of XTAL frequency, i.e.,



TCON Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1 — TCON.7 - Timer 1 overflow flag. Set by Hardware when timer/counter 1 overflows. Cleared by H/W as processor jumps to ISR.

TR1 — TCON.6 - Timer 1 run control bit. Set/cleared by Software to turn timer1/counter1 on/off.

TF0 TCON.5
TR0 TCON.4
} Same function but with respect to timer/counter 0.

IE1 TCON.3 External Interrupt 1 edge flag. Set by CPU when the external interrupt edge (H to L transition) is detected. Cleared by CPU when the interrupt is processed.

IT1 TCON.2. Interrupt 1 type control bit. Set/cleared by S/W to specify edge / low level triggered ext int.

IT1 = 0 ⇒ low level.
= 1 ⇒ Edge triggered.

IE0 TCON.1
IT0 TCON.2
} Same function but with respect to INT0.