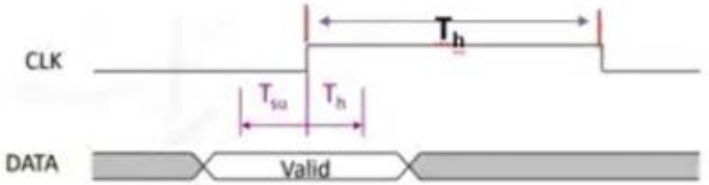
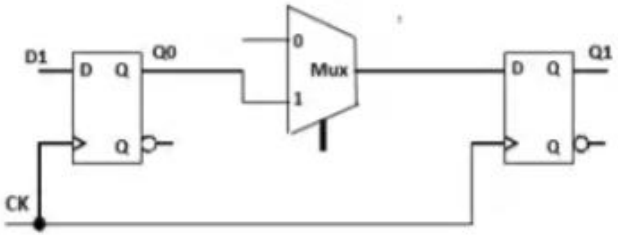
How to fix hold time violations



Hold: $T_{ck->q} + T_{prop} > T_{hold} + T_{skew}$

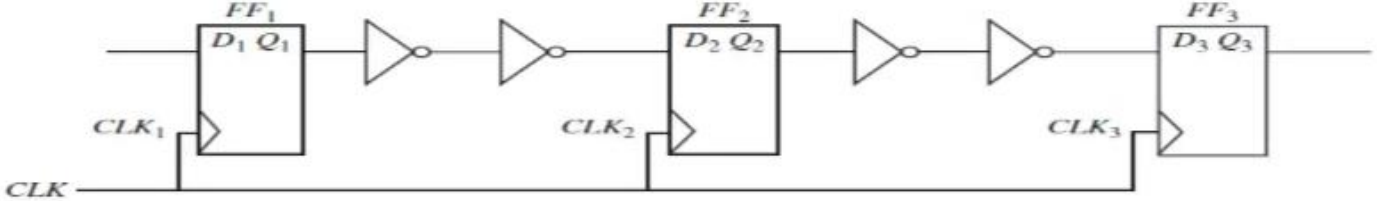


Fixing Hold Timing Violations:

- Increasing the **clk->q** delay of launching flop
- Decreasing the hold requirement of capturing flop
- Decreasing clock skew between capturing clock and launching flip-flops

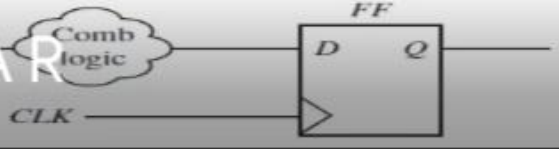
Shift Registers with buffers meeting hold time constraints

Designing shift registers and counters by chaining together flip-flops is very easy from a functional perspective, however, it is very difficult to meet hold-time constraints, because combinational circuit delay is zero. One way to correct such designs is by inserting buffers between flip-flops as in Figure 1-38.



Timing Rules for Input to Flip-Flop Paths

Now let us consider a timing path from primary input to flip-flop as in Figure 1-39. The changes in primary input X should happen such that the value propagates to the flip-flop input satisfying both setup and hold-time constraints. In other words, flip-flop setup time and hold time dictate when primary inputs are allowed to change.



Rule No. 3 Setup time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop setup time.

A setup time violation could occur if the X input to the circuit changes too close to the active edge of the clock. When the X input to a sequential circuit changes, we must make sure that the input change propagates to the flip-flop inputs such that the setup time is satisfied before the active edge of the clock. If X changes at time t_x before the active edge of the clock (see Figure 1-40), then it could take up to the maximum propagation delay of the combinational circuit before the change in X propagates to the flip-flop input. There should still be a margin of t_{su} left before the edge of the clock. Hence, the setup time is satisfied if

$$t_x \geq t_{cxmax} + t_{su} \tag{1-36}$$

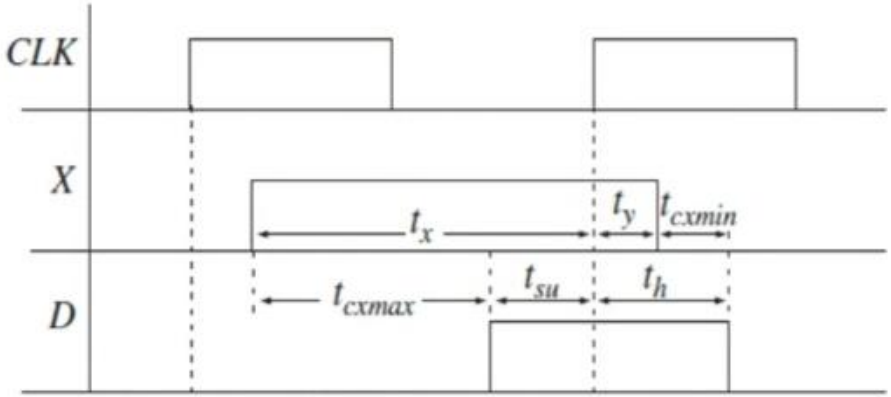
where t_{cxmax} is the maximum propagation delay from X to the flip-flop input.

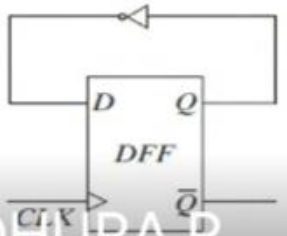
Rule No. 4 Hold-time rule for input to flip-flop path: External input changes to the circuit should satisfy flip-flop hold times.

In order to satisfy the hold time, we must make sure that X does not change too soon after the clock. If a change in X propagates to the flip-flop input in zero time, X should not change for a duration of t_h after the clock edge. Fortunately, it takes some positive propagation delay for the change in X to reach the flip-flop. If t_{cxmin} is the minimum propagation delay from X to the flip-flop input, changes in X will not reach the flip-flop input until at least a time of t_{cxmin} has elapsed after the clock edge. So, if X changes at time t_y after the active edge of the clock, then the hold time is satisfied if

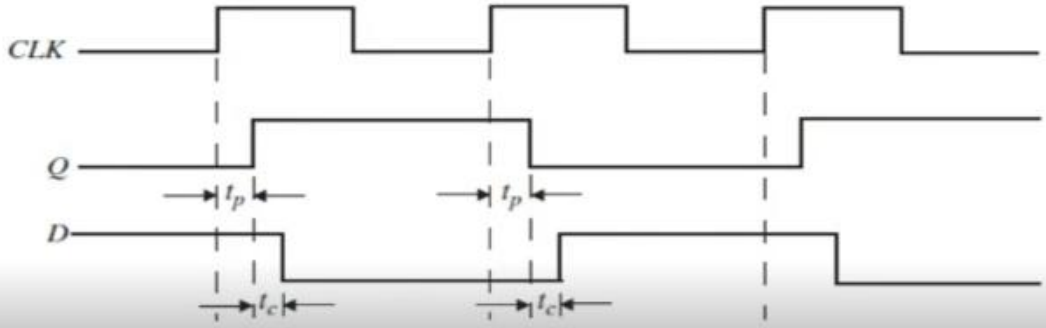
$$t_y \geq t_h - t_{cxmin} \tag{1-37}$$

If t_y is negative, X can change before the active clock edge and still satisfy the hold time.





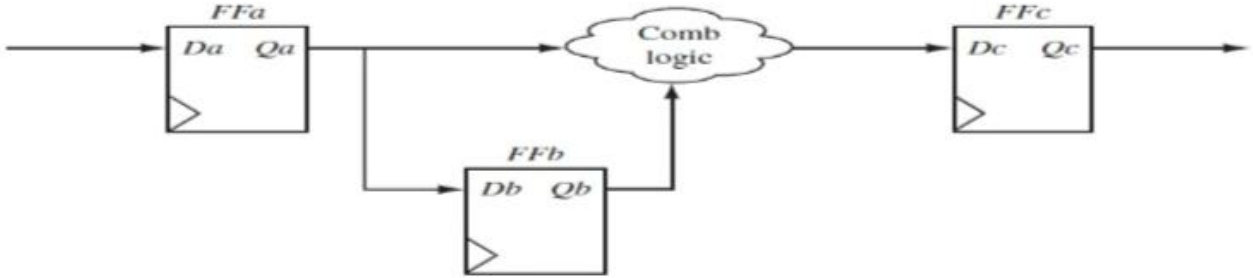
(a) A frequency divider



(b) Frequency divider timing diagram

Consider the circuit in Figure 1-43 with the following minimum/maximum delays:

CLK-to-Q for flip-flop A: 7 ns/9 ns
CLK-to-Q for flip-flop B: 8 ns/10 ns
CLK-to-Q for flip-flop C: 9 ns/11 ns
Combinational logic: 3 ns/4 ns
Setup time for flip-flops: 2 ns
Hold time for flip-flops: 1 ns



Answer: Remember that a timing path starts at either a primary input or at the input of a flip-flop. A path terminates at the input of a flip-flop or at a primary output.

Delay for path from flip-flop A to B = $t_{clk\text{-}to\text{-}Q(A)} + t_{su}(B) = 9\,ns + 2\,ns = 11\,ns$

Delay for path from flip-flop A to C = $t_{clk\text{-}to\text{-}Q(A)} + t_{combo} + t_{su}(C) = 9\,ns + 4\,ns + 2\,ns = 15\,ns$

Delay for path from flip-flop B to C = $t_{clk\text{-}to\text{-}Q(B)} + t_{combo} + t_{su}(C) = 10\,ns + 4\,ns + 2\,ns = 16\,ns$

Delay for path from input to flip-flop A = $t_{su}(A) = 2\,ns = 2\,ns$

Delay for path from flip-flop C to output = $t_{clk\text{-}to\text{-}Q(C)} = 11\,ns$

Since the delay for path from B to C is the largest of the path delays, the maximum clock frequency is determined by this delay of 16 ns. The frequency is $1/t_{min} = 1/16\,ns = 62.5$ MHz.

Consider the circuit in Figure 1-35 with the following minimum/maximum delays:

CLK-to-Q for flip-flop 1: 5 ns/8 ns

CLK-to-Q for flip-flop 2: 7 ns/9 ns

XOR Gate: 4 ns/6 ns

AND Gate: 1 ns/3 ns

Setup time for flip-flops: 5 ns

Hold time for flip-flops: 2 ns

(a) What is the minimum clock period that this circuit can be safely clocked at?

Answer: Since XOR gate delay is higher than the AND gate delay, and the second flip-flop's delay is greater than that of the first flip-flop, the path from the second flip-flop to input of the second flip-flop via the XOR is the longest path. This path determines the maximum clock frequency. The maximum frequency is dictated by

$$f_{max} = 1/(t_{flip\text{-}flop\text{-}max} + t_{XORmax} + t_{su})$$
$$= 1/(9 + 6 + 5) = 1/20\,ns = 50\ MHz$$

(b) What is the earliest time after the rising clock edge that input A can safely change?

Answer: The earliest time after the rising clock edge that A can safely change can be obtained from equation (1-37)

$$t_y = t_h - t_{ANDmin} = 2\,\text{ns} - 1\,\text{ns} = 1\,\text{ns}$$

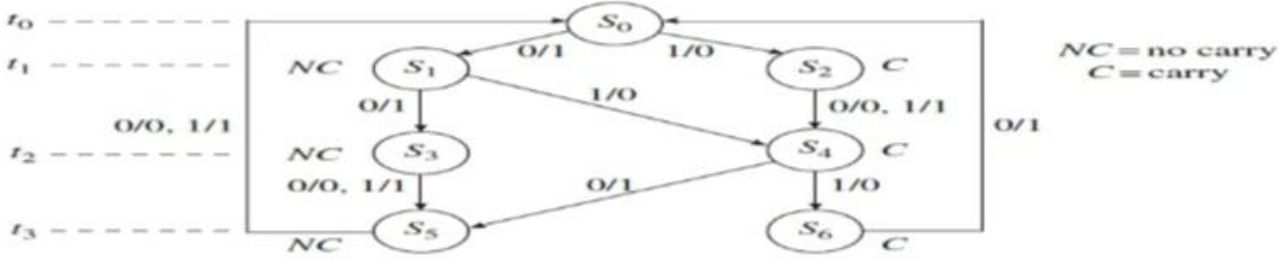
(c) What is the latest time before the rising clock edge that input A can safely change?

Answer: The latest time before the rising clock edge that A can safely change can be obtained from equation (1-36)

$$t_x = t_{ANDmax} + t_{su} = 3\,\text{ns} + 5\,\text{ns} = 8\,\text{ns}$$

Glitches In Sequential Circuits

- Sequential circuits often have external inputs that are asynchronous. Temporary false values called glitches can appear at the outputs and next states. For example, if the state table of Figure



(a) Mealy state graph

PS	NS X=0	NS X=1	Z X=0	Z X=1
S_0	S_1	S_2	1	0
S_1	S_3	S_4	1	0
S_2	S_4	S_4	0	1
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_0	—	1	—

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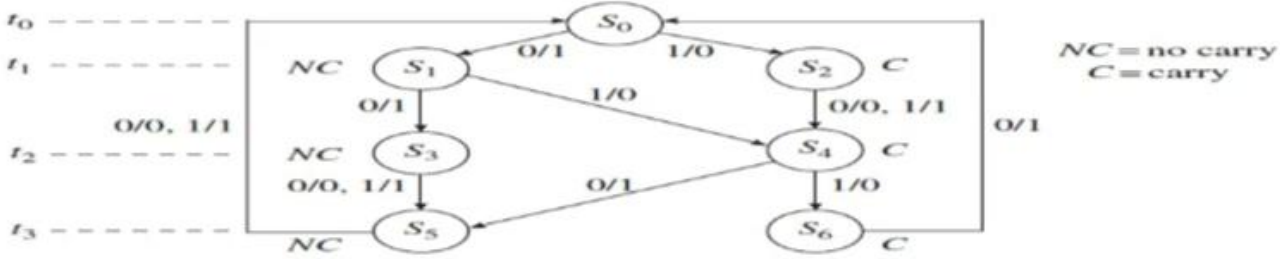

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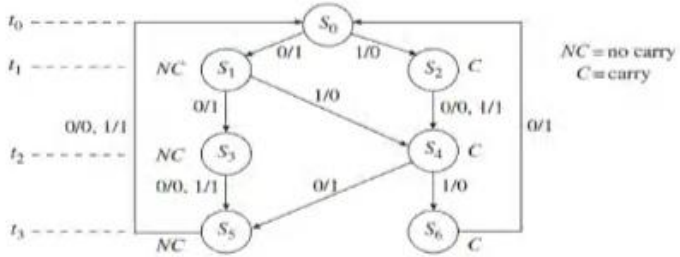
S_1	S_3	S_4	1	0
S_2	S_4	S_4	0	1
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_0	—	1	—

- Propagation delays in the flip-flop have been neglected; hence state changes are shown to coincide with clock edges. In this example, the input sequence is 00101001, and *X* is assumed to change in the

the middle of the clock pulse. At any given time, the next state and Z output can be read from the next state table. For example, at time t_a, State $= S_5$ and $X = 0$, so Next State $= S_0$ and $Z = 0$. At time t_b following the rising edge of the clock, State $= S_0$ and X is still 0, so Next State $= S_1$ and $Z = 1$. Then X changes to 1, and at time t_c Next State $= S_2$ and $Z = 0$. Note that there is a *glitch* (sometimes called a false output) at t_b. The Z output momentarily has an incorrect value at t_b, because the change in X is not exactly synchronized with the active edge of the clock. The correct output sequence, as indicated on the waveform, is 1 1 1 0 0 0 1 1. Several glitches appear between the correct outputs; however, these are of no consequence if Z is read at the right time. The glitch in the next state at t_b (S_1) also does not cause a problem, because the next state has the correct value at the active edge of the clock.

00101001 11100011

- the timing waveforms are as shown in Figure



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	NS		Z	
PS	X=0	X=1	X=0	X=1
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S_1	S_3	S_4	1	0
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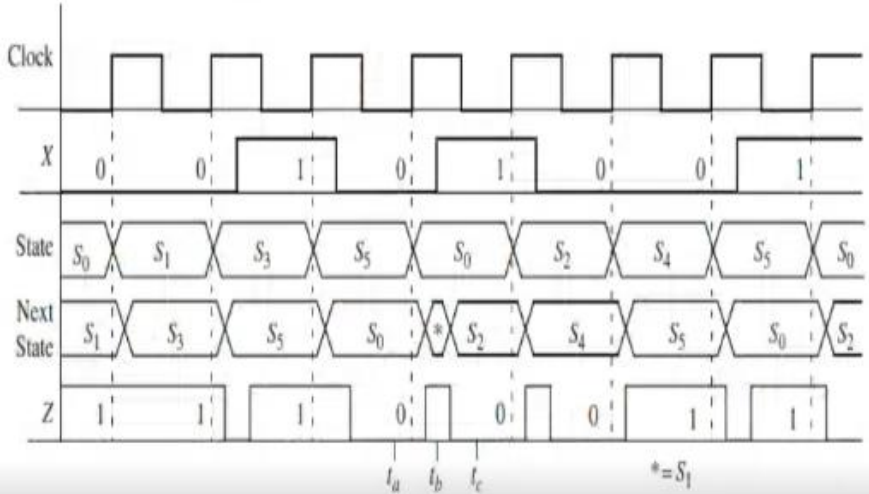
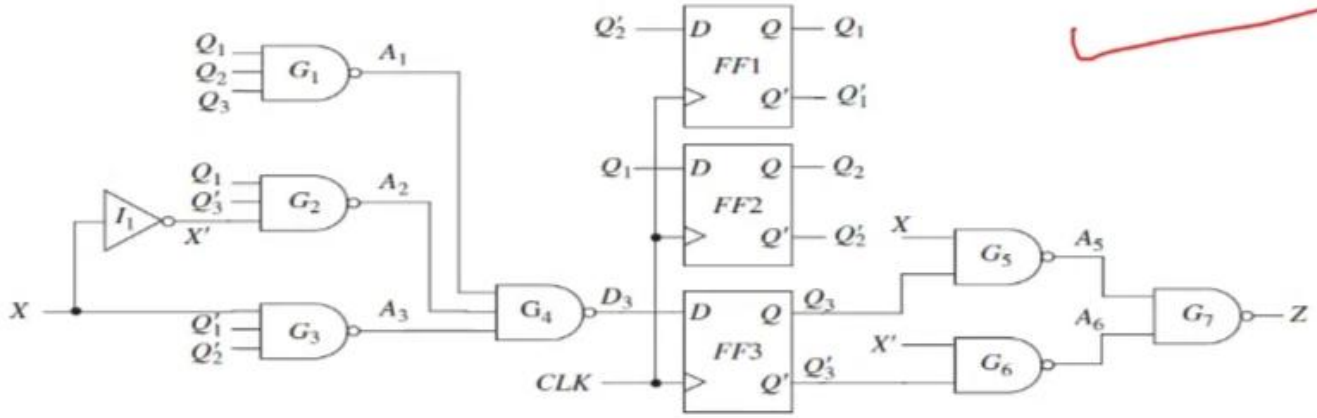
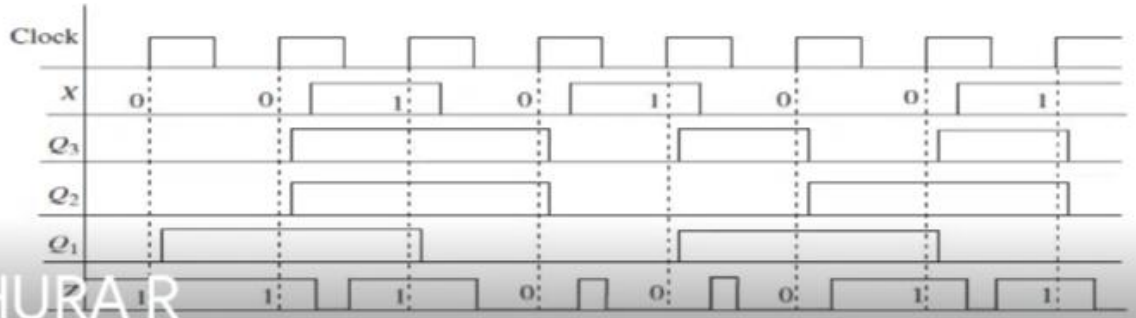
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_5	S_5	1	0

(b) State table







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State has been replaced with the states of three flipflops and propagation delay of 10 ns has been assumed