C:/Modeltech_pe_edu_10.4a/examples/verilog_01/and_example.v

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C:/Modeltech_pe_edu_10.4a/examples/verilog_01/and_example.v - Default

Ln#

```
1  //Verilog design in data flow model
2  module and_gate(
3      input a,b
4      output y);
5     assign y = a & b;
6
7  endmodule
8
9  //TestBench
10 `timescale 1ns/1ns
11 module tb_and_gate;
12     reg A,B;
13     wire Y;
14
15     and_gate a1 (.a(A) ,.b(B),.y(Y));
16
17     //Above style is connecting by name
18     initial begin
19         A =1'b0;
20         B= 1'b0;
21         #10;
22         A=1;
23          B=1;
24          #45 $finish;
25     end
26
27     always #6 A =~A;
28     always #3 B =~B;
29
30     always @(Y)
31       $display( "time =%0t \tINPUT VALUES: \t A=%b B =%b \t output value Y  =%b",$time,A,B,Y);
32 endmodule
```

<No Design Loaded> <No Context>

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You

Type here to search

24-09-2020

C:/Modeltech_pe_edu_10.4a/examples/verilog_01/and_example.v (/tb_and_gate)

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C:/Modeltech_pe_edu_10.4a/examples/verilog_01/and_example.v (/tb_and_gate) - Default

Ln#

```
1  //Verilog design in data flow model
2  module and_gate(
3      input a,b,
4      output y);
5     assign y = a & b;
6
7  endmodule
8
9  //TestBench
10 `timescale 1ns/1ns
11 module tb_and_gate;
12     reg A,B;
13     wire Y;
14
15     and_gate a1 (.a(A) ,.b(B),.y(Y));
16
17     //Above style is connecting by name
18     initial begin
19         A =1'b0;
20         B= 1'b0;
21         #10;
22         A=1;
23          B=1;
24          #45 $finish;
25     end
26
27     always #6 A =~A;
28     always #3 B =~B;
29
30     always @(Y)
31       $display( "time =%0t \tINPUT VALUES: \t A=%b B =%b \t output value Y  =%b",$time,A,B,Y);
32 endmodule
```

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Transcript Window Help

100 ns

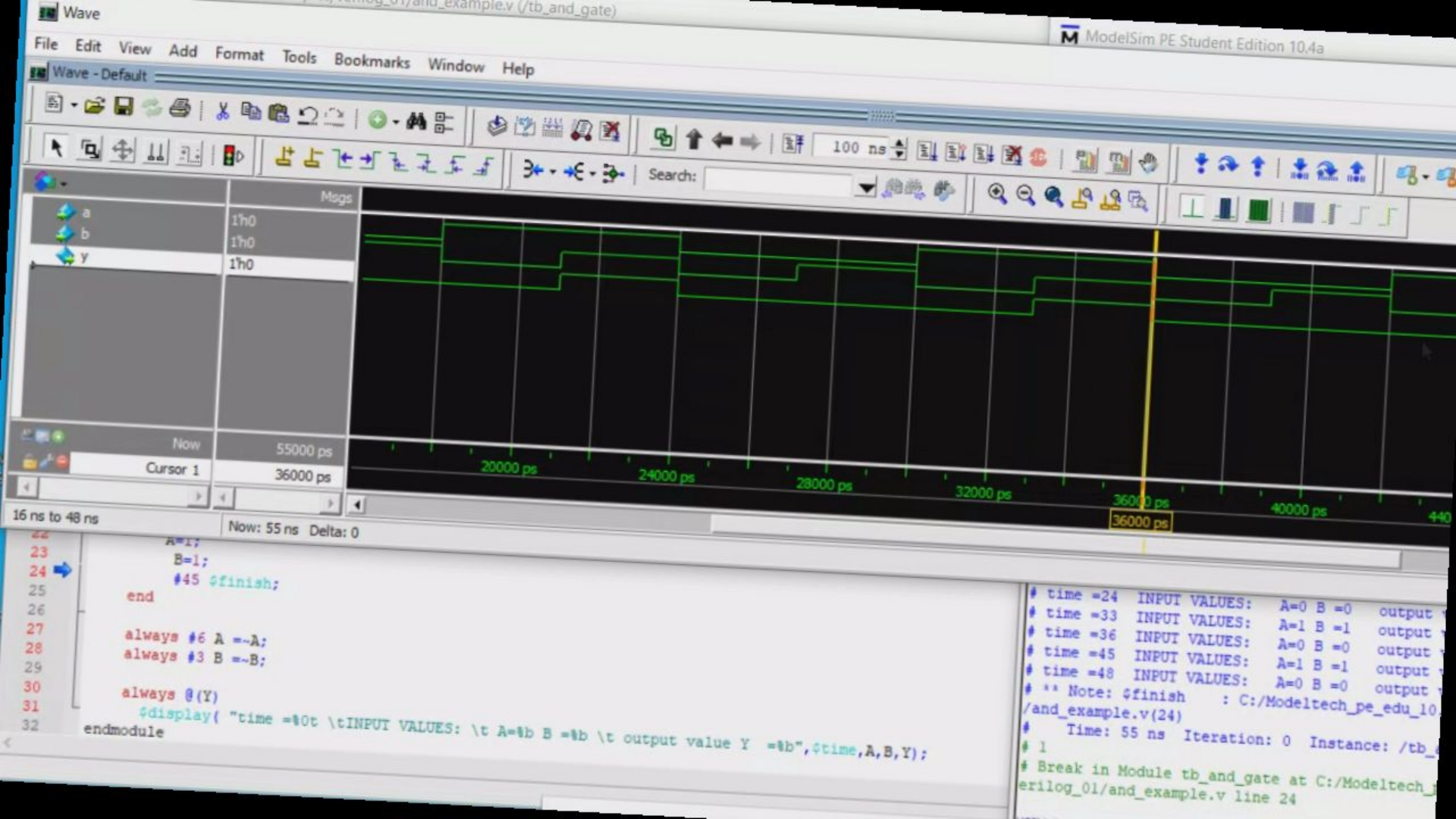
Layout Simulate

ColumnLayout AllColumns

Transcript

```
#           File in use by: hp  Hostname: EXCEL
#
#           Attempting to use alternate WLF fil
# ** Warning: (vsim-WLF-5001) Could not open WL
#
#           Using alternate file: ./wlftw0216h
#
VSIM 4> log -r *
VSIM 5> run -all
# time =0   INPUT VALUES:   A=0 B =0   output va
# time =9   INPUT VALUES:   A=1 B =1   output va
# time =12  INPUT VALUES:   A=0 B =0   output v
# time =21  INPUT VALUES:   A=1 B =1   output v
# time =24  INPUT VALUES:   A=0 B =0   output v
# time =33  INPUT VALUES:   A=1 B =1   output v
# time =36  INPUT VALUES:   A=0 B =0   output v
# time =45  INPUT VALUES:   A=1 B =1   output v
# time =48  INPU                       : v
# ** Note: $fini                       10.
/and_example.v(2
#    Time: 55 ns                       ) e
# 1
# Break in Modul                       ) p
erilog_01/and_ex
VSIM 6>
```

You


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
ModelSim PE Student Edition 10.4a
Search:
Msgs
a
b
y
1'h0
1'h0
1'h0
Now
55000 ps
Cursor 1
36000 ps
20000 ps
24000 ps
28000 ps
32000 ps
36000 ps
40000 ps
36000 ps
16 ns to 48 ns
Now: 55 ns Delta: 0
B=1;
#45 $finish;
end
always #6 A =~A;
always #3 B =~B;
always @(Y)
$display("time =%0t \tINPUT VALUES: \t A=%b B =%b \t output value Y =%b",$time,A,B,Y);
endmodule
time =24 INPUT VALUES: A=0 B =0 output
time =33 INPUT VALUES: A=1 B =1 output
time =36 INPUT VALUES: A=0 B =0 output
time =45 INPUT VALUES: A=1 B =1 output
time =48 INPUT VALUES: A=0 B =0 output
** Note: $finish : C:/Modeltech_pe_edu_10
/and_example.v(24)
Time: 55 ns Iteration: 0 Instance: /tb
1
Break in Module tb_and_gate at C:/Modeltech
erilog_01/and_example.v line 24

C:/Modeltech_pe_edu_10.4a/examples/verilog_01/orgate.v

File Edit View Tools Bookmarks Window Help

C:/Modeltech_pe_edu_10.4a/examples/verilog_01/orgate.v - Default

Ln#

```
1  module OR_2_behavioral (output reg Y, input A, B);
2  always @ (A or B) begin
3      if (A == 1'b0 & B == 1'b0) begin
4          Y = 1'b0;
5      end
6      else
7          Y = 1'b1;
8  end
9  endmodule
10
11 //include "OR_2_behavioral.v"
12 module OR_2_behavioral_tb;
13 reg A, B;
14 wire Y;
15 OR_2_behavioral Indtance0 (Y, A, B);
16 initial begin
17     A = 0; B = 0;
18  #1 A = 0; B = 1;
19  #1 A = 1; B = 0;
20  #1 A = 1; B = 1;
21 end
22 initial begin
23     $monitor ("%t | A = %d| B = %d| Y = %d", $time, A, B, Y);
24     $dumpfile("dump.vcd");
25     $dumpvars();
26 end
27 endmodule
```

You

ModelSim PE Student Edition 10.4a

File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

Transcript

```
# Model Technology ModelSim PE Student Edition vlog 10.4a Compiler 2015.03 Apr  7 2015
# Start time: 14:37:15 on Sep 24,2020
# vlog -reportprogress 300 -work work C:/Modeltech_pe_edu_10.4a/examples/verilog_01/orgate.v
# -- Compiling module OR_2_behavioral
# -- Compiling module OR_2_behavioral_tb
#
# Top level modules:
#       OR_2_behavioral_tb
# End time: 14:37:15 on Sep 24,2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
VSIM 7> vsim -gui work.OR_2_behavioral_tb
# vsim
# Start time: 14:37:55 on Sep 24,2020
# Loading work.OR_2_behavioral_tb
# Loading work.OR_2_behavioral
add wave -position insertpoint sim:/OR_2_behavioral_tb/*
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#
#           File in use by: hp  Hostname: EXCEL-VLSI  ProcessID: 5744
#
#           Attempting to use alternate WLF file "./wlft15y5dt".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlft15y5dt
#
VSIM 9> log -r *
VSIM 10> run -all
#                    0 | A = 0| B = 0| Y = 0
#                    1 | A = 0| B = 1| Y = 1
#                    2 | A = 1| B = 0| Y = 1
#                    3 | A = 1| B = 1| Y = 1

VSIM 11>
```

You

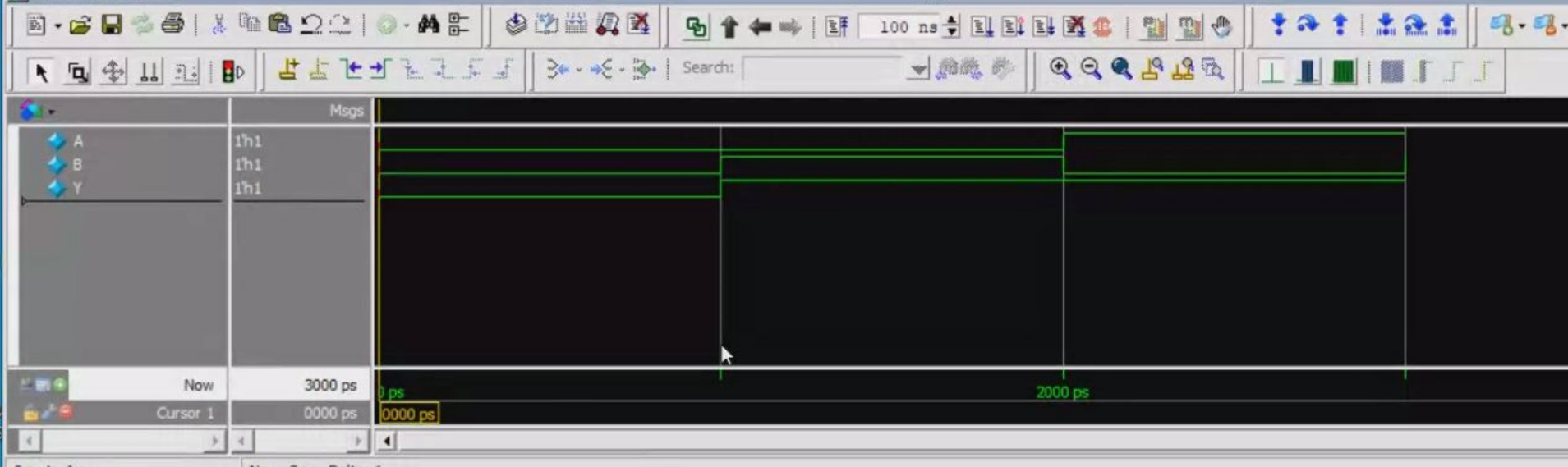
C:/Modeltech_pe_edu_10.4a/examples/verilog_01/orgate.v (/OR_2_behavioral_tb)

ModelSim PE Student Edition 10.4a

Wave

File Edit View Add Format Tools Bookmarks Window Help

Wave - Default



0 ns to 4 ns Now: 3 ns Delta: 1

```
22  initial begin
23      $monitor ("%t | A = %d| B = %d| Y = %d", $time, A, B, Y);
24      $dumpfile("dump.vcd");
25      $dumpvars();
26  end
27  endmodule
```

```
#           Attempting to use alternate WLF file "./wlftl5y5dt".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlftl5y5dt
#
VSIM 9> log -r *
VSIM 10> run -all
#                    0 | A = 0| B = 0| Y = 0
#                    1 | A = 0| B = 1| Y = 1
#                    2 | A = 1| B = 0| Y = 1
#                    3 | A = 1| B = 1| Y = 1
```

You