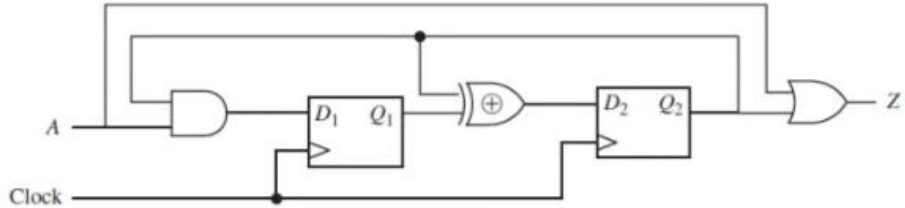
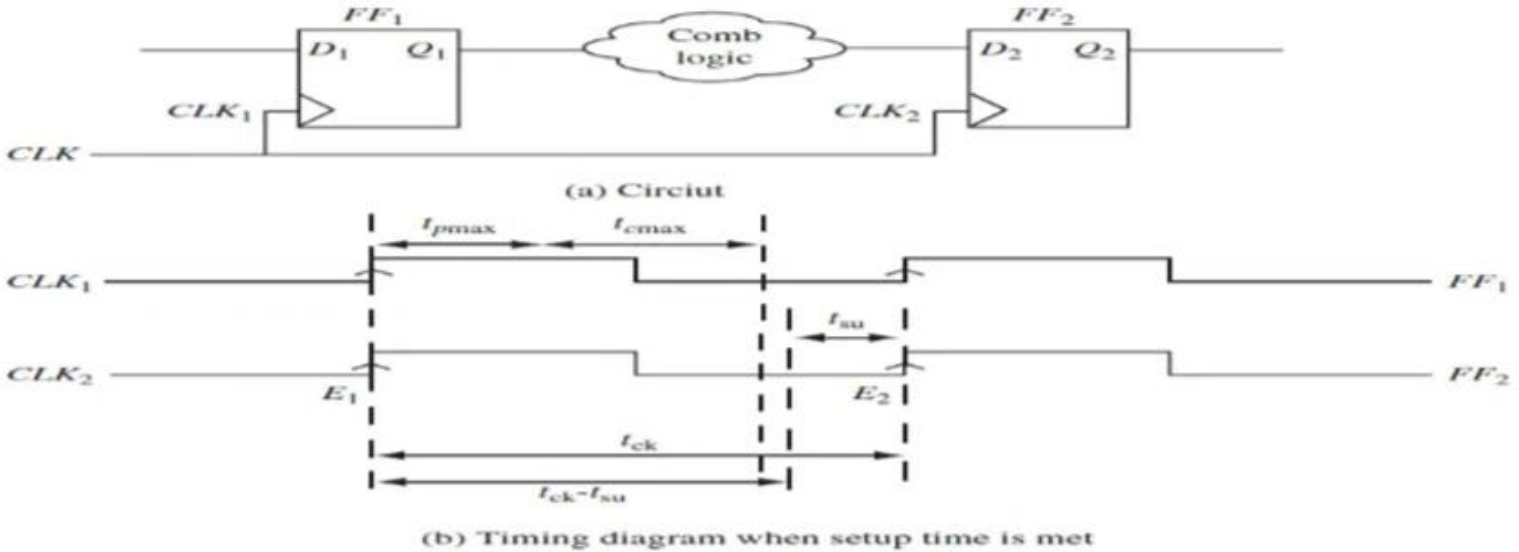
- There are six static timing paths in this circuit:
-
- From *A* to *D*1 (primary input to flip-flop)
- From *D*1 to *D*2 including the XOR (flip-flop to flip-flop
- From *D*2 via XOR to *D*2 (flip-flop to flip-flop)
- From *D*2 to *D*1 via AND (flip-flop to flip-flop)
- From *D*2 to *Z* via the OR gate (flip-flop to output)
- From *A* to *Z* via the OR gate (input to output)



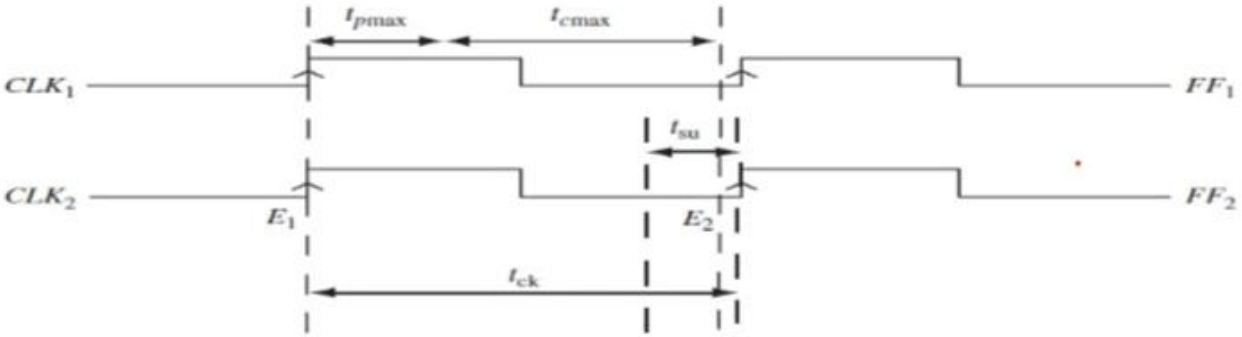
- The most complicated paths are the flip-flop to flip-flop paths; the other paths can be treated as special cases of this type of path.
- Static timing analysis checks how the data arrives with respect to clock. It detects setup and hold-time violations in the design so that they can be corrected. A **setup time violation** occurs if the data changes just before the clock without pro- viding enough setup time for the flip-flop. A **hold-time violation** occurs if the data changes just after the clock without providing enough hold time for the flip-flop.

- **Slack** is the amount of time still left before a signal will violate a setup or hold-time constraint. Paths must have a positive or zero slack in order to have no violations. Paths that have a zero or very small slack are the speed-limiting paths in the design, because any small changes in clock or gate delays will lead to violations in such circuits. Paths that have a negative slack time have already violated a setup or hold constraint. Static timing analysis considers the worst possible timing scenarios, but not the logical operation of the circuit. In comparison with circuit simulation,
- static timing analysis is faster because it doesn't need to simulate multiple test vectors.



Timing Rules for Flip-Flop to Flip-Flop Paths

For a circuit of the general form of Figure 1-36, assume that the maximum propagation delay through the combinational circuit is t_{cmax} and the maximum ***clock- to-Q delay*** or propagation delay from the time the clock changes to the time the flip-flop output changes is t_{pmax}, where t_{pmax} is the maximum of t_{plh} and t_{phl}. Also assume that the minimum propagation delay through the combinational circuit is t_{cmin} and the minimum clock-to-Q delay or propagation delay from the time the clock changes to the time the flip-flop output changes is t_{pmin}, where t_{pmax} data is launched from flip-flop 1's D (i.e., D_1) to FF_1's Q (i.e., Q_1) at the positive edge of clock at FF_1 (i.e., CLK_1). Data is captured at FF_2's D (i.e., D_2) at the positive clock edge at FF_2 (i.e., CLK_2). FF_1 is called the launching flip-flop, and FF_2 is called the capturing flip-flop. There are two rules this circuit has to meet in order to ensure proper operation.



(c) Timing diagram when setup time is violated

Rule No. 1: Setup time rule for flip-flop to flip-flop path: Clock period should be long enough to satisfy flip-flop setup time.

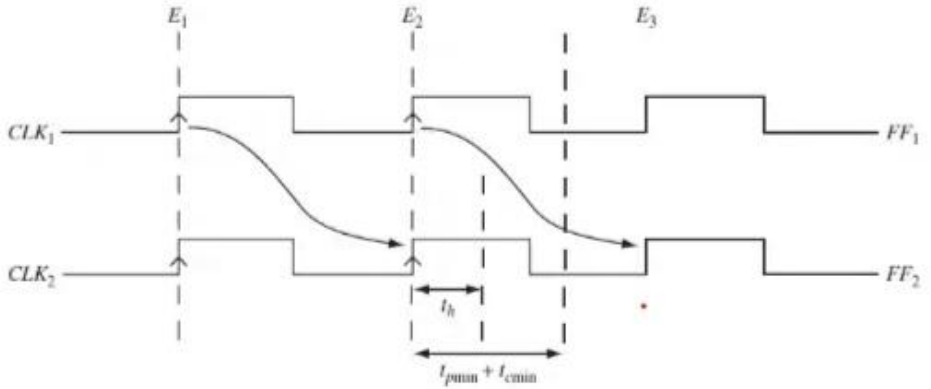
For proper synchronous operation, the data launched by FF_1 at edge E_1 of clock CK_1 should be captured by FF_2 at edge E_2 of clock CK_2. The clock period should be long enough to allow the first flip-flop's outputs to change and the combinational circuitry to change while still leaving enough time to satisfy the setup time. Once the clock CK_1 arrives, it could take a delay of up to t_{pmax} before FF_1's output changes. Then it could take a delay of up to t_{cmax} before the output of the combinational circuitry changes. Thus the maximum time from the active edge E_1 of the clock CK_1 to the time the change in Q_1 propagates to the second flip-flop's input (i.e., D_2) is $t_{pmax} + t_{cmax}$. In

order to ensure proper flip-flop operation, the combinational circuit output must be stable at least t_{su} before the end of the clock E_2 reaches FF_2. If the clock period is t_{ck},

$$t_{ck} \geq t_{pmax} + t_{cmax} + t_{su} \qquad (1\text{-}34\text{-a})$$

Equation (1-34-a) relates the clock frequency of operation of the circuit with setup time of the flip-flops. Therefore, setup time violations can be solved by changing the clock frequency. The difference between t_{ck} and $(t_{pmax} + t_{cmax} + t_{su})$ is referred to as the **setup time margin**. The setup margin has to be zero or positive in order to have a circuit pass timing checks. Figure 1-36 (b) illustrates a situation in which setup time constraint is met, and Figure 1-36 (c) illustrates a situation when setup time constraint is violated. One can check for setup time violations by checking whether

$$t_{ck} - t_{pmax} - t_{cmax} - t_{su} \geq 0 \qquad (1\text{-}34\text{-b})$$



Rule No. 2 Hold-time rule for flip-flop to flip-flop path: Minimum circuit delays should be long enough to satisfy flip-flop hold time.

For proper synchronous operation, the data launched by flip-flop 1 on edge E_1 of clock CK_1 should not be captured by flip-flop 2 on edge E_1 of clock CK_1. This can be understood by thinking about Rule No. 1. According to Rule No. 1, in Figure 1-37 at edge E_2, FF_2 should capture the data launched by FF_1 on the previous edge (i.e., edge E_1). For this to happen successfully, the old data should remain stable at edge E_2 until FF_2's hold time elapses. When FF_2 is capturing this old data at edge E_2, FF_1 has started to launch new data on edge E_2, which should be captured by FF_2 only at edge E_3. A hold-time violation could occur if the data launched by FF_1 at E_2 is fed through the combinational circuit and causes D_2 to change too soon after the clock edge E_2. The new data being launched by FF_1 takes at least t_{pmin} time to pass through FF_1 and at least t_{cmin} to pass through the combinational circuitry. Hence, the hold time is satisfied if

$$t_{pmin} + t_{cmin} \geq t_h \qquad (1\text{-}35)$$

Figure 1-37 illustrates a situation where hold-time is satisfied. When checking for hold-time violations, the worst case occurs when the timing parameters have their minimum values. Since $t_{pmin} > t_h$ for normal flip-flops, a hold-time violation due