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(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – I

Course Name : Computer Organization		Date :	7/10/2020
Course Code : **18EC5DEACO**		Day :	Wednesday
Semester : 5		Timings :	9.30-11.00am
Max Marks : 50 M		Duration :	1½ Hrs.

No.		Question Description	Mks	CO & Levels
Q1	(a)	A 64 bit word consumes ---- bytes of memory i) 2 ii) 4 iii) 8 iv) 16	1	
	(b)	Two basic memory operations are i)Fetch and Execute ii) Load and execute iii) Load and store iv) Decode and execute	1	
	(c)	Which of the following is an example for register transfer notation i)MOVE R1,R2 ii) Operation,src,dst iii) [R1] ← [R1]+[R2] iv) None	1	
	(d)	A 32 bit processor executes the instruction ADD [R2]+,R1. Then contents of R2 are auto incremented by ------ i) 2 ii) 4 iii) 8 iv) 16	1	
	(e)	The processor reads the contents of DATAIN register when flag status i) SI=0 ii) SI=1 iii) Sout=1 iv) Sout=0	1	
	(f)	Stacks and Queues work in ---- and ---- fashion respectively i)LIFO & FIFO ii) FIFO & LIFO iii) FIFO & FIFO iv) LIFO & LIFO	1	
	(g)	Consider R0= 11000010 after performing Ashift ,# 7 ,R0 contents of R0 will be i) 00000000 ii) 10000000 iii) 11111111 iv) 11000010	1	
	(h)	The result of (6+13)Mod 16 in 2's complement system is i) 4 ii) 7 iii) 6 iv) 3	1	
	(i)	If two XOR gates are used to obtain the sum in a carry look ahead adder mention the gate delay associated with the sum. i) 5 ii) 6 iii) 4 iv) 3	1	
	(j)	To reduce the memory access time we generally make use of i)Heaps ii) SDRAM iii) Cache iv) Higher Capacity ram	1	
Q2		Registers R1 and R2 of a computer contains the decimal values 2900 and 3300. Determine the effective- address of the memory operand in each of the following instructions. Also mention the type of addressing mode. (a) Load R1,55(R2) (b) Move #2000, R7 (c) Store 95(R1, R2), R5 (d) Add (R1)+, R5 (e) Subtract -(R2), R5	10M	CO1, L3
Q3		Represent the following decimal values 5,-2,-10,-19,-112 and -98 as signed 8 bit numbers in the following binary formats i)Sign and Magnitude ii)1's Complement iii)2's Complement	10M	CO1 L3

Q4		With a neat block diagram showing connections between processor and memory list the steps taken for execution of instruction ADD X[R1], R0.	10M	CO4, L2
		OR		
Q5		a.)Consider a 32 bit computer has byte organized memory .A program reads ASCII characters for string "Solution" enetered at keyboard and stores them in successive byte locations starting at 4000.Show the contents of two memory words at location 4000 and 4004 for both big endian and little endian schemes with brief explaination for the same. b).Write a program to evaluate the expression $\mathbf{A^2*B^2+C*D}$ using one address machine instruction, briefing the operation of each instruction.	5M 5M	CO1, L3
Q6		a) A program contains 120 instructions, of which 45% instructions consume 1 machine cycle, 25% instruction consume 2 machine cycle and remaining instructions consume 3 machine cycle. Calculate the total time required to execute the program, if operating frequency is 1Ghz and 6 clock cycles make 1 machine cycle. b) Explain subroutine nesting with an example	5M 5M	CO1, CO2 L3
		OR		
Q7		Discuss the advantages of carry look ahead adder over ripple carry adder .Also with a neat block diagram explain a 32 bit carry look ahead adder.	10M	CO1, L3