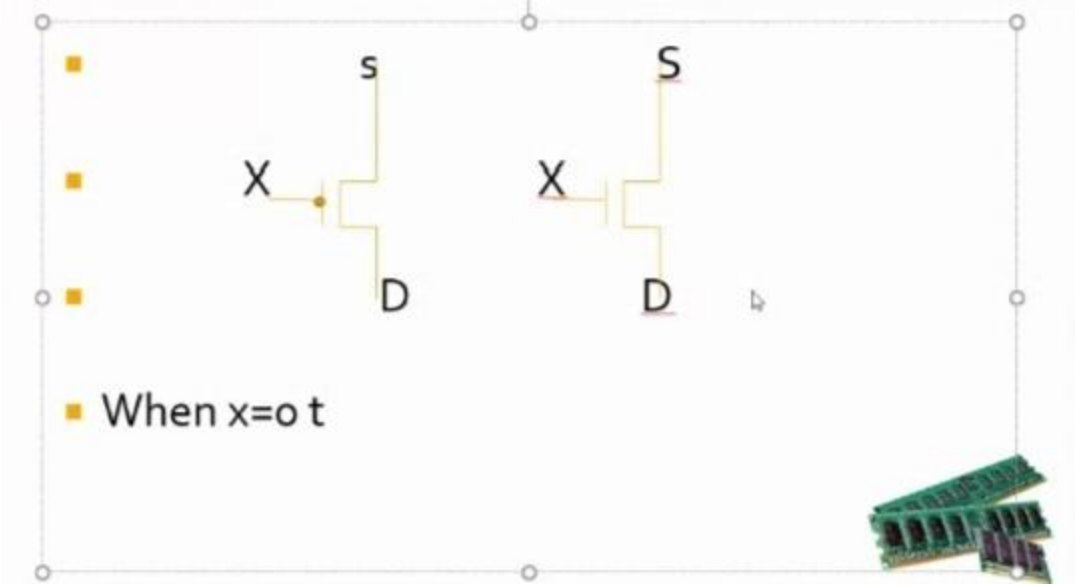
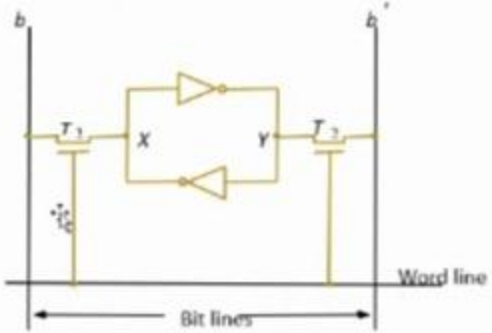

s
X
D
S
X
D
When x=o t

SRAM Cell

- Two transistor inverters are cross connected to implement a basic flip-flop.
- The cell is connected to one word line and two bits lines by transistors T1 and T2
- When word line is at ground level, the transistors are turned off and the latch retains its state
- Read operation: In order to read state of SRAM cell, the word line is activated to close switches T1 and T2. Sense/Write circuits at the bottom monitor the state of b and b'



BASIC CONCEPTS

• Maximum size of memory that can be used in any computer is determined by addressing mode.

Address	Memory Locations
16 Bit	$2^{16} = 64$ K
32 Bit	$2^{32} = 4$G (Giga)
40 Bit	$2^{40} = 1$T (Tera)

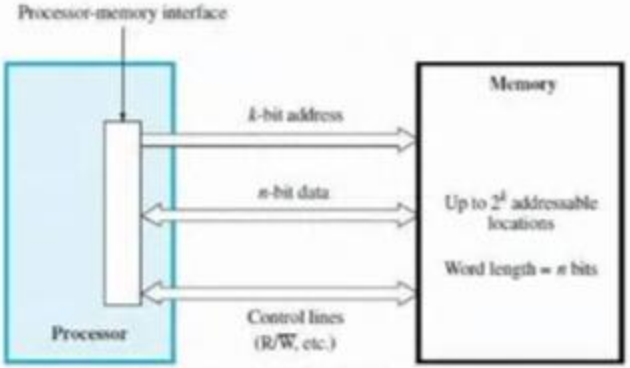


Figure 8.1 Connection of the memory to the processor.

• If MAR is k-bits long then
  → memory may contain upto 2^k addressable-locations
• If MDR is n-bits long, then
  → n-bits of data are transferred between the memory and processor.
• The data-transfer takes place over the processor-bus (Figure 8.1).
• The processor-bus has
  1) Address-Line
  2) Data-line &
  3) Control-Line (R/W*, MFC – Memory Function Completed).
• The Control-Line is used for coordinating data-transfer.
• The processor reads the data from the memory by
  → loading the address of the required memory-location into MAR and

- 5V
- x

Read Operation

- To read the state of the cell, the word-line is activated to close switches T_1 and T_2.
- If the cell is in state 1, the signal on bit-line b is high and the signal on the bit-line b' is low.
- Thus, b and b' are complement of each other.
- Sense/Write circuit
  - → monitors the state of b & b' and
  - → sets the output accordingly.

Write Operation

- The state of the cell is set by
  - → placing the appropriate value on bit-line b and its complement on b' and
  - → then activating the word-line. This forces the cell into the corresponding state.
- The required signal on the bit-lines is generated by Sense/Write circuit.

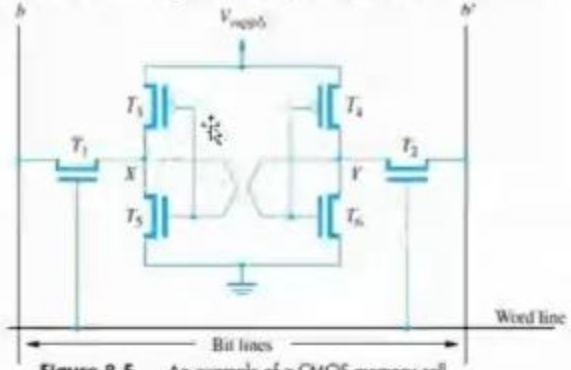


Figure 8.5 An example of a CMOS memory cell.

CMOS Cell

- Transistor pairs (T_3, T_5) and (T_4, T_6) form the inverters in the latch (Figure 8.5).
- In state 1, the voltage at point X is high by having T_5, T_6 ON and T_4, T_5 are OFF.
- Thus, T_1 and T_2 returned ON (Closed), bit-line b and b' will have high and low signals respectively.
- **Advantages:**
  1) It has low power consumption ∴ the current flows in the cell only when the cell is active.
  2) Static RAM's can be accessed quickly. It access time is few nanoseconds.
- **Disadvantage:** SRAMs are said to be volatile memories ∴ their contents are lost when power is

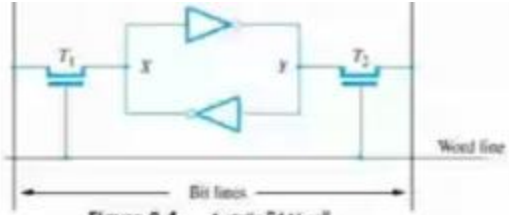


Figure 8.4 A static RAM cell.

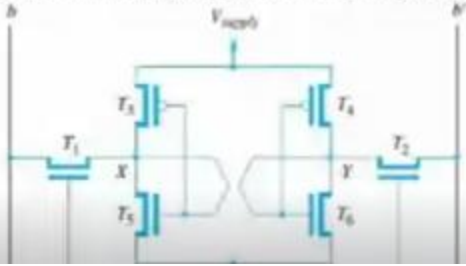
- Two inverters are cross connected to form a latch (Figure 8.4).
- The latch is connected to 2-bit-lines by transistors T_1 and T_2.
- The transistors act as switches that can be opened/closed under the control of the word-line.
- When the word-line is at ground level, the transistors are turned off and the latch retain its state.

Read Operation

- To read the state of the cell, the word-line is activated to close switches T_1 and T_2.
- If the cell is in state 1, the signal on bit-line b is high and the signal on the bit-line b' is low.
- Thus, b and b' are complement of each other.
- Sense/Write circuit
  - → monitors the state of b & b' and
  - → sets the output accordingly.

Write Operation

- The state of the cell is set by
  - → placing the appropriate value on bit-line b and its complement on b' and
  - → then activating the word-line. This forces the cell into the corresponding state.
- The required signal on the bit-lines is generated by Sense/Write circuit.



ASYNCHRONOUS DRAM

- Less expensive RAMs can be implemented if simple cells are used.
- Such cells cannot retain their state indefinitely. Hence they are called **Dynamic RAM (DRAM).**
- The information stored in a dynamic memory-cell in the form of a charge on a capacitor.
- This charge can be maintained only for tens of milliseconds.
- The contents must be periodically refreshed by restoring this capacitor charge to its full value.

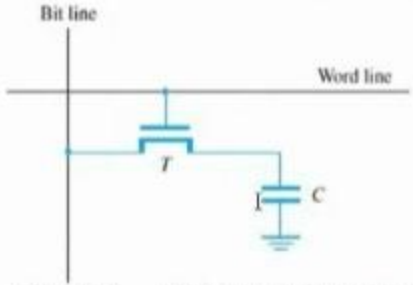


Figure 8.6 A single-transistor dynamic memory cell.

- In order to store information in the cell, the transistor T is turned 'ON' (Figure 8.6).
- The appropriate voltage is applied to the bit-line which charges the capacitor.
- After the transistor is turned off, the capacitor begins to discharge.
- Hence, info. stored in cell can be retrieved correctly before threshold value of capacitor drops down.
- During a read-operation,
  - → transistor is turned 'ON'
  - → a sense amplifier detects whether the charge on the capacitor is above the threshold value.
    - If (charge on capacitor) > (threshold value) Bit-line will have logic value '1'.
    - If (charge on capacitor) < (threshold value) Bit-line will set to logic value '0'.

ASYNCHRONOUS DRAM DESCRIPTION

- The 4 bit cells in each row are divided into 512 groups of 8 (Figure 5.7).
- 21 bit address is needed to access a byte in the memory. 21 bit is divided as follows:
  1) 12 address bits are needed to select a row.
     i.e. A_{8-0} → specifies row-address of a byte.
  2) 9 bits are needed to specify a group of 8 bits in the selected row.
     i.e. A_{20-9} → specifies column-address of a byte.

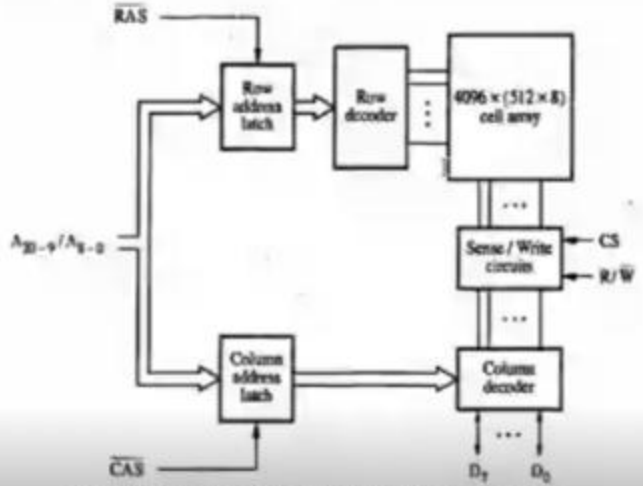


Figure 5.7 Internal organization of a 2M × 8 dynamic memory chip