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(An Autonomous Institute Affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)
(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – III

Course Name : Computer Organization	Date :	06/01/2020
Course Code : 18EC5DEACO	Day :	Wednesday
Semester : 5 A,B,C,D	Timings :	9.30 am-11.00am
Max Marks : 50	Duration :	1½ Hrs.

No.		Question Description	Mks	CO & Levels
Q1	(a)	Which of the following is the fastest means of memory access for CPU? i) Registers ii) Secondary Memory iii) Main memory iv) Cache	1	
	(b)	The Maximum address capacity of a processor with 8 bit data bus and 20 bit address bus is…. i) 64KB ii) 256KB iii) 4GB iv) 1MB	1	
	(c)	A memory device in which a bit is stored as a charge across the stray capacitance i) SRAM ii) EPROM iii) DRAM iv) Bubble memory	1	
	(d)	The minimum time delay between two successive memory read operations is _____. i) Cycle time ii) Latency iii) Delay iv)None of the above	1	
	(e)	Virtual memory is_____. i) memory on the hard disk that the CPU uses an extended RAM ii) in RAM iii)only necessary if you do not have any RAM in your computer iv)a backup device for floppy disk	1	
	(f)	In Set associative mapping cache memory with 256 blocks is divided into 64 sets, then 536 block of main memory consisting of 4096 blocks maps to ---- set in cache memory and can take---- positions in the set. i) Set 0, position 0 or 1 ii) Set 24, positions 0,1,2,3 iii) Set 0, positions 0,1,2,and 3 iv) Set 24, position 0 or 1	1	
	(g)	In memory-mapped I/O _____ i) The I/O devices and the memory share the same address space ii) The I/O devices have a separate address space iii) The memory and I/O devices have an associated address space iv) A part of the memory is specifically set aside for the I/O operation	1	
	(h)	To overcome the lag in the operating speeds of the I/O device and the processor we use ------ i) Buffer spaces ii) Status flags iii) Interrupt signals iv) Exceptions	1	
	(i)	The method of accessing the I/O devices by repeatedly checking the status flags is _____ i) Program-controlled I/O ii) Memory-mapped I/O iii) I/O mapped iv) None of the mentioned	1	
	(j)	In distributed arbitration which among the two devices with ID's 0011 and 0100 will win the arbitration? i) None ii) Both iii) device with ID 0011 iv) Device with ID 0100.	1	
Q2		Sketch and explain organization of 256 x 8 SRAM memory.	10	
Q3		Describe the operation of DMA in detail.	10	
Q4	(a)	Describe the operation of 2M x 8 asynchronous DRAM chip.	6	
	(b)	In a 4-way module interleaving show how the address 1101 is located in high order and low order memory.	4	
		OR		
Q5	(a)	List out the parameters which are effecting the selection of a memory, and explain them briefly.	6	
	(b)	Explain the working of a single-transistor dynamic memory cell.	4	
Q6		Describe the need of enabling and disabling of interrupts and also mention the steps for enabling and disabling the interrupts.	10	
		OR		
Q7		Write short notes on SCSI and PCI Bus.	10	