MODULE 2

ERROR CONTROL CODE

Contents

- **Introduction**
- Linear Block codes-G and H matrix
- Generation and Decoding
- Cyclic codes-g(x) and h(x)
- Encoding using an (n-k) bit shift register
- syndrome calculation
- Convolution Codes: Code generation-Time domain and Transfer domain approach and Code Tree

Introduction

The purpose of error control coding is to enable the receiver to detect or even correct the errors by introducing some redundancies in to the data to be transmitted.

There are basically two mechanisms for adding redundancy:

1. Block coding
2. Convolutional coding

Types of codes

i) Block Codes:

Block code consists of **(n-k)** number of check bits(redundant bits) being added to **k** number of information bits to form 'n' bit code-words.

i) Convolutional code:

In this code, input databits are fed as streams of data bits which convolve to output bits based upon the logic function of the encoder.

meet.google.com is sharing your screen. Stop sharing Hide

Linear Block codes

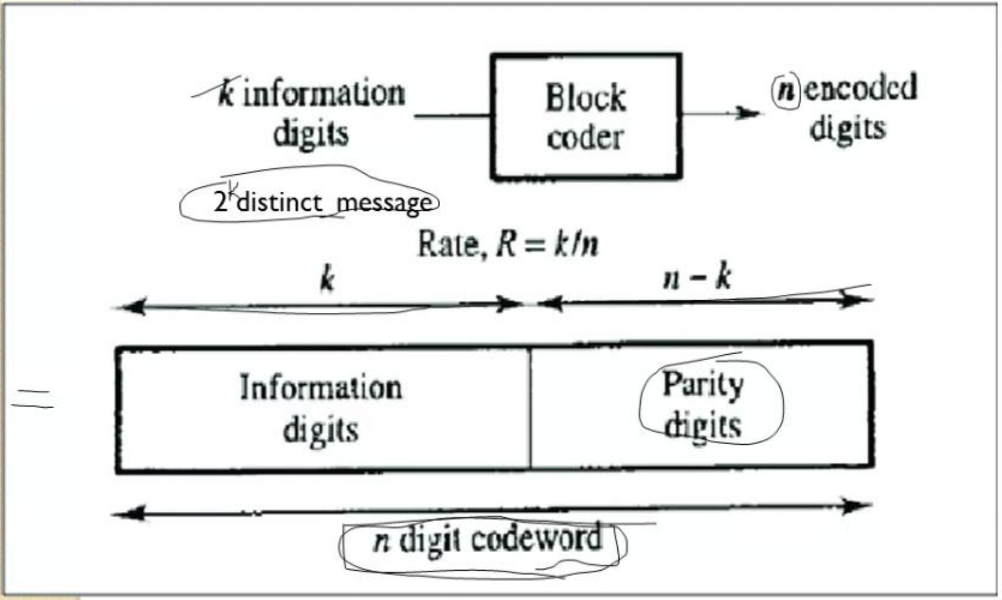
- Let C1 and C2 be any two code words(n-bits) belonging to a set of (n, k) block code

(n,k)

- If C1 $\oplus$ C2, is also a n-bit code word belonging to the same set of(n,k) block code, such a block code is called (n,k)linear block code.

meet.google.com is sharing your screen. Stop sharing Hide

Illustrating the formation of linear block codes



Matrix description of linear block code

- Let the message block of k-bits(code-words) be represented as a "row-vector" or "k-tuple" called "message vector" is given by

  $[D]=\{d_1, d_2, \ldots\ldots d_k\}$

- 2k code-vectors can be represented by

  $C=\{c_1, c_2, \ldots\ldots c_n\}$

- Also $c_i=d_i$ for all $i=1,2,\ldots\ldots k$
- $[C]=\{c_1, c_2, \ldots\ldots c_k, c_{k+1}, c_{k+2}, \ldots\ldots c_n\}$

meet.google.com is sharing your screen. Stop sharing Hide

- (n-k) number of check bits $c_{k+1}, c_{k+2}, \ldots\ldots c_n$ are derived from 'k' message bits using a predetermined rule as below

$$c_{k+1} = p_{11}d_1 + p_{21}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k1}d_k$$
$$c_{k+2} = p_{12}d_1 + p_{22}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k2}d_k$$
$$\vdots$$
$$c_{k+1} = p_{1.\,n-k}d_1 + p_{2.n-k}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k.n-k}d_k$$

- In matrix form,

$$[c_1, c_2, \ldots, c_k,\ c_{k+1}, c_{k+2}, \ldots c_n] = [d_1, d_2, \ldots\ldots d_k] \begin{bmatrix} 1\ 0\ 0 \ldots 0 & p_{11}\ p_{12}\ \ldots\ p_{1.\,n-k} \\ 0\ 1\ 0 \ldots 0 & p_{21}\ p_{22}\ \ldots\ p_{2.\,n-k} \\ & \\ 0\ 0\ 0 \ldots & p_{k1}\ p_{k2}\ \ldots\ p_{k.\,n-k} \end{bmatrix}$$

$$\boxed{\mathbf{[C] = [D]\ [G]}}$$

- [G] is called as ***generator matrix*** of order (k x n)
- $[G] = [I_k \mid P]_{(k \times n)}$ where I_k unit matrix of order 'k'
  $[P]$ = Parity matrix of order $k \times (n-k)$
- Also $[G] = [P \mid I_k]$

- (n-k) number of check bits $c_{k+1}, c_{k+2}, \ldots\ldots. c_n$ are derived from 'k' message bits using a predetermined rule as below

$$c_{k+1} = p_{11}d_1 + p_{21}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k1}d_k$$
$$c_{k+2} = p_{12}d_1 + p_{22}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k2}d_k$$
$$\vdots$$
$$c_{k+1} = p_{1.\,n\text{-}k}d_1 + p_{2.n\text{-}k}d_2 + \ldots\ldots\ldots\ldots\ldots + p_{k.n\text{-}k}d_k$$

- In matrix form,

$$[c_1, c_2, \ldots, c_k,\ c_{k+1}, c_{k+2}, \ldots c_n] = [d_1, d_2, \ldots\ldots d_k] \begin{bmatrix} 1\ 0\ 0\ldots 0 & p_{11}\ p_{12}\ \ldots.\ p_{1.\,n\text{-}k} \\ 0\ 1\ 0\ldots 0 & p_{21}\ p_{22}\ \ldots.\ p_{2.\,n\text{-}k} \\ \\ 0\ 0\ 0\ldots & p_{k1}\ p_{k2}\ \ldots.\ p_{k.\,n\text{-}k} \end{bmatrix}$$

$$\textbf{[C]= [D] [G]}$$

- [G] is called as ***generator matrix*** of order (k x n)
- $[G] = [I_k \,\vdots\, P]_{(k \times n)}$ where I_k unit matrix of order 'k'

  [P]= Parity matrix of order k x (n-k)

- Also $[G] = [P \,\vdots\, I_k]$

remaining $(n-k)$ bits are check bits.

$$C = \{\underbrace{c_1\, c_2\, c_2 \,\ldots\, c_k}_{k \text{ message bits}}\, \underbrace{c_{k+1}\, c_{k+2} \,\ldots\, c_n}_{(n-k) \text{ check bits}}\}$$

These $(n-k)$ check bits are derived from the k message bits using a predefined rule as given below.

$$\left.\begin{aligned}
c_{k+1} &= P_{11}d_1 + P_{21}d_2 + P_{31}d_3 + P_{41}d_4 + \ldots + P_{k1}d_k \\
c_{k+2} &= P_{12}d_1 + P_{22}d_2 + P_{32}d_3 + P_{42}d_4 + \ldots + P_{k2}d_k \\
c_{k+3} &= P_{13}d_1 + P_{23}d_2 + P_{33}d_3 + P_{43}d_4 + \ldots + P_{k3}d_k \\
&\;\vdots \\
c_n &= P_{1(n-k)}d_1 + \ldots + P_{k(n-k)}d_k
\end{aligned}\right\} \text{(iii)}$$

ERROR_CONTROL_CODING.pdf - Adobe Reader

Combining above 3 equations, the equation result can be expressed in matrix form as.

$$[c_1\ c_2\ c_3 \ldots\ldots c_n] = [d_1\ d_2\ d_3 \ldots d_K] \left[\begin{array}{cccccc|cccc} 1 & 0 & 0 & 0 & \ldots & 0 & P_{11} & P_{12} & \ldots & P_{1(n-k)} \\ 0 & 1 & 0 & 0 & \ldots & 0 & P_{21} & P_{22} & \ldots & P_{2(n-k)} \\ 0 & 0 & 1 & 0 & \ldots & 0 & P_{31} & P_{32} & \ldots & P_{3(n-k)} \\ \vdots & \vdots & \vdots & & & & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \ldots & 1 & P_{K1} & P_{K2} & \ldots & P_{K(n-k)} \end{array}\right]$$

$$(1\times n) = (1\times K)\ \underbrace{(K\times K)\quad (K\times (n-k))}_{K\times n}$$

$$[C] = [D]\,[G]$$

where $[G] \rightarrow$ generator matrix which consists of an ider … k & a parity matrix.

$$[C_1\ C_2\ C_3 \ldots\ldots C_n] = [d_1\ d_2\ d_3 \ldots d_K] \underbrace{\left[\begin{array}{cccccc|cccc} 1 & 0 & 0 & 0 & \ldots & 0 & P_{11} & P_{12} & \ldots & P_{1(n-K)} \\ 0 & 1 & 0 & 0 & \ldots & 0 & P_{21} & P_{22} & \ldots & P_{2(n-K)} \\ 0 & 0 & 1 & 0 & \ldots & 0 & P_{31} & P_{32} & \ldots & P_{3(n-K)} \\ \vdots & \vdots & & \vdots & & & \vdots & \vdots & & \vdots \\ 0 & 0 & 0 & 0 & \ldots & 1 & P_{K1} & P_{K2} & \ldots & P_{K(n-K)} \end{array}\right]}_{K \times n}$$

$$(1 \times n) \qquad = \qquad (1 \times K) \qquad (K \times K) \qquad (K \times (n-K))$$

$$[C] = [D]\,[G]$$

where $[G] \rightarrow$ generator matrix which consists of an identity matrix of order K & a parity matrix.

$$[G] = [I \,\vdots\, P_K]$$

[G] is called Generator ...

given by

$$[G] = [I_K \vdots P]_{K \times n}$$

where I_K is unit matrix of order K

P is an arbitrary matrix called parity matrix of the order $K \times (n-K)$

The Generator matrix can also be expressed as

$$[G] = [P \vdots I_K]_{K \times n}$$

In this case, the message bits will be present at the end & the check bits at the beginning of code vector.

P) The Generator matrix for a (6,3) block code is given below. F ... ors.