- Operation:
  - When the DRAM cell is accessed only an m-bit word (data bus width) is transferred.
  - But when we select a row, we can select not only the data of a single column but multiple columns as well.
  - A latch can be connected at the output of the sense amplifier in each column.
  - Once we apply a row address, the row get selected.
    - Different column addresses are required to place different bytes on the data lines
  - Hence consecutive bytes can be transferred by applying consecutive column addresses under the control of successive CAS signals.
  - This also helps in faster transfer of blocks of data.
  - This block transfer capability is termed as *Fast Page Mode* access.

Synchronous DRAM

- The operations are directly synchronized with clock signal .
- The structure of memory is same as asynchronous DRAM.
- The address and data connections are buffered by means of registers.
- The output of each sense amplifier is connected to a latch.
- Mode register is present which can be set to operate the memory chip in different modes.
- To select successive columns column counter is used to generate the required signals.

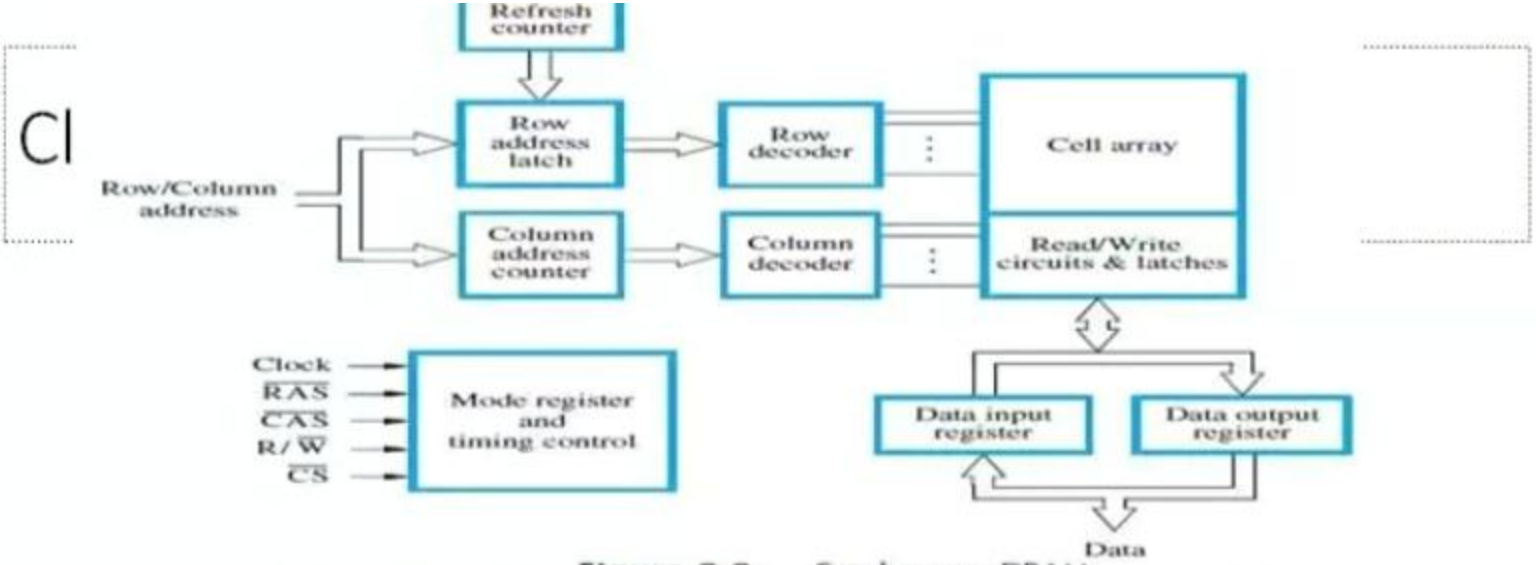
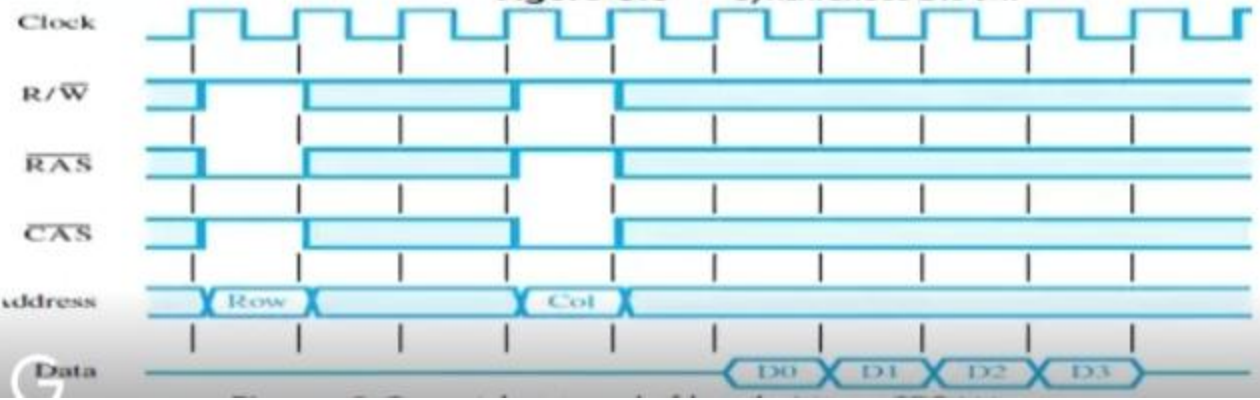


Figure 8.8 Synchronous DRAM.



- A Read-operation causes the contents of all cells in the selected row to be loaded in these latches.
- Data held in latches that correspond to selected columns are transferred into data-output register.
- Thus, data becoming available on the data-output pins.
- First, the row-address is latched under control of RAS" signal (Figure 8.9).
- The memory typically takes 2 or 3 clock cycles to activate the selected row.
- Then, the column-address is latched under the control of CAS" signal.
- After a delay of one clock cycle, the first set of data bits is placed on the data-lines.
- SDRAM automatically increments column-address to access next 3 sets of bits in the selected row.

Burst mode transfer

- As in fast page mode, after the column address is applied, the data from successive addresses are read out or written into.
- In the same way burst operations of different lengths can be specified.
- This uses the same block transfer capability of fast page mode.
- Here the control signals required are provided internally by column counter and clock signals.
- New set of data are available in the data lines after every clock cycle.
- All operations are triggered at the rising edge of the clock.

- A Read-operation causes the contents of all cells in the selected row to be loaded in these latches.
- Data held in latches that correspond to selected columns are transferred into data-output register.
- Thus, data becoming available on the data-output pins.
- First, the row-address is latched under control of RAS' signal (Figure 8.9).
- The memory typically takes 2 or 3 clock cycles to activate the selected row.
- Then, the column-address is latched under the control of CAS" signal.
- After a delay of one clock cycle, the first set of data bits is placed on the data-lines.
- SDRAM automatically increments column-address to access next 3 sets of bits in the selected row.

- **LATENCY & BANDWIDTH**
- A good indication of performance is given by 2 parameters: 1) Latency 2) Bandwidth.
- **Latency**
- It refers to the amount of time it takes to transfer a word of data to or from the memory.
- For a transfer of single word, the latency provides the complete indication of memory performance.
- For a block transfer, the latency denotes the time it takes to transfer the first word of data.
- **Bandwidth**
- It is defined as the number of bits or bytes that can be transferred in one second.
- Bandwidth mainly depends on

1) The speed of access to the stored data &
2) The number of bits that can be accessed in parallel.

- **DOUBLE DATA RATE SDRAM (DDR-SDRAM)**
- The standard SDRAM performs all actions on the rising edge of the clock signal.
- The DDR-SDRAM transfer data on both the edges (loading edge, trailing edge).
- The Bandwidth of DDR-SDRAM is doubled for long burst transfer.
- To make it possible to access the data at high rate, the cell array is organized into two banks.
- Each bank can be accessed separately.
- Consecutive words of a given block are stored in different banks.
- Such interleaving of words allows simultaneous access to two words.
- The two words are transferred on successive edge of the clock.
-

SPEED, SIZE COST

Characteristics	SRAM	DRAM	Magnetis Disk
Speed	Very Fast	Slower	Much slower than DRAM
Size	Large	Small	Small
Cost	Expensive	Less Expensive	Low price

Memory	Speed	Size	Cost
Registers	Very high	Lower	Very Lower
Primary cache	High	Lower	Low
Secondary cache	Low	Low	Low
Main memory	Lower than Seconadry cache	High	High
Secondary Memory	Very low	Very High	Very High

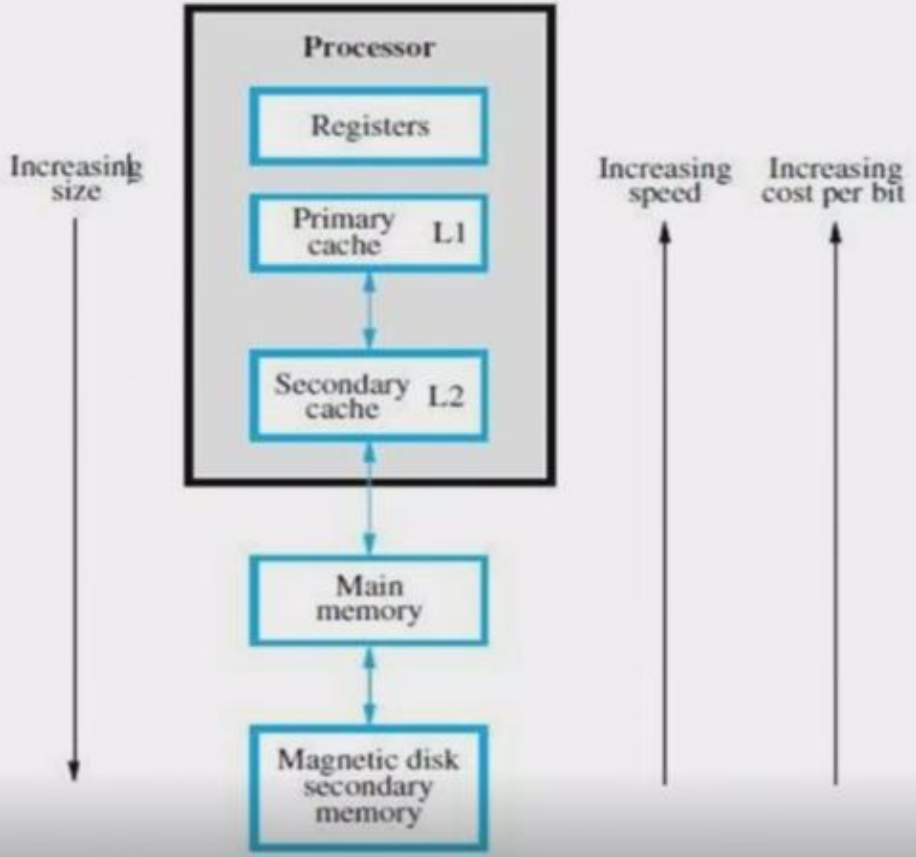


Figure 8.14 Memory hierarchy.

- The main-memory can be built with DRAM (Figure 8.14)
- Thus, SRAM"s are used in smaller units where speed is of essence.
- The Cache-memory is of 2 types:

1) **Primary/Processor Cache** (Level1 or L1 cache)
   - It is always located on the processor-chip.
2) **Secondary Cache** (Level2 or L2 cache)
   - It is placed between the primary-cache and the rest of the memory.

- The memory is implemented using the dynamic components (SIMM, RIMM, DIMM).
- The access time for main-memory is about 10 times longer than the access time for L1 cache.