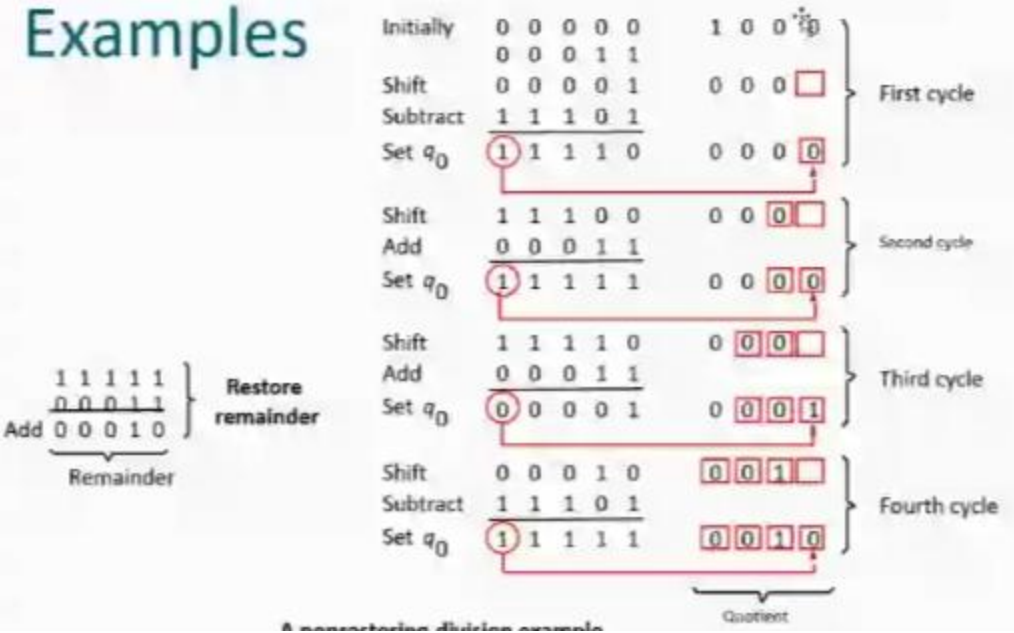
- The n bit +ve divisor is loaded into reg M & n bit +ve dividend is loaded in reg Q at the start of operation. Reg A is set to 0
- Shift left both reg's
- If the sign of A is '0' , subtract M from A, otherwise add M to A
- Now, if the sign of A is '0', set quotient to 1, otherwise set quotient to 0
- Steps 2,3 & 4 are repeated n times
- If the sign of A is 1, add M to A

# Examples


Initially 0 0 0 0 0 1 0 0 0
0 0 0 1 1
Shift 0 0 0 0 1 0 0 0
Subtract 1 1 1 0 1
Set $q_0$ 1 1 1 1 0 0 0 0 0
First cycle
Shift 1 1 1 0 0 0 0 0
Add 0 0 0 1 1
Set $q_0$ 1 1 1 1 1 0 0 0 0
Second cycle
Shift 1 1 1 1 0 0 0 0
Add 0 0 0 1 1
Set $q_0$ 0 0 0 0 1 0 0 0 1
Third cycle
Shift 0 0 0 1 0 0 0 1
Subtract 1 1 1 0 1
Set $q_0$ 1 1 1 1 1 0 0 1 0
Fourth cycle
Quotient
1 1 1 1 1
0 0 0 1 1
Add 0 0 0 1 0
Restore remainder
Remainder

- 00011
- 11100
- 1

- 00001
- 11101
- 11110

# 8/3(4 bit)

| | A | Q |
|---|---|---|
| • | 00000 | 1000 |
| • | M 00011 | |
| SHIFT LEFT A & Q | 00001 | 000_ |
| A-M | 00011 | |
| | 11110 | 0000 |
| SHIFT LEFT A & Q | 11100 | 000_ |
| A+M | 00011 | |
| | 11111 | 0000 |
| SHIFT LEFT A & Q | 11110 | 000_ |
| A+M | 00011 | |
| | 1 00001 | 0001 |

# Chapter 7. Basic Processing Unit

Click to add subtitle

# Overview

- Instruction Set Processor (ISP)
- Central Processing Unit (CPU)
- A typical computing task consists of a series of steps specified by a sequence of machine instructions that constitute a program.
- An instruction is executed by carrying out a sequence of more rudimentary operations.

# Fundamental Concepts

- Processor fetches one instruction at a time and perform the operation specified.
- Instructions are fetched from successive memory locations until a branch or a jump instruction is encountered.
- Processor keeps track of the address of the memory location containing the next instruction to be fetched using Program Counter (PC).
- Instruction Register (IR)

# Executing an Instruction

- Fetch the contents of the memory location pointed to by the PC. The contents of this location are loaded into the IR (fetch phase).

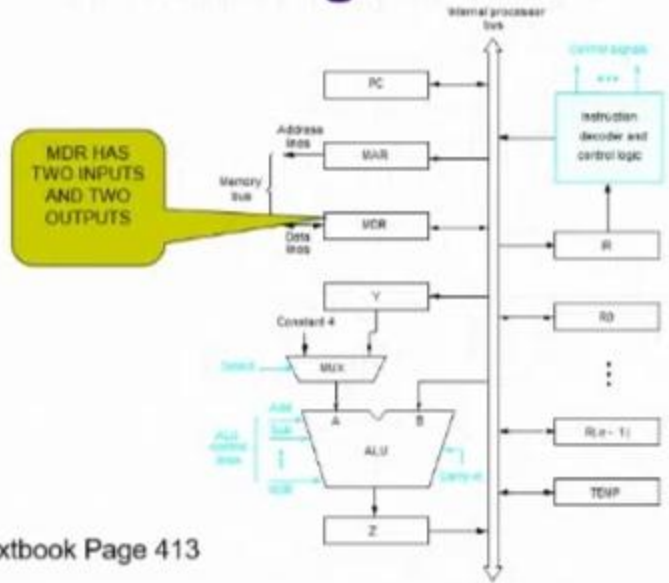
$$IR \leftarrow [[PC]]$$

- Assuming that the memory is byte addressable, increment the contents of the PC by 4 (fetch phase).

$$PC \leftarrow [PC] + 4$$

- Carry out the actions specified by the instruction in the IR (execution phase).

# Processor Organization




Datapath

Textbook Page 413