









Limitations of Verilog for Verification

- Weak randomization br. Snasan
- **Dr. Shasanka Sekhar Rout** has left the meeting.
- Limited constructs for handling large data for complex design
- Automating verification process is difficult
- Lack of standard methodology
- Achieving higher level <u>abstractions</u> is difficult









Industry that offer ASIC Design

This meeting is being recorded cation Jobs









