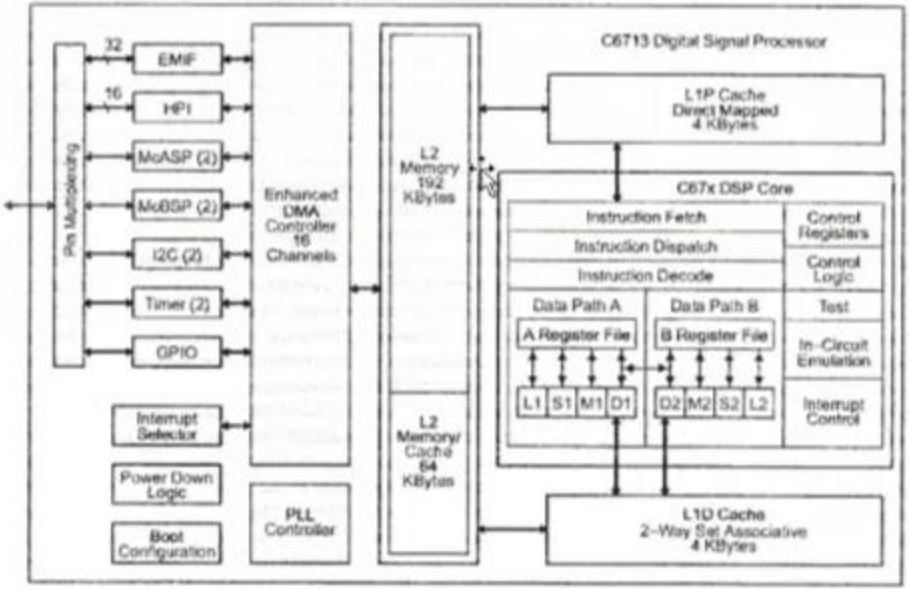
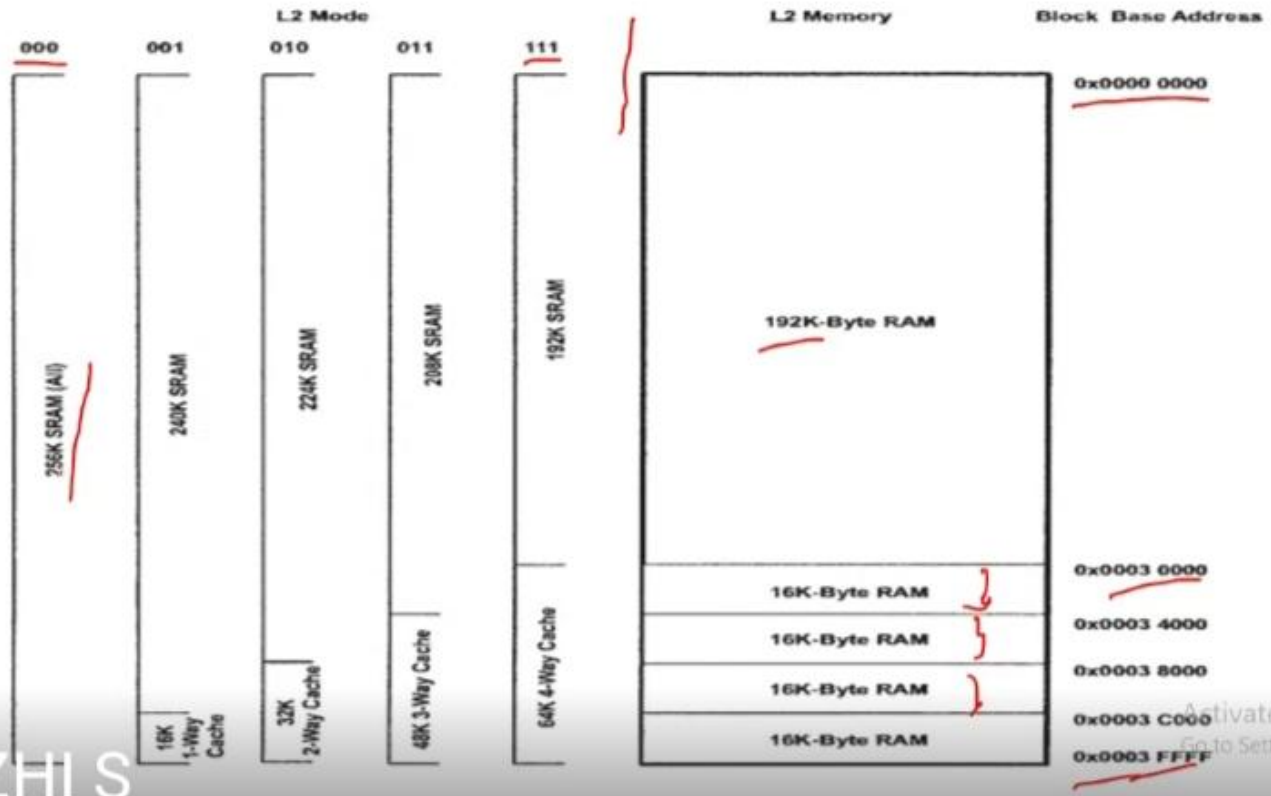
# ARCHITECTURE OF TMS320C6X



# INTERNAL MEMORY CONFIGURATION OF L2



# Fetch and Execute packets

FP EP

An execute packet (EP) consists of a group of instructions that can be executed in parallel within the same cycle time. The number of EPs within a fetch packet (FP) can vary from one (with eight parallel instructions) to eight (with no parallel instructions). The least significant bit of every 32-bit instruction is used to determine if the next or subsequent instruction belongs in the same EP (if 1) or is part of the next EP (if 0).

```
                Instruction A
||              Instruction B

                Instruction C
||              Instruction D
||              Instruction E

                Instruction F
||              Instruction G
||              Instruction H
```

# Pipeline phases and effects

| Program Fetch | | | | Decode | | Execute |
|---|---|---|---|---|---|---|
| PG | PS | PW | PR | DP | DC | E1–E6 (E1–E10 for double precision) |

| Clock Cycle | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 | E6 |
| | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 | E5 |
| | | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 | E4 |
| | | | PG | PS | PW | PR | DP | DC | E1 | E2 | E3 |
| | | | | PG | PS | PW | PR | DP | DC | E1 | E2 |
| | | | | | PG | PS | PW | PR | DP | DC | E1 |
| | | | | | | PG | PS | PW | PR | DP | DC |