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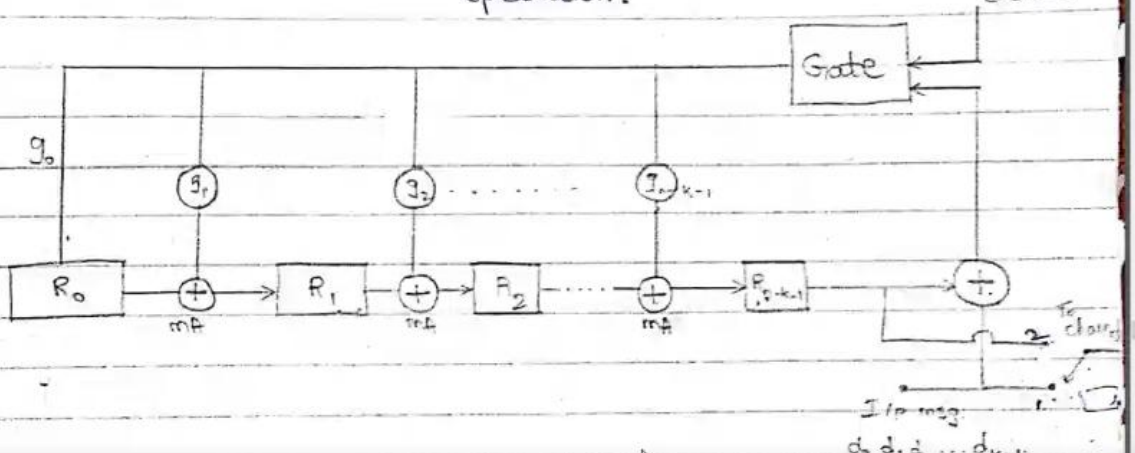
ii) (n-k) modulo-2 adders

iii) AND gate

iv) Counter to keep track of shifting operation.



It is assumed that at the occurence of the clock pulse, [illegible] fted into the registor

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contents of shift register are shifted into the channel.

Thus, the code vector $R_0 R_1 \cdots R_{n-k-1} D_0 D_1 D_2 \cdots D_{k-1}$ is generated & sent over the channel.

P> Design an encoder for (7,4) binary cyclic code generated by $g(x) = 1 + x + x^3$ and verify its operation using message vector (1001) and (1011)

$n - k =$

ex

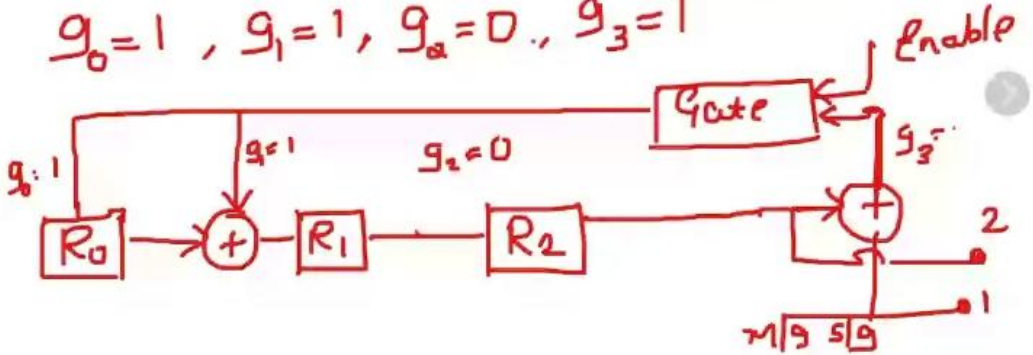
is given by

$n-k = 3$ bit shift register

$g(x) = 1 + X + X^3$

$g(x) = g_0 + g_1 X + g_2 X^2 + g_3 X^3 + \cdots$

$g_0 = 1,\ g_1 = 1,\ g_2 = 0,\ g_3 = 1$



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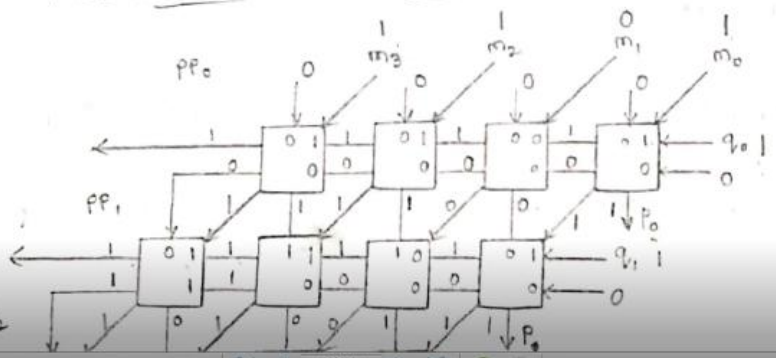
Done

example.

Ex: $1101 \times 1011 \Rightarrow 13 \times 11$

$$\begin{array}{r} 1101 \\ 1101 \\ 0000 \\ 1101 \\ \hline 10001111 \end{array} \qquad 143$$

UNSIGNED MULTIPLICATION USING COMBINATIONAL CIRCUIT:



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MULTIPLICATION :-

Multiplication of Unsigned numbers :

The product of 2 'n' digit nos can be accomodated in '2n' digits, so that the product of 2 '4'-bit numbers fits into 8-bit as shown below.

In the binary number system, the multiplication of Multiplicand by the Multiplier bit is 1, The Multiplicand is entered in the appropriate position to be added to the partial product. If multiplier bit is 0, then 0's are entered as shown in the example.

Ex: $1101 \times 1011 \Rightarrow \frac{13 \times 11}{143}$

(M: 1101, Q: 1011)

1101

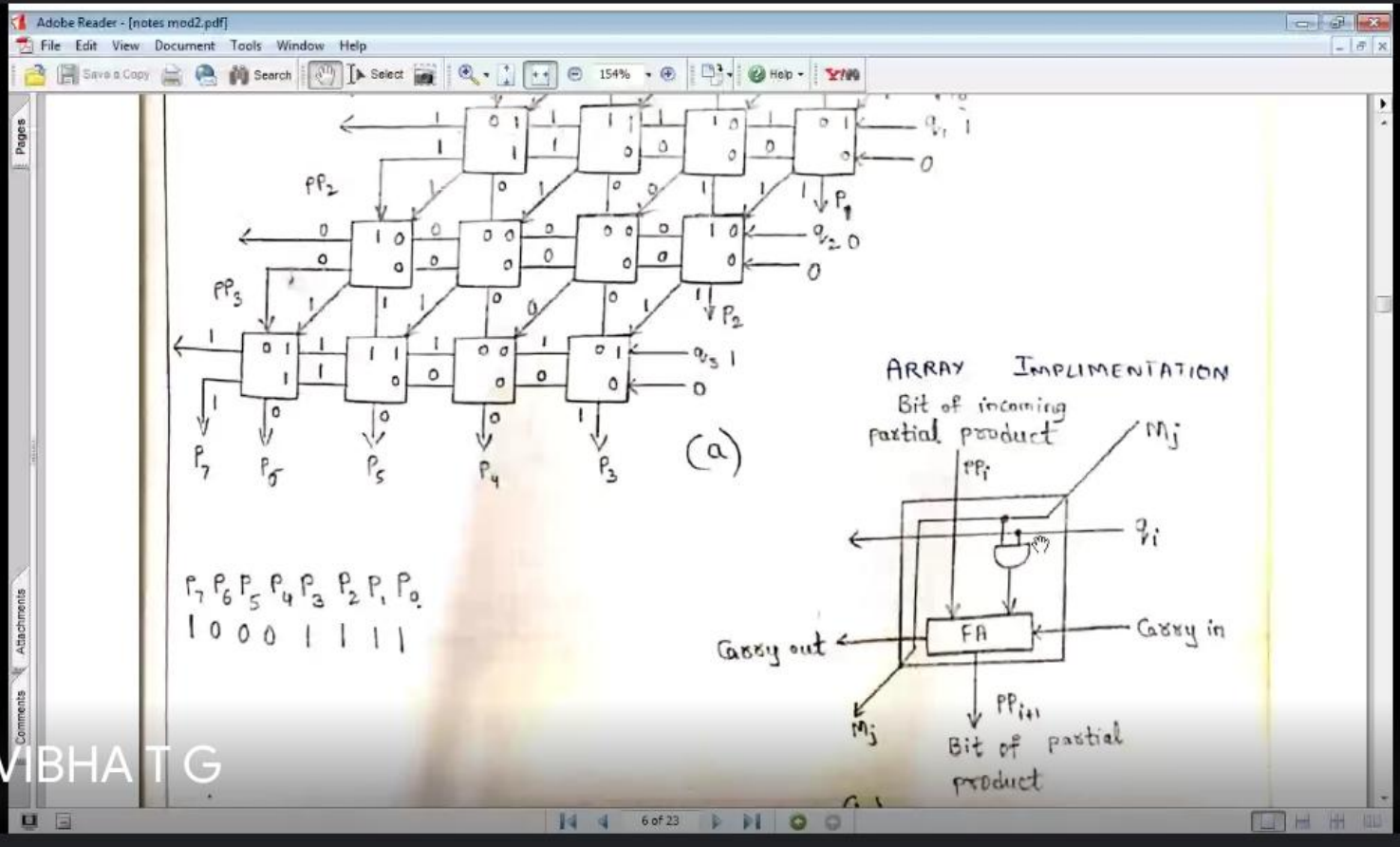
1101

0000

1101

6 of 23

VIBHA T G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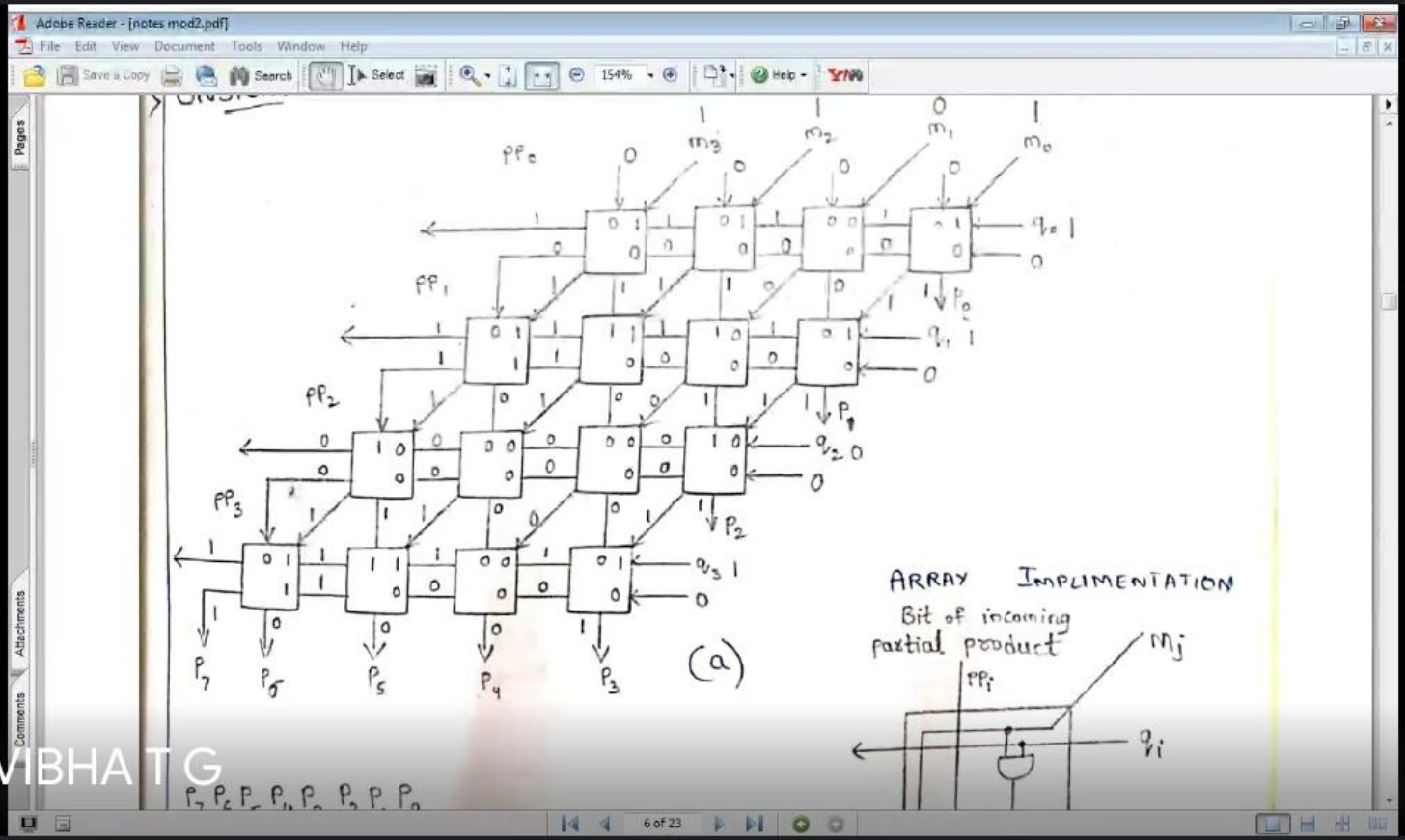
(a)
P7 P6 P5 P4 P3 P2 P1 P0
1 0 0 0 1 1 1 1
ARRAY IMPLIMENTATION
Bit of incoming partial product
PPi
Mj
qi
FA
Carry out
Carry in
PPi+1
Bit of partial product
6 of 23

VIBHAT G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q0 1
q1 1
q2 0
q3 1
P7 P6 P5 P4 P3 P2 P1 P0
(a)
ARRAY IMPLIMENTATION
Bit of incoming partial product
mj
ppi
qi
6 of 23

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