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(An Autonomous Institute Affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)
(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – II

Course Name : Computer Organization	Date :	11/11/2020
Course Code : 18EC5DEACO	Day :	Wednesday
Semester : 5 th Semester	Timings :	9:30-11:00AM
Max Marks : 50 M	Duration :	1½ Hrs.

No.		Question Description	Mks	CO & Levels
Q1	(a)	Which representation is most efficient to perform arithmetic operations on the numbers? i) Sign-magnitude ii) 1's complement iii) 2'S complement iv) None of the mentioned	1	
	(b)	If n bit is multiplied with n bit generates i) n/2 bit product ii) n bit product iii) 2n bit product iv) n^2 it product	1	
	(c)	The Booth recorded multiplier for 01110 is i) +1 0 0 -1 0 ii) -1 1 0 +1 0 iii) 0 +1 0 0 -1 iv) None of them	1	
	(d)	All the statements in a program will have ___ common steps for execution. i)4 ii) 3 iii) 7 iv) 8	1	
	(e)	___ bus processor will take less time to execute an instruction. i)Single ii) double iii) Multiple iv) all of the above	1	
	(f)	Represent the decimal value of 14 in 2's complement (a)0001111(b)1110000 (c)0001110(d)0101110	1	
	(g)	_____ is used to choose between incrementing the PC or performing ALU operations. i) Conditional codes ii) Multiplexer iii) Control unit iv) None of the mentioned	1	
	(h)	If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit. i) Micro programmed ii) Software iii) Logic iv) Hardwired	1	
	(i)	___ gate need to active for loading a value to MAR. i)MARin ii) MARout iii) MDRin iv) none of the above	1	
	(j)	Register x, y, and z are used by _____. i)programmer ii) Processor iii) both iv) none of the above	1	
Q2		Perform signed multiplication of following 2'scomplement numbers using i)Booth's Algorithm ii) bit-pair recoding method. a) A=010111 and B=110110 b) A=110101 and B=011011	10	CO3&L3
Q3		Elaborate the working of single bus organization with neat diagram.	10	C04&L2
Q4	(a)	Perform the multiplication of **9X15**using sequential multiplication with neat diagram. (5 bits)	5	C03&L3
	(b)	Explain with neat diagram the organization of fetching a word from memory.	5	C03&L3
		OR		
Q5		Show and explain how the micro code is generated for an instruction with example.	10	C03&L3
Q6	(a)	List the control sequences required to execute the instruction **ADD R1,(R3)** in single bus organization.	5	C04&L3
	(b)	Describe with neat diagram detailed Hardwired control organization.	5	C04&L3
		OR		
Q7		Elaborate the working of multiple bus organization with neat diagram.	10	C04&L3