Sample question bank
Computer Organization - -18EC5DEACO

MODULE 1

1. List the steps needed to execute the machine instruction Add LOC, R0 in terms of transfers between memory and processor and some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC.

2. Give a short sequence of machine instructions for the task: "Add the contents of memory location A to those of location B, and place the answer in location C."
   a. Instructions Load LOC, R_i
   b. and Store R_i, LOC
   c. are the only instructions available to transfer data between the memory and general purpose register R_i. Do not destroy the contents of either location A or B.

3. Explain different functional units of a digital computer. Mention the functions of different processor registers a)IR b)MAR c)PC

4. What is a bus? Explain single bus structure in architecture.

5. Explain how will you measure the performance of a computer.

6. Explain the methods to improve the performance of a computer.

7. Register R5 is used in a program to point to the top of a stack. Write a sequence of instructions using the Index, Auto increment, and Auto decrement addressing modes to perform each of the following tasks:
   a. Pop the top two items off the stack, and them, and then push the result onto the stack.
   b. Copy the fifth item from the top into register R3.
   c. Remove the top ten items from the stack.

8. Explain Big-Endian, Little-Endian assignment and byte addressability.

9. Explain the Instruction Sequencing and its complete execution.

10. Mention the four types of operations to be performed by an instruction in a computer

11. What is Addressing Mode? Explain any 4 Addressing modes with examples.

12. Write notes on:
a) Register transfer notation. B) Assembly language Notation

13. What is Stack? Explain with examples Push and POP operations.

14. Bring out the comparison between stacks and queues.

15. Write a brief note on Input and output operations with a neat diagram.

16. Write a note on RISC and CISC machines.

17. Describe the use of ROTATE & SHIFT Instructions with examples

18.Explain logical shift and rotate instructions with examples.
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19. Register RI and R2 of computer contain the decimal value 1200 and 4600. What is the effective address of the source operand in each of the following instructions? Also mention addressing modes.

Load 20(Rl), R5

i) Hove # 3000, R5
ii) Store R5, 30(Rl, R2)
iii) Add -(R2), R5
iv)Subtract (RI)+, R5.

20 .What is subroutine? Explain subroutine linkage with a link register.
21.Write basic performance equation. Explain the role of each of the parameters in the equation on the performance of computer.
22. Consider a Processor with 120 instructions set, of which 45% instructions consume 1 machine cycle, 25% instruction consume 2 machine cycle and remaining instructions consume 3 machine cycle time. Calculate the execution time of the process if operating frequency is 1 GHz and 6 clock cycles make 1 machine cycle.

23. Explain subroutine nesting with an example.

24. .Write a program to evaluate the expression **A*B+C*D** .
using i)one address machine instruction, ii)Zero address instruction.

25.Evaluate the expression

$$A = B * (C + D * E - F/G).$$

Using i)Three address instruction. ii)Two address instruction.

26. Register R5 is used in a program to point to the top of a stack. Write a sequence of instructions using the Index, Autoincrement, and Autodecrement addressing modes to perform each of the following tasks:

a) Pop the top two items off the stack, and them, and then push the result onto the stack.
b) Copy the fifth item from the top into register R3.

Other related problems/programs.

Module 2-Arithmetic

1. Explain 2's complement Adder/ Subtracter with a suitable block diagram.
2. Differentiate restoring and non restoring division.
3. Write the algorithm for binary division using restoring division method.
4. Explain floating-point addition and subtraction with a suitable example and also give the h/w structure for that.
5. Give the procedure for floating-point multiplication and division.
6. Design a 16-bit adder using 4-bit ripple-carry adder blocks.
7. Write a note on IEEE standard for floating-point numbers.
8. Write the complete logic diagram of 4-bit carry-look ahead adder. How many logic gates are required?
   08M
9. Multiply each of the following pairs of signed 2's – complement numbers using Booth Algorithm. A is the multiplicand and B is the multiplier. What is your observation in each case?
   a) A = 010111, B = 1101 b) A = 111000, B = 011111
   c) A = 001110, B = 001110 d) A = 001101, B = 010101

10. Multiply each of the following pairs of signed 2's – complement numbers using bit-paring of the multipliers. A is the multiplicand and B is the multiplier. What is your observation in each case?
    a. A = 010111, B = 110110
    b. A = 111000, B = 011111
    c. A = 001110, B = 001110
    d. A = 001101, B = 010101

11. Using Booths multiplication algorithm multiply -13 and +107.

12. Show the sequential multiplication process for each of the following pairs of numbers. X is the multiplier and Y is the multiplicand.
    a. a) X = 0101, Y = 1101 b) X = 1110, Y = 0111

13. Perform the operation of division using a) restoring and b) non-restoring method on the following pairs of numbers. X is the divisor and Y is the dividend.
    a) X = 0101, Y = 11111 b) X = 1001, Y = 10010

14. Represent the following decimal numbers using IEEE standard floating point notation.
    a) +1.725 b) –25.125 c) –0.08125 d) +45

15. With a neat block diagram explain unsigned multiplication using array implementation or combinational circuit.

16. Perform the multiplication of **9X15**using sequential multiplication with neat diagram. (5 bits).

17. Represent the following number in double precision floating point notation.**$(-45.125)_{10}$**

18. Perform the division of 16/5 using Non-restoration technique with neat diagram.(5 bits) 05M
19. Convert the following single precision floating point number into actual decimal number. **(C4900000).**
20. Describe floating point division with an example

21. Represent the following decimal values 5,-2,-10,-19,-112 and -98 as signed 8 bit numbers in the following binary formats
    i)Sign and Magnitude
    ii)1's Complement
    iii)2's Complement

22. Discuss the advantages of carry look ahead adder over ripple carry adder .Also with a neat block diagram explain a 32 bit carry look ahead adder.
23. Represent $(56)_{10}$ and $(-56)_{10}$ in sign magnitude 1's complement and 2's Complement form.
24. Represent the number 81234561 in 32 bit Big Endian and Little Endian memory Organization.
25. Explain 4bit carry look ahead adder and use it to build 12 bit carry look ahead Adder.
26. Explain how a 16 bit carry look ahead adder can be built from 4 bit adder.

27. Show the multiplication of (+13) and (-6) using multiplier bit pair recording technique.
28. Explain the IEEE standard for floating point number representation.
29. Explain Booth's algorithm. Multiply 01110(+14) and 11011(-5) using Booth's Multiplication.

30.Illustrate the steps for non restoring division algorithm for the following data:
Divident=1011 and divisor=0101.

31.If A and B are two single precision floating point numbers where
A=44900000H and B=42A00000H.Show the results for A+B and A-B.

Other related problems/programs.

Module 3 –Basic Processing Unit

1. Elaborate the working of single bus organization with neat diagram.

2. Explain in detail ALU operation in a single processor bus unit with an example.

3. Describe one bit organization of registers with a neat diagram.

4. Explain with neat diagram the organization of fetching a word in memory.

5. Elaborate on execution of a complete instruction in a single bus organization with an example.

6. Write and explain control sequences for the execution of an instruction SUB R1,(R4) for single bus organization.

7. Write and explain control sequences for the execution of an unconditional branch Instruction.

8. List the actions needed to execute the instruction ADD (R3),R1. Write the control sequences required to execute the instruction ADD (R3),R1 in single bus organization.

9. With the help of a neat sketch, explain three-bus organization of the processor with an example instruction.

10. Describe with neat diagram detailed Hardwired control organization.

11. Explain with a block diagram the basic organization of micro programmed control unit.

12.Compare hardwired control unit with multi programmed control unit.

13. Define the following terms: microinstruction, micro operation, microroutine, control word and control store.

14.Write microroutine for the instruction Add (Rsrc)+, Rdst.

Other related problems/programs.

Module -4 The Memory System

1. Sketch and explain organization of 256 x 8 SRAM memory.

2. Explain the Read/Write operation of an SRAM cell designed using CMOS, with the help of a neat diagram.

3. Describe the operation of 2M x 8 asynchronous DRAM chip.

4. Discuss the main features of SDRAM with a neat diagram.

5. Explain the working of a single-transistor dynamic memory cell.

6.With a neat block diagram explain the operation of 16 megabit DRAM configured as 2Mx8.

7. Describe the terms latency, bandwidth, locality of reference, mapping function and replacement algorithm, With reference to cache memory.

8. Write a block diagram of 256K x 8 memory using 256K x 1 chips.

9. Design a 4M x 32 module using 512K x 8 memory chips. Show the address lines and control signals required.

10. Discuss how read and write operations are carried out in a cache memory.

11. List out the parameters which are effecting the selection of a memory, and explain them briefly.

12. Explain different mapping functions used in cache memory.

13. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

a. How many bits are there in the tag, index, block and word fields of the address format?
b. How many blocks can the cache accommodate?

14. Consider a system having 512K main memory organized as 16K blocks of 32 words each and a cache memory of 16K arranged as 512 blocks of 32 words each. Show how the mapping is done using direct mapping.

15. A set-associative cache consists of 128 blocks divided into 4 block / set. The main memory has 8192 blocks each consists of 128 words.

a. How many address bits are required to access a main memory location?
b. What are the number of bits in TAG, SET and WORD fields?

16. Differentiate between Miss Penalty and hit rate.

17. What do you mean by memory interleaving? Explain

18. Explain with block diagram how TLB is used in implementing virtual memory.

19. Explain with a neat diagram virtual memory organization and also describe how address translation is done.

20. Show the organization of virtual memory address translation and explain its working.

21. Consider a cache memory of 256 blocks of 32 words each.Total cache size=8Kwords. Main memory is addressable by 24 bit address and each bock stores 32 words. Show with a neat mapping diagram how direct mapping ,associative mapping and set associate mapping are used for the above example explaining how memory blocks are placed in the cache.Also show the tag field,block and word field values for each of the above mentioned mapping tecchniques.

Other related problems/programs.

MODULE 5- INPUT/OUTPUT ORGANIZATION

1. What is Program Controlled I/O? Explain.

2. Differentiate memory mapped I/O and I/O mapped I/O

3. What is Interrupt driven I/O? Explain how an I/O is serviced?

4. What is an ISR? Write how interrupts are enabled or disabled.

5. With flow diagram, explain each step involved in interrupt driven I/O processing

6. Explain any two methods of handling multiple I/O devices.

7. What are Vectored Interrupts? Explain.

8. What are Priority Interrupts? Explain.

9. Describe the operation of DMA in detail.

10. What is bus arbitration? Explain how it is resolved when requested for service by both processor and memory.

11. Explain different types of arbitration.

12. Describe the need of enabling and disabling of interrupts and also mention the steps for enabling and disabling the interrupts.

13.Explain Interrupt priority schemes.

14.Write a note on exceptions.

15.Write a note on privileged exceptions.

16. What is Synchronous Bus Transfer? Explain with a timing diagram.

17. What is Asynchronous Bus Transfer? Explain with a timing diagram.

18. What is an Interface? Write a note on its types.

19. Write a note on Serial Interface.

20. Write a note on Parallel Interface.

21. Write a note on Standard Interfaces.

22. Write a note on Peripheral Component Interconnect (PCI) Bus.

23. Explain data transfer using PCI Bus.

24. Write a note on SCSI bus signals.

25. Differentiate all the three buses.
26. Write a note on USB protocols.
27. Explain how a read operation is performed using PCI Bus.

28. Explain the USB architecture with a neat diagram.

29. a) Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line.
b) Which type of I/O devices is interfaced through DMA?
c) Explain the bus-arbitration process used for DMA.

30. With a block diagram, explain how a keyboard is connected to a processor.

31.Explain with block diagram and an interface circuit showing Keyboard interfaced to processor.

32.Explain in detail with a block diagram and an interface circuit showing how the printer is interfaced to processor.

33.Explain general 8 bit parallel interface.

34.How are simultaneous interrupts from more than one devices are handled?

35.Define the terms cycle stealing and block mode/burst mode.

36.Write a note on any one bus arbitration scheme.

Other related problems/programs.