Week 4: Assignment Solutions

1. Which of the following statements are true for horizontal micro-instruction encoding?
    a. If there are *k*control signals, every control word stored in control memory (CM) consists of *k* bits, one bit for every control signal.
    b. Parallel activation of several micro-operations in a single time step can be performed.
    c. Parallel activation of several micro-operations in a single time step cannot be performed.
    d. None of the above

    Correct answer is (a) and (b).

    In horizontal microinstruction encoding, there is one separate bit for every control signal. Hence any number of control signals can be activated simultaneously.

2. Which of the following instructions can be used for storing the contents of processor register R1 to memory location LOCA in a typical RISC architecture? The first operand is destination and second operand is source.
    a. LOAD R1, LOCA
    b. STORELOCA, R1
    c. MOVE LOCA, R1
    d. STORE R1, LOCA

    Correct answer is (b).

    In typical RISC architecture, the STORE instruction is used to move the contents of a register to a memory location.

3. Which of the following set of control signals can be used totransfer data from register R4 to register R5?
    a. $R4_{out}$, $R5_{in}$
    b. $R4_{out}$, MAR_{in}, MDR_{out}
    c. $R5_{out}$, $R4_{in}$
    d. $R5_{out}$, MAR_{in}, $R4_{in}$

    Correct answer is (a).

    For the data transfer to take place, the data output of register R4 should be enabled ($R4_{out}$) and the data load control of R5 should be activated ($R5_{in}$).

4. Which of the following statements are true when the control signalsPC_{out}, MAR_{in}, and READ are activated simultaneously?
    a. Content of PC is made available in the internal processor bus
    b. The content of PC is moved to MAR and MDR
    c. The instruction fetch operation is activated

d. The content of PC is moved to MAR

Correct answers are (a), (c) and (d).

When the control signals PC_{out} and MAR_{in} are activated, the contents of PC will get transferred via the internal processor bus to the MAR register. And since READ is also active, the address in MAR will be used to initiate a read operation to memory to fetch the next instruction.

5. The minimum number of time steps needed to execute the instruction "ADD R1, R2" (Meaning: R1 ← R1 + R2) in a single bus architecture will be …….. Consider the single bus architecture provided in the slides for the calculation.

Correct answer is 6.

Steps	Action
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}
4	$R1_{out}$, Y_{in}
5	$R2_{out}$, SelectY, Add, Z_{in}
6	Z_{out}, $R1_{in}$, End

6. The minimum number of time steps needed to execute the instruction "ADD R1,LOCA" (Meaning: R1 ← R1 + Mem[LOCA]) in a single bus architecture will be …….. Consider the single bus architecture provided in the slides for the calculation.

Correct answer is 7.

Steps	Action
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}
4	Address field of IRout, MAR_{in}, Read
5	$R1_{out}$, Y_{in}, WMFC
6	MDR_{out}, SelectY, Add, Z_{in}
7	Z_{out}, $R1_{in}$, End

7. Consider the instruction set architecture of a general-purpose machine. Suppose that a total of 20 control signals are present, out of which 7 are mutually exclusive while the rest are not. The number of bits required in the control word (for microprogramming) will beat least …….. .

   Correct answer is 16.

   The 7 mutually exclusive signals can be encoded in ceiling($\log_2$ 7) = 3 bits, while the remaining 13 signals will remain un-encoded. So the number of bits in a control word will be 3 + 13 = 16.

8. Suppose an instruction set architecture of a general-purpose machine has a total of 126 control signals. The number of bits required in control word for horizontal and vertical micro-instruction encoding are:
   a. 126, 7
   b. 128, 7
   c. 7, 126
   d. 126, 8

   Correct answer is (a).

   For horizontal encoding, one bit is used for each control signal; therefore, we shall require 126 control signals.

For vertical encoding, the 126 control signals can be encoded in ceiling($\log_2$ 126) = 7 bits.

9. Which of the following is true for MIPS32 register bank?
    a. There is one read port and one write port.
    b. There is one read port and two write ports
    c. There are two read ports and one write port
    d. None of the above

    Correct answer is (c).

    In MIPS32 architecture, two register operands are prefetched during the ID stage, which required two read ports in the register bank. Also, for pipelined implementation, a register write can occur during WB. Thus two read and one write ports are required in the register bank.

10. Which of the following is true for the ID(Instruction Decode) stage of the MIPS32 data path?
    a. The instruction is decoded.
    b. Two register operands are read from the register bank.
    c. The PC is incremented.
    d. All of the above.

    Correct answers are (a) and (b).

    For the MIPS32 instruction execution, the instruction is decoded and the register operands are pre-fetched during ID stage.

11. Which of the following is not true for a branch instruction in MIPS32?
    a. The target address is computed in EX stage.
    b. The new PC value is loaded in the MEM stage.
    c. The branch condition is computed in ID stage.
    d. The WB stage is not required.

    Correct answer is (c).

    The branch condition is computed in the EX stage.

12. For the MIPS32 data path, the total number of micro-operations required to execute the instruction LW R4, 400(R5) will be ……

    Correct answer is 8.

    The micro-operations will be:

    i. IR = Mem [PC]
    ii. NPC = PC + 4
    iii. A = Reg [rs]
    iv. Imm = $(IR_{15})^{16}$ ## $IR_{15..0}$
    v. ALUout= A + Imm
    vi. PC = NPC
    vii. LMD = Mem [ALUOut]
    viii. Reg [rt] = LMD