Module 1

- **Computer-Aided Design , Hardware Description Languages, Module modelling styles(ming bo lin), Verilog Description of Combinational Circuits,**
- **Data flow modelling-dataflow modelling, operands, operators, (ming bo lin), Verilog Modules, Verilog Assignments, Procedural Assignments), Modeling Flip-Flops Using Always Block, Always Blocks Using Event Control Statements.[Text book 1 and 3] Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code , Simple Synthesis Examples**
- TEXT BOOKS:Charles H Roth Jr., Lizy Kurian John, Byeong –kill-lee "Digital System Design using Verilog", *publisher Cengage learning*
- Ming-Bo Lin, "Digital System designs and Practices using Verilog H FPGAs", *John Wiley & Sons*, 2008

You

Introduction to verilog

- Complexity
- Tedious and Time consuming
- Hand drawn Schematics,breadbords and wires
- More and more components on a chip,
- Improvements have advanced the **VLSI** (very large scale integration) field

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- **SSI (small-scale integration),**
- **MSI (medium-scale integration),**
- **LSI (large-scale integration)**
- **All depends on the density of integration.**
- **SSI referred to ICs with 1 to 20 gates**
- **MSI referred to ICs with 20 to 200 gates**
- **LSI referred to devices with 200 to a few thousand gates**
- **Building blocks such as adders, multiplexers, decoders, regis ters, and counters are available as MSI standard parts.**
- **Term VLSI was coined, devices with 10,000 gates were called VLSI chips. The boundaries between the different categories are fuzzy today. Many modern microprocessors contain more than 100 million transistors. Compared to what was referred to as VLSI in its initial days**
- **Modern integration capability could be described as ULSI (ultra large integration). Despite the changes in integration ability and the fuzzy the term VLSI remains popular.**

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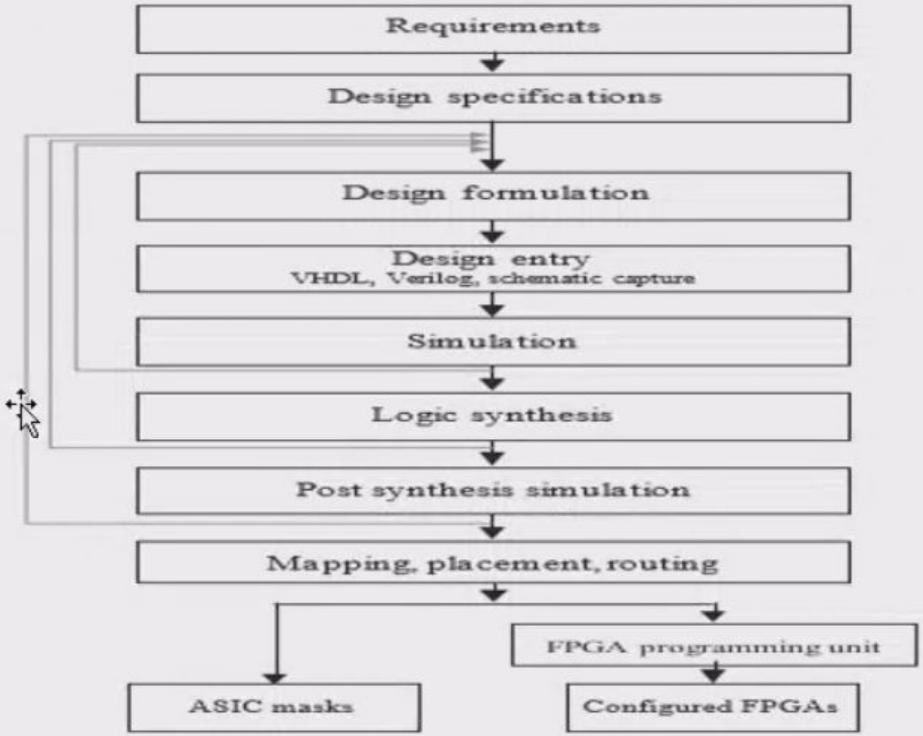
Computer-aided design

- **(CAD)** tools have advanced significantly during the past decade, and nowadays digital design is performed using a variety of software tools.
- Prototypes or even final designs can be created without discrete components and interconnection wires.

Design Flow in Modern Digital System Design



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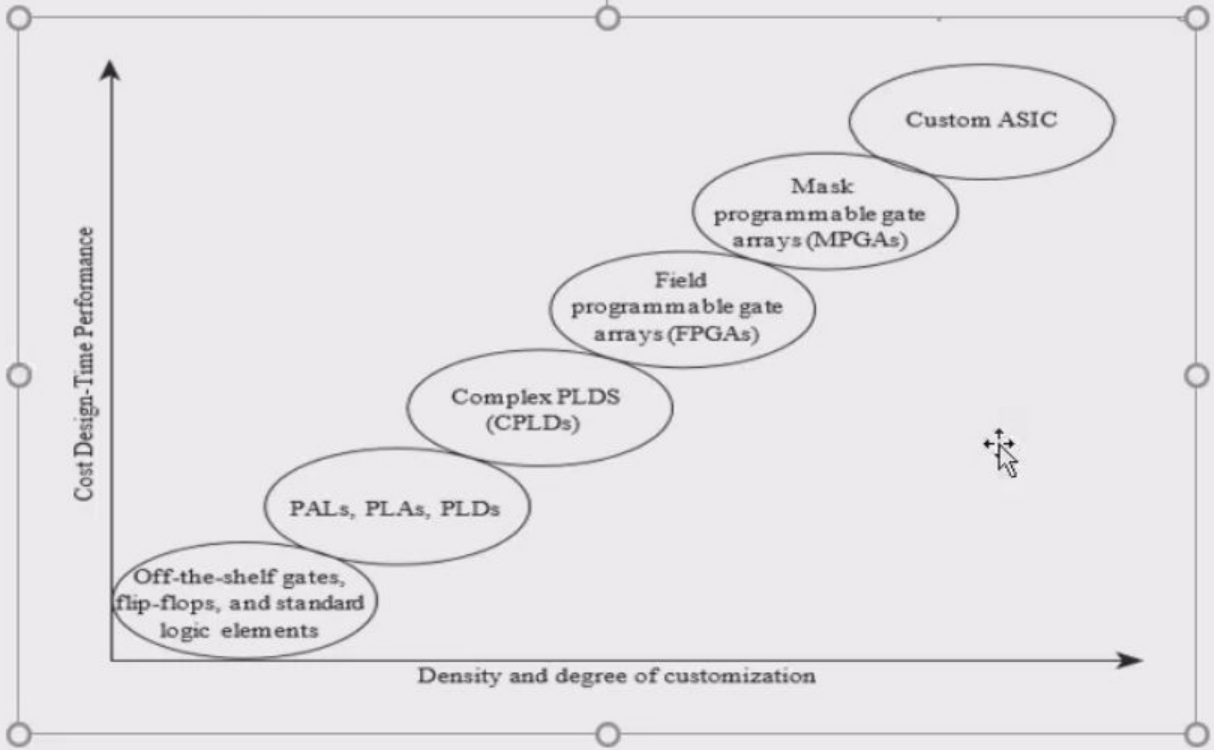
Spectrum of Design Technologies



Hardware Description Languages

- Hardware description languages (HDLs) are a popular mode of design entry for digital circuits and systems.
- There are two popular HDLs—VHDL and Verilog.
- Before the advent of HDLs, designers used graphical schematics and schematic capture tools to document and simulate digital circuits.
- A need was felt to create a textual method of documenting circuits and feeding them into simulators in the textual form as opposed to a graphic form.

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Verilog

- Verilog is a hardware description language used to describe the behavior and/ or structure of digital systems
- Verilog is a general-purpose hardware description language that can be used to describe and simulate the operation of a wide variety of digital systems, ranging in complexity from a few gates to an interconnection of many complex integrated circuits.
- VHDL was orig- inally developed under funding from the Department of Defense (DoD)
- Verilog was developed by the industry. It was initially developed as a proprietary language by a company called Gateway Design Automation around 1984.
- In 1990, Cadence acquired Gateway Design Automation and became the owner of Verilog. Cadence marketed it as a language and as a simulator, but it remained pro- prietary.
- At this time, Synopsis was promoting the concept of top-down design using Verilog. Cadence realized that it needed to make Verilog open in order to prevent the industry from shifting to VHDL and hence opened up the language.
- An organization called Open Verilog International (OVI) was formed, which helped to create a ven- dor- independent language specification for Verilog, clarifying many of the confusions around the proprietary specification. This was followed by an effort to create an IEEE standard for Verilog. The first Veri Standard was created in 1995, which was revised in 2001 and 2005. Synopsis created synthesis Verilog around 1988

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Module Modelling Styles

- Synthesis is process that converts HDL mdules into a structural description
- It s divided into logic synthesis and high level synthesis
- RTL description into gate level netlist
- High level description into RTL results’

- MODULES

- Two parts

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- Interface
- Internal

Modeling the Internal of a Module

- 1.Structural Style
  - -Gate Level
  - -Switch Level

2.Dataflow Style

-Module is specified as a set of continuous assignments statements

3.Behavioral or algorithmic style

4.Mixed style

-modelling Large Designs

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```
module toplevel(clock,reset);
 input clock;
  input reset;
  reg flop1;
  reg flop2;
always @ (posedge reset or posedge clock)
 if (reset)
   begin
      flop1 <= 0;
      flop2 <= 1;
      end
     else
begin
  flop1 <= flop2;
   flop2 <= flop1;
  end
 endmodule
```

You

Limitations of Verilog for Verification

- Weak randomizati
- Limited constructs for handling large data for complex design
- Automating verification process is difficult
- Lack of standard methodology
- Achieving higher level ***abstractions*** is difficult

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