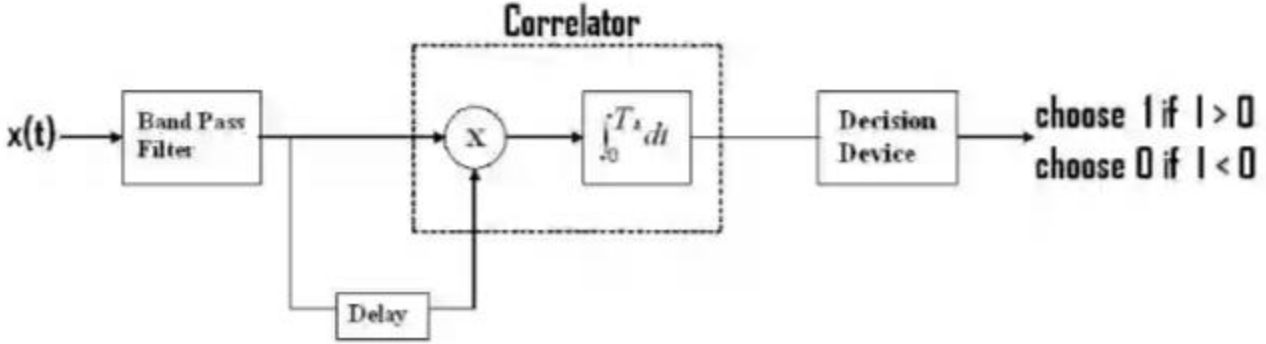


Fig. (b) DPSK Receiver

A DPSK system may be viewed as the non coherent version of the PSK. It eliminates the need for coherent reference signal at the receiver by combining two basic operations at the transmitter

(1) Differential encoding of the input binary wave and

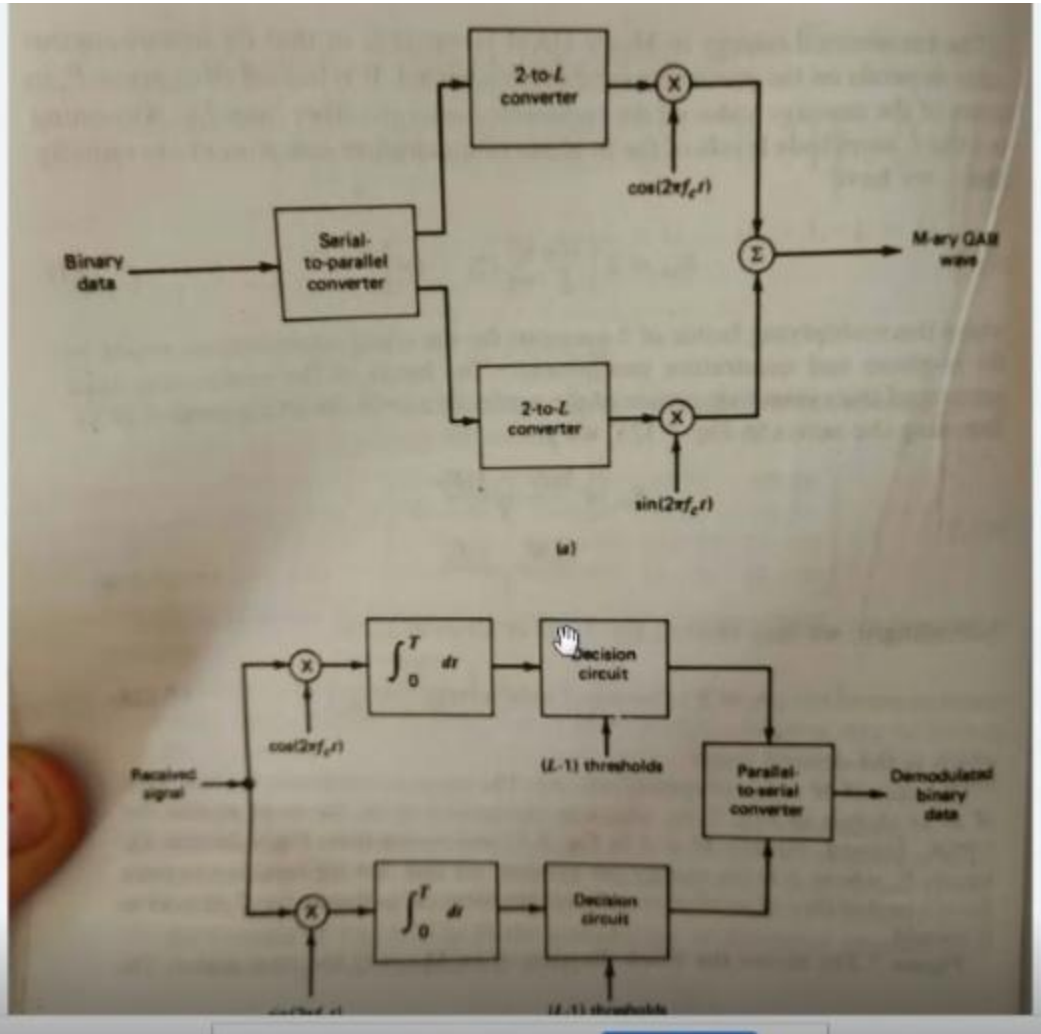
(2) Phase shift keying

$$d_k = d_{k-1} b_k \oplus \overline{d_{k-1}}\,\overline{b_k}$$

Where b_k is the input binary digit at time kT_b and d_{k-1} is the previous value of the differentially encoded digit. Table illustrate the logical operation involved in the generation of DPSK signal.

Input Binary Sequence $\{b_K\}$	1	0	0	1	0	0	1	1
Differentially Encoded 1 sequence $\{d_K\}$	1	0	1	1	0	1	1	1
Transmitted Phase 0	0	Π	0	0	Π	0	0	0
Received Sequence (Demodulated Sequence)	1	0	0	1	0	0	1	1

A DPSK demodulator is as shown in fig(b). The received signal is first passed through a BPF centered at carrier frequency f_c to limit noise power. The filter output and its delay version are a[illegible] correlator is proportional to the cosine of the difference between the carrier phase angles in the two correlator


2-to-L converter
cos(2πf_c t)
Binary data
Serial-to-parallel converter
M-ary QAM wave
2-to-L converter
sin(2πf_c t)
(a)
Received signal
Decision circuit
(L-1) thresholds
Parallel-to-serial converter
Demodulated binary data
Decision circuit