

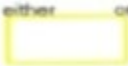





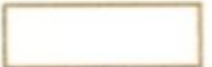





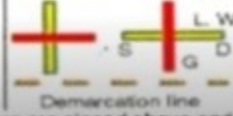
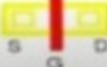
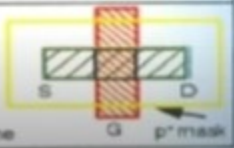




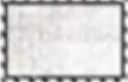
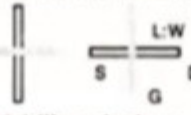
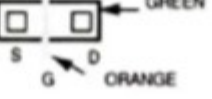
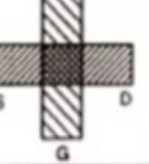

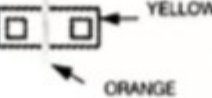





CMOS process

COLOR	STICK ENCODING	LAYER	MASK LAYOUT ENCODING	GIF LAYER
GREEN	Encoding as in Color plate 1 (a)	n-diff (n ⁺)	* Thinox = n-diff. + p-diff. + transistor channels	CAA or CNA
RED		Polysilicon	Encoding as in Color plate 1 (a)	CPF
BLUE		Metal 1		CMF
BLACK		Contact out		CC
GRAY		Overglass		COG
YELLOW (STICK)	 green outline here for clarity	p-diffusion (p ⁺ active)		CAA or CPA
YELLOW	Not shown on diagram	p ⁺ mask		CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	 Demarcation line p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK		V _{DD} or V _{SS} contact		CC
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)	
n-type enhancement mode transistor (as in Color plate 1 (a)) Transistor length to width ratio L/W may be shown.				
p-type enhancement mode transistor Note: p-type transistors are placed above and n-type below the demarcation line				

BiCMOS process

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE	MONOCHROME 	Polysilicon 2	MONOCHROME 	CPS
SEE COLOR PLATE 1(c)		Bipolar npn transistor	see Figure 3-13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor	n-well 	CCA
FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)	
<i>n</i> -type enhancement poly 2 transistor Transistor length to width ratio L:W may be shown.	DEMARICATION LINE 			
<i>p</i> -type enhancement poly 2 transistor Note: <i>p</i> -type transistors are placed above and <i>n</i> -type transistors below the demarcation line.	DEMARICATION LINE 			
<i>n</i> pn bipolar transistor			See Figure 3-13(f) and Color plate 6	

nMOS Design Style

The layout of nMOS involves

1. n-diffusion and other thinoxide regions –green
2. Polysilicon 1-red
3. Metal 1-blue
4. Implant-yellow
5. Contacts-black or brown

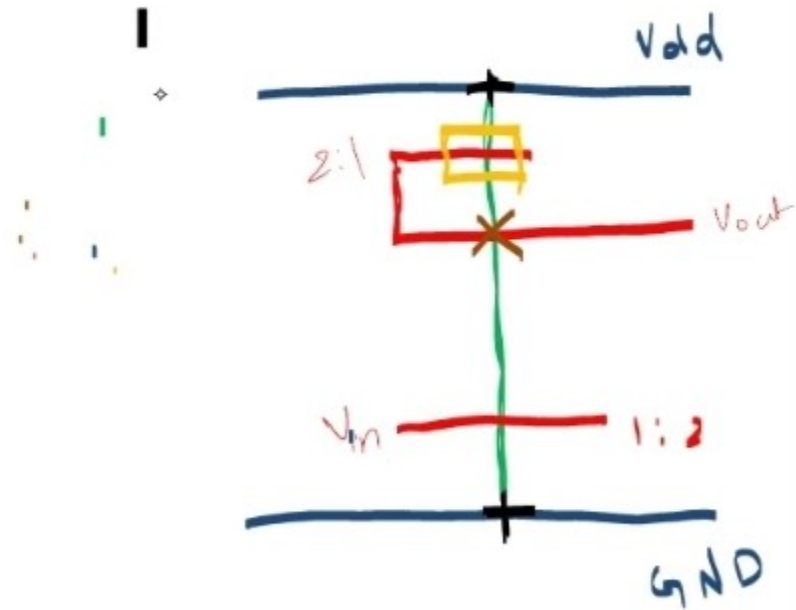
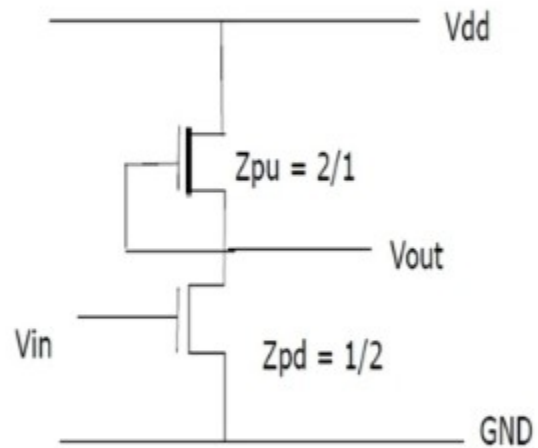
The Transistor is formed wherever poly crosses n-diffusion (red over green) and all diffusion wire(interconnection) are n-type(green)

Steps for Layout

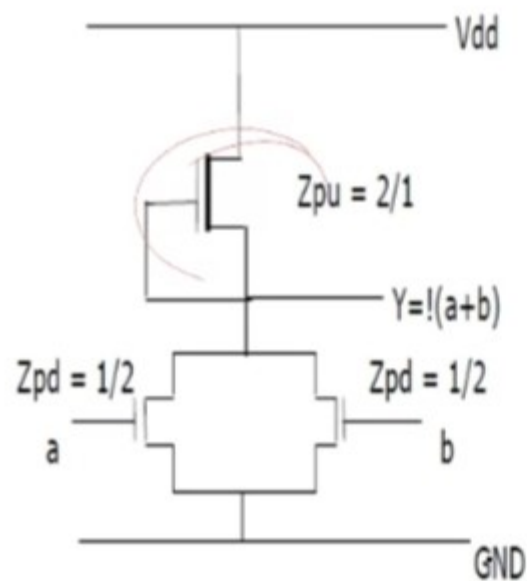
- Draw the meta(blue) VDD and GND rails
- Thinox(green) paths may be drawn between rails for inverters
- Depletion mode transistors connected from output point to VDD and pull-down structure of enhancement mode connected between output and GND
- Implants for depletion mode transistor
- Signal paths may also be switched by pass transistor
- Leaf-cell boundaries are conveniently shown on stick diagram

Examples

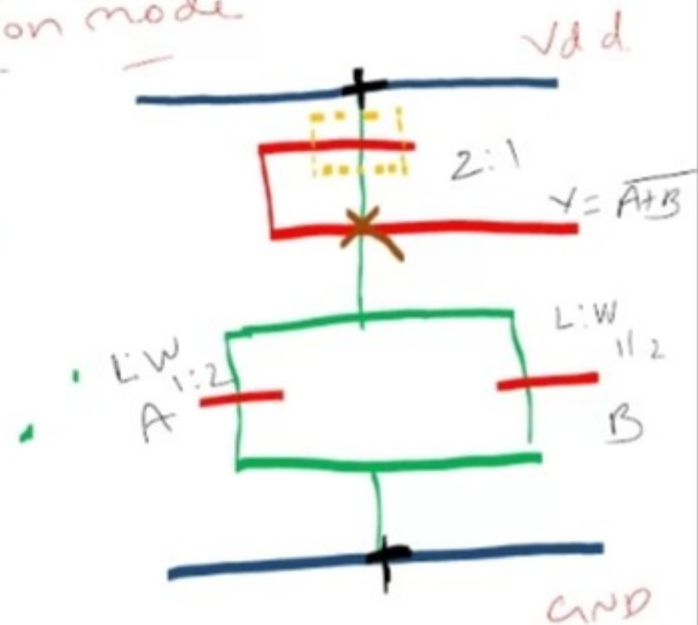
nMOS Inverter



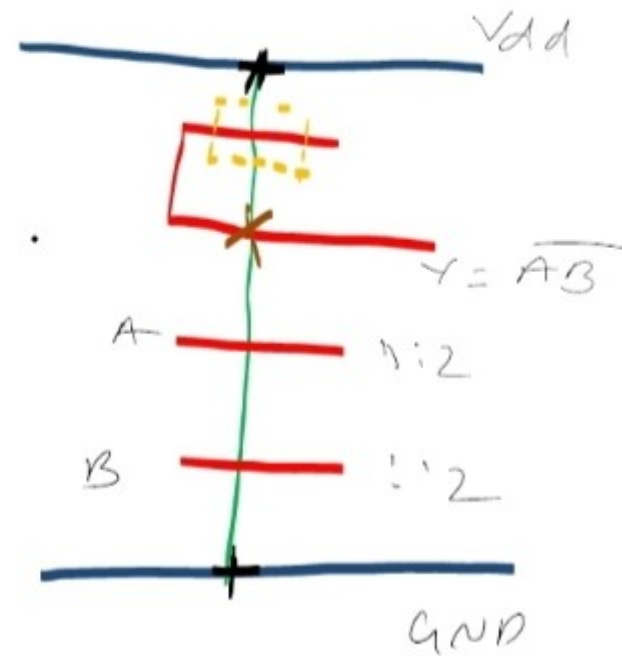
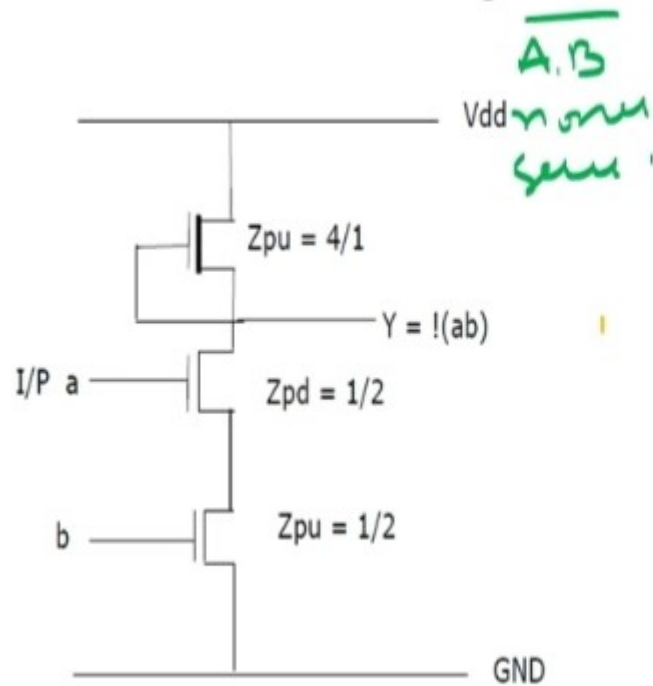
nMOS Depletion load NOR



$Y = \overline{A+B}$ - nmos parallel
depletion mode



nMOS Depletion load NAND



Buses, Control Signals, Interconnections and leaf Boundaries

