





DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

EMBEDDED SYSTEM DESIGN

(Theory Notes)

Autonomous Course

Prepared by

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Module – 4 Contents

Interfacing, Peripherals and Communication Protocols: Interfacing General Purpose Microprocessors, Timers, Watchdog Timers, Counting Devices, PWM, LCD, UART, Keypad Controller, Stepper Motor Controller, ADC, Serial Protocols: I2C, CAN, USB, Parallel Protocols: PCI bus, ARM bus Wireless Protocols: IEEE 802.11

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Embeddstandardusingle-purpose Peripherals

❖ TIMERS :-

A timer is an peripheral device that can measure time intervals.

i) Generat events at specific time or to determine the duration between two external events.

eg: Keeping a traffic light green for a specified duration or communicating bits serially between devices at a specific rate.

ii) To determi<mark>ne duration of two external events.</mark>

eg: Computing a cars speed by measuring the time the car takes to pass over two separated sensors in a road.

A timer measures time by counting pulses that occur on an input clock signal having a known period.

COUNTERS:-

A counter counts pulses onsome other input signal.

eg: A counter may be used to count the number of cars that pass over a road sensor of thr number of people that pass through a turnstile.

TIMERS & COUNTERS are combined to measure rates.

eg: Counting the number of times the car wheel rotates in one second, in order to determine a cars speed.

★ Timer Structure :- Embedded System Design

The timer structures are

- 1) Basic Timer
- 2) A Timer/Counter
- 3) A Timer with a terminal count
- 4) A 16/32-bit Timer
- 5) A Timer with a prescaler

1) Basic Timer :-

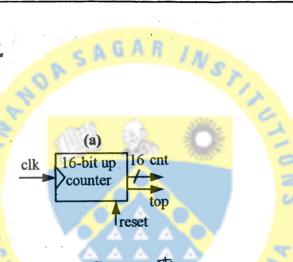


Fig O: A Basic timer

- * The timer has an internal 16 bit up counter which increments its value on each clockpulse
- The oulput value ont represent the number of pulses sinces & the counter was last reset to year.
- * It has additional output top that indicates when the top value of its stange has been steached.

It is also known as overflow occurring in which case the timer galls over to zero

DEpt. MEECE, DISCE a Timer range as the maximum time

interval the timer can measure Embedded System Design

* Also, a time resolution is the minimum interval it can measure

1) If the circo datas one

1) If the given datas we f=100MHz. Cnt = 20,000. Find resalution and range.

Soln:
** Resolution = 1 = 100mH3 = 100 nsec

* Range = Cnt x Resolution = 20,000 × 10 nsec = 200 psec

2) If the given data are 1 = 100MHz, counter = 16-bit find resatution and range.

<u>doln</u>: 16-bit counter will count from 0 to 65,535 .: cnt = 65,535

* Resolution = $\frac{1}{f} = \frac{1}{100 \text{ MHz}} = 10 \text{ nsee}$ * Range = cnt × Resolution = 65,535 × 10 nsec = 655.35 µsec

2) A Timer/Counte :-

* The mode register holds a bit by which the wer Dept. GPECE, DSCE that uses a &x1 Multiplexer to select the clock input to the internal 16-bit Counter

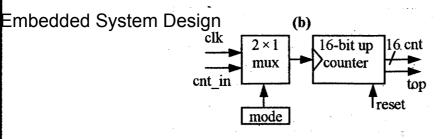


Fig O: A timer/counter

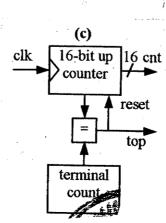
* The clock input can be the external clock signal, in which case the device acts like a timer.

* The clock input can be the enternal clock signal, in which case the the device acts like a limen

* The clock input can be the external <u>cnt-in</u> signal in which case the dewice acts like a counter, counting the occurrence of pulses on cnt-in.

* Crt-in would typically be connected to an external Sensor, so pulses would occur at indeterminate intervals.

3) A Timer with a terminal count :-



Dept. of ECE, DSCE Fig (1): A timer with a terminal count

Explosionabesignant negrister holds a value, which the user sets, indicating the number of clock cycles, in the desired interval & is determined by using simple formulae:

Number of cycles = Desired time interval clock period.

For ex, to obtain a deviation of 3 microseconds from a clock cycle of 10 nsec (f = 100 MHz), then

No q clock cycles = $\frac{3\times10^6}{10\times10^6}$ = 300 cycles.

* The timer structure includes the comparator that asserts the top output (ie top=1) when the terminal count has been reached.

The top output is used to:

- i) Reset the counter to zoro and.
- ii) To inform the user that the desired time interval has passed.
- * To top signal is often connected to an interrupt (Pin). The corresponding ISR would include the actions that must be taken at the specified time interval.
- * To improve efficiency, a down counter is used rather than an upcounter.

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4) A 16/32-bit Timer :-

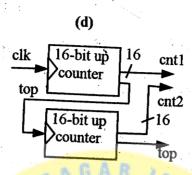


Fig 1 : A 16/32 bit liner

*X Fig-D. Shows the structure of a timer that can be configured as a 16 or 32 bit timer.

The Timer Simply uses the top autput of its first 16 bit up counter as the clock input of its second 16 bit counter.

These are known as cascaded counters.

5) A Timer with a prescaler :-

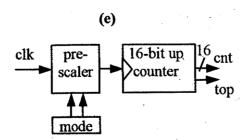


Fig O: A limer with a prescalar

* A prescalor is essentially a configurable cock divider concert. Depending on the mode bits being input to the prescalor.

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Embedded System Design olp signal might be
i> Same as the input dignal frequency
ii> 1/2 of the frequency
iv) 1/8 of the frequency

Mode	e bits	Op frequency
0	0	Same as I/p Signal
0	1	1/2 of Ilp dignal
1	0	Yte of Ty signal
١	ì	1/8 of I/p dignal.

Eg: consider a timer with a resolution of 10 msee and a range of 65,535. If the prescalar is configured to divide the clock frequency by 8, then calculated timer resolution.

Sol !~

- * Resolution = 10 nsecx 8 = 80 nsee
- * Range = ent x Resolution : 65,335 x 80 nsec

Range = 5-24 µsec

REACTION Timersign

Reaction timer is an application that measures the time a person takes to respond to a visual or audio stimulus.

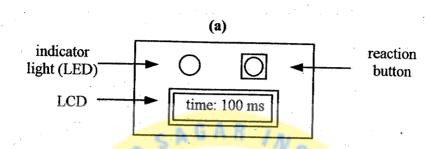


Fig O: Reaction timer: LED, LCD and button

- * The application twens on a LED, then measures the time a person takes to push a button in response, and display this time on an LGD.
- leaction time is expected to be in the order of seconds and displays reaction time to be miliseco-nd precision.
- * In this example, we will use a microcontroller with a built in 16-bit limer. The timer is incremented once every instruction cycle for this microcontroller is 6 clock cycles.
- * The Timer does not have a prescaler on Terminal count register.
- * It has a top signal to indicate overflow also celleus us to load an initial value for its Dept. of ECEIDSCE, counter.

* If the clock prequency is 12 MHz, then Embedded System Design period = 1 = 1 = 83.33 nsec * Each instruction has 6 clock cycles Resalution = 1 instruction eycle x + Resolution = 6 x 83.33 nsec Resolution = 0.5 µsec * The timer is of 16-bit, so manimum value is 216 = 65,536 5 A GAI .. Range = Resolution x Maximum [0-65536 = 65,536] = 0.5 msec x 65,536 Range = 32.77 m sec * We note that this timer's range is smaller than own desirred range of several seconds, while its resolution is finer than our required Imsec. * The initial timer value can be set that the overflow occurs every I msec. Then we can monitar the top output signed of the timer to activate the code. The code keeps a count of oneylows, indicating the number of miliseconds. * The initial value to be loaded is determined ie initial value = Maximum value - Required x Oscillator freq of counter / time No of cycles per inst = 65,536 - [Imsec x 12 MHz] Dept. of ECE, DSCE = 65,536 - 2000

```
Embedded System Design value = 63,536
* The Pseudocode describing the reaction timer implement
 - ation is written below.
   /* main. c*/
  # define MS_INIT 63535
   void main (void)
     int count_miliseconds = 0;
     configure timer mode
      set ont to MS_INIT
      Wait a nandom amount of Time
      twon on indicator light
      Start limer
      While (user has not pushed reaction button)
      { if (top)
         { Stop timer
            set cont to MS_INIT
            Start liner
            reset top
            count - milliseconds ++;
        two of indicator light
        parintf ("Time: 1/1 ms?; count, miliseconds);
```

FORMULAE

- Embedded System Design
- 1) Resolution = 1 instruction cycle x 1
- 2) Range = Resolution x Maximum value (count)
 - NOTE :-

Resolution = $\frac{1}{f}$

- 3) Maximum division needed = Porescalar measurement in a porescalar Man value of the counter
- 4) Terminal court = Desired Time Interval clock period (T= 1)
- 1) A 16-bit timer operates at a clock frequency of 12MHz. Determine the resolution and range of this timer.

Timer = 16-bit

Marinum value = 216 1 = 65,535

$$sol:-$$
 * Resolution = $\frac{1}{f} = \frac{1}{12MH_2}$

Resolution = 83.33 nsec

Range = 5.5 msec

2) Determine the range and resolution of a 16-bit timer which operates Embedded System Design at a clock frequency of 10Mhz and generate an overflow signal when it reaches FFFF. Calculate the terminal count value for measuring a 3 msec time interval. What is the minimum division needed in a prescaler for measuring 100 msec?.

June-09,6M

f = 10MH3

16- bit Timer

.'. Manimum value = $\vartheta_{-1}^{16} = 65,535$

Time intowal = 3 msec prescalar measuremen

prescalar measurement = 100 msee

Range = Resolution x Man value

Dept. of ECE, DSCEnimimum = 1.52 × 10 6

- 3) Given & 16-bit timer with 20 Mhz,
 - i) Determine its range and resolution
 - ii) Calculate the terminal count value needed to measure 1.5 msec interval
 - iii) If a prescalar is added, what is the minimum division needed to measure an interval of 50 msec. Determine its range and resolution, if the division value is a power of 2.

Jan-08,6M

Given:
$$f = 20MH_3$$
, $T = \frac{1}{f} = 50$ nsec

Timer is 16 bit ... Manimum value = 216 1= 65,536

Range = Resolution × Munimum = 50nsec × 65,535

D Desired time interval = 15 msec

Terminal court = Desired time interval period
$$(T = \frac{1}{f})$$

Terminal court = 30,000

© Prescaler measurement interval = 50msec

prescaler minimum = Prescaler measurement

Dept. of ECE, DSQFriision Manimum value

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Embedded System Design

porescal minimum = 0.762 usec division

* Resolution = 1 = 50 nsec

Range = 2 × Resalution

Range = 214, 748 sec

Nate!

* The maximum value of timer = 216

* Determine its stange & resolution if the division value is a power of 2.

ie Marimum value of time = 2 x16 = 32

WATCHDOG TIMER:-

What is watchdog timer? Explain ATM timeout using a watchdog timer.

Jan-11,10M

With a neat diagram, explain functioning of a watch dog timer. Discuss the usage of watch dog timers. Write a Pseudo code for an ATM machine to demonstrate the usage of watch dog timer.

Jan-10,10M

A Special type of timer is a watchdog timer, which will reset the Besteon Eder DS6 Fedefined timeout. 14

Embedded System Design reset timer every X time unit, else timer generates a signal indicating that the system failed.

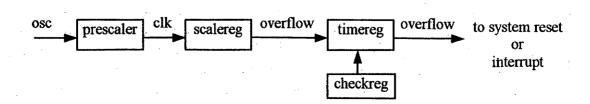
Common use of watchdog timer is to enable an embedded system to restart itself in case of a failure.

Another common use is to support timeouts in a program while keeping the program structure simple.

Example of ATM timeout using a watchdog timer:

* In this example, a watchdog timer is used to implement of a time out for an automatic teller machine (ATM).

- * A normal ATM session involves a user inserting a bank card, typing in a Rensonal identification number (PIN), and then answering questions about whether to deposit or withdraw money, which account will be involved, how much money will be involved, whether another transaction is desired, and so on.
- He want to design the ATM such that it will terminate the session if at any time the user does not press any button for a minutes. In this case the ATM will eject the bank courd and terminate the session.



Dept. of EGE, DEQEtime out using a watchdog time Itucture,

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* An oscillator signal OSC is connected to prescaler that Embedded System Design divides the Oscillator frequency by 12 (OSC/12) to generate a signal clk

* The signal clock is connected to an 11-bit up counter Scalereg. When scalereg overflows, it rolls over to 'o', and its overflow output causes the 16 bit up-counter time steg to increment.

* If timeneg overflows, it triggers the System neset or an interrupt. To neset the watchdog Timen, checkney must be enabled. Then a value can be located into timeney.

* When a value is loaded into time reg, the checkness register is customatically reset. If the checkness register is not enabled, a value cannot be loaded into timereg. This is to prevent our one were software from unintentionally resetting the watchdess timer.

* Let us determine what value to load in timereg to achieve a timeout of 2 minutes

The osc signal frequency is 12MHz. The timereg is incremented at every 't' seconds, where

$$t = Presealar \times Scalereg \times \frac{1}{osc freq}$$

= $12 \times 2'' \times \frac{1}{12 \times 10^{c}}$

t = 0.002 sec

Dept. of ECE, DSCE timer resolution = 2 msce

a 16-bit register, its range is o to * Vince Timerey is Embedded System Design ... Time range = Max count x Resolution = 65,535 x 2mscc Timer sange = 131.070 msec (Approximately 2-18 minutes) * To obtain timereq value: Timeseg value = 131,070 - X X = 131,070 - Timereg value (MKT temereg value = 2 minutes = 120000 msec) X = 131070 - 120000 X = 11070* The pseudocode for the main routine and the watchdog siese to soutine to implement the timeout functionality of the ATM is shown below: Main pseudo-code: /* main. c*/ main () { wait until could inscribed call watchdog-neset - noutire While (toransaction in progress)

if (button pressed)

Experience corresponding action

Dept. of ECE, DSCE watchdog - reset - routine

Embedded Bystem Design reset - routine not called every < @ minutes, interrupt - sorvice - sautine is called */ Watchdog timer neset noutine: Watchdog - reset _ rautine () { /* Checkney is set so we can load value into timerey. Zero is loaded into scalereg and 11070 is loaded into Timoreg */ cheekreg = 1 Scalereg = 1 timueg = 11070 vaid interrept_service_ routine () eject could neset screen

Explain how UART is used for communication highlighting the advantages of UART.

June-07.6M

UART takes parallel data and transmits serially & UART receives serial data and converts to parallel.

A simple UART may possess

- i) Some configuration registers &
- ii) Two independently operating processors, one for receiving and the other for transmitting.

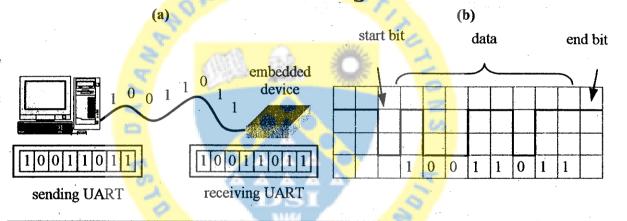


Figure 1: Serial transmission using UARTs, (a) A PC communicating serially with an embedded device, (b) transmission protocol used by the two UARTs.

- * The transmitter may posses a register called a transmit buffer, that holds data to be sent. This register is a shift register, so the data can be transmitted one bit at a time by shifting at the appropriate rate.
- * The receiver receives data into a shift register, and then the data can be read in parallel the receiver in constantly monitoring the receive pin (912) for a start bit. The start bit is typically dignaled by a hight to low transition on the Mx pin

Dept. of ECE, DSCF and bit has been detected, the necesium starts

Shifting each sampled bit into the neceive shift negister to determine whether the transmitted data is correct, the transmitted parity bit.

The VART can be configured to check for even posity or no pariety at all once data is received, the VART signals its host processor. The host processor in two reads the byte out of the receive shift register. The receiver is now ready to receive more data.

Toransmetter Operation:

The host processor (Txing side processor) writes a byte to the transmit buffer of the VART, the transmitter sends a start bit own its transmit pin (tx), signaling the beginning of a transmission to the gremate VART. Then, the transmitter shifts out the data in its transmit buffer over its tre pin at a predeter mined rate.

(Txer can also Tx its an additional pairity bit)

At this point, the UART processor signals its host processor, indicating that it is ready to send more data if available.

* The transmission protocol used by VART's determines the rate at which bits are sent and received 8 is called band rate. The protocol also specifies the number of bits of data and the type of parity sent during each transmission.

Dept. ThECE, Decerate determines the speed at which data is 20 exchanged between two socially connected UART'S. The

Embédirer system Design bound rates oure 2400, 4200, 9600 & 19200.

It to use a UART, we must configure its band rate by writing to the configuration negister, and then we must write data to the transmit register and for read data from the necessued register.

* To use a VART, we must configure its bound rate by writing to the configuration negister, and then we must write data to the transmit negister and for nead data from the neceived negister.

For ex, to configure the VART of an 8051 microcontroller we must use the following equation:

smod corresponds to 2-bits in a special-function register, osc freq is the frequency of the oscillator, & TH1 is an 8-bit rate register of a build-in timer.

Determine the values for smod and TH1 to generate a baud t=rate of 9600 for the 8051 baud rate equation, assuming an 11.981MHz oscillator. Remember that smod is a 2 bit and TH1 is 8-bits. There is more than one correct answer.

Where.

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Baudrate =
$$\left(\frac{\partial^{\text{Smod}}}{\partial \lambda}\right) * \frac{\partial \mathcal{E} \text{ freq}}{[12 \times (256 - \text{TH1})]}$$

for $\text{smod} = 2 = 10$:

$$9600 \leftarrow \left(\frac{2^2}{32}\right) * \frac{11.981 \times 10^6}{\left[12 \times (956 - T + 1)\right]}$$

$$76,800 = \frac{11.981 \times 10^{\circ}}{12 \times (956 - TH1)}$$

$$3072 - 12TH1 = 11.981 \times 10^{6}$$

for smod = 3 = 11:

Band rate =
$$\left(\frac{2^{8}\text{mod}}{32}\right) \times \frac{08C \text{ freq}}{\left[12 \times (256-7\text{H1})\right]}$$

 $9600 = \frac{2^{3}}{32} \times \frac{11.981 \times 10^{6}}{\left[12 \times (256-7\text{H1})\right]}$
 $\frac{9600 \times 32}{8} = \frac{11.981 \times 10^{6}}{\left[12 \times (256-7\text{H1})\right]}$

$$38,400 = 11.981 \times 10^{C}$$
DSCF (12 x 256 = 12 TH1)

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Embedded System Design – 12TH1 =
$$\frac{11.981 \times 10^6}{38400}$$

 $3072 - 12TH1 = 312.0052$
 $12TH1 = 3072 - 312.0052$
 $12TH1 = 2759.994$
 $141 = 229.99$
 $141 = 230 = 11100110$

PULSE WIDTH MODULATION (PWM) :-

❖ Describe the working of PWM unit with timing diagrams. How can it be used for speed control of DC motor.

June-11,10M

* With a neat diagram, explain how the pulse width modulator works. What are the considerations in selecting the clock, the prescalar and the counter? Assuming an 8-bit up counter, calculate the count to be loaded in the 'cycle-high' register to get pulses of duty cycle 75%.

Jan-11,10M June-06,10M

* Describe the working of a PWM unit with a circuit and waveform.

June-09,6M

Describe the working of a PWM unit with timing diagrams. How it can be used for speed control of DC motor.

Jan-08,8M

Schematically explain how a PWM helps in controlling the speed of DC motor.

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June-07,6M

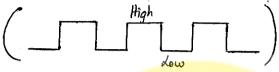
mbedded System Design

* How PWM can be used for speed control of DC motor? Explain.

Jan-07,8M

Pulse width Modelatar (PWM):-

* I pulse width modulator (PWM) generates an elp signal that prepeatedly switches between high and low values



* We control the dividion of the high value and of the low value by indicating the desired period (T) & the desired duty cycle (D).

* Duty cycle is defined as the reation of on time to the total period (on + off) & is expressed in percentage.

$$\left\{ \int \int D = \frac{T_{\text{oN}}}{T_{\text{oN}} + T_{\text{off}}} \times 100 \right\}$$

* There are 3 common use of PWM:

- 1) To generate a clock-like signal to another device ex:-PWM can be used to blink a light at a specific rate.
- 2) To control the average current or voltage input to a device.

Ex: A DC electric motor rotates when its input voltage is set high, with the rotation speed proportional to the input voltage level.

Dept. The Devolutions per minerte (rpm) equals 10 Times 24

Embedded System Design to set the input voltage to 1.25V, where as achieving 250 rpm would require an input vallage of 2.50V

3) To encode control commands in a single signal for use by another device.

en: Me muy contral a radio-controlled can by sending puelses of different widths.

A width of 1-mes corresponds to a twin left command, a 4-msec width to twin sight, and an 8-msec width to forward.

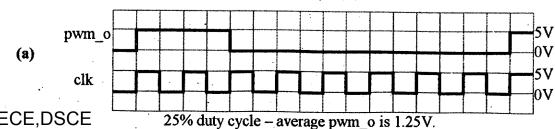
* The PWM approach makes use of the fact that a DC motor does not come to an immediate stop when its input voltage is lawered to 'o', but nather its it coasts.

Thus the average input voltage is set to obtain the desired speed.

using a pwm, duty cycle is set to achieve the appriopriate average voltage.

* Assuming the PWM's out is 5V when high and ov when low, then.

* We can obtain an average of 0 1.25V by setting the duty cycle to 25.1. ie $5V \times 25$ 1. = 1.25V. This duty cycle in shown in fig 1@. $5V \times 0.25 = 1.25V$.

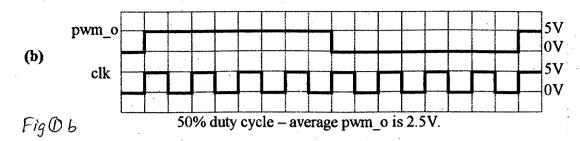


Dept. of ECE, DSCE 25% duty of Fig (1) a.

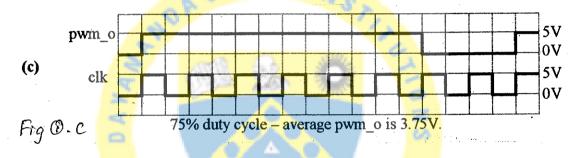
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Ensbedded System Debign can average of of 2.500 by selling the duty cycle to 50% as shown in fig() b.

0.5 x 5 V = 2.5 V



* A duty cycle of 75% would result in accorage of of 3.75 V as shown in fig 10. 0.75 x v = 3.75 v



Controlling a DC Motor Using a PWM

* The speed of the DC Motor is proportional to the voltage applied to the motor. We must set the duty cycle of a PWM such that the average of voltage equals the desired voltage.

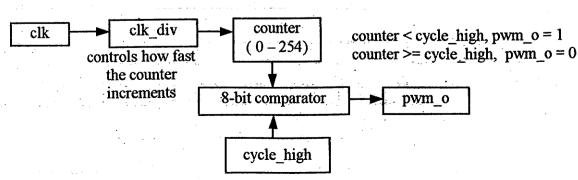


Fig 1@: Internal Structure & PWM
Dept. of ECE, DSCE 1 (1) Internal Structure of PWM

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Empedified System Designo 8 bit registers called <u>clk-div</u> and <u>cycle-high</u>, an <u>8 bit counter</u> and an 8-bit comparator as shown in fig 1. a.

* Initially, the value of CIK-div is loaded into the register. The CIK-div negister works as a clock divider. After a specifical amount of time has elapsed, a pulse is sent to the counter negister. This cause the counter negister to increment itself. The comparator then looks at the values in the counter negister & the cycle-high negister.

* When the counter value < cycle_high, a 1 (+5 v) is outputted.

When the counter value > cycle_high, a 0 (ov) is outputted.

* When the counter value reaches 254, counter is neset to o and the process repeats. Thus clk-div determines the PMM's period, specifying the number of cycles in the period.

The negister cycle-high determines the duty cycle, inclicating how many of periods cycle output a 1.

If the cycle-high is set to 255 (FFh), the op signal is always high nescelling in a duty cycle of 100%.

The cycle-high is set to o(ooh), the op signal is always law resulting in a duty cycle of oil

If the value loaded to the clt_div is too low, the value autputted by the comparator oscillates too quickly. The comparator never outputs zeros long enough for the DC motor to slow down, causing the DC motor to continuesly run at full speed.

Depter porte value of clk_div to ffh, in this case it 27 works best

Enaberhad SystemDosignip between applied voltage & Dc motor speed:

input voltage	% of maximum voltage applied	RPM of DC motor		
0	0	0		
2.5	50	4,600		
3.75	75	6,900		
5.0	100	9,200		

 \star Far the motor to seen at 4,600 RPM, 50% duly cycle is needed. The required duty cycle is computed as $854\times0.5=127=7Fh$.

Thus loading IFh into the cycle-high register.

* 11th to sun motor at 6,900 RPM, 75% duly cycle is needed. The required duly cycle is computed as 254 × 0.75 = 191 = BFh

Thus loading Bfh into the cycle_high register

* The PWM does not provide enough current to seen the DC motor. Thus an (NPN) transistan is used to drive the DC motor as shown below.

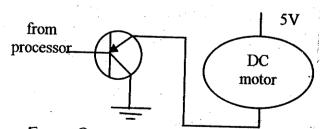


Fig 20: Connection to DC motor

The pseudo code is: void main (void) {

```
/* controls period */
PWMP = 0xff;
/* controls duty cycle */
PWM1 = 0x7f;
while(1){};
```

Dept. of ECE, DSCE

Exploeded System Designihe Clk-div register in PWMP and cycle-high is PWM1.

STEPPER MOTOR CONTROLLER:-

Explain how a stepper motor is controlled using driver. Gice relevant hardware and software details.

Jan-07,8M

- * A stepper motor is an clectric motor that notates fixed number of degrees whenever we apply a 'step' signal.
- * Stepper motor can notate 1.8° (Full step) or 0.9° (half step)
 per step. If the motor notates 1.8° per step, then to move
 360°, the number of steps nequired is 200° ie (1.8 × 200
 steps = 360°)
- * Internally, a stepper motor typically has faur coils. To notate the motor one step, we pass coverent through one or two of the coils. Thus notating the motor 860° nequires current to the coils in a specified Sequence. Applying the sequence is neverse causes neversed notation.
- Stepper motor can be contralled in 2 ways:
- 1) Using a stepper motor obviver
- 2) Contralling a Stepper motor directly

mbedded System Design Stepper motor:

- 1) Dist obinors
- 2) Prienters
- 3) Photocopy
- 4) Fan machines
- 5) Robats
- 6) Camcarders
- 7) VCR's.

Steppen Motor Control using Driver:

* Controlling a stepper motor requires applying a series of voltages to the four cails of the stepper motor. The cails are energised one or two at a time causing the mator to rotate one step.

* In this example, we are using a 9-volts, 2-phase bipal - an stepper motor. The table indicating the input sequence required to notate the motor. The entire Sequence must be applied to get the motor to notate 7.5 degrees.

To rotate the motor in the opposite direction, we simply apply the sequence in neuvous order.

	sequence	Α	В	A'	B'
	1	+	. +	-	-
	2	-	+	+	-
	. 3	-	_	+	+
	CCE 4	+		-	+
pept. of ECE,D	OCE 5	+	+		

embedded System Designan 8051 pc and Mc34797 chip to control the stepper motor. We need only worry about setling the clirection on the clockwise / counter clock wise pin (cw/ccw) and pulsing the clock pin (clk JL) on the stepper motor driver chip using the 8051 microcontroller.

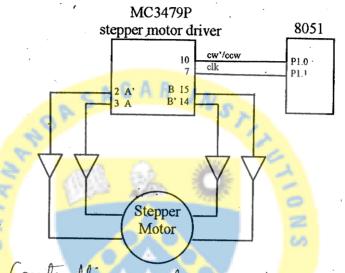


Fig 1 @: Controlling a stepper motor using a driver /* main . c */ Sbit Clk=P121; Shit CW=P10; void delay (void) int i, j; for (i=0; i<1000; i++) for (j=0; j250; j++) i= i+0; void main (void)

Dept. of ECE, DSCE | * Set direction*/

EmbeddetkSystem Designulse clock */

clay();

clk=1;

/** turn the motor backwards */

cw=1; /* set direction */

clk=0; /* pulse clock */

cleay=();

clk=1;

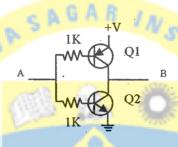


Fig Db. Buffor

* The old pins on the stepper motor deriver do not provide enough current to drive the stepper motor To amplify the uvvient, a buffer is needed and is show in fig 10.

* P, is an PNP transister & Q, is an NPN transister. A is connected to the 8051 microcontroller and 18° is connected to the stepper motor.

CONTROLLING STEPPER MOTOR DIRECTLY:-

(Without Using DRIVER)

In this example, the <u>stepper motor driver</u> is eliminated. The stepper motor is connected directly to the 2051 MC DEPT. OF ECE, DISCETIG 1 @.

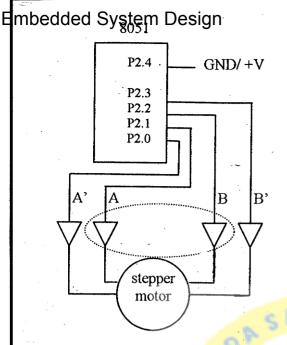


Fig Da: Contralling a stepper motor directly

* The direction of the stepper motor is controlled manually.

If P2.4 is grounded, the motor notales counter clockwise, otherwise the motor notales clockwise

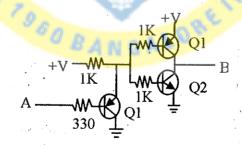


Fig O b Buffer.

* The 8051 ports are unable to directly supply the current needed to drive the motor. To amplify the current, a buffer is needed and is shown is fig 10.

* 9, one PNP bransiston and 92 is an NPN transistory; Dept. of ECE, Decembered to the 8051 microcontroller and B is

```
Embeltitled System Designthe Stepper motor.
 The sample code to sun the stepper motor is shown below
  Sbit notA = P2 10;
  3bit is A = P2 11:
  Sbit not B = P212;
  Sbit is B = P213;
  sbit des = P214;
   void delay ()
     int a, 6;
     for (a = 0; a < 5000; a++)
     for (b=0; b<1000; b++);
   void move (int dist, int steps)
     int Y, Z;
     if ( doi = =1)
       for (Y=0; YX= Steps; (Y++)
      { for (z=0; Z=19; Z+=4)
         is A = lookup[z];
            16 B = lookup [Z+1];
            not A = lookup [z+2];
            not B = lookup[z+3];
            deley ();
    if (disi ==0)
pept. of ECE, PSCEO; YZ=Step; Y++)
```

```
Embedded System Design Z > = 0; Z - = 4)
           is A = lookup [Z];
           isB = lookup [z-i];
           notA= lookup[Z-2];
           not B = lookup [z-3];
           delay ();
   int looup[20] = {1,1,0,0,0,1,1,0,0,0,
                     1,1,1,0,0,1,1,1,0,0};
   void main )
    while (1)
    { 1x move forward 15 degrees x/
      move (1,2);
     /* move backword 7.5 degrees */
     move (0, 1);
                                         _[z]
                                            \frac{1}{[z+1]}[z+2]
Note: int lookup[20] = { 1,1,0,0
```

Dept. of ECE,DSCE

1,1,0,0}

LIQUID CRYSTAL DISPLAY (LCD) :-

* A LCD is a law-cost, low-power device capable of clisplaying text and images. LCD's core extremely common in embedded systems, Since such system often do not have video monitors like those that come standard with desktop systems.

LCD's can be found in numerous common device like watches, for, capy machines and calculators.

{ Basic principle:

The basic principle of one type of LCD, a reflective LCD, works as follows. Firest, incoming light passes through a polarizing plate. Next, that palarized light encounters liquid crystal material

If we entite a region of this material, we cause the material malecules to align, which in two causes the polarized light to pass through the material otherwise, the light does not pass through.

Finally, light that passed through hite a mirror and reflects back, so the excited region appears to light up. Inother type of LCD, an absorption LCD works similarly, but uses a black surface instead of a mirror. The surface below the excited region absorbs light, thus appearing darker than the other regions.

A dot-matrix LCD consists of a matrix of data that can display alphanumeric characters (letters and digits) as well as other dymbols. I common dot-matrix LCD ceptrof EGE, PSCE laumns and eight slows of data for one character

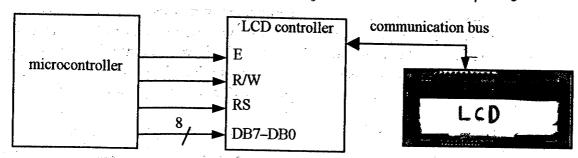
Embodded Systembiosingn converts input data into the appropriate electrical signals necessary to excite the appropriate LCD dots.

* Each type of LCD may be able to display multiple characters. Each characters may be displayed in normal or inverted fashion.

the LCD may permit a Character to be blinking on may permit display of a cursor indicating the 'current' character (blinking underscore). Then functionality would be difficult for us to implement using software thus, we use an LCD controller to provide up us with a simple interface to an LCD having 8-data inputs (DBO-DB7) and one enable input.

* To send a byte to the LCD, we provide a value to the cight inputs and pulse the enable. This byte may be a control word, which instructs the LCD controller to initialize the LCD, clear the display, select the positions of the cursor, brighten the display.

* Alternately, this byte may be a <u>data word</u>, such as an ASCII characters, instructing the LCD to display the character at the currently-selected display position.



```
Embedded System Design
                                                                void WriteChar(char c) {
                                                                    /* indicate data being sent */
         I/D = 1 cursor moves left
                                         DL = 1 8-bit
                                                                   RS = 1;
         I/D = 0 cursor moves right
                                         DL = 0 4-bit
                                                                   /* send data to LCD */
         S = 1 with display shift
                                         N = 1 2 \text{ rows}
                                                                   DATA BUS = c;
         S/C = 1 display shift
                                         N = 0 1 row
                                                                    /* toggle LCD with delay */
         S/C = 0 cursor movement
                                         F = 1.5 \times 10 \text{ dots}
                                                                  EnableLCD(45);
         R/L = 1 shift to right
                                         F = 0.5 \times 7 \text{ dots}
         R/L = 0 shift to left
```

- * In this example, a microprocessor is connected to an LCD controller, which in twen is connected to an LCD as shown in fig. 1 . The LCD controller receives control words from the microcontroller, it decodes the control words and performs the coversponding action on the LCD
- * once the initialization sequence is done, we can send control words or send actual data to be displayed.
- * When RS is set to low to indicate that the data sent is control word.
- * When RS is high; this indicates that the data sent over the communications bus coveresponds to a character that is to be displayed.
- * Everytime data is sent, whether it is a control word or data, the enable bit E must be toggled (ie I)
- By using initialization code, the LCD has been set with an 8-bit interface. In addition, the display has been cleared, the courser is in the home position, and the curser moves to the sight as data is displayed. The LCD is now bready to be written to.
- of In order to write data, we set RS=1. The actual Deptoblished By DBO-DB7. The write chose functions accepts a character which will be sent to the

Empedded System Designto display on the LCD.

The Enabled LCD function togglis the enables bit and cuts as a delay so that the command can be processed and executed.

KEYPAD CONTROLLERS:-

* A keypad consist of a set of buttons that may be pressed to provide conput to an embedded system. Again, keypads are entremely common in embedded dystern, dince duch systems may lock the keyboard that comes standard with desktop systems.

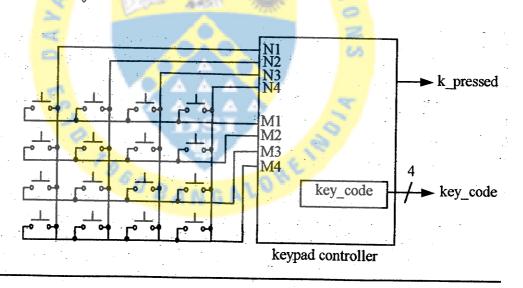


Figure (i) Internal keypad structure, with N = 4 and M = 4.

Fig (1) Shows a simple keypad having buttons avanged in an NI-coloumn by M-sow gold.

The device has N autputs, each output corresponding to a colourn, and another (N) autputs, each output corresponds to a row.

Ulhen we press a button, one coloumn autput and one dept of ECE DSCE go high, uniquely identifying the pressed 39

Embladded System Dasignal Such a keypad from software, we must sean the colourn & now outputs. The scanning may be performed by a keypad controller. Such a device decodes nother than controls, but we will call it a "controller".

* Fig D shows the controller, which scans the coloumn and now outputs of the keypad. When the controller detects a button posess, it stores a code corresponding to that button into a register, key-code, and sets an output high, k-pressed, indicating that a button has been pressed.

the software may pall this of every 100 milliseconds on so and read the register when the of is high alternative by, this autput can generate an interrupt on awar general - purpose processor, climinating the need for palling.

Analog to digital converter (ADC) :-

June-07,8M

- Highlight the advantages of using data in digital form over its analog form. Explain the working of successive approximation types of analog to digital converter.
- * In analog-to-digital converter (ADC, AID on AZD) converts on analog signal to a digital signal and a digital-to-analog converter (DAC, D/A on DZA) does the opposite.
- * <u>Analog</u> refers to a continuously valued signal, such as limpurature or speed.
- * <u>Digital</u> refers to discretely valued signals, such as integers. and these signals we encoded in binary.

 Dept. of ECE, DSCE

For enample consider an analog input signal whose

Embedded Systemblesignange from o to 7.5 volts. We want to represent each possible voltage winthis range using a 4 bit binary numbers. The <u>oooo</u> would be the most obivious encoding for <u>ov</u> and IIII for 7.5 v. The <u>encodings</u> between <u>oooo</u> and <u>IIII</u> would den be evenly distributed to the range between o and 7.5 v. as shown in fig 1 a.

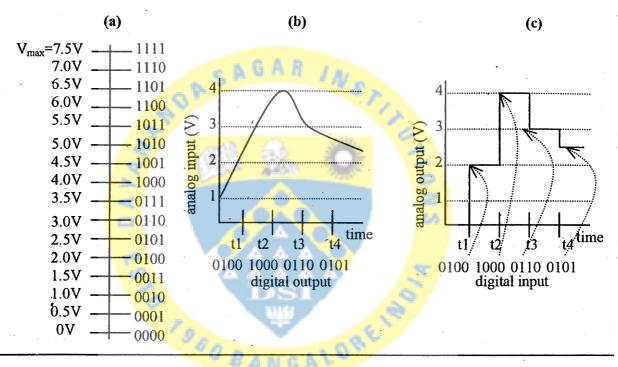


Figure 1: Conversion: (a) proportionality, (b) analog-to-digital, (c) digital-to-analog.

Fig 1 B ranging from IV upto 4V and then down to just over 2V. The digital encoding of this signal, sampled at times t1, t2, t3 and t4, into four bits.

* Whe can compute the digital values from the analog values, and vice-versa using the following ratio:

Dept. of ECE DSCE is the manimum voltage that the analog signal contact Assume

Embedded System Designber of bits available for the digital encoding

d is the present digital encoding and e is the present analog voltage.

for excemple: duppose Vman is 7.5V, desume analog Voltage e=3V, WKT it is a 4-bit converter : n=4

Then
$$\frac{3V}{7.5V} = \frac{d}{24-1}$$

$$\frac{3\times15}{7.5\text{V}}=d$$

* The resolution of ADC an DAC is <u>Uman</u>. This suppresents the number of voltes between " successive digital encoding"

Resolution =
$$\frac{V_{man}}{(a^n 1)} = \frac{7.5V}{a^4 1} = 0.5V$$
.

:- Resolution is 0.5V between Luccessive encoding

1) Given an analog input signal whose voltage ranges from 0 to 15v and an 8-bit digital encoding is used. Calculate the correct encoding for 5v and then trace the successive approximation approach to find the correct encoding.

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June-07,10M

Engledded System Design encoding should be

$$\frac{e}{Vman} = \frac{d}{\partial^n I}$$

When Vman = Vman - Vmin

$$\frac{5}{15} = \frac{d}{2^8}$$

$$\frac{5}{15} \times (2^{8}-1) = d$$

$$\frac{5}{15} \times (2^{8}-1) = d$$

$$[d = 85] \leftarrow coverest encoding.$$

Resolution =
$$\frac{Vman}{3^{n}-1} = \frac{15V}{2^{8}-1} = \frac{15}{255}$$

Resolution = 0.058823V

* Applying the successive approximation method we Start by finding the halfway point between the marimum and minimum voltages.

Where Uman = 15V & Vmin = OV

$$e' = \frac{\text{Vman} + \text{Vmin}}{2} = \frac{15 \text{V} + 0 \text{V}}{2} = 7.5 \text{V}$$

* Since the above voltage is higher than the input voltage (5V). Me insert a zero into the highest bit shown below.

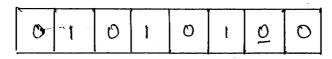
Dept. of ECE, DSOFman + Vmin = 7.5 V + 0 V = 3.75 V

Embedded System Design
Since ele 1e 8.75V < 5V .. We insert a one into the next MSB as shown below 000 * Now Vman = 7.5 V & Vmin = 3.75 V :. e = Vmant Vmin = 7.5V+3.5V = 5.63V Since else le 5-63V>SV .. We insert a zero into the next MSB as shown below. 0000 * Now Umax = 5-63V & Vmin = 3.75V $e^{1} = \frac{\text{Umanfl/min}}{2} = \frac{5.63 \text{V} + 3.75 \text{V}}{2} = \frac{4.69 \text{ V}}{2}$ Since e'ke, we insert a one into neut MSB as shown. 0 * Now Uman = 5-634 & Vmin = 4.69V -. e = \frac{1}{2} = \frac{5-63+4.69}{2} = 5.16 V since ele, we insert a zero into nent MSB as Shown below. * Now Ymax = 5-16 V & Ymin = 4.93 V

Dept. of ECE, DS CE an + Vmin = 5.16 V + 4.93 V = 5.05 V

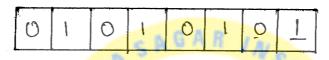
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Embédoiset Systém Designe insert a zero into the nort MSB Bit on Shown Below.



* Now Vmaz = 5-05 V & Vmin = 4.93 V

since elce, we insert a one into LSB as shown below.



- Resulting value 01010101 = 85d

2) Given an analog input signal whose voltage ranges from 0 to 5v and an 8-bit digital encoding. Calculate the correct encoding for 3.5v and then trace the successive approximation approach to find the correct encoding.

w



Jan-11,8M

Determine the resolution of an 8-bit ADC with an analog input voltage range of 0 to 5V. Determine the digital encoding for 3.5 volts using a formula and trace the steps using successive approximation technique. Write successive approximation technique. Write the steps for this technique in the form of a table. With necessary columns/informations.

Jan-08,8M

Enstanded System Designmen = 5V, Umin = OV e = 3.5 V, n = 8 - bit

WKT, The encoding should be

$$\frac{e}{V_{\text{max}}} = \frac{d}{(2^{n} - 1)}$$
3.5V

$$\frac{3.5V}{5V} = \frac{0}{2^8-1}$$

d = 178.5

d ≈ 179 -> correct encoding

179 = 10110011

Using successive approximation approach.

Now else thus clear the bit 1200000

$$e^{1} = \frac{3.75 \text{ V} + 2.5 \text{ V}}{3.125 \text{ V}} = 3.125 \text{ V}$$

Now elce le 3.125 < 3.5 v, thus set the bit

$$e^{1} = \frac{3.75 + 3.125 \text{ V}}{2} = 3.437 \text{ V}$$

Dept. OPECE, DSCE ie 3.437 V < 3.75 V, flus set the bit

10110000. Now else, thus clear the bit

$$e^1 = \frac{3.594 + 3.437}{2} = 3.515 \text{ V}$$

e'se thus clear the bit 10110000

7)
$$llment = 3.515$$
 $llmin = 3.437$ $el = 3.515 + 3.437 = 3.476$

elce, thus set the bit 10110010

10110011.

Extend the ratio and resolution equations of analog to digital conversion to any voltage range between Vmin to Vmax rather than O to Vmax.

the resolution of this ADC and also the digital output in binary when the input is 3.5V using formula. Also trace the successive approximation steps for verification. Write it in a tabular form with necessary columns.

June-09,8M

Given: -
$$V_{min} = -5V$$
, $V_{man} = +5V$, $N = 8 - bit$ $8 = 2.5V$

Soln: $e - V_{min}$
 $(2n-i)$
 $3.5 - (-5V)$
 $5V - (-5V)$
 $(28-i)$
 $(3.5 + 5V) = d$
 $(28-i)$
 $216.75 = d$
 $d = 217 \Rightarrow [101001]$

Using Successive approximation approach:

Now e'ce, thus set the bit 10000000

2)
$$V_{max} = 5V$$
, $V_{min} = 0V$
 $e^{1} = \frac{5+0}{2} = 2.5V$ Now $e^{1}X_{e}$, thus set the bit 11000000.

Dept. of ECE, DSCE SV = 3.75 V. Now elee, thus clear the bit

Embedded System Design

11000000

4> Uman = 3.75V, Umin = 2.5V

e = 3.75+2.5V = 3.125 V.

Now ele, set the bit

11010000.

5) Vman = 3.75 V, Vmin = 3.125 V

 $e^{1} = \frac{3.75V + 3.125V}{2} = 3.4375V$

Now elce, thus set the bit

1101 7000

6) Vman = 3.75V, Vmin = 3.4375V

e' = 3.75 + 3.4375 = 3.59375

Now else Thus clear the bit 11011000

7) Vman = 3.59375 V Vmin = 3.4375 V

e = 3.59375 + 3.4375 = 3.515625 V.

Now else, Thus clear the bit 11011020.

8) Vman = 3.515625V , Vmin = 3.4375V

 $e^{1} = \frac{3.515625 + 3.4375}{2} = 3.4765625$

Now e'ce. Thus set the bit 11011001

.: Resulting value 11011001 = 217 d.

4) Assume 8-bit encoding of input voltage in the range -5V to +5V. Calculate the encoding for 1.2V and trace the successive approximation approach to find the correct encoding. What is the resolution of the conversion? Extend the ratio and resolution of ECE DSCE any voltage in the range V_{min} to V_{max}.

Embedded System Design

Soln:
$$e - (Vmin) = d$$

$$Vman - Vmin = 2^{n} - 1$$

$$\frac{1 \cdot 2V - (-5V)}{5 - (-5V)} = \frac{d}{2^{6} - 1}$$

$$e^{1} = \frac{5+0}{7} = 2.5 V$$

Now else. Thus clear the bit 10000000

Dept. of ECE, DSCE Now e'ce. Thus set the bit 10010000.

nbedded System Design 5> Vmax = 1.25 v , Vm)n = 0.625 v $e^{1} = \frac{1.25 + 0.625}{2} = 0.9375 V$ Now e'ce. Thus set the bit 10011000 6) Vman = 1.25V, Vmin = 0.9375V $e^{1} = \frac{1.25 + 0.9375 }{2} = 1.09375$ Now ele. Thus set the bit 10011100 7> Uman = (1.25V, Ymin = 1.09375V Now ele. Thus set the bit 10011110 8> $V_{max} = 1.25 \text{ V}$, $V_{min} = 1.171$ el = 1.25+1.771 = 1.2109 V. Now elge Thus clear the bit 10011110 : Resulting value 100/11/10 = 158 d

5) In successive approximation ADC, calculate the correct encoding of 5V given an analog signal whose voltage ranges from 0 to 5V and an 8-bit digital encoding. Also determine the resolution of this ADC.

Given: - Vman = 5V, Vmin = 0V e = 5V n = 8 - bits.

Saln: - e = dent of ECE DSOF: Vmin $(2^n - 1)$

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Dept. of ECE, DSCE+ 4.8 4375 = 4.921875 V

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Embedded System Designs, set the bit 11111100

7) Vmenx = 5V, Vmin 4.921875V

e1 = 5V + 0.921875V = 4.9609375V

Now e12e. Thus, set the bit 111111110

8) Vmon = 5V, Vmin = 4.9609375V

e1 = 5V + 4.9609375V

e1 = 5V + 4.9609375V

Now e12e. Thus, set the bit 11111111

Pescelting value 11111111 = 255d.

- 6) Given an analog output signal whose voltage should range from 0 to 10V and an 8-bit digital encoding provide the encodings for the following desired voltages.
 - a) Ov b) 1V c) 5.33v d) 10V
 - e) What is the resolution of our conversion?

Given! n=8, $2^{n} = 2^{n} = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^{n} = 2^{n} = 2^{n} = 2^{n} = 2^{n}$ $a) = 2^{n} = 2^$

b) e = 1V $\frac{1V}{10V} = \frac{d}{255}$

pept. of ECE, DSCEd = 25.5

d=25 00011001

Embedded System Design

$$\frac{5.33V}{10} = \frac{d}{255}$$

d> e= lov

e) Resolution = $\frac{V_{man} - V_{min}}{2^{n} - 1} = \frac{10V - 0V}{2^{n} - 1}$