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(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

Department of Electronics & Communication Engg.

Continuous Internal Evaluation – I

Course Name : **EMBEDDEDSYSTEM DESIGN and IOT APPLICATIONS**	Date :	**14/06/2021**
Course Code : **18EC6DCEAI**	Day :	**Monday**
Semester : **6th A, B , C and D**	Timings :	3 TO 4:30PM
Max Marks : **50 M**	Duration :	1½ Hrs.

No.		Question Description	Mks	CO & Levels
Q1	(a)	A design metric is a measurable features of a ……implementation: i) System ii) Software iii) Design iv) NONE	1	
	(b)	Which of the processors have large NRE cost to build the processor? i) Single Purpose ii) General Purpose iii) Application Specific iv) All	1	
	(c)	If a products lifetime is 74 weeks, what is the value of W? i) 34 ii) 35 iii) 36 iv) 37	1	
	(d)	What is the configuration status of control unit in RISC processor? i) Hardwired ii) Micro programmed iii) Both a&b iv) None of the above.	1	
	(e)	The time required for each phase to complete its operations, assuming equal delay in all phases is defined as i) Latency ii) Cycles per Instruction iii) Pipeline cycle iv) Delay	1	
	(f)	Which of the following helps in the generation of waveforms? i) timer ii) inputs iii) outputs iv) memory	1	
	(g)	The Range of 16 bit timer which operates at a clock frequency of 10Mhz is i) 3.55 msec ii) 5.5msec iii) 0.1µsec iv) 6.55m sec	1	
	(h)	The Time between the start of task execution and the end is i) Latency ii) Throughput iii) Speed Up iv) Cycles per Instruction	1	
	(i)	The monetary cost of manufacturing each copy of the system, excluding NRE cost is called as i) Unit Cost ii) Design Cost iii) Both i) &ii) iv) None	1	
	(j)	Assuming PWM output is 5V when High and 0V when Low, Then the duty cycle of 75% would result in average output of i) 1.25V ii) 0.75V iii) 3.75V iv) 3.25V	1	
Q2		Give the comparison between all the three Processor Technologies with schematics.	10	CO3, L3
Q3		Illustrate the important properties which satisfies Memory Hierarchy.	10	CO2, L3
Q4		Explain different types of timer structure with diagram.	10	CO2, L2
		OR		
Q5		List the basic methods used for mapping of information fetched from the main memory to the cache memory. Explain any 2 methods in detail.	10	CO1, L2
Q6		Summarize the SPARC RISC architecture with the processor and a register window.	10	CO2, L2
		OR		
Q7		Determine the most efficient replacement policy among FIFO, LFU & OPT for following conditions No. of Pages in Primary memory = No of word per page = 04 Execution Sequence: 7,0,1,2,0,3,0,4,2,3,0,3,2,3	10	CO2, L

Prepared By
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Approved By
Head of the Department