# Fall time

→ To calculate fall time ($t_f$), assume that $V_{in}$ changes from 0 to $V_{DD}$ at time $t = 0$

The initial condition at the output is $V_{out}(0) = V_{DD}$ when the input is switched, the nFET goes active while the PFET is driven into cutoff. In terms of the switch models, the nFET switch is closed and PFET switch is open. This gives the simplified discharge circuit shown in fig (a). The capacitor $C_{out}$ is initially charged to a voltage $V_{DD}$ and is allowed to discharge through the nFET resistance $R_n$.

The discharging current is given by.

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

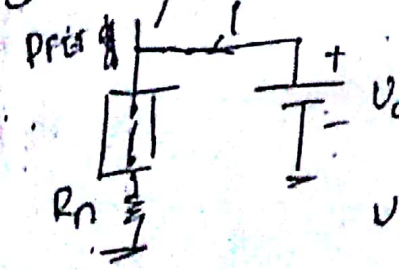
(differential eqn for the discharge event)

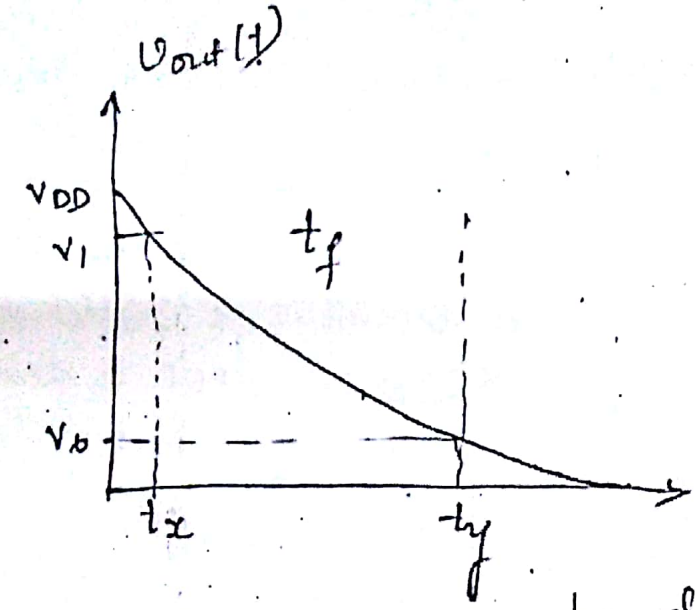
Solving with the initial condition $V_{out}(0) = V_{DD}$ results in the form

$$V_{out}(t) = V_{DD}\, e^{-t/\tau_n} \rightarrow (2)$$

where $\tau_n = R_n C_{out} \rightarrow (3)$ is the nFET time constant

The function is plotted in fig (b).






the fall time $t_f$ may be defined as - it is the time interval from $V_1 = 0.9V_{DD}$ to $V_0 = 0.1V_{DD}$, which are respectively known as the 90% and the 10% voltages as referenced to the full rail swing of $V_{DD}$.

Take a natural logarithm to the eq ② and rearrange.

$$\ln v_{out}(t) = \ln V_{DD}\left(-t/\tau_n\right)$$

$$-t/\tau_n = \ln v_{out}(t) - \ln V_{DD}$$

$$t = \tau_n\left[\ln V_{DD} - \ln v_{out}(t)\right]$$

$$t = \tau_n \ln\left[\frac{V_{DD}}{v_{out}}\right] \longrightarrow ④$$

$$\left[\ln(a) - \ln b = \ln(a/b)\right]$$

fall time $t_f = t_y - t_x$

$$= \tau_n \ln\left(\frac{V_{DD}}{0.1V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9V_{DD}}\right)$$

$$= \tau_n \ln\left(\frac{1}{0.1}\right) - \tau_n \ln\left(\frac{1}{0.9}\right)$$

$= T_n \ln(9)$

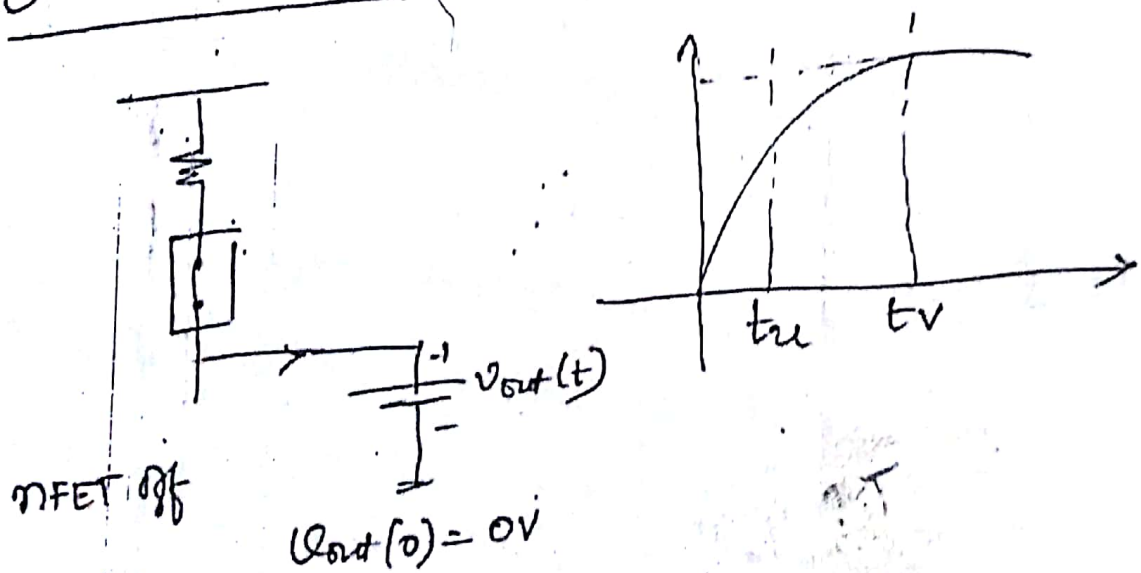
$= 2.2 T_n$

$$\boxed{t_f = 2.2 T_n}$$

The output-fall time in a generic digital logic gate is usually called the output high-to low time $t_{HL}$

$$\boxed{t_{HL} = t_f}$$

The rise time: $t_r$




To calculate rise time $t_r$ Initially input voltage is at $v_{in} = V_{DD}$ and. i.e switched to $v_{in} = 0V$ at $t = 0$ this turns on the PFET while simultaneously driving the nFET into cutoff, this gives the Simplified charging circuit shown in the fig (a)

The output voltage at $t=0$ is given by.

$V_{out}(0) = 0V$.

The charging current is given by.

$$I = C_{out}\frac{dV_{out}}{dt} =$$

$$= \frac{V_{DD} - V_{out}}{R_p} \rightarrow (1)$$

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau_p}\right) \rightarrow (2)$$

$\tau_p$ is the time constant of PFET and is given by.

$$\tau_p = R_p C_{out} \rightarrow (3)$$

Shows the o/p voltage as a function of time the rise time i.e taken between 10% and 90% points such that.

$$t_1 = t_v - t_u$$

taking natural logarithm, & rearrange the terms in eq (2)

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

from eq (2).

$$\left(1 - e^{-t/\tau_p}\right) = \frac{V_{out}}{V_{DD}}$$

$$-e^{-t/\tau_p} = \frac{V_{out}}{V_{DD}} - 1$$

$$-t/\tau_p = \ln\left(\frac{V_{out}}{V_{DD}}\right) - \ln(1)$$

$$t = \tau_p \ln\left(\frac{V_{out}}{V_{DD}}\right) - \tau_p \ln(1)$$

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = \tau_p \ln\left(\frac{V_{out}}{V_{DD}}\right)$$

$$= \tau_p \ln\left(\frac{0.9 V_{DD}}{V_{DD}}\right) - \tau_p \ln\left(\frac{0.1 V_{DD}}{V_{DD}}\right)$$

$$= \tau_p \ln\left(\frac{0.9}{0.1}\right) = \tau_p \ln 9.$$

$$t_f = \ln(9)\,\tau_p = 2.2\tau_p.$$

$$\boxed{t_f = t_{HL}}$$