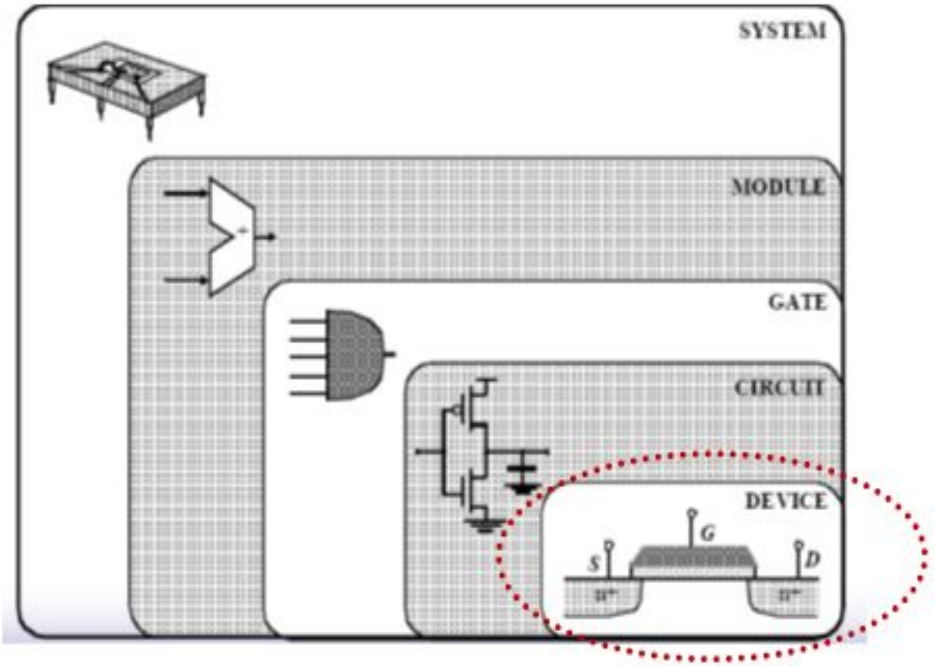
Dayananda Sagar College of Engineering
Department of Electronics and Communication

FUNDAMENTALS OF VLSI DESIGN

By
Dr.Usha. C

VLSI- Different Levels



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COURSE OBJECTIVES:

- To understand the basic concepts of MOSFET and study of MOSFET based circuits.
- To understand the basic fabrication process and lambda-based design rules.
- To acquire the knowledge of Additional CMOS logic structures.
- To design combinational circuits used in data path subsystems.
- To apply MOSFET properties for memory cell design.
- To understand the concept of MOSFET based single stage amplifiers

Module-1

- **Basic MOS Technology:** Introduction to MOS transistors, nMOS fabrication, CMOS fabrication, Bi-CMOS technology. (Text book-1)
- **MOS Transistor Theory:** Introduction, MOS Device Design Equations, nMOS inverter, Alternate form of Pull up, (Text book-1), DC Characteristics of CMOS Inverter, Inverter switching characteristics, Power dissipation (Text book-2),

Module-2

- **Design with MOSFETs:** Ideal switches and Boolean operations, MOSFETs as switches, Basic logic gates in CMOS, Transmission gate (Text book-2)
- **Circuit Design Processes:** MOS layers, Stick diagrams, Design rules and layout – lambda-based design and other rules. Examples. (Text book-1)
- **Additional CMOS Logic Structures:** CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Clocked CMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic (Text book-2)

Module-3

- **CMOS Sub System Design:** Introduction, Addition/Subtraction, Single bit addition, Full adder design, Carry-Propagate Adders, Carry Generation and Propagation, PG Carry-Ripple Addition, Manchester Carry Chain Adder, Carry-Skip Adder, Carry-Look ahead Adder, Carry-select adder, Zero/one detectors, comparators, Shifters, Multiplication. (Text book-3)

Module-4

- **Array Subsystems:** Introduction, Static Random-Access Memory (SRAM), Dynamic Random-Access Memory (DRAM), Read only Memory, Serial Access Memories, Content addressable memory. (Text 3)

Module-5

- **The MOS Amplifiers:** The Basis for Amplifier Operation, Analysis of Transfer characteristics (both graphical and Analytical), Small-Signal Operation and Models, The DC Bias Point , The Signal Current in the Drain Terminal, The Voltage Gain, Separating the DC Analysis and the Signal Analysis ,Small-Signal Equivalent-Circuit Models ,The Trans conductance (Text book-4), Single-Stage MOS Amplifiers : The Common-Source (CS) Amplifier , The Common-Source Amplifier resistive load , The Common-Gate (CG) Amplifier ,The Common-Drain or Source-Follower Amplifier , Basic Current mirrors (Text book -5)

TEXT BOOKS:

Douglas A. Pucknell, Kamran E., "Basic VLSI Design", 3rd Edition, *PHI Publication*, India.

John P.Uyemura, "Introduction to VLSI Circuits and Systems", Wiley India Edition, 3rd print, 2007.

Neil H.E. Weste, Harris, Banerjee, "CMOS VLSI design", *Pearson*, Third Edition, 2007.

Adel A. Sedra and K.C. Smith, "Microelectronics Circuits", 7th edition, *Oxford University Press*, *International Version*, 2009.

Behzad Razavi, "Design of Analog CMOS Integrated Circuits", *TMH*, India, 2007.

REFERENCE BOOKS :

Behzad Razavi, "Fundamentals of Microelectronics", *John Wiley India* Pvt. Ltd, 2008.

Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, *Pearson Education* (*Asia*) *Pvt. Ltd*. 2000.

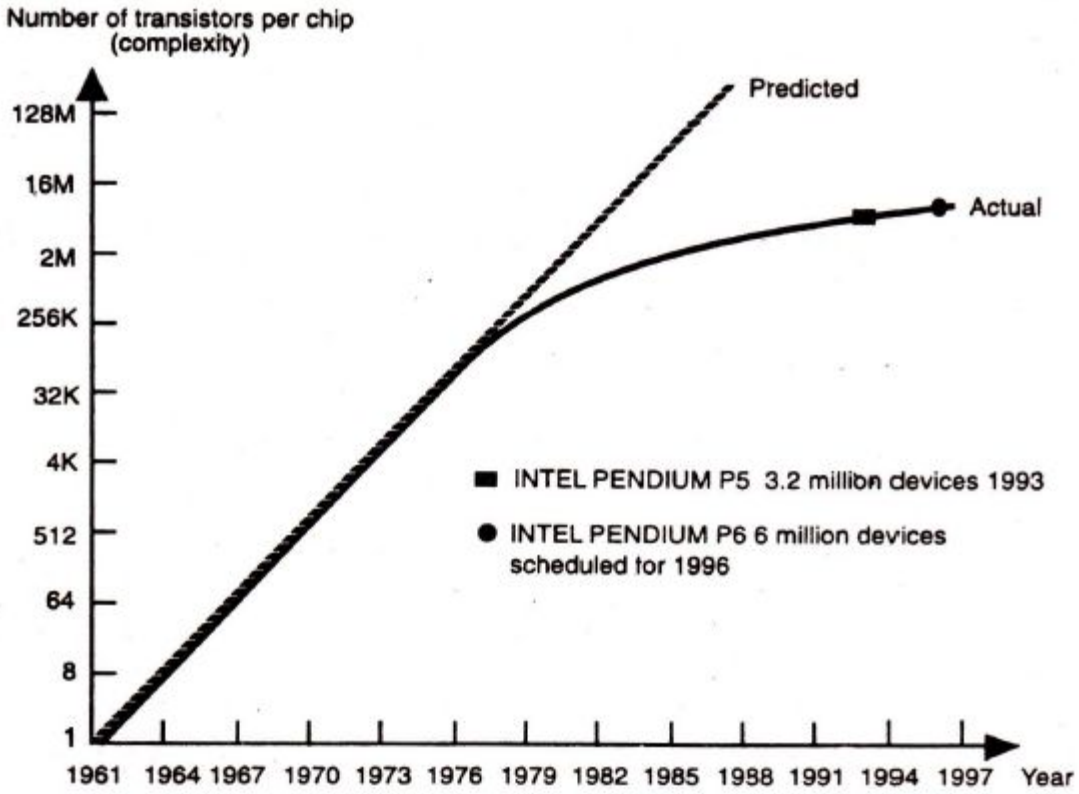
Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", *Tata McGraw-Hill*, Third Edition.

Jhon P Uyemura, "Introduction to VLSI Circuits and Systems", *Wiley India* (*P*) *Ltd*., New Delhi, 2002.

Sung Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits: *Analysis and Design*", 3rdEdition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.

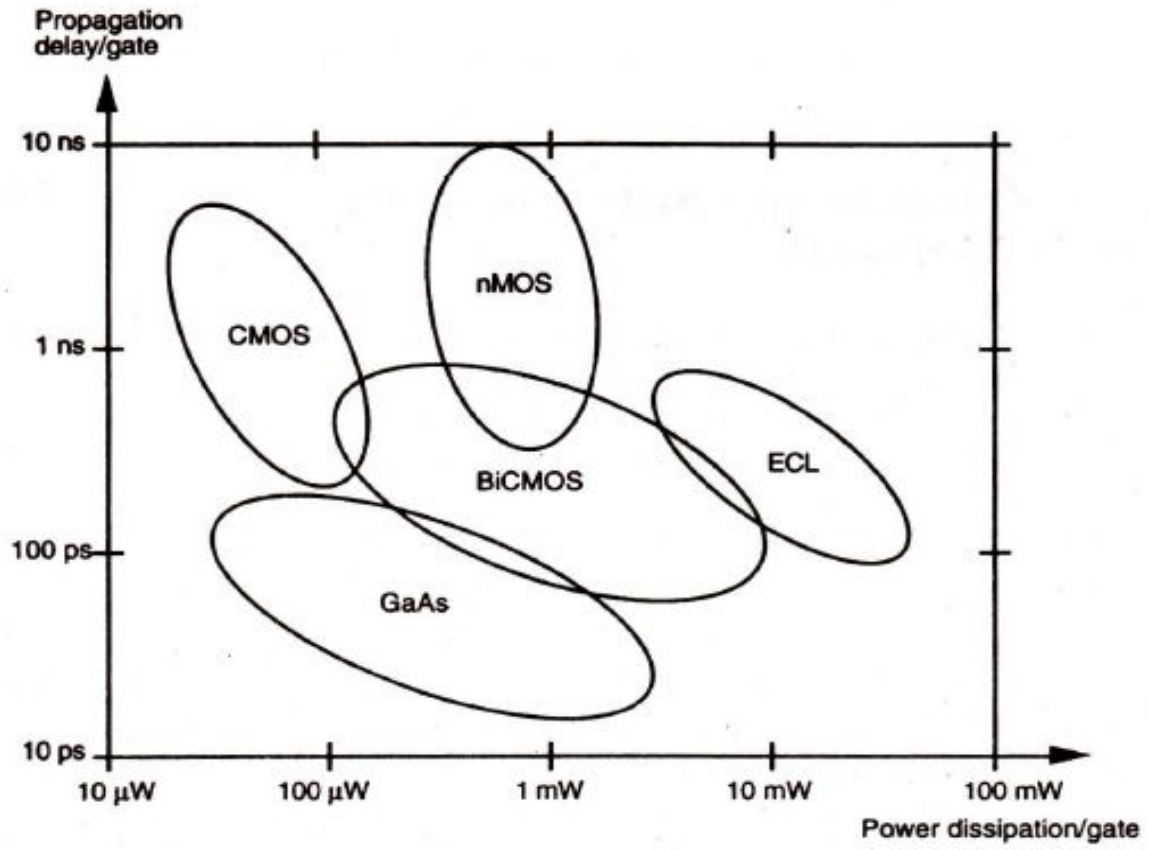
D.A. Hodges, H.G. Jackson and R.A. Saleh, "Analysis and Design of Digital Integrated Circuits", 3rd Edition, *Tata McGraw-Hill Publishing Co. Limited*, New Delhi, 2007.

INTRODUCTION TO INTEGRATED CIRCUIT TECHNOLOGY



Note: K signifies a multiplier of 1024 and M a multiplier of 1,048,576.

DIFFERENT FABRICATION TECHNOLOGIES



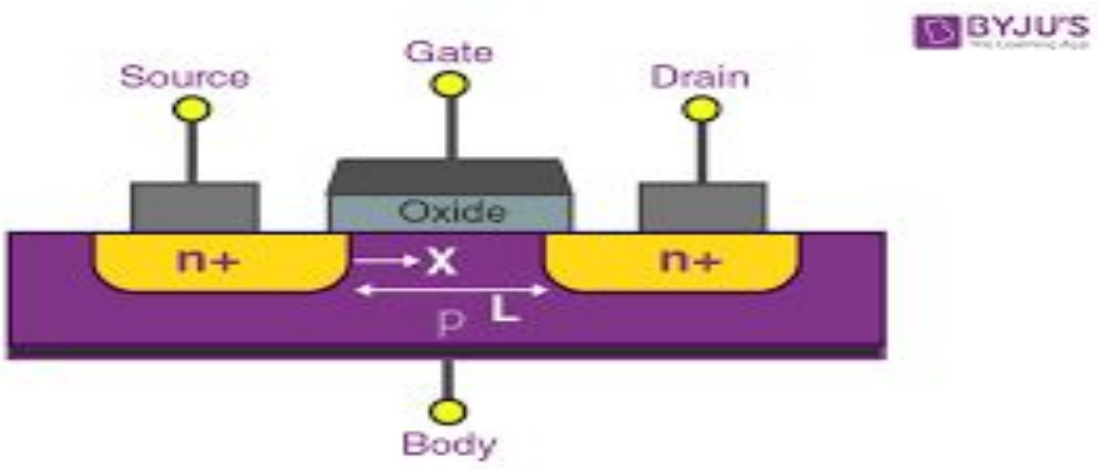
METAL-OXIDE-SEMICONDUCTOR (MOS) AND RELATED VLSI TECHNOLOGY

TABLE 1.1 Microelectronics evolution

Year	*1947*	*1950*	*1961*	*1966*	*1971*	*1980*	*1990*	*2000*
Technology	*Invention of the transistor*	*Discrete components*	*SSI*	*MSI*	*LSI*	*VLSI*	*ULSI**	*GSI†*
Approximate numbers of transistors per chip in commercial products	1	1	10	100–1000	1000–20,000	20,000–1,000,000	1,000,000 10,000,000	>10,000,000
Typical products	—	Junction Transistor and diode	Planar devices Logic gates Flip-flops	Counters Multiplexers Adders	8 bit micro-processors ROM RAM	16 and 32 bit micro-processors Sophisticated peripherals GHM Dram	Special processors, Virtual reality machines, smart sensors	

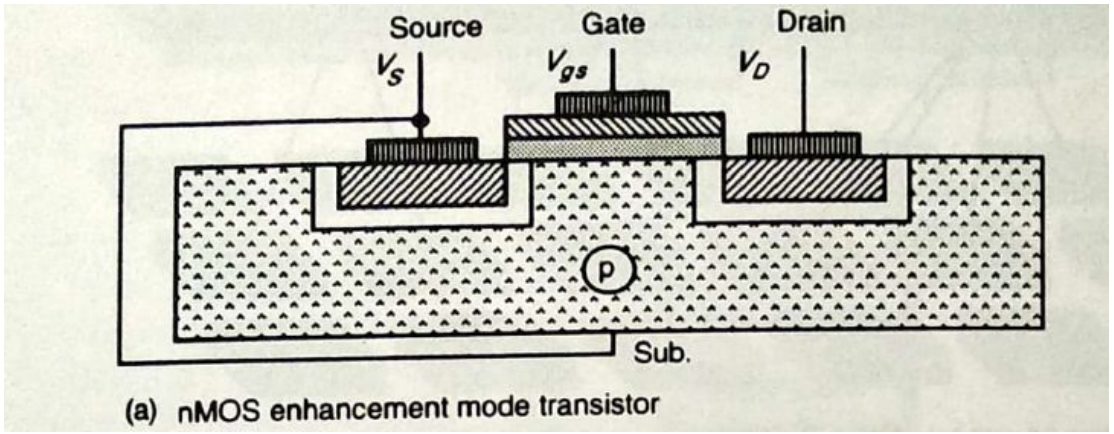
* Ultra large-scale integration
† Giant-scale integration

MOSFET

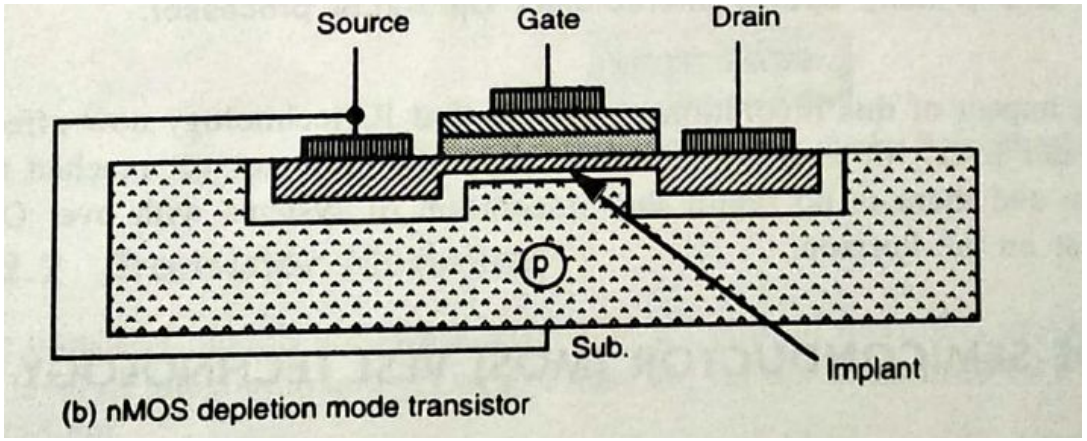


Fundamentals of MOSFET

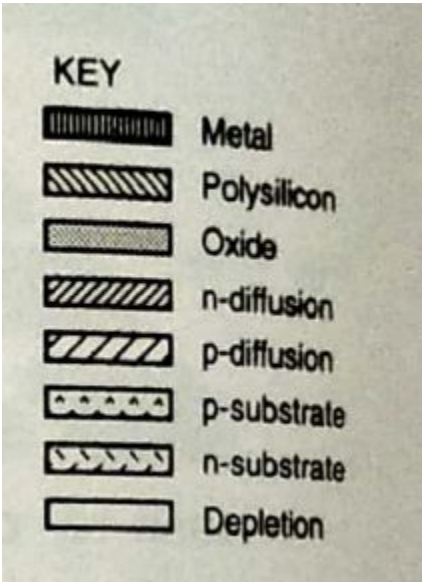
Basic MOS Transistor

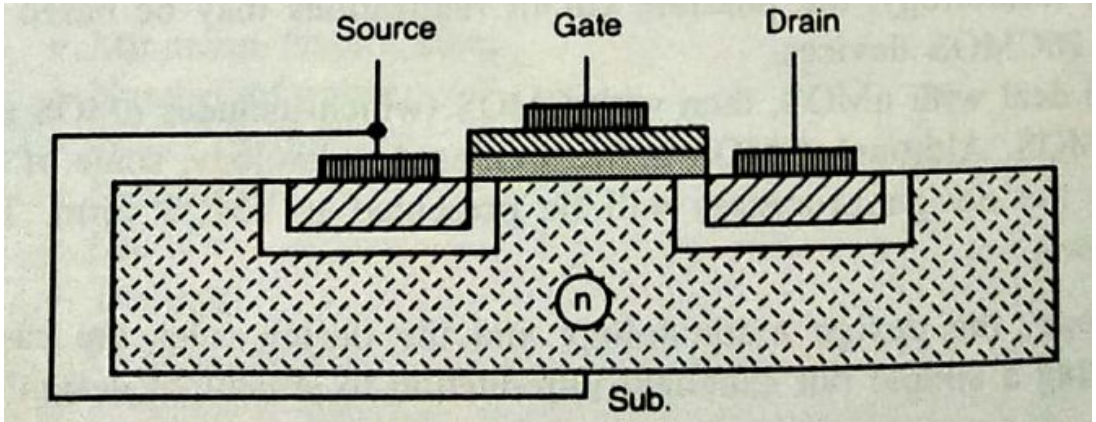


(a) nMOS enhancement mode transistor



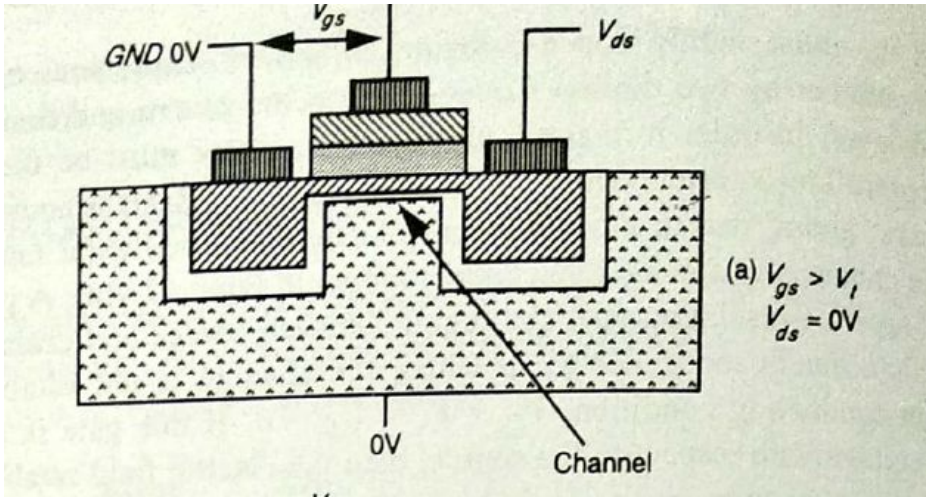
(b) nMOS depletion mode transistor

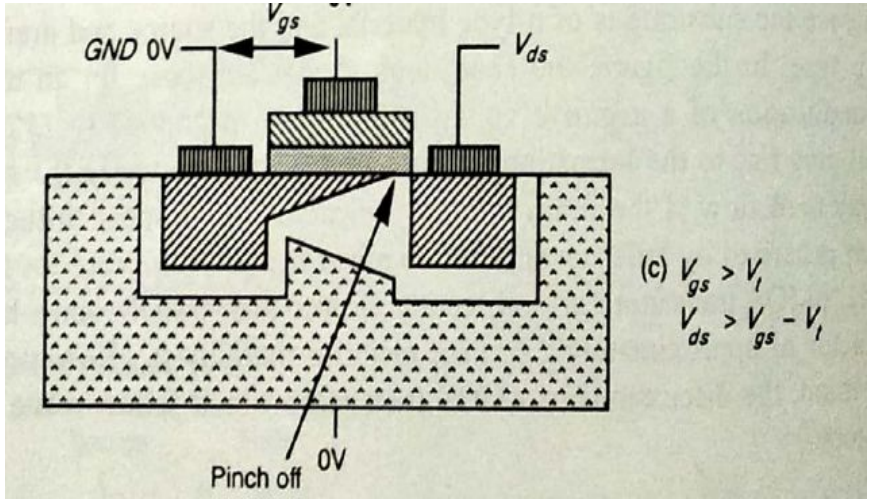


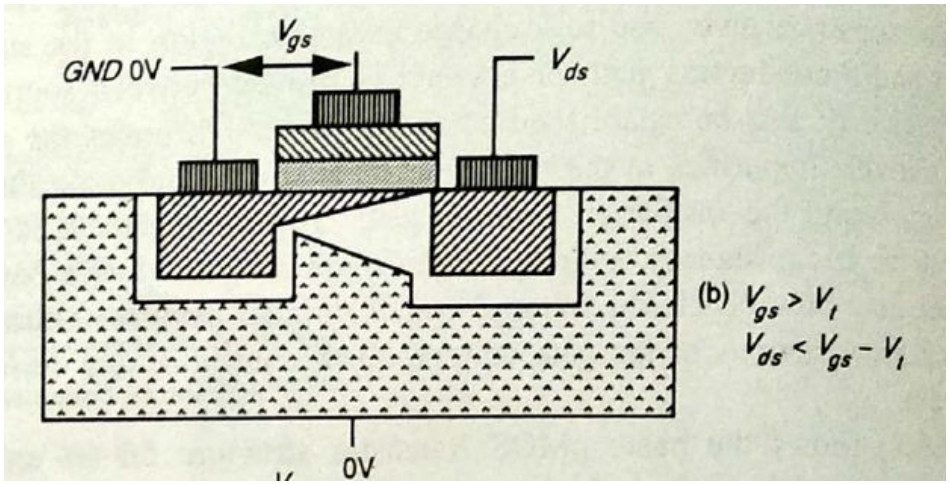


(c) pMOS enhancement mode transistor

Enhancement mode Transistor



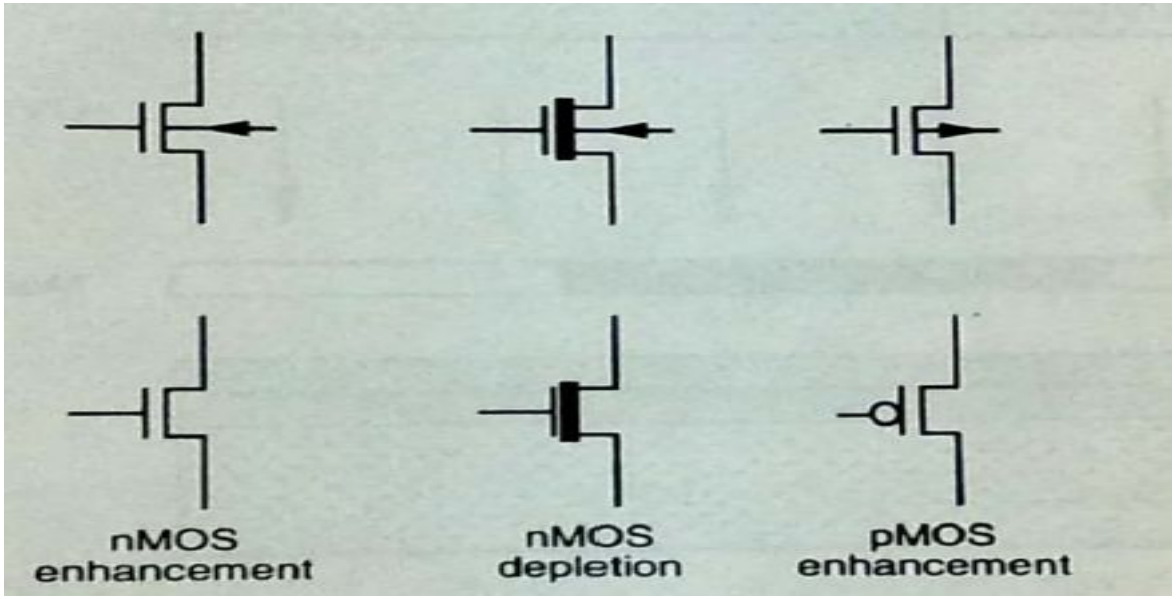




Enhancement mode transistor for particular values Vds with (Vgs>Vt)

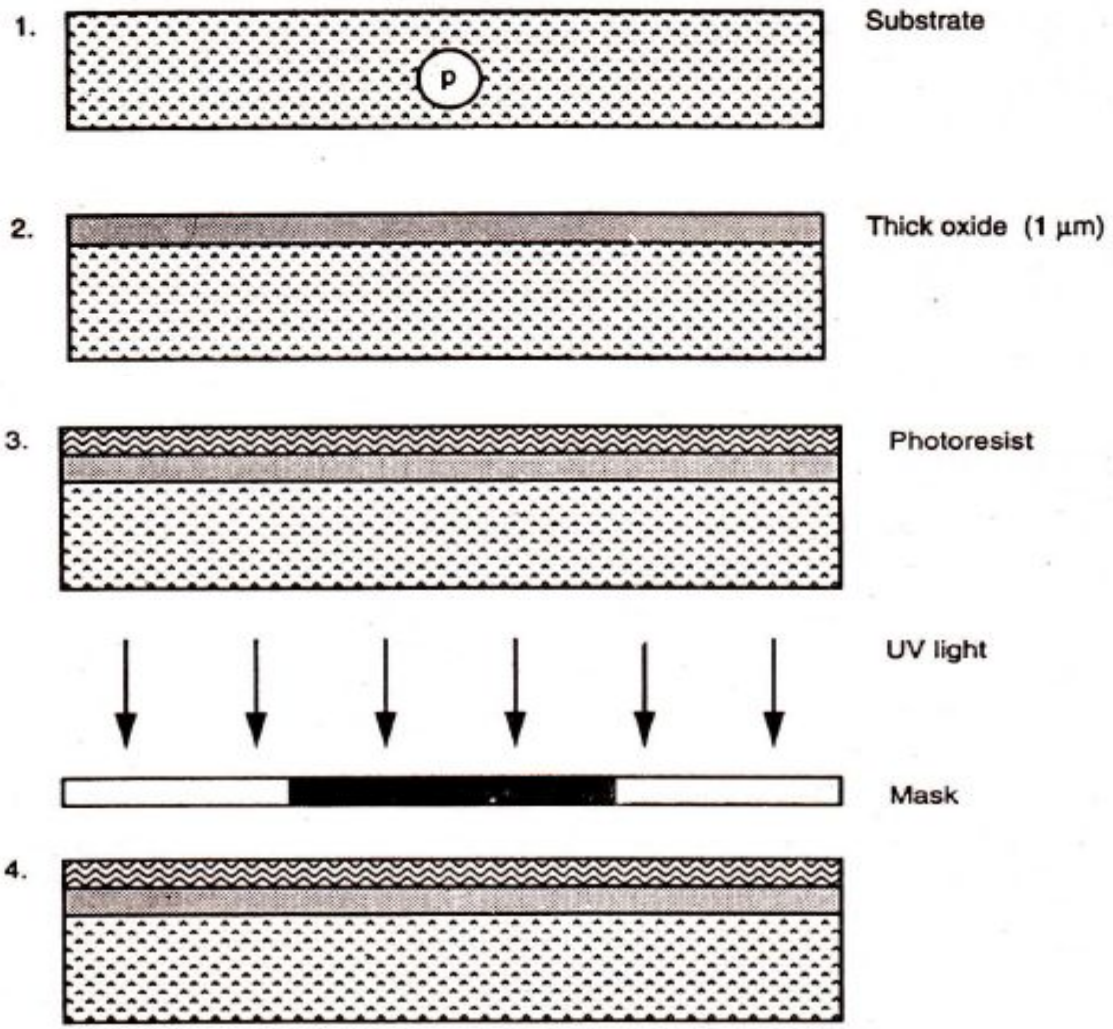
Depletion Mode Transistor

- The channel is established because of the implant even when Vgs=0 and
- To cause the channel to cease to exist a negative voltage Vtd must be applied between gate and source
- V_{td}<-0.8V_{DD}



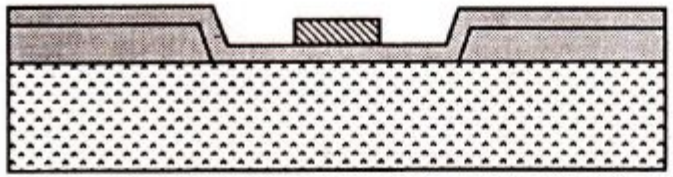
Transistor Circuit Symbols

nMOS FABRICATION

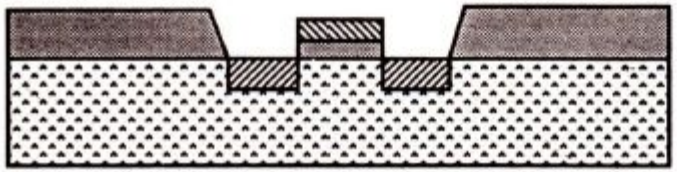


5. 

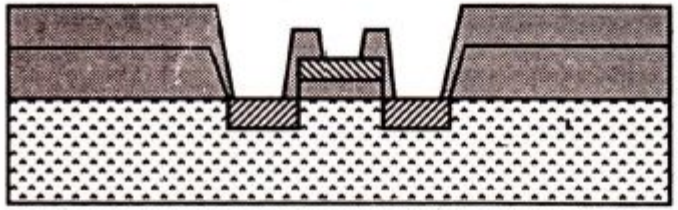
Window in oxide

6. 

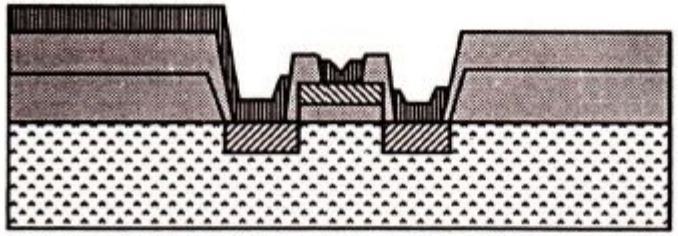
Patterned poly. (1–2 μm)
on thin oxide (800–1000 Å)

7. 

n^+ diffusion (1 μm deep)

8. 

Contact holes (cuts)

9. 

Patterned metallization
(aluminum 1 μm)

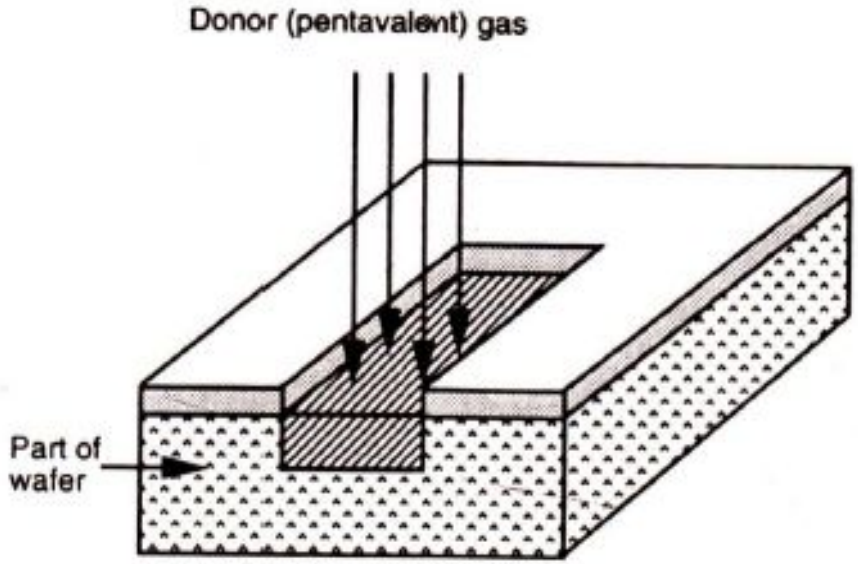
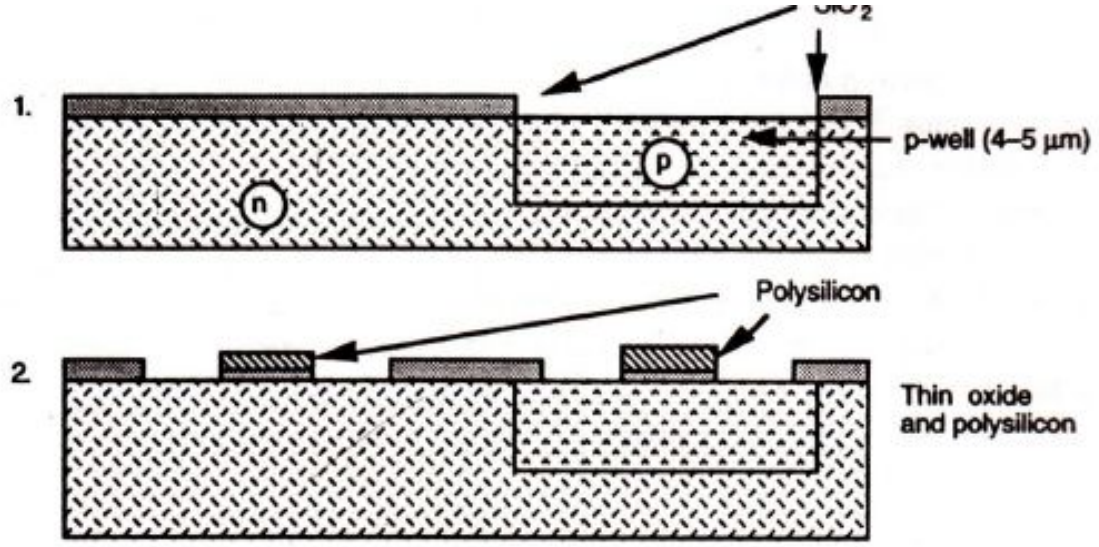
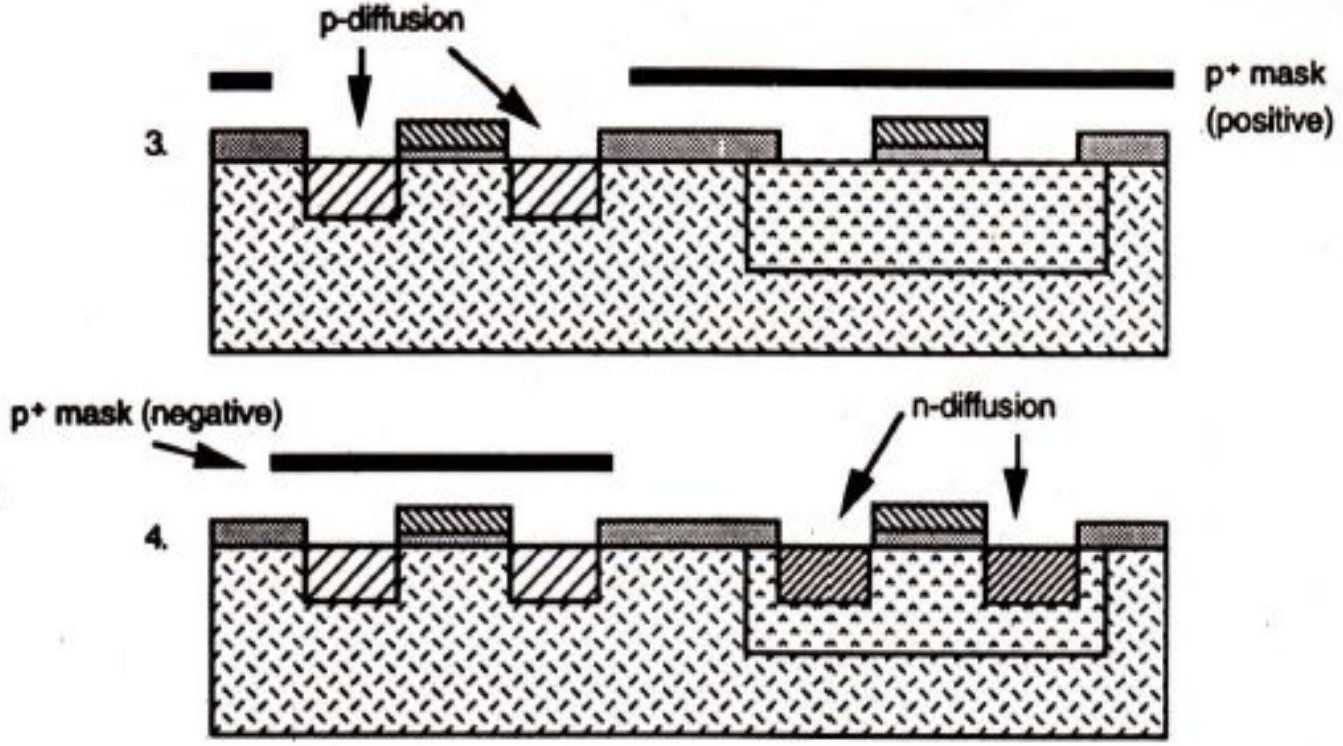


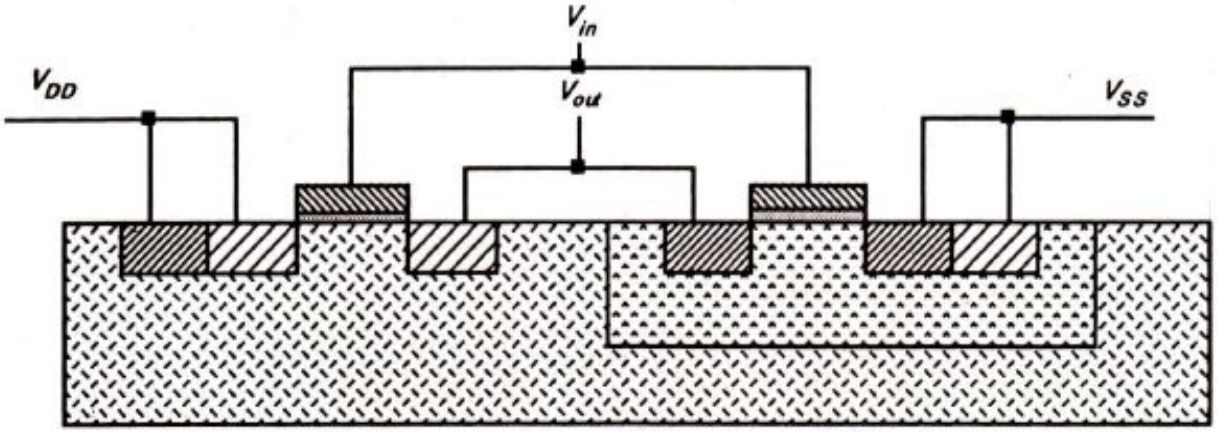
FIGURE 1.8 Diffusion process.

CMOS FABRICATION

- **The p-well Process**




p-diffusion
p+ mask
(positive)
3.
p+ mask (negative)
n-diffusion
4.



CMOS p-well inverter showing *VDD* and *VSS* substrate connections.

The n-well Process

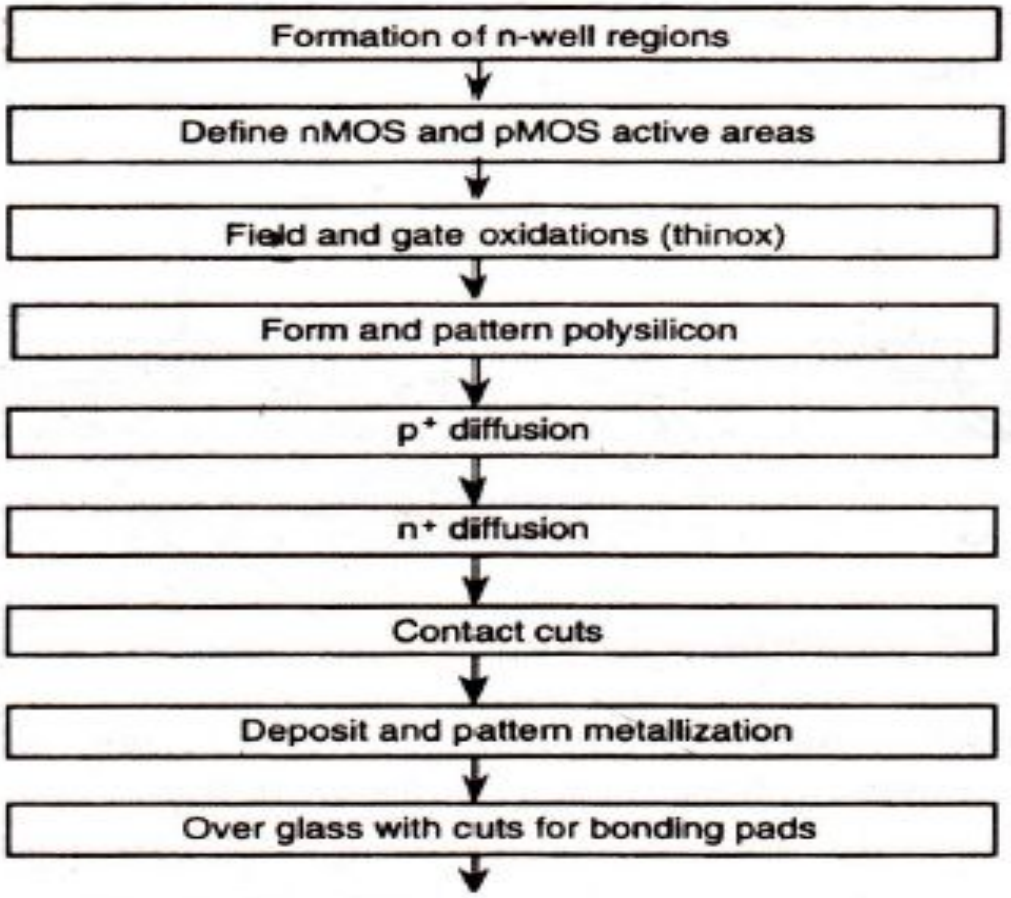


FIGURE 1.11 Main steps in a typical n-well process.

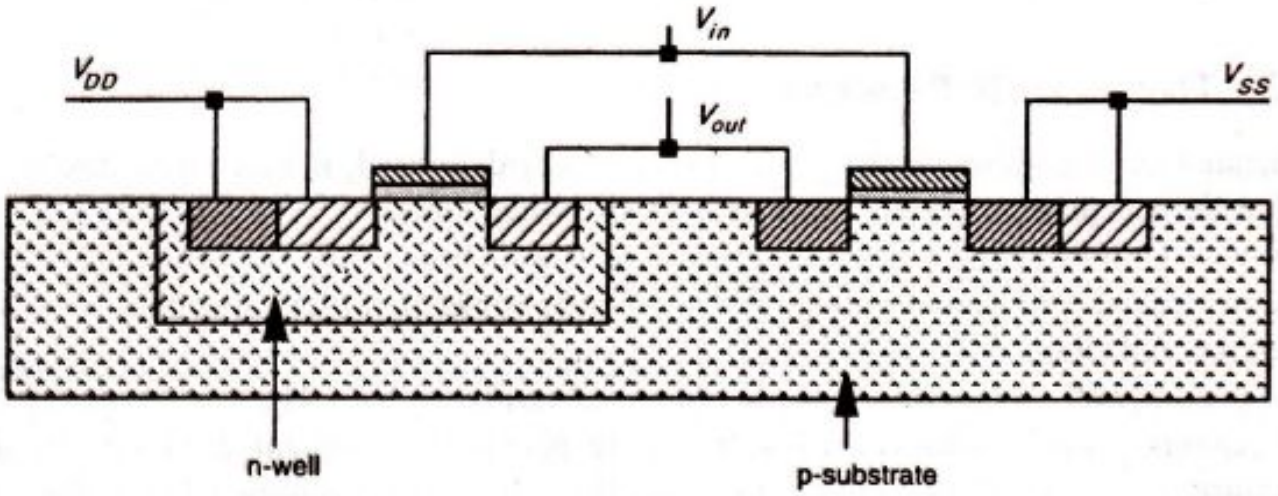


FIGURE 1.12 Cross-sectional view of n-well CMOS inverter.

The Twin-Tub Process

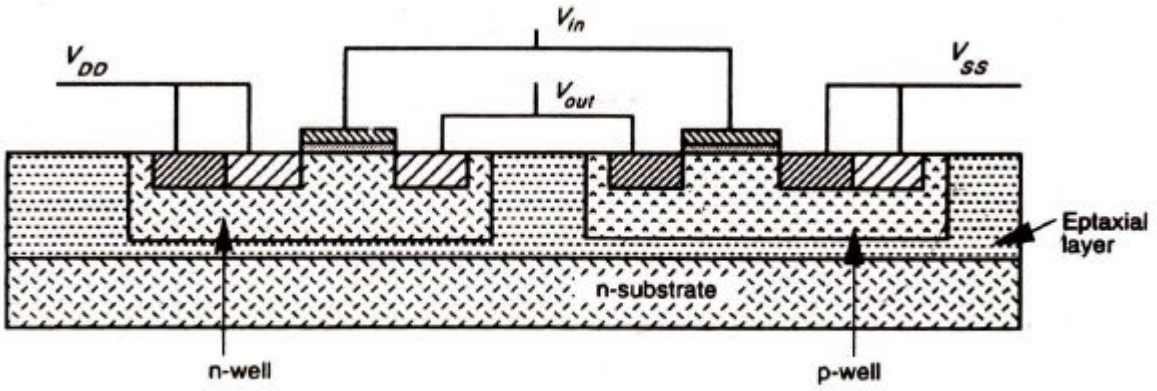
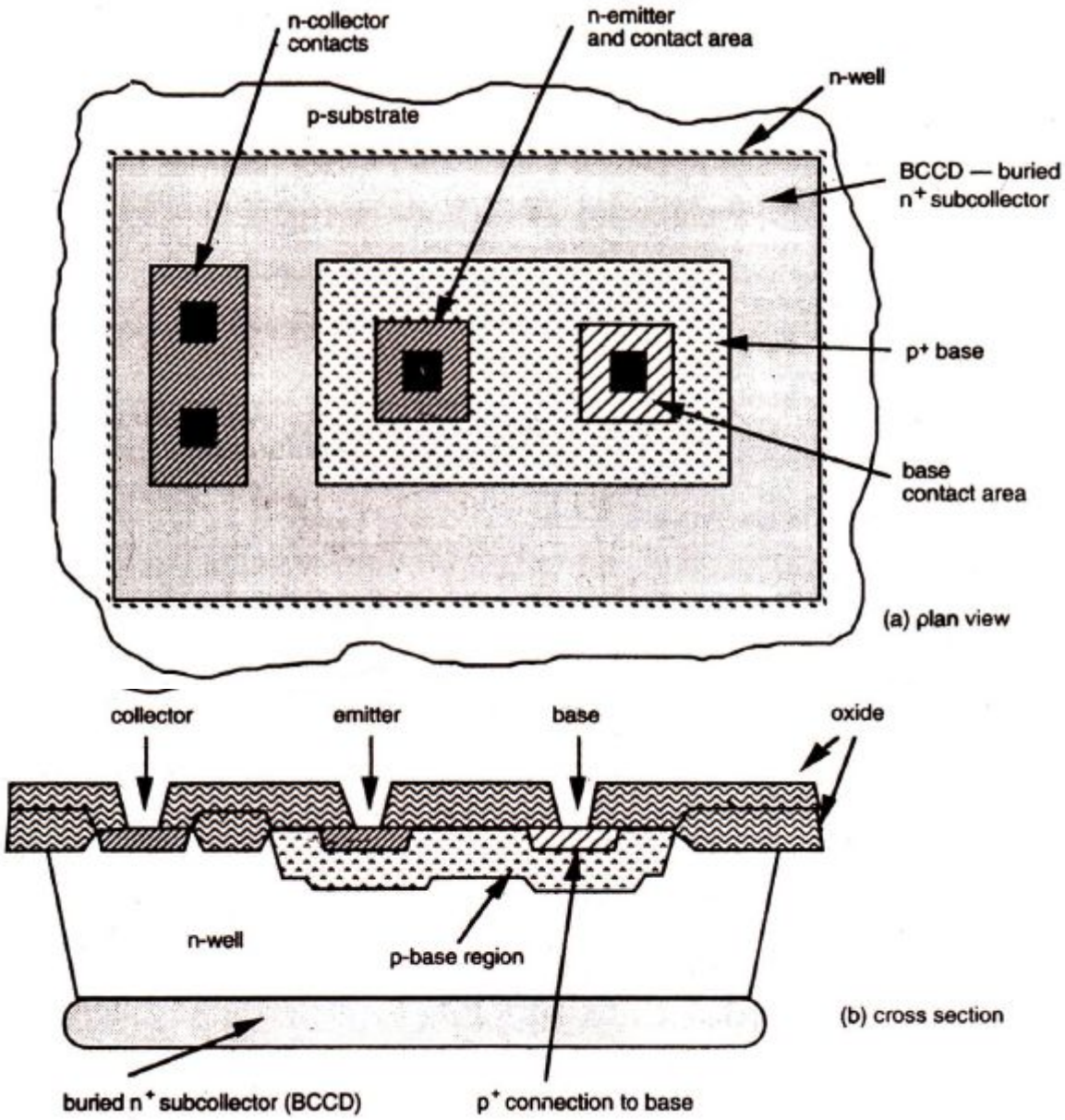


FIGURE 1.14 Twin-tub structure.

BICMOS TECHNOLOGY



Comparison of CMOS and Bipolar Technology

CMOS technology	*Bipolar technology*
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load (fan-out limitations)	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m ($g_m \alpha V_{in}$)	• High g_m ($g_m \alpha e^{V_{in}}$)
	• High f_t at low currents
• Bidirectional capability (drain and source are interchangeable)	• Essentially unidirectional
• A near ideal switching device	

Drain to Source Current I_{ds} versus Voltage V_{ds} Relationships

$$I_{ds} = -I_{sd} = \frac{Charge\ induced\ in\ channel(Q)}{Electron\ Transit\ Time(\tau)}$$

$$\tau_{sd} = \frac{Length\ of\ channel(L)}{Velocity(v)}$$

$$v = \mu E_{ds}$$

$$\mu = electron\ or\ hole\ mobility(surface)$$

$$E_{ds} = electric\ field(drain\ to\ source)$$

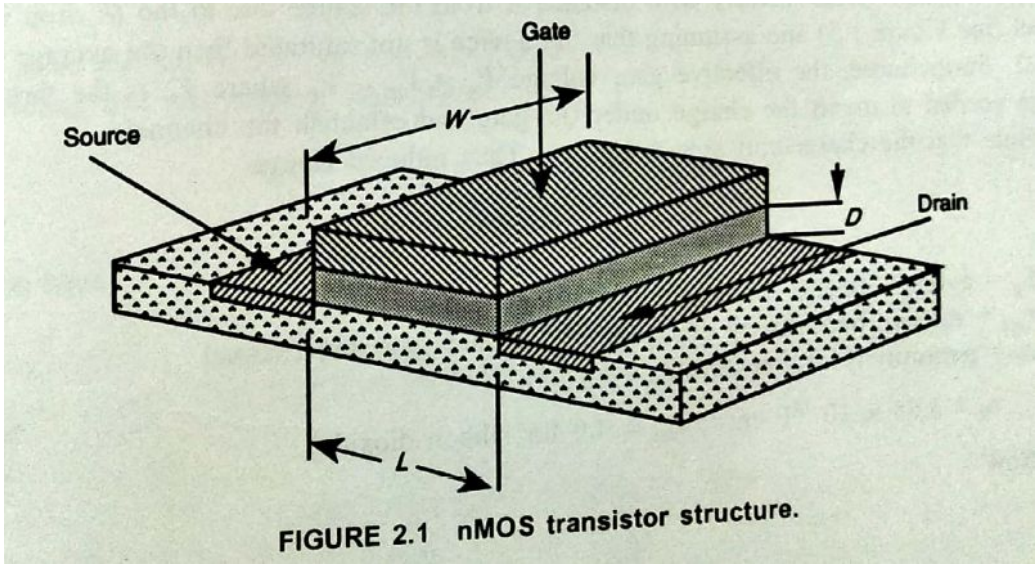


FIGURE 2.1 nMOS transistor structure.

$$E_{ds} = \frac{V_{ds}}{L} \qquad v = \frac{\mu V_{ds}}{L}$$

Thus, Transit Time is

$$\tau_{sd} = \frac{L^2}{\mu V_{ds}} \qquad (2)$$

Typical Values of μ at room temperature

$$\mu_n = 650\,cm^2/V\ \sec(surface)$$

$$\mu_p = 240\,cm^2/V\ \sec(surface)$$

The Non Saturated region

- Charge induced in channel due to gate voltage is due to the voltage difference between the gate and channel
- Voltage along the channel varies linearly with distance X from the source due to the IR drop in channel
- Device in non saturated then the average value is Vds/2
- The effective gate voltage Vb=Vgs-Vt
- Vt is the threshold voltage needed to invert the charge under the gate and establish the channel

$$\text{Charge/unit area} = E_g \varepsilon_{ins} \varepsilon_0$$

Induced Charge is

$$Q_c = E_g \varepsilon_{ins} \varepsilon_0 WL$$

$$\varepsilon_0 = 8.85 \times 10^{-14} \, Fcm^{-1}$$

$$\varepsilon_{ins} = 4.0 \;\; for \; Silicon \; dioxide$$

Eg= average electric field gate to channel

ε_{ins}= relative permittivity of insulation between gate and channel

ε_0 =permittivity of free space

$$E_g = \frac{\left(\left(V_{gs} - V_t \right) - \frac{V_{ds}}{2} \right)}{D}$$

D- oxide thickness

$$Q_c = \frac{WL\varepsilon_{ins}\varepsilon_0}{D}\left(\left(V_{gs} - V_t \right) - \frac{V_{ds}}{2} \right) \qquad (3)$$

Combining equations (2) and (3) in (1), we have

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}\frac{W}{L}\left(\left(V_{gs} - V_t \right) - \frac{V_{ds}}{2} \right)V_{ds}$$

$$I_{ds} = K\frac{W}{L}\left(\left(V_{gs} - V_t \right)V_{ds} - \frac{V^2 ds}{2} \right) \qquad (4)$$

In the non-saturated or resistive region where $V_{ds} \langle V_{gs} - V_t$

$$K = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}$$

The factor W/L is of course, contributed by the geometry and it is common practice to write

$$\beta = K\frac{W}{L}$$

$$I_{ds} = \beta\left(\left(V_{gs} - V_t \right)V_{ds} - \frac{V_{ds}^2}{2} \right) \qquad (4a)$$

Gate/channel capacitance is given as

$$C_g = \frac{\varepsilon_{ins}\varepsilon_0 WL}{D}(parallel\ \ plate)$$

$$K = \frac{C_g \mu}{WL}$$

$$I_{ds} = \frac{C_g \mu}{L^2}\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right) \qquad (4b)$$

It is convenient to use Gate capacitance per unit area

$$C_g = C_0 WL$$

we may also write

$$I_{ds} = C_0 \mu \frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right)$$

The Saturated Region

- Saturation begins when Vds=Vgs-V, since at this point the IR drop in the channel equals the effective gate to channel voltage at the drain.
- The current remains constant as Vds increases

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2} \qquad (5)$$

Or we may write

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 \qquad (5a)$$

$$I_{ds} = K\frac{C_g \mu}{2L^2}(V_{gs} - V_t)^2 \qquad (5b)$$

we may also write

$$I_{ds} = C_0 \mu \frac{W}{2L}(V_{gs} - V_t)^2 \qquad (5c)$$

Threshold voltage for nMOS depletion mode device denoted as Vtd

Aspects of MOS Transistor Threshold Voltage Vt

The threshold voltage Vt may be expressed as

$$V_t = \phi_{ms} \frac{Q_B - Q_{ss}}{C_0} + 2\phi_{fN} \qquad (6)$$

Where

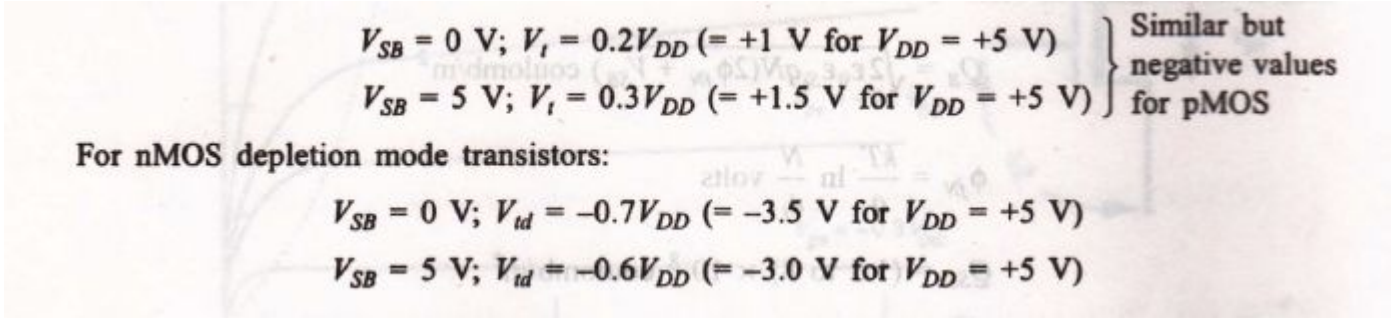
Q_B= the charge per unit area in the depletion layer beneath the oxide

Qss=Charge density at Si:SiO2 interface

C0=capacitance per unit gate area

ϕ_{ms}=Workfunction difference between gate and Si

ϕ_{fN} = Fermi level potential between inverted surface and bulk Si



MOS TRANSISTOR TRArNSCONDUCTANCE *gm,* AND OUTPUT CONDUCTANCE gds

Transconductance expresses the relationship between output current and the input voltage is defined as

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \Big| V_{ds} = \text{constant}$$

To find an expression for gm in terms of circuit and transistor parameters, consider the charge in channel Qc is such that

$$\frac{Q_c}{I_{ds}} = \tau$$

Where τ is transit time. Thus change in current

$$\delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$$

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$\delta I_{ds} = \frac{\delta Q_c V_{ds} \mu}{L^2}$$

but change in charge

$$\delta Q_c = C_g \delta V_{gs}$$

so that

$$\delta I_{ds} = \frac{C_g \delta V_{gs} \mu V_{ds}}{L^2}$$

Now

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

In saturation

$$V_{ds} = V_{gs} - V_t$$

$$g_m = \frac{C_g \mu}{L^2} (V_{gs} - V_t) \tag{2.7}$$

and substituting for $C_g = \frac{\varepsilon_{ins} \varepsilon_0 WL}{D}$

$$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0}{D} \frac{W}{L} (V_{gs} - V_t) \tag{2.7a}$$

Alternatively,

$$g_m = \beta (V_{gs} - V_t)$$

The output conductance g_{ds} can be expressed by

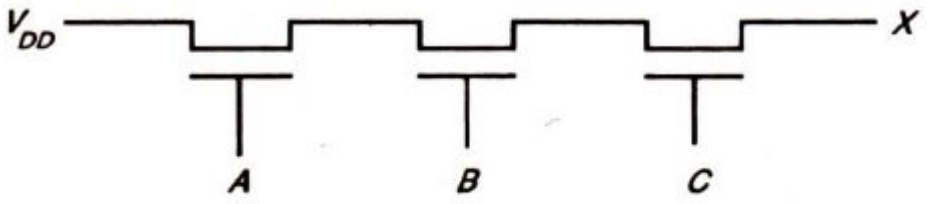
$$g_{ds} = \frac{\delta I_{ds}}{\delta V_{gs}} = \lambda . I_{ds} \; \alpha \left(\frac{1}{L} \right)^2$$

Here the strong dependence on the channel length is demonstrated as

$$\lambda \alpha \left(\frac{1}{L} \right) \text{ and } I_{ds} \; \alpha \left(\frac{1}{L} \right)$$

for the MOS device.

THE PASS TRANSISTOR



$X = A.B.C$ (Logic 1 = $V_{DD} - V_t$)

$\overline{X} = ?$

THE nMOS INVERTER

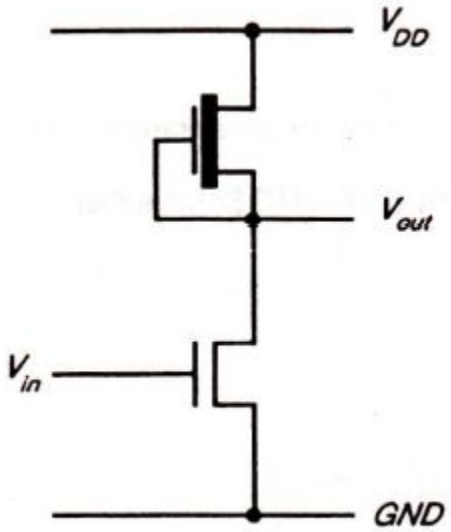
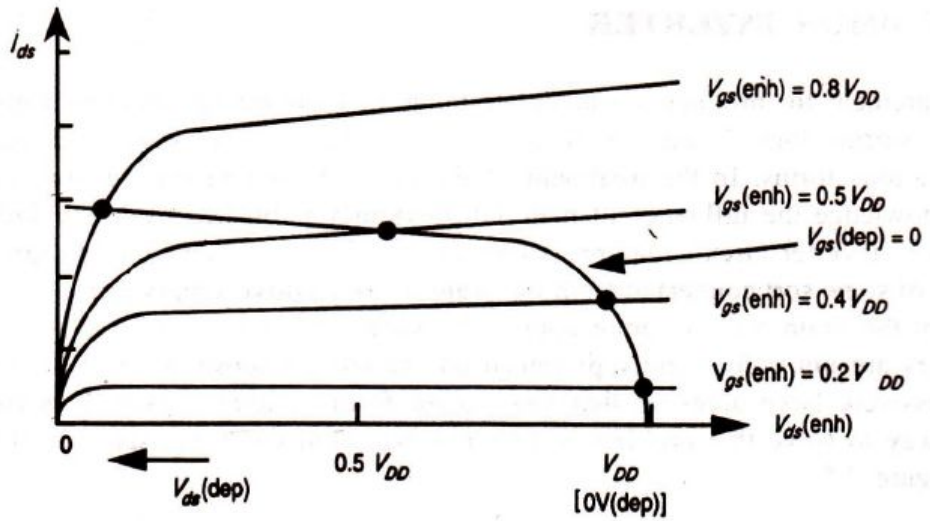
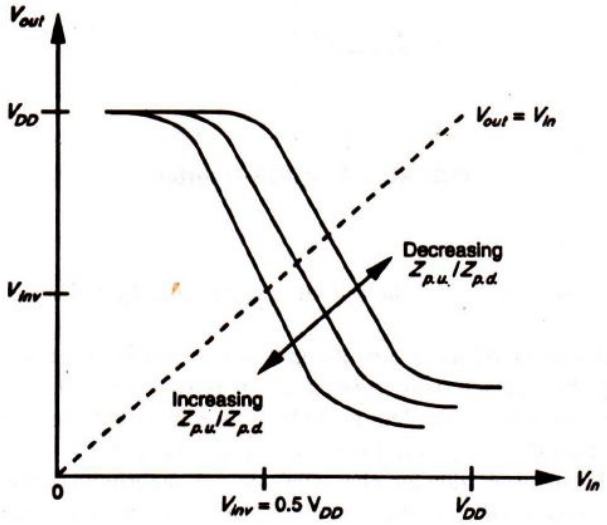


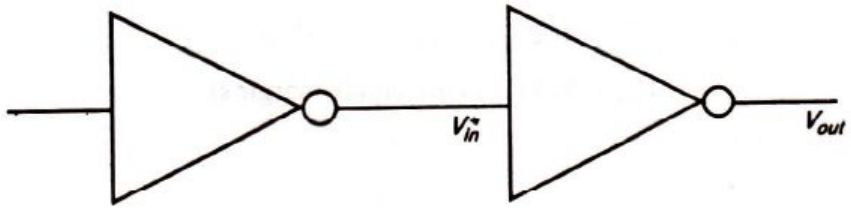
FIGURE 2.5 nMOS inver





DETERMINATION OF PULL-UP TO PULL-DOWN RATIO *(Zp.u} Zp.d.)* FOR AN nMOS INVERTER DRIVEN BY ANOTHER nMOS INVERTER

$$V_{in} = V_{out} = V_{inv}$$



For equal margins around the inverter threshold, we set $V_{inv} = 0.5V_{DD}$. At this point both transistors are in saturation and

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2}$$

In the depletion mode

$$I_{ds} = K\frac{W_{p.u.}}{L_{p.u.}}\frac{(-V_{td})^2}{2} \text{ since } V_{gs} = 0$$

and in the enhancement mode

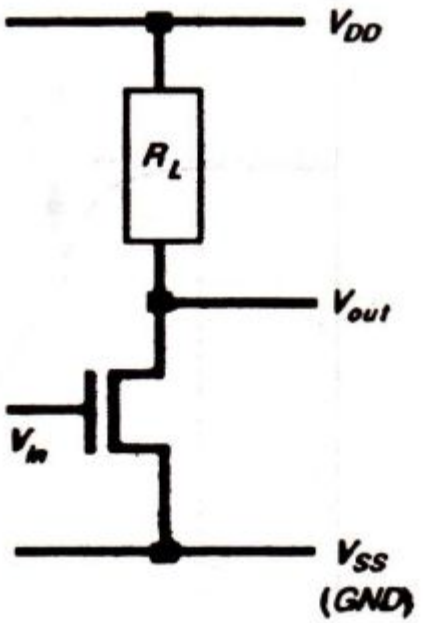
$$I_{ds} = K\frac{W_{p.d.}}{L_{p.d.}}\frac{(V_{inv} - V_t)^2}{2} \text{ since } V_{gs} = V_{inv}$$

Equating (since currents are the same) we have

$$\frac{W_{p.d.}}{L_{p.d.}}(V_{inv} - V_t)^2 = \frac{W_{p.u.}}{L_{p.u.}}(-V_{td})^2$$

Alternative forms of Pull-Up

1. Load resistance RL



2. nMOS depletion mode transistor pull-up

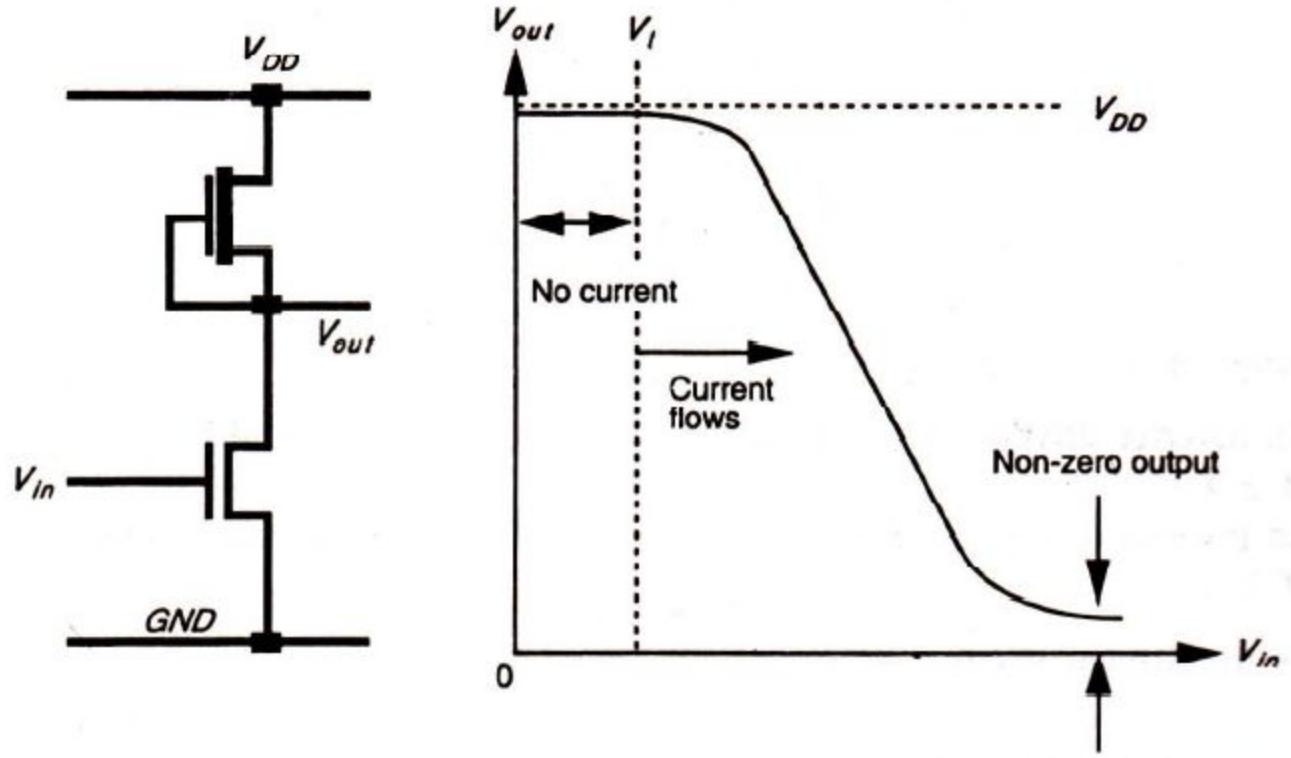


FIGURE 2.12 nMOS depletion mode transistor pull-up and transfer characteristic.

3. nMOS enhancement mode pull-up

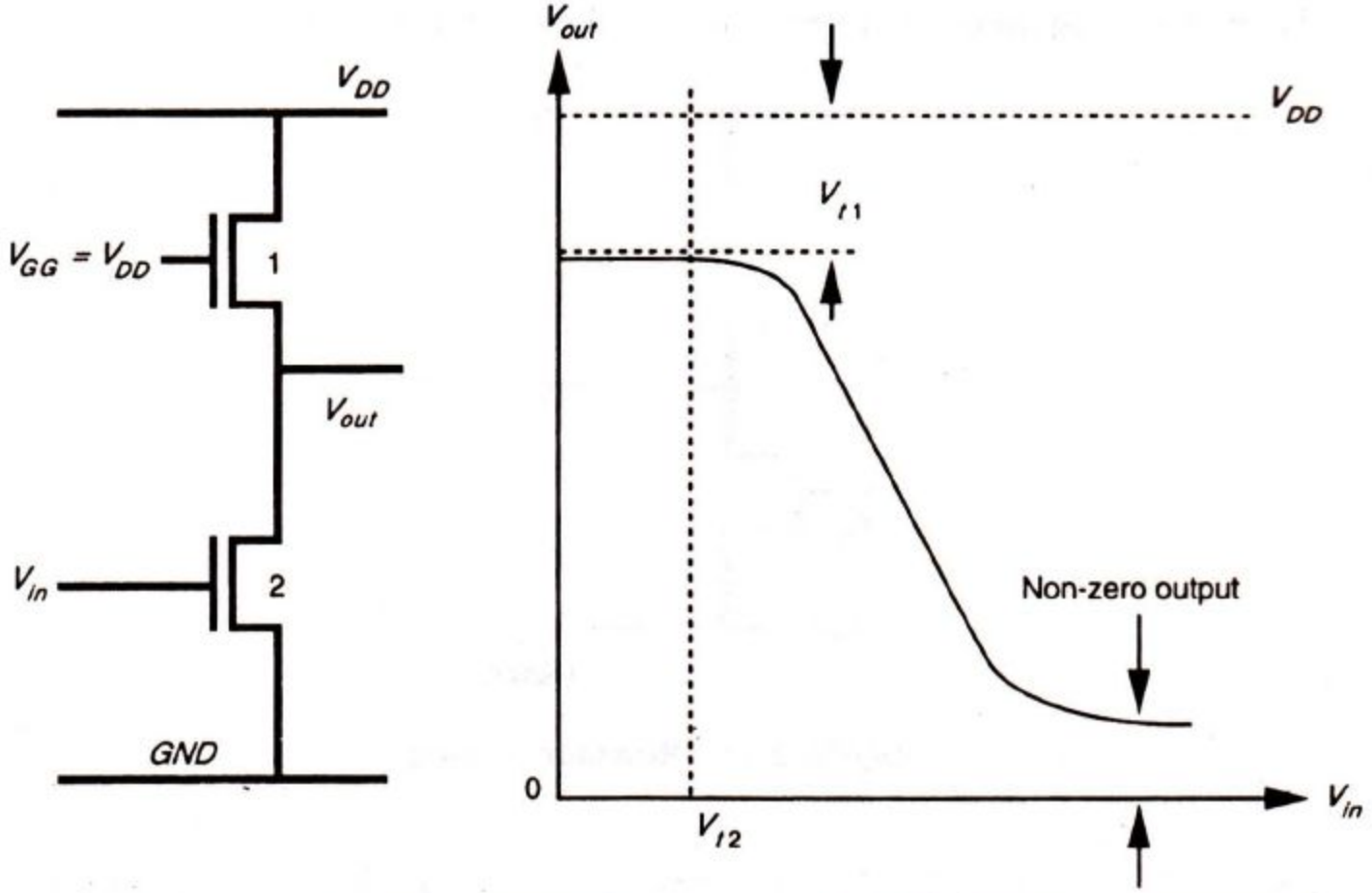
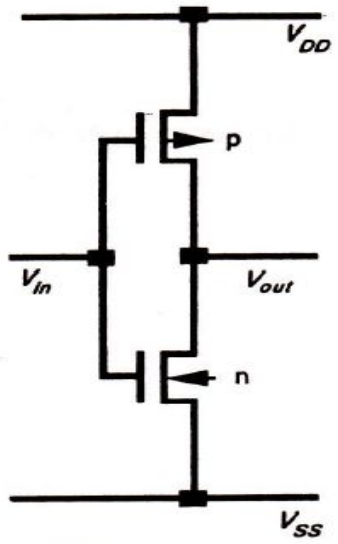
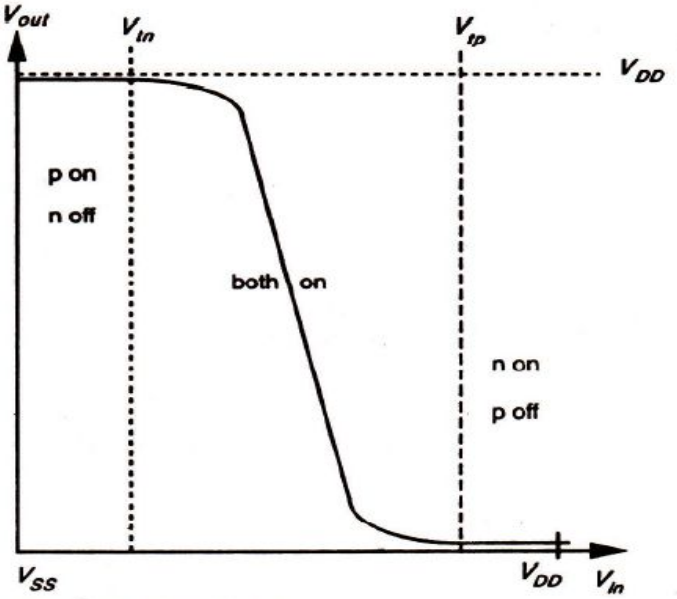


FIGURE 2.13 nMOS enhancement mode pull-up and transfer characteristic.

4. Complementary transistor pull up (CMOS)



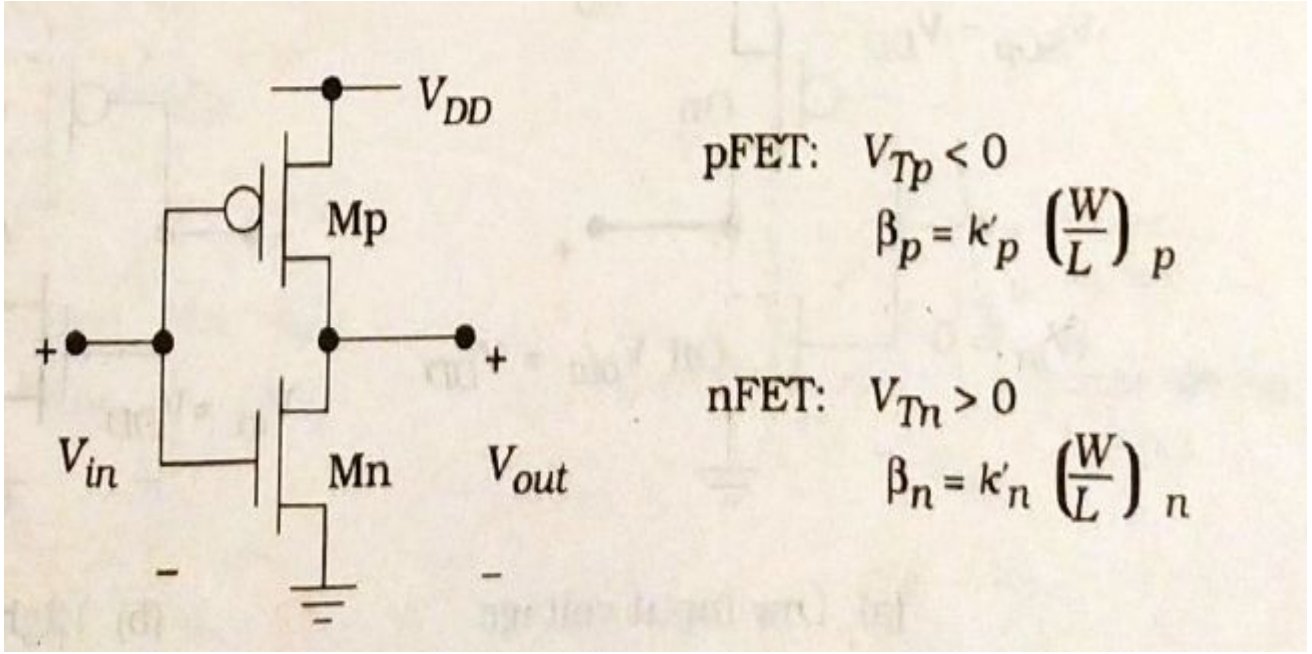
(a) Circuit



(b) Transfer characteristic

DC Characteristics of the CMOS Inverter

1. DC Analysis
2. Transient Analysis



Voltage Transfer Characteristics

VOH=VDD

VOL=0V

VL=VOH-VOL=VDD

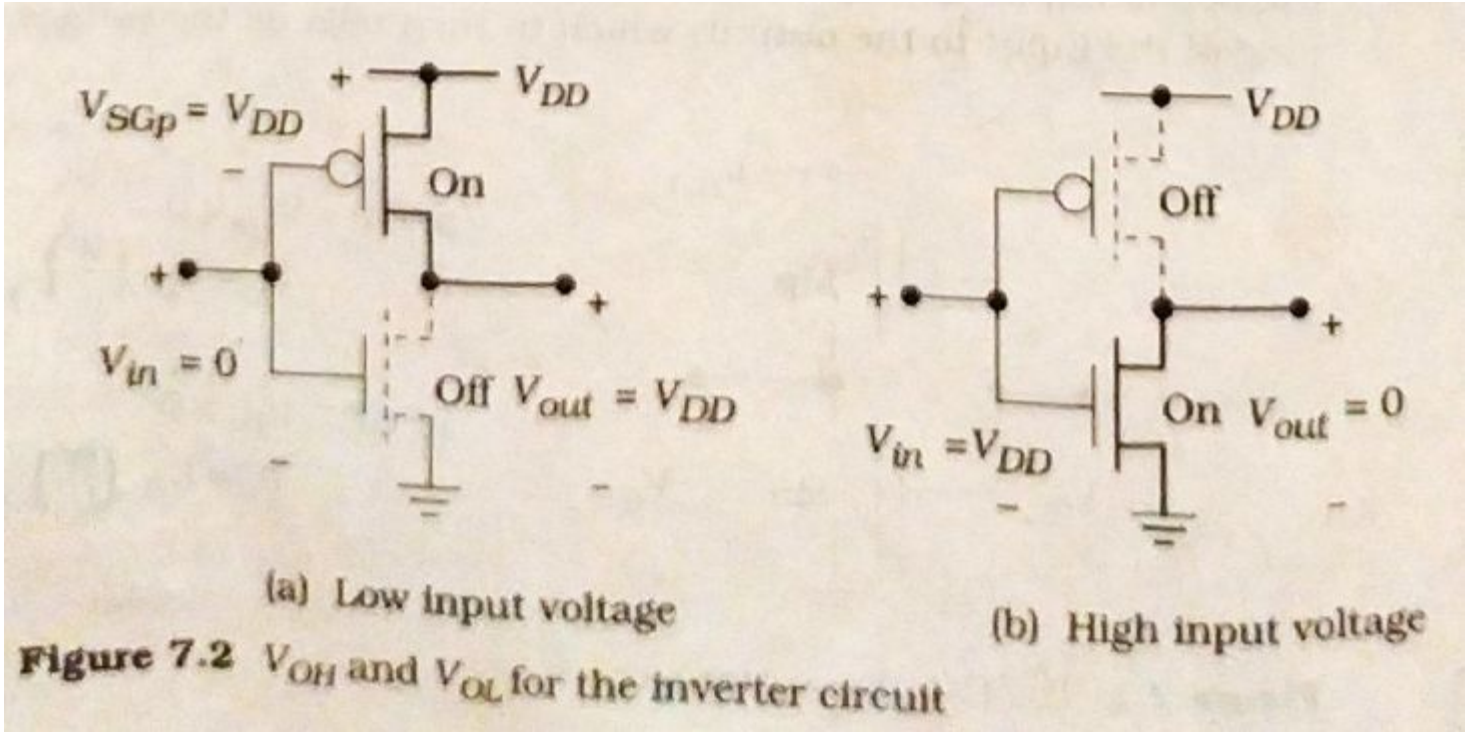


Figure 7.2 V_{OH} and V_{OL} for the inverter circuit

The VTC for the circuit is obtained by starting with an input voltage of Vin=0 and then increasing it up to the value of Vin=VDD

VGsn=Vin
VGsp=VDD-Vin

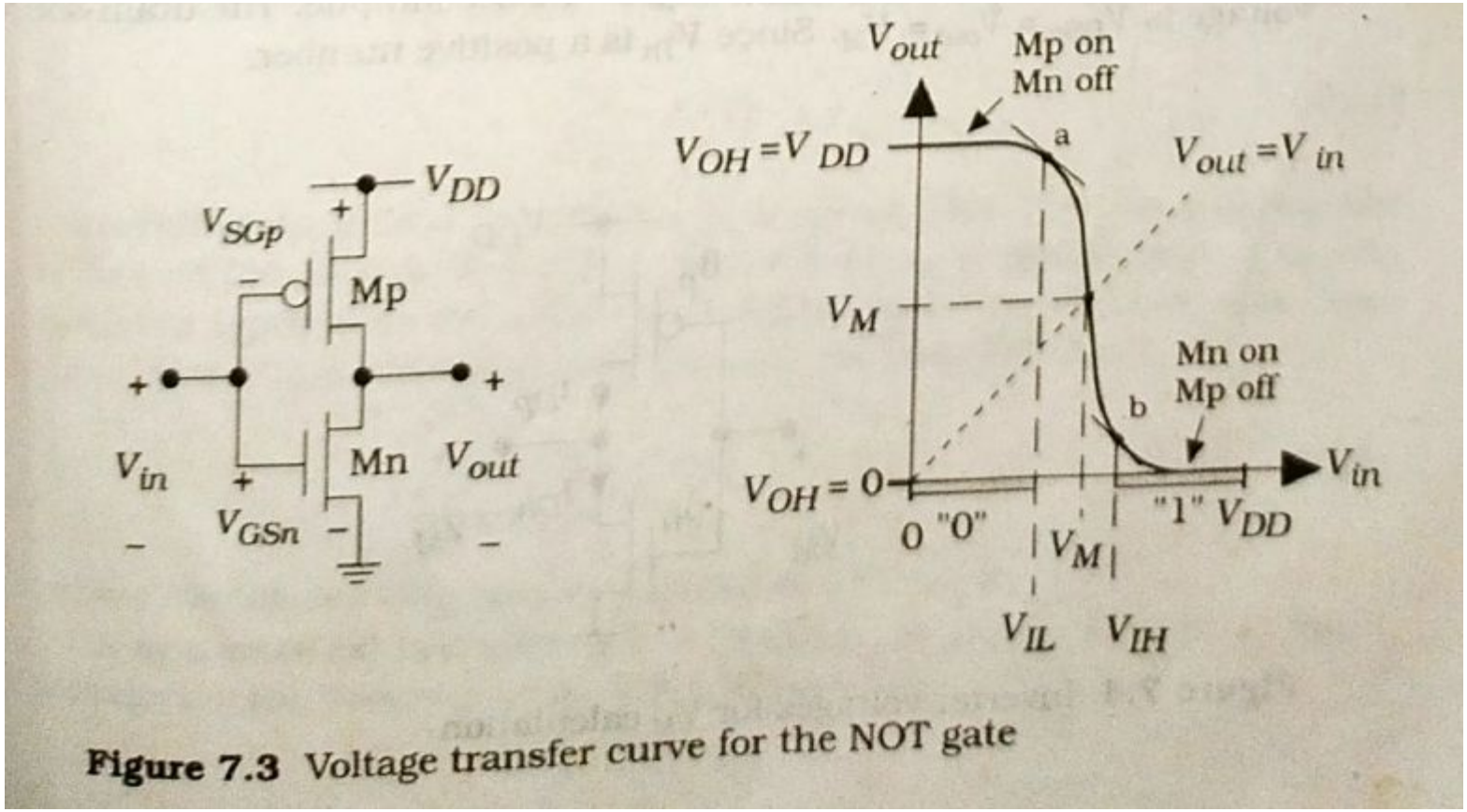


Figure 7.3 Voltage transfer curve for the NOT gate

Inverter Voltages for VM calculations

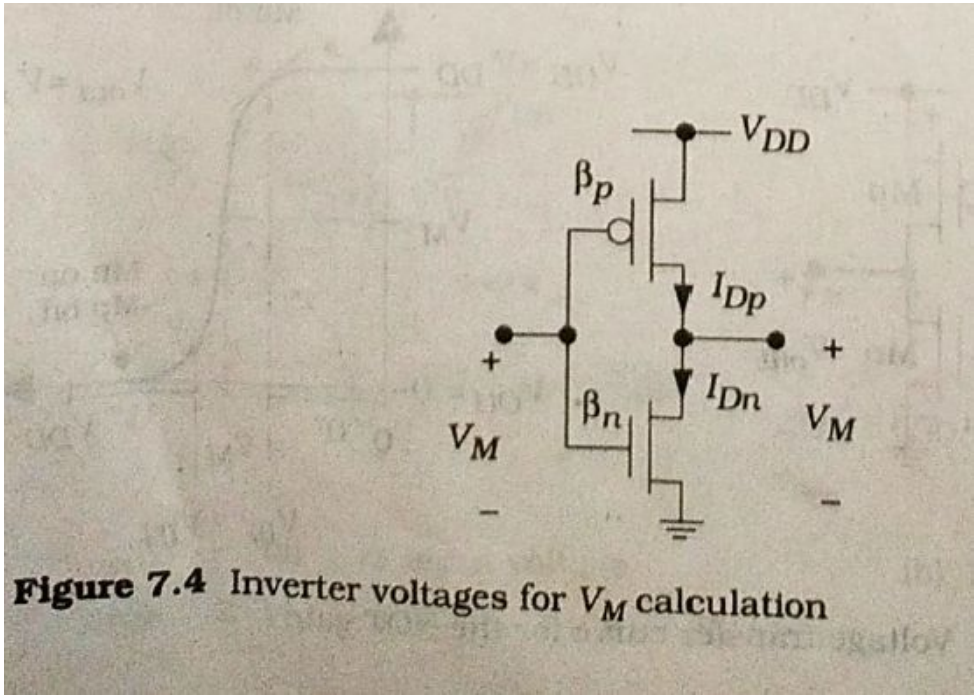


Figure 7.4 Inverter voltages for V_M calculation

To calculate the midpoint voltage we set $V_{in} = V_{out} = V_M$ as shown in Figure 7.4. Equating the drain currents of the FETs gives

$$I_{Dn} = I_{Dp} \tag{7.9}$$

but we need to find the operating region (saturation or non-saturation) of each FET before we can use the expression. Consider first the nFET and recall that the saturation voltage is given by

$$\begin{aligned} V_{sat} &= V_{GSn} - V_{Tn} \\ &= V_M - V_{Tn} \end{aligned} \tag{7.10}$$

where we have used $V_{in} = V_{GSn} = V_M$ in the second line. The drain-source voltage is $V_{DSn} = V_{out} = V_M$. Since V_{Tn} is a positive number,

$$V_{DSn} > V_{sat} = V_M - V_{Tn} \tag{7.11}$$

which says that Mn must be saturated. The same arguments can be applied to the pFET Mp since $V_{SGp} = V_{SDp}$. Using the saturation current equations from Chapter 6 gives

$$\frac{\beta_n}{2}(V_M - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \tag{7.12}$$

Dividing by β_p and taking the square root gives

$$\sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{Tn}) = V_{DD} - V_M - |V_{Tp}| \tag{7.13}$$

Simple algebra then gives the midpoint voltage as

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{7.14}$$

This equation shows that V_M is set by the nFET-to-pFET ratio

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p} \tag{7.15}$$

$$\frac{k'_n}{k'_p} \approx 2 \text{ to } 3 \tag{7.16}$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r \tag{7.17}$$

$$V_M = \frac{1}{2} V_{DD} \tag{7.18}$$

in equation (7.12). Rearranging gives us the design equation

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{1}{2} V_{DD} - |V_{Tp}|}{\frac{1}{2} V_{DD} - V_{Tn}} \right)^2 \tag{7.19}$$

This allows us to compute the transistor sizes for this particular choice of V_M. Note that if $V_{Tn} = |V_{Tp}|$, then a symmetric design requires that

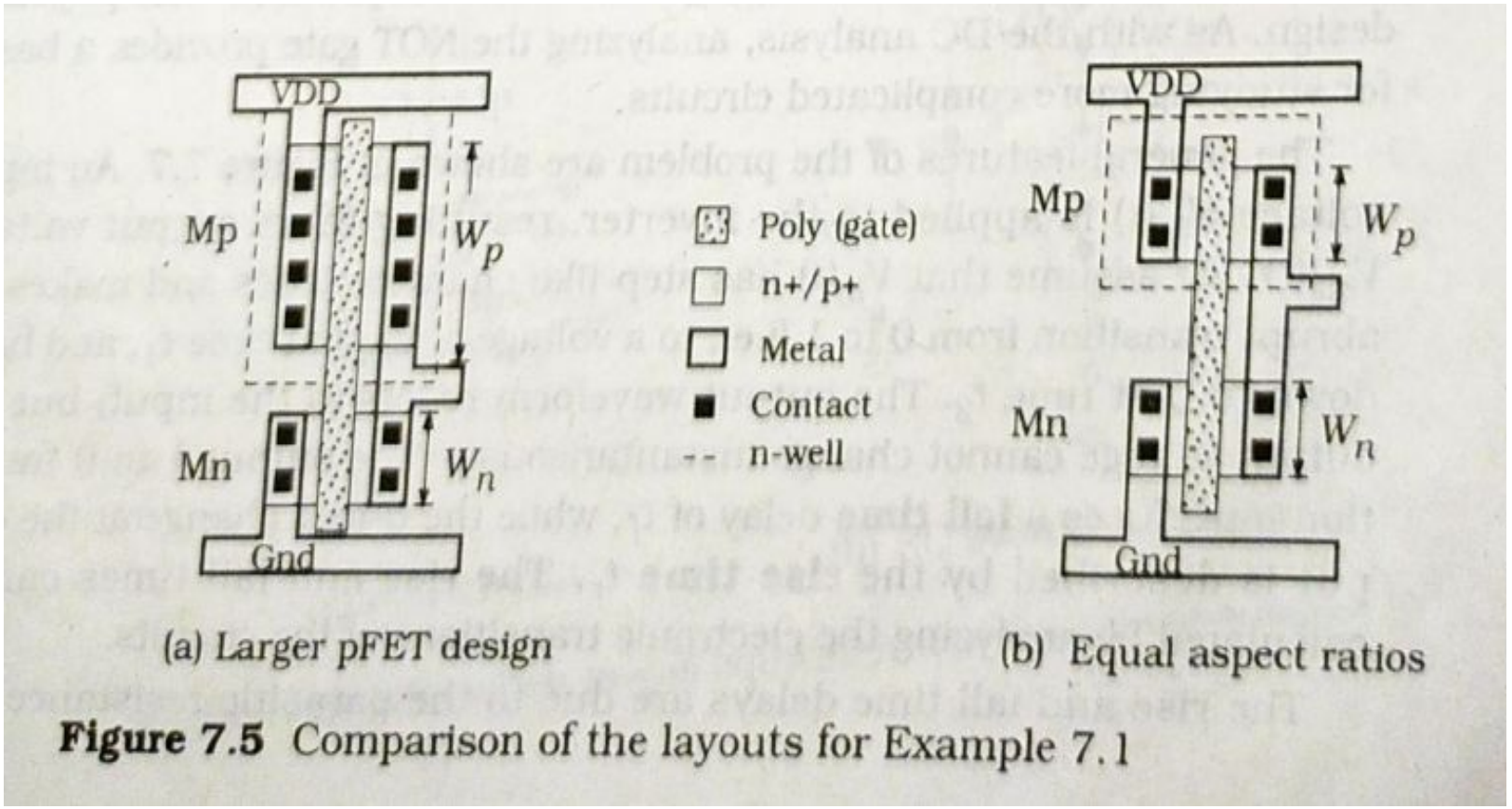
$$\beta_n = \beta_p \tag{7.20}$$

Consider a CMOS process with the following parameters

$$k'_n = 140\ \mu A/V^2 \qquad V_{Tn} = +0.70\ V$$
$$k'_p = 60\ \mu A/V^2 \qquad V_{Tp} = -0.70\ V \tag{7.21}$$

with $V_{DD} = 3.0$ V.

Consider the case where $\beta_n = \beta_p$. We can verify that this is a symmetrical design by calculating



(a) Larger pFET design

(b) Equal aspect ratios

Figure 7.5 Comparison of the layouts for Example 7.1

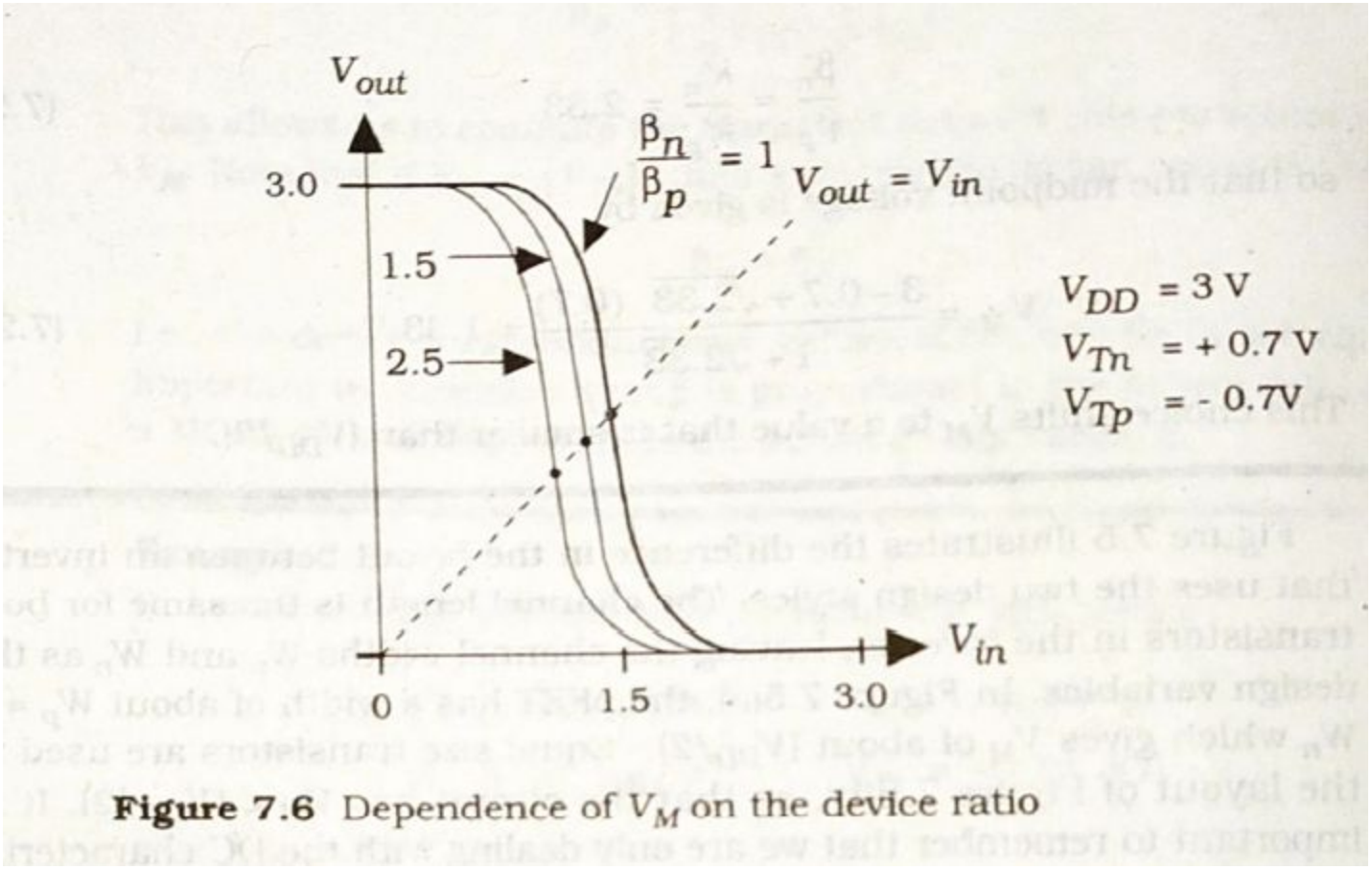


Figure 7.6 Dependence of V_M on the device ratio

Inverter Switching Characteristics

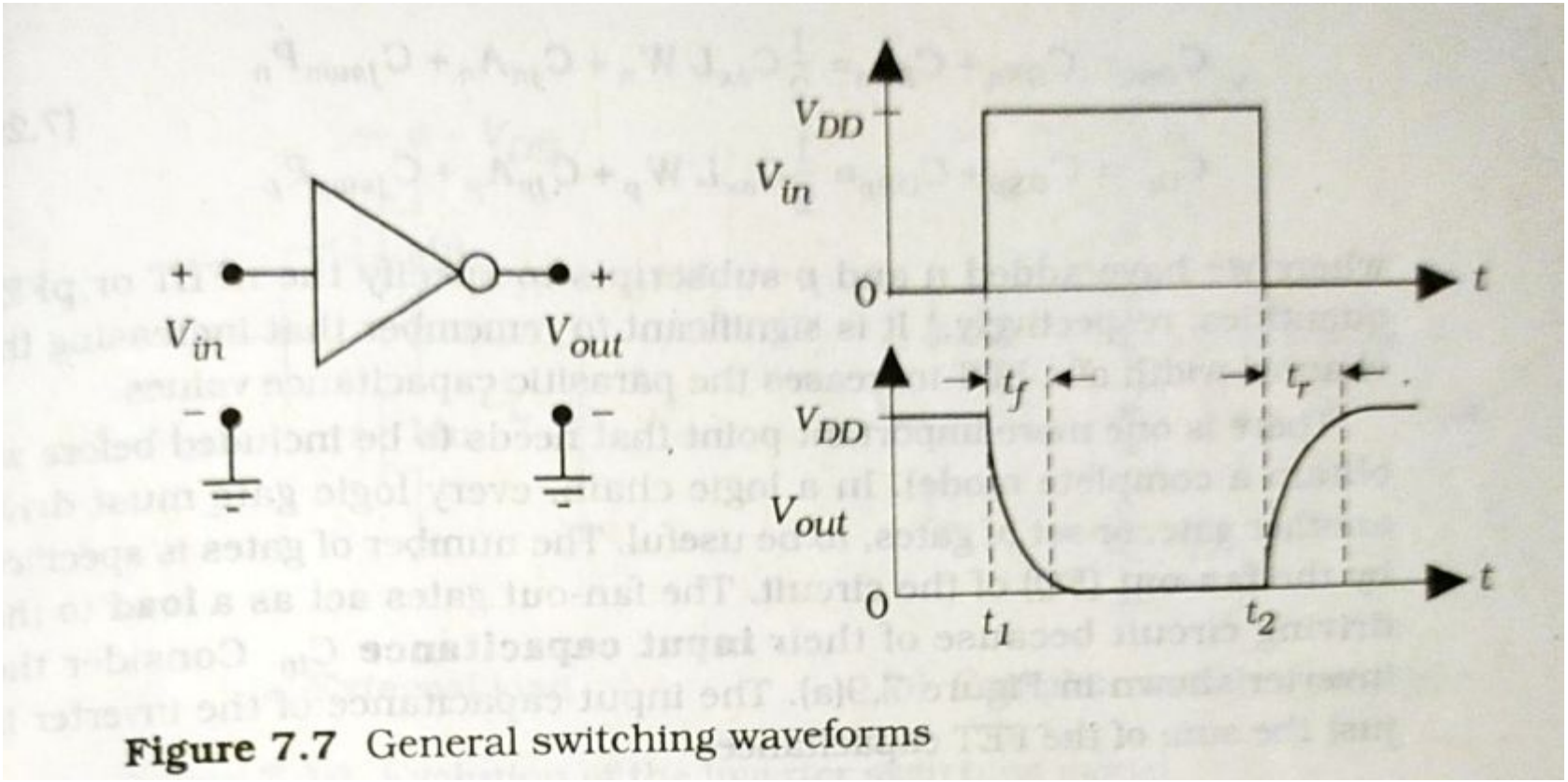
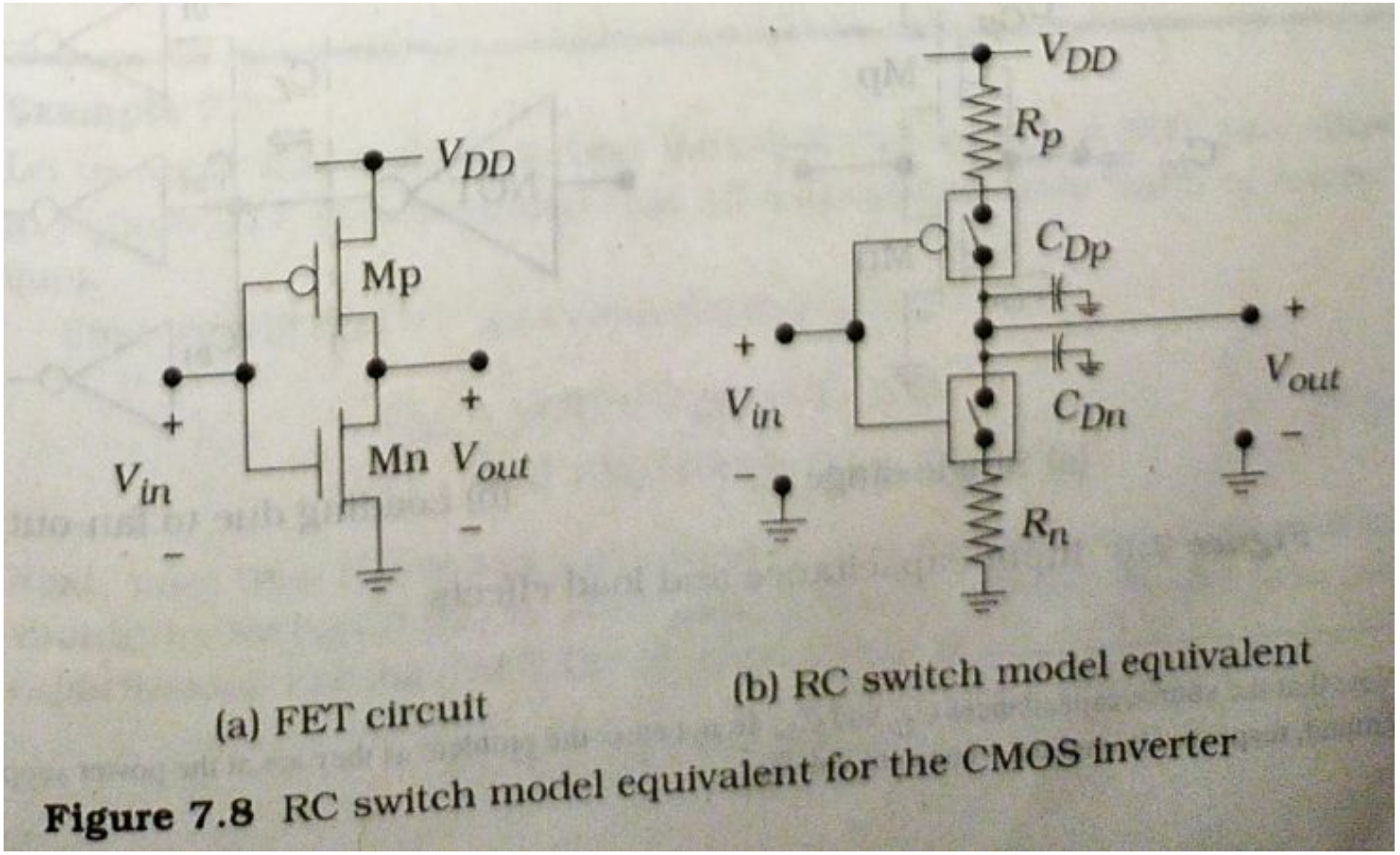


Figure 7.7 General switching waveforms



(a) FET circuit

(b) RC switch model equivalent

Figure 7.8 RC switch model equivalent for the CMOS inverter

Capacitance

$$C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n$$

$$C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_p + C_{jp} A_p + C_{jswp} P_p$$

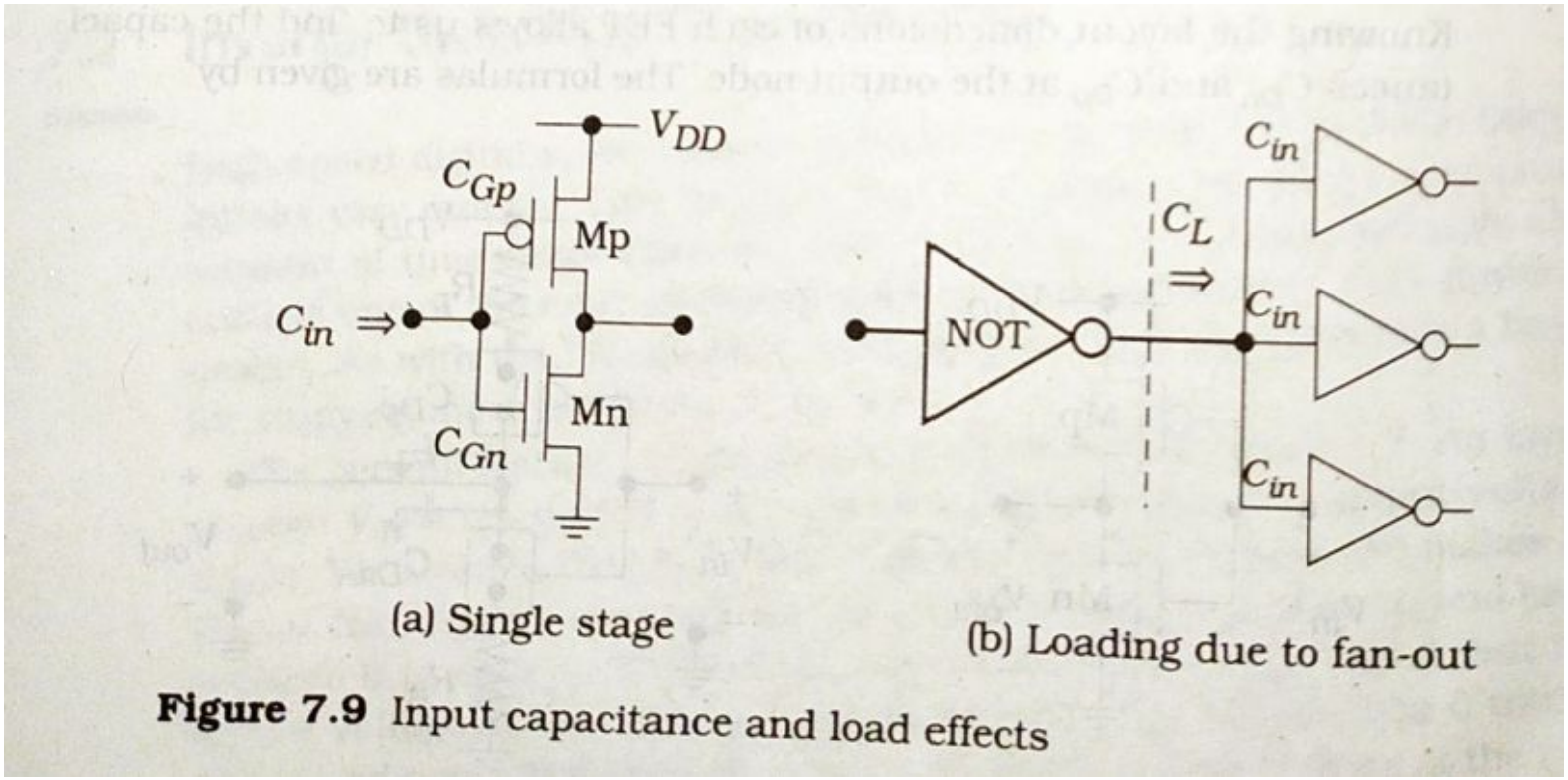
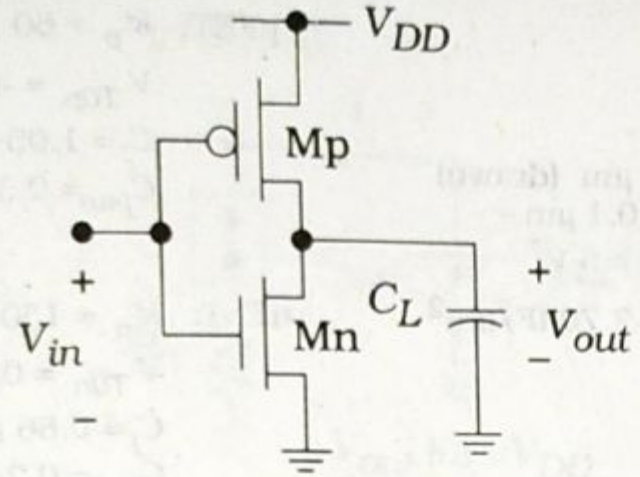
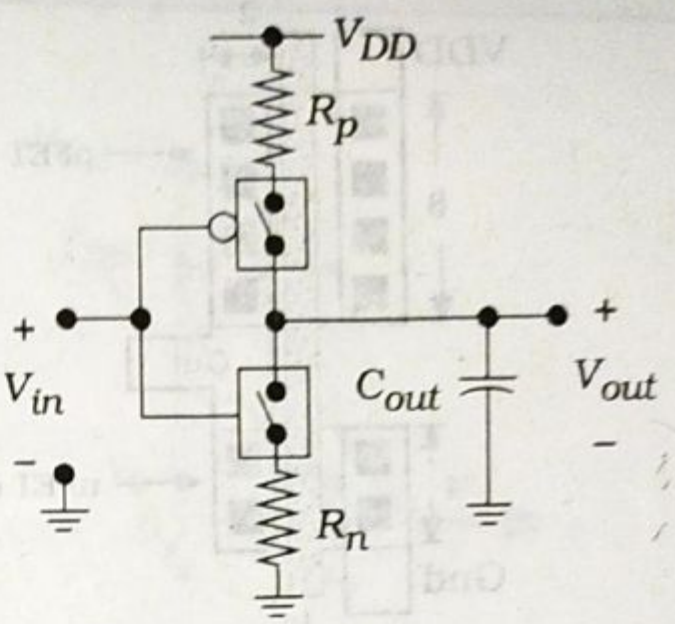


Figure 7.9 Input capacitance and load effects



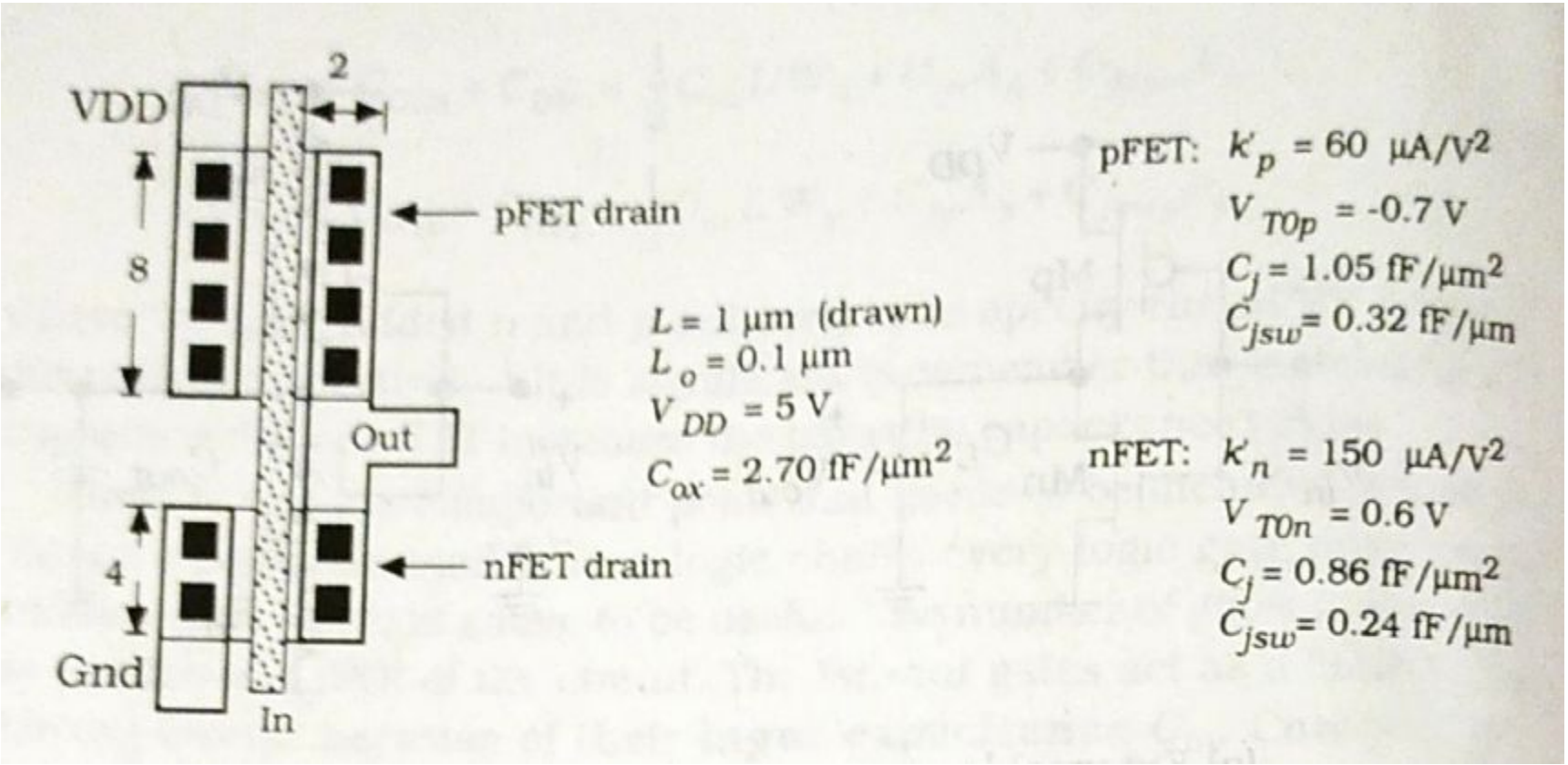
(a) External load



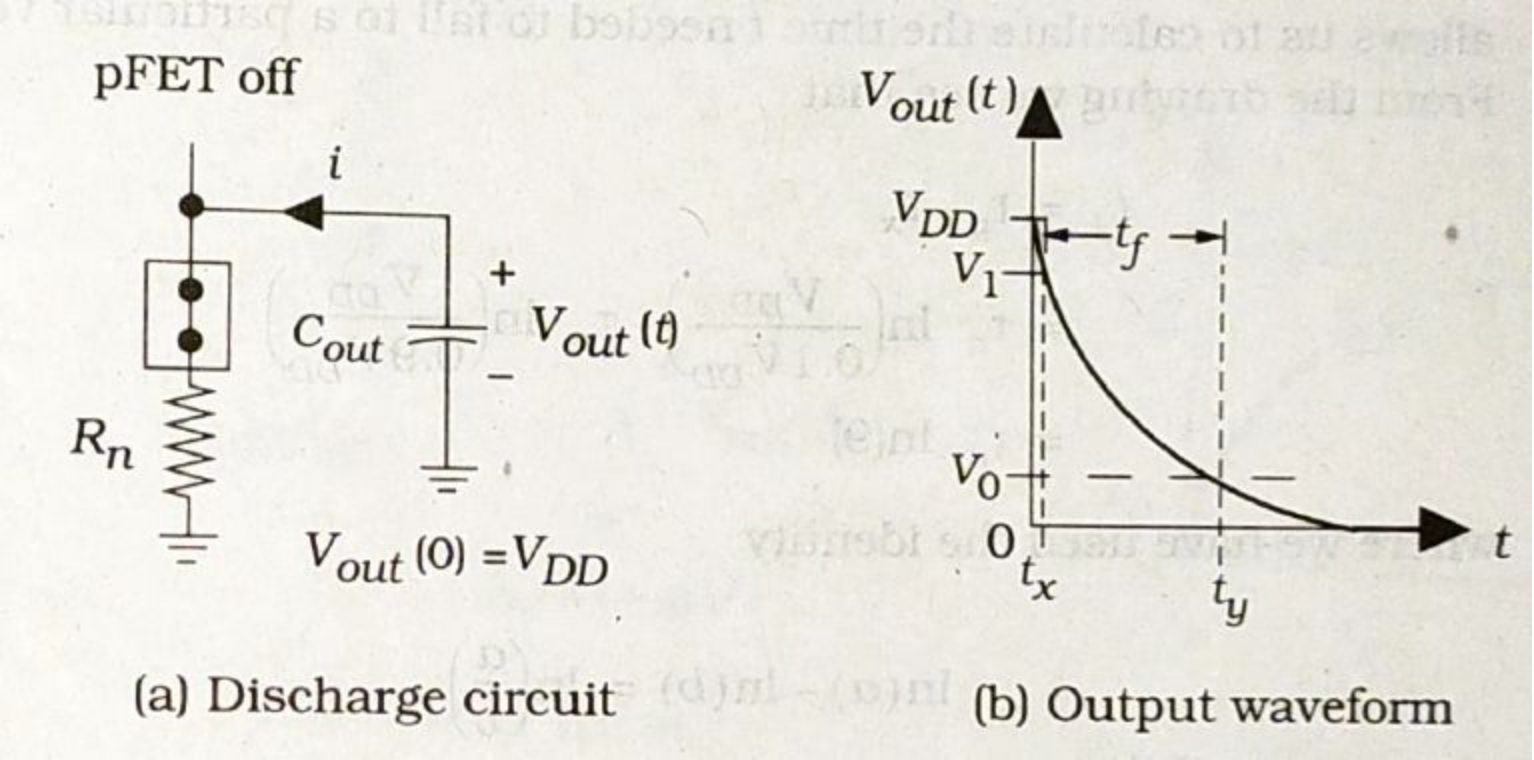
(b) Complete switching model

Figure 7.10 Evolution of the inverter switching model

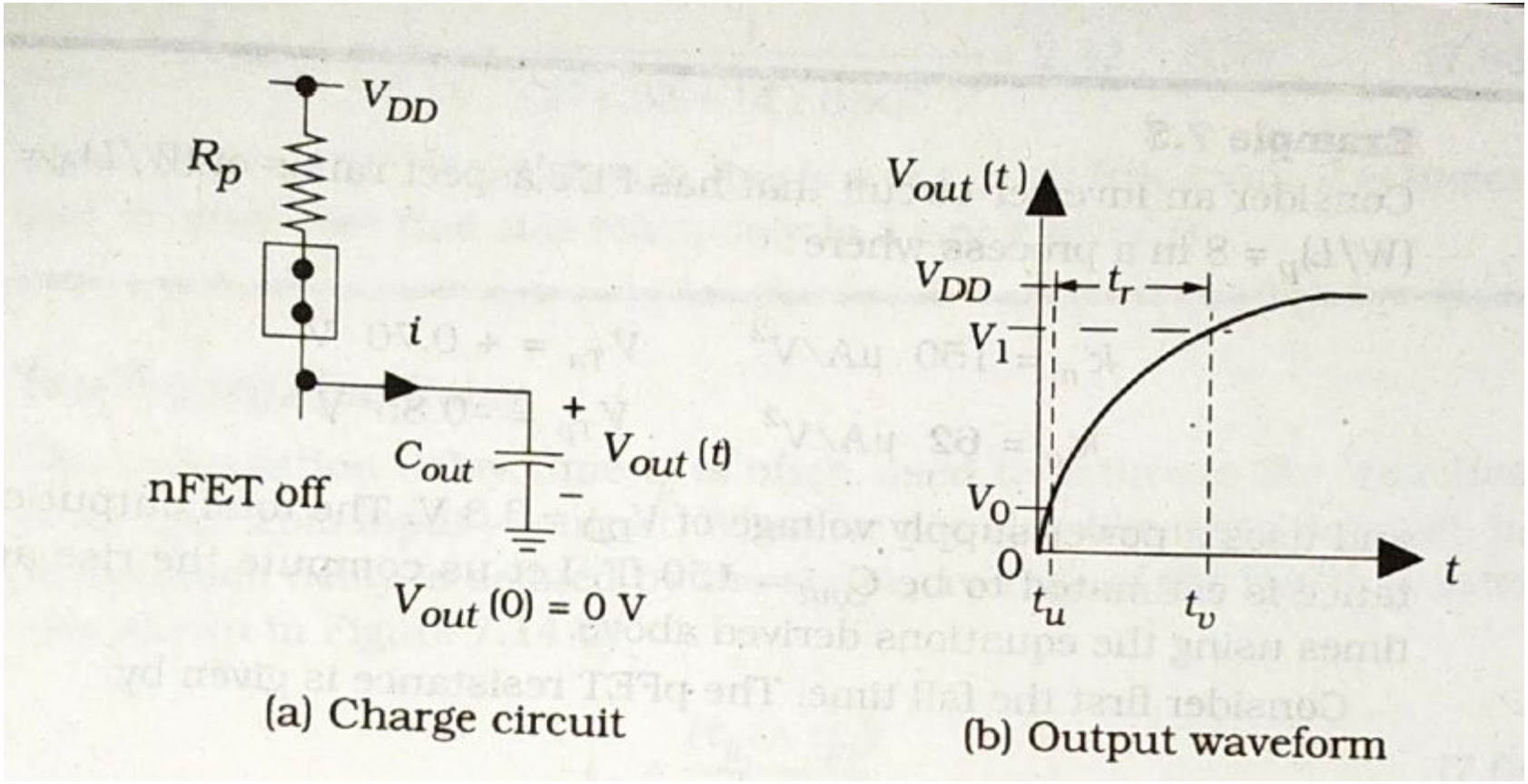
Example: Analysis to Find the Capacitances in the NOT gate



Fall Time Calculation



The Rise Time



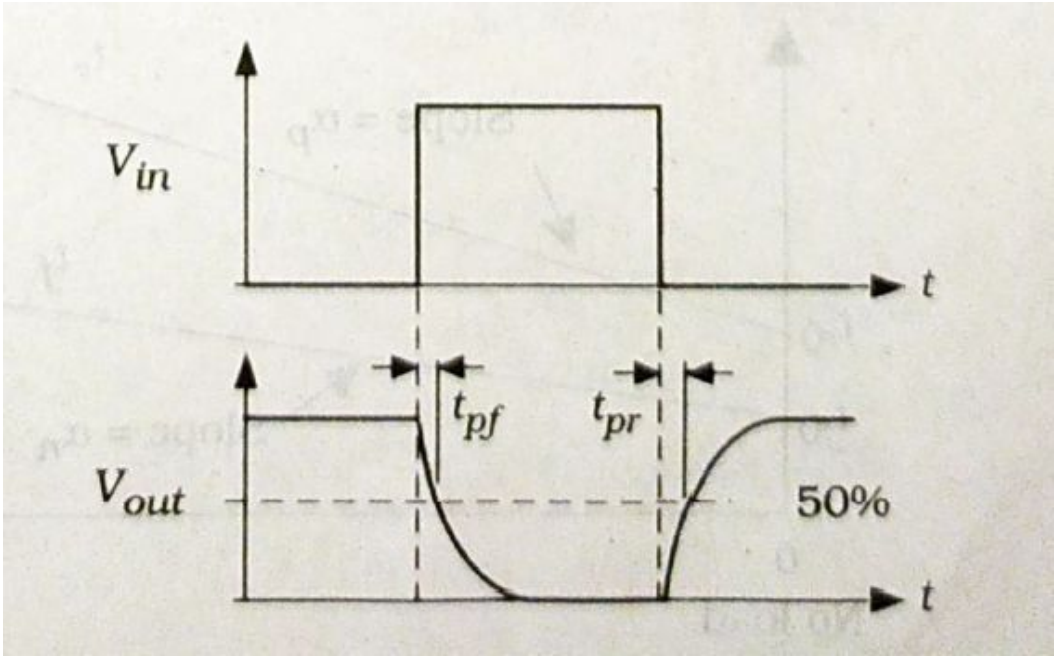
Example

Consider an inverter circuit that has FET aspect ratios of (W/L)n=6 and (W/L)p=8 in a process where

$$k'_n = 150\ \mu A/V^2 \qquad V_{Tn} = +0.70\ V$$
$$k'_p = 62\ \mu A/V^2 \qquad V_{Tp} = -0.85\ V$$

And uses a power supply voltage of VDD=3.3V. The total output capacitance is estimated to be Cout=150fF

The Propagation delay



General Analysis

The total output capacitance consist of two terms such as

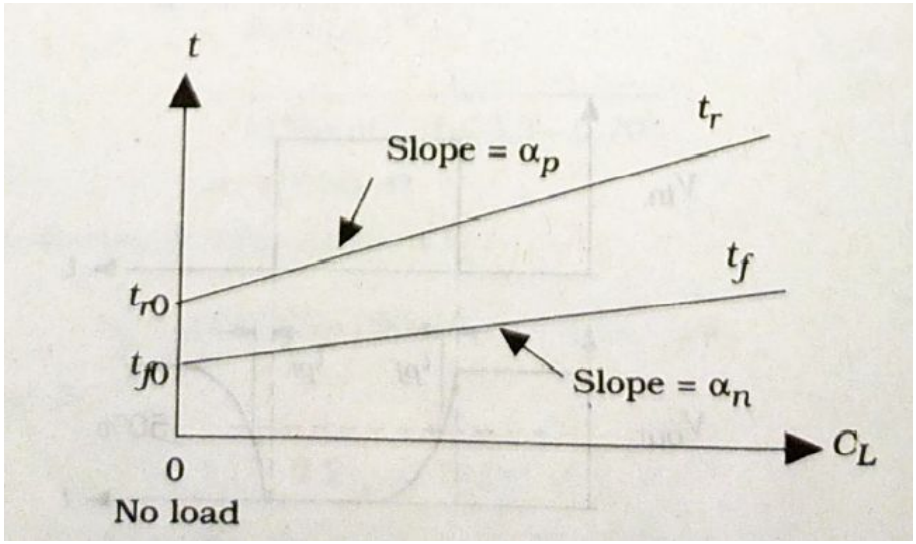
$$C_{out} = C_{FET} + C_L$$

Substituting this expression into the rise and fall time equations gives

$$t_r \approx 2.2R_p(C_{FET} + C_L)$$
$$t_f \approx 2.2R_n(C_{FET} + C_L)$$

Which can be cast into the forms

$$t_r = t_{r0} + \alpha_p C_L$$
$$t_f = t_{f0} + \alpha_n C_L$$



Under Zero-Load conditions(CL=0) the inverter drives its own capacitances such that

$$t_r = t_{r0} \approx 2.2 R_p C_{FET}$$
$$t_f = t_{f0} \approx 2.2 R_n C_{FET}$$

The dependence is described by the slope values

$$\alpha_p = 2.2 R_p = \frac{2.2}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$\alpha_n = 2.2 R_n = \frac{2.2}{\beta_n (V_{DD} - V_{Tn})}$$

Inversely proportional to the aspect ratios

$$\beta_p = k_p' \left(\frac{W}{L}\right)_p, \qquad \beta_n = k_n' \left(\frac{W}{L}\right)_n$$

Speed Versus Area Tradeoff

Example

Let us use the results of Example 7.3 to find the general delay equations for the case where the internal FET capacitance is $C_{FET} = 80$ fF.

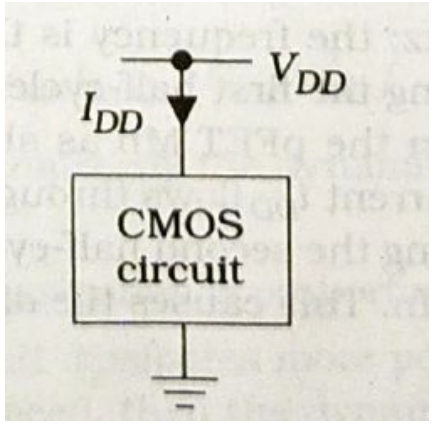
The rise time t_r is controlled by the pFET that has a resistance of $R_p = 822.9\ \Omega$. The slope is given by

Summary of the inverter circuit

The electrical characteristics of an isolated CMOS inverter are established by two sets of parameters

1. **The processing variables such as K and VT values and parasitic capacitances**
2. **The transistor aspects ratios (W/L)n and (W/L)p**

Power Dissipation



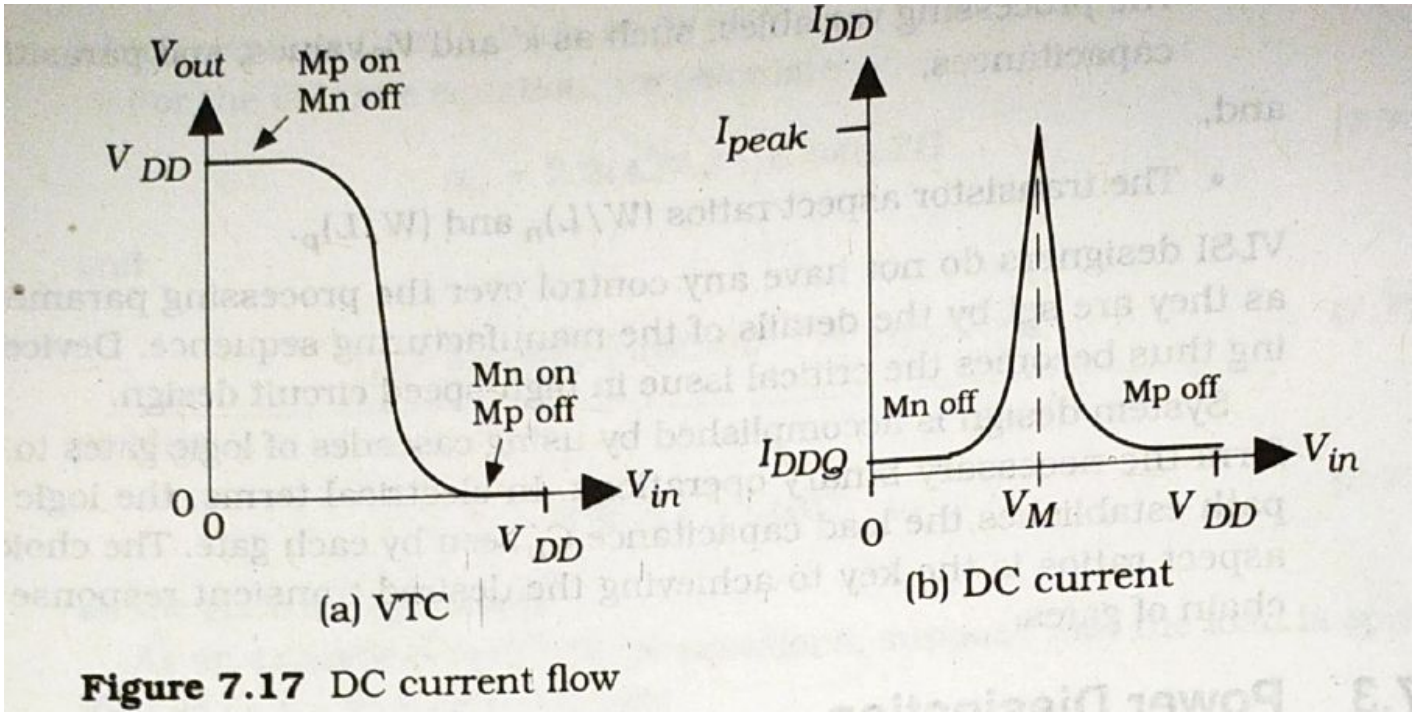
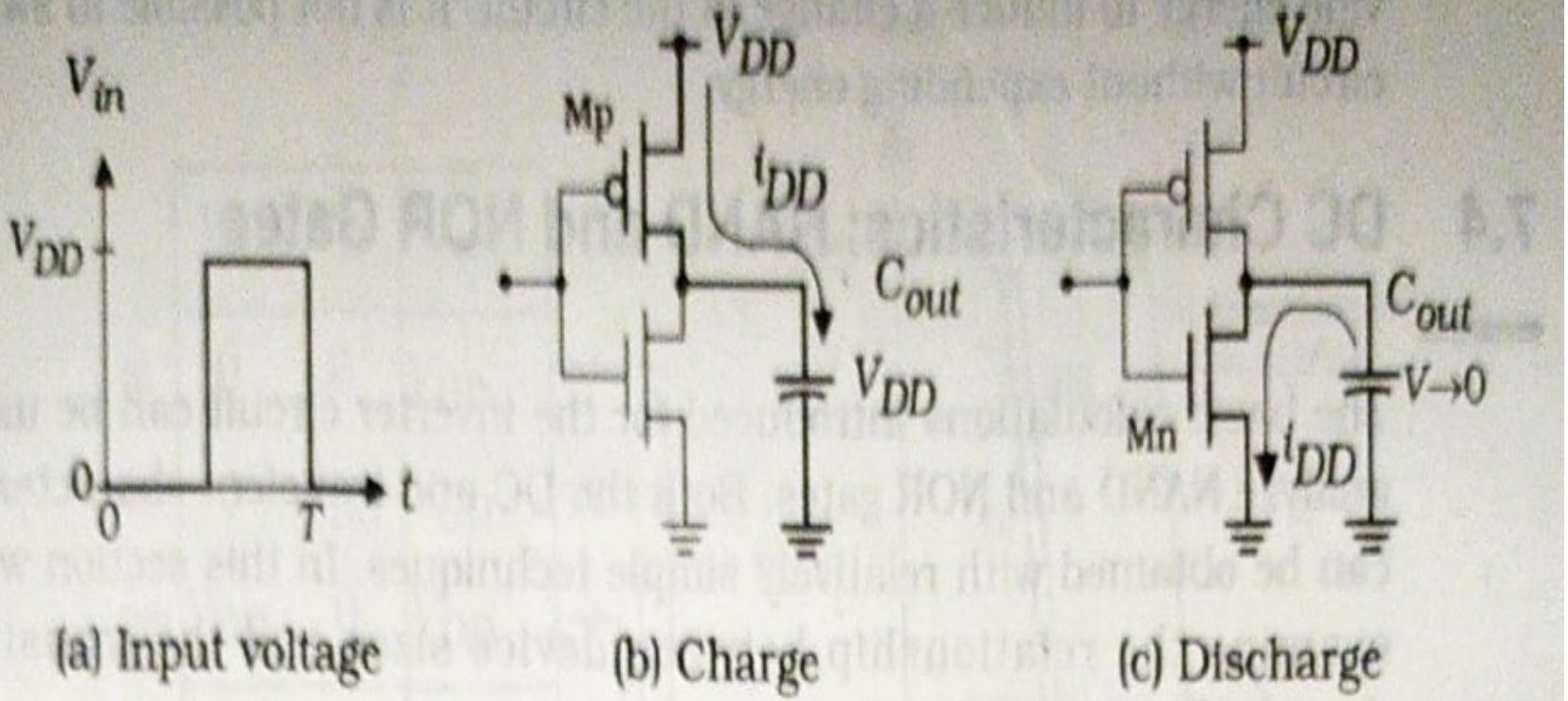


Figure 7.17 DC current flow



(a) Input voltage (b) Charge (c) Discharge

Figure 7.18 Circuit for finding the transient power dissipation