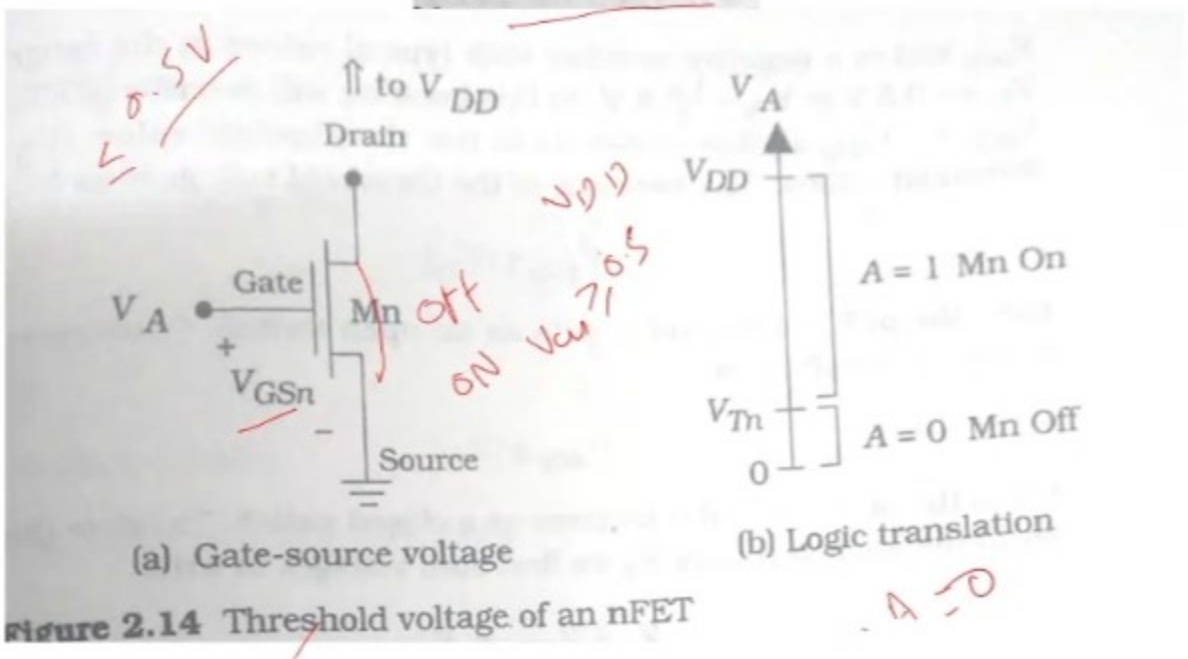
FET Threshold Voltages

nFET

V_{Tn} = 0.5 V to 0.7 V



(a) Gate-source voltage

(b) Logic translation

Figure 2.14 Threshold voltage of an nFET

Open Switch

$V_{GSn} \leq V_{Tn}$

Closed Switch

$V_{GSn} \geq V_{Tn}$

A=0

$V_A = V_{GSn}$ $V_A \leq V_{Tn}$

A=1

$V_A \geq V_{Tn}$

Pass Characteristics

nFET

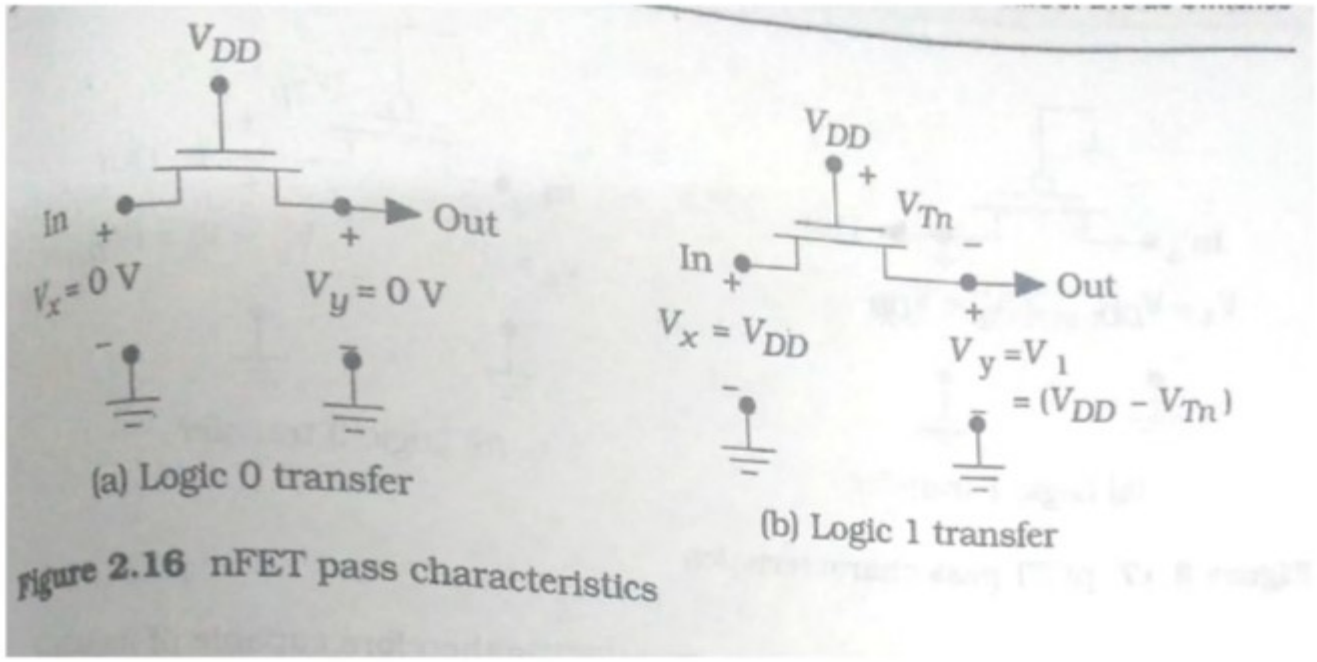


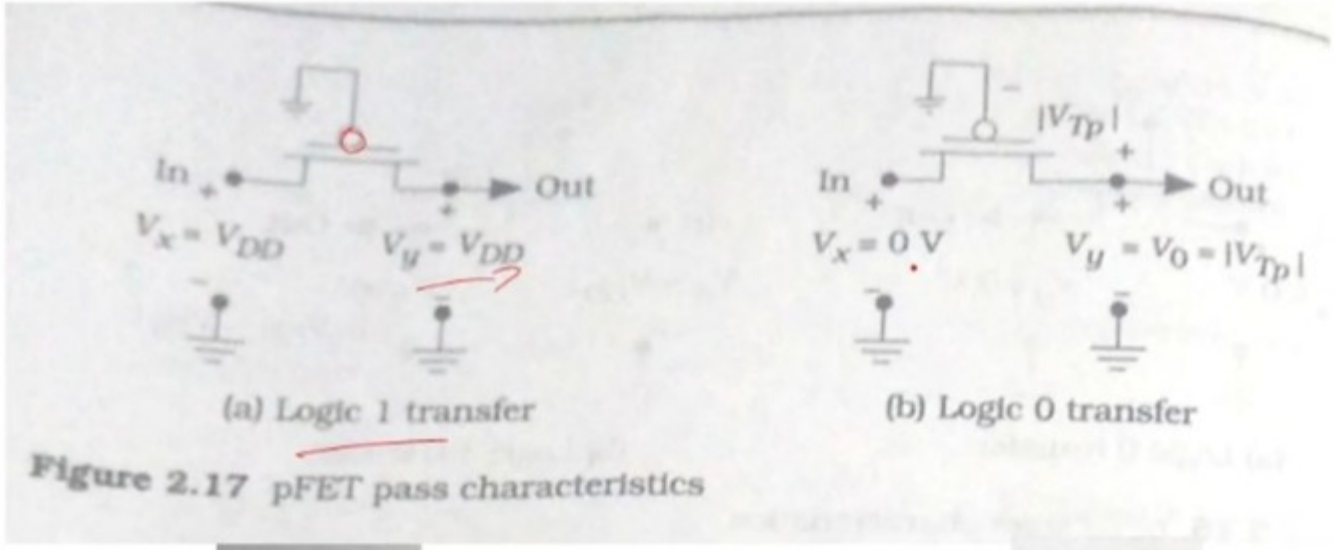
Figure 2.16 nFET pass characteristics

Threshold Voltage Loss

$$V_1 = V_{DD} - V_{Tn}$$

nFET can pass Weak logic 1 and strong logic 0

pFET



(a) Logic 1 transfer

(b) Logic 0 transfer

Figure 2.17 pFET pass characteristics

$V_y = V_{DD}$

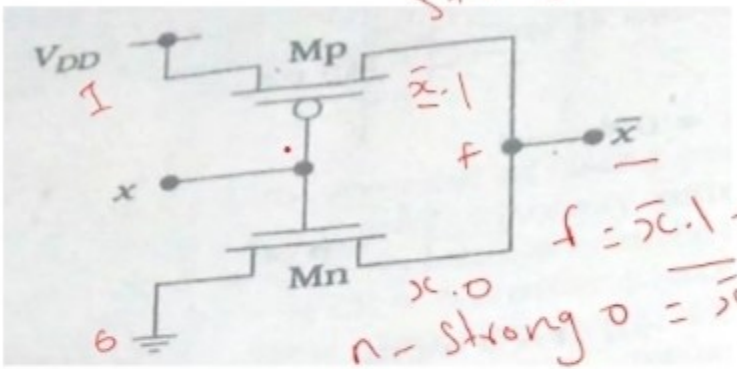
$V_y = |V_{Tp}|$

pFET can pass Weak logic 0 and strong logic 1

CMOS circuits are designed to account for the transmission levels.
The following rules are the basis for our design

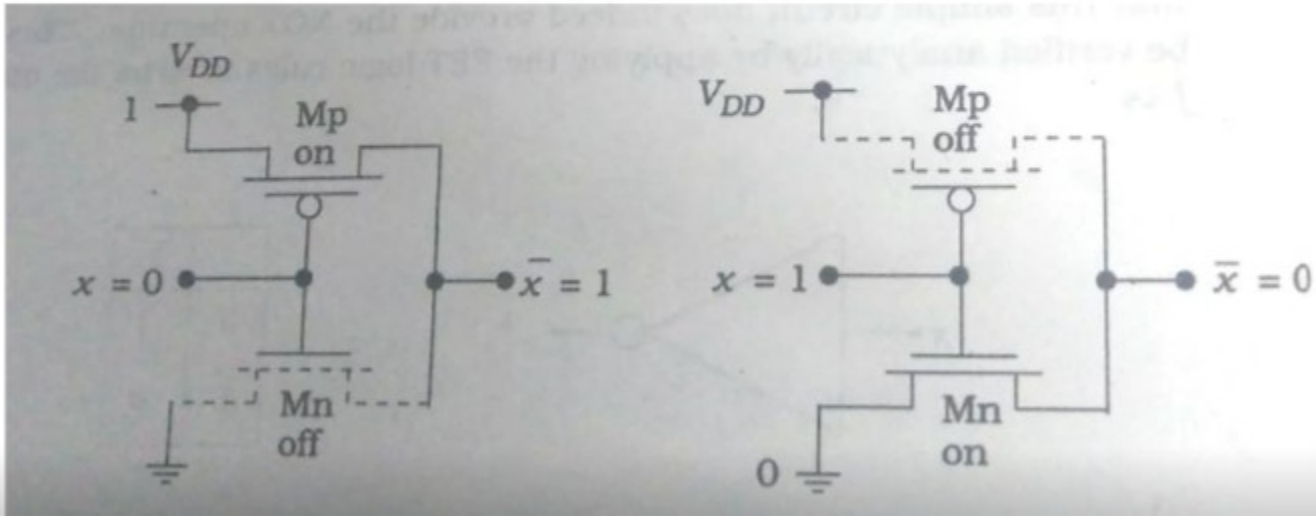
1. Use pFETs to pass logic 1 voltages of VDD
2. Use nFETs to pass logic 0 voltages of VSS=0V

CMOS NOT Gate



$f = \bar{x}\cdot 1 + x\cdot 0$

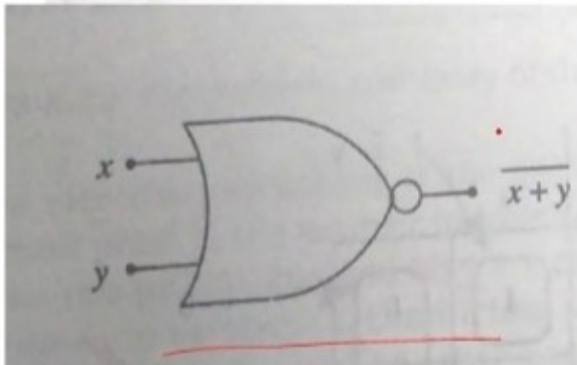
$f = \bar{x}$



CMOS NOR Gate

$g(x, y) = \overline{x+y}$

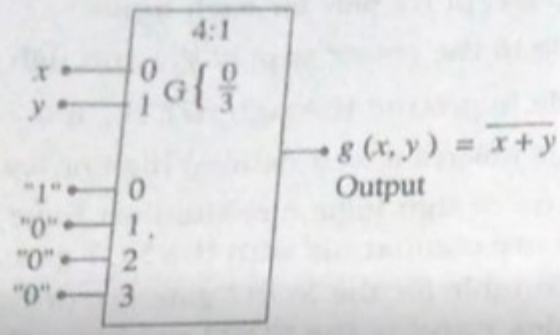
$g(x, y) = \bar{x} \cdot \bar{y} \cdot 1 + \bar{x} \cdot y \cdot 0 + x \cdot \bar{y} \cdot 0 + x \cdot y \cdot 0$



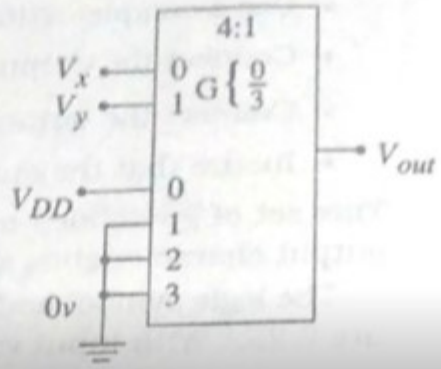
(a) Logic symbol

x	y	$\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table

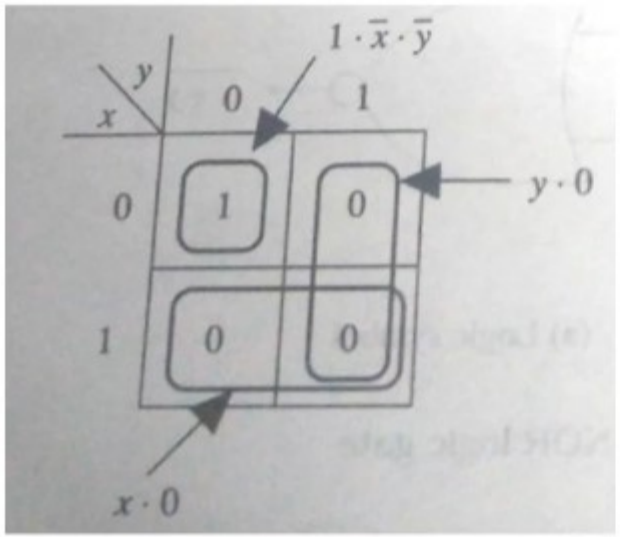


(a) Logic diagram



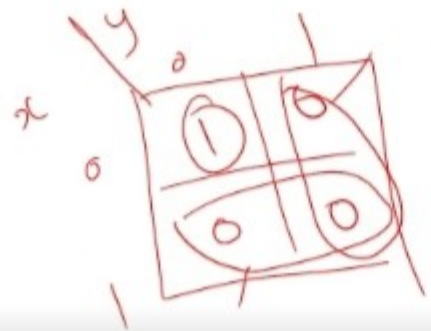
(b) Voltage network

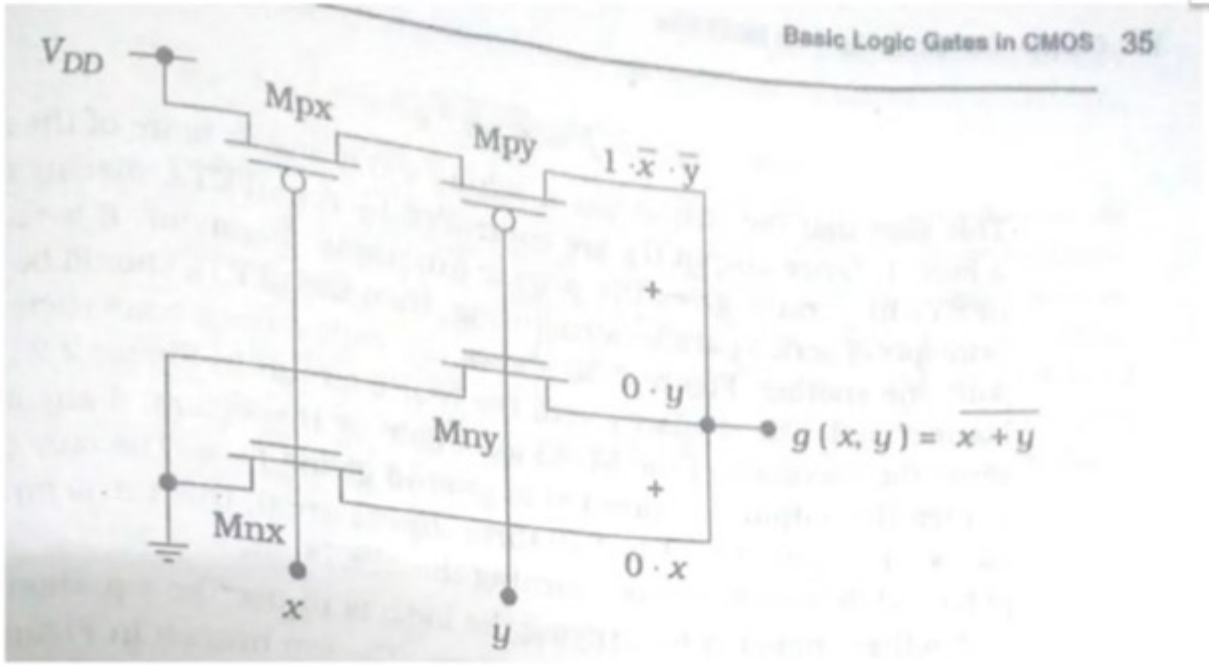
NOR2 Operation



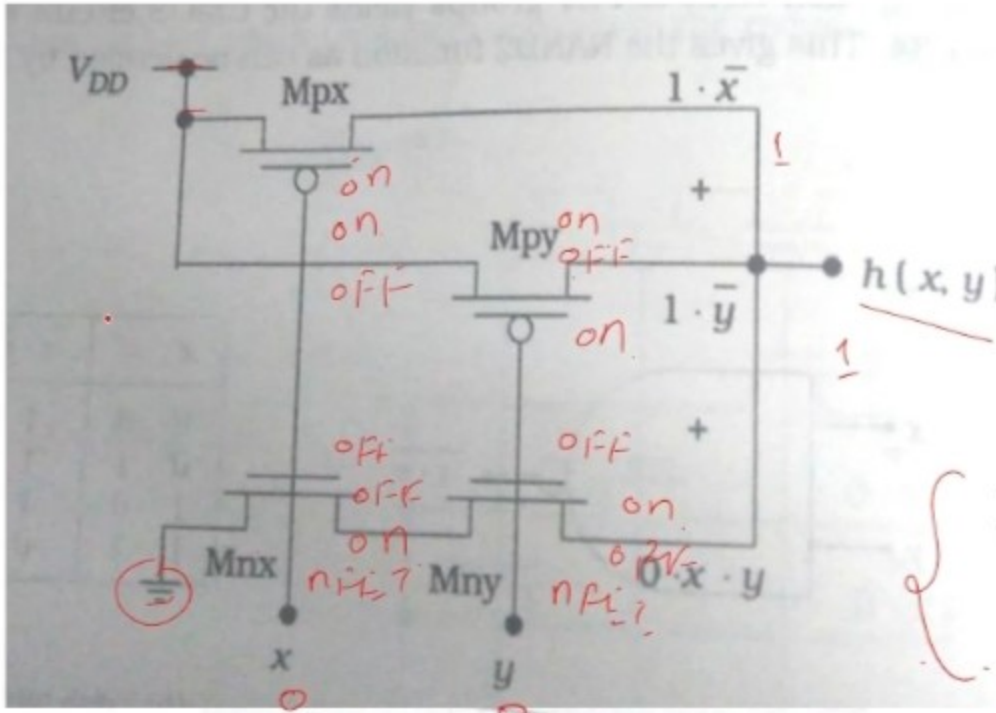
$$g(x, y) = \bar{x} \cdot \bar{y} \cdot 1 + x \cdot 0 + y \cdot 0$$

$$g = \bar{x} \cdot \bar{y} \cdot 1 + x \cdot 0 + y \cdot 0$$





x	y	Mpx	Mpy	Mnx	Mny	g
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0



x	y	Mpx	Mpy	Mnx	Mny	h
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0