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Department of Electronics & Communication Engg.
Continuous Internal Evaluation – II

Course Name : FOVLSI		Date :	9/7/2019
Course Code : 18EC6DCFOV		Day :	Friday
Semester : 6th		Timings :	11.15-12.45
Max Marks : 50		Duration :	1½ Hrs.

No.		Question Description	M	CO &BL
Q1	(a)	The full adder circuit can be constructed using i. Two half adders and one NAND gate iii.Two half adders and one NOR gate ii. Two half adders and one OR gate iv.Two half adders and one AND gate	1	
	(b)	Carry generator expression in full adder is------ i.G=AB ii.G=A+B iii.G=A-B iv.G=A\B	1	
	(c)	…….. no. of transistors are needed to construct full adder using transmission gates. i.32 ii.24 iii.24 iv.28	1	
	(d)	Funnel shifter performs i. Arithmetic shift only iii. Arithmetic, Logical Shift and Rotate operation ii. Rotate & Arithmetic shift operation iv. Logical shift & Rotate operation	1	
	(e)	Pseudo nMOS NOR structure can be used to detect i. All ones ii. All zeros iii. All ones and all zeros iv. None of the above	1	
	(f)	Which of the following memory technology is highly denser? i. DRAM ii. SRAM iii. EPROM iv. Flash memory	1	
	(g)	A RAM is i. Non- volatile memory ii. Volatile memory ii. Static and dynamic memory iv. None of the above	1	
	(h)	Which of the following memories can be programmed once by the user and cannot be erased and reprogrammed? i. EPROM iii. EEPROM iii. ROM iv.PROM	1	
	(i)	Critical path delay of carry select adder is …… i. a.$t_{select}=t_{pg}+[n+(k-2)]t_{A0}+t_{mux}$ iii. $t_{select}=t_{pg}+[n+(k-1)]2t_{A0}+t_{mux}$ ii. c. $t_{select}=t_{pg}+[n+(k-4)]t_{A0}+t_{mux}$ iv. d $t_{select}=t_{pg}+[n+(k-6)]t_{A0}+t_{mux}$	1	
	(j)	Data after LSL1 for 1011 is i. 0101 ii. 0110 iii. 1011 iv. 1010	1	
Q2	(a)	Discuss the implementation of transmission gate full adder	6	CO3,L 4
	b)	Design the Manchester carry chain using transmission gate and pass transistor logic. Explain the same	4	CO3,L 3
Q3	(a)	Describe the read/write operation of 6T SRAM cell with schematic and suitable waveform.	10	CO4,L 2

Q4	(a)	Show the construction of unsigned magnitude comparator using ripple carry adder and explain the same.	05	CO4,L 3
	(b)	Elaborate the working of array funnel shifter	05	CO4,L 2
		OR		
Q5	(a)	b) Realize Y=A+BC using Domino CMOS logic and Clocked CMOS Logic	06	CO3, L2
	(b)	Show the implementation of sum output of full adder using CPL and mention its advantages.	04	CO3,L 3
Q6	(a)	Implement a 4 bit carry ripple adder using PG logic and discuss the operating principle.	06	CO3, L2
	(b)	Explain Basic Dynamic CMOS gate .	04	CO3,L 2
		OR		
Q7	(a)	Discuss the different bit line conditioning circuits used in SRAM.	06	CO4, L2
	(b)	Draw the circuit of one/zero detectors using AND/ NOR gates.	04	CO4,L 2