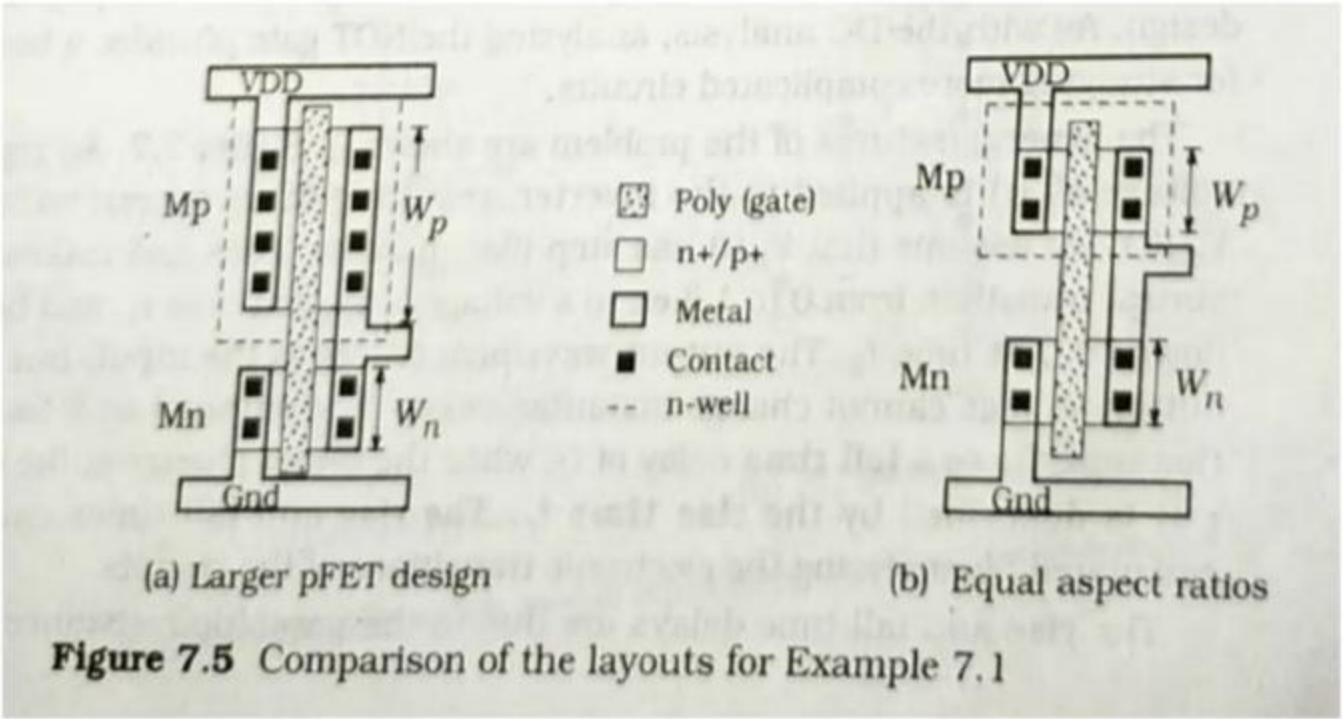


(a) Larger pFET design

(b) Equal aspect ratios

Figure 7.5 Comparison of the layouts for Example 7.1

Consider a CMOS process with the following parameters

$$k'_n = 140\ \mu A/V^2 \qquad V_{Tn} = +0.70\ V$$
$$k'_p = 60\ \mu A/V^2 \qquad V_{Tp} = -0.70\ V \tag{7.21}$$

with $V_{DD} = 3.0$ V.

Consider the case where $\beta_n = \beta_p$. We can verify that this is a symmetrical design by calculating

$\left(\frac{W}{L}\right)_p = 2.33\left(\frac{W}{L}\right)_n$

PFET = 2.33 NFET

$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n$

$V_M = \frac{1}{2}V_{DD}$ $\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p}$

$1 = \frac{140\times10^{-6}\left(W/L\right)_n}{60\times10^{-6}\left(W/L\right)_p}$

$= 2.33\cdot\frac{(W/L)_n}{(W/L)_p}$

$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$

Inverter Switching Characteristics

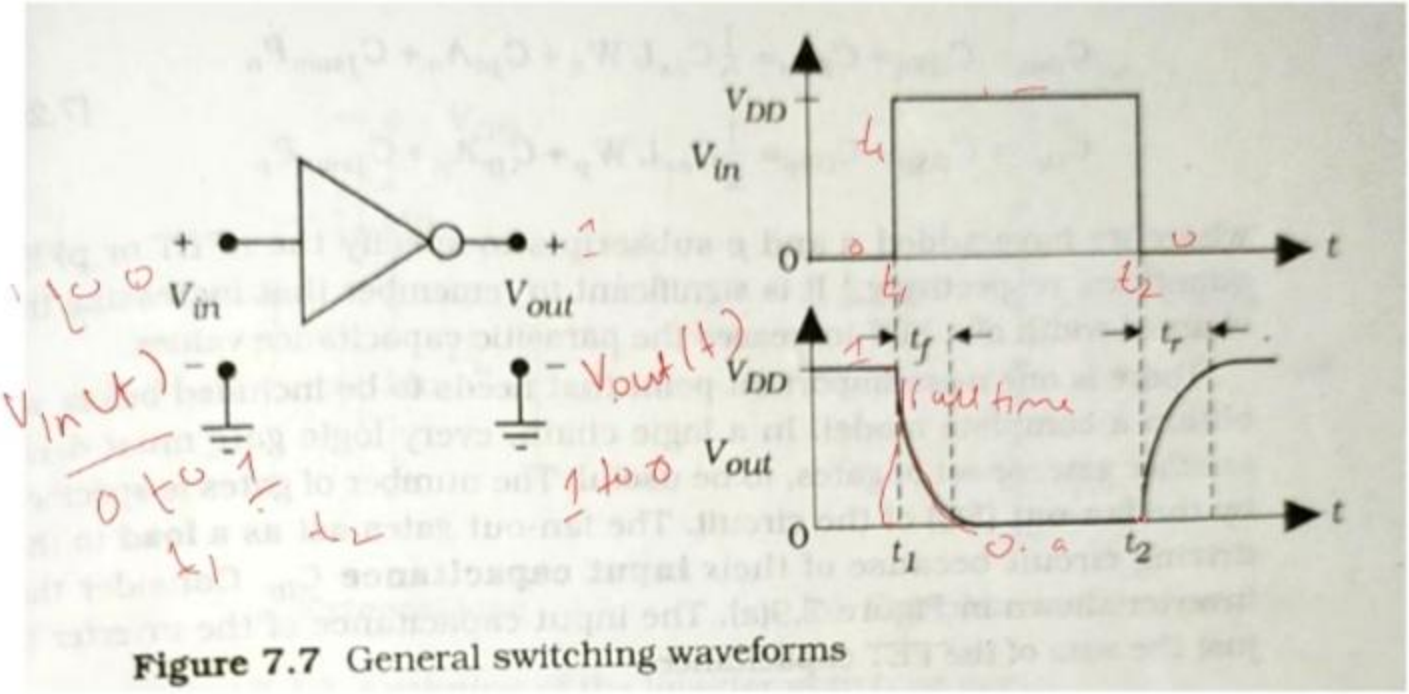
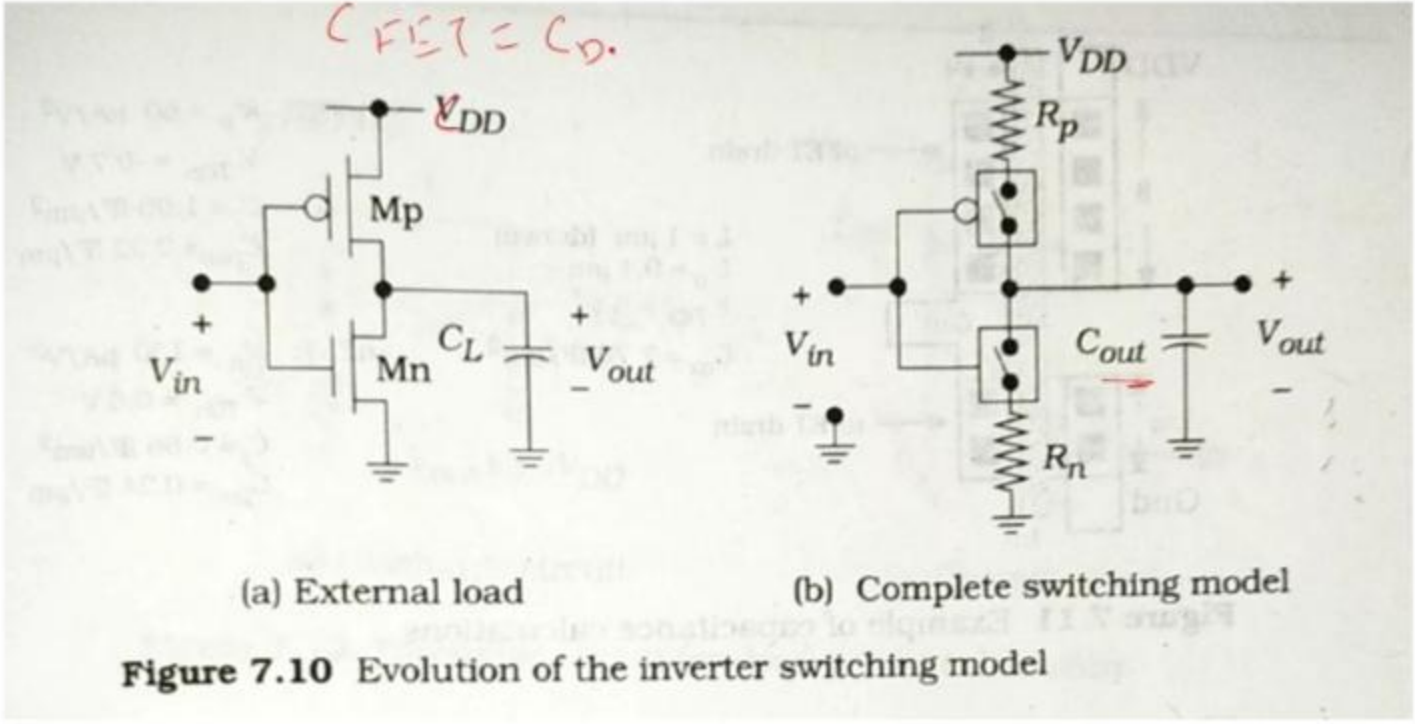


Figure 7.7 General switching waveforms

$C_L = 3C_{in}$ $C_{out} = C_{FET} + C_L$

$C_{FET} = C_D$.



(a) External load (b) Complete switching model

Figure 7.10 Evolution of the inverter switching model