Figure 12.8 *Space/time model of the collision in CSMA*

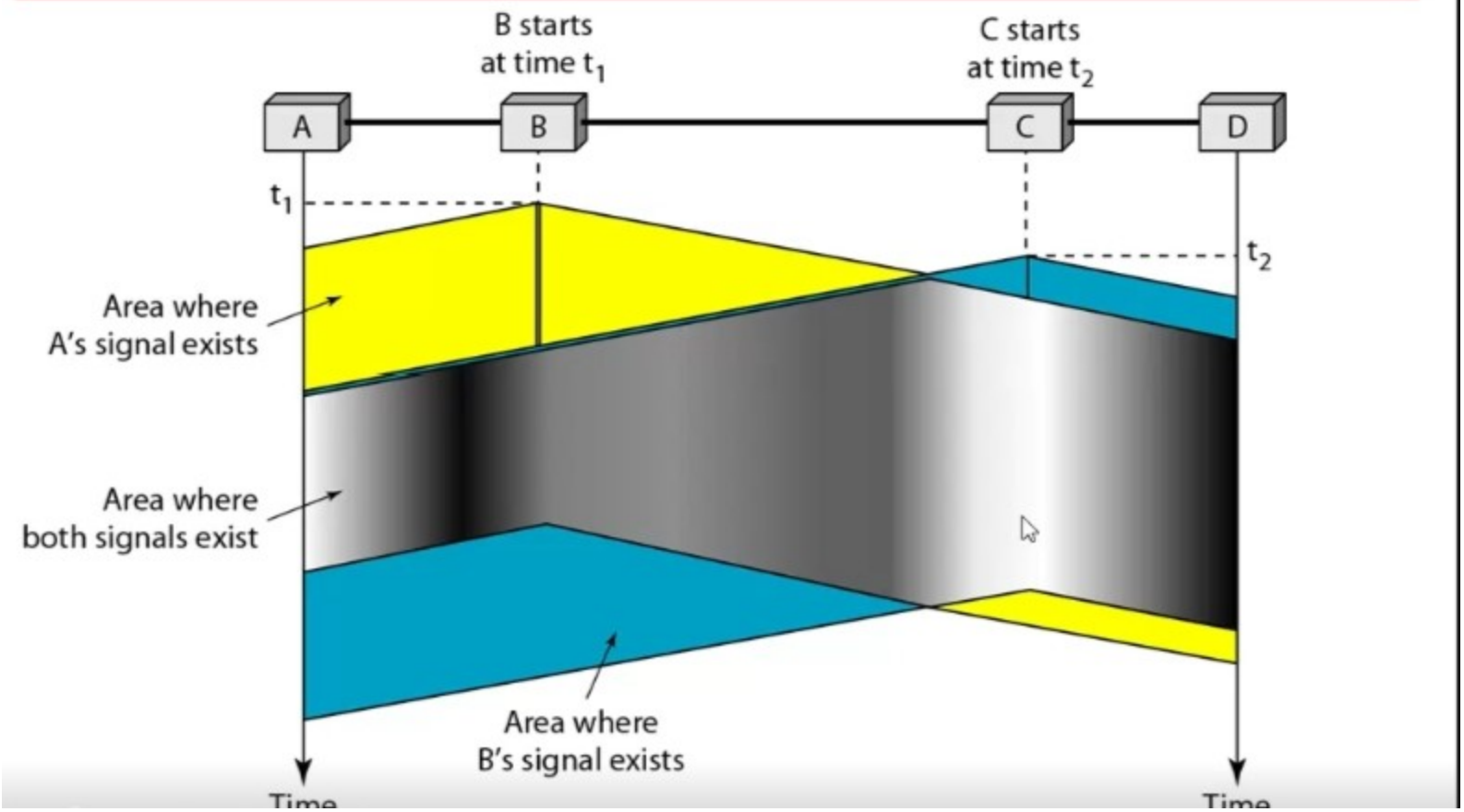
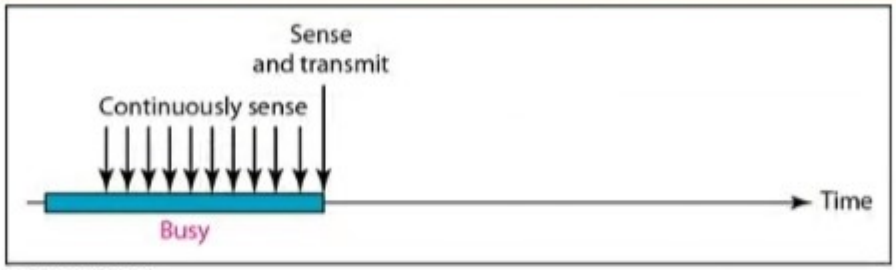
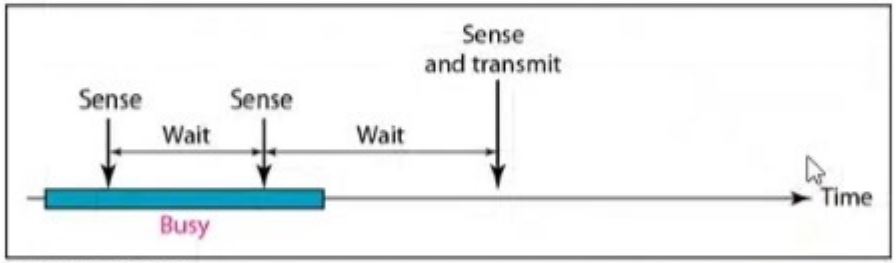


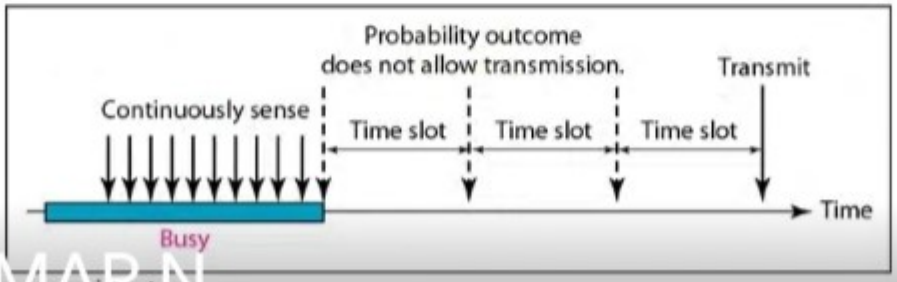
Figure 12.10 *Behavior of three persistence methods*



a. 1-persistent

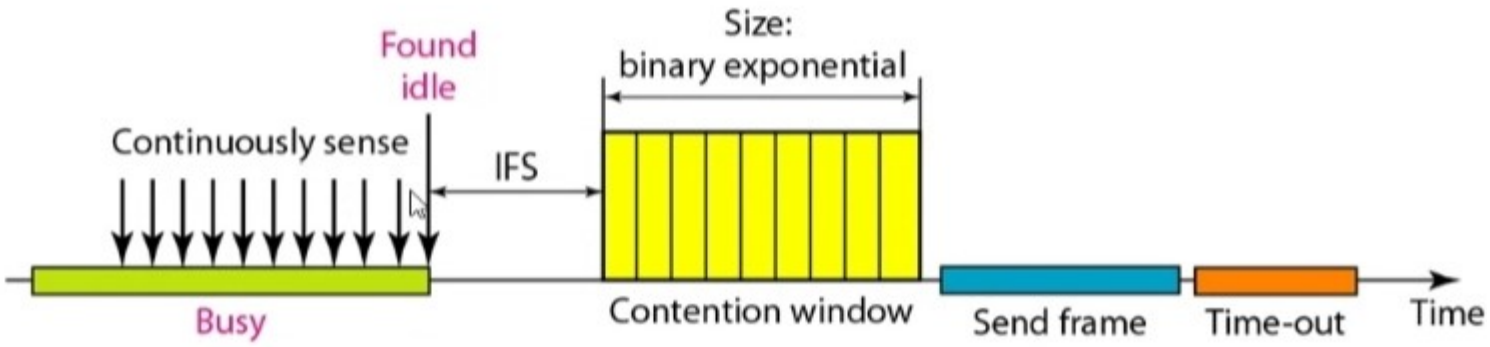


b. Nonpersistent



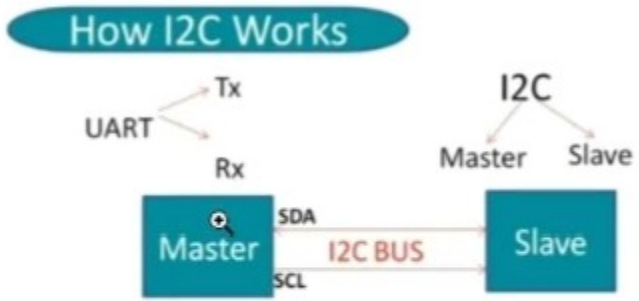
c. p-persistent

Figure 15.16 *Timing in CSMA/CA*



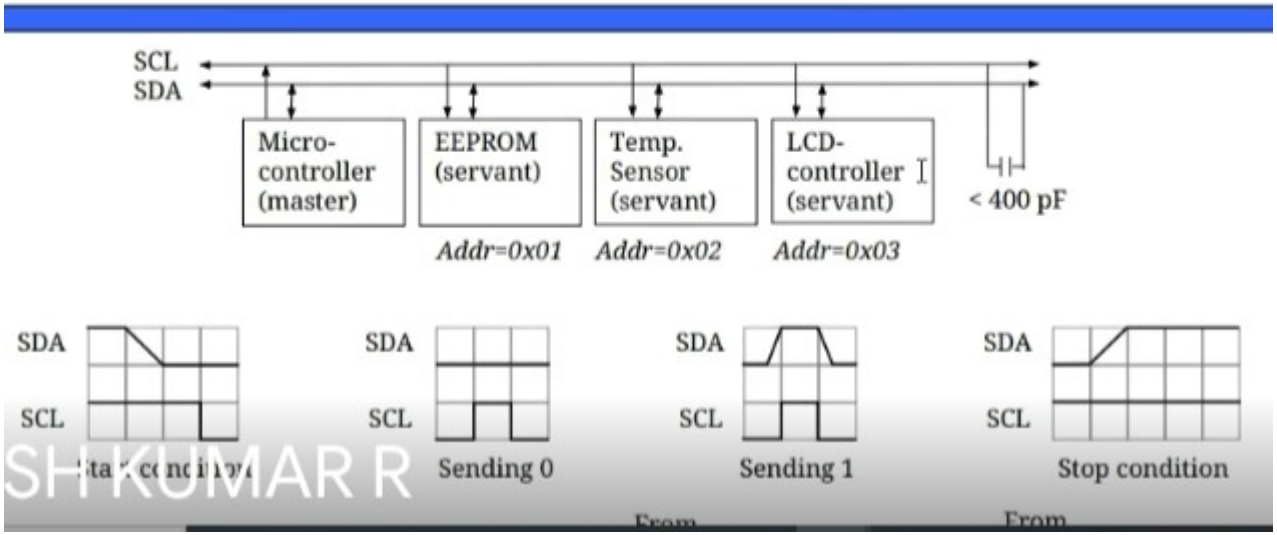
Serial protocols: I^2C

- I^2C (Inter-IC)
  - Two-wire serial bus protocol developed by Philips Semiconductors nearly 20 years ago
  - Enables peripheral ICs to communicate using simple communication hardware
  - Data transfer rates up to 100 kbits/s and 7-bit addressing possible in normal mode
  - 3.4 Mbits/s and 10-bit addressing in fast-mode
  - Common devices capable of interfacing to I^2C bus:
    - EPROMS, Flash, and some RAM memory, real-time clocks, watchdog timers, and microcontrollers



1. SDA (Serial Data)- Bidirectional
2. SCL (Serial Clock) - Clock Signal

I2C bus structure



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12-1 RANDOM ACCESS

In random access or contention methods, no station is superior to another station and none is assigned the control over another. No station permits, or does not permit, another station to send. At each instance, a station that has data to send uses a procedure defined by the protocol to make a decision on whether or not to send.

Topics discussed in this section:

ALOHA
Carrier Sense Multiple Access
Carrier Sense Multiple Access with Collision Detection
Carrier Sense Multiple Access with Collision Avoidance

Figure 12.3 *Frames in a pure ALOHA network*

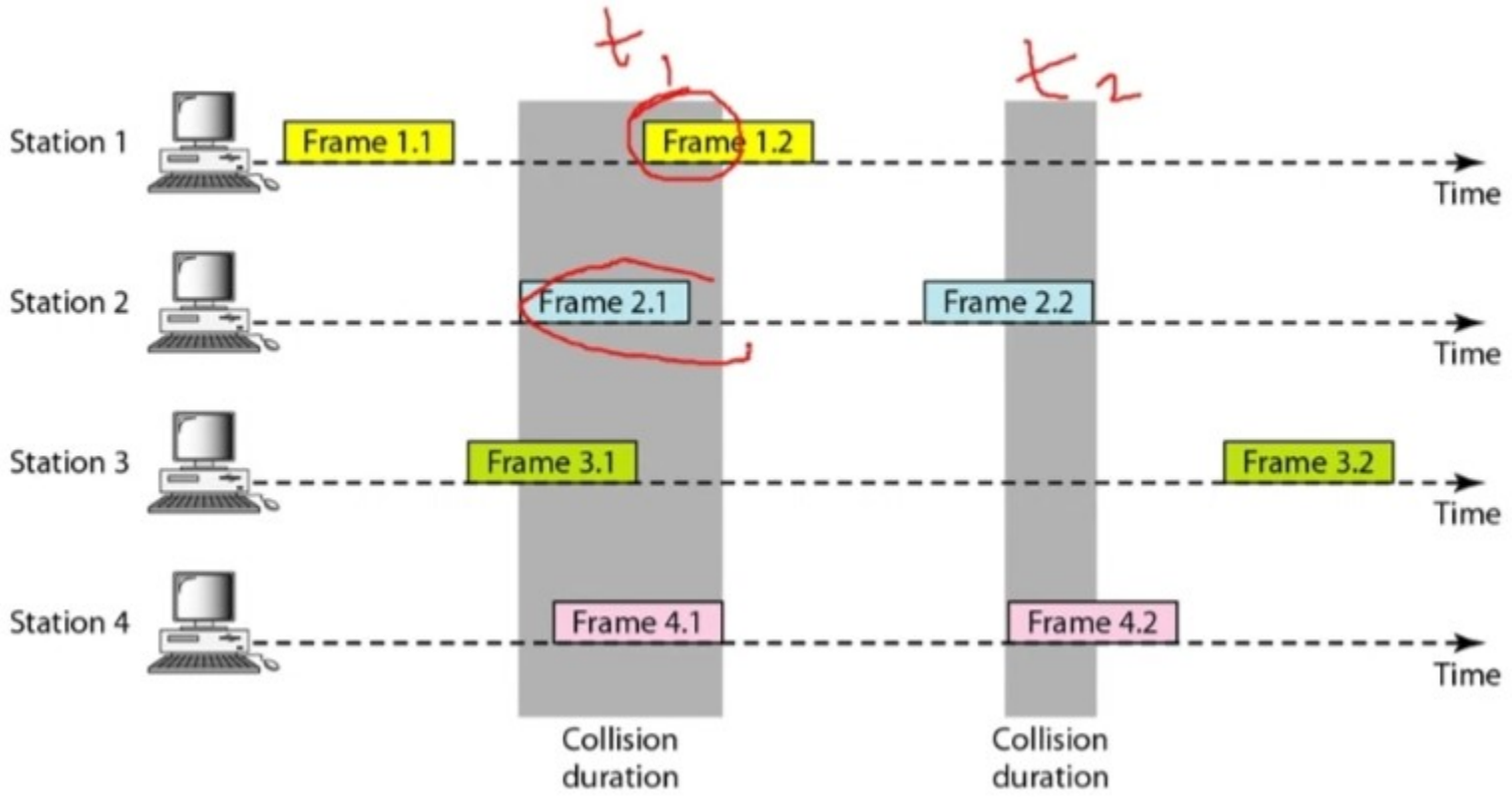
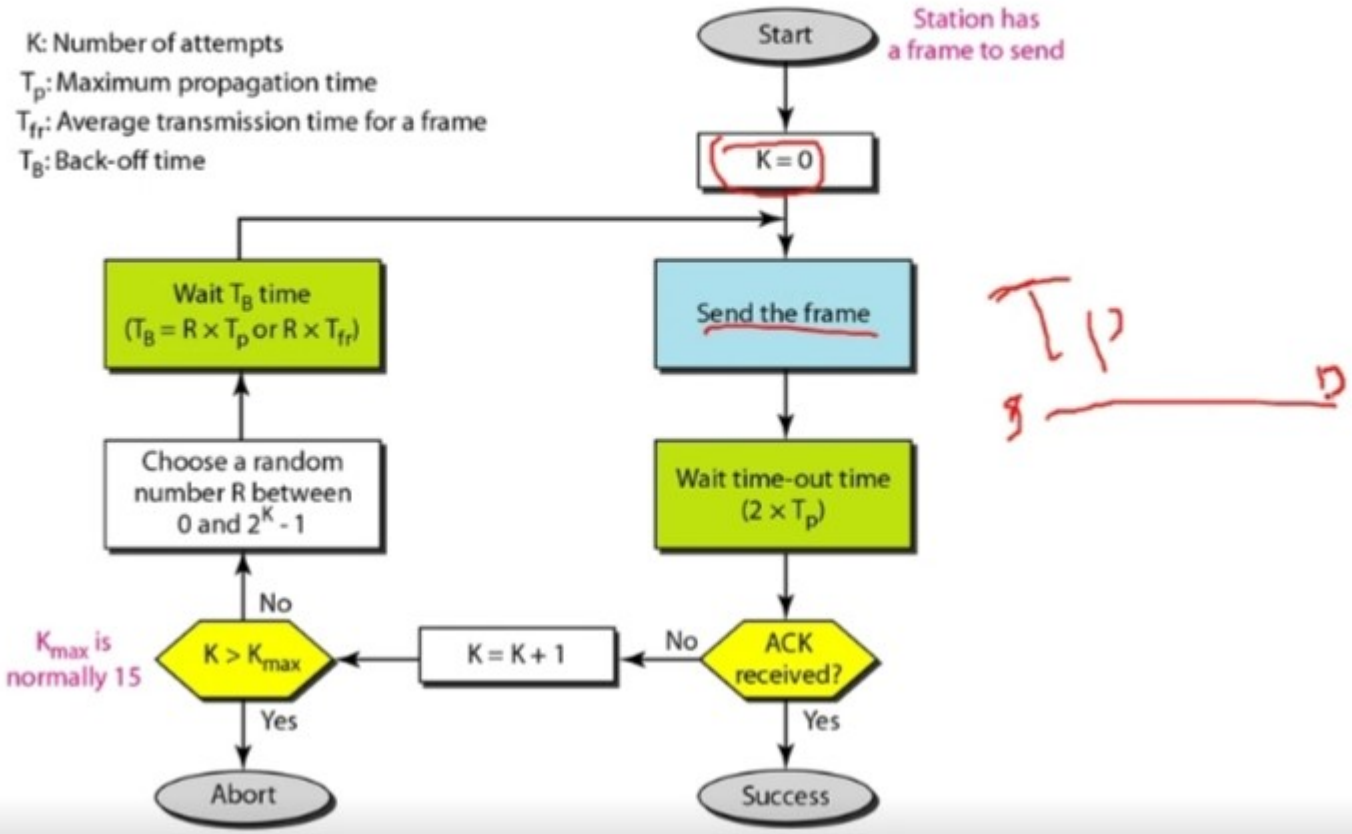


Figure 12.4 *Procedure for pure ALOHA protocol*



Example 12.1 (continued)

b. *For $K = 2$, the range is $\{0, 1, 2, 3\}$. This means that T_B can be 0, 2, 4, or 6 ms, based on the outcome of the random variable.*

c. *For $K = 3$, the range is $\{0, 1, 2, 3, 4, 5, 6, 7\}$. This means that T_B can be 0, 2, 4, . . . , 14 ms, based on the outcome of the random variable.*

d. *We need to mention that if $K > 10$, it is normally set to 10.*

Figure 12.5 *Vulnerable time for pure ALOHA protocol*

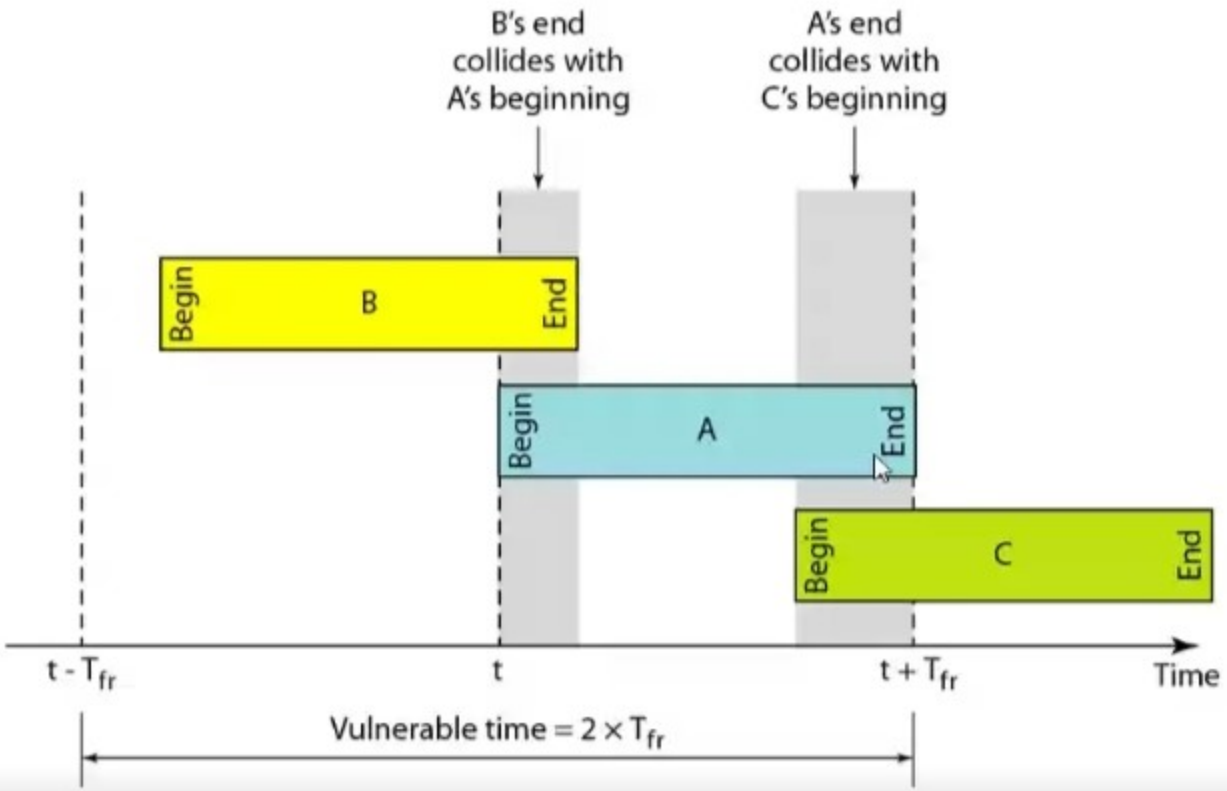
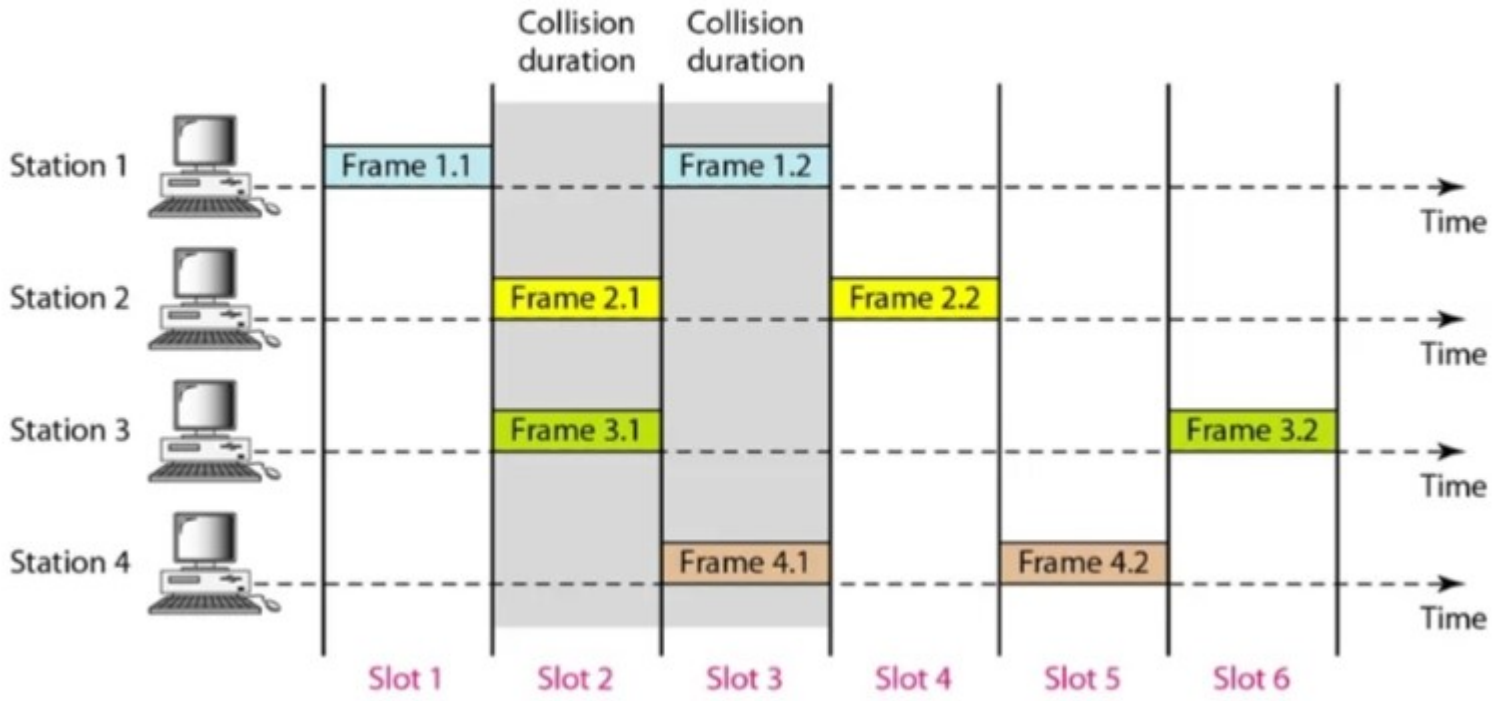


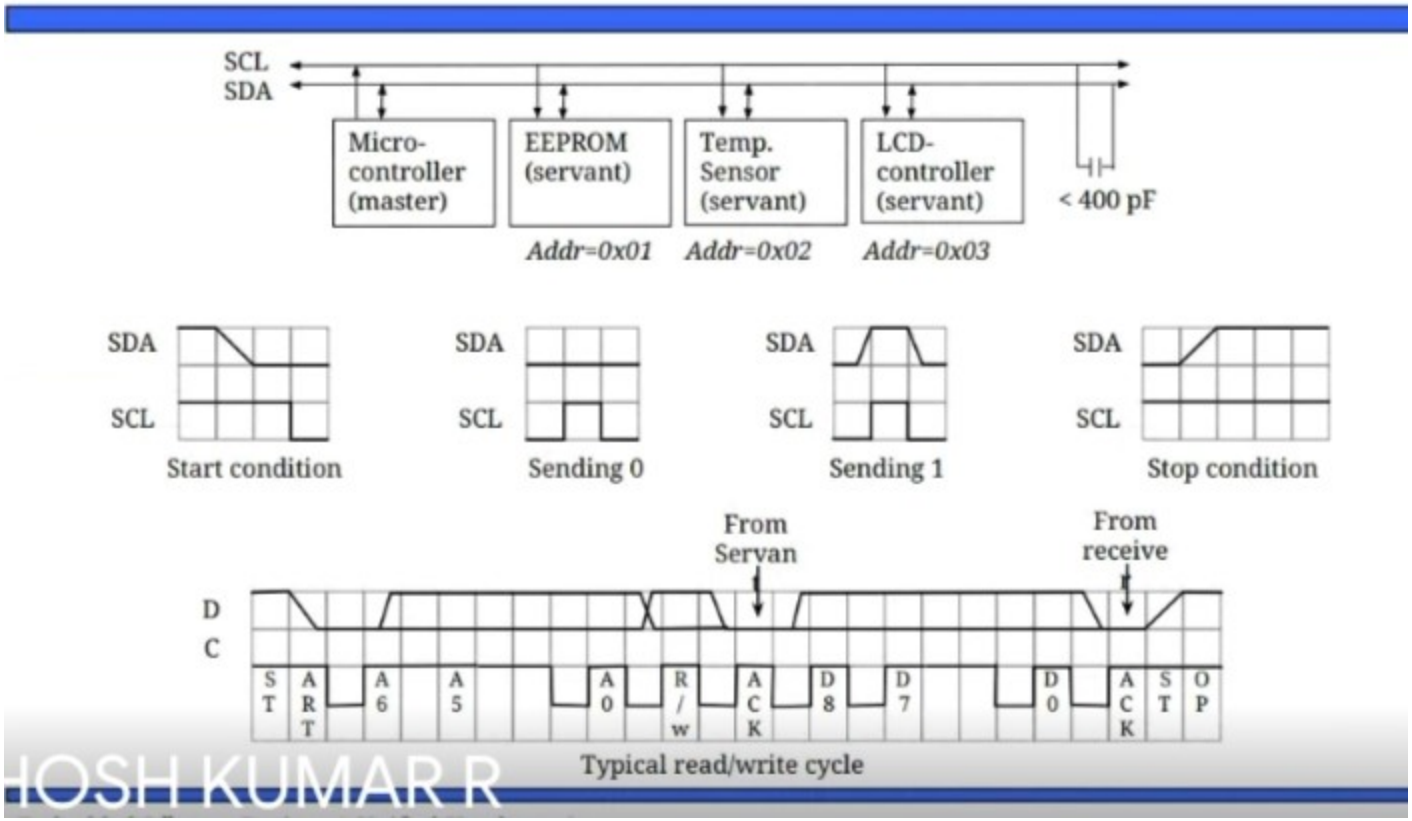
Figure 12.6 *Frames in a slotted ALOHA network*



Note

The throughput for slotted ALOHA is $S = G \times e^{-G}$.

The maximum throughput $S_{max} = 0.368$ when $G = 1$.


SCL
SDA
Micro-controller (master)
EEPROM (servant)
Temp. Sensor (servant)
LCD-controller (servant)
< 400 pF
Addr=0x01
Addr=0x02
Addr=0x03
SDA
SCL
Start condition
Sending 0
Sending 1
Stop condition
From Servan
From receive
D
C
ST
ART
A6
A5
A0
R/w
ACK
D8
D7
D0
ACK
ST
OP
Typical read/write cycle

- CAN (Controller area network)
  - Protocol for real-time applications
  - Developed by Robert Bosch GmbH
  - Originally for communication among components of cars
  - Applications now using CAN include:
    - elevator controllers, copiers, telescopes, production-line control systems, and medical instruments
  - Data transfer rates up to 1 Mbit/s and 11-bit addressing
  - Common devices interfacing with CAN:
    - 8051-compatible 8592 processor and standalone CAN controllers
  - Actual physical design of CAN bus not specified in protocol
    - Requires devices to transmit/detect dominant and recessive signals to/from bus
    - e.g., '1' = dominant, '0' = recessive if single data wire used
    - Bus guarantees dominant signal prevails over recessive signal if asserted

Serial protocols: USB

- USB (Universal Serial Bus)
  - Easier connection between PC and monitors, printers, digital speakers, modems, scanners, digital cameras, joysticks, multimedia game equipment
  - 2 data rates:
    - 12 Mbps for increased bandwidth devices
    - 1.5 Mbps for lower-speed devices (joysticks, game pads)
  - Tiered star topology can be used
    - One USB device (hub) connected to PC
      - hub can be embedded in devices like monitor, printer, or keyboard or can be stand-alone
    - Multiple USB devices can be connected to hub
    - Up to 127 devices can be connected like this
  - USB host controller
    - Manages and controls bandwidth and driver software required by each peripheral
    - Dynamically allocates power downstream according to devices connected

Parallel protocols: PCI Bus

- PCI Bus (Peripheral Component Interconnect)
  - High performance bus originated at Intel in the early 1990's
  - Standard adopted by industry and administered by PCISIG (PCI Special Interest Group)
  - Interconnects chips, expansion boards, processor memory subsystems
  - Data transfer rates of 127.2 to 508.6 Mbits/s and 32-bit addressing
    - Later extended to 64-bit while maintaining compatibility with 32-bit schemes
  - Synchronous bus architecture
  - Multiplexed data/address lines