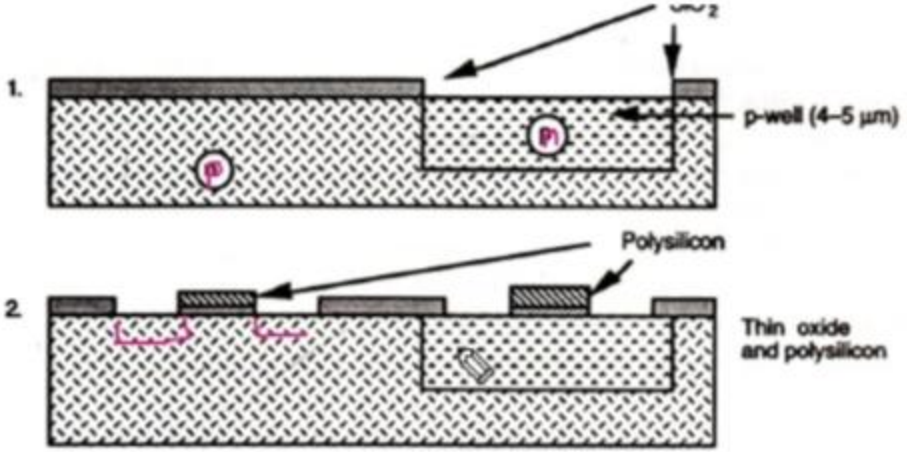
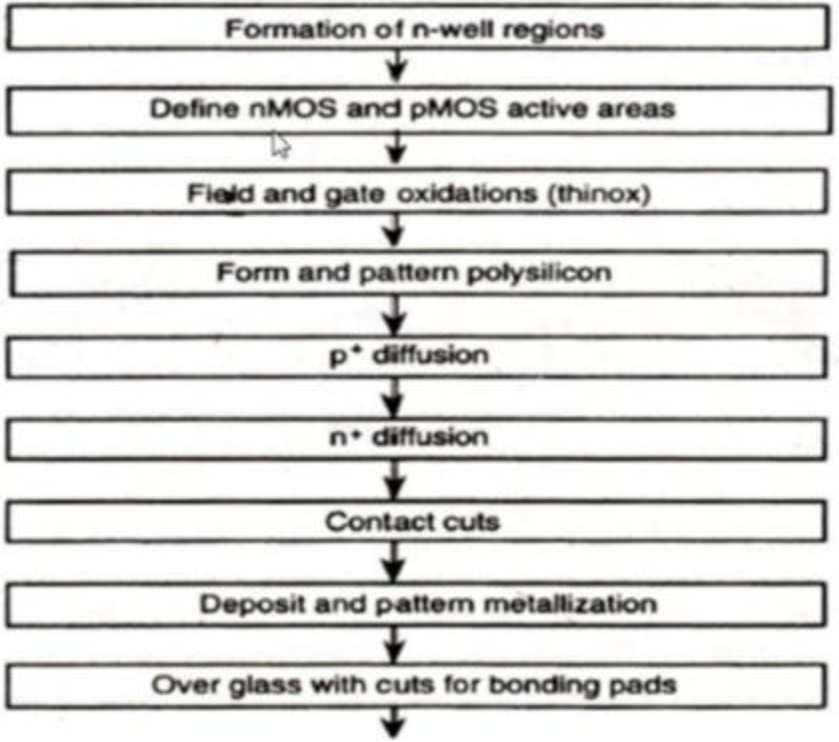
CMOS FABRICATION

- **The p-well Process**



The n-well Process



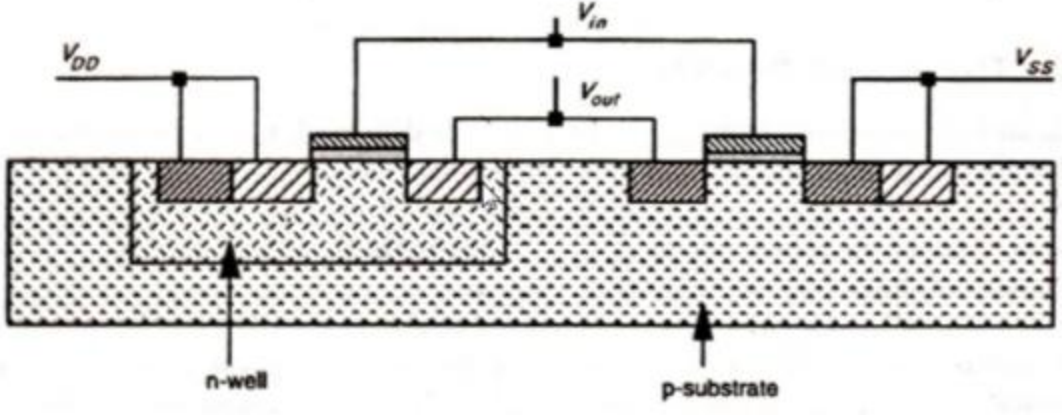


FIGURE 1.12 Cross-sectional view of n-well CMOS inverter.

The Twin-Tub Process

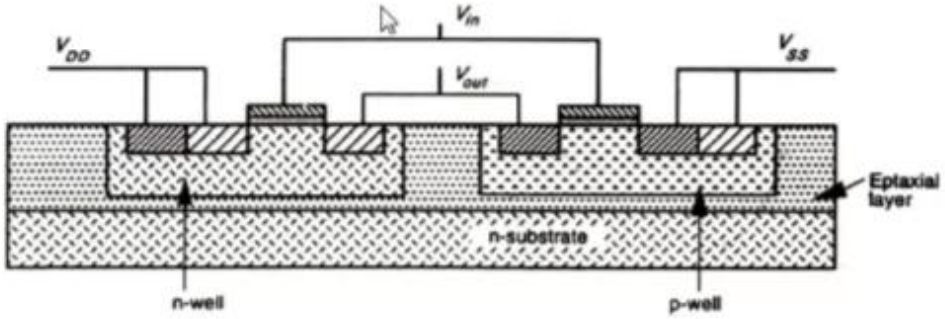
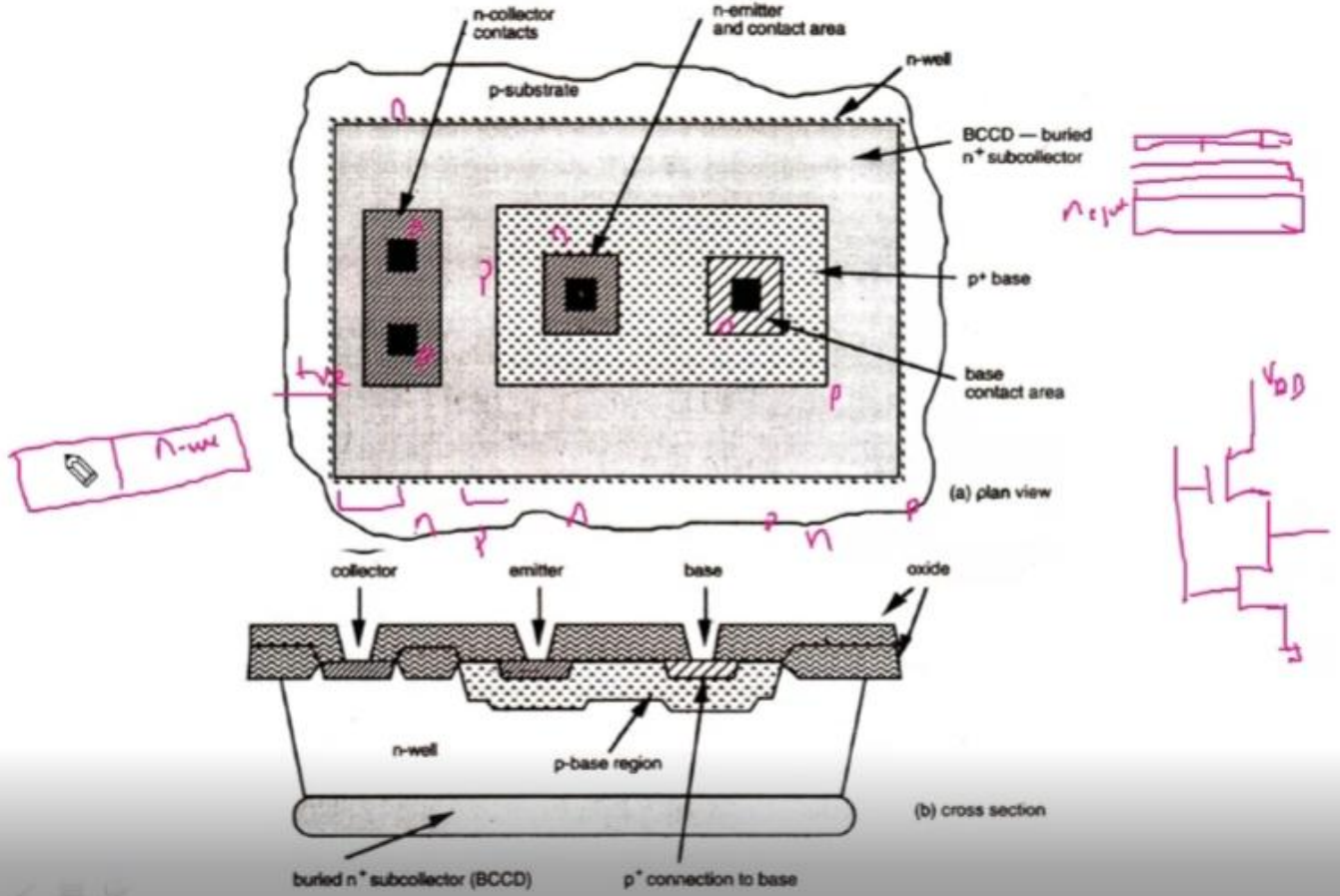


FIGURE 1.14 Twin-tub structure.

BICMOS TECHNOLOGY



Comparison of CMOS and Bipolar Technology

CMOS technology	*Bipolar technology*
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load (fan-out limitations)	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m ($g_m \alpha V_{in}$)	• High g_m ($g_m \alpha e^{V_{in}}$)
	• High f_t at low currents
• Bidirectional capability (drain and source are interchangeable)	• Essentially unidirectional
• A near ideal switching device	