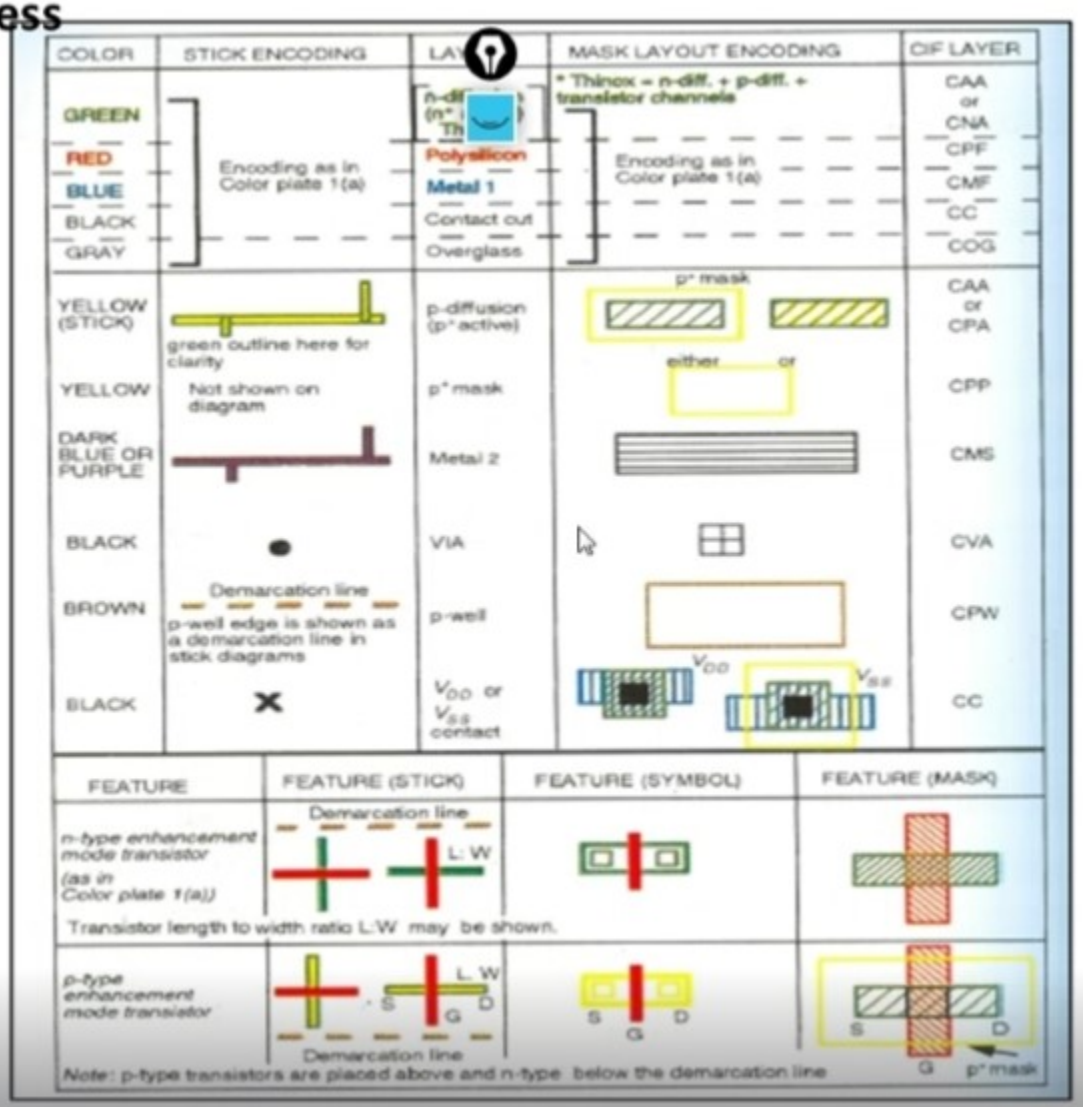
CMOS process



BiCMOS process

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE	MONOCHROME	Polysilicon 2	MONOCHROME	CPS
SEE COLOR PLATE 1(c)		Bipolar npn transistor	see Figure 3–13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor	n-well	CCA

FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement poly 2 transistor	DEMARCATION LINE, L:W, S, D, G	GREEN, S, D, G, ORANGE	S, D, G
Transistor length to width ratio L:W may be shown.			
p-type enhancement poly 2 transistor	L:W, DEMARCATION LINE	YELLOW, ORANGE	
Note: p-type transistors are placed above and n-type transistors below the demarcation line.			
npn bipolar transistor			See Figure 3–13(f) and Color plate 6

nMOS Design Style

The layout of nMOS involves

1. n-diffusion and other thinoxide regions –green
2. Polysilicon 1-red
3. Metal 1-blue
4. Implant-yellow
5. Contacts-black or brown

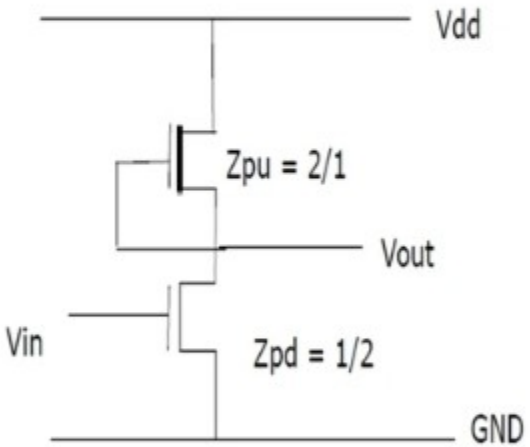
The Transistor is formed wherever poly crosses n-diffusion (red over green)and all diffusion wire(interconnection)a re n-type(green)

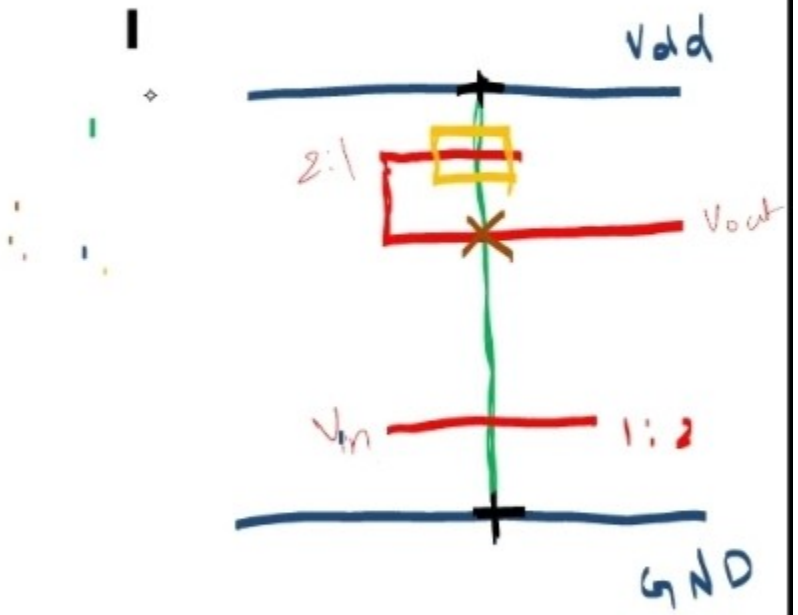
Steps for Layout

- Draw the meta(blue) VDD and GND rails
- Thinox(green) paths may be drawn between rails for inverters
- Depletion mode transistors connected from output point to VDD and pull-down structure of enhancement mode connected between output and GND
- Implants for depletion mode transistor
- Signal paths may also be switched by pass transistor
- Leaf-cell boundaries are conveniently shown on stick diagram

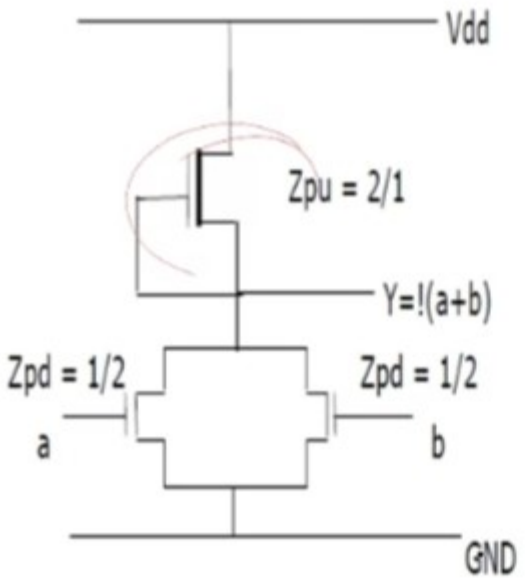
Examples

nMOS Inverter



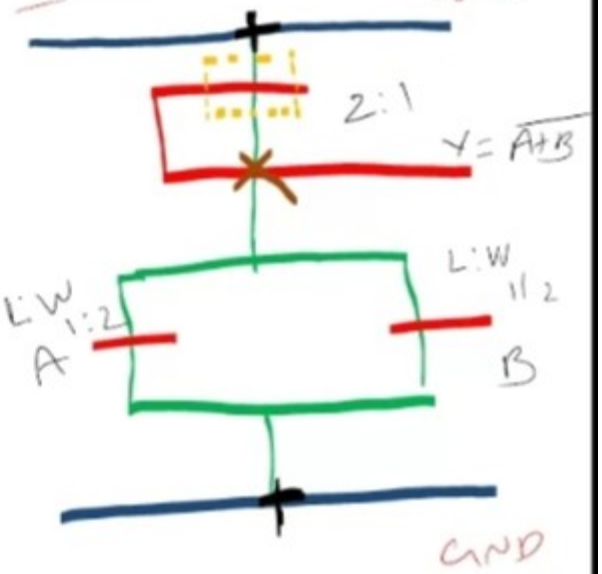


nMOS Depletion load NOR

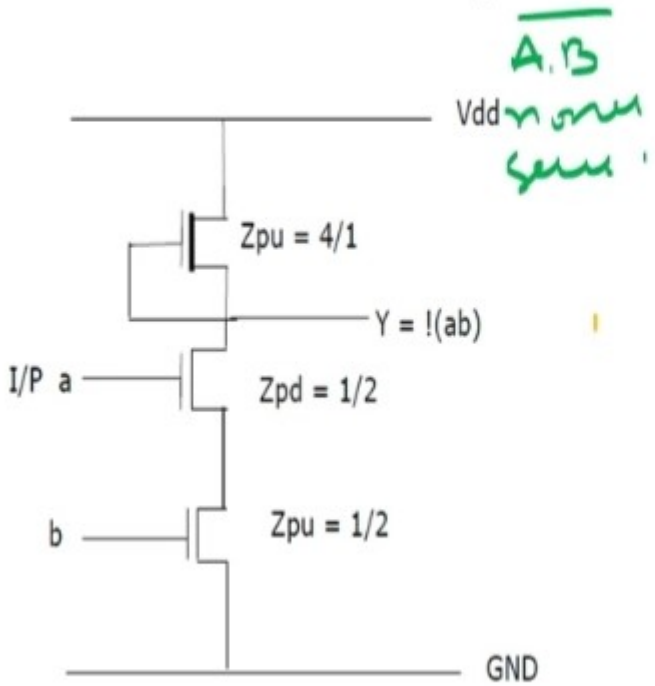


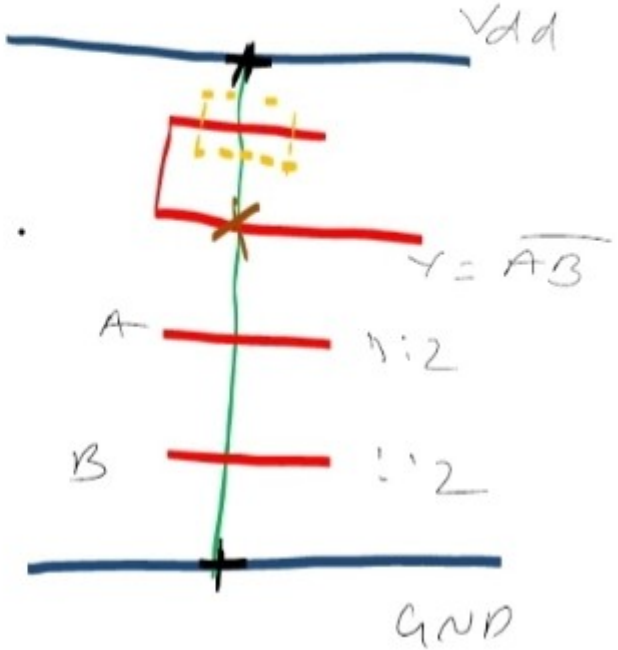
$y = \overline{A+B}$ – nmos parallel

depletion mode



nMOS Depletion load NAND





Buses, Control Signals, Interconnections and leaf Boundaries