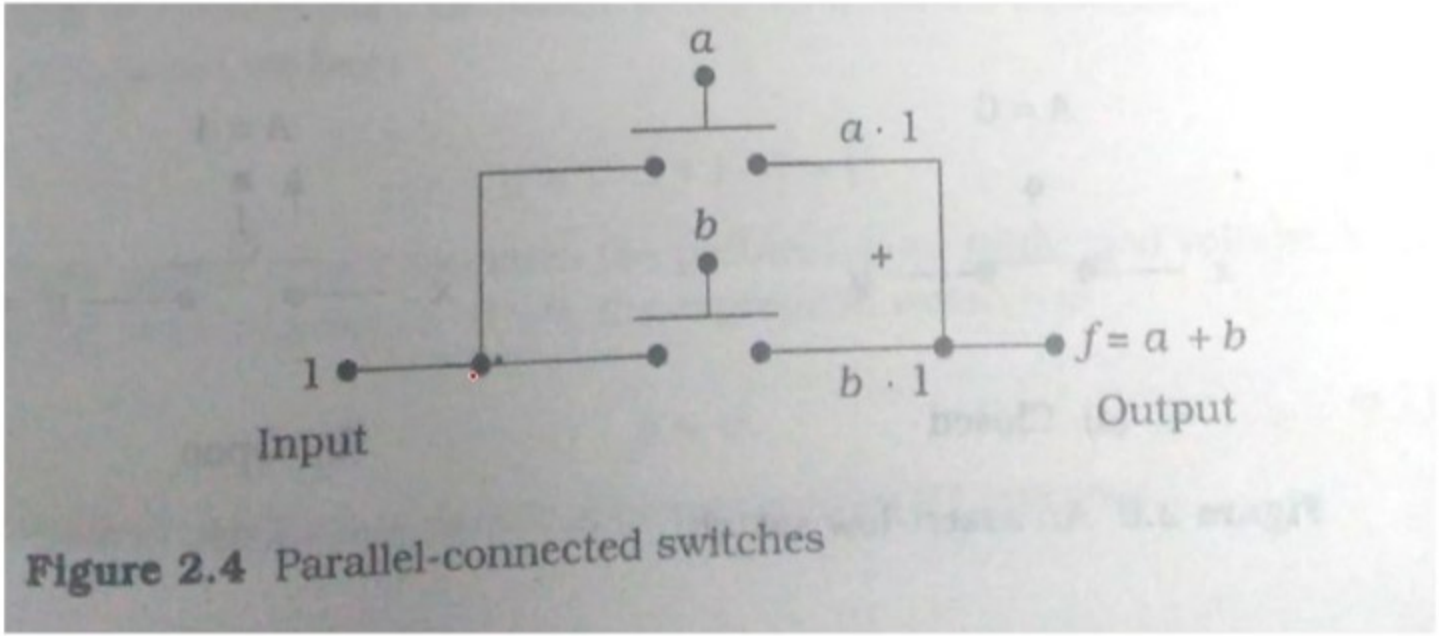
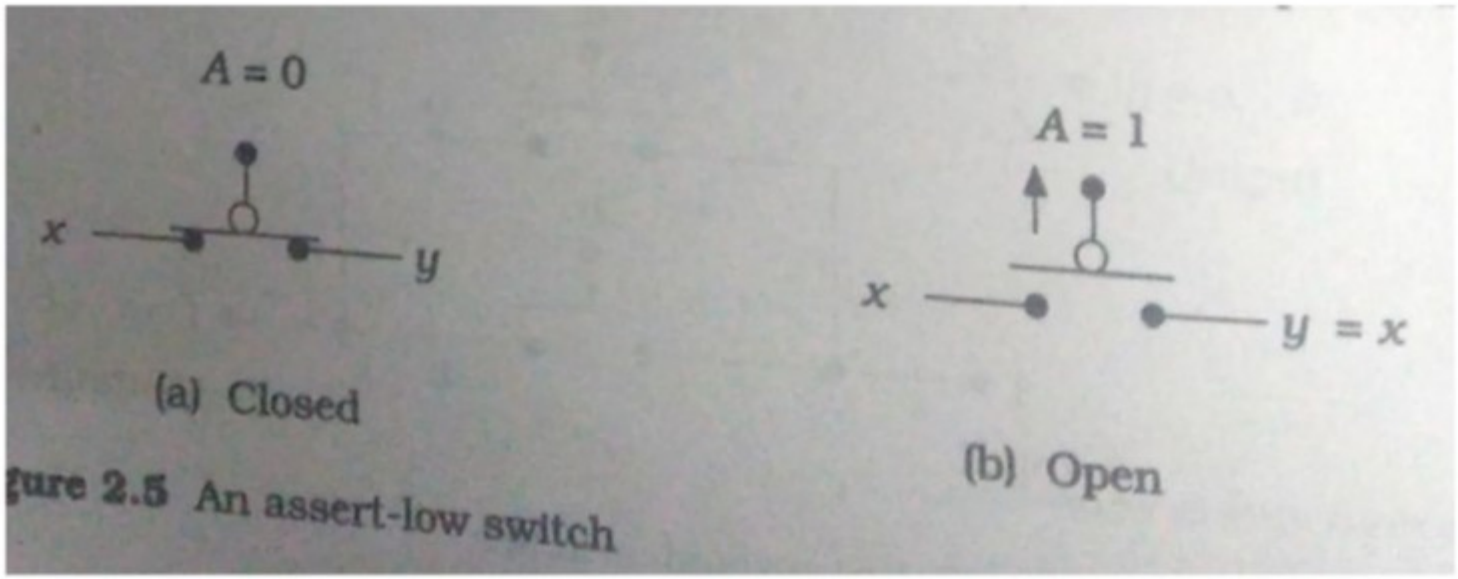


Figure 2.4 Parallel-connected switches



ure 2.5 An assert-low switch

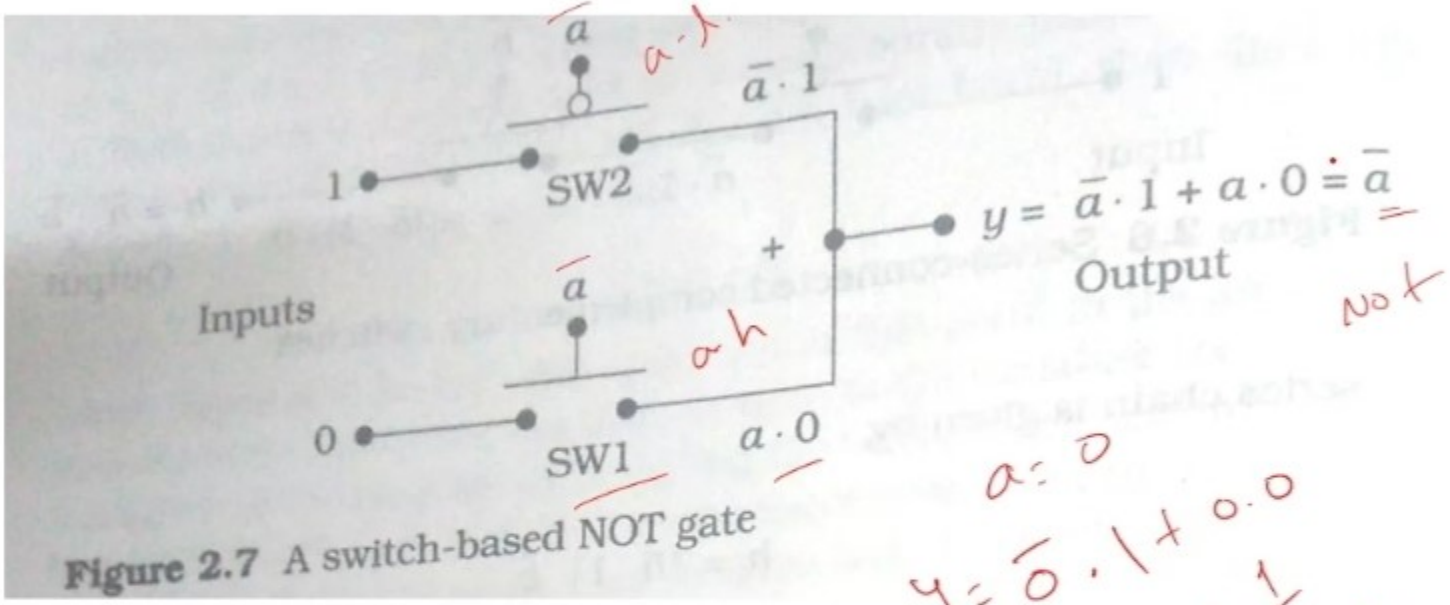


Figure 2.7 A switch-based NOT gate

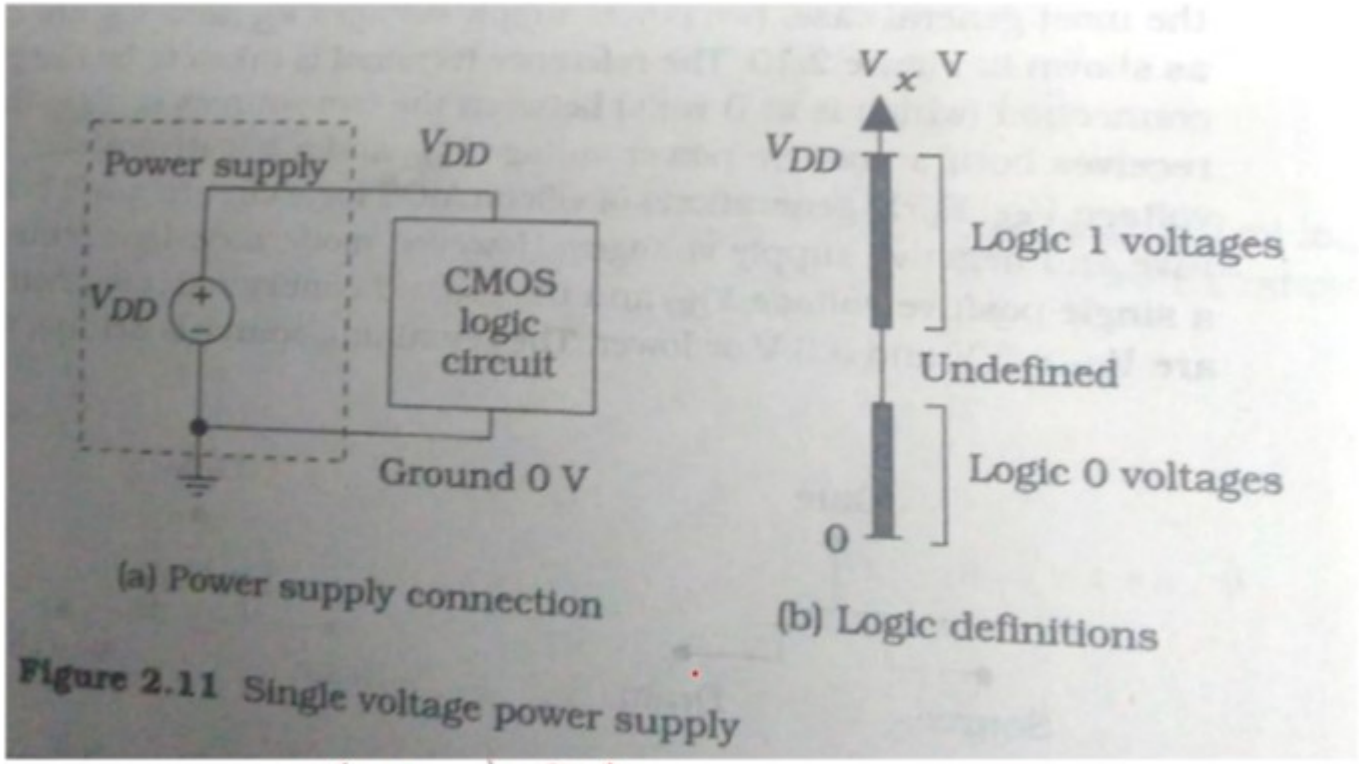


Figure 2.11 Single voltage power supply

Logic 0 i/p 0
Logic 1 if V_{DD}

V_{DD}

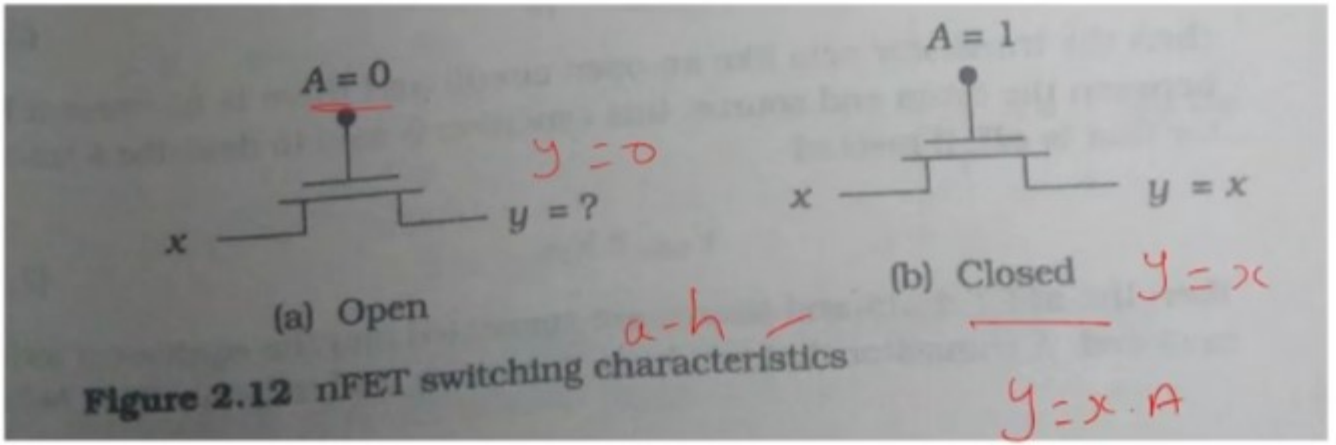


Figure 2.12 nFET switching characteristics

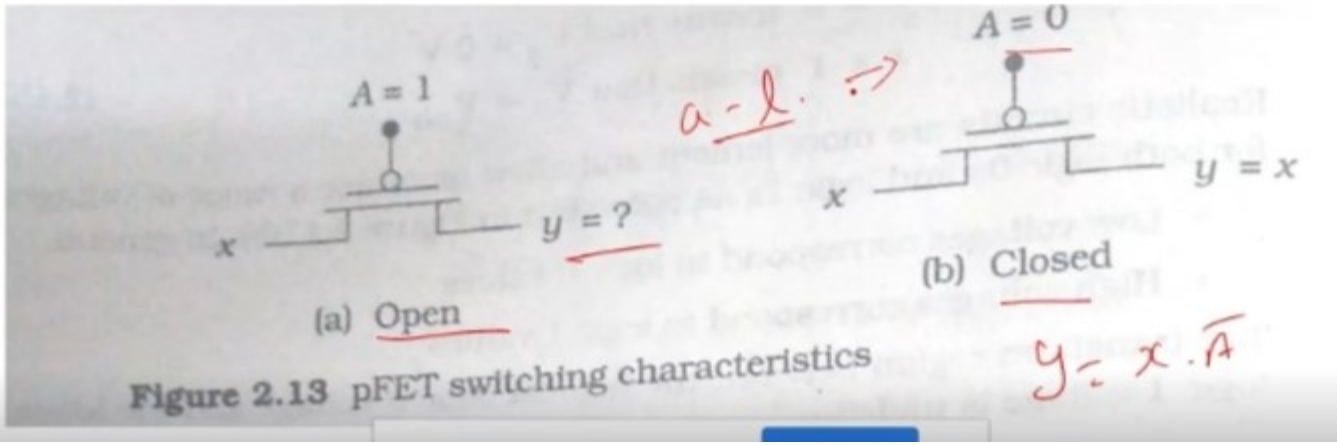


Figure 2.13 pFET switching characteristics