Dayananda Sagar College of Engineering
Department of Electronics and Communication

FUNDAMENTALS OF VLSI DESIGN

By
Dr.Usha. C

MODULE-2
Design with MOSFETs

Ideal Switches and Boolean Operation

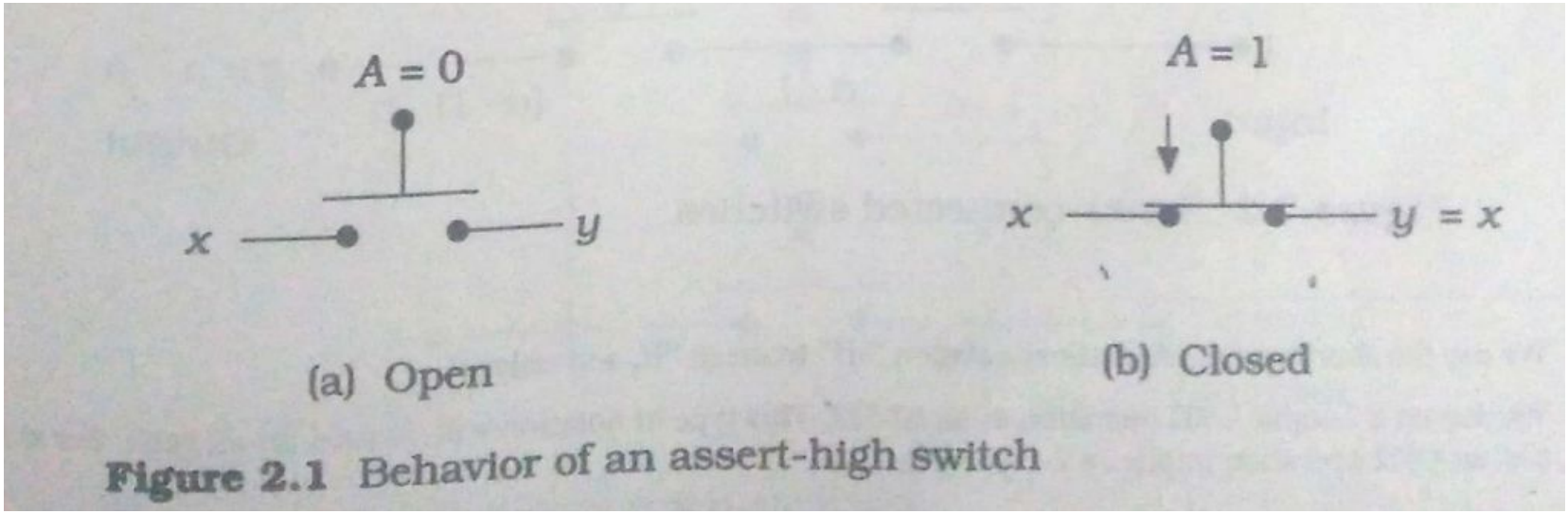


Figure 2.1 Behavior of an assert-high switch

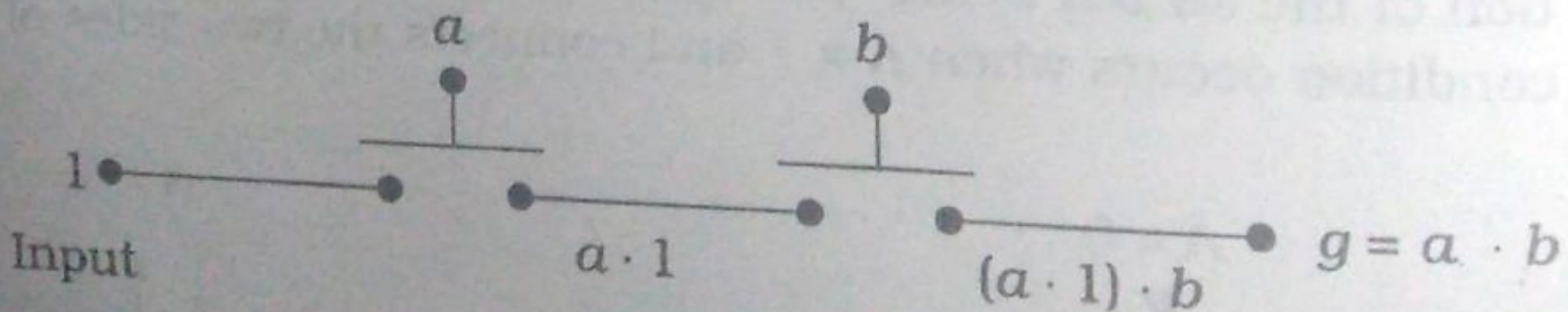


Figure 2.2 Series-connected switches

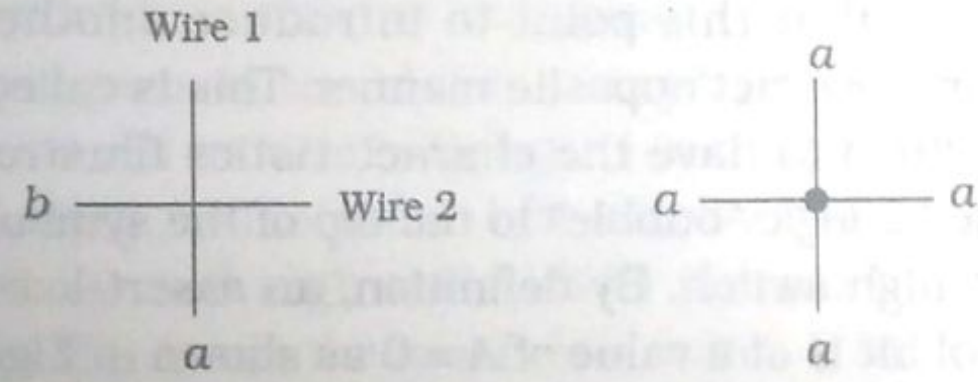


Figure 2.3 Connection convention used in schematic diagrams

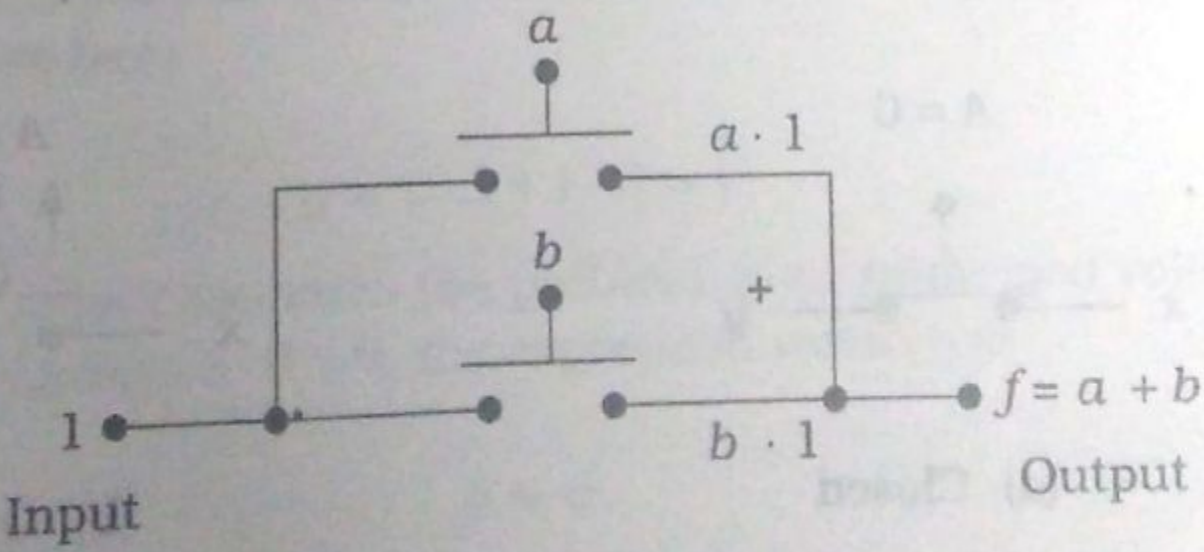
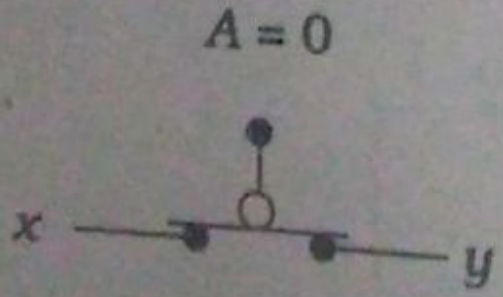
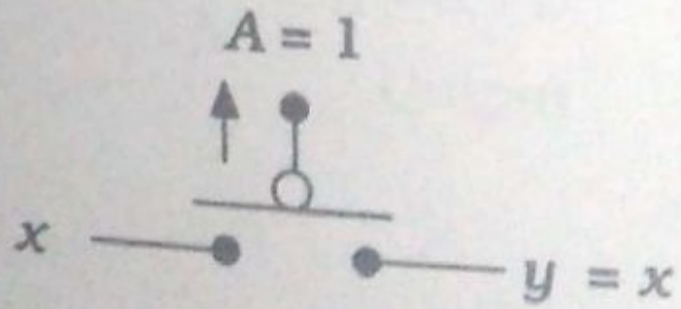


Figure 2.4 Parallel-connected switches



(a) Closed



(b) Open

ure 2.5 An assert-low switch

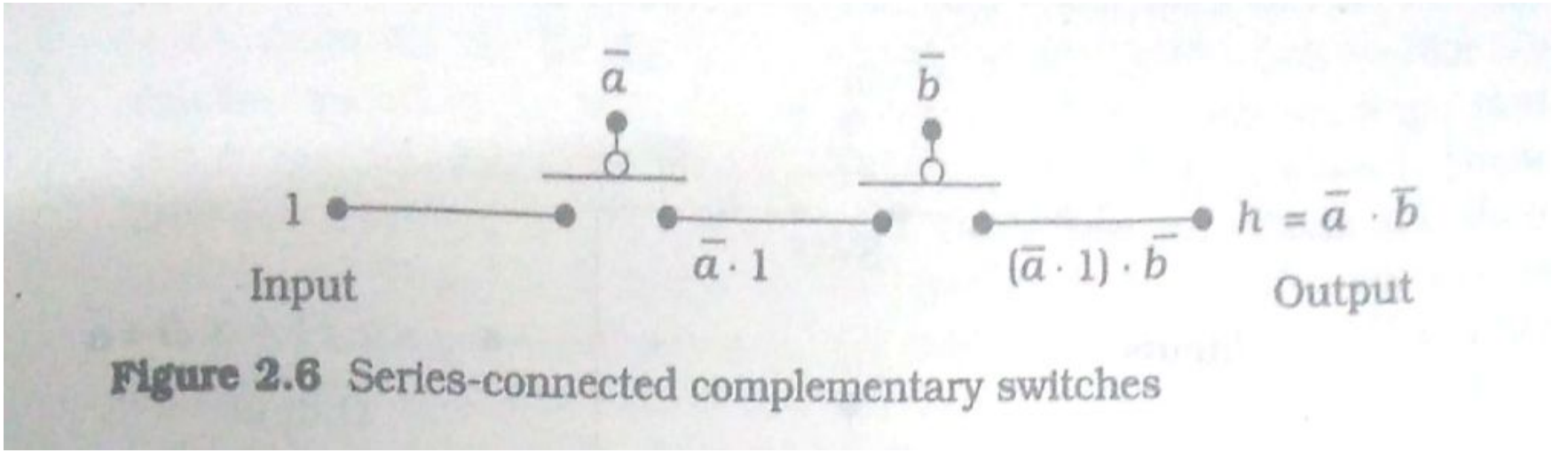


Figure 2.6 Series-connected complementary switches

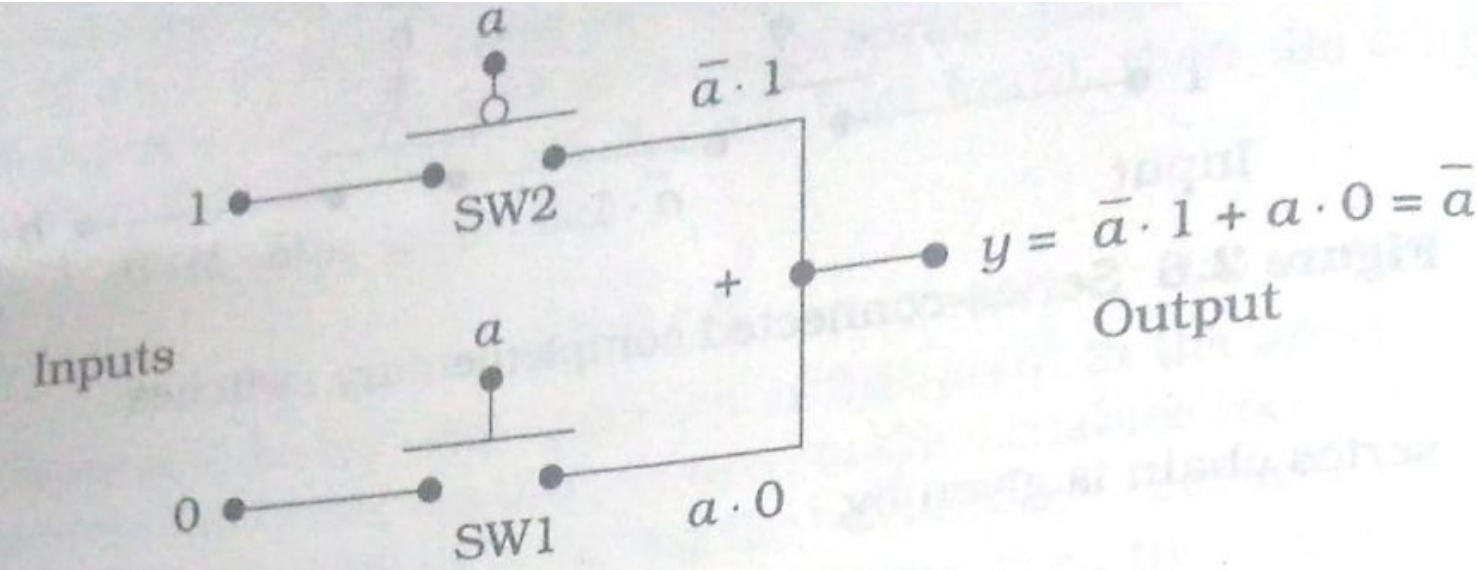


Figure 2.7 A switch-based NOT gate

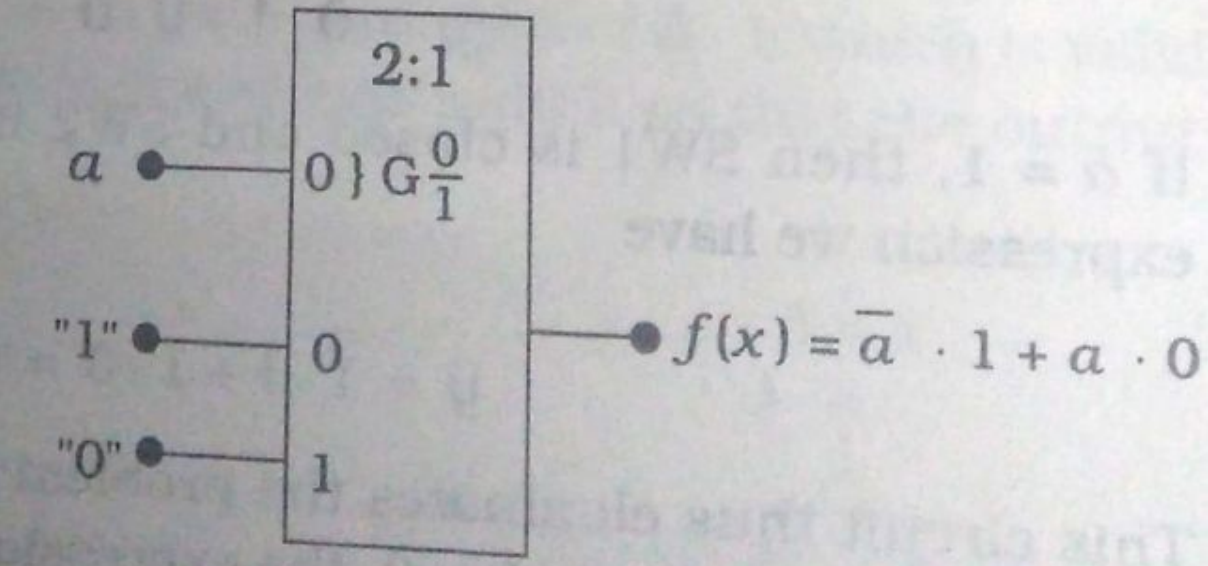
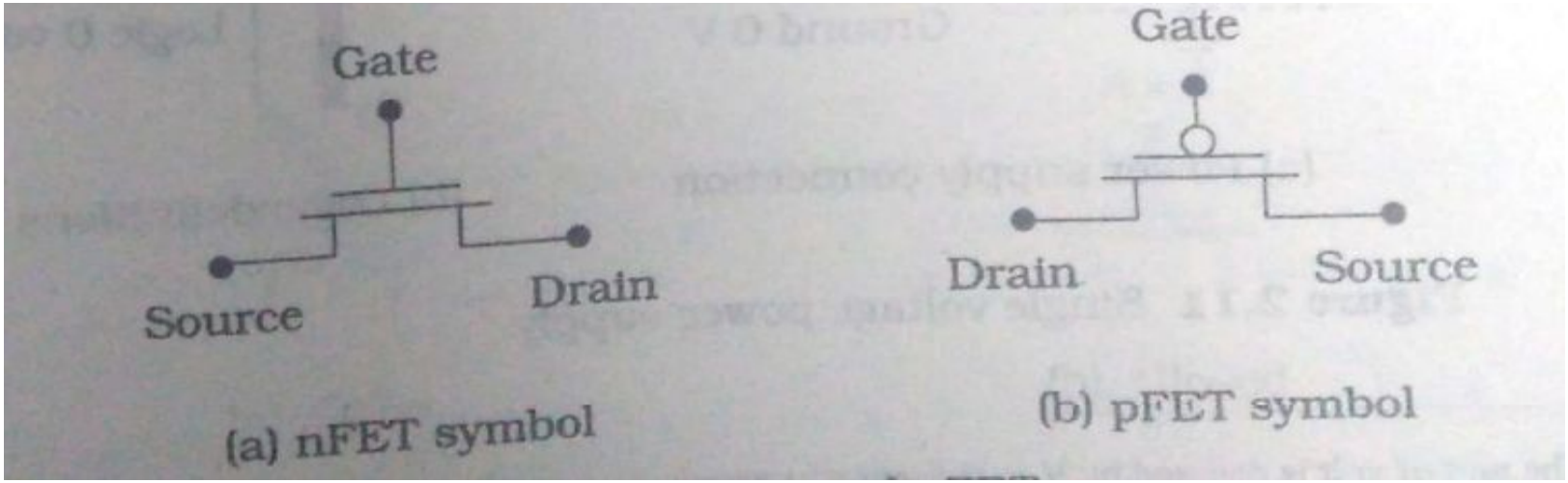
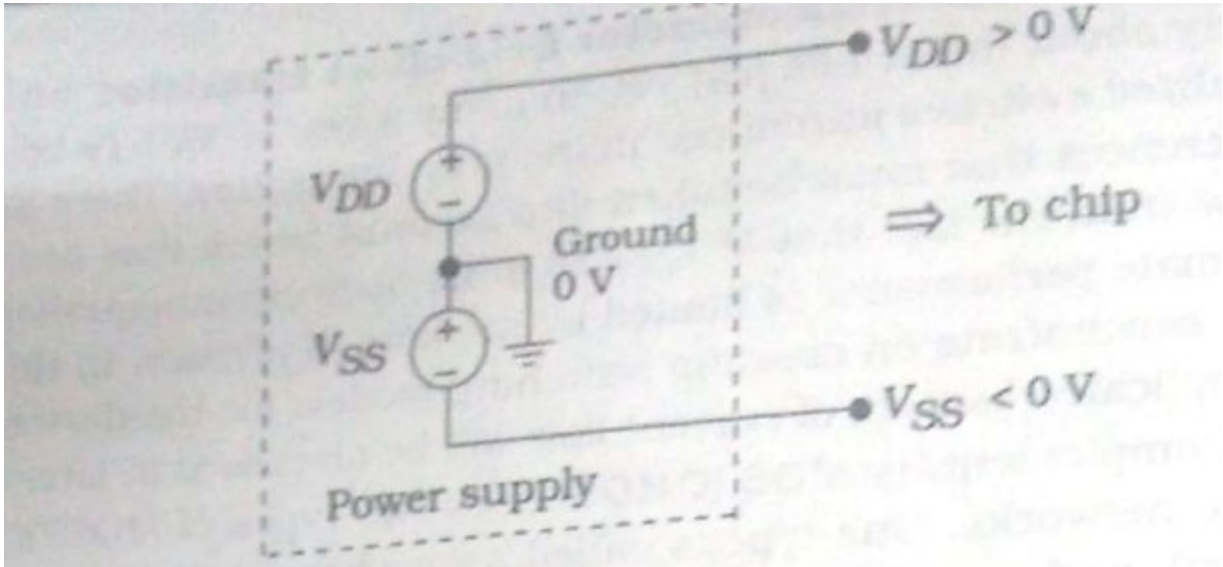


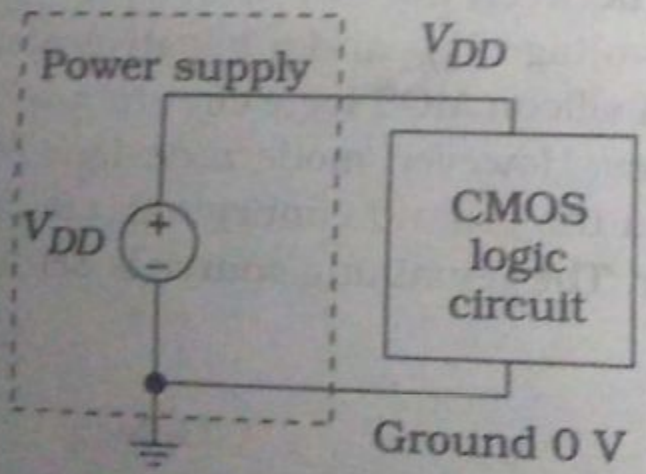
Figure 2.8 A MUX-based NOT gate

MOSFET as switches

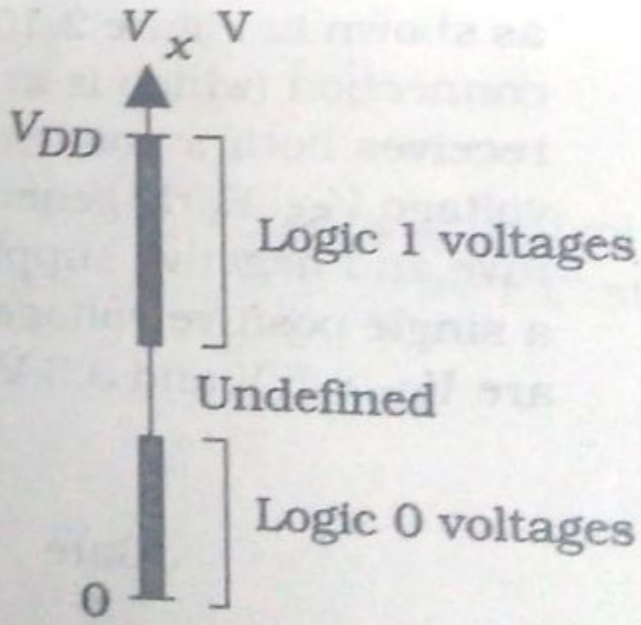




ure 2.10 Dual power supply voltages

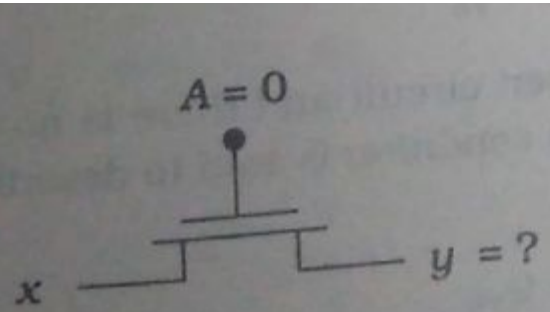


(a) Power supply connection

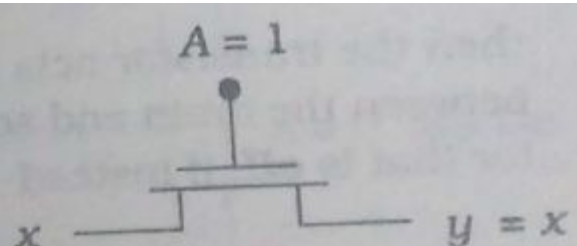


(b) Logic definitions

Figure 2.11 Single voltage power supply

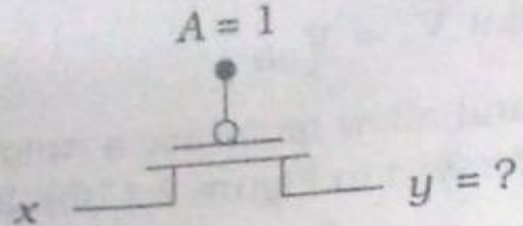


(a) Open

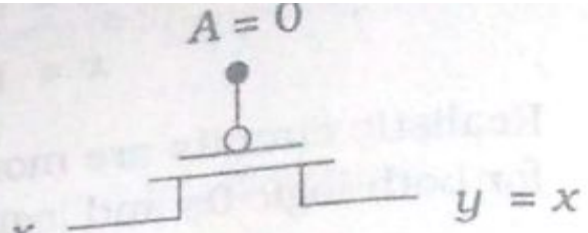


(b) Closed

Figure 2.12 nFET switching characteristics



(a) Open



(b) Closed

Figure 2.13 pFET switching characteristics

FET Threshold Voltages

nFET

V_{Tn} = 0.5 V to 0.7 V

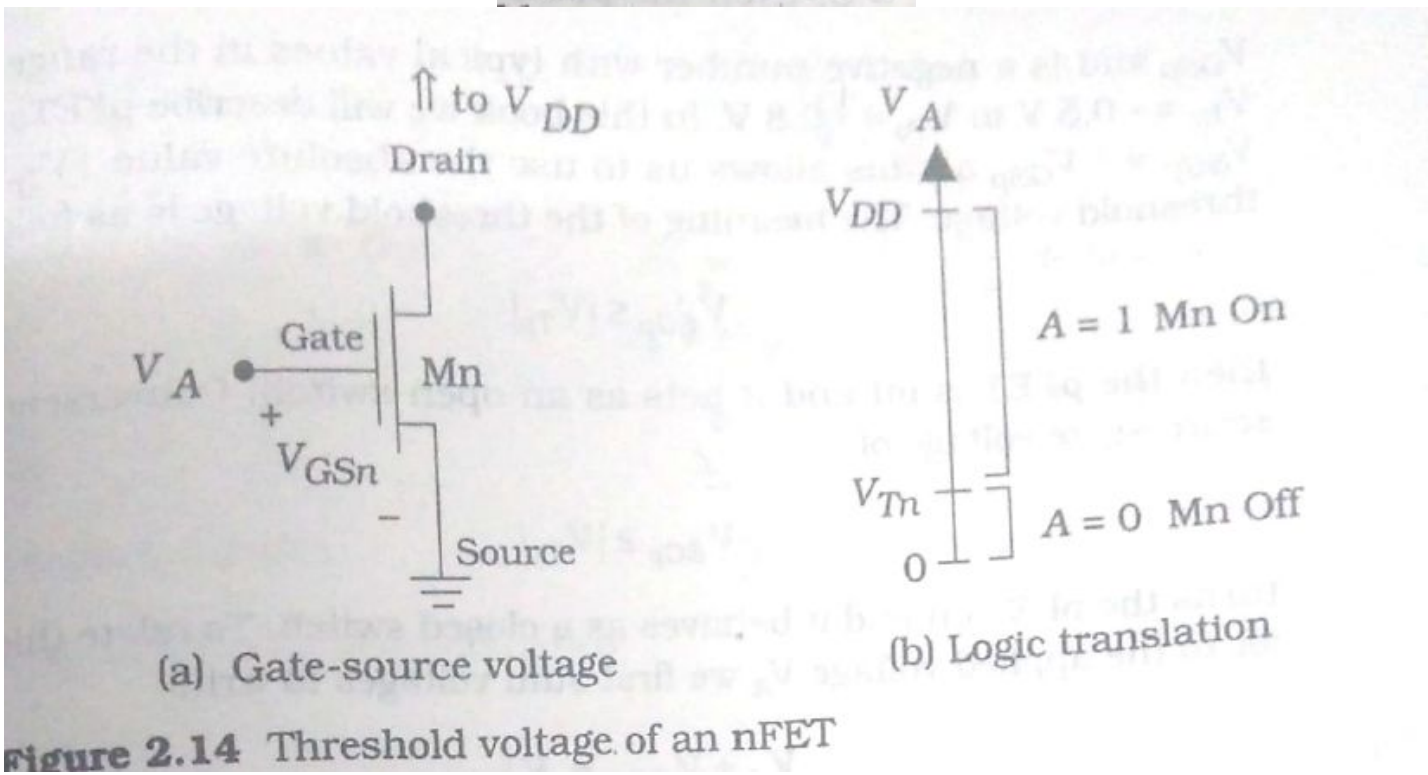


Figure 2.14 Threshold voltage of an nFET

Open Switch

$V_{GSn} \leq V_{Tn}$

Closed Switch

$V_{GSn} \geq V_{Tn}$

A=0

$V_A = V_{GSn}$ $V_A \leq V_{Tn}$

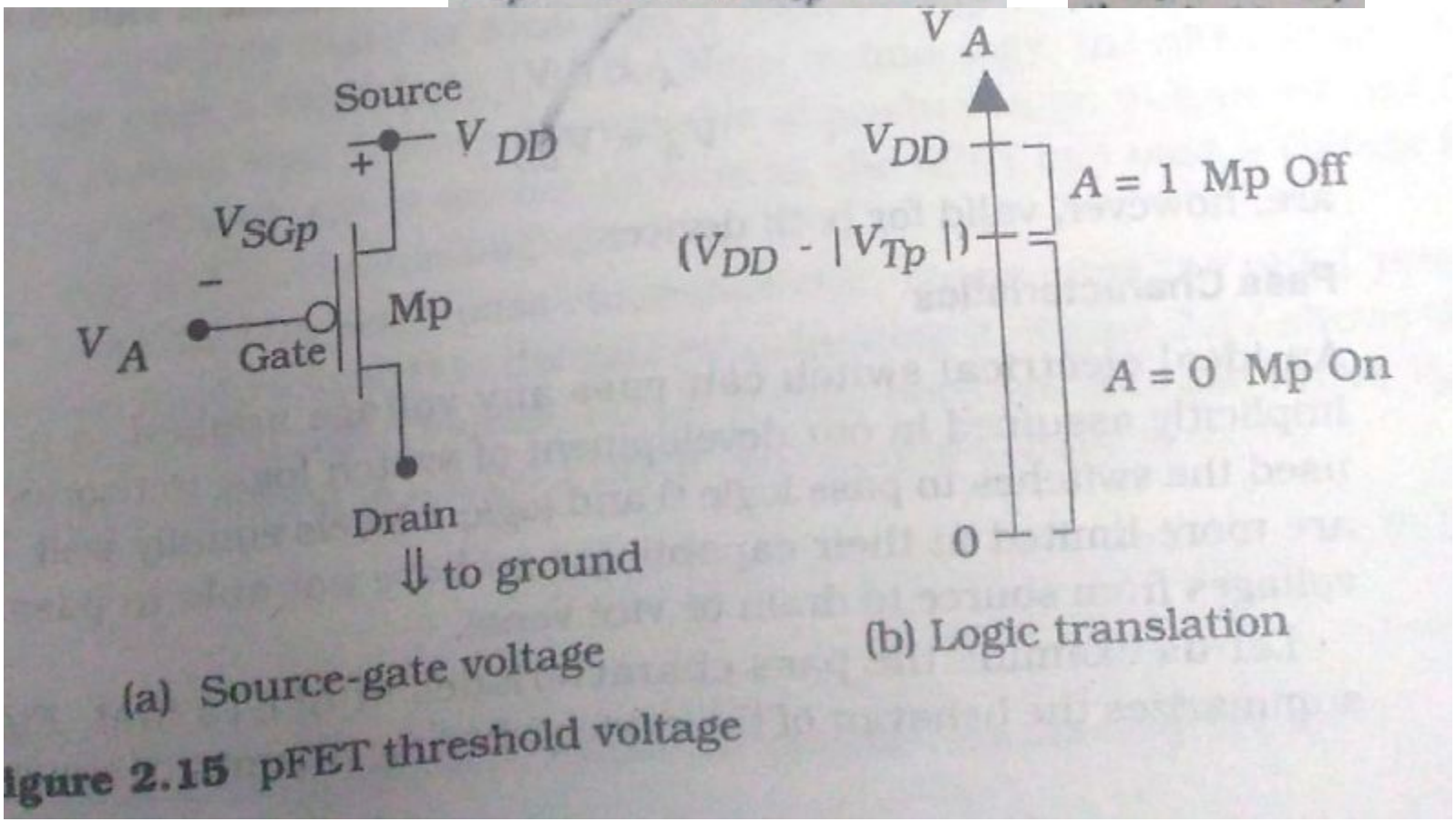
A=1

$V_A \geq V_{Tn}$

pFET

$V_{Tp} = -0.5$ V to $V_{Tp} = -0.8$ V.

$V_{SGp} = -V_{GSp}$



igure 2.15 pFET threshold voltage

Open Switch

$V_{SGp} \leq |V_{Tp}|$

Closed Switch

$V_{SGp} \geq |V_{Tp}|$

$V_A + V_{SGp} = V_{DD}$

$V_A = V_{DD} - V_{SGp}$

$V_{DD} - |V_{Tp}|$

Pass Characteristics

nFET

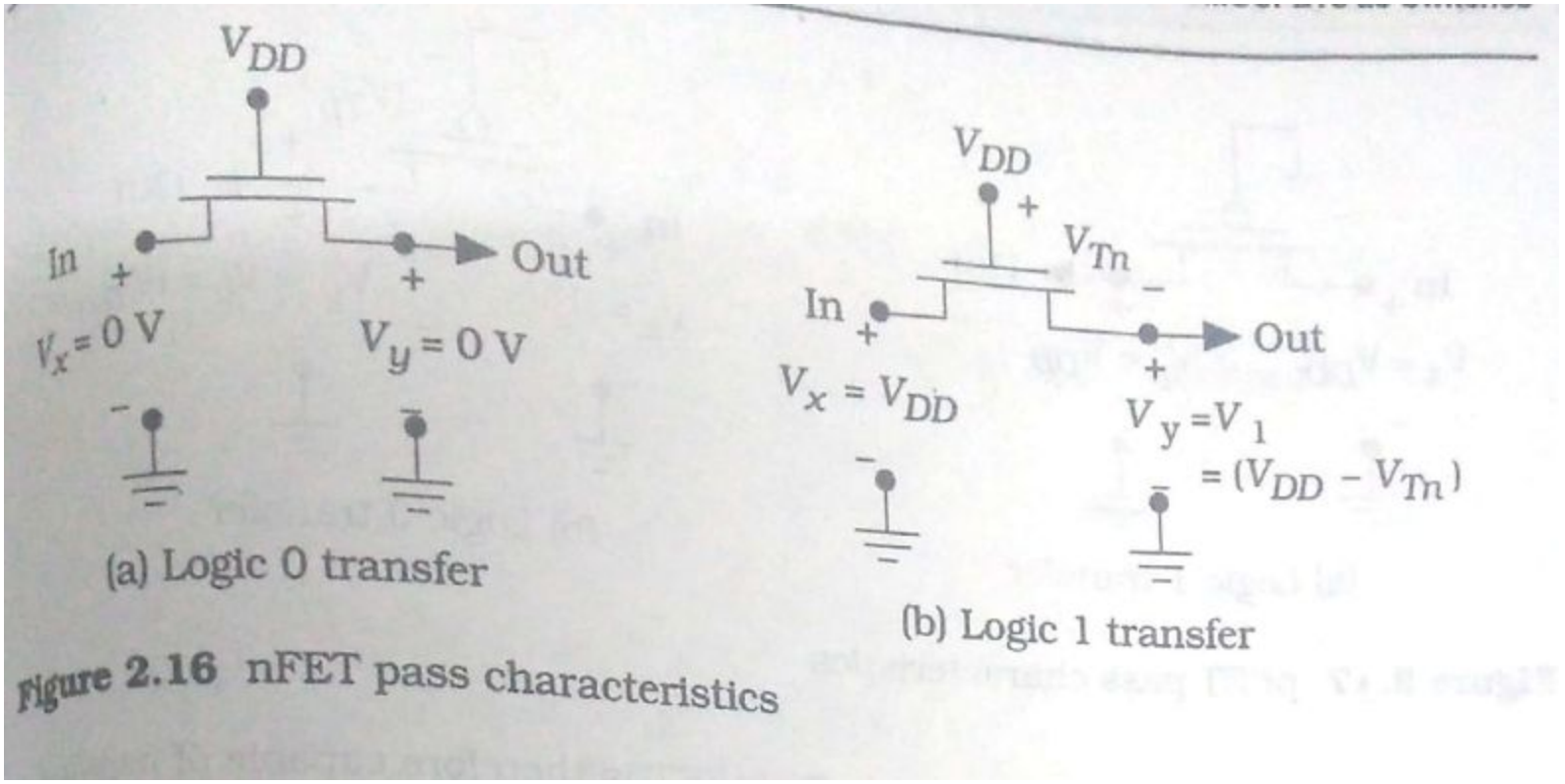


Figure 2.16 nFET pass characteristics

Threshold Voltage Loss

$$V_1 = V_{DD} - V_{Tn}$$

nFET can pass Weak logic 1 and strong logic 0

pFET

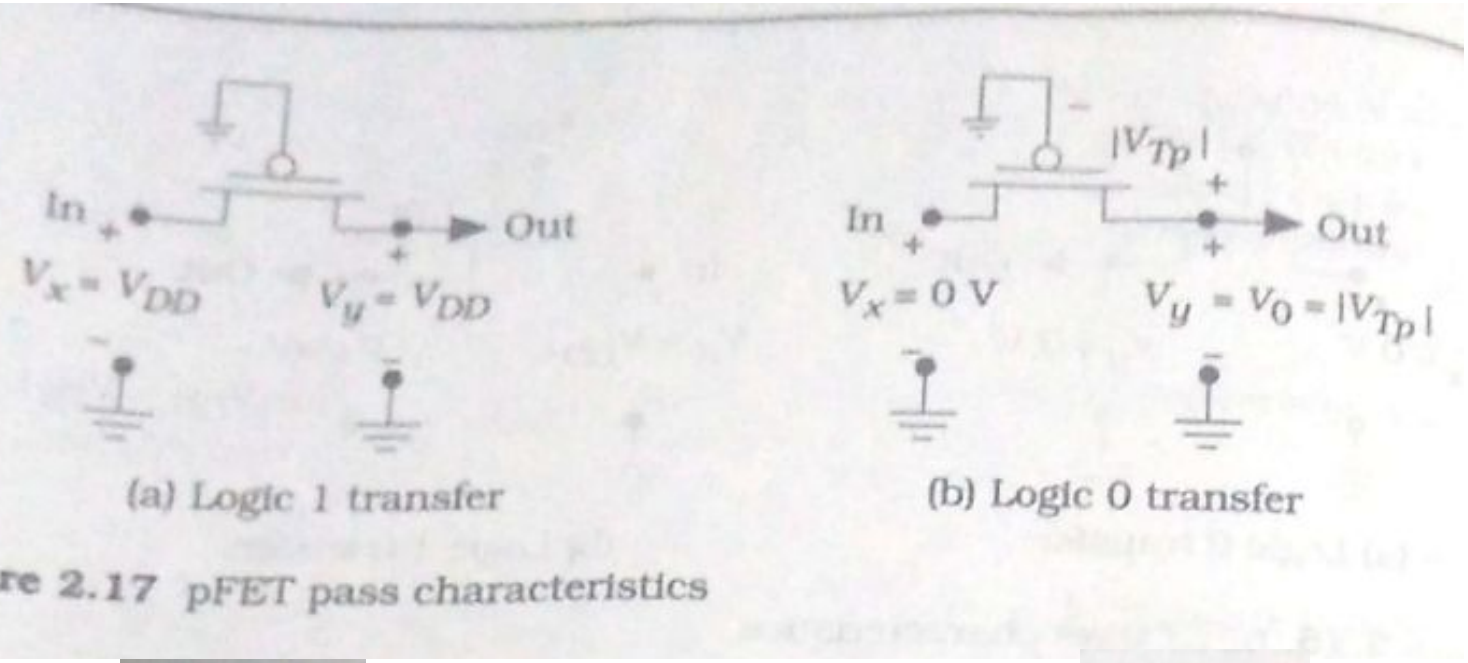


Figure 2.17 pFET pass characteristics

$V_y = V_{DD}$

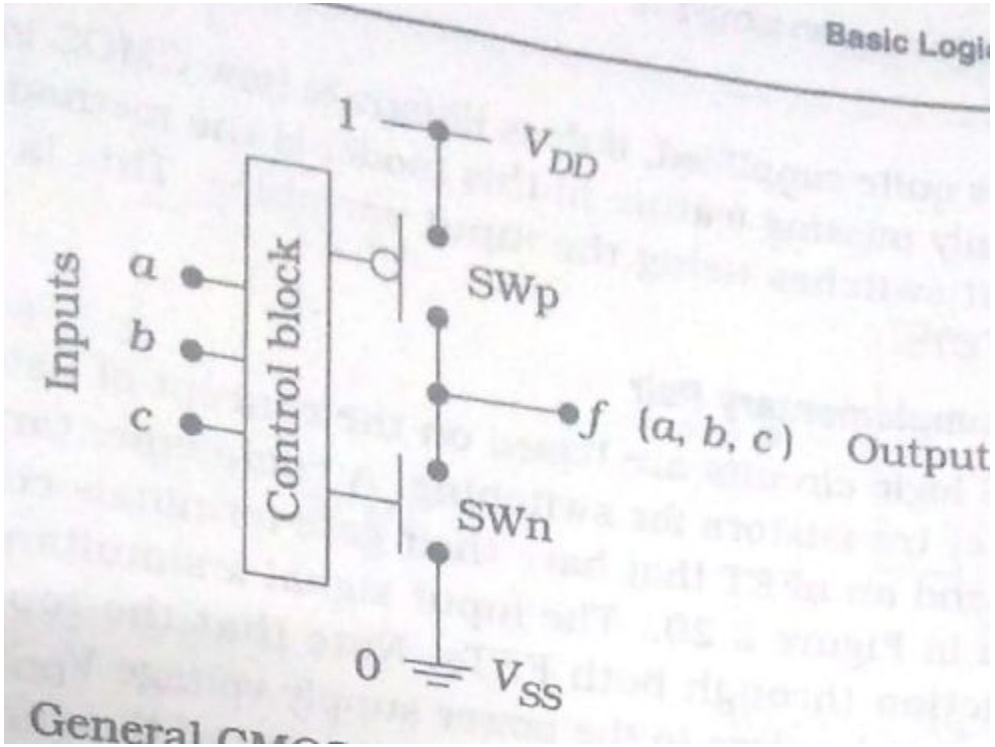
$V_y = |V_{Tp}|$

pFET can pass Weak logic 0 and strong logic 1

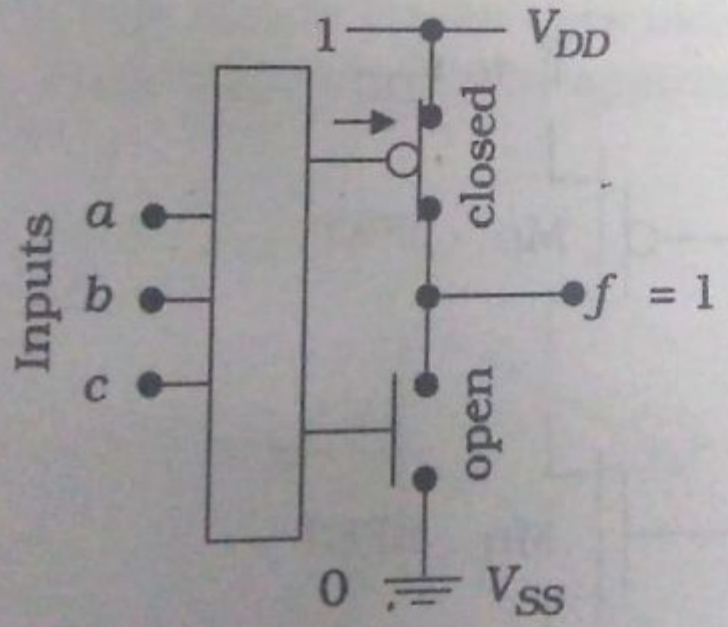
CMOS circuits are designed to account for the transmission levels.
The following rules are the basis for our design

1. Use pFETs to pass logic 1 voltages of VDD
2. Use nFETs to pass logic 0 voltages of VSS=0V

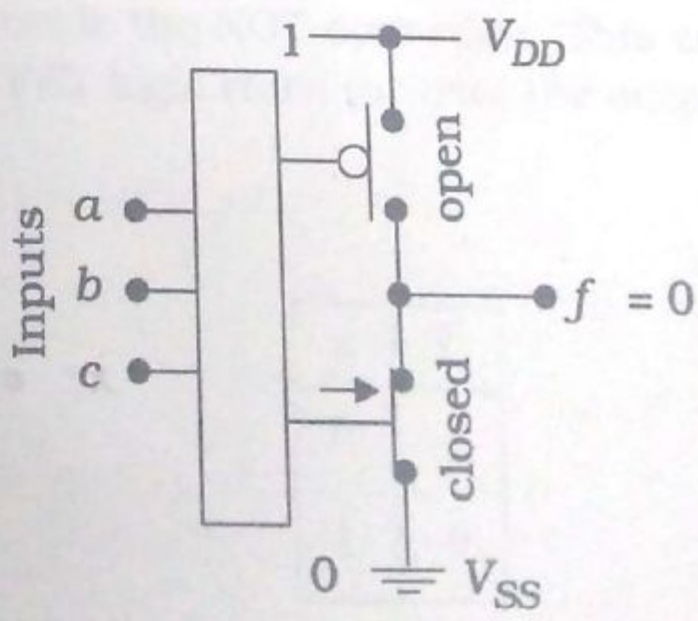
Basic Logic Gates in CMOS



General CMOS logic gate



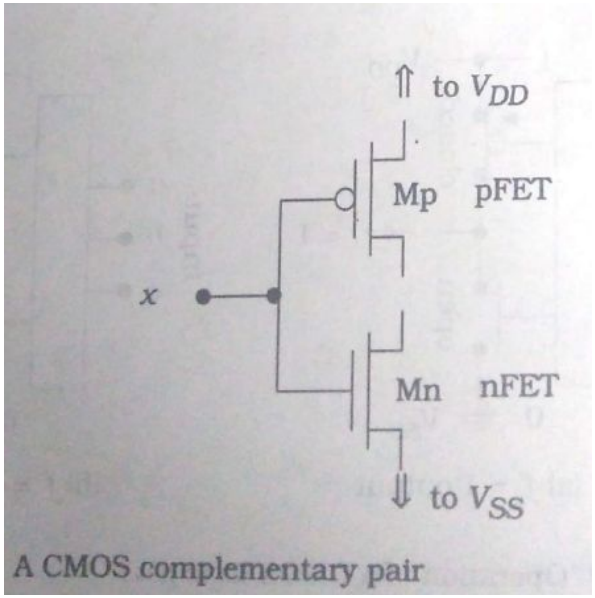
(a) $f = 1$ output



(b) $f = 0$ output

Figure 2.19 Operation of a CMOS logic gate

Complementary Pair



A CMOS complementary pair

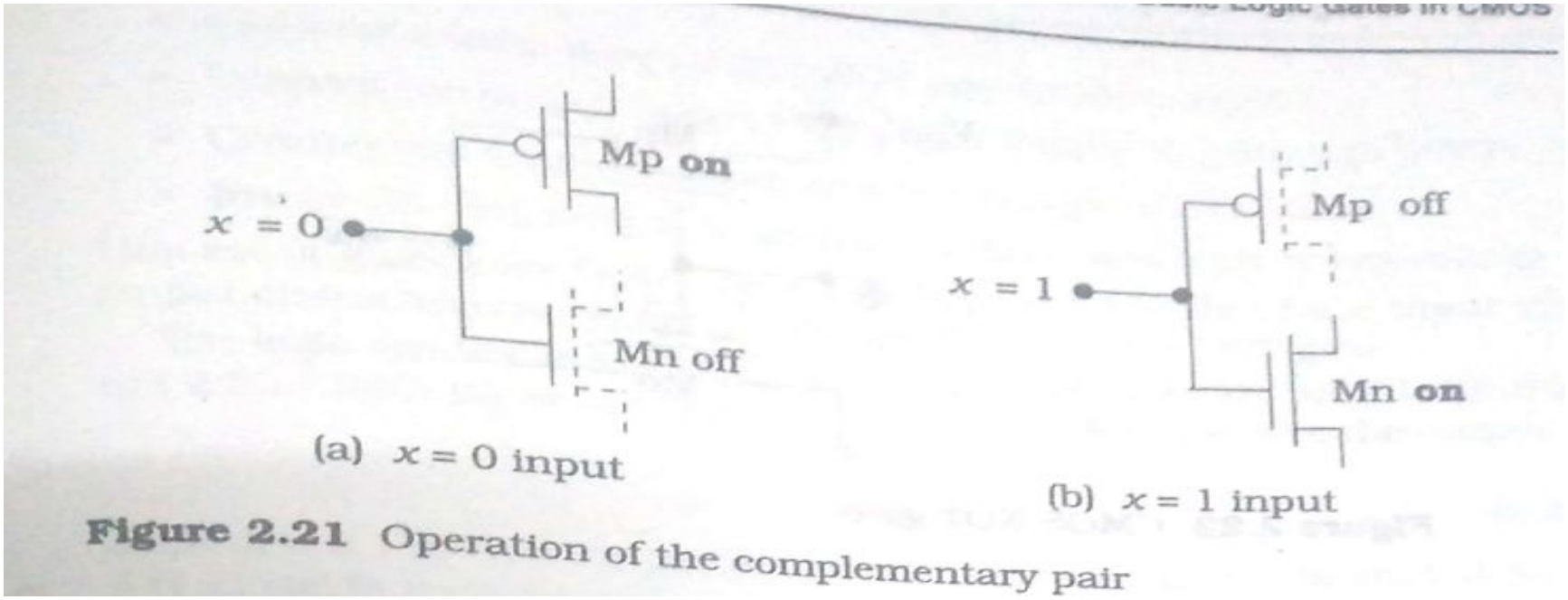
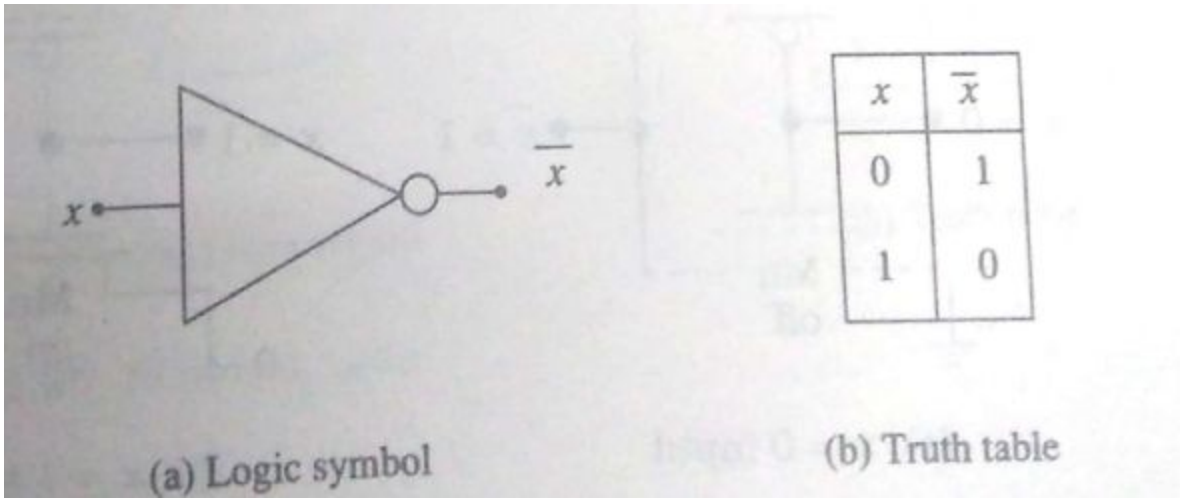


Figure 2.21 Operation of the complementary pair

NOT Gate

$$f(x) = \text{NOT}(x) = \bar{x}$$

If $x = 0$ then $\bar{x} = 1$
If $x = 1$ then $\bar{x} = 0$

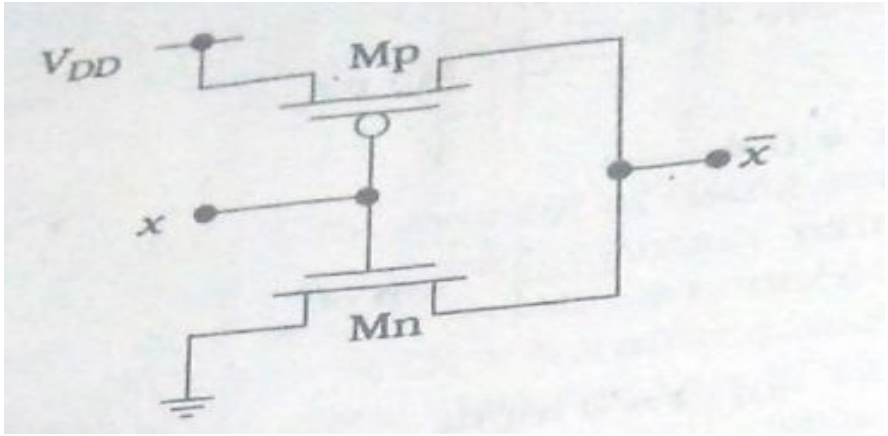


(a) Logic symbol

x	$\bar{x}$
0	1
1	0

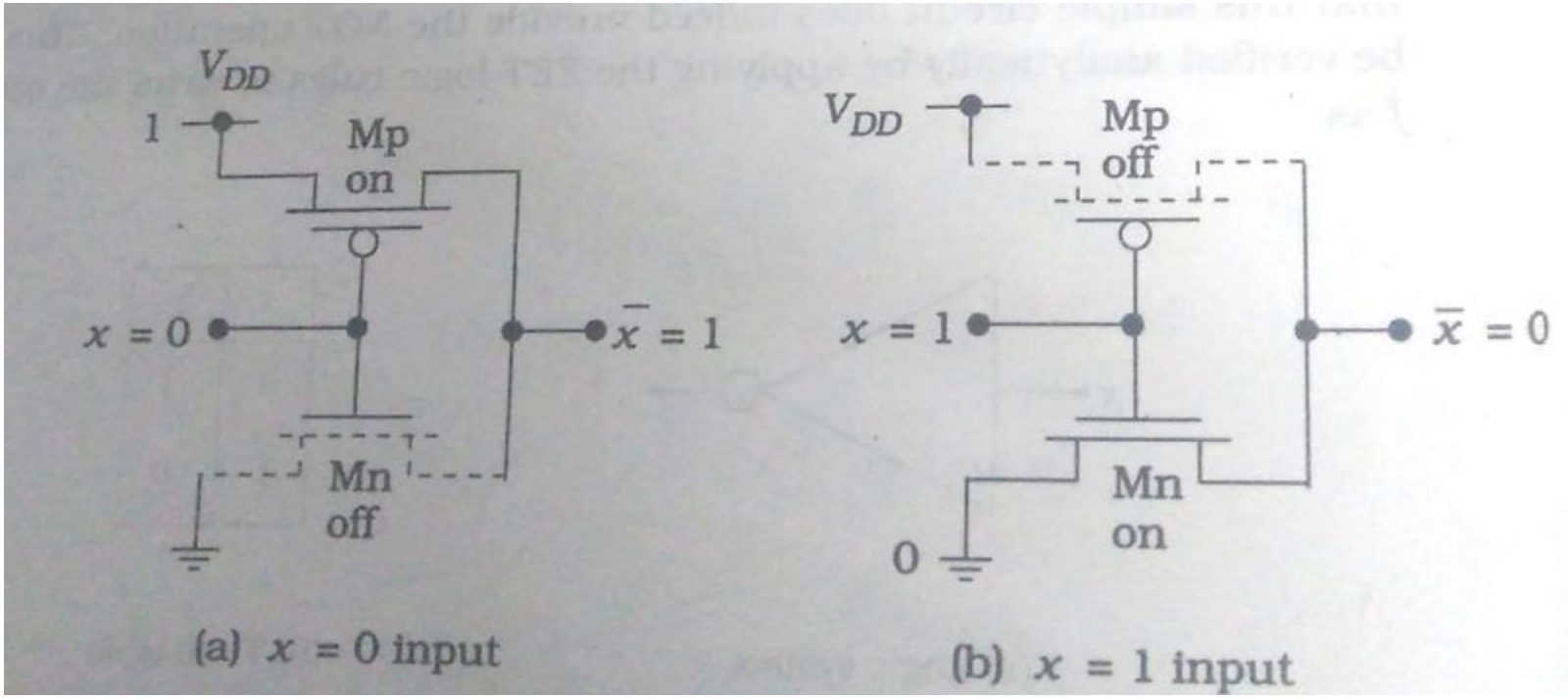
(b) Truth table

CMOS NOT Gate



$$f = \bar{x} \cdot 1 + x \cdot 0$$

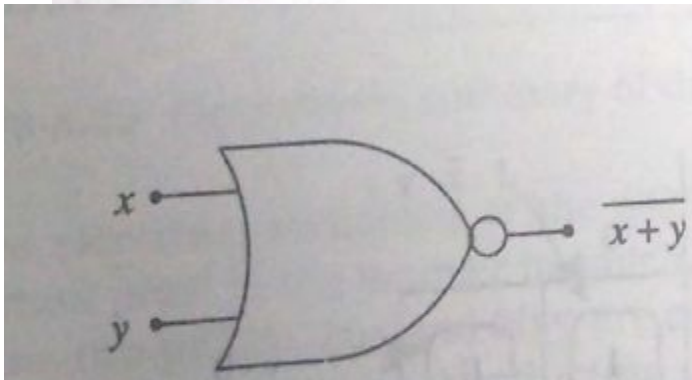
$$f = \bar{x}$$



CMOS NOR Gate

$g(x, y) = \overline{x + y}$

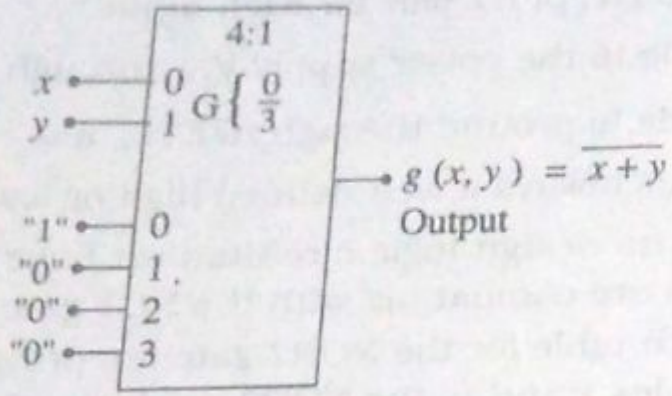
$g(x, y) = \bar{x} \cdot \bar{y} \cdot 1 + \bar{x} \cdot y \cdot 0 + x \cdot \bar{y} \cdot 0 + x \cdot y \cdot 0$



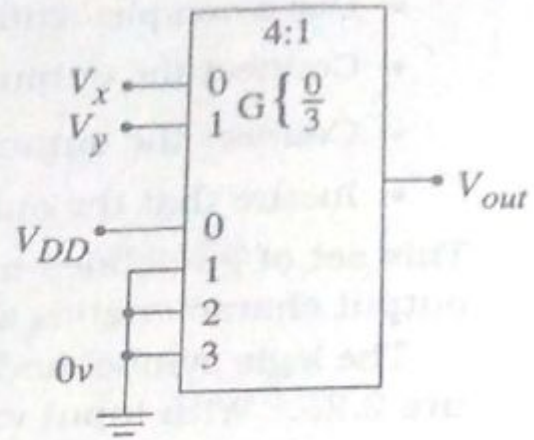
(a) Logic symbol

x	y	$\overline{x+y}$
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table

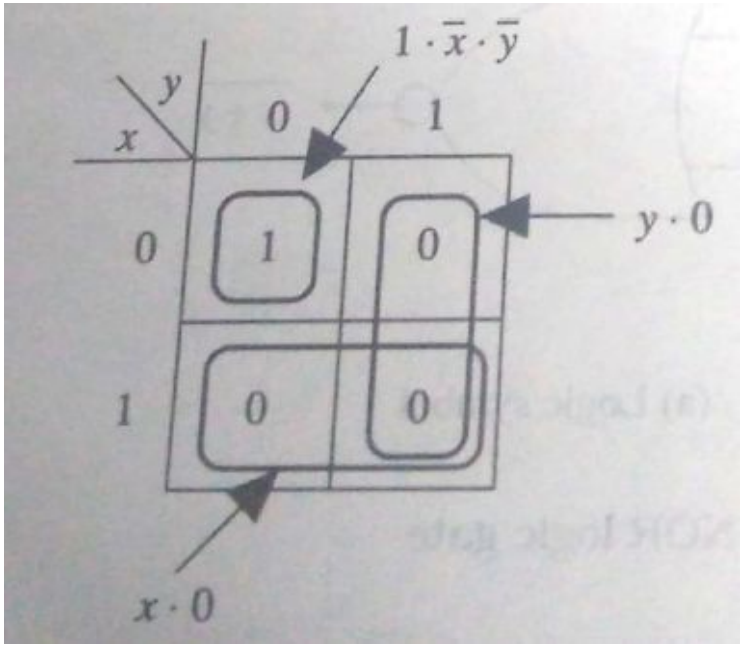


(a) Logic diagram

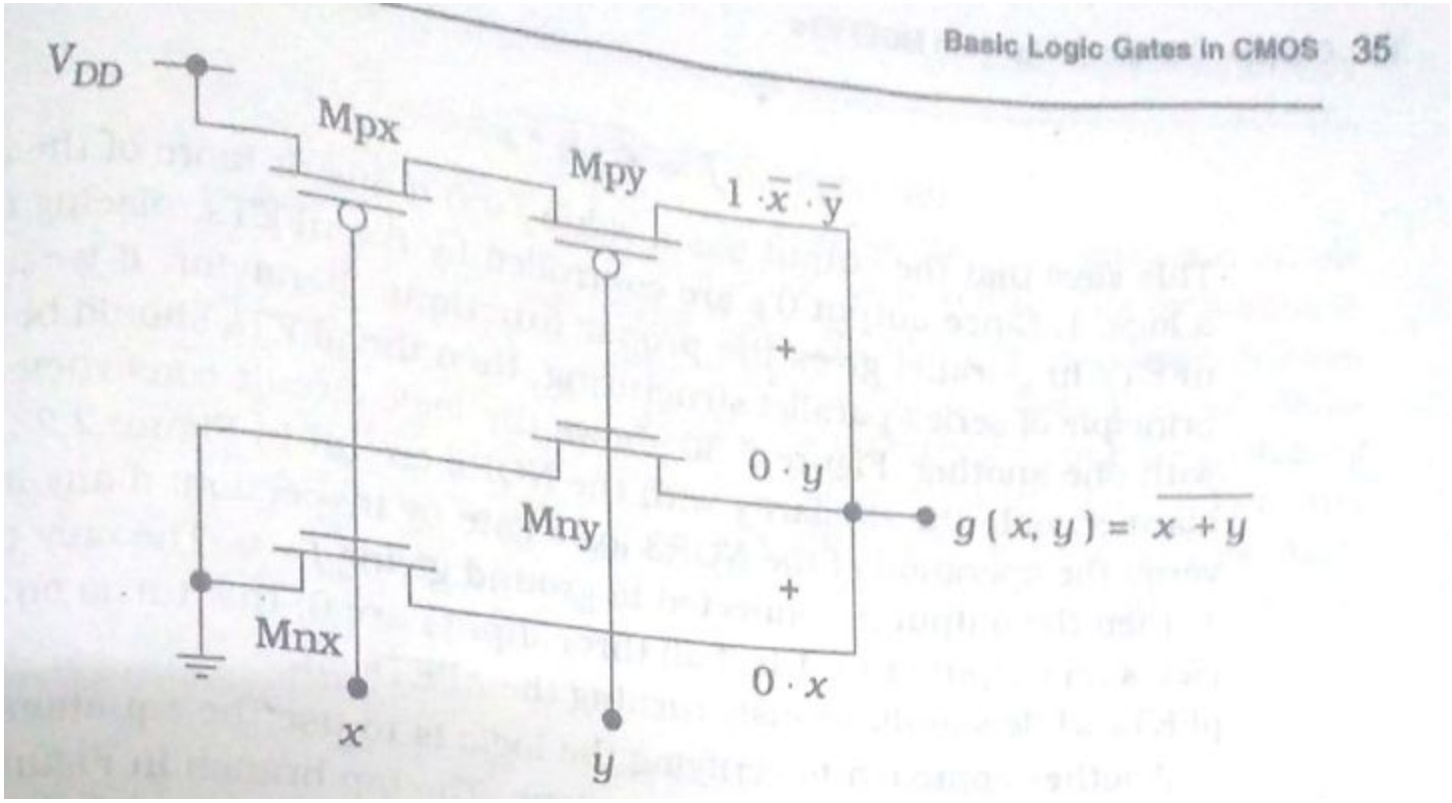


(b) Voltage network

NOR2 Operation

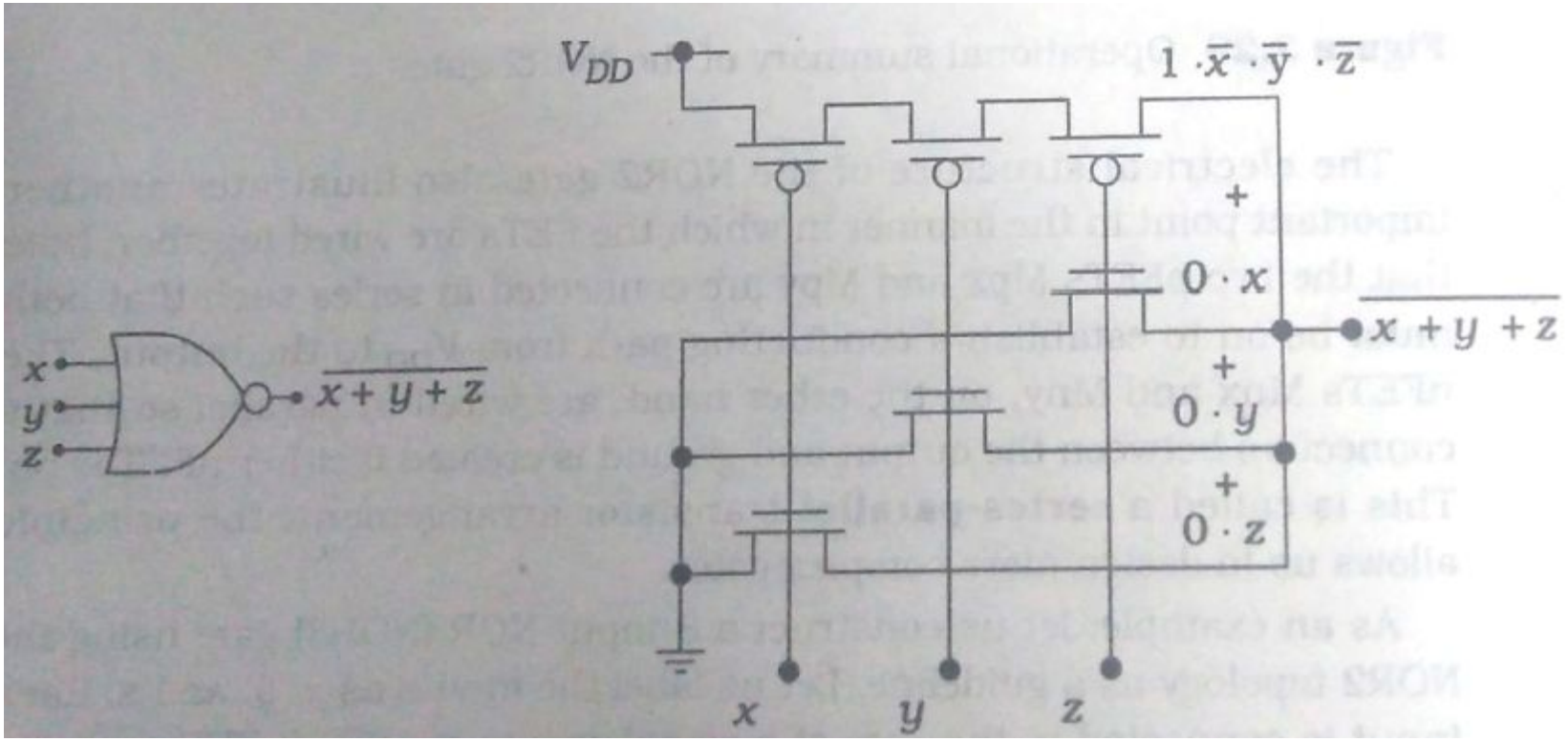


$$g(x, y) = \bar{x} \cdot \bar{y} \cdot 1 + x \cdot 0 + y \cdot 0$$



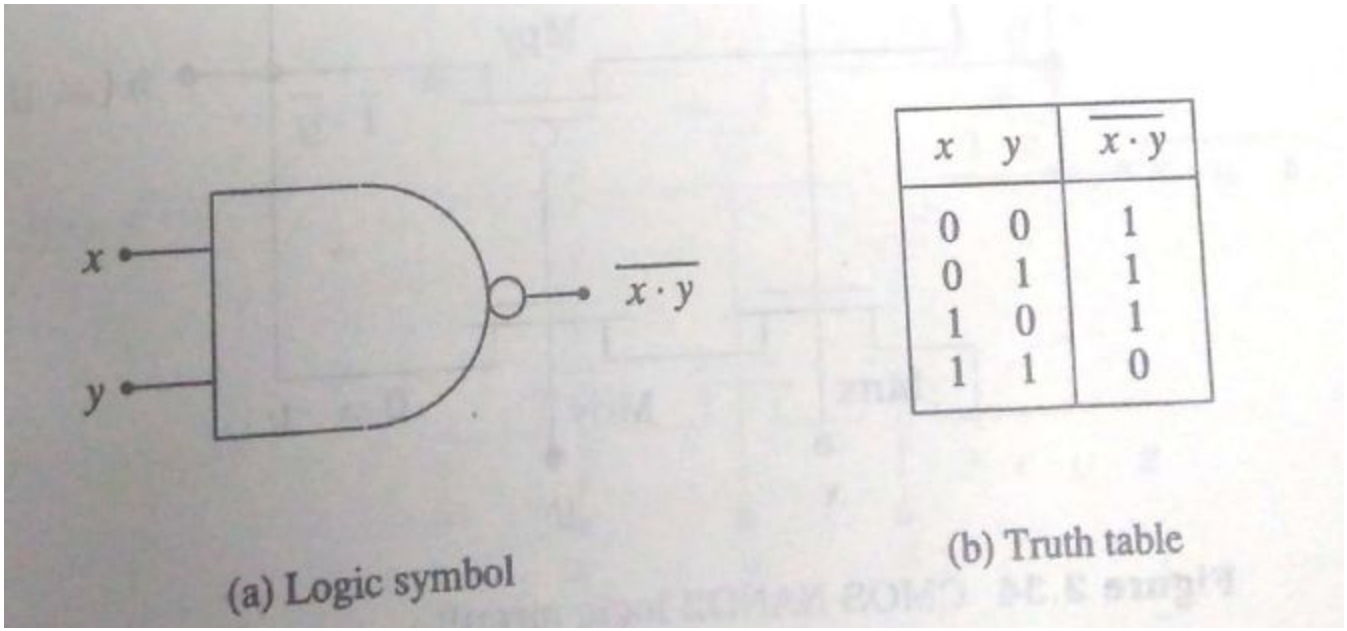
x	y	Mpx	Mpy	Mnx	Mny	g
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

NOR3 Logic Gates



CMOS NAND Gates

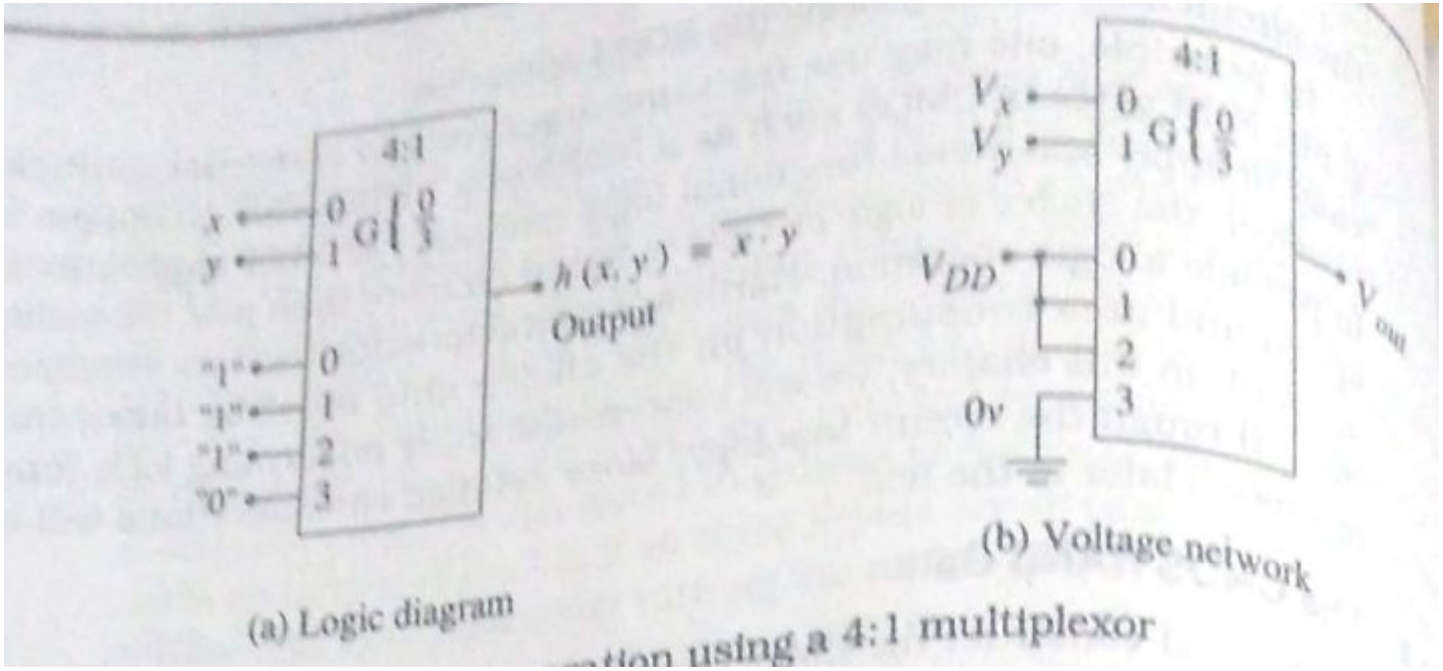
$$h(x, y) = \bar{x} \cdot \bar{y} \cdot 1 + \bar{x} \cdot y \cdot 1 + x \cdot \bar{y} \cdot 1 + x \cdot y \cdot 0$$



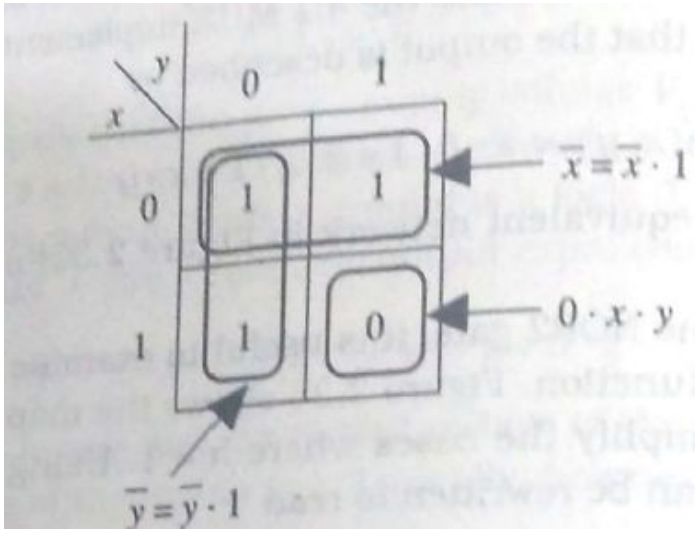
(a) Logic symbol

x	y	$\overline{x \cdot y}$
0	0	1
0	1	1
1	0	1
1	1	0

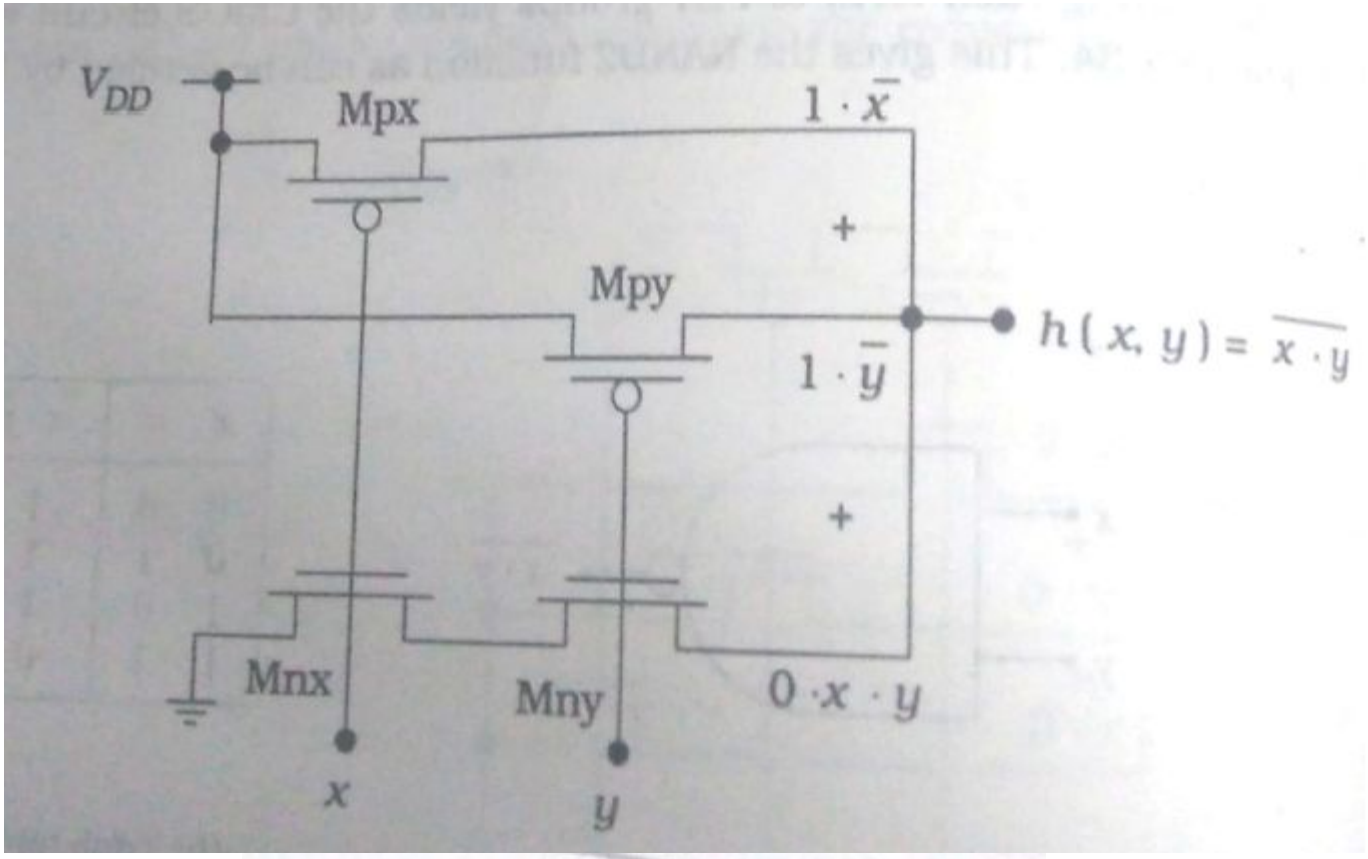
(b) Truth table



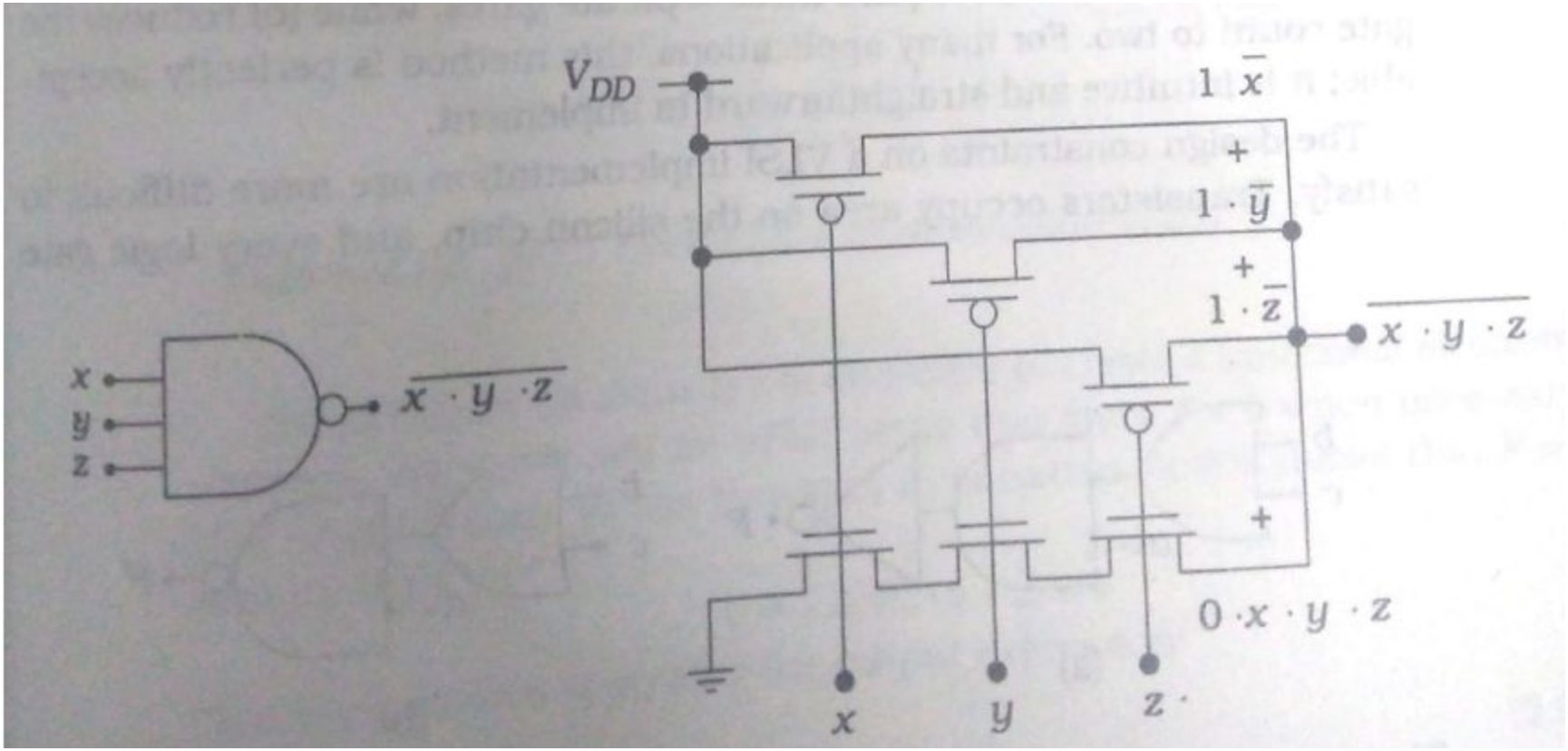
ation using a 4:1 multiplexor



$$h(x, y) = \bar{x} \cdot 1 + \bar{y} \cdot 1 + x \cdot y \cdot 0$$

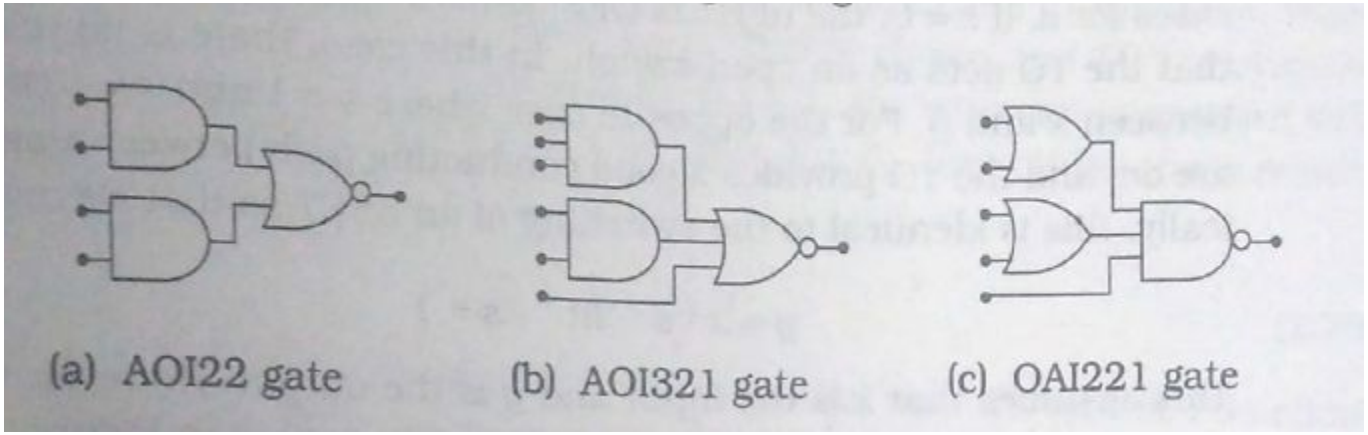


x	y	Mpx	Mpy	Mnx	Mny	h
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0


V_{DD}
$1 \cdot \bar{x}$
+
$1 \cdot \bar{y}$
+
$1 \cdot \bar{z}$
$\overline{x \cdot y \cdot z}$
+
$0 \cdot x \cdot y \cdot z$
x
y
z
$\overline{x \cdot y \cdot z}$
x
y
z

Complex Logic Gates in CMOS

Generalized AOI and OAI Logic Gates



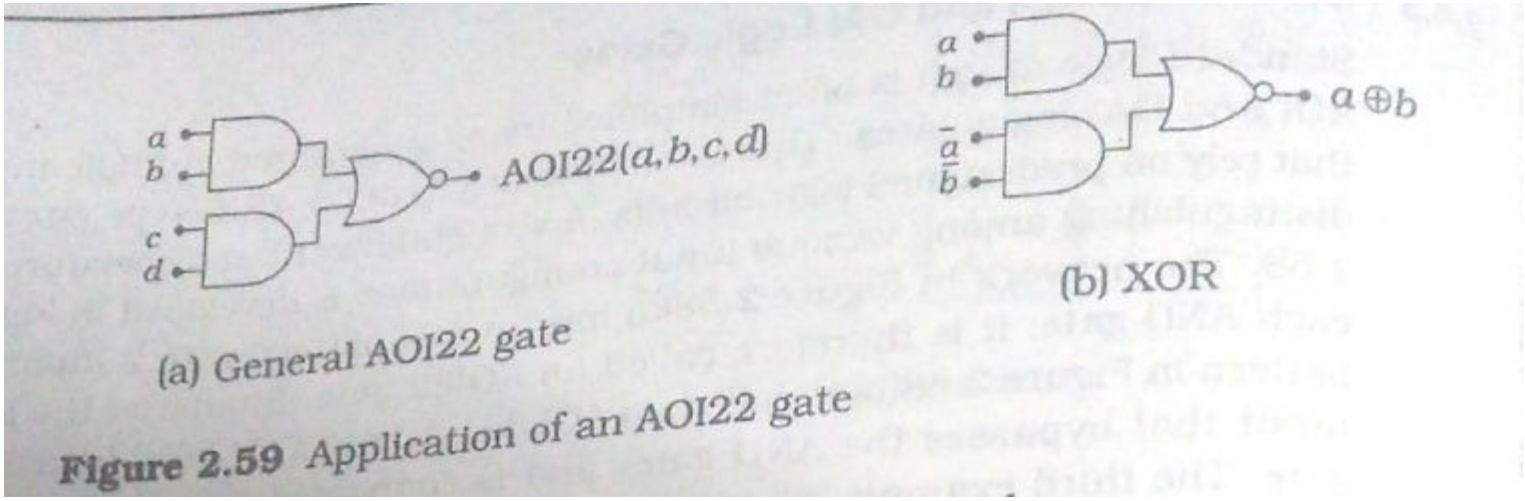
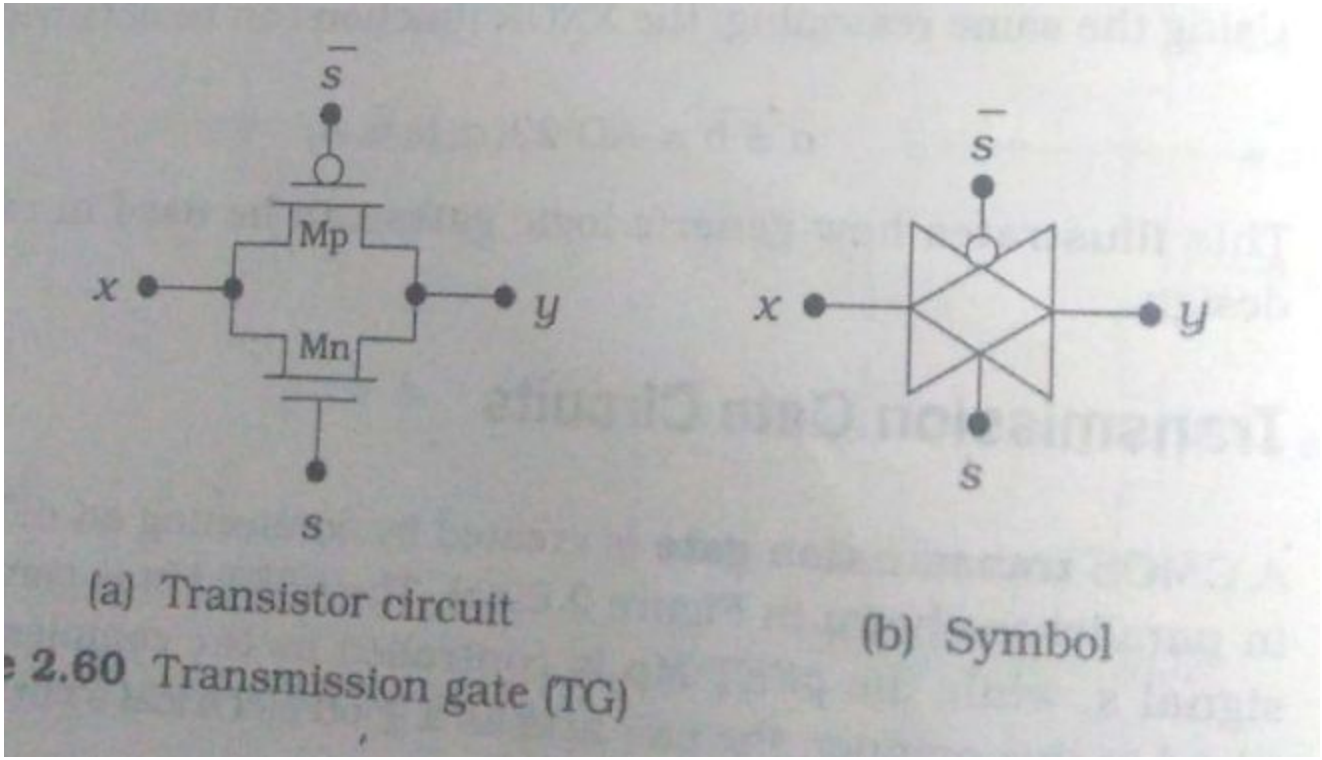


Figure 2.59 Application of an AOI22 gate

Transmission Gate Circuits



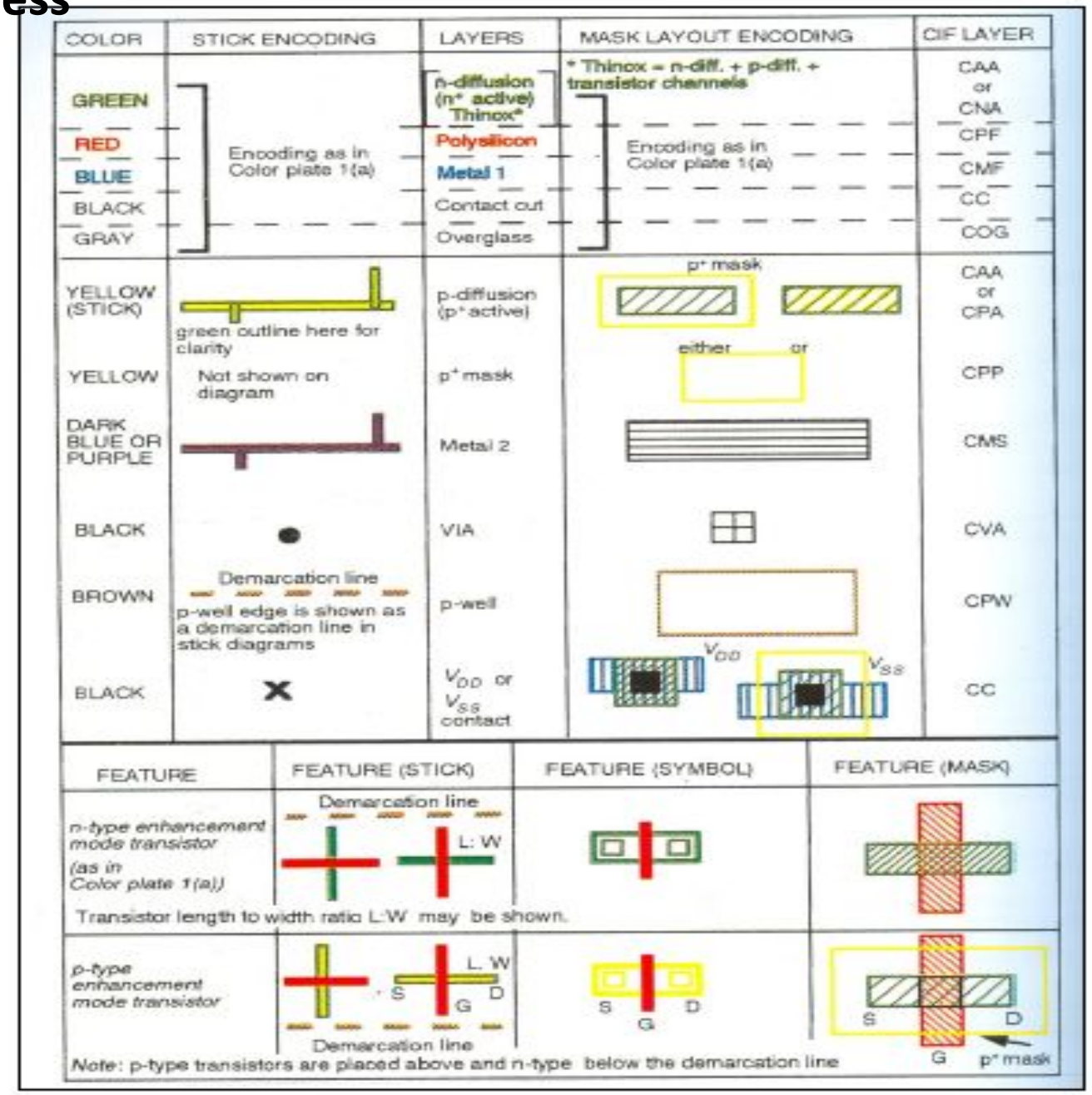
2.60 Transmission gate (TG)

nMOS process

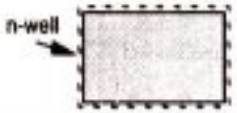
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	*Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

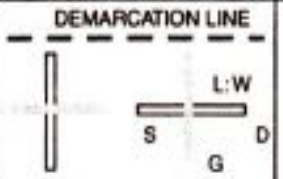
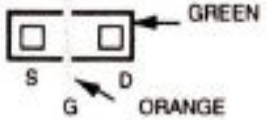
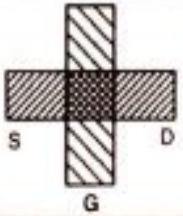
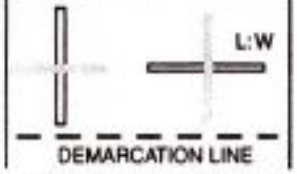
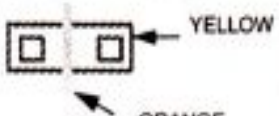
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	D, L: W, G, S; L: W, S, G, D	L: W, S, D, G	(L: W = 1:1), S, D, G
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only	L: W; L: W	L: W, S, G, D	(L: W = 1:1)
Source, drain and gate labelling will not normally be shown.			

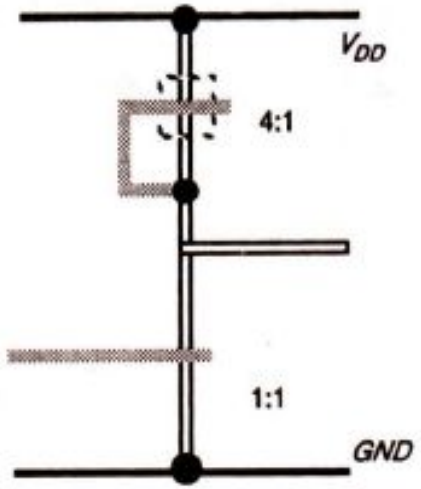
CMOS process



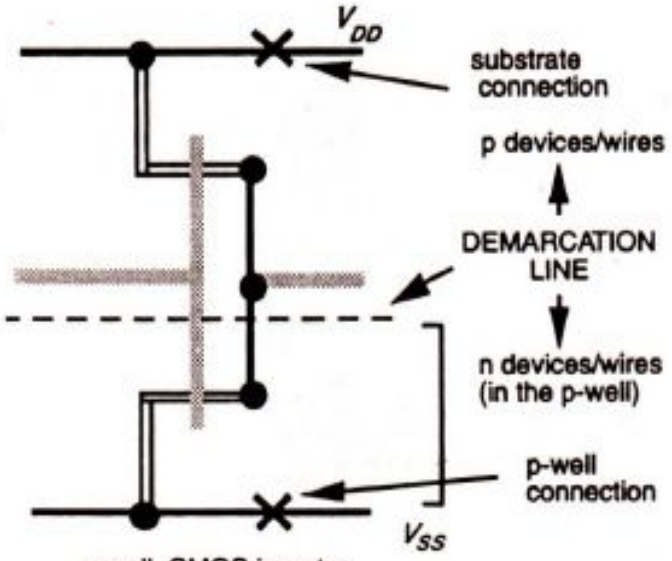
BiCMOS process

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE	MONOCHROME 	Polysilicon 2	MONOCHROME 	CPS
SEE COLOR PLATE 1(c)		Bipolar npn transistor	see Figure 3–13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor		CCA

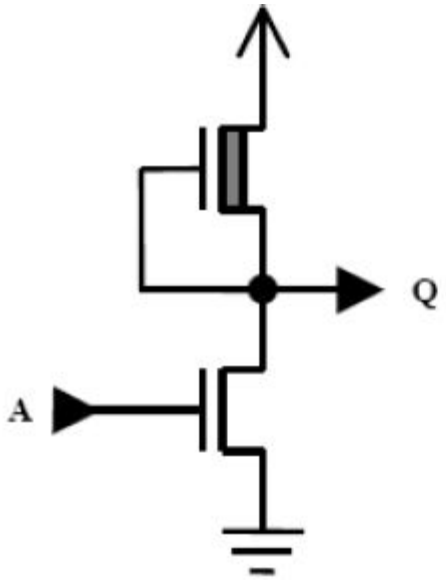
FEATURE	FEATURE (STICK) (MONOCHROME)	FEATURE (SYMBOL) (MONOCHROME)	FEATURE (MASK) (MONOCHROME)
n-type enhancement poly 2 transistor			
Transistor length to width ratio L:W may be shown.			
p-type enhancement poly 2 transistor			
Note: p-type transistors are placed above and n-type transistors below the demarcation line.			
npn bipolar transistor			See Figure 3–13(f) and Color plate 6

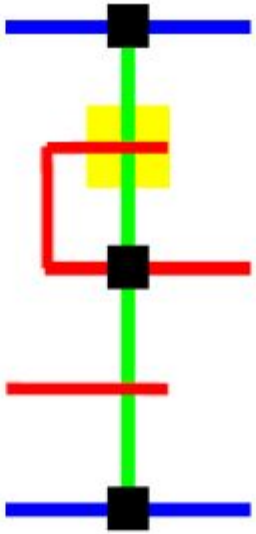


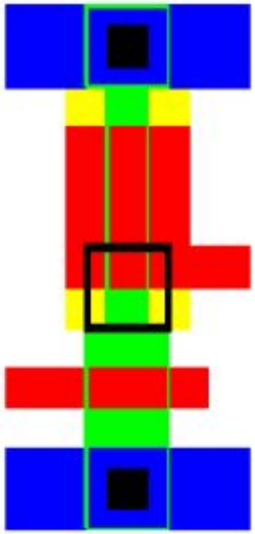
4:1 nMOS inverter

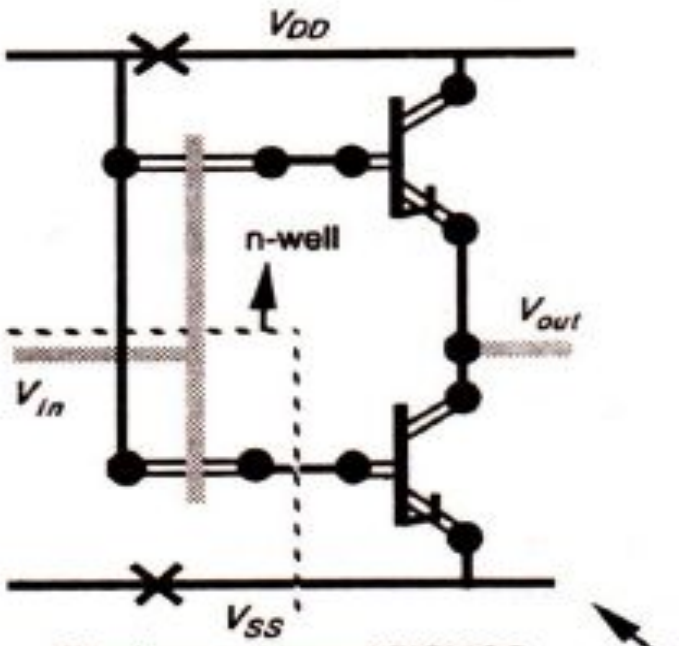


p-well CMOS inverter



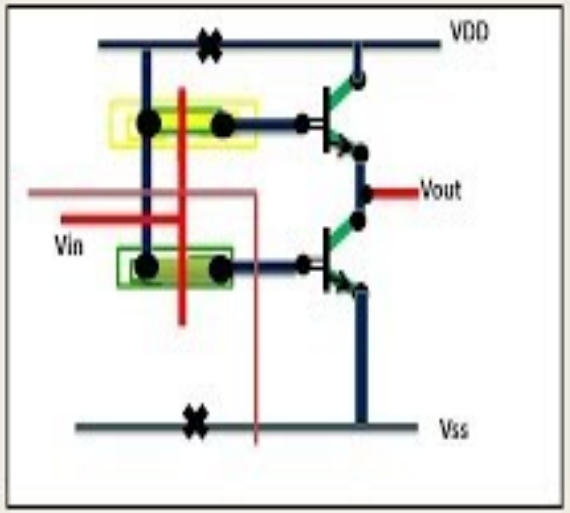






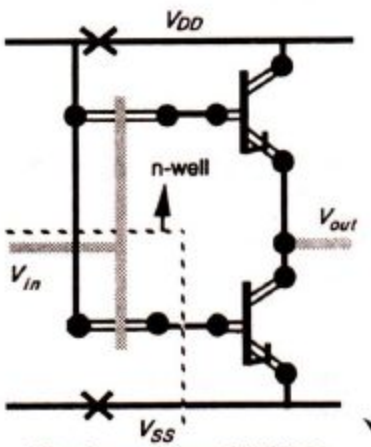
Simple n-well based BiCMOS inverter (stick diagram)

BiCMOS Inverter stick diagram

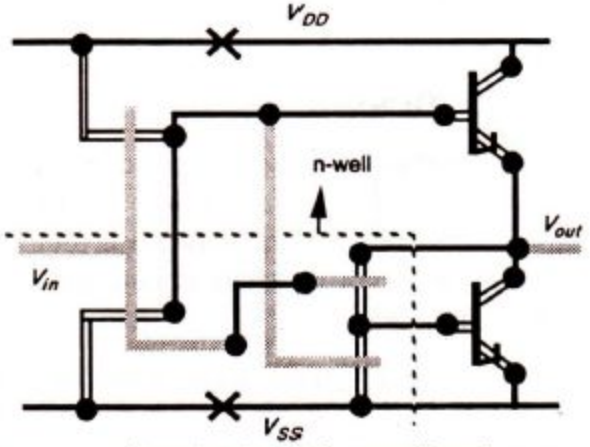


(हिन्दी)

V L S I



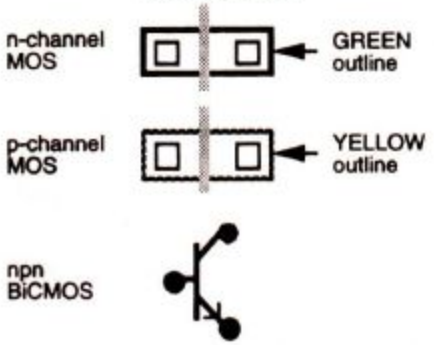
Simple n-well based BiCMOS inverter (stick diagram)



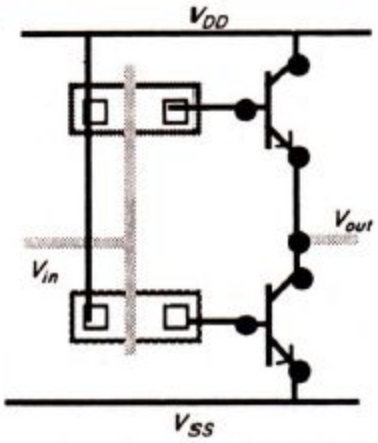
Alternative design of an n-well based BiCMOS inverter

SIMPLE SYMBOLIC NOTATION

TRANSISTORS



Wires etc. as for stick diagrams



Simple n-well based BiCMOS inverter (symbolic diagram)

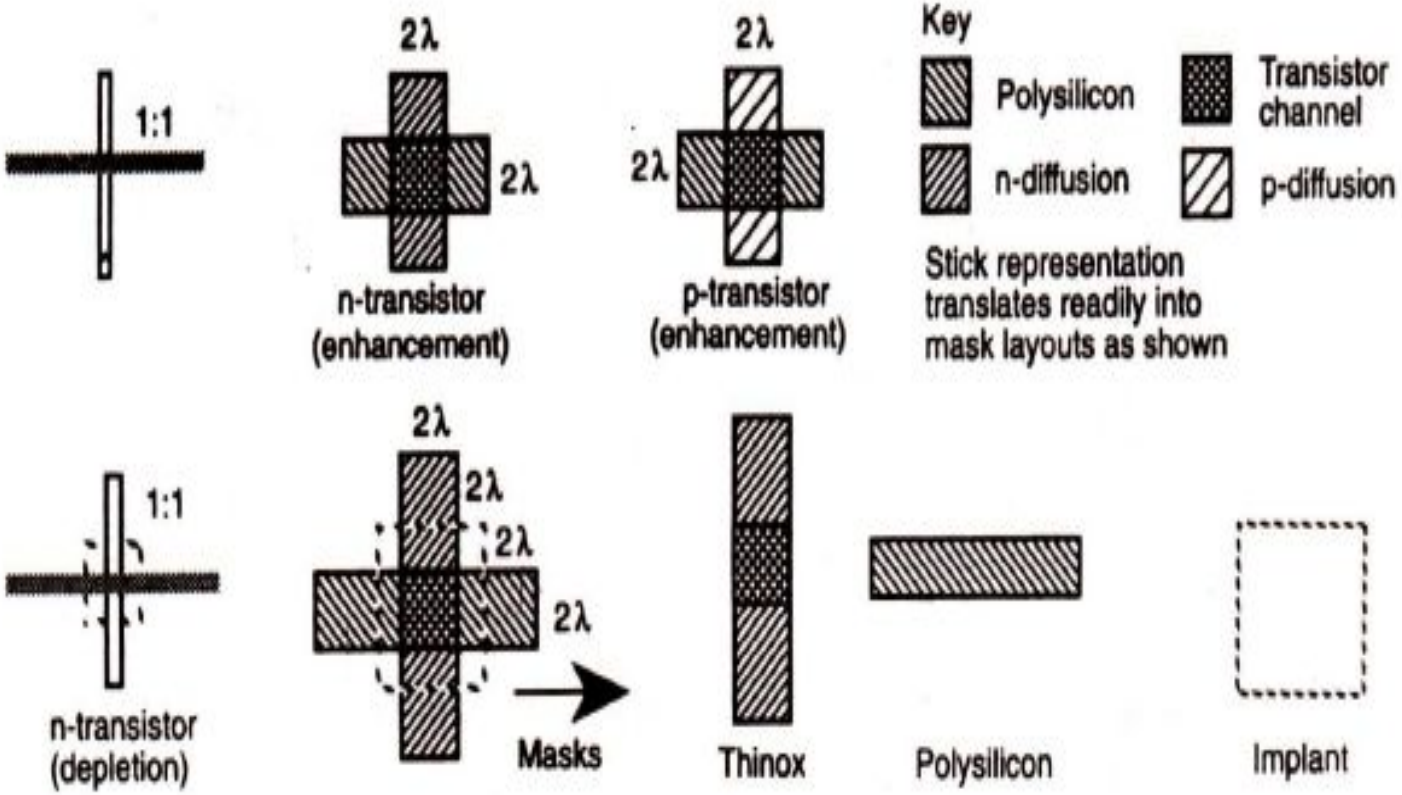


FIGURE 3.2 Stick diagrams and corresponding mask layout examples.

nMOS Design Style

The layout of nMOS involves

1. n-diffusion and other thinoxide regions –green
2. Polysilicon 1-red
3. Metal 1-blue
4. Implant-yellow
5. Contacts-black or brown

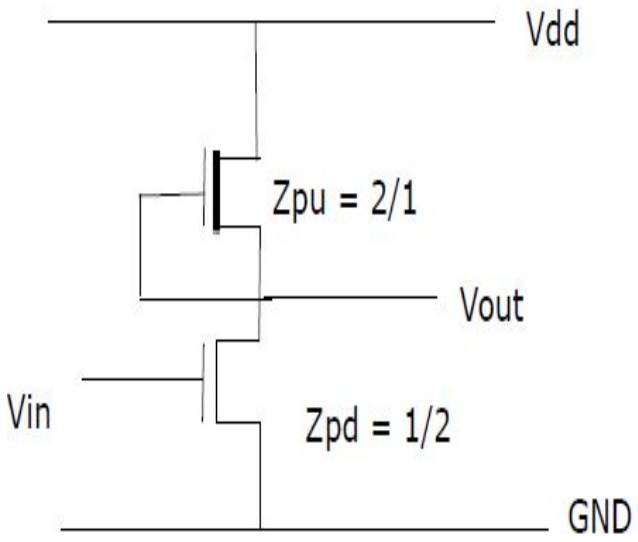
The Transistor is formed wherever poly crosses n-diffusion (red over green)and all diffusion wire(interconnection)a re n-type(green)

Steps for Layout

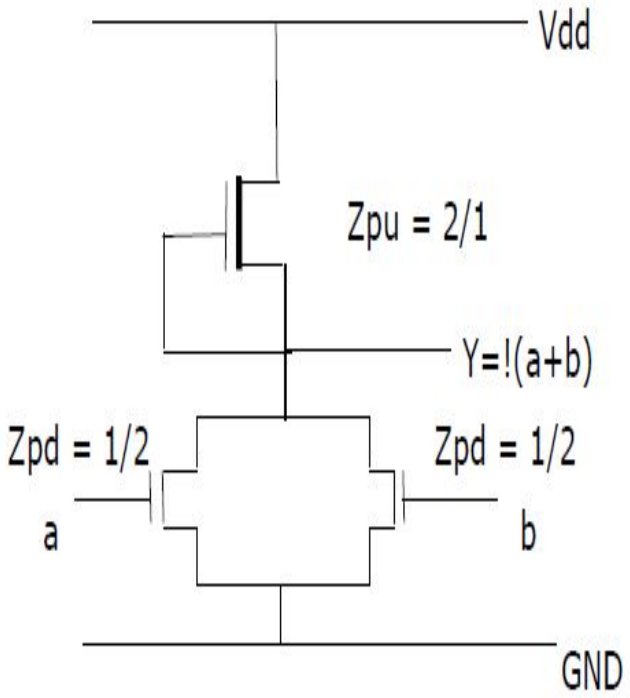
- Draw the meta(blue) VDD and GND rails
- Thinox(green) paths may be drawn between rails for inverters
- Depletion mode transistors connected from output point to VDD and pull-down structure of enhancement mode connected between output and GND
- Implants for depletion mode transistor
- Signal paths may also be switched by pass transistor
- Leaf-cell boundaries are conveniently shown on stick diagram

Examples

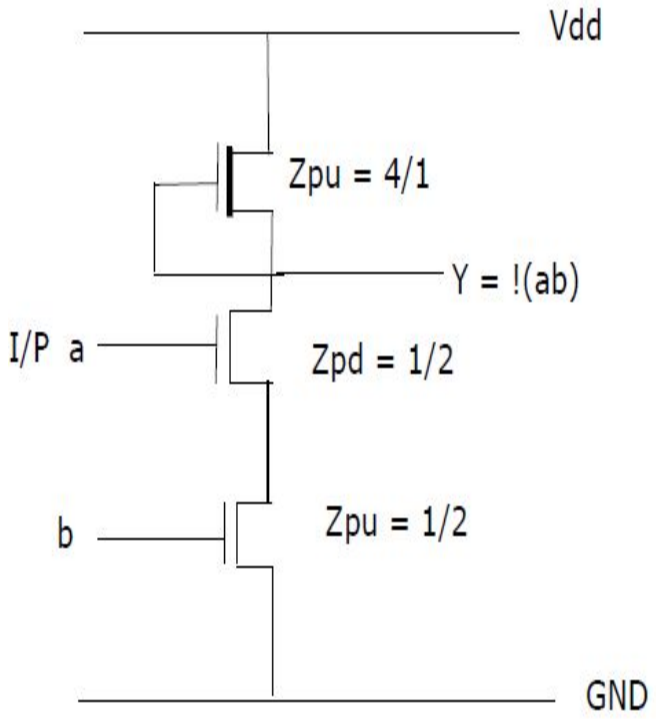
nMOS Inverter



nMOS Depletion load NOR

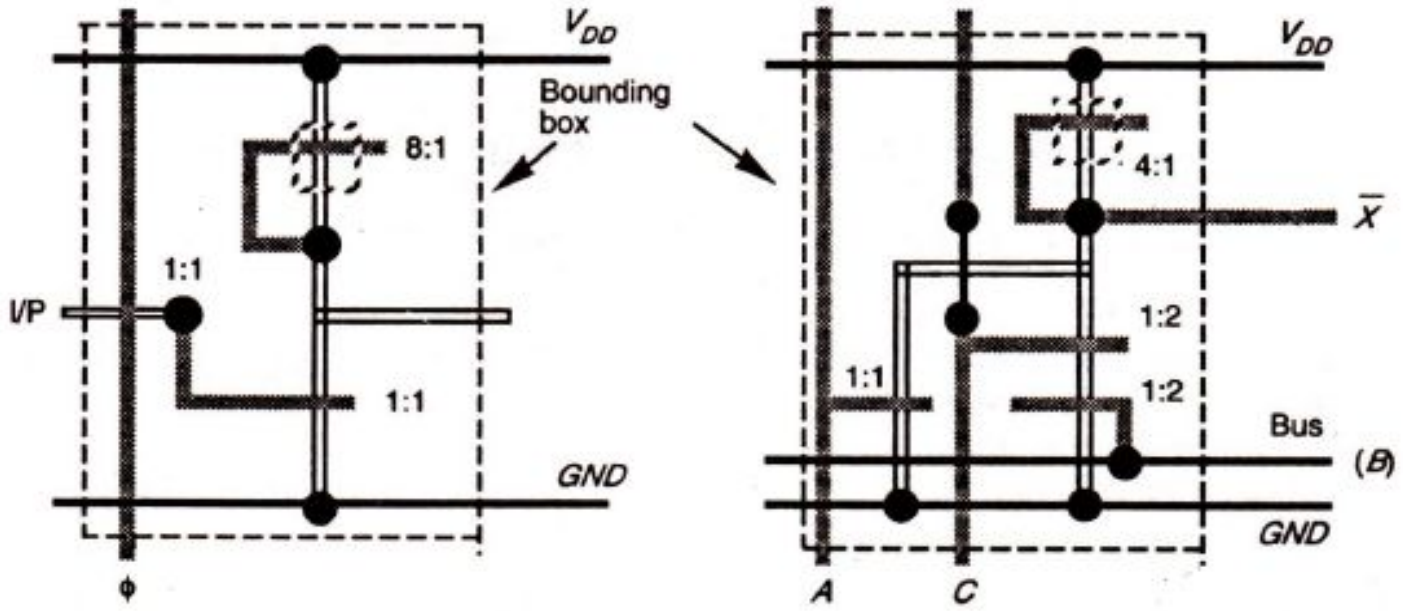


nMOS Depletion load NAND



nMOS Depletion load for function f=(xy+z)’

Buses, Control Signals, Interconnections and leaf Boundaries



CMOS DESIGN STYLE

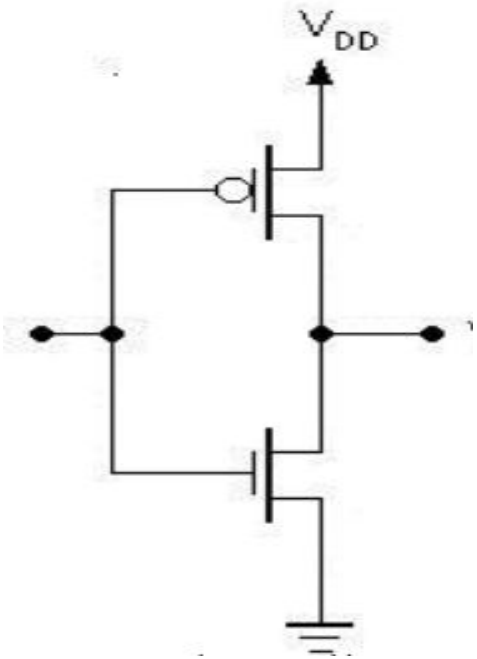
CMOS stick Diagram Basic steps

- Steps for CMOS are similar to NMOS
- But one difference is that depletion mode FETs are not used.
- Here, yellow/ brown is used to identify PMOS.
- The two types of FET, n and p, are separated in the diagram by the demarcation line.
- This line represents the well (n/p-well).
- Above this line are all p-type MOSFETs.
- Below this line n-type MOSFET are present.

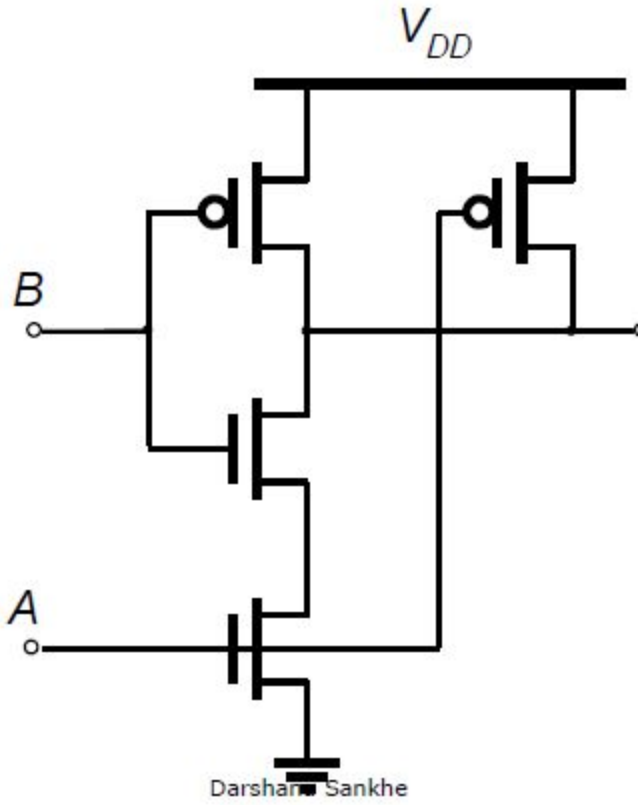
- No Diffusion can cross demarcation line.
- Only poly and metal can cross demarcation line
- N-diffusion and p-diffusion are joined using a metal wire.
- First step is to draw two parallel rails for VDD and GND.
- Next draw a demarcation line (brown)
- Place all PMOS above and NMOS below this line.
- Connect them using wires (metal).

Examples

CMOS INVERTER

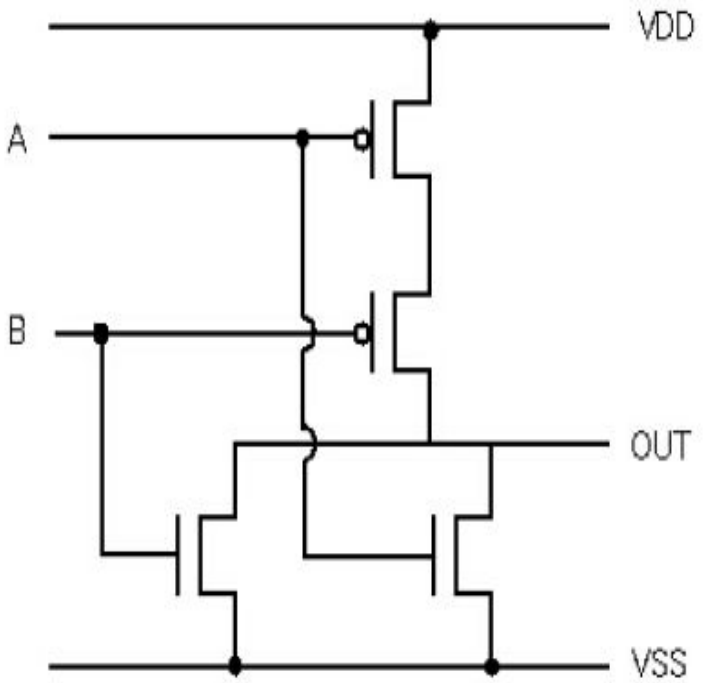


CMOS NAND



Darshan Sankhe

CMOS NOR



NOR gate in CMOS

Types of Design Rules

1. **Industry Standard: Micron Rule**

- All device dimensions are expressed in terms of absolute dimension(µm/nm)
- These rules will not support proportional scaling

2. λ Based Design Rules :

- Developed by Mead and Conway.
- All device dimensions are expresses in terms of a scalable parameter λ.
- λ = L/2; L = The minimum feature size of transistor
- L = 2 λ
- These rules support proportional scaling.
- They should be applied carefully in sub-micron CMOS process

λ Based Design Rules

- In MOS, the minimum feature size of Tr is:
  - (L/W)n = 1/1 = 2
  - λ/2 λ Active area = L*W = 4 λ2
- In CMOS, the minimum feature size of Tr is:
  - (L/W)n = 1/1.5 = 2 λ/3 λ
  - Active area = L*W = 6 λ2
- Minimum length or width of a feature on a layer is **2**λ
  - To allow for shape contraction
- Minimum separation of features on a layer is 2λ
  - To ensure adequate continuity of the intervening materials.

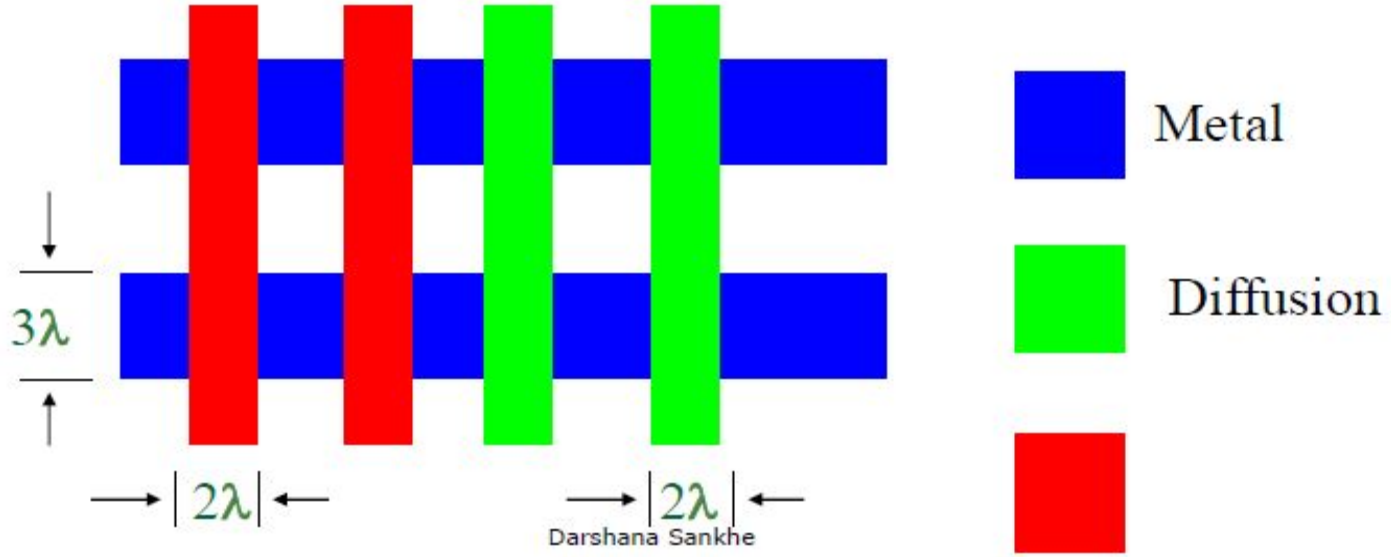
Design Rules

Two Features on different mask layers can be misaligned by a maximum of 2λ on the wafer.

- If the overlap of these two different mask layers can be catastrophic to the design, they must be separated by at least 2λ
- If the overlap is just undesirable, they must be separated by at least λ

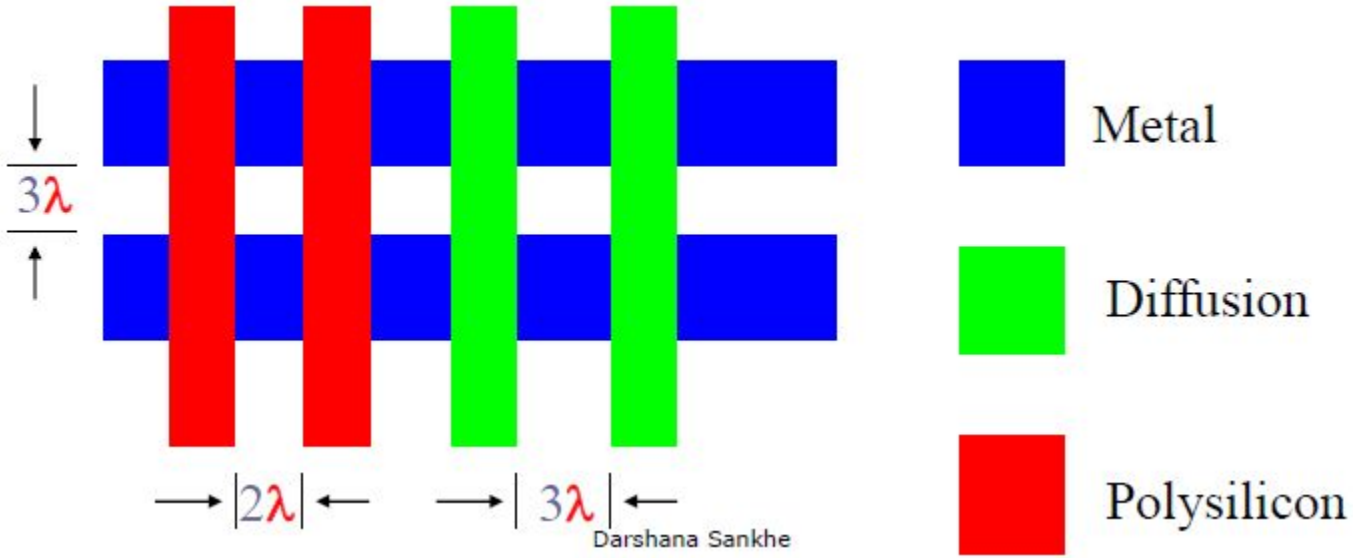
Design rules: NMOS

- Minimum width of PolySi and diffusion line **2**λ
- Minimum width of Metal line **3**λ as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



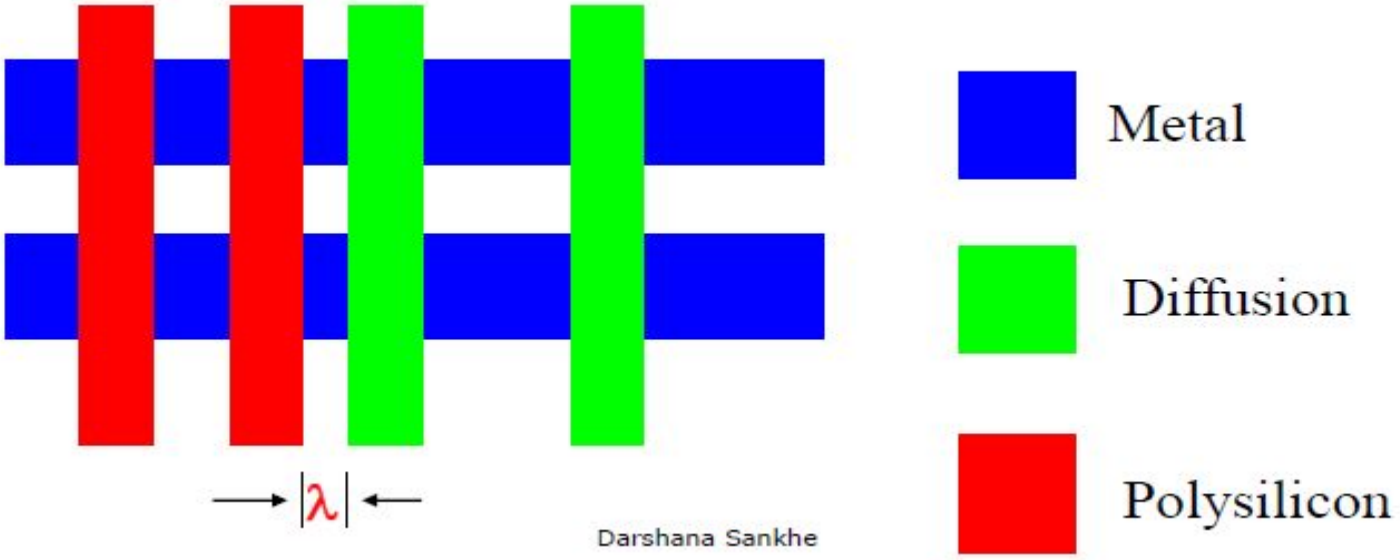
Design rules: NMOS

- PolySi – PolySi spacing 2λ
- Metal - Metal spacing 3λ
- Diffusion – Diffusion spacing 3λ : To avoid the possibility of their associated regions overlapping and conducting current



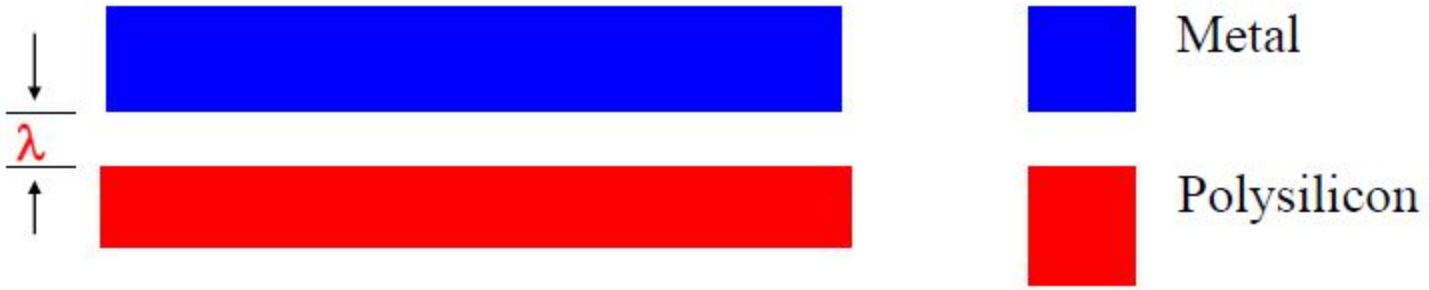
Design rules: NMOS

- Diffusion – PolySi spacing λ: To prevent the lines overlapping to form unwanted capacitor.
- Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross.



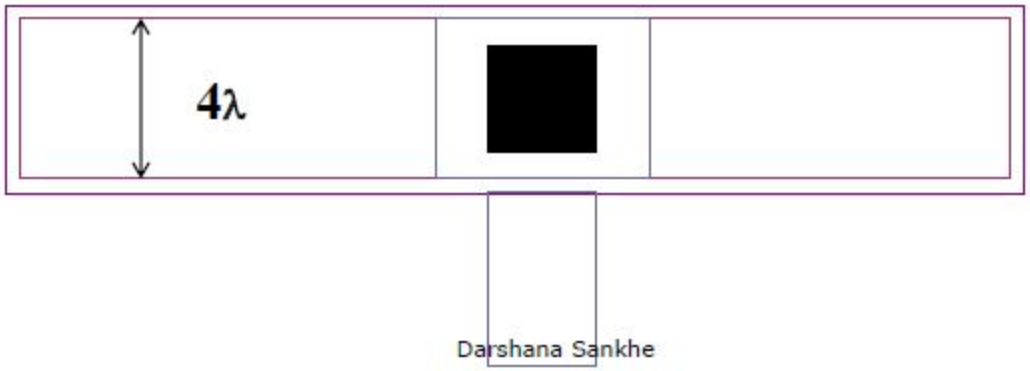
Design rules: NMOS

- Metal lines can pass over both diffusion and polySi without electrical effect
- It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected



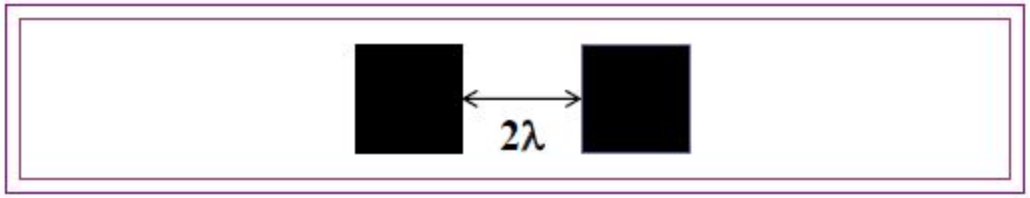
Contact cut

- **Metal connects to polySi/diffusion by contact cut.**
  Contact area: 2 λ *2 λ
- **Metal and polySi or diffusion must overlap this contact area by λ so that the two desired conductors encompass the contact area despite any mis-align**



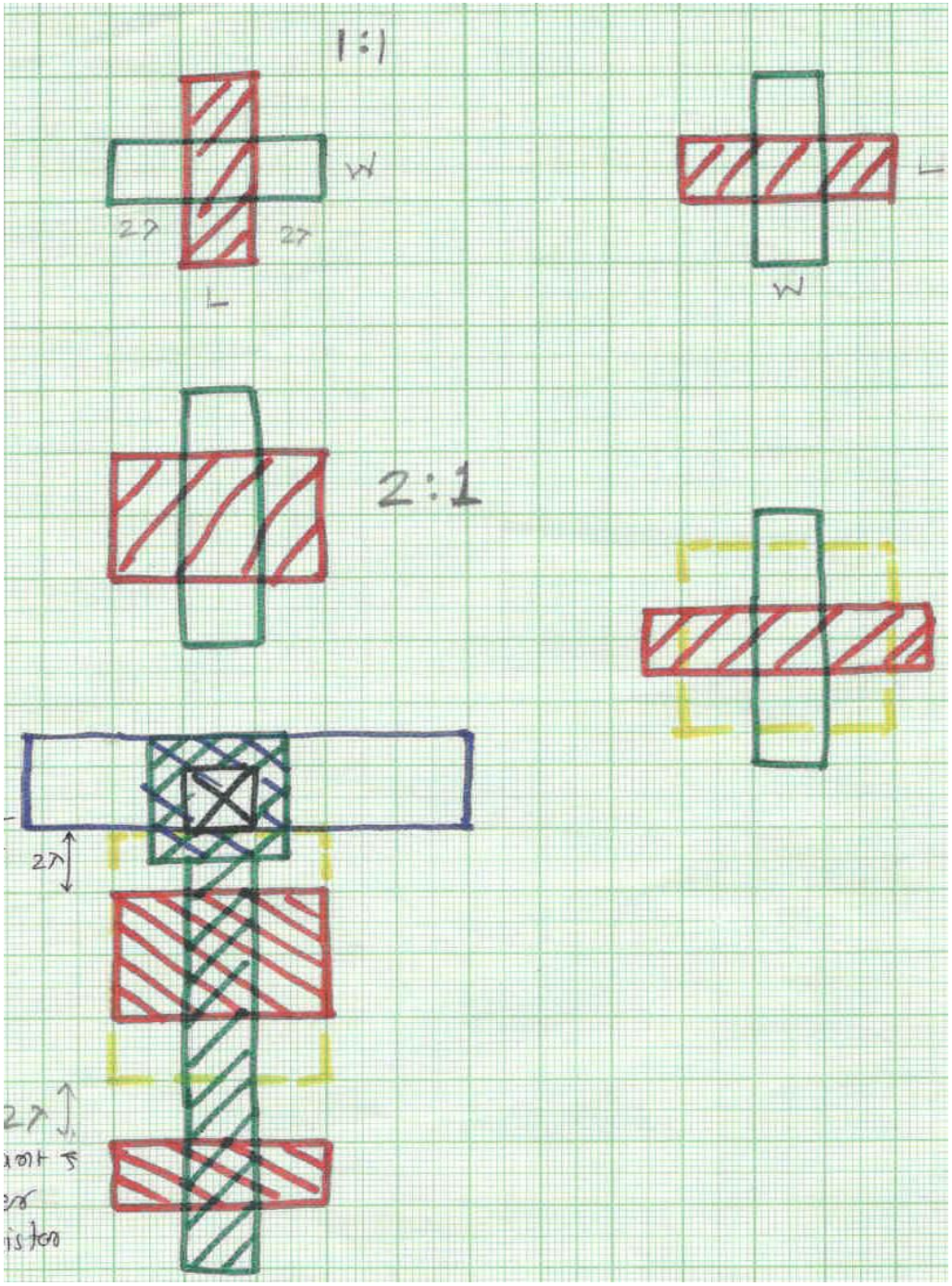
Contact cut

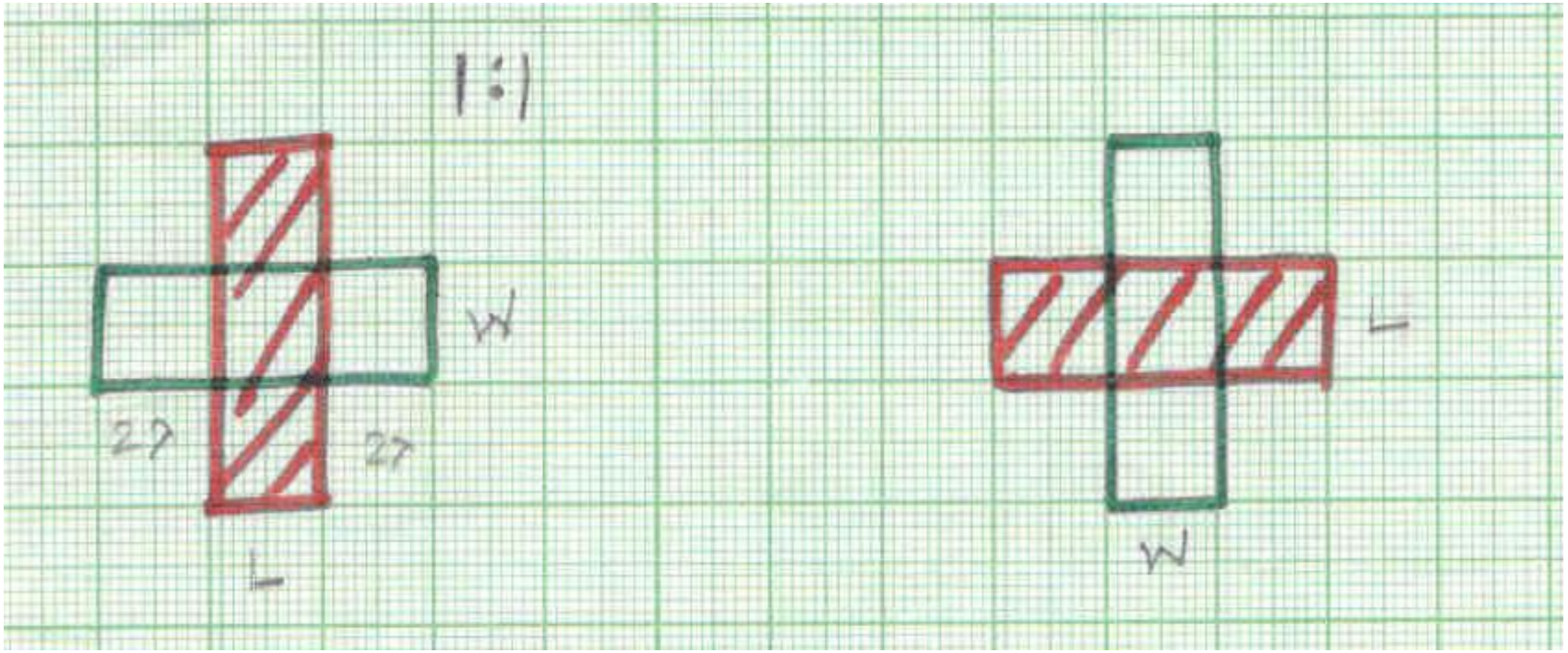
Contact cut – contact cut: 2 λ apart
To prevent holes from merging.



Design Rules to be followed:NMOS

- Minimum diff width 2 λ
- Minimum poly width 2 λ
- Minimum metal width 3 λ
- poly-poly spacing 2 λ
- diff-diff spacing 3 λ (depletion regions tend to spread outward)
- metal-metal spacing 3 λ
- diff-poly spacing λ
- Poly gate extend beyond diff by 2 λ
- Diff extend beyond poly by 2 λ
- Contact size 2 λ * 2 λ
- Contact diff/poly/metal overlap 1 λ
- Contact to contact spacing 2 λ
- Contact to poly/diff spacing 2 λ
- Buried contact to active device spacing 2 λ
- Buried contact overlap in diff direction 2 λ
- Buried contact overlap in poly direction 1 λ
- Implant gate overlap 2λ


1:1
W
2?
2?
L
L
W
2:1
2?
2?


1:1
W
2?
2?
L
L
W

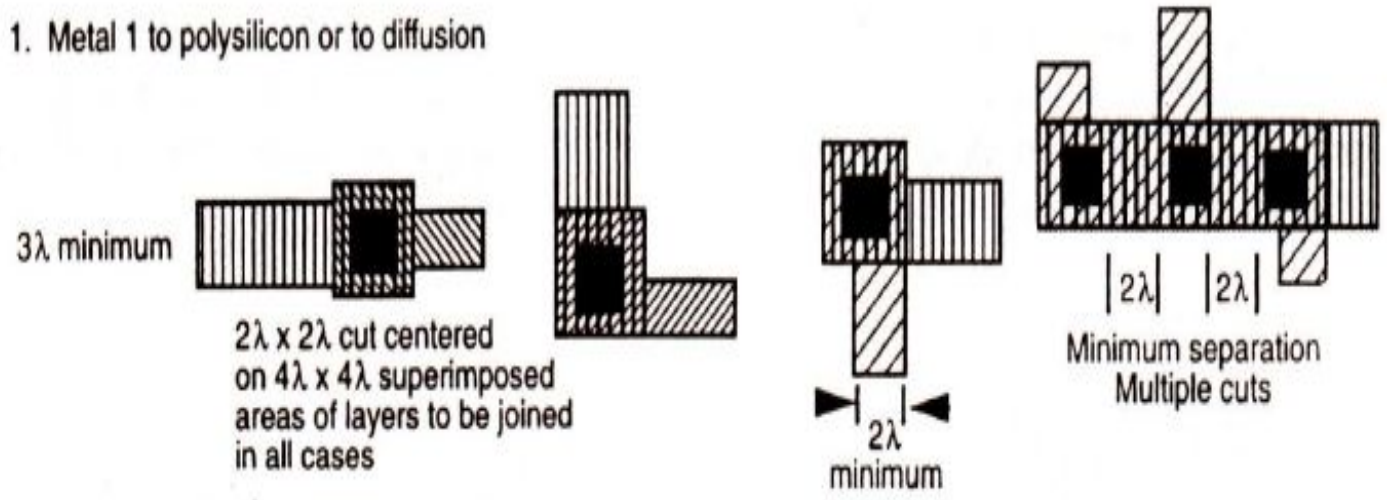
Interlayer Contacts

Interconnection between poly and diffusion is done by contacts.

1. Metal contact
2. Butting contact
3. Buried contact

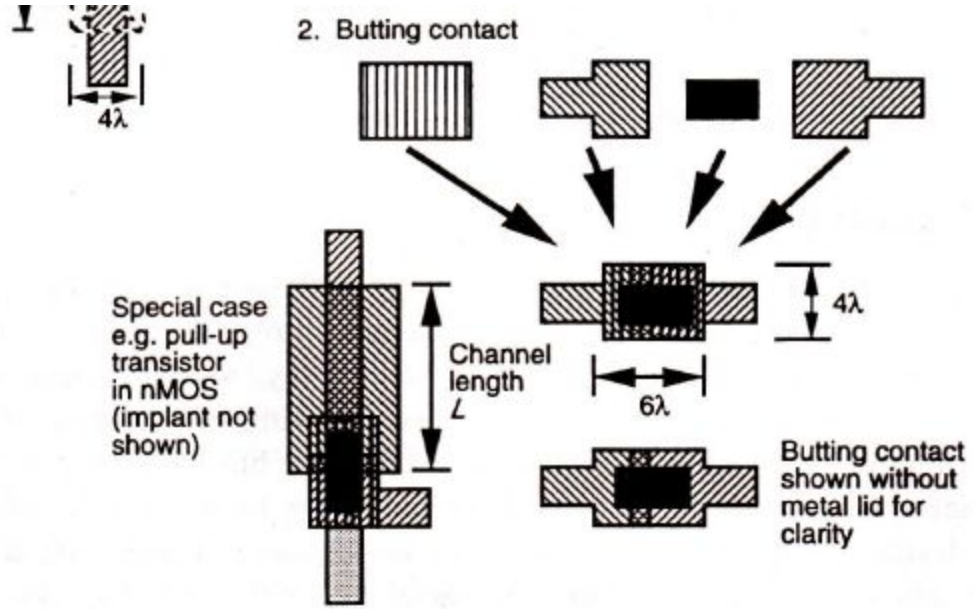
Metal 1 to polysilicon or to diffusion

- Contact cut of 2λ * 2λ in oxide layer above poly and diffusion
- Metal used for interconnection
- Individual contact size becomes 4λ * 4λ



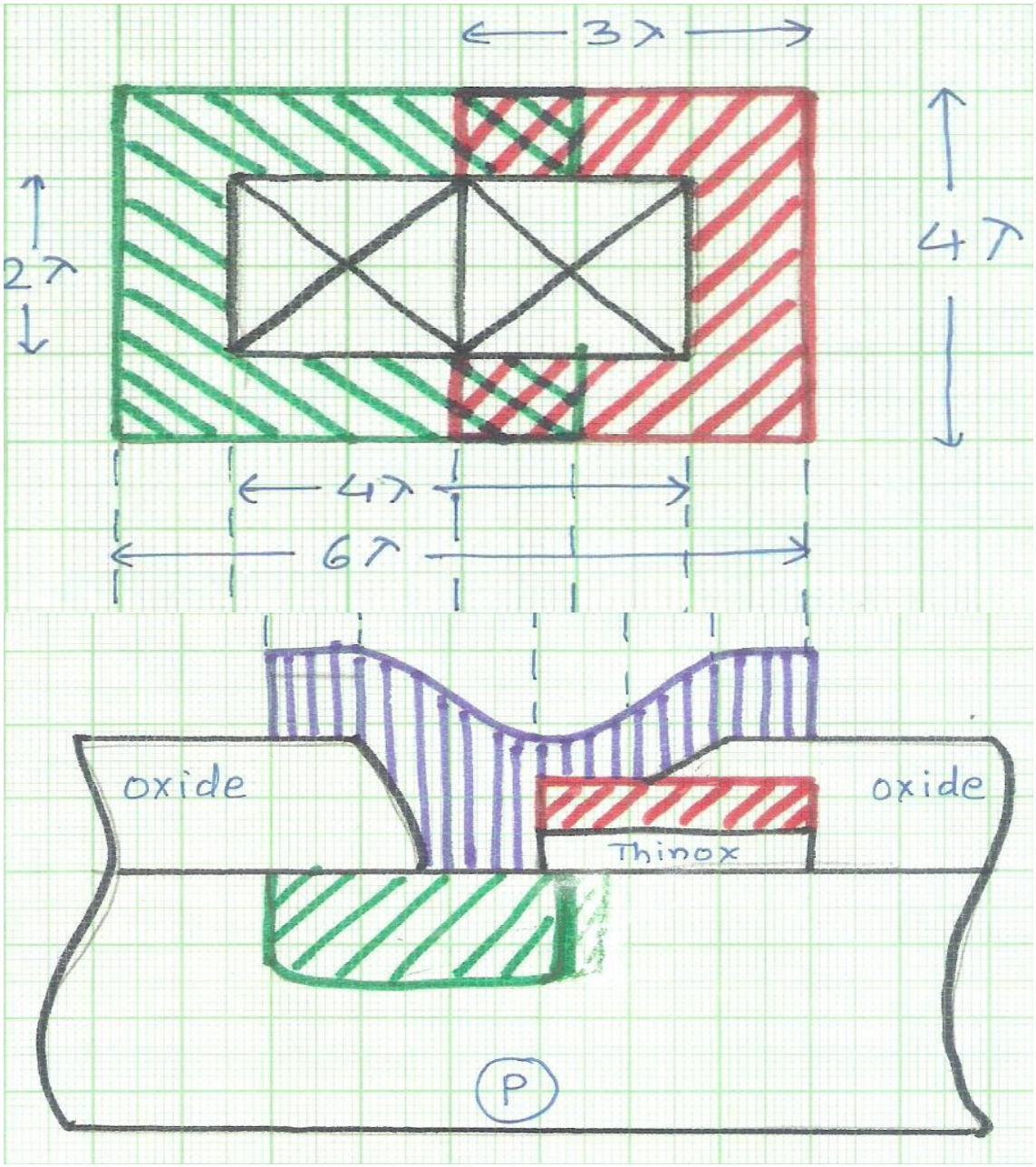
When deposition of the metal layer takes place the metal is deposited through the contact cut areas onto the underlying area so that contact is made between the layers.

Butting Contact



The gate and diffusion of NMOS device can be connected by a **butting contact.**

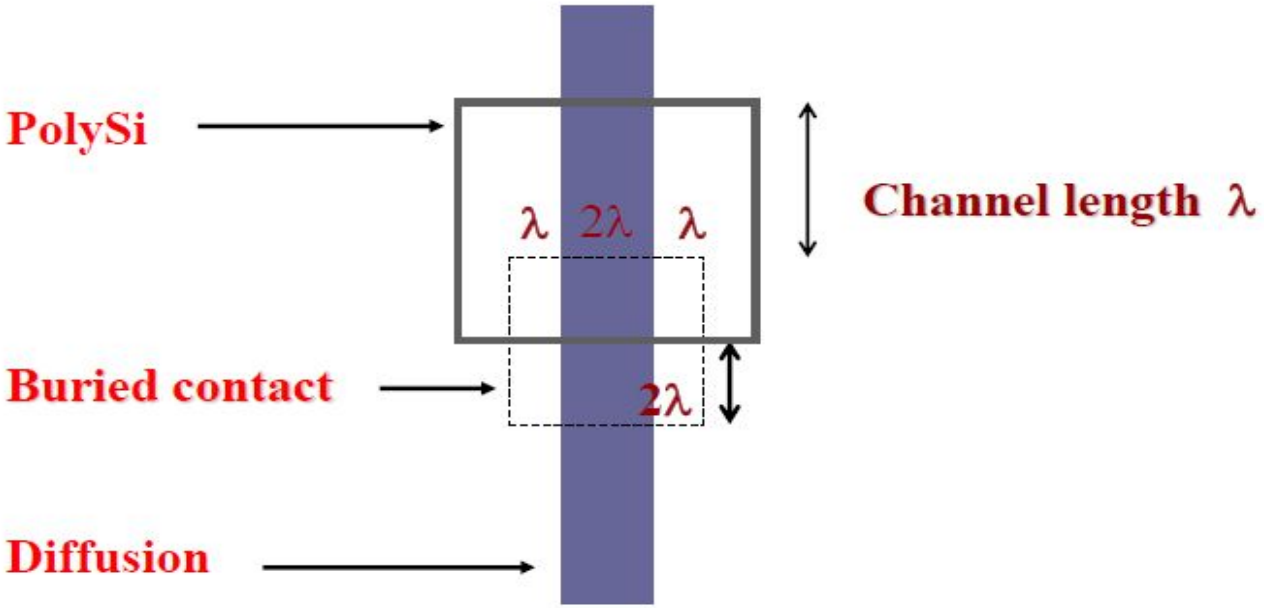
- **Two contact cuts are adjacent to each other**
- **Therefore effective contact area is less**
- Here metal makes contact to both the diffusion forming the drain of the transistor and to the polySi forming this device's gate.


3λ
2λ
4λ
4λ
6λ
oxide
oxide
Thinox
P

Buried Contact

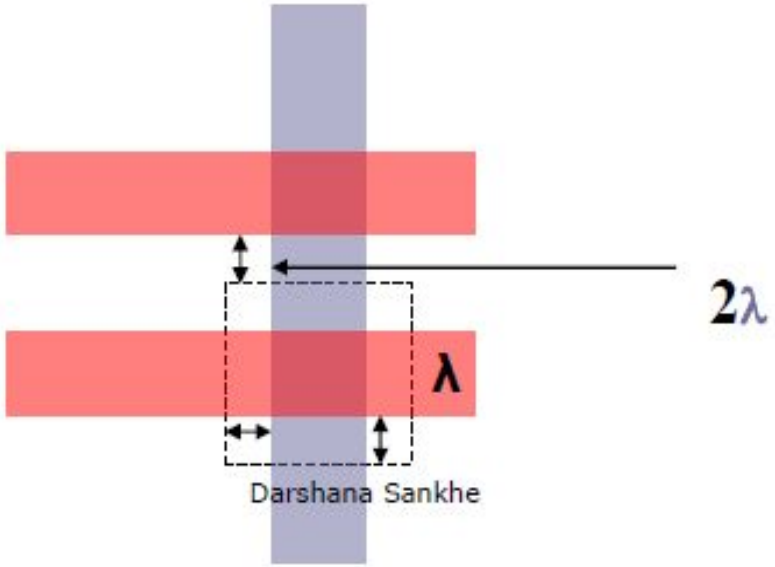
The buried contact window defines the area where oxide is to be removed so that polySi connects directly to diffusion.

- Contact Area must be a min. of 2 λ *2λ to ensure adequate contact area.
- Advantages: No metal cap required.
- Disadvantage: An extra mask is required.

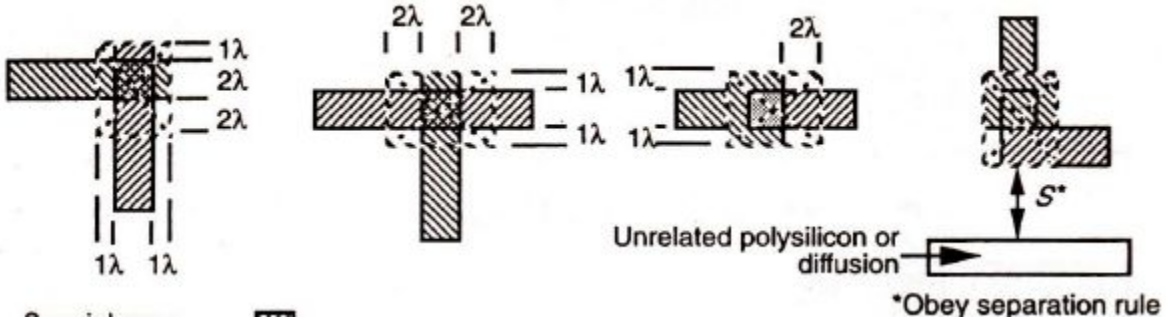


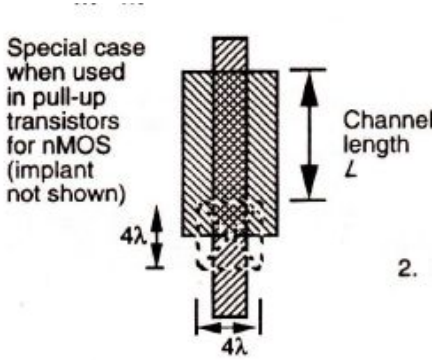
- The buried contact window surrounds this contact by λ in all directions to avoid any part of this area forming a transistor.

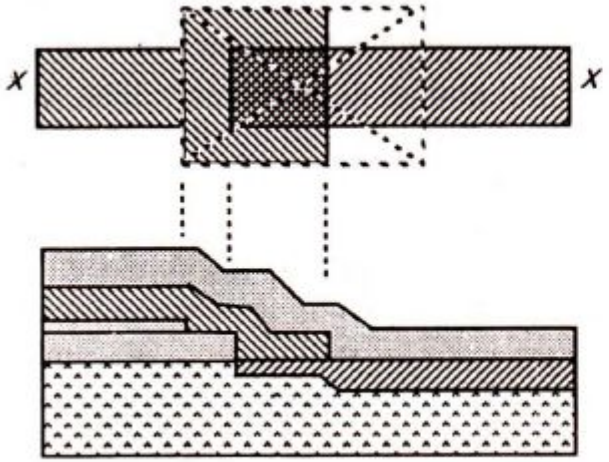
- Separated from its related transistor gate by 2λ to prevent gate area from being reduced.



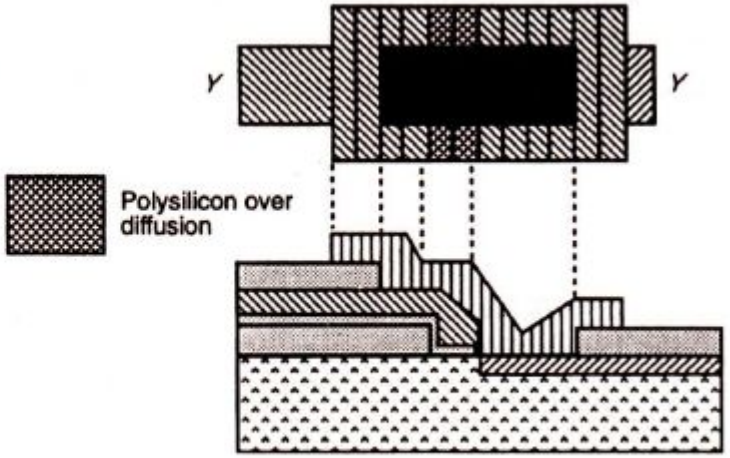
Buried Contact







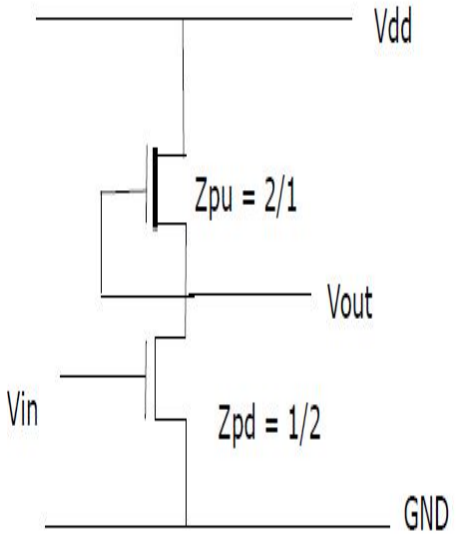
(a) Buried contact . . . section through *XX*

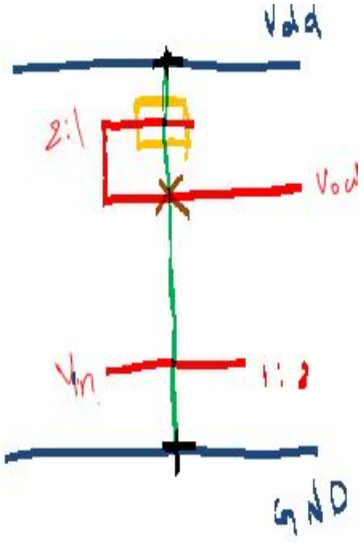


(b) Butting contact . . . section through *YY*

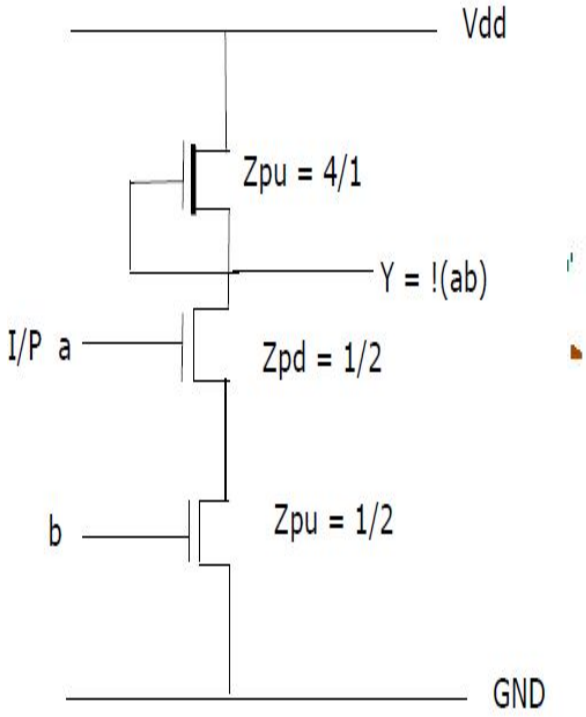
Examples of layout

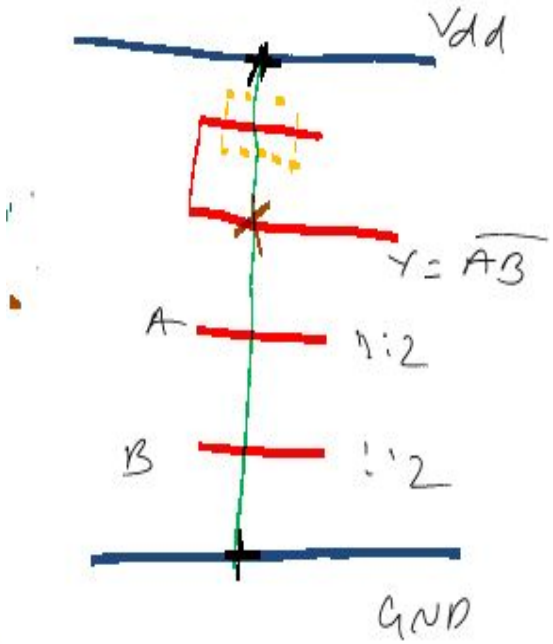
NMOS Depletion load Inverter



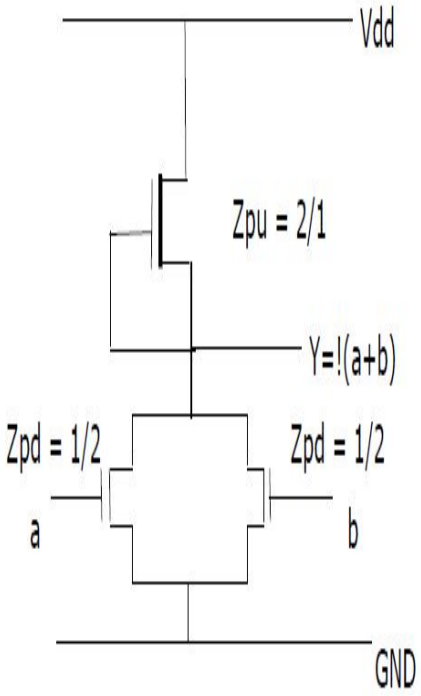


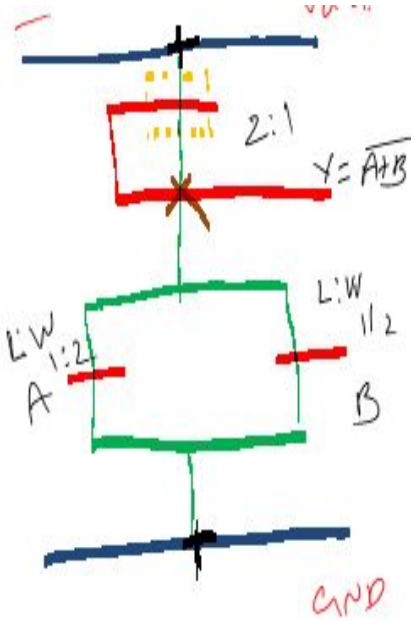
NMOS NAND


Vdd
Zpu = 4/1
Y = !(ab)
I/P a
Zpd = 1/2
b
Zpu = 1/2
GND


Vdd
Y = $\overline{AB}$
A
1:2
B
1:2
GND

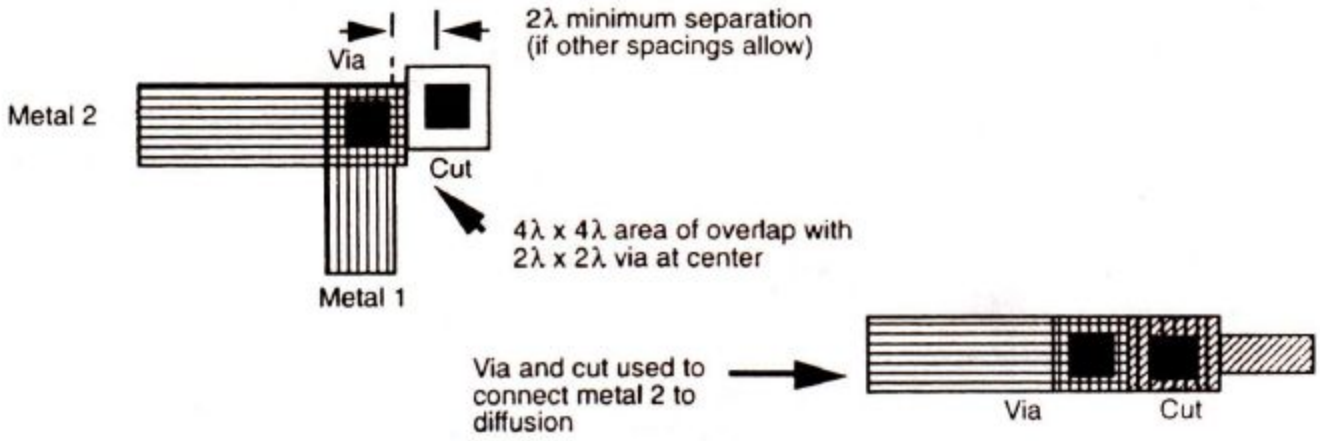
NMOS NOR





Double Metal MOS Process Rules

Via(contact from Metal 2 to Metal1)



- Second level metal layers are coarser than the first (conventional) layer and the isolation layer between the layers may also be of relatively greater thickness
- Contacts between first and second metal layers, they are known as *vias*
- The second metal layer representation is color coded dark blue (or purple)

Fabrication process

- The oxide below the first metal layer is deposited by atmospheric chemical vapor deposition (CVD) and the oxide layer between the metal layers is applied in a similar manner.
- Depending on the process, removal of selected areas of the oxide is accomplished by plasma etching, which is designed to have a high level of vertical ion bombardment to allow for high and uniform etch rates.
- The bulk of the process steps for a double polysilicon layer process are similar in nature to those already described, except that a second thin oxide layer is grown after depositing and patterning the first polysilicon layer (Poly. 1) to isolate it from the now to be deposited second poly. layer (Poly. 2).
- The presence of a second poly. layer gives greater flexibility in interconnections and also allows Poly. 2 transistors to be formed by intersecting Poly. 2 and diffusion.

The approach taken

1. Use the second level metal for the global distribution of power buses, that is, *VDD* and *GND* (*Vss),* and for clock lines.
2. Use the first level metal for local distribution of power and for signal lines.
3. Lay out the two metal layers so that the conductors are mutually orthogonal wherever possible.

CMOS Lambda-based Design Rules

Line size and spacing:

1. **metal1:**
   - Minimum width=3λ Minimum Spacing=3λ
2. **metal2:**
   - Minimum width=3λ Minimum Spacing=4λ
3. **poly:**
   - Minimum width= 2λ Minimum Spacing=2λ
4. **ndiff/pdiff:**
   - Minimum width= 3λ Minimum Spacing=3λ,
5. **wells:**
   - minimum width=6λ, minimum n-well/p-well space = 6λ (They are at same potential) = 9λ (They are at different potential)

Transistors:

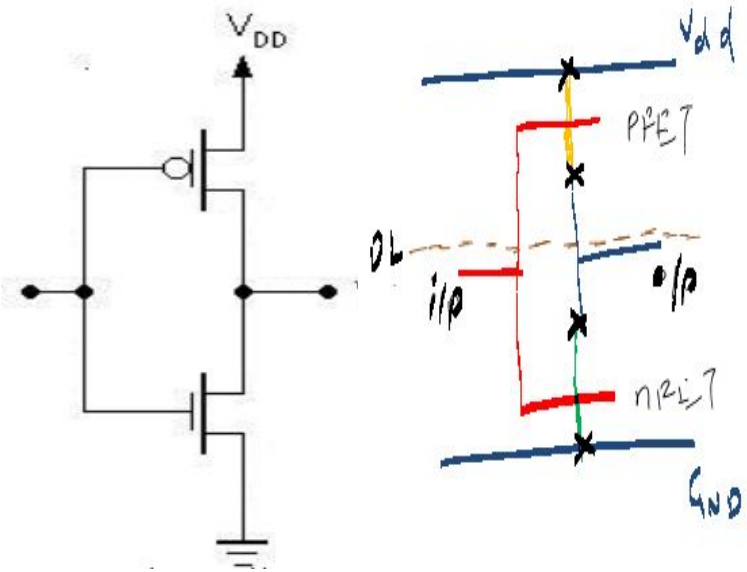
- Min width=3λ
- Min length=2λ
- Min poly overhang=2λ

Contacts (Vias):

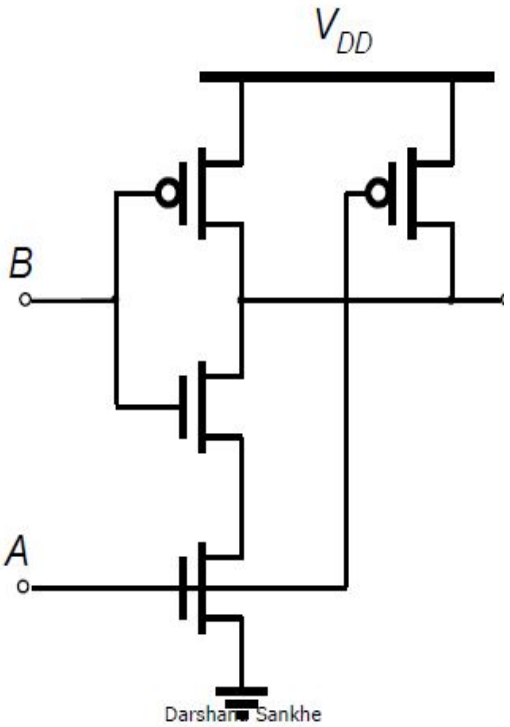
- Cut size: exactly 2λX 2λ
- Cut separation: minimum 2λ
- Overlap: min 1λin all directions

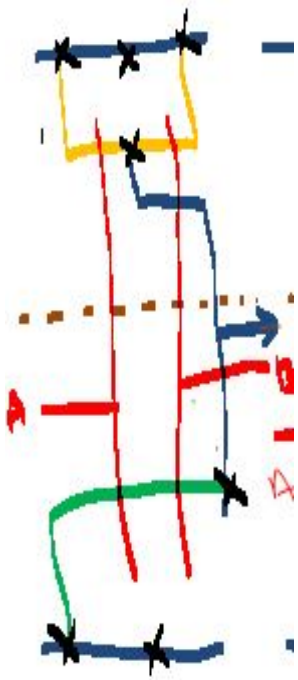
CMOS Examples

CMOS Inverter

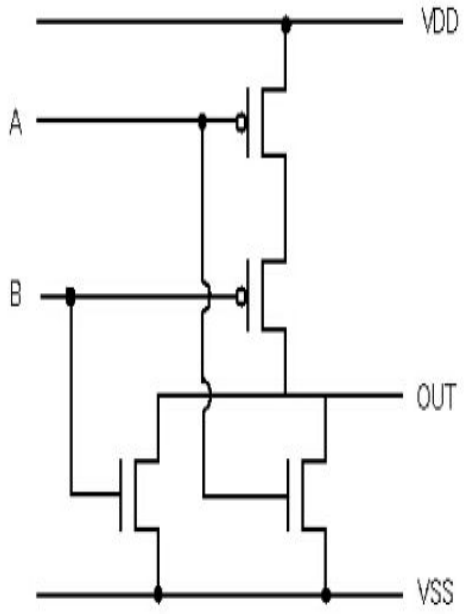


CMOS NAND

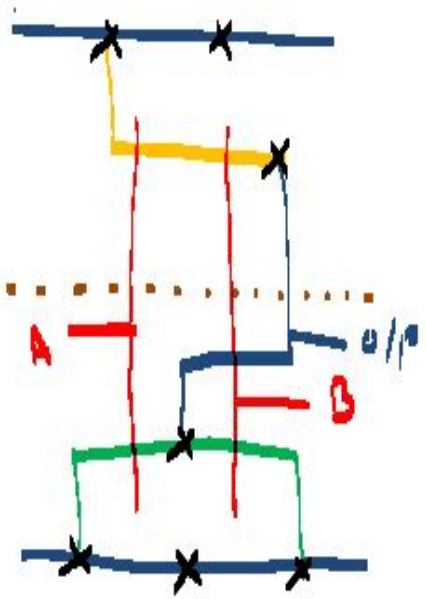




CMOS NOR



NOR gate in CMOS



CMOS Complementary Logic

- The various applications require logic structures have different optimization
- Circuits needs
  1. Fast response
  2. Some slow but very precise response
  3. Large functionality in a small space
- Optimizations are specific because of he trade off between the n number of design parameters

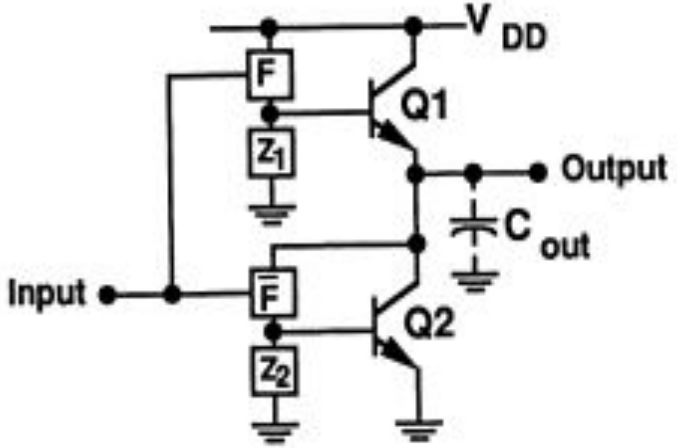
CMOS Complementary Logic

- CMOS NAND and NOR : Fixed sizes for n and p gates
- Variable ratios ---- to vary the threshold and speed
- If all gates are of same sizes
  1. Functions more correctly
  2. Supply voltage can be increased to get better noise
  3. Supply voltage can be decreased for reduced power dissipation
  4. Power down with low power dissipation

- A CMOS requires a n block an p block for completion of the logic. That is for a n input logic 2n gates are required
- Variation include
  1. Reduction of noise margins
  2. Reducing the function determining transistors to one polarity

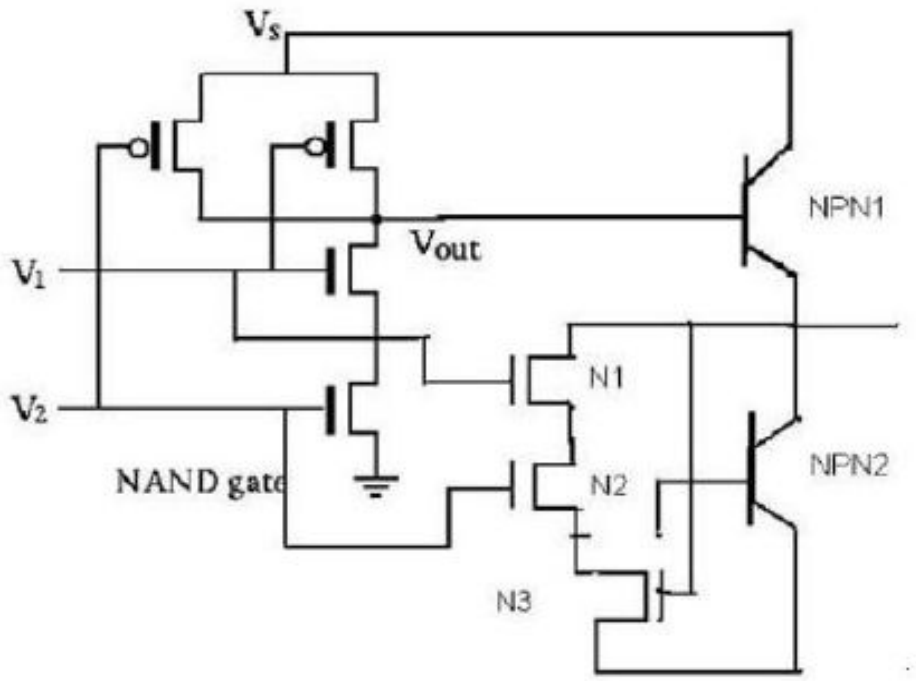
BICMOS Logic

- The CMOS logic structures have low output drive capability
- The bipolar transistors produces larger output -----current controlled devices
- We can have the bipolar transistors both for pull up and pull down or only for pull up

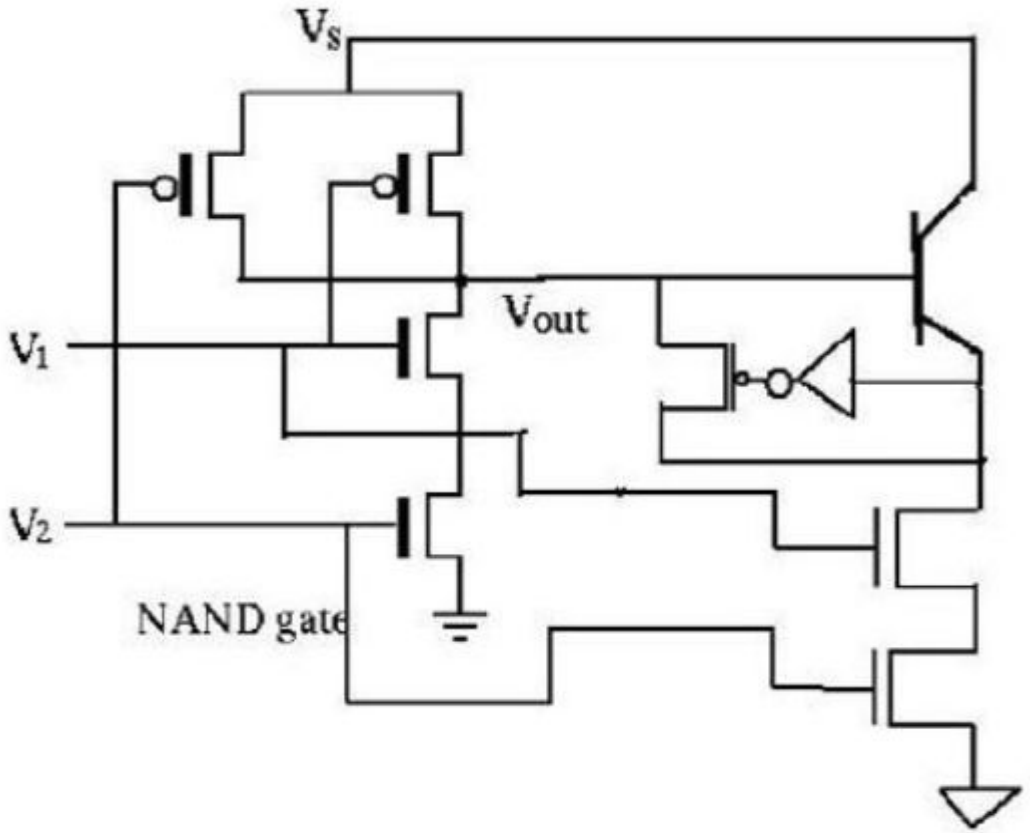


Generalized BICMOS Logic gate

NAND with two NPN drivers



NAND with one NPN in pull up



Pseudo nMOS

- Adding a single pFET to otherwise of nFET only circuit----------Pseudo –nMOS
- Pseudo nMOS logic uses fewer transistors
- For N inputs, a pseudo nMOS logic gates requires (N+1) FETs

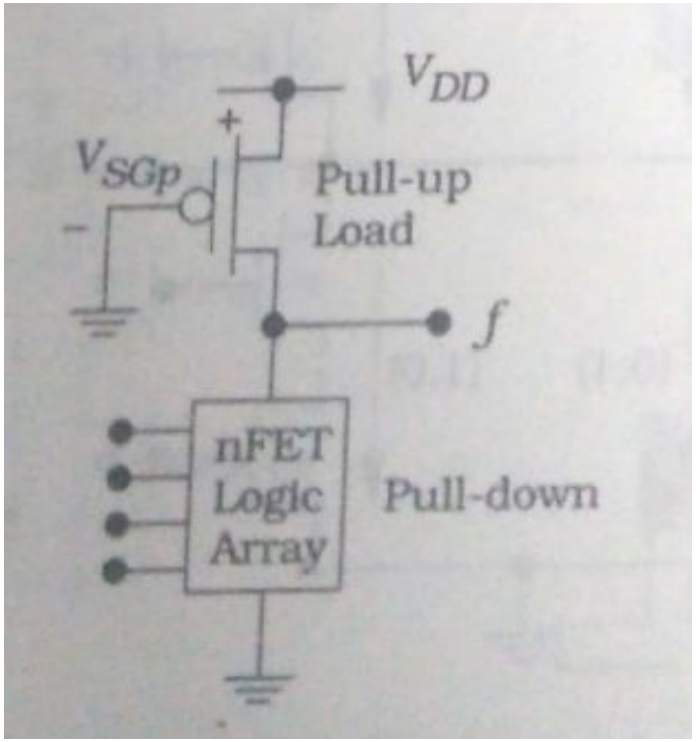
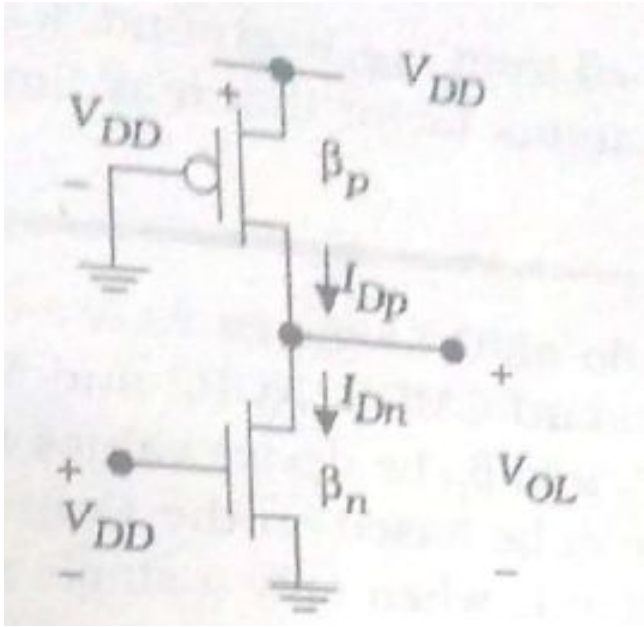


ILLUSTRATION OF SIZING PROBLEM



$$\frac{\beta_n}{2}[2(V_{DD}-V_{Tn})V_{OL}-V_{OL}^{\,2}] = \frac{\beta_p}{2}(V_{DD}-|V_{Tp}|)^2$$

$$V_{OL} = (V_{DD}-V_{Tn}) - \sqrt{(V_{DD}-V_{Tn})^2 - \frac{\beta_p}{\beta_n}(V_{DD}-|V_{Tp}|)^2}$$

EXAMPLE

Consider a CMOS process with VDD=5V, VTn=0.7V, VTp=-0.8V, Kn=150*10^-6A/V^2 And Kp= 68*10^-6A/V^2. A pseudo nMOS inverter sixe with(W/L)n=4 and (W/L)p=6 Gives an inverted with an output low voltage

Clocked CMOS

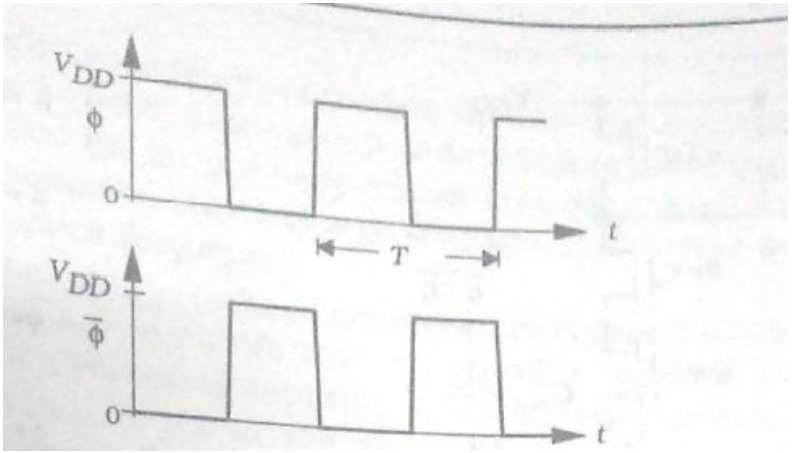
The real power of digital logic is realized only when we progress the concept of clock control and sequential circuits.
The clock signal ϕ(or clock) is periodic waveform with a well defined period T(sec) and frequency f[Hz]

$$F=1/T$$

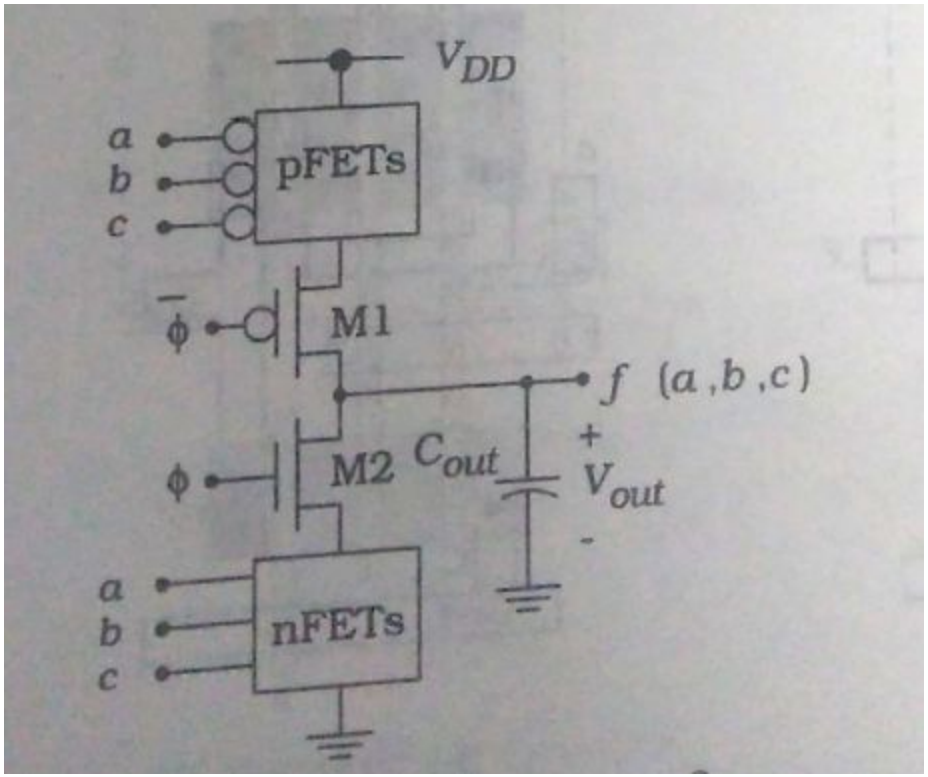
The clock ϕ(t) and its complement ϕ(t)'. Ideally these are non-overlapping such that

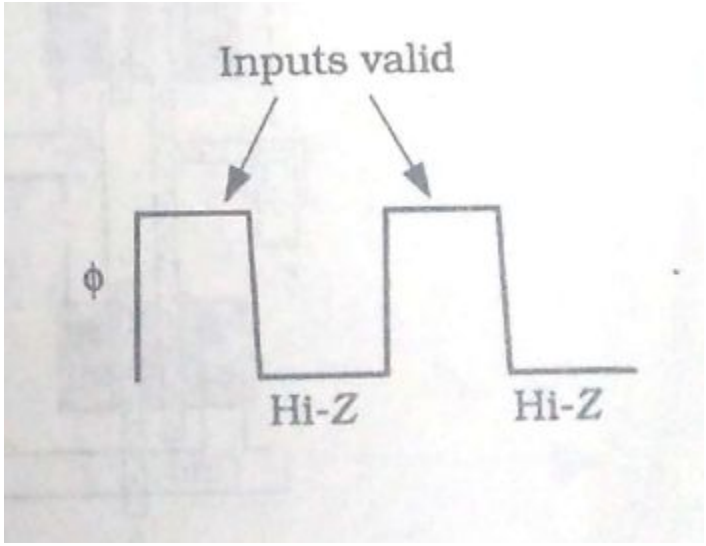
$$\phi(t)\,\phi(t)'=0$$

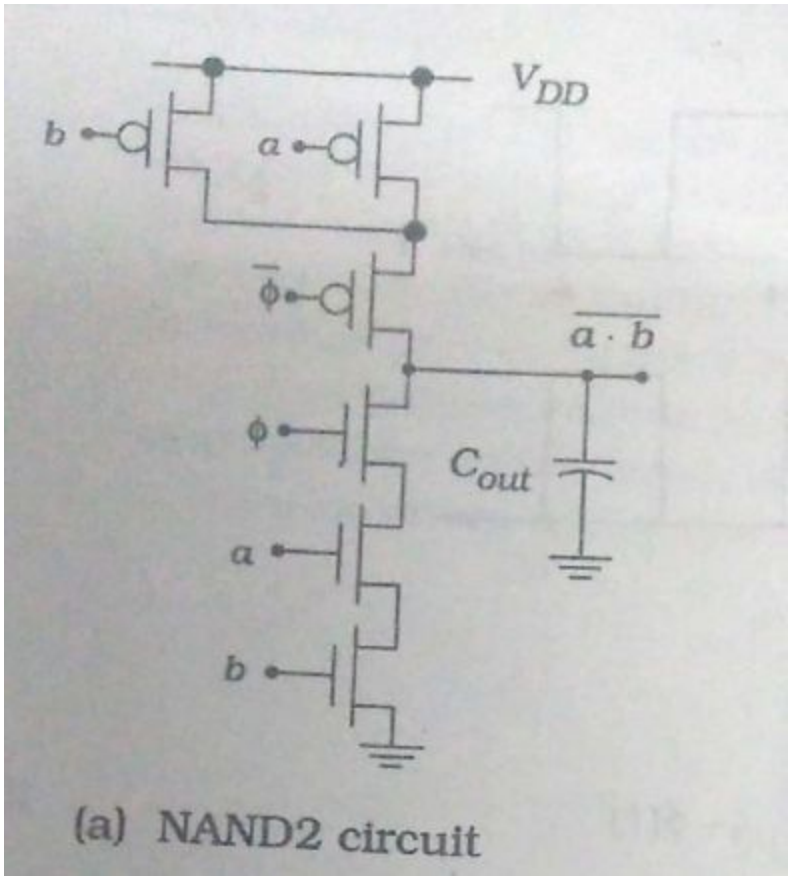
$$\phi(t)'=VDD-\phi(t)$$



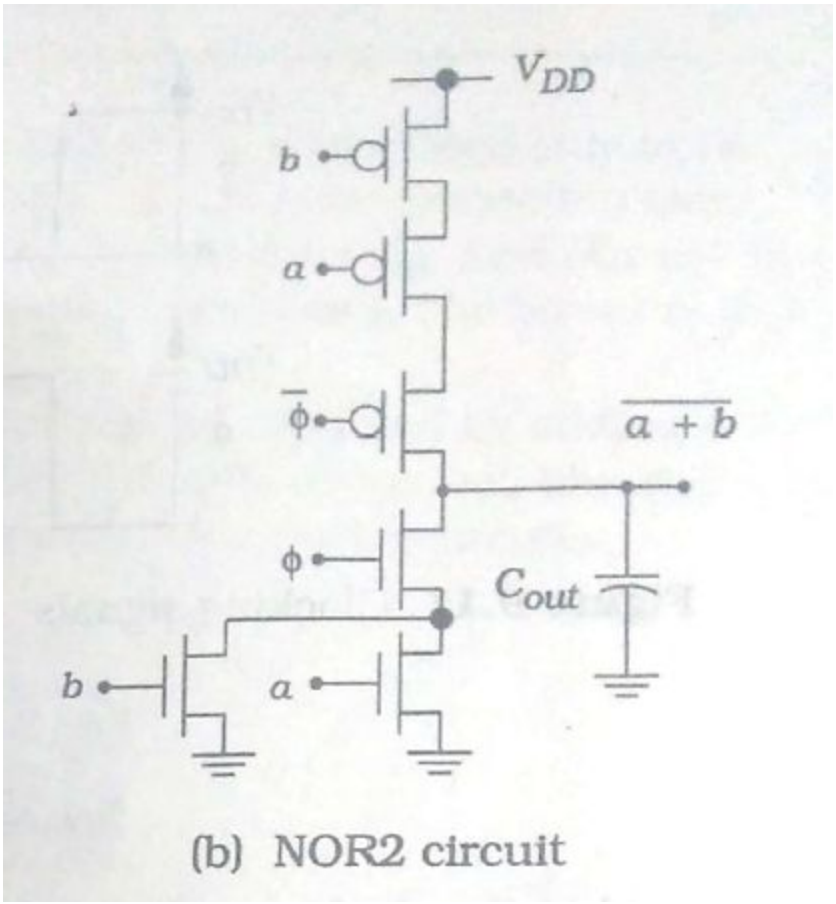
General Structure of a C^2MOS



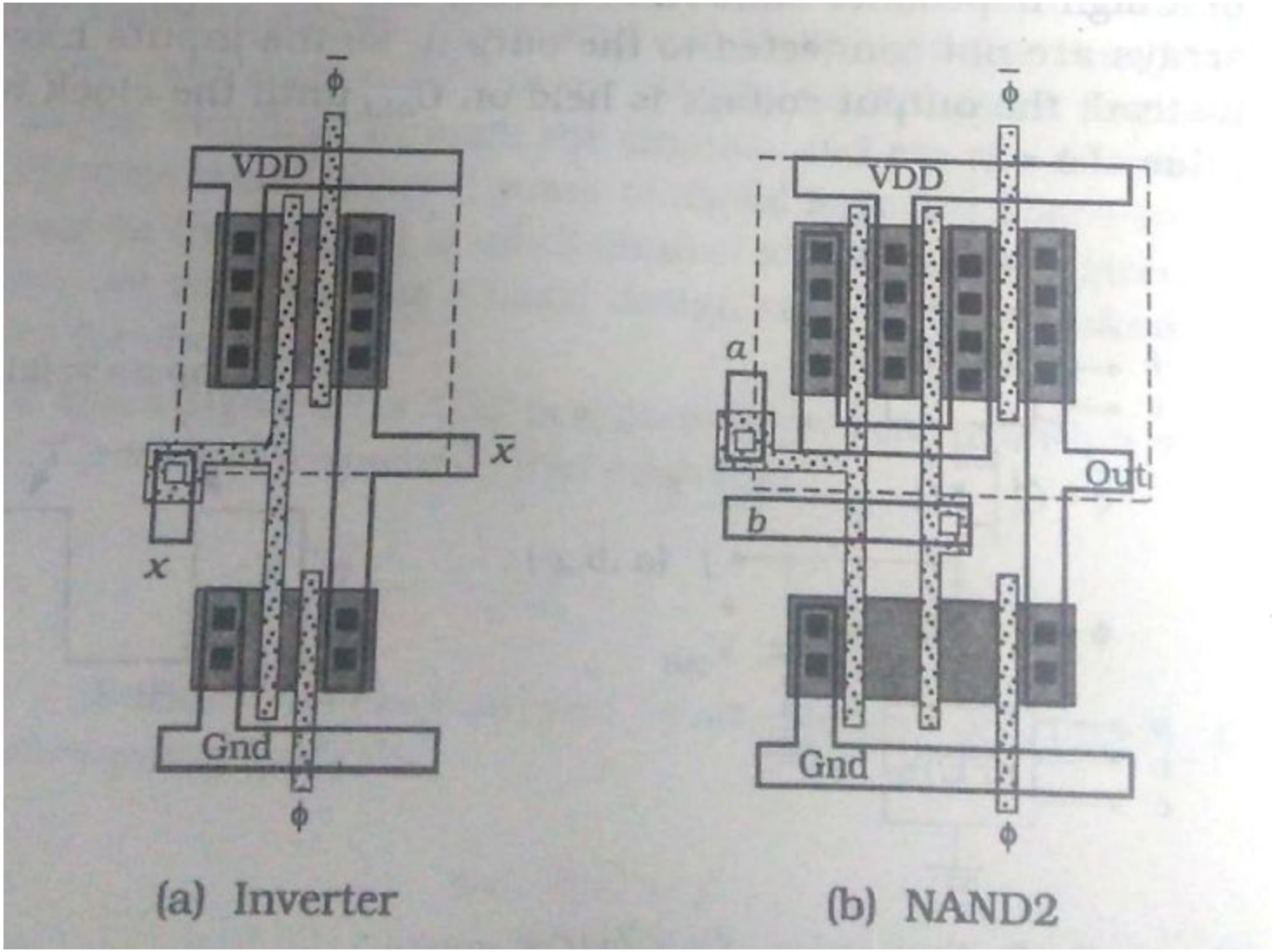




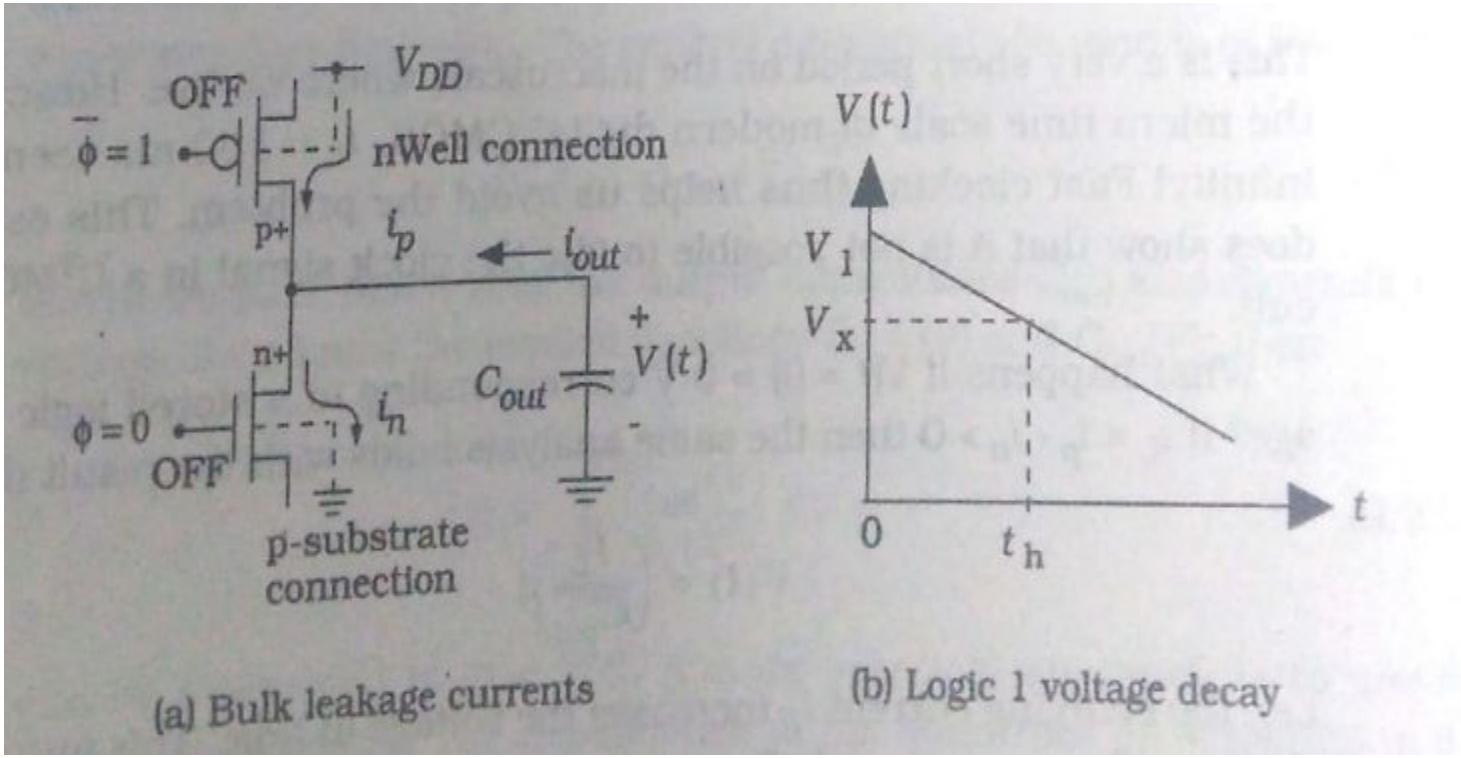
(a) NAND2 circuit



(b) NOR2 circuit


$\bar{\phi}$
VDD
$\bar{x}$
x
Gnd
ϕ
(a) Inverter
$\bar{\phi}$
VDD
a
Out
b
Gnd
ϕ
(b) NAND2

Charge leakage



(a) Bulk leakage currents

(b) Logic 1 voltage decay

Denoting the current off of the capacitor by iout, we may sum the contribution to obtain

$$i_{out} = i_n - i_p$$
$$= -C_{out}\frac{dV}{dt}$$

To see the effects of the leakage currents, suppose that we have an initial voltage v(t=0)=V1 Stored on the capacitor

If in>ip, then iout=iL is a positive number, indicating current flow off of the capcitor Rewriting the equation as

$$I_L = -C_{out}\frac{dV}{dt}$$

$$\int_{V_1}^{V(t)} dV = -\int_0^t \left(\frac{I_L}{C_{out}}\right) dt$$

Assuming IL is constant, equation may be integrated to yield

$$V(t) = V_1 - \left(\frac{I_L}{C_{out}}\right)t$$

The hold time the corresponds to the maximum time that the logic 1 voltage can be stored

$$V(t_h) = V_1 - \left(\frac{I_L}{C_{out}}\right) t_h = V_x$$

$$t_h = \left(\frac{C_{out}}{I_L}\right)(V_1 - V_x)$$

Cout=50fF, IL=0.1pA, voltage change=1V

If V(t=0)=0V, IL=ip-in>0 then the same analysis holds with the result

$$V(t) = \left(\frac{I_L}{C_{out}}\right)t$$

Subthreshold Current

$$I = I_{D0}\left(\frac{W}{L}\right)e^{-(V_{GS}-V_T)/(nV_{th})}$$

If ID0=10^-9, VGS=0V

Physical structure

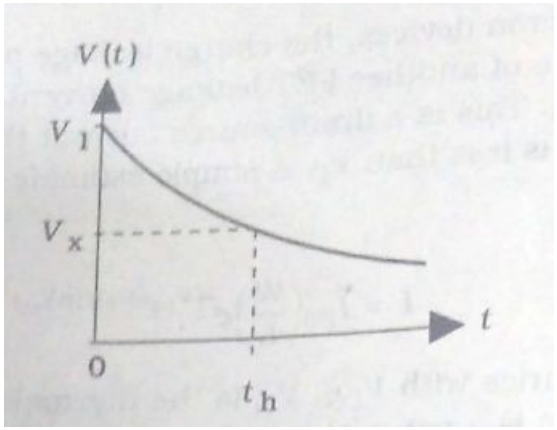
$$t_h = \left(\frac{50\times10^{-15}}{10^{-7}}\right)(1) = 0.5 \ \mu\text{sec}$$

The general differential equation is of the form

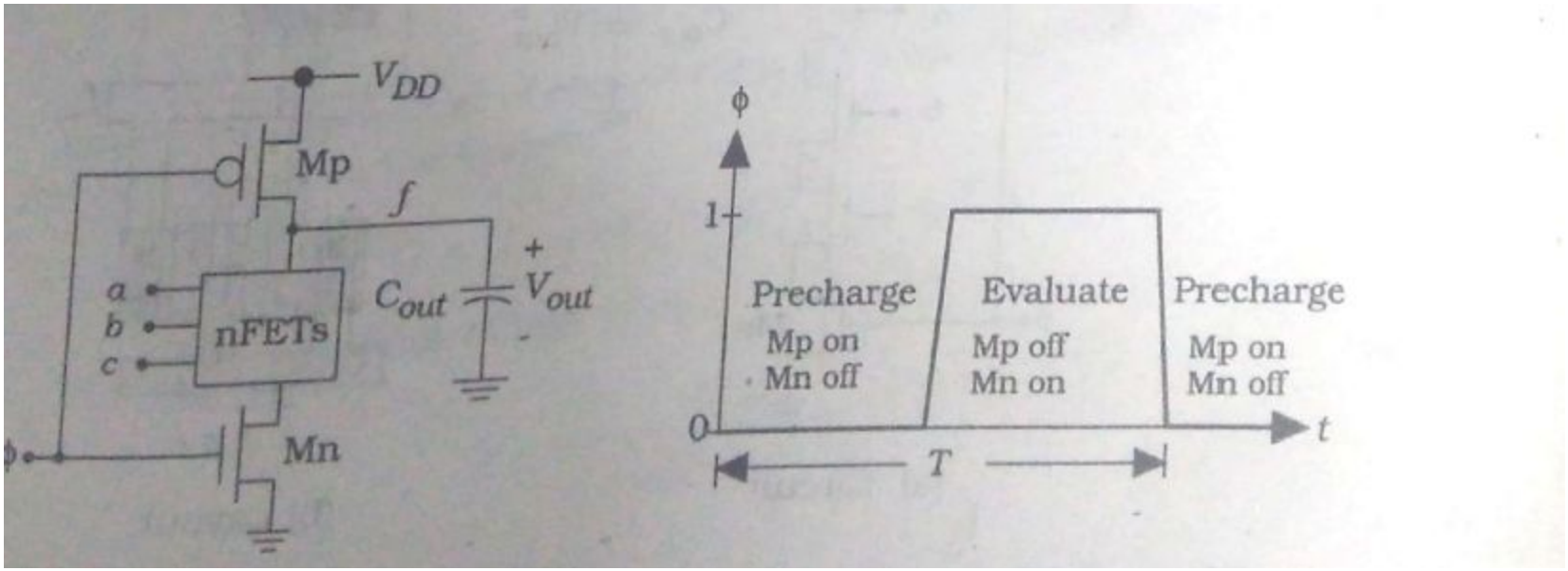
$$I_L(V) = -C_{out}(V)\frac{dV}{dt}$$

If we know the explicit functions for IL(V) and Cout(V) then

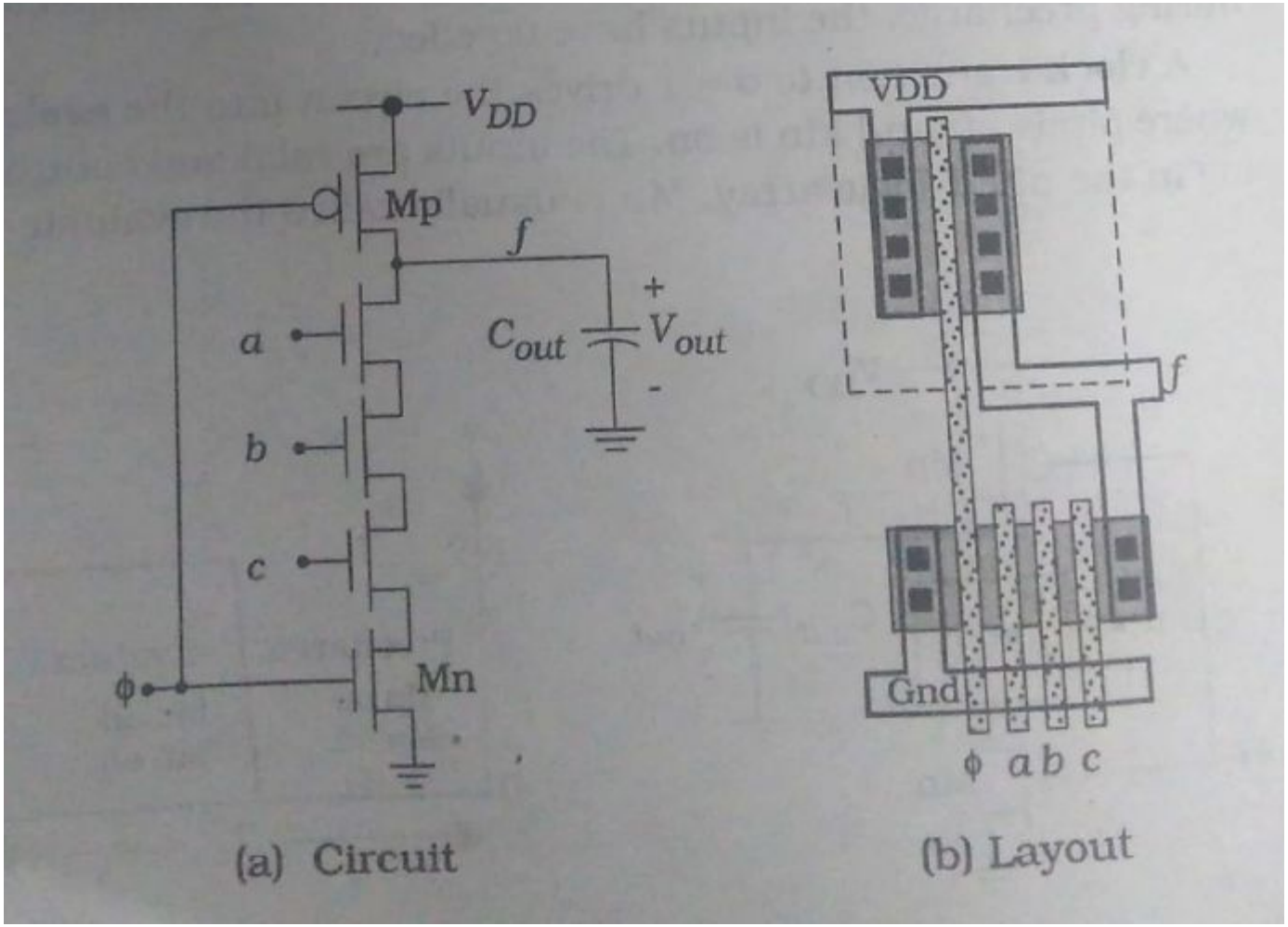
$$\int_0^t dt = \int_{V_x}^{V(t)} \frac{C_{out}(V)}{I_L(V)}\,dV = t$$



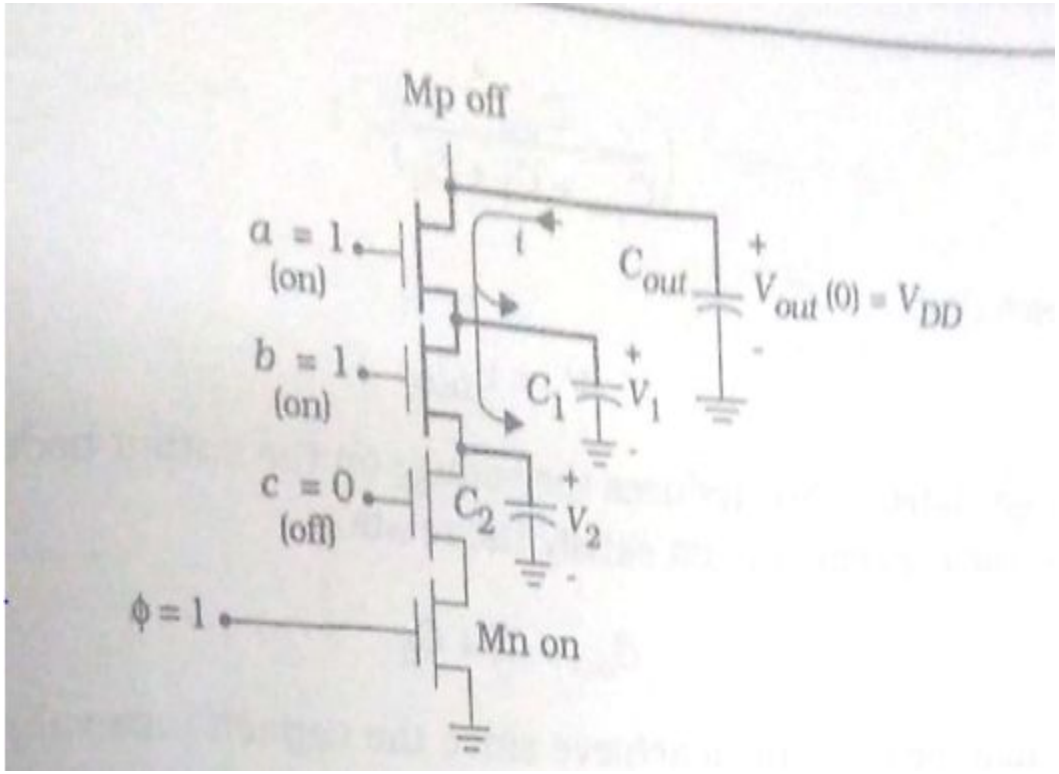
Dynamic CMOS Logic Circuits



Dynamic Logic gate Example



Charge Sharing



The current flow caused when the voltages are equal with a final value

$$V_{out} = V_2 = V_1 = V_f$$

The total charge on the current is then distributed according to

$$\begin{aligned} Q &= C_{out}V_f + C_1V_f + C_2V_f \\ &= (C_{out} + C_1 + C_2)V_f \end{aligned}$$

Applying the principle of conservation of charges this must be equal to the initial charge in the system

$$Q = (C_{out} + C_1 + C_2)V_f = C_{out}V_{DD}$$

$$V_f = \left(\frac{C_{out}}{C_{out} + C_1 + C_2}\right)V_{DD}$$

$$\left(\frac{C_{out}}{C_{out} + C_1 + C_2}\right) < 1$$

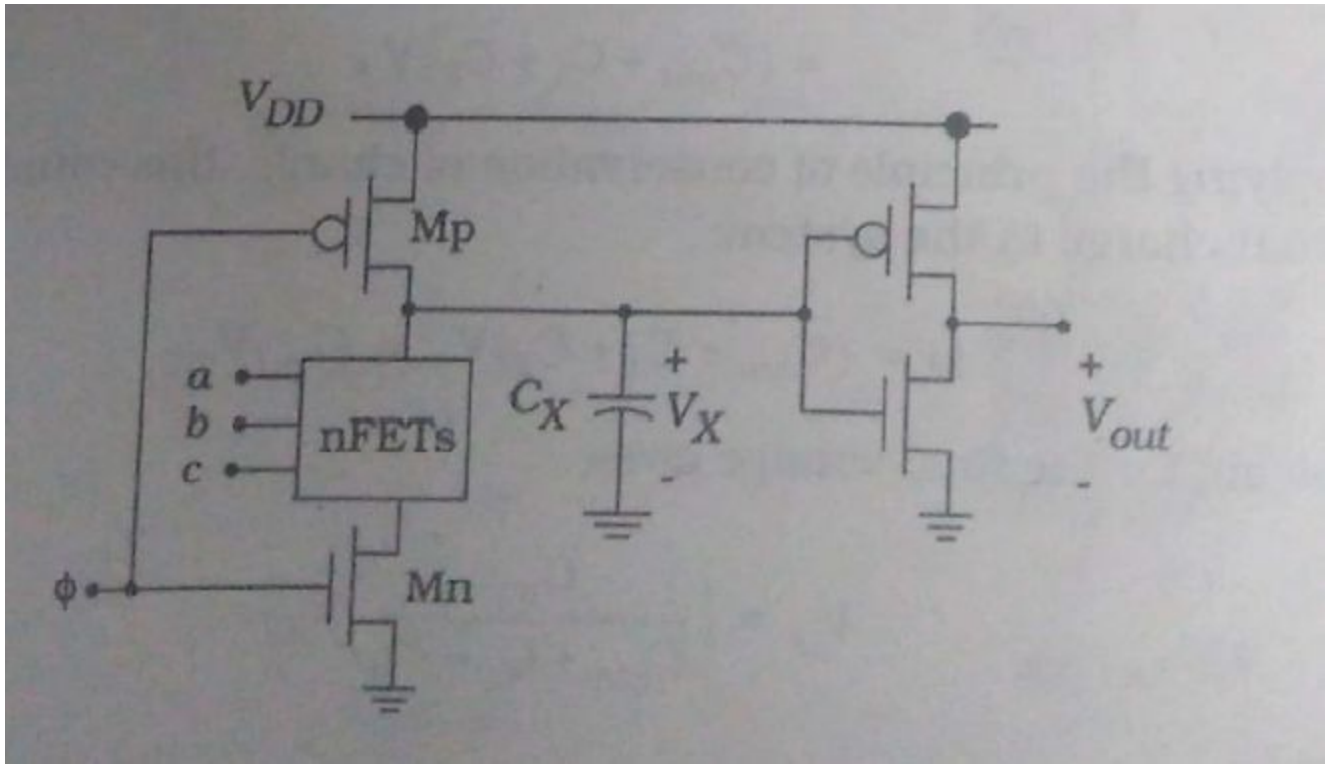
we see that

$$V_f < V_{DD}$$

$$C_{out} \gg C_1 + C_2$$

Domino Logic

Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit



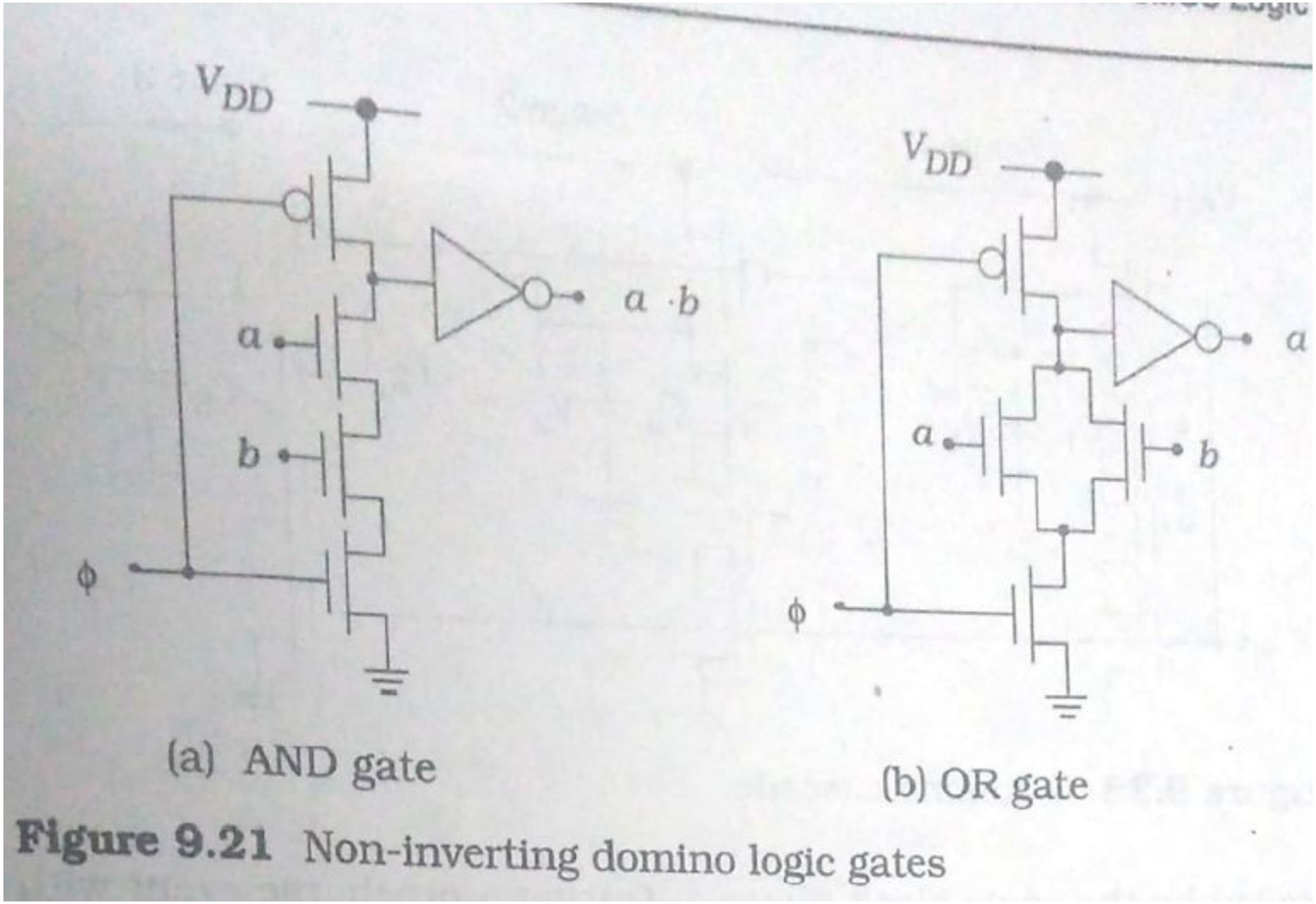
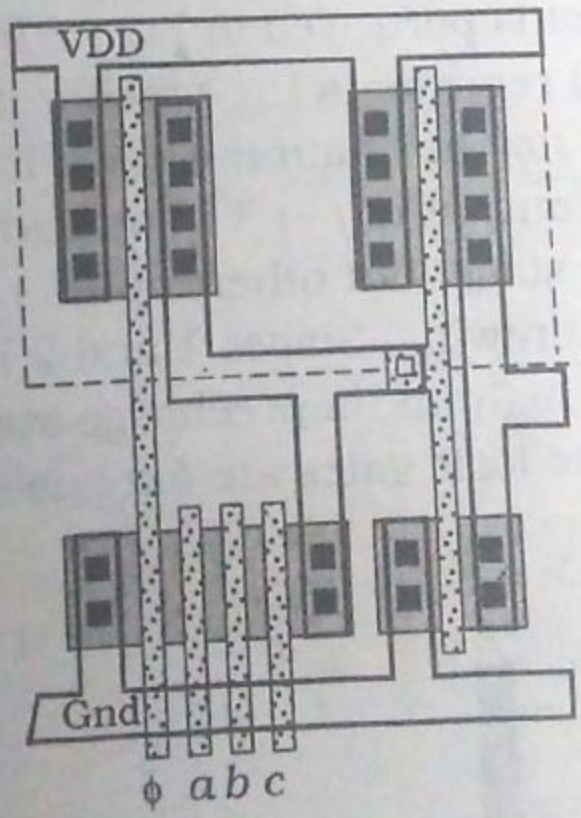


Figure 9.21 Non-inverting domino logic gates



gure 9.22 Layout for a domino AND gate

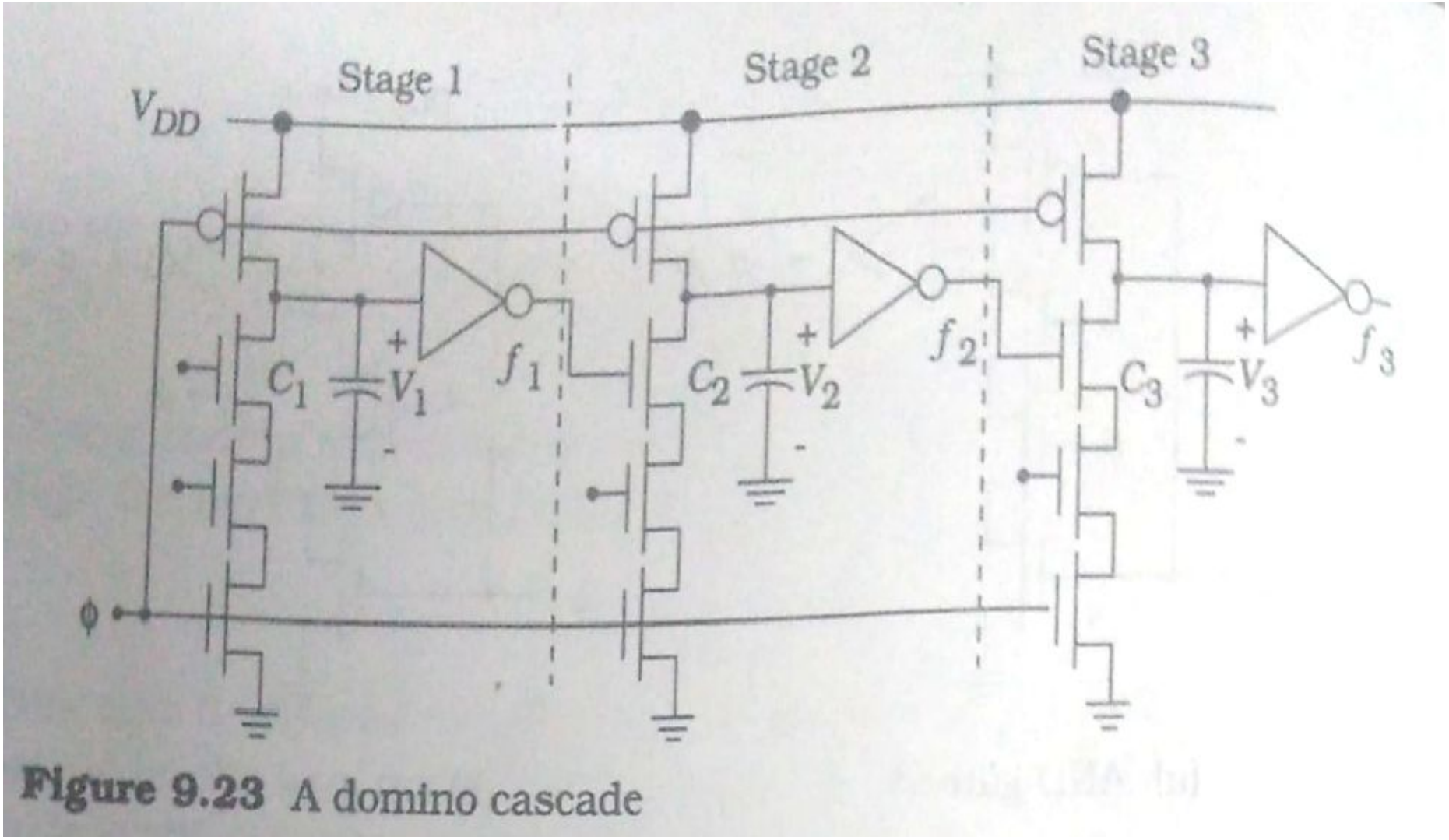
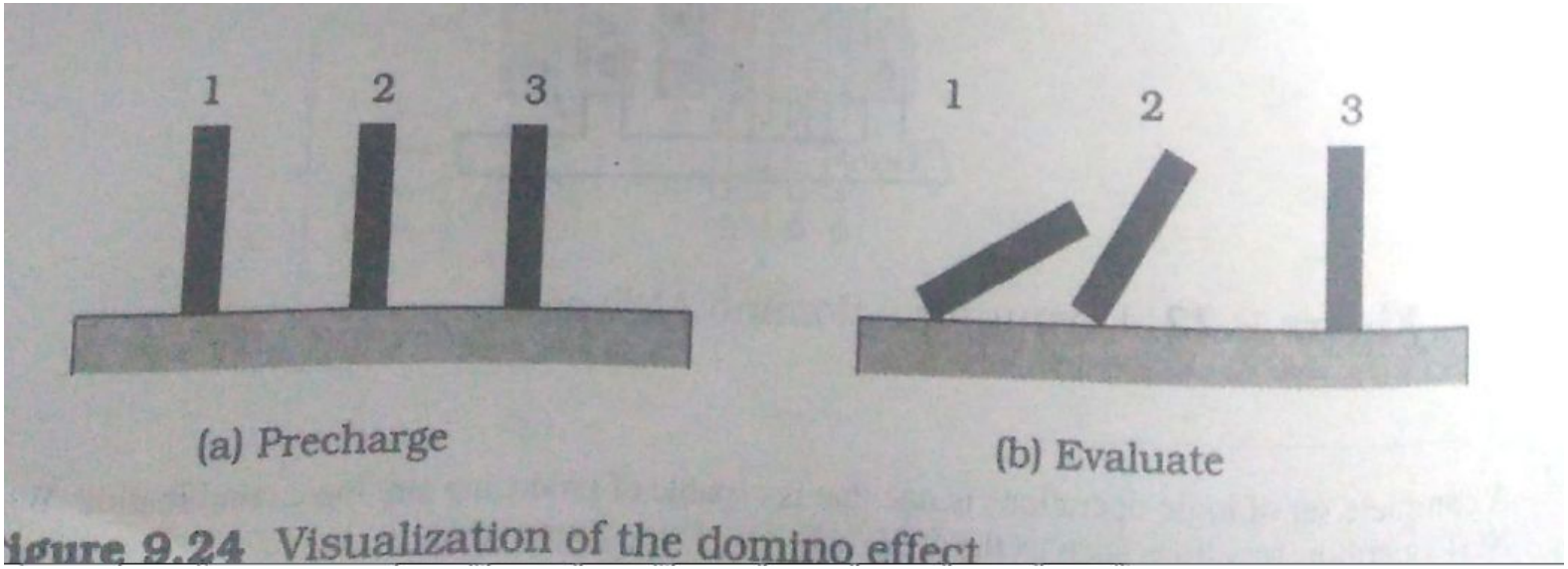
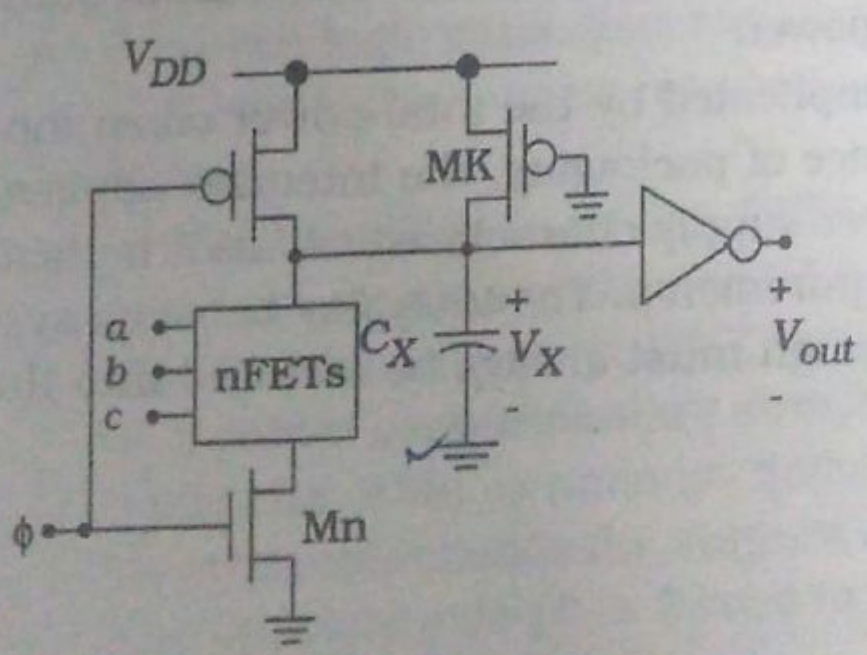


Figure 9.23 A domino cascade

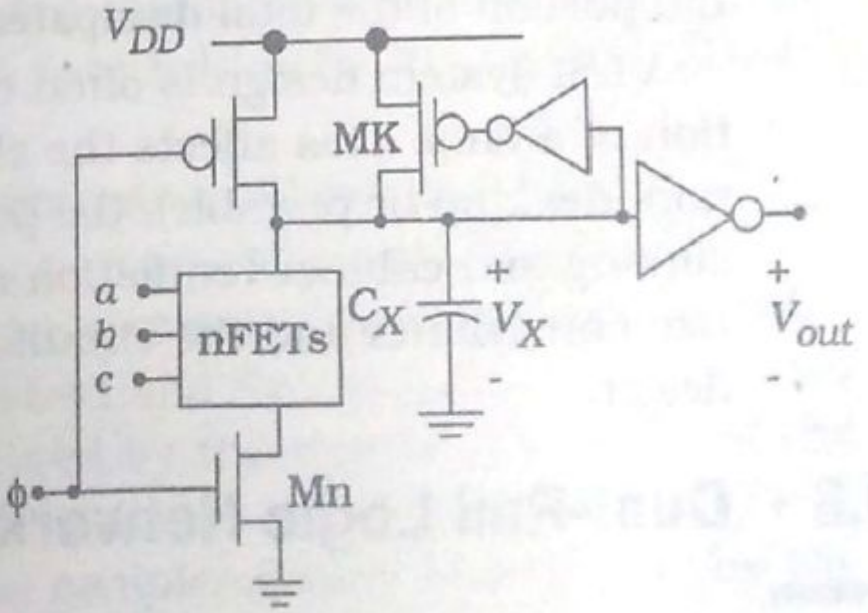


igure 9.24 Visualization of the domino effect

Charge Keeper



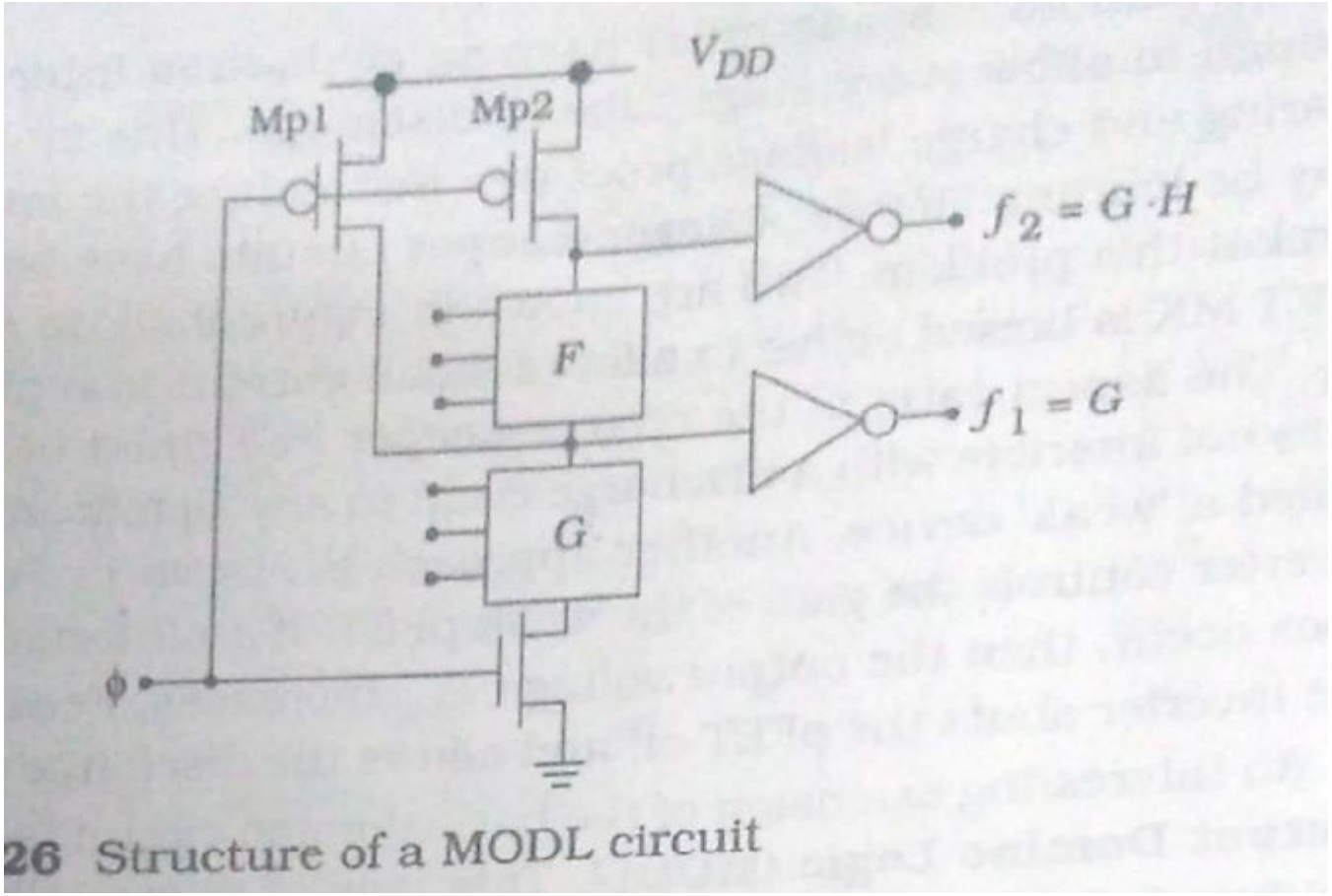
(a) Single-FET charge keeper



(b) Feedback controlled keeper

Figure 9.25 Charge-keeper circuits

Multiple output Domino Logic



26 Structure of a MODL circuit

Power Dissipation of Dynamic Logic Circuits

- CMOS dynamic logic circuits can be designed to provide very fast switching with modest real estate consumption
- Successfully used in several well-known chips and are the basis of DRAMS and other important computer components
- They can be quite power hungry which may limit their usage
- The clock defines the precharge and evaluate operations in every cycle
- Charge cannot be held on a capacitive node every precharge cycle will pull current from the voltage source
- Adding to the overall power dissipation of the circuit

End of Module-2