iii) The DC gate voltage and current increases losses in the thyristor. Pulsed gate drive has reduced losses.

iv) The pulsed gate drive can be easily passed through isolation transformers to isolate thyristor and trigger circuit.

### 3.2.2 Requirement of Gate Drive

The gate drive has to satisfy the following requirements:

i) The maximum gate power should not be exceeded by gate drive, otherwise thyristor will be damaged.

ii) The gate voltage and current should be within the limits specified by gate characteristics (Fig. 3.6) for successful turn-on.

iii) The gate drive should be preferably pulsed. In case of pulsed drive the following relation must be satisfied: (Maximum gate power x pulse width) x (Pulse frequency) ≤ Allowable average gate power

iv) The width of the pulse should be sufficient to turn-on the thyristor successfully.

v) The gate drive should be isolated electrically from the thyristor. This avoids any damage to the trigger circuit if in case thyristor is damaged.

e general transistor equations are,

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_C + I_B$$

$$I_B = I_E (1-\alpha) - I_{CBO}$$

ie SCR can be considered to be made up of two transistors as shown in above figure.

sidering PNP transistor of the equivalent circuit, Considering NPN transistor of the equivalent circuit,

$$I_C = I_{C_2}, I_B = I_{B_2}, I_{E_2} = I_K = I_A + I_G$$

$$I_{C_2} = \alpha_2 I_k + I_{CBO_2}$$

$$I_{C_2} = \alpha_2 (I_A + I_G) + I_{CBO_2} \qquad ---(2)$$

From the equivalent circuit, we see that

$$\therefore \qquad I_{C_2} = I_{B_1}$$

$$\Rightarrow \qquad I_A = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$



...lid only till SCR reaches ON state

$$\Rightarrow \qquad I_A = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1-(\alpha_1+\alpha_2)}$$

Two transistors analog is valid only till SCR reaches ON state

**Case 1:** When $I_g = 0$,

$$I_A = \frac{I_{CBO_1} + I_{CBO_2}}{1-(\alpha_1+\alpha_2)}$$

The gain $\alpha_1$ of transistor $T_1$ varies with its emitter current $I_E = I_A$. Similarly varies with $I_E = I_A + I_g = I_K$. In this case, with $I_g = 0$, $\alpha_2$ varies only with $I_A$. Initially when the applied forward voltage is small, $(\alpha_1+\alpha_2)<1$.

## Two Transistor Model