

of duration equal to or slightly greater than the turn-on time of the thyristor is applied.

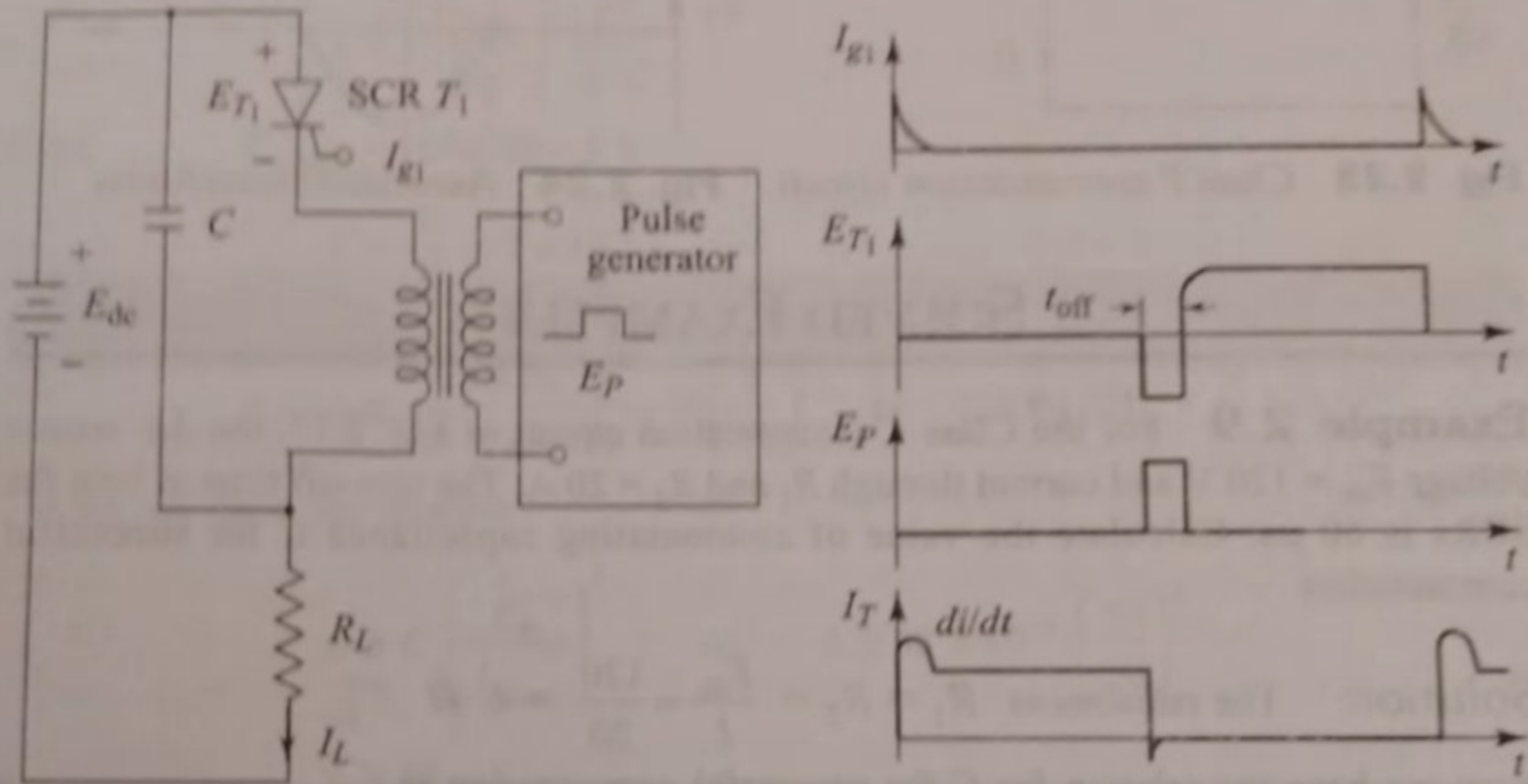
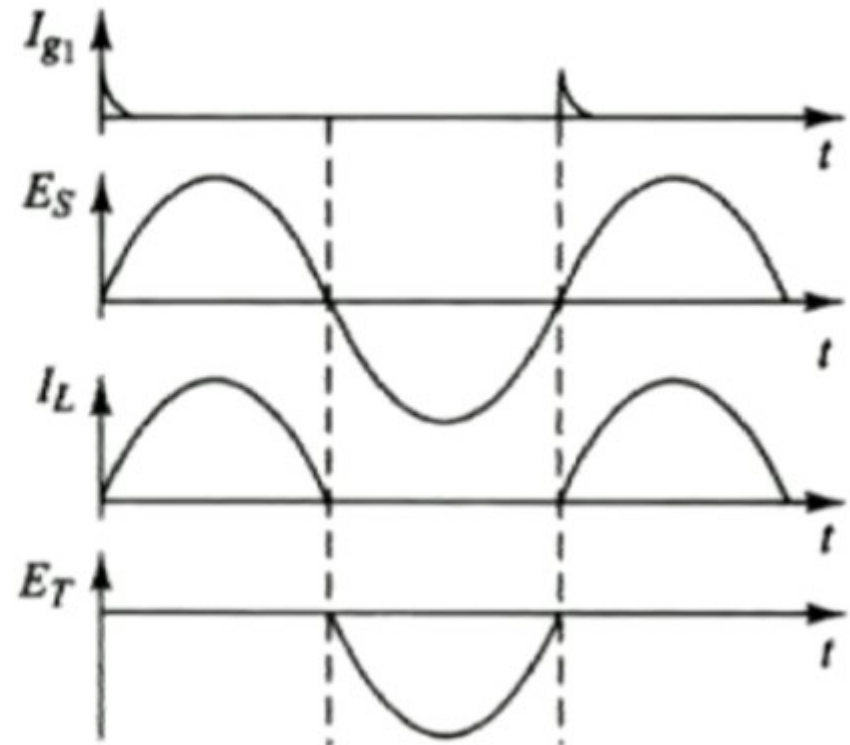
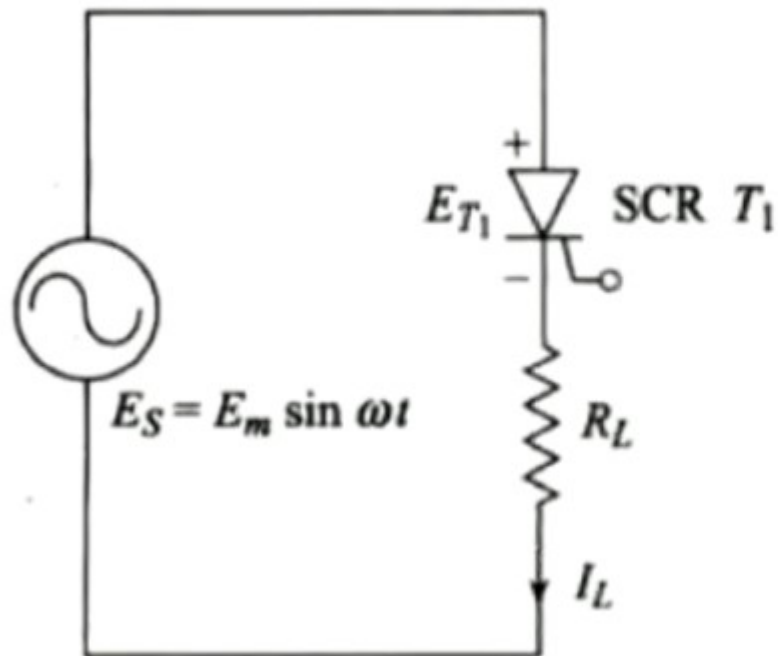


Fig. 2.22 Associated waveforms.



**Fig. 2.23** Class F commutation circuit

**Fig. 2.24** Associated waveforms

## SOLVED EXAMPLES

**Example 2.9** For the Class *C* commutation circuit of Fig. 2.17, the d.c. source voltage  $E_{dc} = 120$  V and current through  $R_1$  and  $R_2 = 20$  A. The turn-off time of both the SCRs is  $60 \mu\text{s}$ . Calculate the value of commutating capacitance  $C$  for successful commutation.

**Solution:** The resistances  $R_1 = R_2 = \frac{E_{dc}}{I} = \frac{120}{20} = 6 \text{ } \Omega$

Now, we have the relation for  $C$  for successful commutation as

$$C = 1.44 \cdot \frac{t_{\text{off}}}{R_1} = 1.44 \times \frac{60 \times 10^{-6}}{6} = 14.4 \mu\text{F}.$$

**Example 2.10** For the Class *D* commutation circuit of Fig. 2.19, compute the value of the commutating capacitor  $C$  and commutating inductor  $L$  for the following

voltage  $E_{dc} = 120$  V and current through  $R_1$  and  $R_2 = 20$  A. The turn-off time of both the SCRs is  $60 \mu\text{s}$ . Calculate the value of commutating capacitance  $C$  for successful commutation.

**Solution:** The resistances  $R_1 = R_2 = \frac{E_{dc}}{I} = \frac{120}{20} = 6 \text{ } \Omega$

Now, we have the relation for  $C$  for successful commutation as

$$C = 1.44 \cdot \frac{t_{off}}{R_1} = 1.44 \times \frac{60 \times 10^{-6}}{6} = 14.4 \mu\text{F}.$$

**Example 2.10** For the Class  $D$  commutation circuit of Fig. 2.19, compute the value of the commutations capacitor  $C$  and commutating inductor  $L$  for the following data;

$$E_{dc} = 50\text{V}, I_{L(\text{max})} = 50 \text{ A}, t_{off} \text{ of } SCR_1 = 30 \mu\text{s}$$

Chopping frequency  $f = 500$  Hz and the load voltage variation required is 10 to 100%.

**Solution:** For reliable operation, let us assume 50% tolerance on turn-off time of  $SCR_1$ .

$$\therefore t_{\text{off}} = \left( 30 + \frac{50}{100} \times 30 \right) = 45 \mu\text{s}$$

Now, we have the relation for the commutating capacitor,  $C$  as

$$C = \frac{I_L t_{\text{off}}}{E_{\text{dc}}} = \frac{50 \times 45 \times 10^{-6}}{50} = C = 45 \mu\text{F}.$$

The resetting time for capacitor voltage could be reduced by decreasing the value of  $L$ , but the peak capacitor current would increase as seen from Eq. (2.51). A large resetting time would limit the minimum voltage available at the load, which means the range of voltage available at the load is reduced.

Therefore, the minimum load voltage available is given by

$$V_{0(\min)} = \frac{t_1 - t_2}{T} E_{dc}$$

where  $t$  is chopping time period, or

$$V_{0(\min)} = \frac{\pi \sqrt{LC}}{T} E_{dc}$$

$$\therefore L \leq \left( \frac{V_{0(\min)}}{E_{dc}} \right)^2 \frac{T^2}{\pi^2 C} \quad (i)$$

Given  $V_{0(\min)} = 10\%(50) = 5 \text{ V}$

$$T = \frac{1}{f} = 2 \times 10^{-3} \text{ s}$$

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$$(2 \times 10^{-3})^2 \quad (5)^2$$

$$\therefore L \leq \left( \frac{V_{0(\min)}}{E_{dc}} \right)^2 \frac{T^2}{\pi^2 C}$$

Given  $V_{0(\min)} = 10\%(50) = 5 \text{ V}$

$$T = \frac{1}{f} = 2 \times 10^{-3} \text{ s}$$

$$\therefore L \leq \frac{(2 \times 10^{-3})^2}{\pi^2 \times 45 \times 10^{-6}} \times \left( \frac{5}{50} \right)^2 \quad \text{or} \quad L \leq 90 \mu\text{H}$$

Also, we have the relation

$$L \geq C \left( \frac{E_{dc}}{I_{L(\max)}} \right)^2 \quad \text{or} \quad L \geq 45 \times 10^{-6} \left( \frac{50}{50} \right)^2$$

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$$\therefore L \leq \frac{(2 \times 10^{-3})^2}{\pi^2 \times 45 \times 10^{-6}} \times \left(\frac{5}{50}\right)^2 \quad \text{or} \quad L \leq 90 \mu\text{H}$$

Also, we have the relation

$$L \geq C \left( \frac{E_{\text{dc}}}{I_{L(\text{max})}} \right)^2 \quad \text{or} \quad L \geq 45 \times 10^{-6} \left( \frac{50}{50} \right)^2$$

or  $L \geq 45 \mu\text{H}$

Hence, the range of commutating inductor is  $45 \mu\text{H} < L < 90 \mu\text{H}$

The choice of lower value of  $L$  would allow a larger voltage variation at the load.

## 2.11 THYRISTOR RATINGS

All semiconductor devices have definite limits to their capability and exceeding these even for short times will result in failure, loss of control, or irreversible



$$\therefore L \leq \left( \frac{V_{0(\min)}}{E_{dc}} \right)^2 \frac{T^2}{\pi^2 C} \quad (i)$$

Given  $V_{0(\min)} = 10\%(50) = 5 \text{ V}$

$$T = \frac{1}{f} = 2 \times 10^{-3} \text{ s}$$

$$\therefore L \leq \frac{(2 \times 10^{-3})^2}{\pi^2 \times 45 \times 10^{-6}} \times \left( \frac{5}{50} \right)^2 \quad \text{or} \quad L \leq 90 \mu\text{H}$$

Also, we have the relation

$$L \geq C \left( \frac{E_{dc}}{I_{L(\max)}} \right)^2 \quad \text{or} \quad L \geq 45 \times 10^{-6} \left( \frac{50}{50} \right)^2$$

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or  $L \geq 45 \mu\text{H}$

Both transistors and thyristors are semiconductor devices, but they differ in many ways as under:

<i>Transistors</i>	<i>Thyristors</i>
(1) Transistor is a three-layer, two junction device.	(1) Thyristor is a four layer, three junction device.
(2) To keep a transistor in the conducting state, a continuous base current is required.	(2) Thyristors require a pulse to make it conducting and thereafter it remain conducting.
(3) When transistors (power transistor) conduct appreciable current, the forward voltage drop is of the order of 0.3 to 0.8 V.	(3) The forward voltage drop across the device is of the order of 1.2 to 2 V.
(4) The voltage and current ratings of transistors available at present are not as high as those of thyristors.	(4) Due to the difference in fabrication and operation, thyristors with very high voltage and current ratings are available.

(9) There has been little operating experience in high power applications of transistors. Power transistors or Darlington pairs are more susceptible to failure.

(9) Thyristor circuits, on the other hand, have a proven record of many years of reliable operation.

## REVIEW QUESTIONS

- 2.1 Describe the different modes of operation of a thyristor with the help of its static  $V-I$  characteristic.
- 2.2 Describe the holding current and latching current as applicable to an SCR with the help of its static  $V-I$  characteristic.
- 2.3 With the help of a neat diagram, explain the two transistor analogy of an SCR. Also discuss the triggering conditions of SCR.
- 2.4 Give the constructional details of an SCR. Sketch its schematic diagram and the circuit symbol.