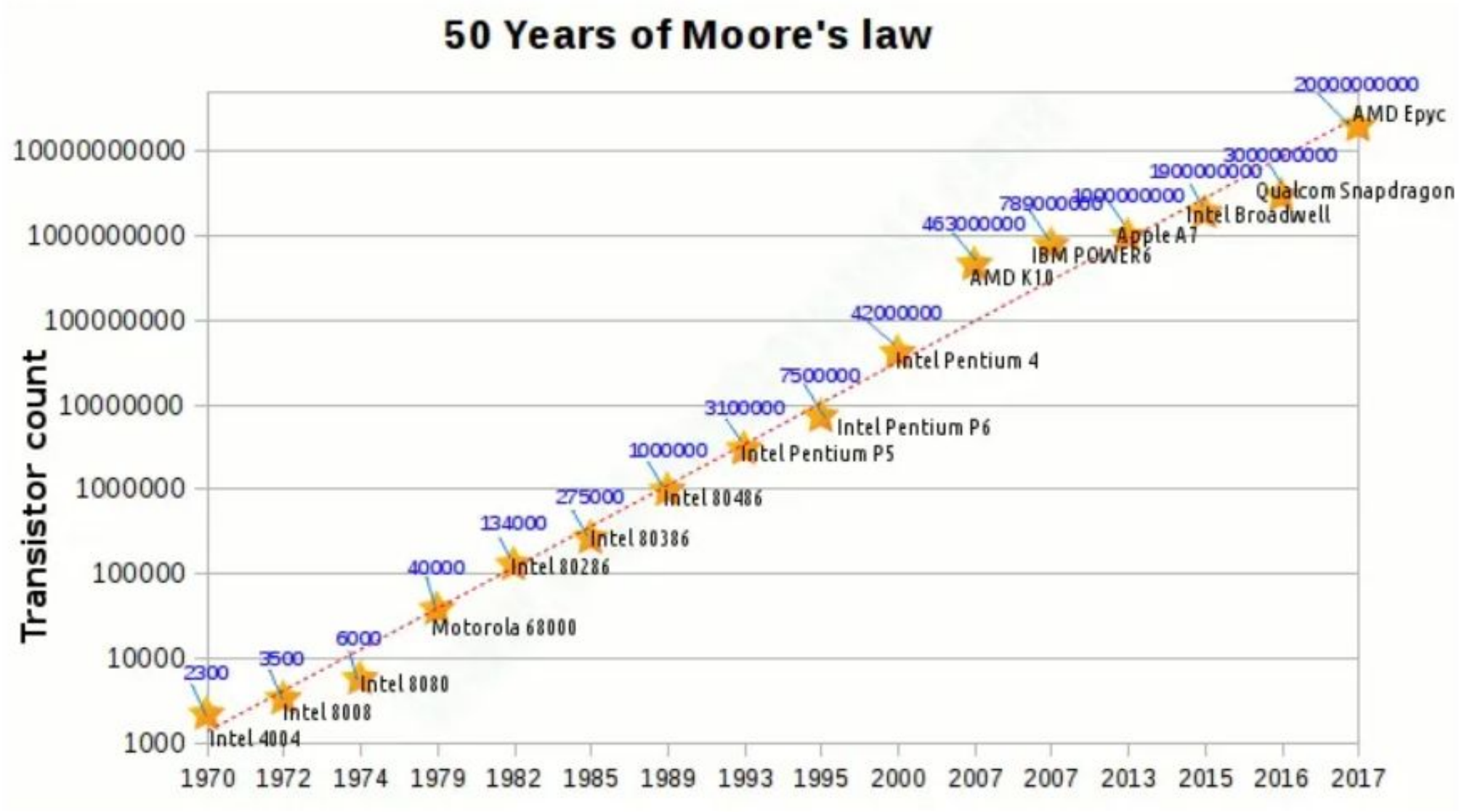
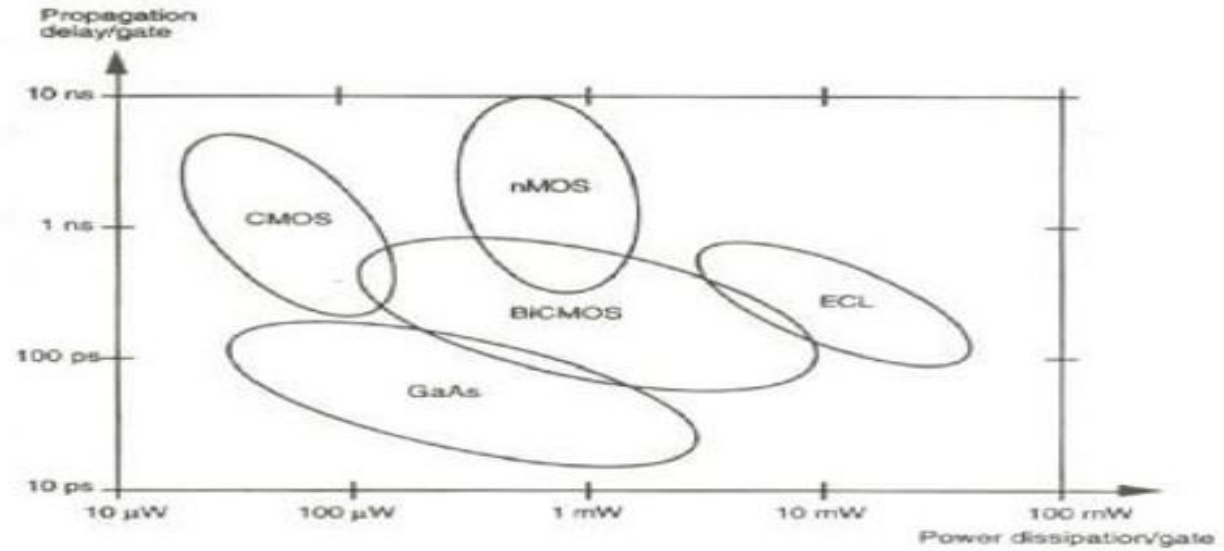
MODULE1

- **Moore‟s Law:-**
- —The number of transistors embedded on the chip doubles after every one and a half years.The number of transistors is taken on the y-axis and the years in taken on the x-axis.

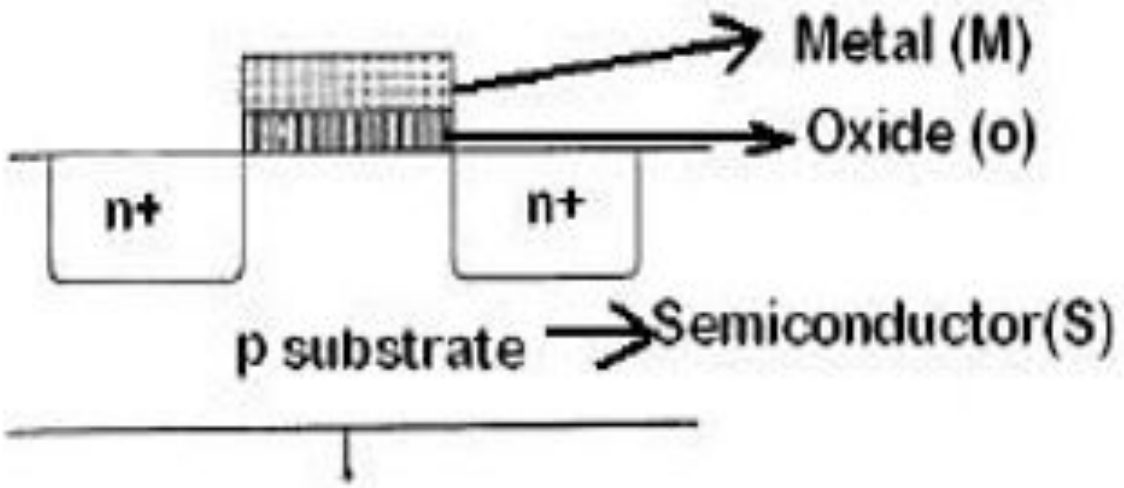

50 Years of Moore's law
Transistor count
10000000000
1000000000
100000000
10000000
1000000
100000
10000
1000
1970
1972
1974
1979
1982
1985
1989
1993
1995
2000
2007
2007
2013
2015
2016
2017
2300
Intel 4004
3500
Intel 8008
6000
Intel 8080
40000
Motorola 68000
134000
Intel 80286
275000
Intel 80386
1000000
Intel 80486
3100000
Intel Pentium P5
7500000
Intel Pentium P6
42000000
Intel Pentium 4
463000000
AMD K10
789000000
IBM POWER6
1900000000
Intel Broadwell
3000000000
Qualcom Snapdragon
20000000000
AMD Epyc

Comparison of available technologies.-speed power performance



From the graph we can conclude that GaAs technology is better but still it is not used because of growing difficulties of GaAs crystal. CMOS looks to be a better option compared to nMOS since it consumes a lesser power. BiCMOS technology is also used in places where highdriving capability is required and from the graph it confirms that, BiCMOS consumes more power compared to CMOS.

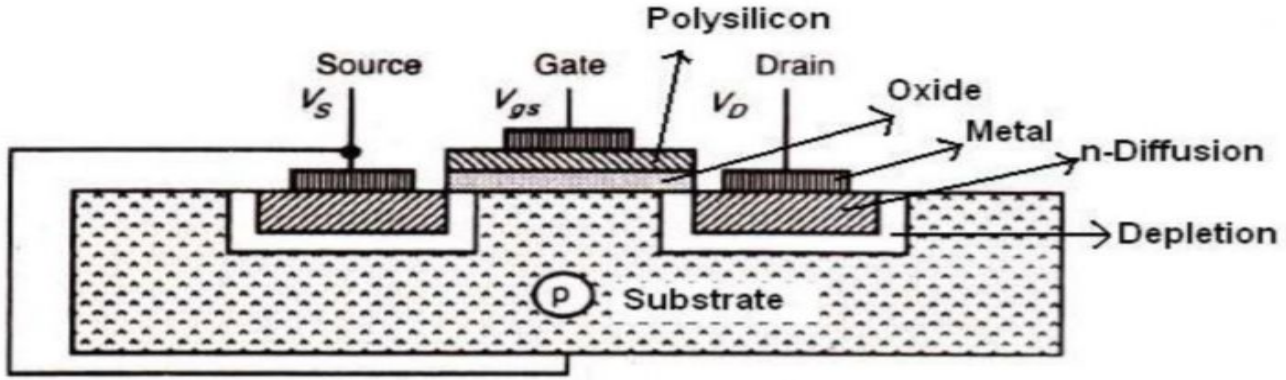
- We should first understand the fact that why the name Metal Oxide Semiconductor transistor, because the structure consists of a layer of Metal (gate), a layer of oxide (Sio2) and a layer of semiconductor. Figure below clearly tell why the name MOS.



- We have two types of FETs. They are Enhancement mode and depletion mode transistor.
- Also we have PMOS and NMOS transistors.
- In **Enhancement mode transistor** channel is going to form after giving a proper positive gate voltage. We have NMOS and PMOS enhancement transistors.
- In **Depletion mode transistor** channel will be present by the implant. It can be removed by giving a proper negative gate voltage. We have NMOS and PMOS depletion mode transistors.

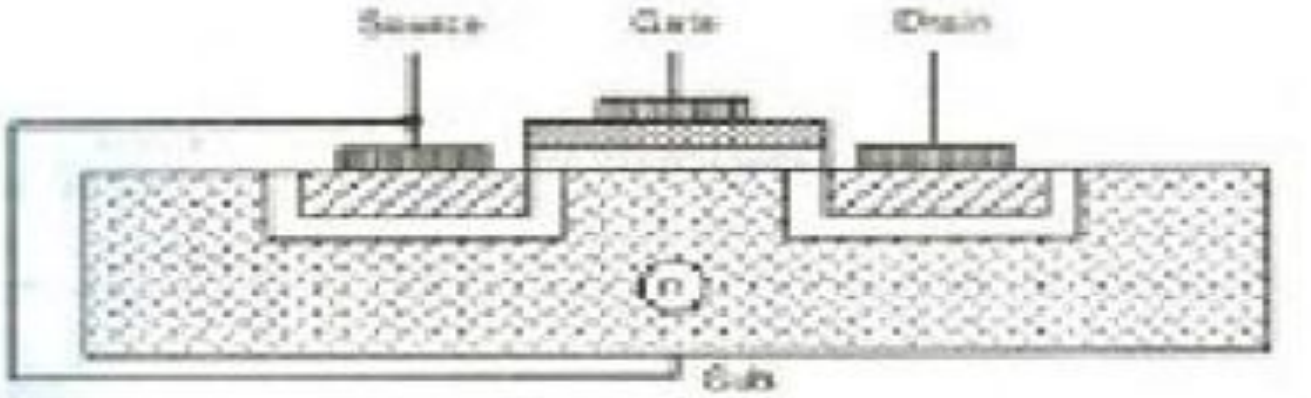
N-MOS enhancement mode transistor:-

- This transistor is normally off. This can be made ON by giving a positive gate voltage.
- By giving a +ve gate voltage a channel of electrons is formed between source drain.



P-MOS enhancement mode transistor:-

- This is normally on. A Channel of Holes can be performed by giving a –ve gate voltage.
- In P-Mos current is carried by holes and in N-Mos it‘s by electrons. Since the mobility is of holes less than that of electrons P-Mos is slower.



N-MOS depletion mode transistor:-

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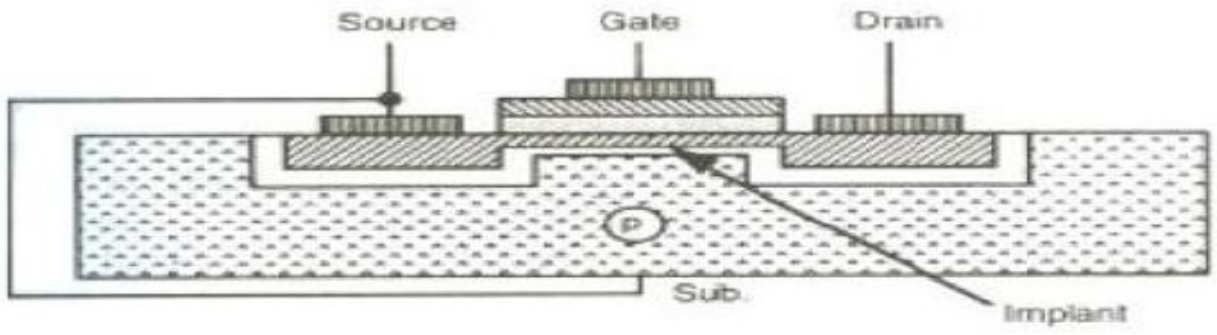
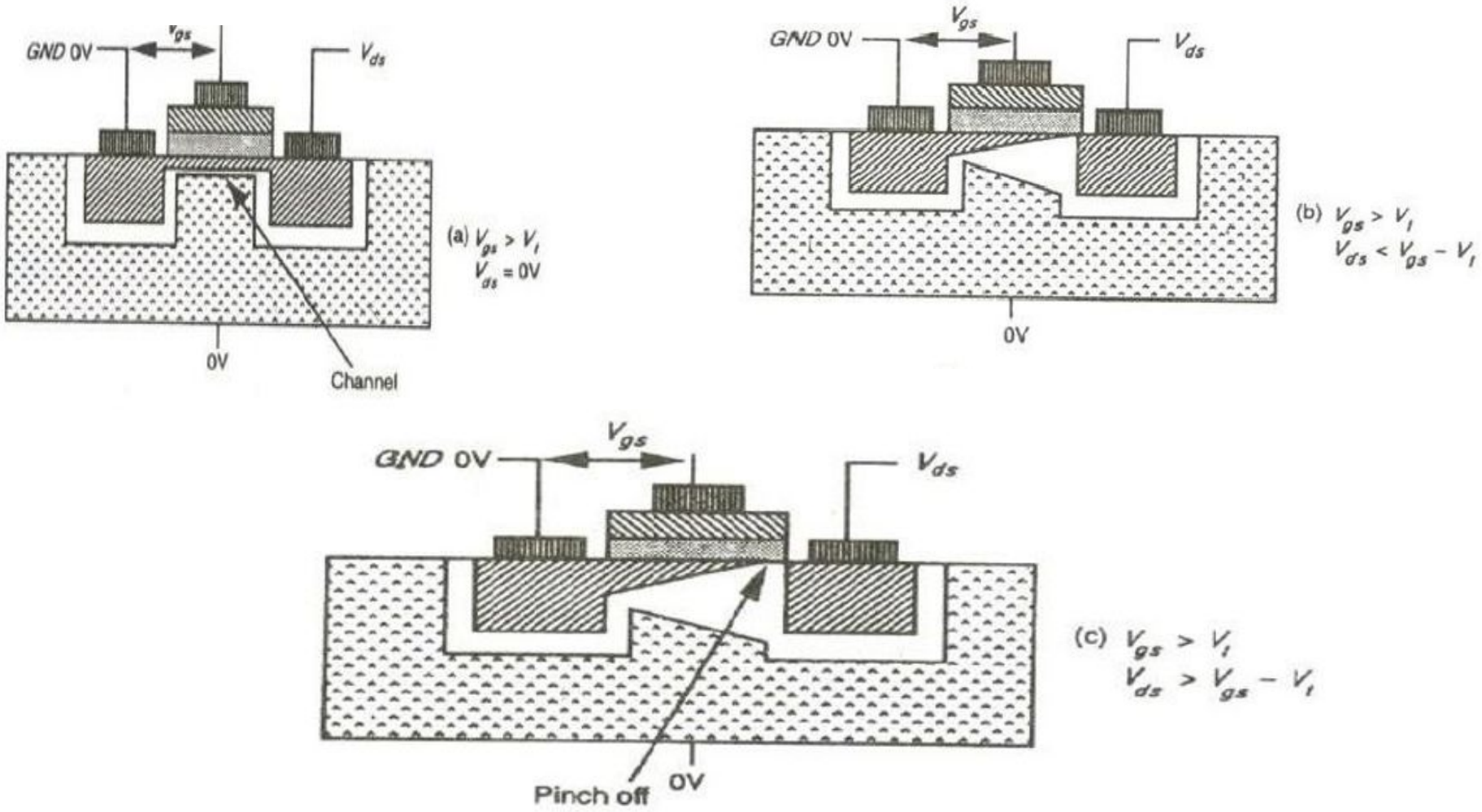
- This transistor is normally ON, even with Vgs=0. The channel will be implanted while fabricating, hence it is normally ON. To cause the channel to cease to exist, a – ve voltage must be applied between gate and source.



Enhancement mode Transistor action:-



- To establish the channel between the source and the drain a minimum voltage (Vt) must be applied between gate and source. This minimum voltage is called as —Threshold Voltage .
- The complete working of enhancement mode transistor can be explained with the help of diagram a, b and c.

a) $V_{gs} > V_t$
$V_{ds} = 0$

Since $V_{gs} > V_t$ and $V_{ds} = 0$ the channel is formed but no current flows between drain and source.

b) $V_{gs} > V_t$

$V_{ds} < V_{gs} - V_t$

This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased (hence more depletion region towards the drain end) and the channel starts to pinch. This is called as the pinch off point.

c) $V_{gs} > V_t$

$V_{ds} > V_{gs} - V_t$

•This region is called Saturation Region where the drain current remains almost constant. As the drain voltage is increased further beyond (Vgs-Vt) the pinch off point starts to move from the drain end to the source end. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current. The typical threshold voltage for an enhancement mode transistor is given by $V_t = 0.2 * V_{dd}$.

Depletion mode Transistor action:-

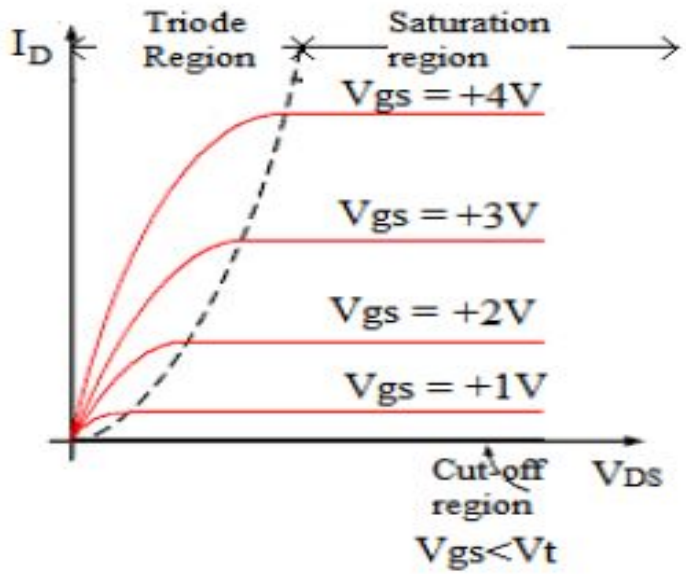
We can explain the working of depletion mode transistor in the same manner, as that of the enhancement mode transistor only difference is, channel is established due to the implant even when Vgs = 0 and the channel can be cut off by applying a –ve voltage between the gate and source. Threshold voltage of depletion mode transistor is around 0.8*Vdd.

I_D-V_{DS} Characteristics of MOS Transistor :

The graph below shows the I_D Vs V_{DS} characteristics of an n- MOS transistor for several values of Vgs .It is clear that there are two conduction states when the device is ON, they saturated state and the non-saturated state. The saturated curve is the flat portion and defines the saturation region. For Vgs < V_{DS} + Vt, the nMOS device is conducting and I_D is independent of V_{DS}.

For Vgs > V_{DS} + Vth, the transistor is in the non-saturation region and the curve is a half parabola.

When the transistor is OFF (Vgs < Vt), then I_D is zero for any V_{DS} value.



The boundary of the saturation/non-saturation bias states is a point seen for each curve in the graph as the intersection of the straight line of the saturated region with the quadratic curve of the non-saturated region. This intersection point occurs at the channel pinch off voltage called V_{DSAT}. V_{DSAT} is defined as the minimum drain-source voltage that is required to keep the transistor in saturation for a given Vgs .

In the non-saturated state, the drain current initially increases almost linearly from the origin before bending in a parabolic response. Thus the name, ohmic or triode or linear for the non- saturated region. The drain current in saturation is virtually independent of V_{DS} and the transistor acts as a current source. This is because there is no carrier inversion at the drain region of the channel. Carriers are pulled into the high electric field of the drain/substrate pn junction and ejected out of the drain terminal.