## Drain to Source Current $I_{ds}$ versus Voltage $V_{ds}$ Relationships

$$I_{ds} = -I_{sd} = \frac{\text{Charge induced in channel}(Q)}{\text{Electron Transit Time}(\tau)}$$

$$\tau_{sd} = \frac{\text{Length of channel}(L)}{\text{Velocity}(v)}$$

$$v = \mu E_{ds}$$

$\mu$ = *electron or hole mobility(surface)*

$E_{ds}$ = *electric field(drain to source)*

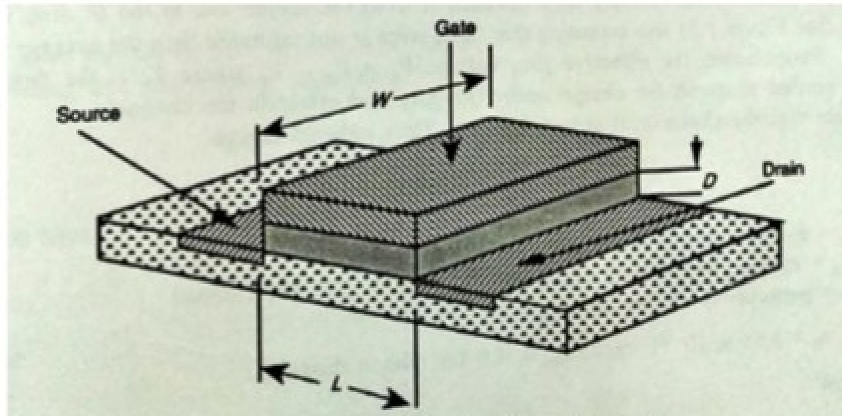


FIGURE 2.1 nMOS transistor structure.

$$E_{ds} = \frac{V_{ds}}{L} \qquad v = \frac{\mu V_{ds}}{L}$$

*Typical Values of μ at room temperature*

*Thus, Transit Time is*

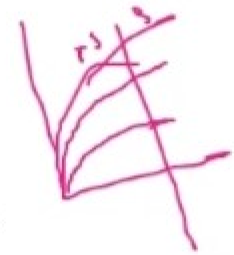
$$\tau_{sd} = \frac{L}{\frac{\mu V_{ds}}{L}} = \frac{L^2}{\mu V_{ds}}$$

$\mu_n = 650\ cm^2/V\ sec\ (surface)$

$\mu_p = 240\ cm^2/V\ sec(surface)$

USHA C

$$\tau_{sd} = \frac{L^2}{\mu V_{ds}} \qquad (2)$$



**The Non Saturated region**

- Charge induced in channel due to gate voltage is due to the voltage difference between the gate and channel
- Voltage along the channel varies linearly with distance X from the source due to the IR drop in channel
- Device in non saturated then the average value is Vds/2
- The effective gate voltage Vb=Vgs-Vt
- Vt is the threshold voltage needed to invert the charge under the gate and establish the channel

$$\text{Charge/uni t area} = E_g \varepsilon_{ins} \varepsilon_0$$

Induced Charge is

$$Q_c = E_g \varepsilon_{ins} \varepsilon_0 WL \qquad \varepsilon_0 = 8.85\times10^{-14} Fcm^{-1}$$

$$\varepsilon_{ins} = 4.0 \quad \textit{for Silicon dioxide}$$

Eg= average electric field gate to channel

$\varepsilon_{ins}$ = relative permittivity of insulation between gate and channel

$\varepsilon_0$ =permittivity of free space

$$E_g = \frac{\left( (V_{gs} - V_t) - \frac{V_{ds}}{2} \right)}{D}$$

D- oxide thickness

$$Q_c = \frac{WL\varepsilon_{ins}\varepsilon_0}{D}\left( (V_{gs} - V_t) - \frac{V_{ds}}{2} \right) \qquad (3)$$

Combining equations (2) and (3) in (1), we have

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0 \mu}{D}\frac{W}{L}\left( (V_{gs} - V_t) - \frac{V_{ds}}{2} \right)V_{ds}$$

$$I_{ds} = K\frac{W}{L}\left( (V_{gs} - V_t)V_{ds} - \frac{V^2{}_{ds}}{2} \right) \qquad (4)$$

In the non-saturated or resistive region where $V_{ds} \langle V_{gs} - V_t$

$$K = \frac{\varepsilon_{ins}\varepsilon_0 \mu}{D}$$

The factor W/L is of course, contributed by the geometry and it is common practice to write

$$\beta = K\frac{W}{L}$$

$$I_{ds} = \beta\left( (V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right) \qquad (4a)$$

USHA C

$$I_{ds} = k\frac{W}{L}\left[(V_{gs}-V_t)(V_{gs}-V_t) - \frac{(V_{gs}-V_t)^2}{2}\right]$$

$$= k\frac{W}{L}\left[(V_{gs}-V_t)^2 - \frac{(V_{gs}-V_t)^2}{2}\right]$$

## The Saturated Region

- Saturation begins when Vds=Vgs-$V_t$ since at this point the IR drop in the channel equals the effective gate to channel voltage at the drain.
- The current remains constant as Vds increases

$$= k\frac{W}{L}\left[\frac{(V_{gs}-V_t)^2}{2}\right]$$

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs}-V_t)^2}{2} \qquad (5)$$

Or we may write

$$I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2 \qquad (5a)$$

$$I_{ds} = K\frac{C_g\mu}{2L^2}(V_{gs}-V_t)^2 \qquad (5b)$$

we may also write

$$I_{ds} = C_0\mu\frac{W}{2L}(V_{gs}-V_t)^2 \qquad (5c)$$

Threshold voltage for nMOS depletion mode device denoted as Vtd

USHA C

## Aspects of MOS Transistor Threshold Voltage Vt

The threshold voltage Vt may be expressed as

$$V_t = \phi_{ms} \frac{Q_B - Q_{SS}}{C_0} + 2\phi_{fN} \qquad (6)$$

Where

$Q_B$= the charge per unit area in the depletion layer beneath the oxide

Qss=Charge density at Si:SiO2 interface

C0=capacitance per unit gate area

$\phi_{ms}$=Workfunction difference between gate and Si

$\phi_{fN}$= Fermi level potential between inverted surface and bulk Si

$$\left.\begin{array}{l} V_{SB} = 0\text{ V};\ V_t = 0.2V_{DD}\ (= +1\text{ V for } V_{DD} = +5\text{ V}) \\ V_{SB} = 5\text{ V};\ V_t = 0.3V_{DD}\ (= +1.5\text{ V for } V_{DD} = +5\text{ V}) \end{array}\right\} \text{Similar but negative values for pMOS}$$

**For nMOS depletion mode transistors:**

$$V_{SB} = 0\text{ V};\ V_{td} = -0.7V_{DD}\ (= -3.5\text{ V for } V_{DD} = +5\text{ V})$$

$$V_{SB} = 5\text{ V};\ V_{td} = -0.6V_{DD}\ (= -3.0\text{ V for } V_{DD} = +5\text{ V})$$

# MOS TRANSISTOR TRArNSCONDUCTANCE *gm,* AND OUTPUT CONDUCTANCE gds

Transconductance expresses the relationship between output current and the input voltage is defined as

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} \,|V_{ds} = \text{constant}$$

To find an expression for gm in terms of circuit and transistor parameters, consider the charge in channel Qc is such that

$$\frac{Q_c}{I_{ds}} = \tau$$

Where τ is transit time. Thus change in current

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$\delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$$

$$\delta I_{ds} = \frac{\delta Q_c V_{ds} \mu}{L^2}$$

USHA C

but change in charge

$$\delta Q_c = C_g \delta V_{gs}$$

so that

$$\delta I_{ds} = \frac{C_g \delta V_{gs} \mu V_{ds}}{L^2}$$

Now

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

In saturation

$$V_{ds} = V_{gs} - V_t$$

$$g_m = \frac{C_g \mu}{L^2} (V_{gs} - V_t) \tag{2.7}$$

and substituting for $C_g = \dfrac{\varepsilon_{ins} \varepsilon_0 WL}{D}$

$$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0}{D} \frac{W}{L} (V_{gs} - V_t) \tag{2.7a}$$

Alternatively,

$$g_m = \beta (V_{gs} - V_t)$$