Dayananda Sagar College of Engineering

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Department of Electronics & Communication Engg.

Continuous Internal Evaluation – III

Course Name :	**FOVLSI**	Date :	/06/2021
Course Code :	**18EC6DCFOV**	Day :	day
Semester & Section :	6th A,B,C,D	Timings :	
Max Marks : 50 M	50 Mks	Duration :	1½ Hrs.
Subject handling teacher's name & sign	Dr.P.Vimala, Dr.C.Usha, Prof.Madhura, Prof. Santosh		
HOD Name & Sign	Dr. T.C.Manjunath		

No.		Question Description	Mks	CO & Levels
Q1	(a)	In DRAM, i)Periodic refreshing is not required ii)Information is stored in a capacitor iii) Information is stored in a latch iv) Both read and write operations can be performed simulataneously	1	
	(b)	Which memory is difficult to interface with processor i)Static Memory ii) Dynamic Memory iii) ROM iv) None of these	1	
	(c)	Floating gate transistor in Flash memory has i)two gates ii) one gate iii) two sources iv) two drains	1	
	(d)	Transistors in NAND type flash are connected in i)Series ii) Parallel iii) Cascade iv) randomly	1	
	(e)	Which has high storage capacity. i)NOR type flash ii) NAND type flash iii) both (i) and (ii) iv) None of the mentioned	1	
	(f)	In MOSFET amplifier the parameter that changes due to the changes in input is i) Small signal drain current ii) Large signal drain current iii)Voltage across substrate and source iv) None of the mentioned	1	
	(g)	Input impedence of MOSFET amplifier in common source configuration is i)very high at high frequency ii) very high at low frequency iii) very low at high frequency iv) very low at low frequency	1	
	(h)	Voltage gain of the MOSFET is given by i)Av=-βRd ii) Av=-γRd iii) Av=-gmRd iv) None of the mentioned	1	
	(i)	The MOSFET for highest gain, one should use _____ configuration i)CC ii)CB iii)CE iv) None of the mentioned	1	
	(j)	According to the principle of current mirror, if gate-source potentials of two identical MOS transistors are equal, then the channel currents should be _____ i) Equal ii) Different iii) Both a and b iv)None of the above	1	
Q2	(a)	Explain one Transistor DRAM read and write operation	6	CO4 L2
	(b)	Design the pseudo NMOS ROM with the following contents. Word0:010101, Word1:001100, Word2:011010, Word3:111100	4	CO4 L6
Q3	(a)	Explain the large signal and small signal behavior of Source Follower	10	CO5 L2

Q4	(a)	With neat cross sectional of floating gate nMOS explain the role of floating gate in PROMs and its applications	6	CO4 L2
	(b)	Explain the NAND ROM with diagram	4	CO4 L2
		OR		
Q5	(a)	Explain in detail the Content Addressable Memory with neat diagrams	10	CO4 L2
Q6	(a)	Derive an voltage gain expression for the MOSFET device by considering input signal v_{gs}	10	CO5 L5
		OR		
Q7	(a)	Write a Short notes on i) T-Equivalent Circuit Model of MOSFET ii) Basic Current Mirrors	10	CO5 L2