2. nMOS depletion mode transistor pull-up

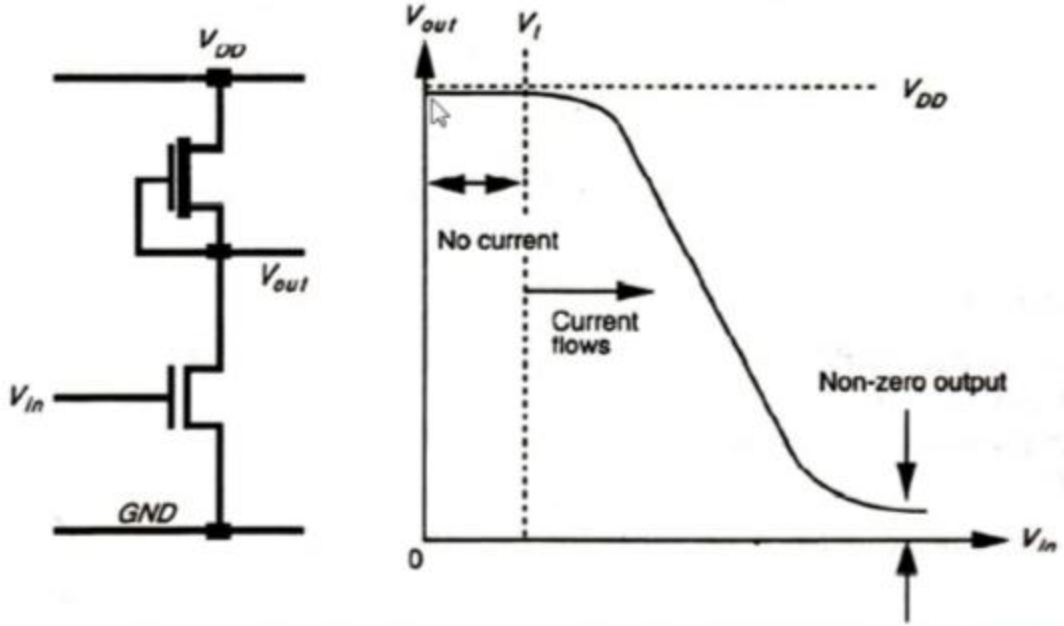
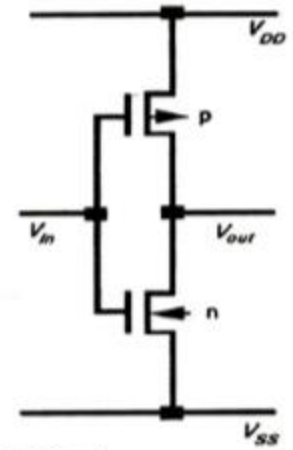
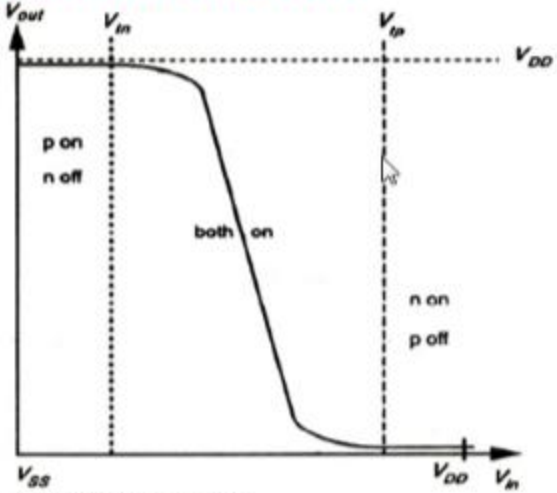


FIGURE 2.12 nMOS depletion mode transistor pull-up and transfer characteristic.

4. Complementary transistor pull up (CMOS)



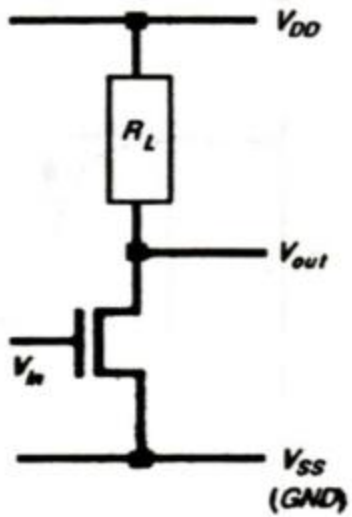
(a) Circuit



(b) Transfer characteristic

Alternative forms of Pull-Up

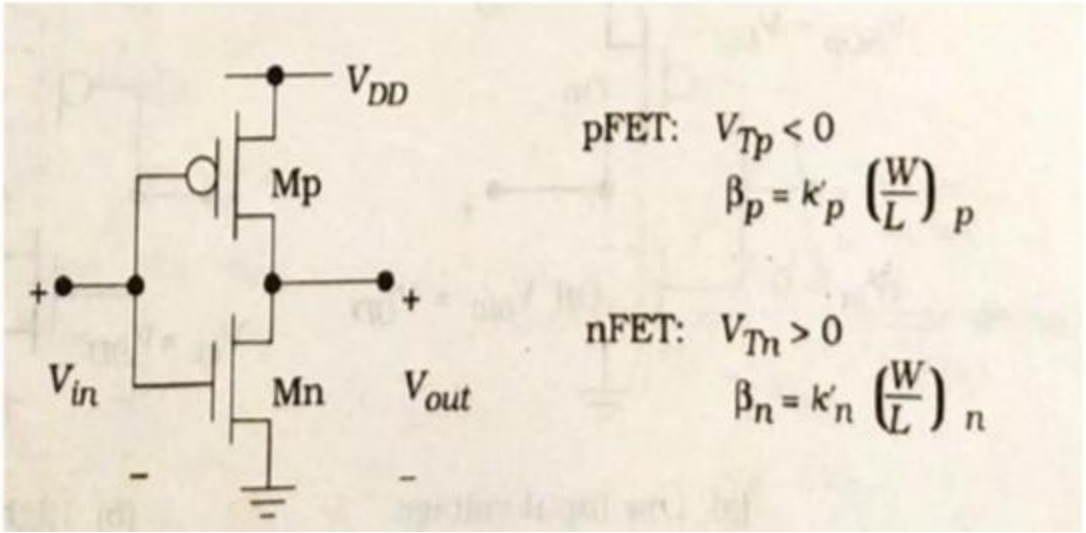
1. Load resistance RL



DC Characteristics of the CMOS Inverter

1. DC Analysis

2. Transient Analysis



pFET: $V_{Tp} < 0$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

nFET: $V_{Tn} > 0$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

Voltage Transfer Characteristics

VOH=VDD

VOL=0V

VL=VOH-VOL=VDD

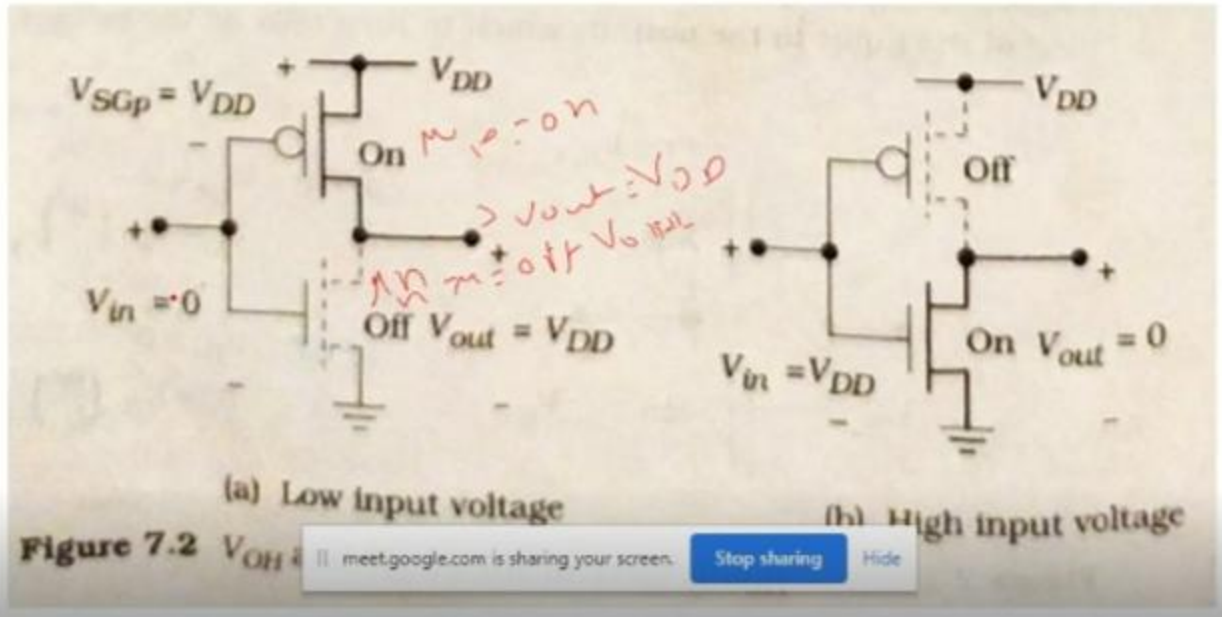


Figure 7.2 V_{OH}

The VTC for the circuit is obtained by starting with an input voltage of Vin=0 and then increasing it up to the value of Vin=VDD

VGsn=Vin

VGsp=VDD-Vin

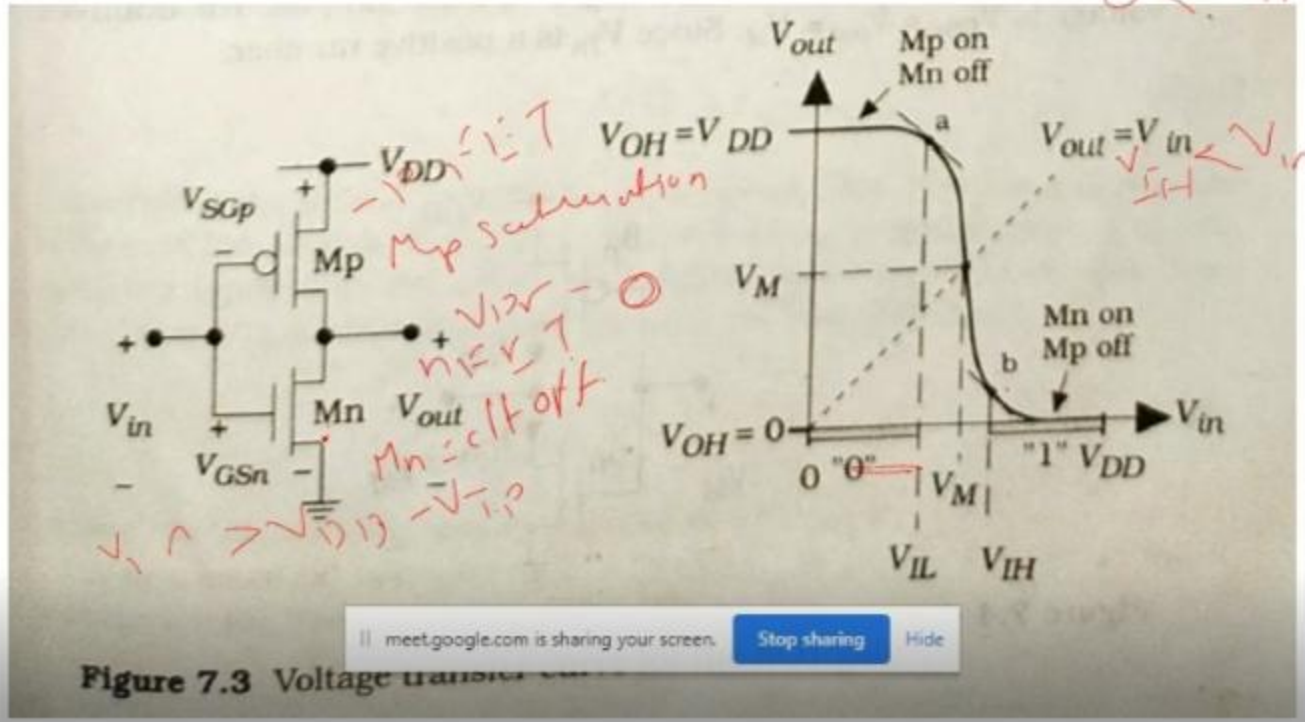


Figure 7.3 Voltage transfer curve

Inverter Voltages for VM calculations

$V_M = V_{out} = V_{in}$

$I_{Dp} = I_{Dn}$

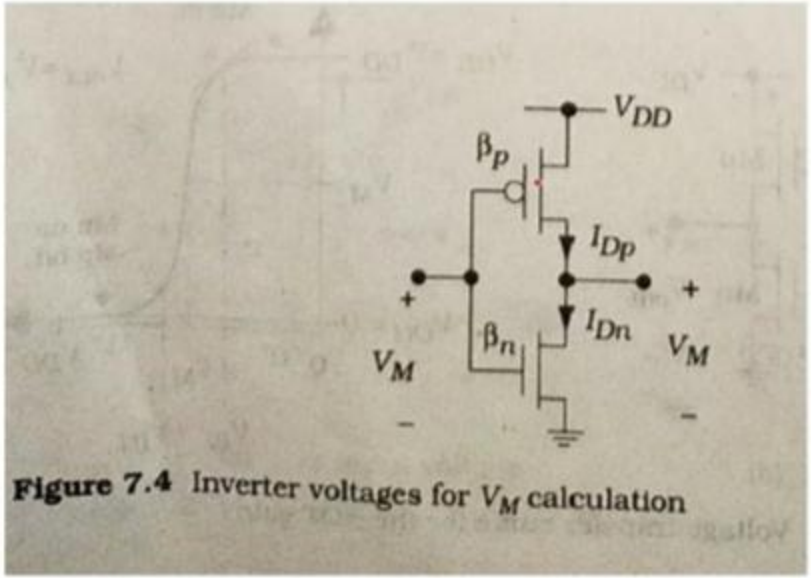


Figure 7.4 Inverter voltages for V_M calculation

To calculate the midpoint voltage we set $V_{in} = V_{out} = V_M$ as shown in Figure 7.4. Equating the drain currents of the FETs gives

$$I_{Dn} = I_{Dp} \tag{7.9}$$

but we need to find the operating region (saturation or non-saturation) of each FET before we can use the expression. Consider first the nFET and recall that the saturation voltage is given by

$$\begin{aligned} V_{sat} &= V_{GSn} - V_{Tn} \\ &= V_M - V_{Tn} \end{aligned} \tag{7.10}$$

where we have used $V_{in} = V_{GSn} = V_M$ in the second line. The drain-source voltage is $V_{DSn} = V_{out} = V_M$. Since V_{Tn} is a positive number,

$$V_{DSn} > V_{sat} = V_M - V_{Tn} \tag{7.11}$$

which says that Mn must be saturated. The same arguments can be applied to the pFET Mp since $V_{SGp} = V_{SDp}$. Using the saturation current equations from Chapter 6 gives

$$\frac{\beta_n}{2}(V_M - V_{Tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \tag{7.12}$$

Dividing by β_p and taking the square root gives

$$\sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{Tn}) = V_{DD} - V_M - |V_{Tp}| \tag{7.13}$$

Simple algebra then gives the midpoint voltage as

$$V_M = \frac{V_{DD} - |V_{Tp}| + \sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{7.14}$$

This equation shows that V_M is set by the nFET-to-pFET ratio

$$\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p} \tag{7.15}$$

$$\frac{k'_n}{k'_p} = 2 \text{ to } 3 \tag{7.16}$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r \quad \diamond \tag{7.17}$$

$$V_M = \frac{1}{2} V_{DD} \tag{7.18}$$

in equation (7.12). Rearranging gives us the design equation

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{1}{2} V_{DD} - |V_{Tp}|}{\frac{1}{2} V_{DD} - V_{Tn}} \right)^2 \tag{7.19}$$

This allows us to compute the transistor sizes for this particular choice of V_M. Note that if $V_{Tn} = |V_{Tp}|$, then a symmetric design requires that

$$\beta_n = \beta_p \tag{7.20}$$