Explain how UART is used for communication highlighting the advantages of UART.

June-07,6M

UART takes parallel data and transmits serially & UART receives serial data and converts to parallel.

A simple UART may possess

- i) Some configuration registers &
- ii) Two independently operating processors, one for receiving and the other for transmitting.

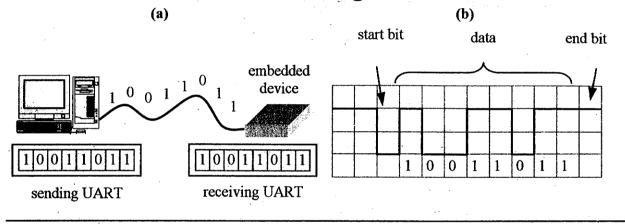


Figure 1: Serial transmission using UARTs, (a) A PC communicating serially with an embedded device, (b) transmission protocol used by the two UARTs.

- \* The transmitter may posses a negister called a transmit buffer, that holds data to be sent. This negister is a shift negister, so the data can be transmitted one bit at a time by shifting at the appropriate nate.
- \* The neceiver neceives data into a shift negister, and then the data can be need in parallel The neceiver in constantly monitoring the neceive pin (91%) for a start bit. The steart bit is typically dignaled by a hight to low transition on the Mx pin

\* After the start bit has been detected, the succeiver starts

Sampling the orx pin at predetermined interreals shifting each sampled bit into the neceive shift negister \* To determine whether the transmitted data is correct, the transmitter transmits an additional parity bit.

The VART can be configured to check for even pevily or no parity at all once data is received, the VART signals its host processor. The host processor in two reads the byte out of the neceive shift negister. The neceiver is now neady to neceive more data.

# Towarsmitter Operation:

The host processor (Txing side processor) writes a byte to the transmit buffer of the VART, the transmitter sends a start bit over its transmit pin (tx), signaling the beginning of a transmission to the semale VART. Then, the transmitter shifts out the data in its transmit buffer over its trx pin at a predeter mined rate.

(Txen can also Tx its an additional pairity bit)

At this point, the UART processor signals its host
processor, indicating that it is ready to send more
data if available.

\* The transmission protocol used by VART's determines the rate at which bits are sent and received 8 is called band rate. The protocal also specifies the number of bits of data and the type of parity sent during each transmission.

\* The bandrate determines the speed at which data is exchanged between two socially connected UART'S. The

commonly used bound rates are 2400, 4200, 9600 & 19200.

- \* To use a UART, we must configure its band rate by writing to the configuration negister, and then we must write data to the transmit negister and for nead data from the necessued negister.
- \* To use a VART, we must configure its bound rate by writing to the configuration negister, and then we must write data to the transmit negister and for nead data from the neceived negister.

for ex, to configure the VART of an 8051 microcontroller we must use the following equation:

Whore,

smod coversponds to 2-bits in a special-function register, osc freq is the frequency of the oscillator, & TH1 is an 8-bit rate register of a build-in timer.

Determine the values for smod and TH1 to generate a baud t=rate of 9600 for the 8051 baud rate equation, assuming an 11.981MHz oscillator. Remember that smod is a 2 bit and TH1 is 8-bits. There is more than one correct answer.

Bandrate = 
$$\left(\frac{3^{\text{Smod}}}{32}\right) * \frac{080 \text{ freq}}{[12 \times (256 - \text{TH1})]}$$
  
for smod = 2 = 10:-

$$9600 \leftarrow \left(\frac{2^2}{32}\right) * \frac{11.981 \times 10^6}{\left[12 \times (956 - TH1)\right]}$$

$$76,800 = \frac{11.981 \times 10^{\circ}}{12 \times (956 - TH1)}$$

$$12 \times 256 - 12 \text{ TH1} = \frac{11.981 \times 10^6}{76800}$$

$$3072 - 127H1 = 11.981 \times 10^{6}$$

$$12TH1 = 3072 - 156,0026$$

for smod = 3 = 11:

$$9600 = \frac{2^3}{32} \times \frac{11.981 \times 10^6}{[12 * (256 - TH1)]}$$

$$\frac{9600 \times 32}{8} = \frac{11.981 \times 10^{6}}{[12 \times (256-TH1)]}$$

$$38,400 = \frac{11.981 \times 10^{C}}{(12 \times 256 - 12 \text{ TH 1})}$$

$$3072 - 12TH1 = 11.981 \times 10^{6}$$
 $38400$ 
 $3072 - 12TH1 = 312.0052$ 
 $12TH1 = 3072 - 312.0052$ 
 $12TH1 = 2759.994$ 
 $TH1 = 229.99$ 
 $TH1 = 230 = 11100110$ 

#### PULSE WIDTH MODULATION (PWM) :-

Describe the working of PWM unit with timing diagrams. How can it be used for speed control of DC motor.

June-11,10M

\* With a neat diagram, explain how the pulse width modulator works. What are the considerations in selecting the clock, the prescalar and the counter? Assuming an 8-bit up counter, calculate the count to be loaded in the 'cycle-high' register to get pulses of duty cycle 75%.

Jan-11,10M June-06,10M

\* Describe the working of a PWM unit with a circuit and waveform.

June-09,6M

Describe the working of a PWM unit with timing diagrams. How it can be used for speed control of DC motor.

Jan-08,8M

Schematically explain how a PWM helps in controlling the speed of DC motor.

June-07,6M

### ❖ How PWM can be used for speed control of DC motor? Explain.

Jan-07,8M

## Pulse width Modulator (PWM):-

\* I pulse width modulator (PWM) generates an elp signal that repeatedly switches between high and low values

\* We control the diviation of the high value and of the low value by indicating the desired period (T) & the desired duty cycle (D).

\* Duty cycle is defined as the scatio of on time to the total period (on + off) & is enpressed in percentage.

$$\left\{ \int \int D = \frac{T_{\text{on}}}{T_{\text{on}} + T_{\text{off}}} \times 100 \right\}$$

\* There are 3 common use of PWM:

- 1) To generate a clock-like signal to another device ex:-PWM can be used to blink a light at a specific rate.
- 2) To control the average current or voltage input to a device.

Ex: A DC electric motor rotates when its input voltage is set high, with the notation speed proportional to the input voltage level.

Suppose the revolutions per minerte (rpm) equals 10 Times the input voltage. To achieue a desired rpm of 125, we

we would need to set the input voltage to 1.25V, where as achieving 250 rpm would require an input vallage of 2.50V

3) To encode control commands in a single signal for use by another device.

en: We muy control a radio-controlled can by sending puelses of different widths.

A width of 1-mes corresponds to a twin left command, a 4-msec width to twin sight, and an 8-msec width to forward.

\* The PWM approach makes use of the fact that a DC motor does not come to an immediate stop when its input voltage is lawered to 'o', but nother its it coasts.

Thus the average input voltage is set to obtain the desired speed.

using a pwm, duty cycle is set to achieve the appropriate average voltage.

- \* Assuming the PWM's out is 5V when high and ov when low, then.
- \* We can obtain an average of 0 1.25V by setting the duty cycle to 25.1. ie  $5V \times 25$ 1. = 1.25V. This duty cycle in shown in fig 1@.  $5V \times 0.25 = 1.25V$ .

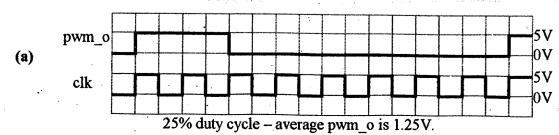
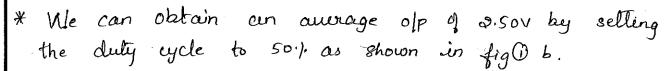
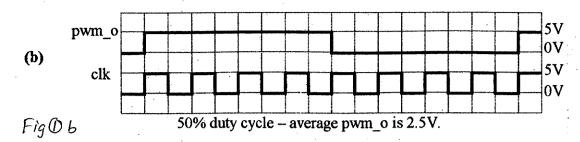


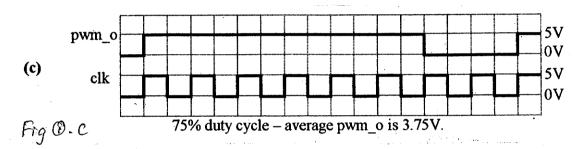
Fig Da.



0.5 x5V = 2.5V



\* A duty cycle of 75% would result in accorage of of 3.75 V as shown in fig 10.



### Controlling a DC Motor Using a PWM

\* The speed of the DC Motor is proportional to the voltage applied to the motor. We must set the duty cycle of a PWM such that the average of voltage equals the desired voltage.

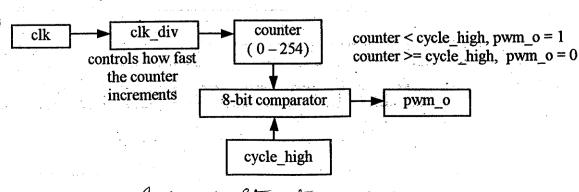


Fig 1@: Internal Structure of PWM
Lig 1@: Internal Structure of PWM

- \* There are two 8 bit registers called <u>clk-div</u> and <u>cycle-high</u>, an <u>8 bit counter</u> and an 8-bit comparator as shown in fig 1. @.
- \* Initially, the value of CIK-div is loaded into the register. The CIK-div negister works as a clock divider. After a specifical amount of time has elapsed, a pulse is sent to the counter negister. This causes the counter negister to increment itself. The comparator then looks at the values in the counter negister state cycle-high negister.
- \* When the counter value < cycle\_high, a 1 (+5 v) is outputted.

  When the counter value > cycle\_high, a 0 (ov) is outputted.
- \* When the counter value reaches 254, counter is neset to o and the process repeats. Thus clk-div determines the PMM's period, specifying the number of cycles in the period.
  - The negister cycle-high determines the duty cycle, indicating how many of periods cycle output a 1.

    If the cycle-high is set to 255 (FFh), the op signal is always high nescelling in a duty cycle of 100%.
    - The cycle-high is set to o(ooh), the opsignal is always law resulting in a duty cycle of oil
- If the value loaded to the clt\_div is too low, the value autputted by the comparator oscillates too quickly. The comparator never outputs zeros long enough for the DC motor to slow down, causing the DC motor to continuesly run at full speed.
  - Selling the value of clk\_div to ffh, in this case it warks best.

\* The relationship between applied voltage & Dc motar speed:

input voltage	% of maximum voltage applied	RPM of DC motor
0	0	0
2.5	50	4,600
3.75	75	6,900
5.0	100	9,200

 $\times$  For the motor to seen at 4,600 RPM, 50% duly cycle is needed. The required duty cycle is computed as  $854\times0.5=127=7Fh$ .

Thus loading IFh into the cycle-high register.

\*  $11^{19}$  to sun motor at 6,900RPM, 75% duly cycle is needed. The nequired delty cycle is computed as  $254 \times 0.75 = 191 = BFh$ 

Thus loading Bfh into the cycle\_high riegister

\* The PWM does not provide enough current to seen the DC motor. Thus an NPN transistan is used to drive the DC motor as shown below.

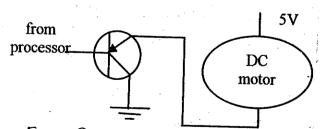


Fig 2 @: Connection to DC motor

The pseudo code is: void main (void) {

```
/* controls period */
PWMP = 0xff;
/* controls duty cycle */
PWM1 = 0x7f;
while(1){};
```