INTERRUPT ROUTINES IN RTOS EN VIRONMENT HANDELING OF INTERRUPT SOURCE CALLS

In a system the ISR should functions as following.

1.ISR have higher priorities over the OS functions and the applications tasks.an ISR does not wait for a semaphore mailbox message or queue message

2.An ISR does not also wait for mutex else it has to wait for other critical sections code to finish before the critical codes in the ISR can run. only the accept functon for these events can be used

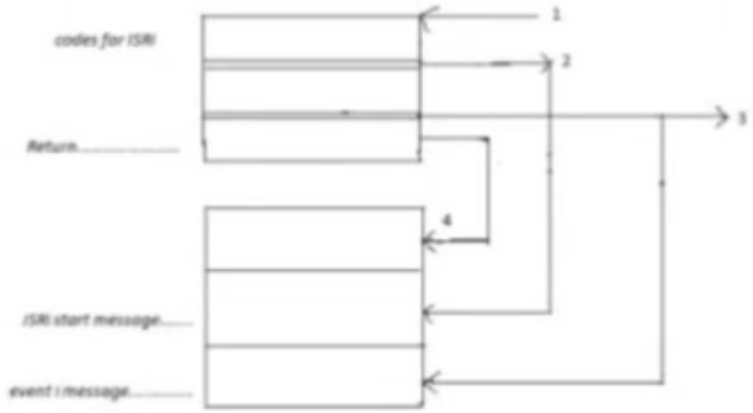
There are three alternative systems for the used to respond to the hardware source calls from the interrupts

- The following sections explain the OS is to respond to the hardware source calls from the interrupts
- 1.direct call to an ISR by an interrupting.
- 2.RTOS first interrupting on an interrupt then 0S calling the corresponding ISR.
- 3.RTOS first interrupting on an interrupt then RTOS initiating the ISR and then an ISR

2.RTOS FIRST INTERRUPTING ON AN INTERRUPT,THEN OS CALLING THE CORRESPOMDING

- On an interrupt of a task system k-th task the OS first gets the hardware source call(step1).
- And initiates the corresponding ISR after saving present process status (step2) .
- An i-th interrupt source causes the OS to get the notes of that after step1 it finish the critical code till the pre-emption point and calls the i-th ISR –I executs (step3).

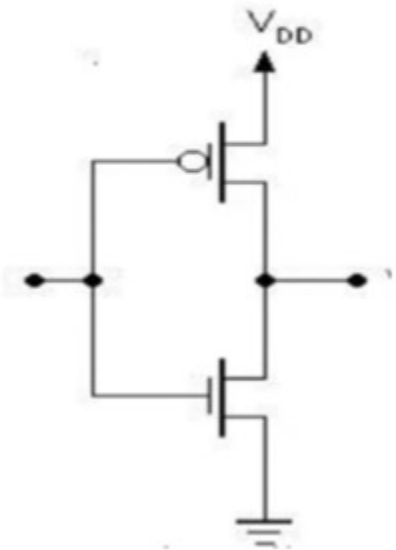
Direct call to an ISR by an interrupting



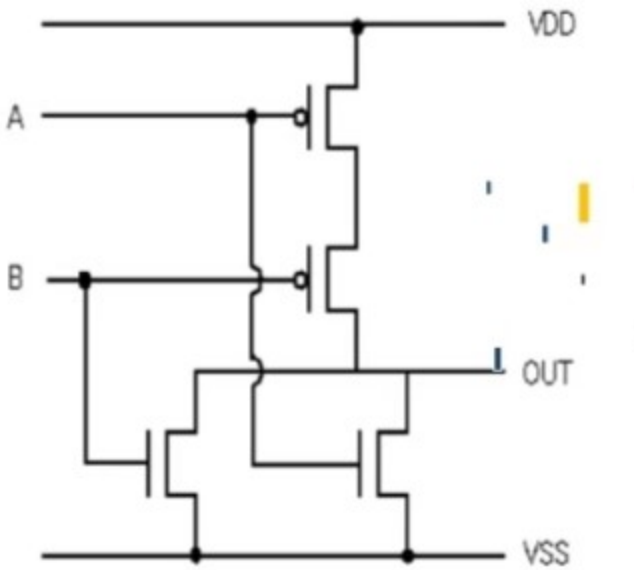
- No Diffusion can cross demarcation line.
- Only poly and metal can cross demarcation line
- N-diffusion and p-diffusion are joined using a metal wire.
- First step is to draw two parallel rails for VDD and GND.
- Next draw a demarcation line (brown)
- Place all PMOS above and NMOS below this line.
- Connect them using wires (metal).

Examples

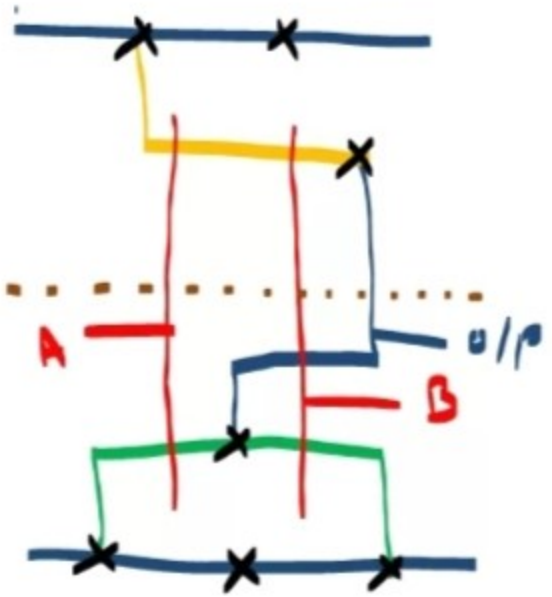
CMOS INVERTER



CMOS NOR



NOR gate in CMOS



λ Based Design Rules

- In MOS, the minimum feature size of Tr is:
  - (L/W)n = 1/1 = 2
  - λ/2 λ Active area = L*W = 4 λ2
- In CMOS, the minimum feature size of Tr is:
  - (L/W)n = 1/1.5 = 2 λ/3 λ
  - Active area = L*W = 6 λ2
- Minimum length or width of a feature on a layer is **2**λ
  - To allow for shape contraction
- Minimum separation of features on a layer is 2λ
  - To ensure adequate continuity of the intervening materials.

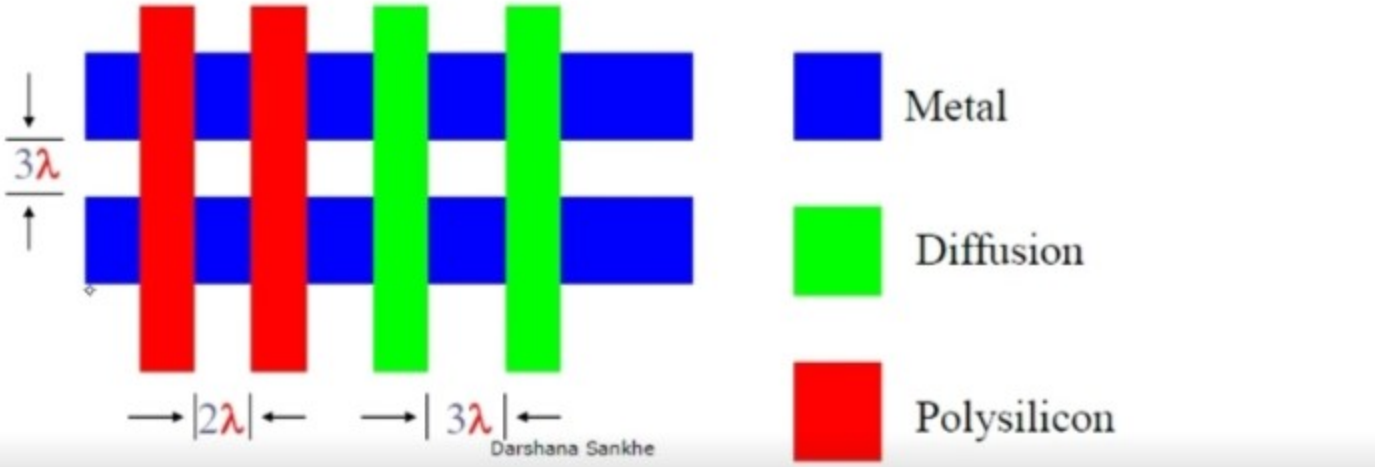
Design Rules

Two Features on different mask layers can be misaligned by a maximum of 2λ on the wafer.

- If the overlap of these two different mask layers can be catastrophic to the design, they must be separated by at least 2λ
- If the overlap is just undesirable, they must be separated by at least λ

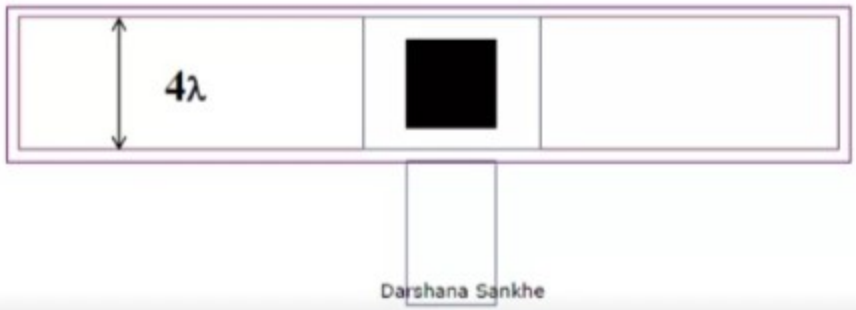
Design rules: NMOS

- PolySi – PolySi spacing 2λ
- Metal - Metal spacing 3λ
- Diffusion – Diffusion spacing 3λ : To avoid the possibility of their associated regions overlapping and conducting current



Contact cut

- Metal connects to polySi/diffusion by contact cut.
  Contact area: 2 λ *2 λ
- Metal and polySi or diffusion must overlap this contact area by λ so that the two desired conductors encompass the contact area despite any mis-align

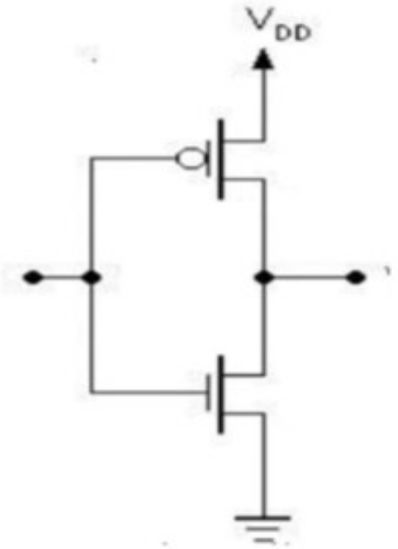


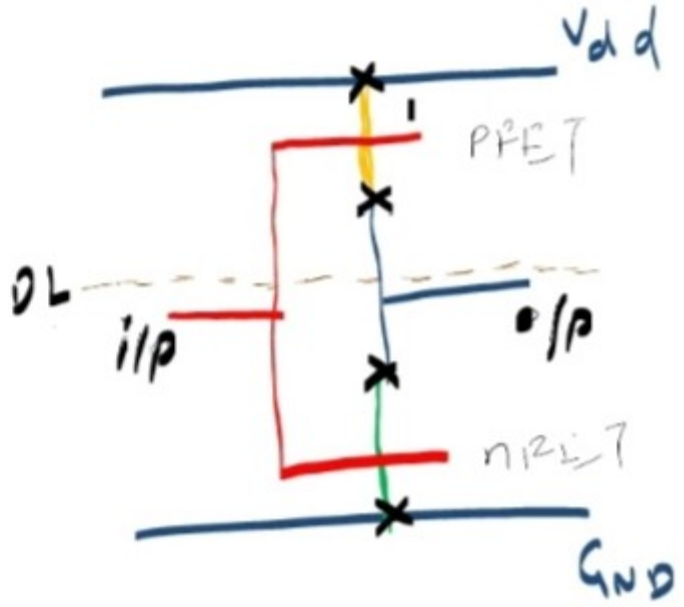
Design Rules to be followed:NMOS

- Minimum diff width 2 λ
- Minimum poly width 2 λ
- Minimum metal width 3 λ
- poly-poly spacing 2 λ
- diff-diff spacing 3 λ (depletion regions tend to spread outward)
- metal-metal spacing 3 λ
- diff-poly spacing λ
- Poly gate extend beyond diff by 2 λ
- Diff extend beyond poly by 2 λ
- Contact size 2 λ * 2 λ
- Contact diff/poly/metal overlap 1 λ
- Contact to contact spacing 2 λ
- Contact to poly/diff spacing 2 λ
- Buried contact to active device spacing 2 λ
- Buried contact overlap in diff direction 2 λ
- Buried contact overlap in poly direction 1 λ
- Implant gate over

Examples

CMOS INVERTER





CMOS NAND