MODULE- 2

ASIC Library Design: Logical effort: predicting delay, logical area and logical efficiency, logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design. (3.3 & 3.4)

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place, attributes, Netlist screener, Schematic-Entry tools Back annotation. (9.1)

by,

Dr.P.Vimala
Department of ECE
Dayananda Sagar College of Engineering
Bangalore

Figures from M.J.S .Smith, - "**Application - Specific Integrated Circuits**"

Logical Effort

- Explore a delay model- basis for time constant analysis
- All nonideal component of delay, t_q, includes

  (1)delay due to internal parasitic capacitance;

  (2)the time for the input to reach the switching threshold of the cell;

  (3)the dependence of the delay on the slew rate of the input waveform.
- With these assumptions we can express the delay as follows:

$$t_{PD} = R\,(C_{out} + C_p) + t_q$$

- Logic cell by a scaling factor, s
  - pull resistance R will decrease to R / s
  - parasitic capacitance Cp will increase to sCp
  - assume that tq scales linearly with s for all cells (stq)

Total cell delay $t_{PD} = (R/s)\cdot(C_{out} + sC_p) + st_q$

- Rewrite above Eq. using the input capacitance of the scaled logic cell $C_{in} = sC$,

$$t_{PD} = RC\frac{C_{out}}{C_{in}} + RC_p + st_q$$

- Finally we normalize the delay using the time constant formed from the pull resistance Rinv and the input capacitance Cinv of a minimum-size inverter:

$$d = \frac{(RC)(C_{out}/C_{in}) + RC_p + st_q}{t}$$ where, $t = R_{inv}C_{inv}$

- The delay equation is the sum of three terms with special names as follows: $d = f + p + q$

  delay = effort delay + parasitic delay + nonideal delay

  - Effort delay , f = gh

    where, g-logical effort (g = RC/ t) & h-electrical effort ($h = C_{out}/C_{in}$)
  - Parasitic delay, $p = RC_p/t$
  - Nonideal delay, $q = st_q/t$

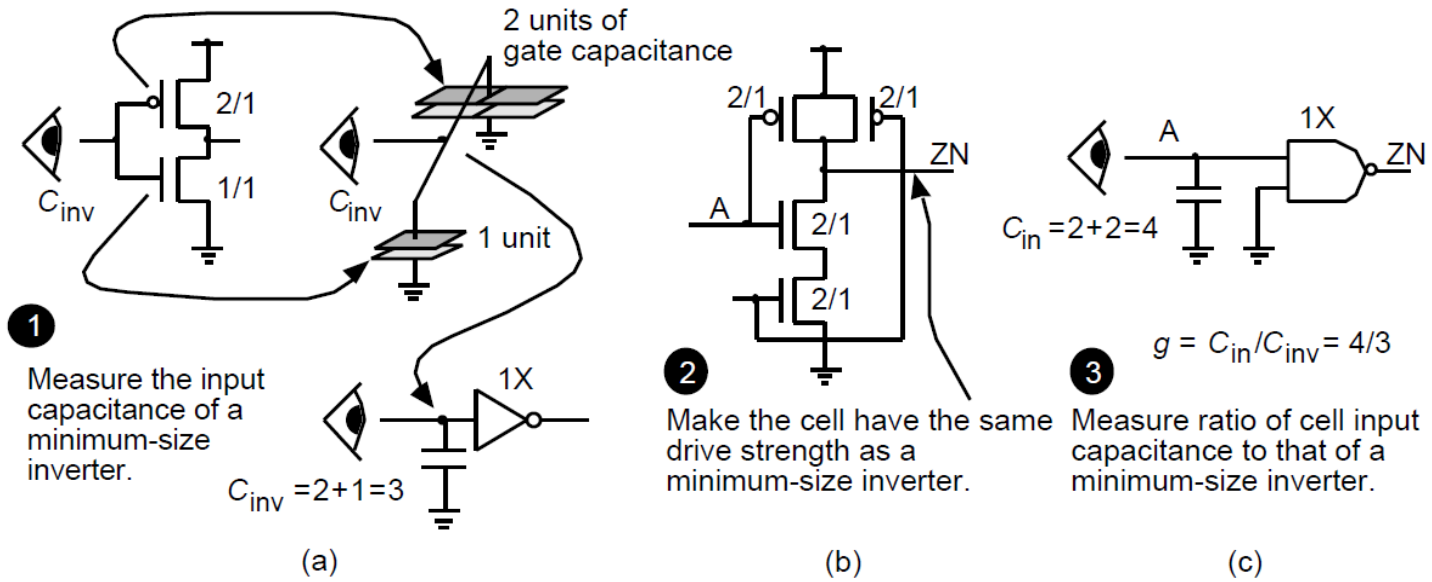
- delay = (logical effort X electrical effort)+ parasitic delay + nonideal delay

logical effort , g = RC/ t

- R and C will change as we scale a logic cell, but the RC product stays the same
- Logical effort is independent of the size of a logic cell
- We can find logical effort by scaling a logic cell to have the same drive as a 1X minimum-size inverter
- Then the logical effort, g, is the ratio of the input capacitance, Cin, of the 1X logic cell to Cinv.

The logical effort of a cell (g) = Cin/ Cinv

Cell	Cell effort (logic ratio = 2)	Cell effort (logic ratio = r)	Parasitic delay/ t	Nonideal delay/ t
inverter	1 (by definition)	1 (by definition)	p_{inv} (by definition) 1	q_{inv} (by definition) 1
n -input NAND	(n + 2)/3	(n + r)/(r + 1)	$n\,p_{inv}$	$n\,q_{inv}$
n -input NOR	(2 n + 1)/3	(nr + 1)/(r + 1)	$n\,p_{inv}$	$n\,q_{inv}$



- For a two-input NAND cell, the logical effort, g=4/3

(a) Find the input capacitance, Cinv, looking into the input of a minimum-size inverter in terms of the gate capacitance of a minimum-size device

(b) Size a logic cell to have the same drive strength as a minimum-size inverter (assuming a logic ratio of 2). The input capacitance looking into one of the logic-cell terminals is then Cin

(c) The logical effort of a cell is Cin/ Cinv

We can size a logic cell using these basic rules:

- Any string of transistors connected between a power supply and the output in a cell with 1X drive should have the same resistance as the n -channel transistor in a 1X inverter.
- A transistor with shape factor W 1 /L 1 has a resistance proportional to L 1 /W 1 (so the larger W 1 is, the smaller the resistance).
- Two transistors in parallel with shape factors W 1 /L 1 and W 2 /L 2 are equivalent to a single transistor (W 1 /L 1 + W 2 /L 2)/1. For example, a 2/1 in parallel with a 3/1 is a 5/1.
- Two transistors, with shape factors W 1 /L 2 and W 2 /L 2 , in series are equivalent to a single 1/(L 1 /W 1 + L 2 /W 2) transistor.

Predicting Delay

Example: Let us predict the delay of a three-input NOR logic cell with 2X drive, driving a net with a fan out of four, with a total load capacitance of 0.3 pF.

Where

For C5 technology, Cinv and is approximately 0.036 pF and qinv=1.7

We can calculate Cin from the fact that the input gate capacitance of a 1X drive, three-input NOR logic cell is equal to gCinv and for a 2X logic cell, Cin= 2 gCinv

The delay of the NOR logic cell, in units of t ,

= 12.266667 t

For C5 technology, t= 0.06ns $p = 3\,p_{inv}$ and $q = 3\,q_{inv}$

Absolute delay ,t_{pd} = 12.3 * 0.06 ns = 0.74 ns

$$gh = g\frac{C_{out}}{C_{in}} = \frac{g\cdot(0.3\text{ pF})}{2\,g\,C_{inv}} = \frac{(0.3\text{ pF})}{(2)\cdot(0.036\text{ pF})}$$

$$d = gh + p + q = \frac{0.3\ \mathbf{X}\ 10^{12}}{(2)\cdot(0.036\ \mathbf{X}\ 10^{12}\ )} + (3)\cdot(1) + (3)\cdot(1.7)$$

In the C5 library,

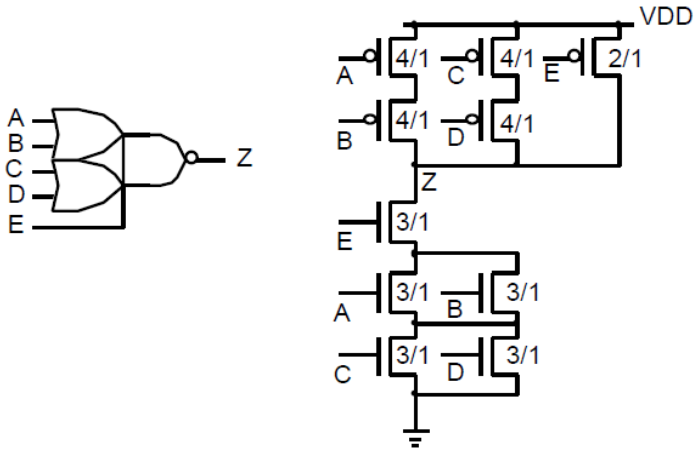
- The delay for a 2X drive, three-input NOR logic cell is t_{PD} = (0.03 + 0.72Cout + 0.60) ns
- With Cout=0.3pF, tPD = 0.03 + (0.72)·(0.3) + 0.60 = **0.846 ns** compared to our prediction of **0.74ns**

Error comes here due to,

- Inaccuracy in predicting the nonideal delay
- Logical effort gives us a method to examine relative delays and not accurately calculate absolute delays.
- More important is that logical effort gives us an insight into why logic has the delay.

Logical Area and Logical Efficiency

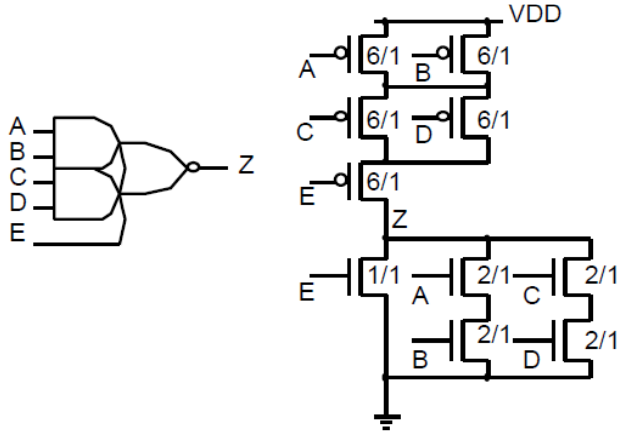
Example -1 (OAI221)



An **OAI221** logic cell

- Logical-effort vector g=(7/3, 7/3,5/3)
- The logical area is 33 logical squares

Example -2 (AOI221)



An **AOI221** logic cell

- g=(8/3, 8/3, 7/3)
- Logical area is 39 logical squares
- Less logically efficient than OAI221