AAT2 List

Subject: System Verilog for verification Semester: 7th

Faculty: Dr. Jamuna S Submission date: **10/1/2022**

All of you should design and verify the problem statement assigned to each one of you as in the table. Report should be submitted on or before the due date.(using Verilog/System Verilog)

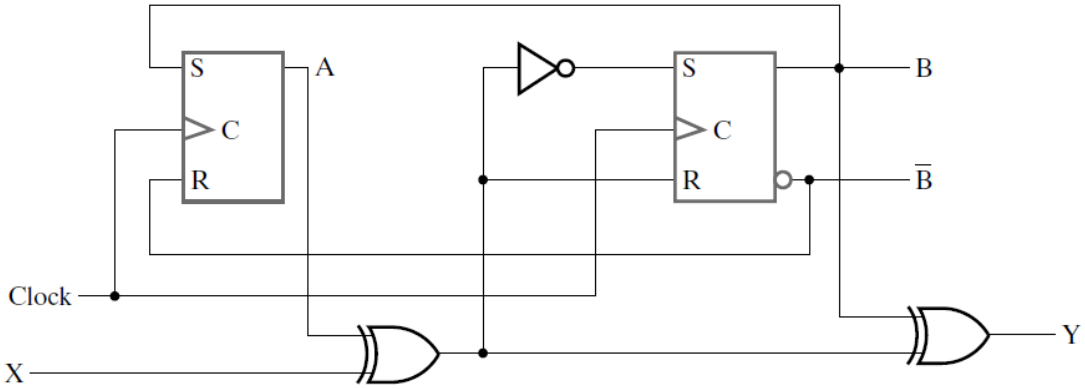
1) Design and verify D Flip flop with synchronous reset and asynchronous reset.
2) Sequence Detector using Mealy machine (1101,Non-Overlapping).
3) Sequence Detector using Moore machine (1101,Non-Overlapping).
4) Sequence Detector using Mealy machine (1101, Overlapping).
5) Sequence Detector using Moore machine (1101,Overlapping).
6) Count the no.of 1's in given input sequence (16-bit input).
7) Binary to gray conversion. It should work for n number of inputs. The number of inputs should be mentioned from test bench.
8) Three-bit up/down counter. It should include a control input called Up/Down. If Up/Down = 0, then the circuit should behave as an up-counter. If Up/Down = 1, then the circuit should behave as a down-counter.
9) Design a 4-bit counter with asynchronous reset, synchronous load and enable inputs. On reset the counter is set to 1000 and counts sequence in the order specified below (top to bottom and loop back). Counter can be loaded with any value present in the sequence. Counter should go back to reset state if loaded with some invalid count. Enable pin can be used to halt the counter if set to 0.

1000
0111
1011
0100
1001
0010
0101
1100
0110
0011
1111
0001
1110
1101

10) Clock divider with input frequency of 400MHz and output of 100MHz.
11) Design a 16-bit parallel in parallel out universal right shift register which performs following operations.
    a. Load, Shift enable
    b. Logical Left shift
    c. Logical Right shift
    d. Arithmetic Left shift

e. Arithmetic Right shift

12) N bit universal shift register.
13) 4-bit Linear Feedback Shift Register(LFSR).
14) Write a Verilog/system Verilog description for the following circuit.
15) Single prort RAM (128x8). Perform Read and write operations.
16) Dual port RAM (128*8). Perform Read and write operations.
17) Synchronous FIFO (8x8). Test bench should use task for read and write operations.
18) Asynchronous FIFO (8x8) Test bench should use task for read and write operations.
19) Write a Verilog/system Verilog description for the following circuit.



20) Design an 8x8 sequential multiplier. The multiplier has asynchronous reset, synchronous load and output valid signal.
21) 64-bit Pipelined Multiplier (latency should be 6 cycles).
22) Design and verify a 4 bit Gray counter ,successive values should differ only in one bit.Reset signal resets the counter to zero using FSM design concept.
23) Bus arbiter design
24) Design a SPI
25) UART block
26) I2C bus

Sl no	USN	Name	Design number to be done
1	1DS16EC708	ANKITH S	3
2	1DS17EC703	AKHIL H A	3
3	1DS18EC003	ADITHYA U	9
4	1DS18EC004	AKSHAY K J	11
5	1DS18EC008	AMRUTHA N HOLLA	15
6	1DS18EC009	ANANYA RAJ	7
7	1DS18EC010	ANIKETH B G	8
8	1DS18EC013	ARPITHA N	15
9	1DS18EC014	ASAAD UR RAHEMAN DODAMANI	11
10	1DS18EC016	BANDI RAGHAVENDRA	
11	1DS18EC018	BASAVARAJ R MUDDI	16
12	1DS18EC023	DARSHAN A M	16
13	1DS18EC035	HARSHITH K	
14	1DS18EC043	M SIDDARTH	17
15	1DS18EC055	NAGARAJ V	17
16	1DS18EC070	PUNEETHA RAMYA	22
17	1DS18EC079	SAMRUDH M	
18	1DS18EC091	SUDHAMSHU B N	23
19	1DS18EC114	BHOOMIREDDY VENKATA SRAVANTHI REDDY	22
20	1DS18EC123	KAKARLA SUBBA REDDY	20
21	1DS18EC127	MADIREDDY SAI VISHAL REDDY	20
22	1DS18EC149	SOMIL KUMAR	23
23	1DS18EC150	SRINIVASAREDDY MAHAREDDY	9
24	1DS18EC159	SAHANA S M	19
25	1DS18EC409	DARSHAN AMARESH ANGADI	12
26	1DS18EC430	P MANASA	11
27	1DS18EC431	P N BELLIAPPA	20
27	1DS18EC448	SONALI YADAV	20
28	1DS18EC451	THIRUMALESHA.S	22
30	1DS18EC458	DEEPAK J M	1
31	1DS18EC462	PRAJWAL B	4
32	1DS18EC465	UMAR FAROOQ.K	5
33	1DS18EC465	RAHUL DATTAWADE	6
34	1DS18EC710	MOUNASHREE P	13
35	1DS18EC717	RAM RATHAN K R	18
36	1DS18EC719	RAVI L BELLUBBI	19
37	1DS18EC720	RISHIRA S M	25
38	1DS18EC721	SANJAY SAMPATH	26
39	1DS18EC728	SRAJANA CHANDRASHEKHAR	26
40	1DS18EC732	AKANSHA MUKESH SHARMA	25
41	1DS18EC733	D CHIRAG CHINVAR	26
42	1DS18EC748	SAHIR SHRIVASTAVA	12
43	1DS18EC749	SAI NIKHIL KANDAGIRI	24
44	1DS19EC409	DUNDAPPA SUKALI	24

45	1DS19EC432	SHOBHA S AIRADDI	6
46	1DS19EC435	SURAJ KULKARNI	6
47	1DS19EC442	VIJAY V BENAL	2
48	1DS19EC445	POORNESH HAVLAKAR	2