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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078

UG Semester End Examination, February/March 2022

Course: **SYSTEM VERILOG FOR VERIFICATION** Maximum marks: **100**
Course Code: **18EC7DEESV** Duration: **03 hours**
Semester: **VII**

Note: i). Question ONE (a to t) has to be answered from pages 5 to 7 only, also candidate must write the answer along with the option.
ii). Question 1 to 4 is compulsory.
iii). Any missing data should be suitably assumed

Q. No.		Marks
1a)	Simulators are static type of tools, i) true ii) false iii) neither i) nor ii) iv) can't say	01
b)	Human introduced errors can be minimized by i) Automation ii)Poka-Yoka iii) Redundancy iv) all	01
c)	Which of the following is correct? i) Design and Test bench are synthesizable ii) Design is synthesizable but not test bench iii) Only test bench is synthesizable iv) None	01
d)	Which type of mistake is not recommended? i) Type1- false negative ii) Type2-false positive iii) both i) and ii) iv) None	01
e)	In System Verilog, class can be defined inside, i) Program ii) Module iii) Package iv) all	01
f)	100% code coverage indicates that the design is perfect, i) True, ii) False iii) Can't say iv) Sometimes true	01
g)	$unknown returns _____ if any bit of the expression is x or z i) 1 ii) 0 iii) x iv) z	01
h)	For int f[6] = '{ 1,6,2,6,8,6}, tq = f unique() gives _____ i){1,6,2,6} ii) {6,2,6,8} iii) {1,6,2,8} iv) {2,6,8,6}	01
i)	A single System Verilog "interface" can have multiple mod ports and multiple clocking blocks inside i)True ii) False iii) only mod port and two clocking blocks iv)None	01
j)	Default port direction in a task is _____ i)Input ii) Output iii) In-out iv) reference	01
k)	Void function in System Verilog returns _____ value i) Single ii) Multiple iii) None iv) High Impedance	01
l)	Clocking block default delay is i)input #1step output #0 ii) input #0step output #1 iii) input #0step output #0 iv)none	01
m)	In System Verilog, test bench is _____ i) more robust ii) easy to maintain iii)re-usable iv) all	01
n)	BusTran has two 32-bit registers (addr and crc) and an array with 8, 32 bit entries.How much space would new allocate for an object of BusTran? i)320 bits ii) 100 bits iii) 32 bits iv)64bits	01
o)	Handle in System Verilog is like a, i) pointer to an object ii) address of the object iii) both i) and ii) iv) None	01
p)	Benefits of a program block are , i)Separates the testbench from the DUT ii)Reduces race conditions by running in separate region iii)Provides an entry point for execution iv)all	01
q)	Implecation Operators are are, i) - > ii) = = iii) < - iv) !=	01
r)	The $urandom_range takes _____ arguments, i) One ii) Two iii) Three iv) Zero	01
s)	**randc** is stands for i) random-cyclic. Ii) random circular iii)random code iv)none	01
t)	Constraints blocks are class members like , i)tasks ii) functions iii) variables iv) all	01
2 a)	What is formal verification? Explain the various techniques used for performing the formal verification.	08
b)	How do you classify the code coverage verification tools? Explain any three coverage types with suitable examples.	08

3	a)	Explain the verification process with respect to different design levels of the present day technology.	08
	b)	Mention the array methods supported in system verilog. Explain array reduction method in detail.	08
4	a)	Summarize the advantages of using interface in connecting DUT and testbench.	04
	b)	Briefly discuss about Tasks, Functions and Void Functions in System Verilog.	08
	c)	Write a System Verilog code using break and continue while reading a file.	04
5	a)	Elaborate on the features of Object oriented programming (OOP) available in system Verilog.	08
	b)	Discuss how a routine can be defined outside the class with a suitable example.	08
		OR	
6	a)	Discuss in detail the concept of copying objects in System Verilog.	10
	b)	With the help of a neat diagram, explain the concept of building a layered test bench in System Verilog.	06
7	a)	Elaborate on constraint gaurds with suitable example code.	08
	b)	Develop a random array of unique values in System Verilog.	08
		OR	
8	a)	Write a explanatory note on constraint details in System Verilog.	06
	b)	What are the issues encountered when creating a random stimulus.	04
		How is randomization done in system Verilog? Explain with an example code.	06