# Question Bank

# ASIC Design

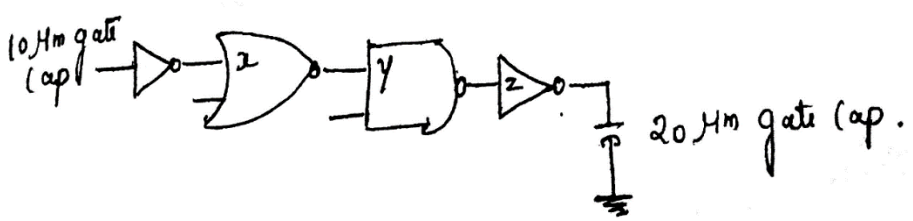
All Questions carries 10M. Exceptional are mentioned near the question

## ***MODULE- 1***

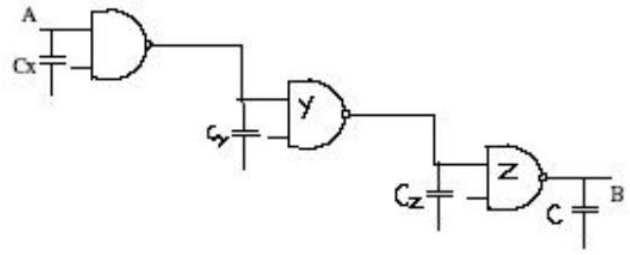
1. Brief introduction to ASICs. Give the classification of ASIC? (12M)
2. Detail explanation about the classification of ASIC (12M)
3. Explain about different types of gate-array–based ASICs
4. Short notes on
    a) Full Custom ASIC.
    b) Programmable ASIC
5. Write about the steps involved in designing an ASIC with suitable diagram?
6. Brief explanation about ASIC cell libraries.
7. Detail explanation about Data path Logic Cells using ripple-carry adder
8. List all symbols and elements for an adder.
9. Explain the functional and limitation of conventional ripple-carry adder?
10. Explain in detail about Carry Select Adder.
11. Detail explanation about Look ahead Carry Adder.
12. Give the detail explanation for symmetric 6-bit array multiplier.
13. Explain briefly about Wallace-tree multiplier.
14. Explain about DADDA multiplier?
15. With neat diagram explain about Array multiplier?
16. Give the details about I/O cell and Cell Compilers.

# ***MODULE-2***

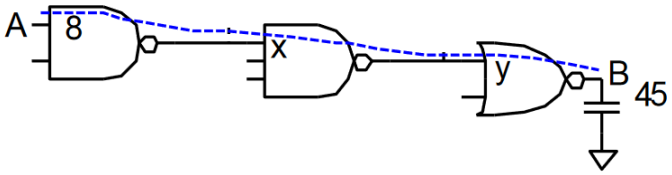
1. Derive delay model based on Logical effort.
2. Design a CMOS circuit for $\overline{AB + (C + D)E}$. Also calculate the Logical effort vector and logical area for the design.
3. Define logical effort. Calculate optimal stage effort and size of transistors for circuit shown in Figure.




4. Consider the path from A to B involving three two input NAND gates as in figure. The input capacitance of first gate is C and the load capacitance is also C . Find the least delay in this path and how should the transistors be sized to achieve least delay?




5. Find the gate sizes x and y and least delay from A to B




6. Short notes on:
    a) Predicting delay
    b) Logical area and logical efficiency
7. Explain in detail about logical paths and multi stage cells
8. Write short notes about optimum delay and optimum no. of stages
9. Give an introduction about ASIC Schematic Entry and write about Hierarchical design.
10. Give explanation about the cell library of ASIC Schematic Entry
11. With neat diagram explain about Schematic Icons and Symbols with examples.
12. Explain schematic Names and Nets with examples
13. Write about the following terms

a) Schematic entry for ASIC'S
b) Connections

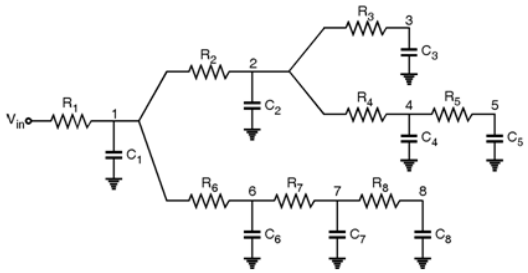
14. Detail explanation about
    a) Vectored instances and buses
    b) Edit in place
15. Give the details about Attributes and Netlist screener of Schematic Entry.
16. Describe the netlist screener program of a schematic entry tool to detect simple errors.
17. Explain in detail about Schematic-Entry tools and Back annotation

## ***MODULE-3***

1. Brief explanation about the types of Programmable ASICs
2. How many types are there in Antifuse? Explain in detail.
3. Short notes on
    a) Static RAM
    b) EPROM and EEPROM Technology
4. Discuss the Practical Issues of Programmable ASICs.
5. Explain in detail about the history of FPGA manufactures.
6. Explain the ACT1 logic module with neat diagram. Derive Shannon's theorem with a Boolean logic function.
7. Explain the multiplier mapping using ACT1 logic.
8. Briefly explain the ACT2 and ACT 3 logic modules with neat diagram.
9. Explain the Xilinx 3000 CLB architecture
10. Explain the functional logic of Xilinx 4000 family IOB along with necessary diagram.
11. Detail explanation about Altera FLEX and Altera MAX with neat diagram.
12. What is input/output cell? List the different types of I/O cells that are used in programmable ASICs and their functions.
13. Detail explanation about DC output of programmable ASICs.
14. What is AC output? Explain in detail.
15. With neat diagram explain about DC input of ASICs
16. Give brief explanation about ASCIs AC input.
17. Write about the Clock input of programmable ASICs
18. Briefly explain about the Power input of programmable ASICs
19. Explain in detail about Xilinx I/O Block

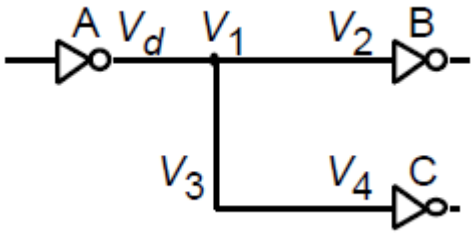
# MODULE-4

1. Explain the interconnect architecture used in Actel Act with routing resources.
2. Write the expression for Elmore's constant. Also write the Elmore delay at node 3,4 &7 in the following RC network.




RC tree network

3. Draw the RC model for the given circuit. Also write the Elmore delay at node 2,3 &4 for the RC network. Write the expression for Elmore's constant.




4. Define Synthesis. With neat flow chart explain the steps involved in synthesis process.
5. Short notes on
   a) RC delay in antifuse connections
   b) Antifuse parasitic capacitance
6. Give detail explanation about Verilog and logic synthesis.
7. Write a Verilog behavioural code for a 2X1 multiplexer. Show the gate level synthesis of the code.
8. Write Verilog code for signal assignment statement Y=2*X+3 for 2 bit input. Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram.
9. Explain the mapping of else if statement by taking the following example.
   The system with BP (input) and ADH (output) are of natural type ranging 0 to 7 and 0 to 15 respectively. Assume that if BP less than or equal to 2, then ADH=15 or if BP greater than 5 then ADH is 0 otherwise ADH = BP *(-5) +25.
10. Draw the gate level synthesis information extracted from the following Verilog code

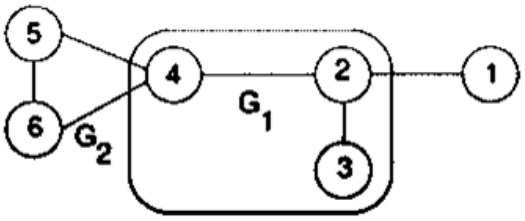
```
always @ (a, X, X1)
begin
if (a == 1'b1)
Y = X;
```

```
else
Y = X1;
end
```

11. Find the gate level synthesis mapping for a 3bit input ‘a’ and single bit output ‘y’ has the condition as output is high when the input value is less than 5 otherwise low.
12. Write Verilog description for 3:8 decoder using case statement and show the synthesized logic symbol and gate level diagram.
13. Write Verilog description for 8:3 encoder using case statement and show the synthesized logic symbol and gate level diagram.
14. Draw the gate level synthesis information extracted from 8:1 Multiplexer. Also write the Verilog code using case statement.
15. Draw the gate level synthesis information extracted from 1:8 DeMux. Also write the Verilog code using case statement.
16. Write Verilog code for y=2*a+5 for 3-bit input. If a is greater than four, y retains its previous value. Also, show the synthesized gate level diagram and logic symbol for the given example.
17. What are the different modes of simulation are available? Explain.

## ***MODULE-5***

1. Explain the physical design steps for an ASIC with neat diagram.
2. Explain in detail about the sources of power dissipation in CMOS logic.
3. How to measure connectivity using help from the mathematics of graph theory?
4. Explain in detail about a simple partitioning with an example.
5. Short notes on
    a) Constructive Partitioning
    b) Iterative Partitioning
6. Explain KL algorithm for system partitioning?
7. Implement the KL algorithm for given network. (12M)

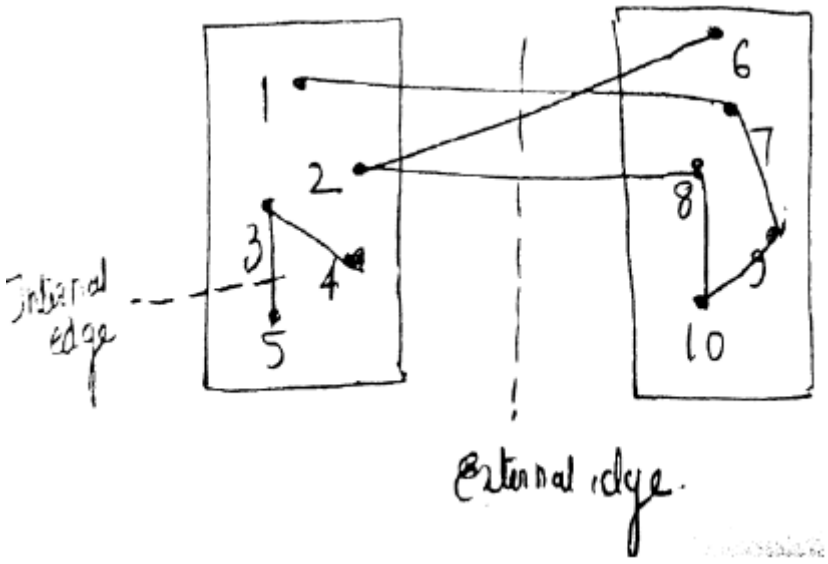



8. Implement the KL algorithm for the given connectivity matrix. Consider a,b,c are in 1st group and d,e,f are in 2nd group. (12M)

| | a | b | c | d | e | f |
|---|---|---|---|---|---|---|
| a | 0 | 1 | 2 | 3 | 2 | 4 |
| b | 1 | 0 | 1 | 4 | 2 | 1 |
| c | 2 | 1 | 0 | 3 | 2 | 1 |
| d | 3 | 4 | 3 | 0 | 4 | 3 |
| e | 2 | 2 | 2 | 4 | 0 | 2 |
| f | 4 | 1 | 1 | 3 | 2 | 0 |

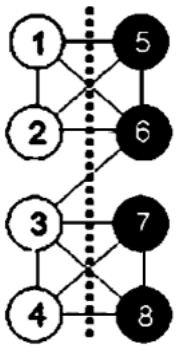
9. With equivalent equations, explain the KL algorithm. Construct the connectivity matrix for the network graph shown in figure. Also, find the gain and cutset in the network, if:

(i) Nodes 1 and 6 are swapped
(ii) Nodes 2 and 8 are swapped




10. Construct the connectivity matrix for the network graph shown in figure. Also, find the gain and cutset in the network, for the following:

(i) swap (3,5)
(ii) swap (4,6)




11. Discuss about Ratio-cut algorithm and the look-ahead algorithm.
12. What is floor planning? Discuss about the Goals and objectives of floor planning. (6M)

13. How the interconnect delays can measure in floor planning? Explain with an example.
14. Discuss about the tools used for floor planning a cell-based ASIC.
15. What is channel definition? Explain with an example.
16. Discuss about I/O and Power planning.
17. Explain in detail about clock planning.
18. What is placement? List the placement goals and objectives. (4M)
19. Detail explanation about Iterative placement improvements. (12M)
20. Illustrate the Force-directed placement and different kinds of force-directed placement algorithms.
21. Give the detail explanation for floorplanning and placement design flow with necessary diagram.
22. What is global routing? Explain in detail about the goals and objectives of global routing? (6M)
23. Explain in detail about the Detailed Routing with necessary diagrams.
24. Discuss about special routings apart from global and detailed routing.
25. Explain about circuit extraction and DRC?