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DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi)

Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560078

UG Semester End Examination, February/March 2022

Course: **ASIC DESIGN** Maximum marks: **100**

Course Code: **18EC7DEDAD** Duration: **03 hours**

Semester: **VII**

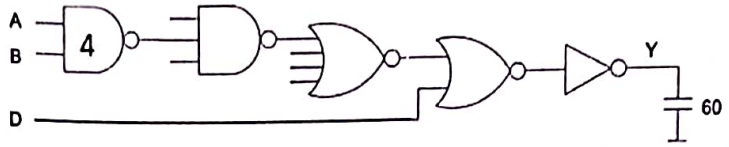
Note: **i). Question ONE (a to t) has to be answered from pages 5 to 7 only, also candidate must write the answer along with the option.**
ii). Question 1 to 4 is compulsory.
iii). Any missing data should be suitably assumed

Q. No.		Marks
1a)	AC output functionality requires the capability for_____outputs (i) two- state (ii) three-state (iii) four- state (iv) None	01
b)	The predefined pattern of a gate-array-based ASIC is called _____ (i) base array (ii) Primitive cell (iii)Mask (iv) base	01
c)	Number of CSA & CPA required for 6-bit Dadda multiplier is ___ respectively (i) 20 & 10 (ii) 10 &20 (iii) 26 & 4 (iv) 4 & 26	01
d)	For a 16-bit binary adder, how much delay required for a carry to propagate from input to output? (i) 16unit (ii) 3unit (iii) 15unit (iv) 32	01
e)	Path electrical effort is the_____of the electrical efforts on the path. (i) half (ii) Sum (iii) double (iv) product	01
f)	Which of the following is not used to represent the terminals of the input/output cells? (i) pins (ii)connectors (iii)signals (iv) nets	01
g)	Logical effort gives us a method to examine (i) relative delays (ii) accurate delays (iii) absolute delays (iv) both a & b	01
h)	An antifuse element initial provides_____between two conductors in absence of theapplication of sufficient programming voltage. Conduction ii)Insulation iii) Conduction and Insulation iv)None	01
i)	Which one is the following is not true for static RAM? (i) Use in reconfigurable hardware (ii) Use of PROM to hold the configuration (iii) Cannot be reused (iv) volatile memory	01
j)	ACTELs Antifuse is called as _____(i) PLICE (ii) PILCE (iii) PILEC (iv) PLIEC	01
k)	An Antifuse programming technology is predominantly associated with___ (i) PLDs (ii) FPGAs (iii) CPLDs (iv) none	01
l)	Altera FPGAs use_____programming technology. (i) EPROM (ii) Antifuse (iii)DRAM (iv) SRAM	01
m)	Compared to FPGA, ASIC consumes_____power and____. (i) low,faster (ii) high,faster (iii) high, slower (iv) None	01
n)	The number of interconnects handle by interconnect channel is called _____ (i)ratio of channel density (ii)interconnect chip (iii)routability display (iv)channel capacity	01
o)	Initial Prelayout simulations include logic-cell delays but no_____. (i)Physical Design (ii) logic synthesizer (iii) interconnect delays (iv)Components	01
p)	Xilinx based FPGA device are (i) EPROM (ii) Antifuse (iii)DRAM (iv) SRAM	01
q)	_____extend vertically into routing channels above and below logic module (i) Input stubs (ii) Output stubs (ii) vertical tracks (iv) horizontal tracks	01
r)	_____defines the location of the logic cells. (i) Partitioning (ii) Floorplanning (iii) Placement (iv) Routing	01
s)	In floorplanning, which phase/s play/s a crucial role in minimizing the ASIC areaand the interconnection density? (i) Placement (ii) Global routing (iii) Detailed routing (iv) None	01

t) Which of the following design steps needs more logic design details? 01
(i) Design entry (ii) Logic synthesis (iii) System partitioning (iv) Prelayout simulation

2 a) Explain about different types of gate-array-based ASICs 06
b) Explain the function and limitation of conventional ripple-carry adder. 06
c) With neat diagram explain about Array multiplier. 04

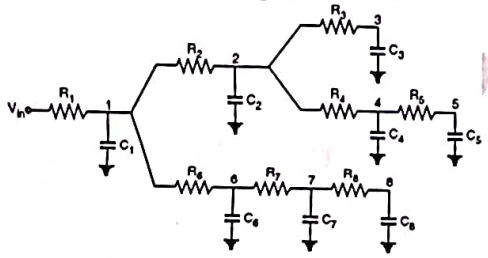
3 a) Compute the optimum delay for the path A to Y in Fig.1. Also find the gate sizes for cells available between A to Y. 10



b) Explain in detail about Back annotation. 06

4 a) Describe ACTEL, ACT- 1 logic module to implement the Boolean function using Shannon's expansion theorem. F= AB+B'C+D. 06
b) How many types are there in Antifuse? Explain in detail. 06
c) List the different types of I/O cells that are used in programmable ASICs and their functions. 04

5 a) Write the expression for Elmore's constant. Also write the Elmore delay at node 3,4 &7 in the following RC network. 06



RC tree network

b) Write a Verilog behavioural code for a 2X1 multiplexer. Show the gate level synthesis of the code. 05
c) Write a note on Antifuse parasitic capacitance. 05

OR

6 a) What are the different modes of simulation available? Explain. 08
b) Draw the gate level synthesis information extracted from 8:1 Multiplexer. Also write the Verilog code using case statement. 08

7 a) Explain in detail about the sources of power dissipation in CMOS logic. 06
b) Explain in detail about a simple partitioning with an example. 10

OR

8 a) Explain KL algorithm for system partitioning? 08
b) What is floor planning? Discuss about the Goals and objectives of floor planning. 04
c) What is placement? List the placement goals and objectives. 04