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A
Mini Project Work (18EC6ICMPR) Report
on

LDPC DECODING FOR FPGA IMPLEMENTATION

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering
in
Electronics & Communication Engineering
by

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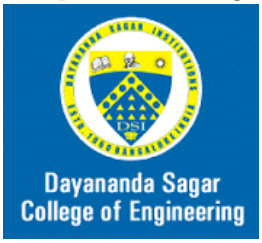

Department of Electronics & Communication Engineering
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Certificate

Certified that the Mini project work entitled "LDPC Decoding for FPGA Implementation" carried out by Sudhamshu.B.N(1DS18EC091), Sumanth.B.P(1DS18EC093), Ramesh.C.S(1DS18EC075), Suprith.N(1DS18EC094) is bonafide students of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2020-21. It is certified that all corrections / suggestions indicated for Mini project work have been incorporated in the report deposited to the ECE department, the college central library & to the university. This Mini project report **(18EC6ICMPR)** has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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External Project Viva-Voce

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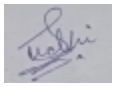
Declaration

Certified that the Mini project work entitled, "LDPC Decoding for FPGA Implementation" is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2020-21. We, the students of the Mini project group/batch no. B-1 hereby declare that the entire Mini project work has been done on our own & we have not copied or duplicated any other's work. The results embedded in this Mini project work report have not been submitted elsewhere for the award of any type of degree.

Student Name1 : Sudhamshu B N USN : 1DS18EC091 

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Abstract

In information theory, a Low-Density Parity-Check (LDPC) code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel. An LDPC is constructed using a sparse Tanner graph (subclass of the bipartite graph). LDPC codes are capacity-approaching codes, which means that practical constructions exist that allow the noise threshold to be set very close to the theoretical maximum (the Shannon limit) for a symmetric memoryless channel.

The noise threshold defines an upper bound for the channel noise, up to which the probability of lost information can be made as small as desired.Using iterative belief propagation techniques, LDPC codes can be decoded in time linear to their block length. LDPC codes are finding increasing use in applications requiring reliable and highly efficient information transfer over bandwidth-constrained or return-channel-constrained links in the presence of corrupting noise. Low density parity check (LDPC) codes are linear block codes used for error detection and correction mostly in high speed digital communication systems like digital broadcasting, optical fibre communications and wireless local area networks. LDPC codes have been subject to extensive research because of their significant performance in error correction.

LDPC Code is a type of Block Error Correction code discovered and performance very close to Shanon's limit .Good error correcting performance enables reliable communication. Since its discovery by Gallagar there is more research going on for its efficient construction and implementation. Though there is no unique method for constructing LDPC codes. Implementation of LDPC Code is done by taking different factors into consideration such as error rate, parallelism of decoder, ease in implementation etc.

This mini-project work undertaken by us involves the simulation of LDPC decoding ModelSim, Writing Verilog code for the hardware implementation of LDPC decoding. Testing and verification of the results in suitable hardware.

In this mini-project we as a team are exploring different fields of electronics using a single mini-project which has simulation, hardware and software parts.

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CHAPTER 1 INTRODUCTION

Looking back over the last six decades or so, one can reasonably surmise that the family of low-density parity-check codes (LDPC) and that of turbo codes constitute the two most practical realizations of Shannon's theory, which has revolutionized the field of error correction coding.

Shannon demonstrated that it is possible to transmit information arbitrarily reliably over any unreliable channel, provided that the information transmission rate is lower than the capacity of the channel. Therefore, the channel capacity sets the bound on how much information we can transmit over a channel. Shannon's claim can be realized by a technique referred to as forward error correction. The basic idea is that of incorporating redundant bits, or check bits, thus creating what is known as a codeword. If the check bits are introduced in an "appropriate manner" so as to make each codeword sufficiently distinct from each other, the receiver will then become capable of determining the most likely codeword that has been transmitted. The channel capacity will determine the exact amount of redundancy that has to be incorporated by the encoder in order to be able to correct the errors imposed by the channel. However, Shannon's theory only quantifies the maximum attainable rate, but refrains from specifying the means of achieving it. This triggered widespread research efforts resulting in diverse extensions, deeper interpretations and practical realizations of Shannon's original work, which reached its pinnacle in the definition of LDPC and turbo codes.

Today LDPC are used for 10 GBASET Ethernet, which sends 10 gigabits per second over twisted pair cables, LDPC are a part of WiFi 802.11, 802.11n and 802.11ac in High Throughput (HT) PHY specification in 5G.

LDPC codes, with iterative decoding, have been shown to achieve excellent performance over many channels, nearly approaching capacity on additive white Gaussian noise (AWGN) channel, and as code's length tends to infinity, achieving it on the binary erasure channel (BEC). In this project as a continuation of the CRC project from the 5th sem, we are trying to implement LDPC decoding using Min-Sum Algorithm.

CHAPTER 2: LITERATURE SURVEY

This survey is on Advancements that happened in the field of LDPC codes and its rateless relatives and its history. We also do a survey on different techniques used for LDPC Encoding and Decoding in the present scenario.

2.1 Near Shannon Limit Performance of Low Density Parity Check Code by David J.C. MacKay Cavendish Laboratory, Cambridge

This paper rediscovered LDPC codes that were invented by Gallager 30 years ago. This paper is cited in most of the LDPC code papers. It's short but a good read for a start.

It gives the empirical performance of Gallager's low density parity check codes on Gaussian channels. We show that performance substantially better than that of standard convolutional and concatenated codes can be achieved; indeed the performance is almost as close to the Shannon limit as that of Turbo codes.

2.2 Gallager Codes – Recent Results David J. C. MacKay

This paper reviews low–density parity–check codes (Gallager codes), repeat-accumulate codes, and turbo codes, emphasising recent advances. Some previously unpublished results are then presented, describing

a) Experiments on Gallager codes with small block lengths

b) A stopping rule for decoding of repeat-accumulate codes, which saves computer time and allows block decoding errors to be detected and flagged

c) The empirical power-laws obeyed by decoding times of sparse graph codes.

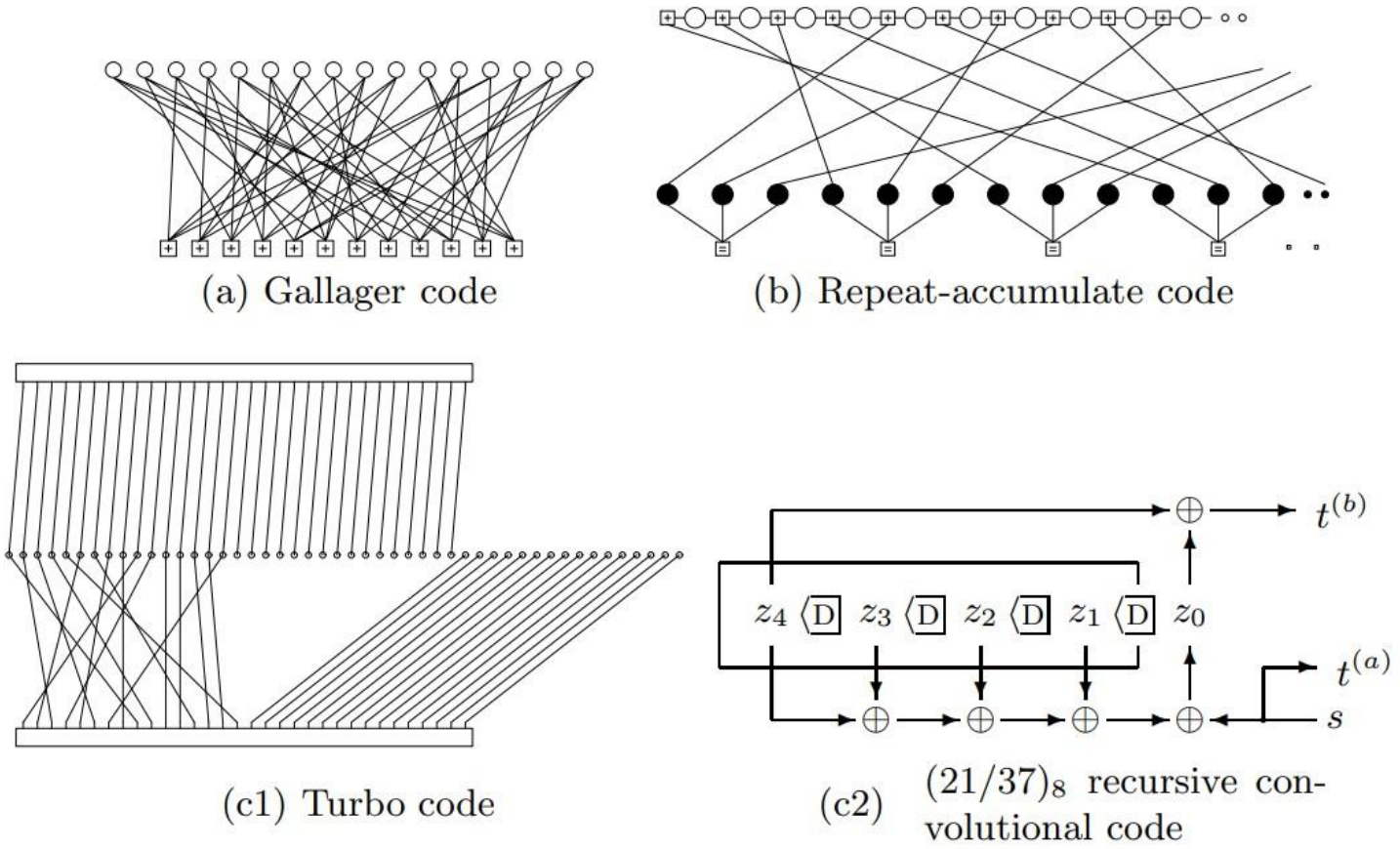


fig1.

2.3 Parallel Decoding Architectures for Low Density Parity Check Codes, C.Howland and A. Blanksby

A parallel architecture for decoding Low Density Parity Check (LDPC) Codes is proposed that achieves high coding gain together with extremely low power dissipation, and high throughput. The feasibility of this architecture is demonstrated through the design and implementation of a 1024 bit. rate-1/2, soft decision parallel LDPC decoder.

A parallel architecture has been proposed for decoding Low Density Parity Check (LDPC) codes that achieves extremely low power dissipation and high throughput when compared to turbo and block turbo code decoders.

The feasible design space for parallel LDPC codecs spans a wider range of code rates and throughputs than turbo and block turbo codes. Possible applications of parallel LDPC codecs include disk drive read channels. wireless and satellite communications.

2.4 Reduced-Complexity Decoding of Q-ary LDPC Codes for Magnetic Recording,Hongxin Song, Member, IEEE, and J. R. Cruz, Fellow, IEEE

This paper researched that Binary low-density parity-check (LDPC) codes perform very well on magnetic recording channels (MRCs) with additive white Gaussian noise (AWGN). However, an MRC is subject to other impairments, such as media defects and thermal asperities. Binary LDPC codes may not be able to cope with these impairments without the help of a Reed–Solomon code. A better form of coding may be Q-ary LDPC codes, which have been shown to outperform binary LDPC codes and Reed–Solomon codes on the AWGN channel. In this paper, we report on our investigation of Q-ary LDPC coded MRCs, both with AWGN and with burst impairments, and we present a new reduced-complexity decoding algorithm for Q-ary LDPC codes. A reduced-complexity decoding algorithm for -LDPC codes was presented, which brings the complexity of LDPC codes over GF(16) to about 12 times that of comparable binary codes. This reduced-complexity algorithm makes -LDPC codes attractive for magnetic recording. We have investigated the performance of these codes on Lorentzian–Gaussian magnetic recording channel models equalized to high-order PR targets. -LDPC codes were shown to be a good alternative to B-LDPC or RS codes for magnetic recording, because they perform well with AWGN and outperform B-LDPC codes when burst impairments are present. We further conclude that future hard disk drive systems could use a single sector-size LDPC code over GF(16) without the need for an outer RS code.

2.5 High Throughput Low-Density Parity-Check Decoder Architectures, Engling Yeo, Payam Pakzad, Borivoje Nikolić, and Venkat Anantharam

In this paper two decoding schedules and the corresponding serialized architectures for low-density parity-check (LDPC) decoders are presented. They are applied to codes with parity check matrices generated either randomly or using geometric properties of elements in Galois fields. Both decoding schedules have low computational requirements. The original concurrent decoding schedule has a large storage requirement that is dependent on the total number of edges in the underlying bipartite graph, while a new, staggered decoding schedule which uses an approximation of the belief propagation, has a reduced memory requirement that is dependent only on the number of

bits in the block. The performance of these decoding schedules is evaluated through simulations on a magnetic recording channel.

The implementation of LDPC decoders for two classes of LDPC codes, based on random matrices and Euclidean geometries in Galois Fields have been described. The arithmetic structures are straightforward, and meet the high throughput requirements of magnetic recording applications. The proposed staggered decoding schedule decouples the memory requirement from its dependency on the number of edges in the graph. It is recognized that the staggered the decoding schedule will not achieve the same results as LDPC decoding under belief propagation. However, it represents a heuristic approach that results in significant reduction in implementation complexity. In consideration that practical power and area constraints are likely to limit the number of iterations to three, the staggered decoding schedule performs systematically better than the concurrent decoding schedule. Besides magnetic recording applications, the staggered decoding schedule is also appropriate for forward error correction applications in wireless, wireline, and optical communication systems.

2.6 VLSI Implementation of Low Density Parity Check Decoder W L Lee and Angus Wu

In this paper, a low complexity digital Low Density Parity Check (LDPC) turbo code decoder architecture for real-time cellular personal communication application is presented. The proposed VLSI decoder architecture alleviates the use of complex operations such as combinational arithmetic, exponent computations and reduce intermediate storage as well as interleaving latency by incorporating in-place algorithm, index look-up table and address counter. Besides, the output section and termination of iteration are implemented by simple decision logic. The entire decoder is designed and synthesized using Synopsys VHDL computer aided design tool.

2.7 Reduced Complexity Iterative Decoding of Low-Density Parity Check Codes Based on Belief Propagation Marc P. C. Fossorier, Member, IEEE, Miodrag Mihaljevic, and Hideki Imai, ´ Fellow, IEEE

In this paper, two simplified versions of the belief propagation algorithm for fast iterative decoding of low-density parity check codes on the additive white Gaussian noise channel are proposed. Both versions are implemented with

real additions only, which greatly simplifies the decoding complexity of belief propagation in which products of probabilities have to be computed. Also, these two algorithms do not require any knowledge about the channel characteristics. Both algorithms yield a good performance–complexity tradeoff and can be efficiently implemented in software as well as in hardware, with possibly quantized received values.

In this paper, two simple iterative algorithms for decoding LDPC codes have been proposed. Both algorithms require real additions only, and therefore achieve a good tradeoff between error performance and decoding complexity as well as fit hardware implementation with quantized received values. In particular, for the LDPC codes considered, the UMP BPbased decoding algorithm performs within a few tenths of a decibel of the BP algorithm at the BER 10 . Based on these results, we conclude that the UMP BP-based decoding algorithm provides an attractive solution to implement iterative decoding of LDPC codes. The UMP BP-based decoding algorithm has been derived from the BP algorithm by considering only the dominant contribution when evaluating the reliability associated with each check sum. Therefore, the performance of this algorithm can be further enhanced by adding correction values, as described in for MAP-based decoding algorithms. Furthermore, since for an LDPC code, each check sum consists of bits, with small, this approach provides an alternative way to implement the BP algorithm as at most correcting values have to be added. This method becomes attractive for hardware implementation of the BP algorithm since the corrective terms can be stored in a ROM.

2.8 LDPC and their Rateless Relatives:

In this, we have provided a comprehensive survey of the associated open literature that is related to LDPC codes and their rateless relatives.

LDPC codes were conceived by Gallager in his doctoral dissertation in 1962. However, having limited computing resources prevented him from proving the near-capacity operation of these codes and from finding rigorous performance bounds of the decoding algorithm. In addition to this, the introduction of Reed-Solomon (RS) codes a few years earlier , and the widely accepted belief that concatenated RS and convolutional codes were perfectly suited for

practical error-control coding resulted in Gallager's work becoming neglected by researchers for approximately 30 years.

Margulis proposed a structured regular construction for a half-rate Gallager code based on the Cayley graph, which is nowadays known as the 'Margulis' code. The algebraic construction rules for LDPC codes given by Margulis were still found to be valid and applicable by Rosenthal and Vontobel 20 years later, who proposed a similar code known as the 'Ramanujan-Margulis' code.

Tanner was first to propose the previously described graphical representation of LDPC codes using bipartite graphs. Tanner also introduced the min-sum as well as the sum-product decoding algorithms and demonstrated their convergence on cycle free-graphs. It was Wiberg , who first referred to these graphs as 'Tanner graphs' and extended them to include trellis codes. Forney is called these graphs as Tanner - Wiberg - Loeliger (TWL) graphs.

Another contribution related to that of Tanner was later made by Kschischang et al, when they introduced the so-called factor graphs. The natural association of factor graphs with the sum-product algorithm (SPA) was also discussed.

The advantages offered by linear block codes having low-density PCMs were rediscovered by MacKay and Neal, who proposed the MacKay-Neal (MN) codes and showed that pseudo-randomly constructed LDPC codes can perform within about 1.2 dB of the theoretical upper bound of the Shannon limit . Mao and Banihashemi in employed a heuristic technique, which compares LDPC codes using pseudo-randomly generated PCMs for short block lengths according to the 'girth distribution' performance criterion.Their method is based upon the intuition that the presence of short cycles (i.e. having a graph with a low girth) severely violates the independence assumption between the messages exchanged between the left and right vertices of the graph, potentially propagating errors propagate at a faster rate than they can be corrected.

Alon and Luby made the first attempt to design an LDPC code capable of correcting erasures. A more practical algorithm based on cascading random bipartite graphs was then devised . It is important to note that up to this point in time the understanding of LDPC codes was mostly limited to the regular codes. The understanding of both regular and irregular graphs was further deepened in and it was demonstrated that the performance of the latter may be superior to that exhibited by the former. Luby et al. devised a new probabilistic tool, which significantly simplified the analysis of the probabilistic decoding algorithm proposed by Gallager [1]. Richardson et al. further improved the results by using a technique referred to as density evolution] for analysing the behaviour of irregular LDPC codes. Discrete density evolution was used by Chung et al. in order to simulate a half-rate code having a block length of 107 exhibiting a performance within 0.04 dB of the Shannon limit at a bit error ratio (BER) of 10^{-6}.

Lentmaier et al. as well as Boutros et al. proposed a more generalized version of the classic LDPC codes of Gallager, which were referred to as generalized low-density (GLD) codes (sometimes also known as generalized LDPC (GLDPC)) codes. Instead of having each check node corresponding to a single-parity check (SPC) equation as in the conventional LDPC codes proposed by Gallager , the check nodes of GLDPC codes are associated with more powerful codes such as 9 Hamming codes,2 Bose Chaudhuri Hocquenghem (BCH) codes and RS codes. Irregular GLDPC codes have also been proposed by Liva et al. Recently, Wang et al. proposed the doubly-GLDPC (D-GLDPC), which represents a wider class of codes than those GLDPC codes proposed in , where linear block codes can be used as component codes for both the check and variable nodes.

2.9 RELATED PAPERS:

1) Near Shannon Limit Performance of Low Density Parity Check Codes by David J.C. MacKay and Radford M. Neal was the first paper to discuss LDPC, It is referenced in many research papers, 30 years old but still relevant.

2) Gallager Codes, Recent Results by David J. C. MacKay discusses Gallager Codes for LDPC.

3) Comprehensive Algorithmic Review and Analysis of LDPC Codes by Waheed Ullah, University of the Witwatersrand, Abid Yahya, Universiti Malaysia Perlis which gives the overall review of LDPC.

4) Overview of LDPC Codesby Zongjie Tu and Shiyong Zhang , Department of Computer and Information Technology ,Fudan University, Shanghai, China, gives very detailed information on LDPC.

5) Reduced Complexity Iterative Decoding of Low-Density Parity Check Codes Based on Belief Propagation by Marc P. C. Fossorier, Member, IEEE, Miodrag Mihaljevic, and Hideki Imai, ´ Fellow, IEEE gives the overview of new approaches in the field of LDPC.

6) Implementation of Near Shannon Limit Error-Correcting Codes Using Reconfigurable Hardware by Benjamin Levine , R Reed Taylor , Herman Schmit uses efficient PSK techniques.

7) Parallel Decoding Architectures for Low Density Parity Check Codes by C.Howland and A. Blanksby gives a good understanding of different decoding techniques for LDPC.

8)A 220mW 1Gb/s 1024-Bit Rate-1/2 Low Density Parity Check Decoder by Chris Howland and Ansrew Blanksby, High Speed Communications VLSI Research Department, Agere Systems, Holmdel NJ 07733 is an FPGA implementation of LDPC.

9) Performance Analysis and Code Optimization of Low Density Parity-Check Codes on Rayleigh Fading Channels

by Jilei Hou, Student Member, IEEE, Paul H. Siegel, Fellow, IEEE, and Laurence B. Milstein, Fellow, IEEE, gives the detailed performance analysis of LDPC codes.

10) Low-Density Parity-Check (LDPC) Coded OFDM Systems with M-PSK by Hisashi Futaki, Tomoaki Ohtsuki, Graduate School of Science and Technology, Tokyo University of Science, Faculty of Science and Technology, Tokyo University of Science

11) Reduced-Complexity Decoding of Q-ary LDPC Codes for Magnetic Recording Hongxin Song, Member, IEEE, and J. R. Cruz, Fellow, IEEE is the latest research paper.

12) Efficient Encoding of Low-Density Parity-Check Codes by Thomas J. Richardson and Rüdiger L. Urbanke

13) High Throughput Low-Density Parity-Check Decoder Architectures, Engling Yeo, Payam Pakzad, Borivoje Nikolić, and Venkat Anantharam Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720-1770, again a latest paper which increases efficiency.

CHAPTER 3: METHODOLOGY

3.1 Verilog:

Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL). It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip−flop. It means, by using a HDL we can describe any digital hardware at any level. Designs, which are described in HDL are independent of technology, very easy for designing and debugging, and are normally more useful than schematics, particularly for large circuits.
We are using Verilog to model the LDPC Decoder.

3.2 Quartus Prime:

- Intel Quartus Prime is programmable logic device design software produced by Intel; prior to Intel's acquisition of Altera the tool was called Altera Quartus Prime, earlier Altera Quartus II. Quartus Prime enables analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Quartus Prime includes an implementation of VHDL and Verilog for hardware description, visual editing of logic circuits, and vector waveform simulation.
- The Lite Edition is a free version of Quartus Prime that can be downloaded for free. This edition provided compilation and programming for a limited number of Intel FPGA devices. The low-cost Cyclone family of FPGAs is fully supported by this edition, as well as the MAX family of CPLDs, meaning small developers and educational institutions have no overheads from the cost of development software.
- We are using a lite version of Quartus Prime in this project.

3.3 ModelSim:

ModelSim is a multi-language environment by Mentor Graphics, for simulation of hardware description languages such as VHDL, Verilog and SystemC, and includes a built-in C debugger. ModelSim can be used independently, or in conjunction with Intel Quartus Prime, PSIM, Xilinx ISE or Xilinx Vivado.
Here we are using ModelSim in conjunction with Intel Quartus Prime to view the waveforms and verify in hardware.

3.4 DESim:

The DESim application provides a graphical user interface (GUI) that represents some of the features of a DE1-SoC board. This GUI serves as a "front end" for the ModelSim simulator. Using the DESim GUI you can invoke both the ModelSim Verilog compiler and simulator. Inputs to the ModelSim simulator can be provided by clicking on features in the DESim GUI, which also shows results produced by the simulator on displays that look like the ones on a DE1-SoC board.

3.4 Matlab:

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. In this project we are using Matlab for simulation of a modulation using LDPC encoding decoding and to compare the bit error rate of the proposed Min Sum algorithm to the Hard Decision algorithm.

3.6 Methodology

This mini-project work undertaken by us involves writing Verilog code for the hardware implementation of LDPC decoding using tools like Quartus Prime and ModelSim. Testing and verification of the results in suitable hardware in DeSim. Compare the Min Sum algorithm bit error rate with the Hard Decision algorithm to understand which one is better.

CHAPTER 4 : BLOCK DIAGRAM & IMPLEMENTATION

4.1 IMPLEMENTATION:

4.1.1 General Block Diagram of LDPC Encoder and Decoder

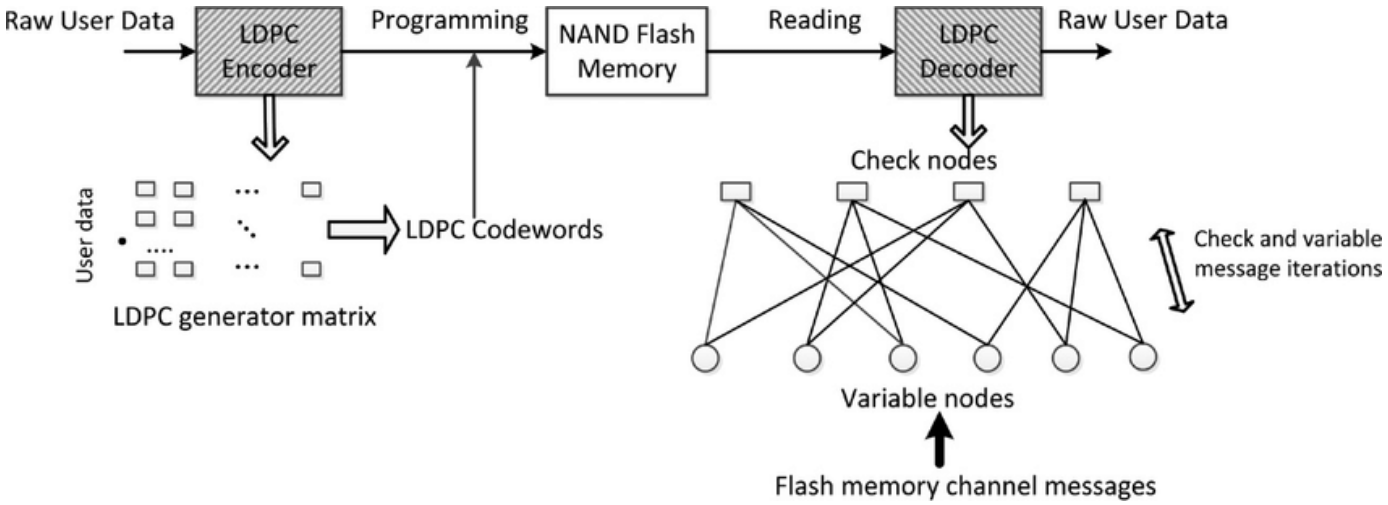


fig2.Encoder and Decoder Block Diagram

The above figure fig 2 is a basic block diagram showing the Encoding and Decoding of LDPC. The point to note here is that at the decoding end the architecture uses Check Nodes and Variable Nodes along with RAM flash memory for the decoding process.

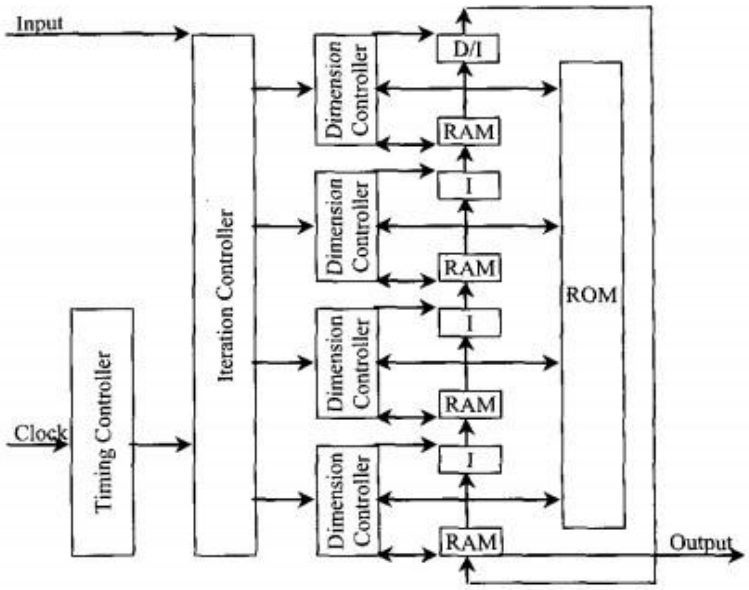
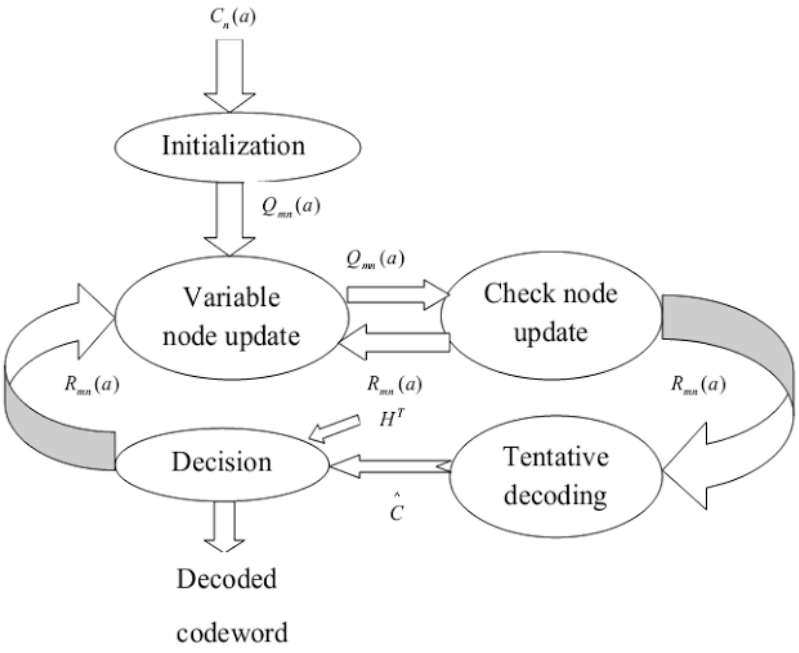


fig3 Basic Components of LDPC Decoder

The architecture proposed mainly has 4 components. LDPC Control circuit, Address Generator, 36 RAM cells and Comparator, where the Check Node Update and Variable Node Update is done. The above figure fig 3 shows a basic block diagram showing that the timing,dimension and iteration control is important in LDPC, which is carried out by LDPC Control. RAM of course requires an Address Generator. Inside RAM cells and comparator decoding is done and the output is buffered till proper timing signal sync_out is obtained and output is written out.



STEP 1 Initialization: Set $i = 0$ and the maximum number of iterations to I_{max}. Set $q_{vc} = y_v$.

STEP 2 Check node update: at check node $0 \leq c \leq \gamma m - 1$, for $0 \leq v < \rho m - 1$, compute $\sigma_{cv}^{(i)}$ by

$$\sigma_{cv} = \alpha \cdot \min_{v' \in \mathcal{N}(c) \backslash v} |q_{cv'}| \cdot \prod_{v' \in \mathcal{N}(c) \backslash v} \text{sign}\left(q_{cv'}\right)$$

STEP 3 Variable node update: At variable node $0 \leq v < \rho m - 1$, for $0 \leq c \leq \gamma m - 1$, compute q_{vc} and z_v by

$$\begin{aligned} q_{vc} &= y_v + \sum_{c' \in \mathcal{M}(v) \backslash c} \sigma_{c'v} \\ z_v &= y_v + \sum_{c \in \mathcal{M}(v)} \sigma_{cv} \end{aligned}$$

STEP 4 Tentative decode: If $\text{sign}\left(\mathbf{z}\right) \cdot \mathbf{H}^T = 0$ or I_{max} is reached, go to (5). Otherwise, $i \leftarrow i + 1$ and go to (2).

STEP 5 Termination: Take $\text{sign}\left(\mathbf{z}\right)$ as the decoded codeword and stop the decoding process.

fig 4 Min-Sum Algorithm flow

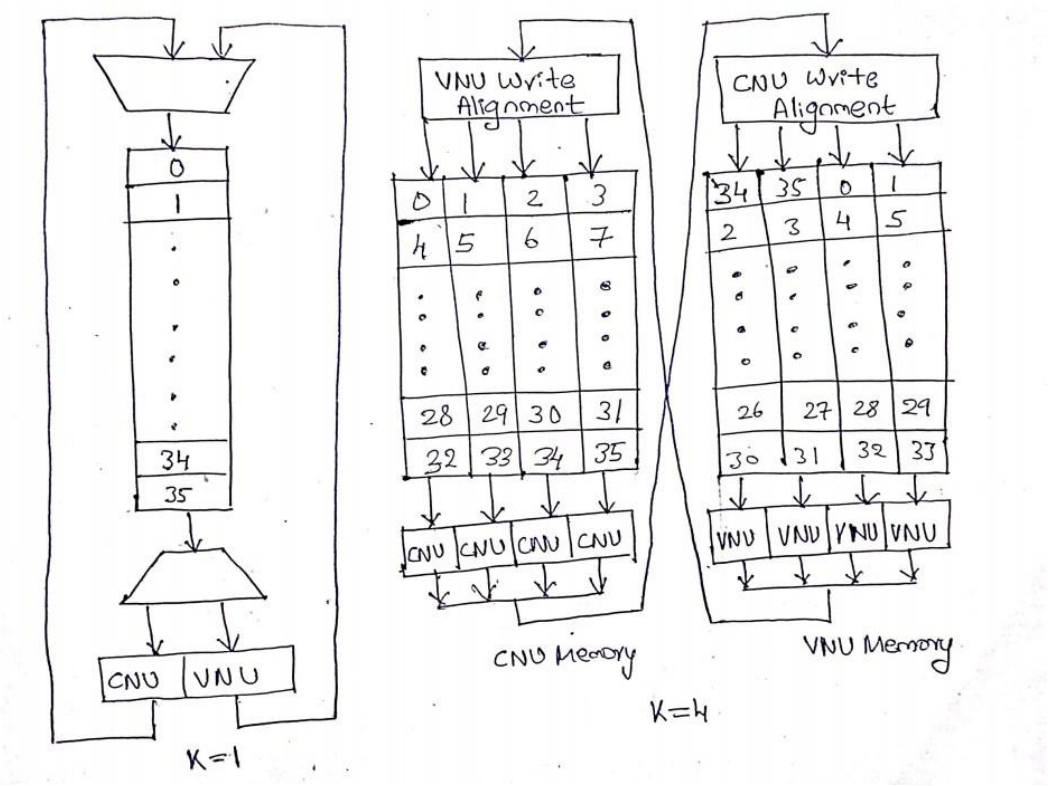


fig 5 Message Packing and Alignment

In the above figure two examples for Message Packing and Alignment inside comparator are given. The Check Node Update, Variable Node Update and number of iterations are carried out here. The 36 RAM cells are used for these operations.

4.1.2 HARDWARE & SOFTWARE REQUIREMENTS

Verilog

ModelSim

Quartus Prime

DESim

Matlab

CHAPTER 5: RESULT AND DISCUSSIONS

LDPC Decoding

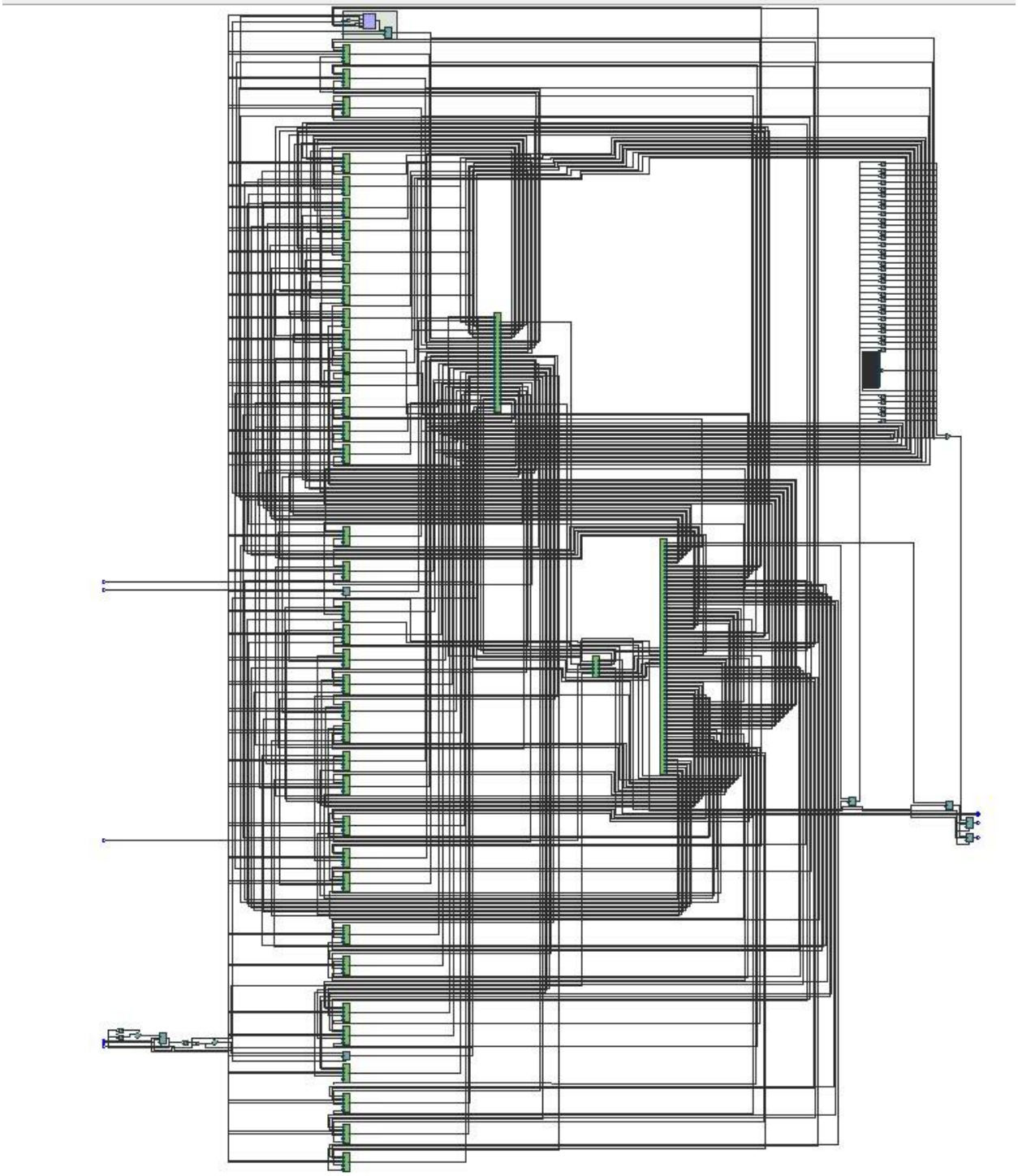


fig 6 RTL of LDPC Decoder

The RTL above mainly has 4 components. Ldpc_cntrl, addr_generator, 36 RAM cells and data_comparator.

The input is given to ldpc_cntrl which is an fsm ,gives the correct timing and calculates the sigma value for the message packing and alignment operation. The output is given to the address generator which generates 36 write addresses to drive the 36 RAM cells and dynamically allocate memory for the operation of decoding which takes place in data Comparator, after the number of iterations completed, the outputs are buffered for proper sync_out signal and when it is high, data_out is written out.

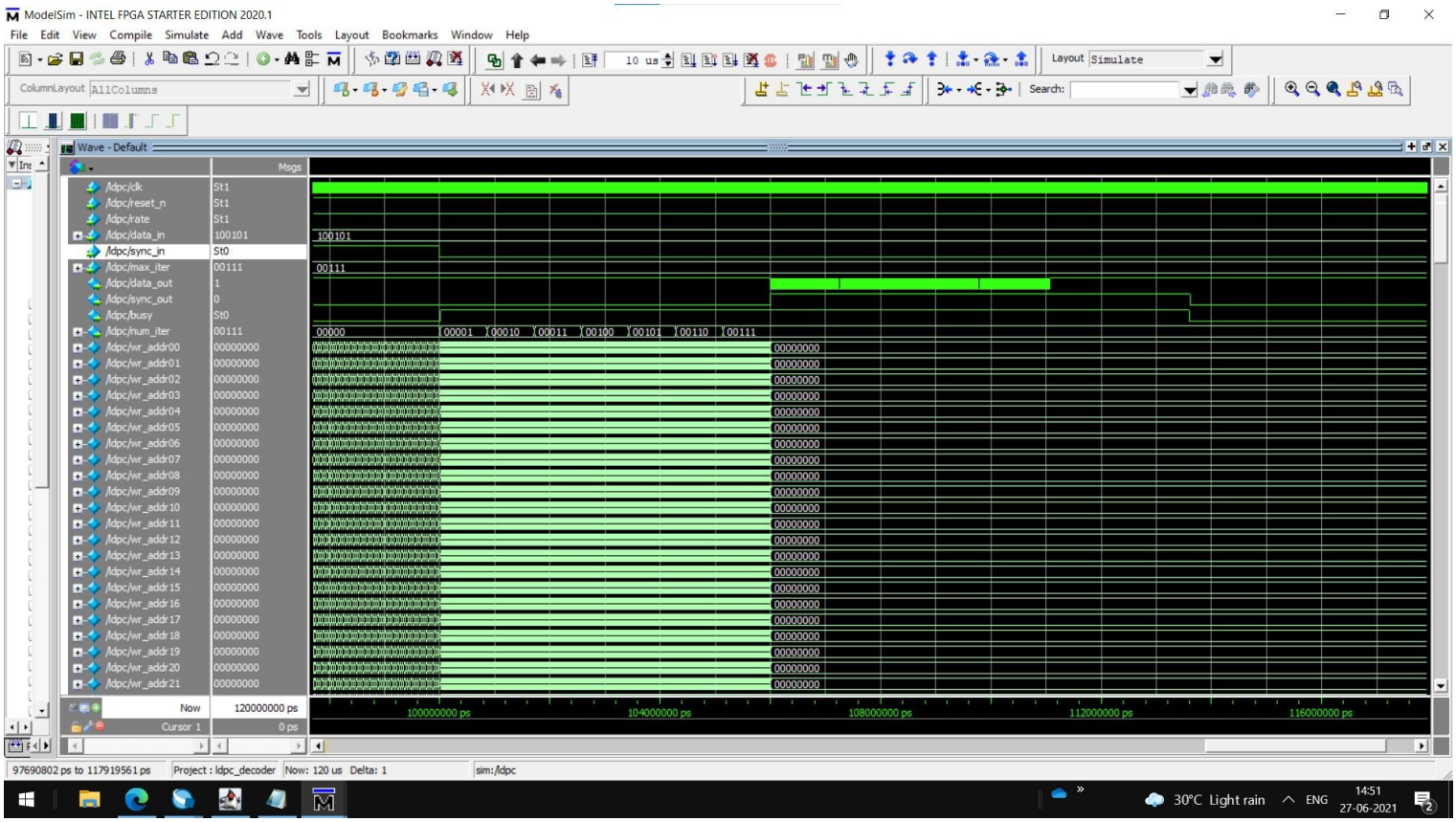


fig 7 ModelSim simulation

Above figure is the simulation using ModelSim software, which shows the result that after no. of iterations that is here max_iter = 7, the sync_out is high and the data is written out serially.

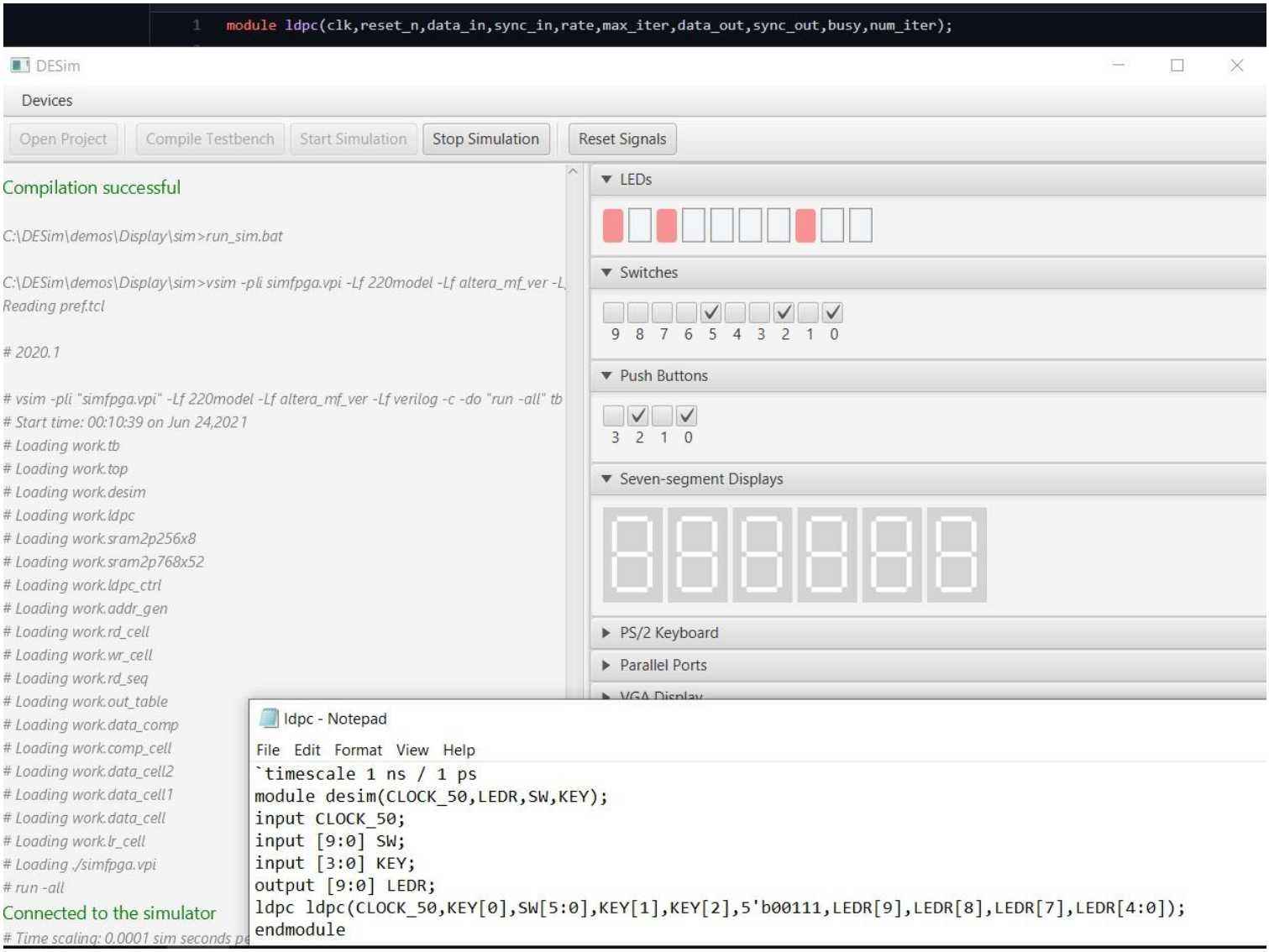
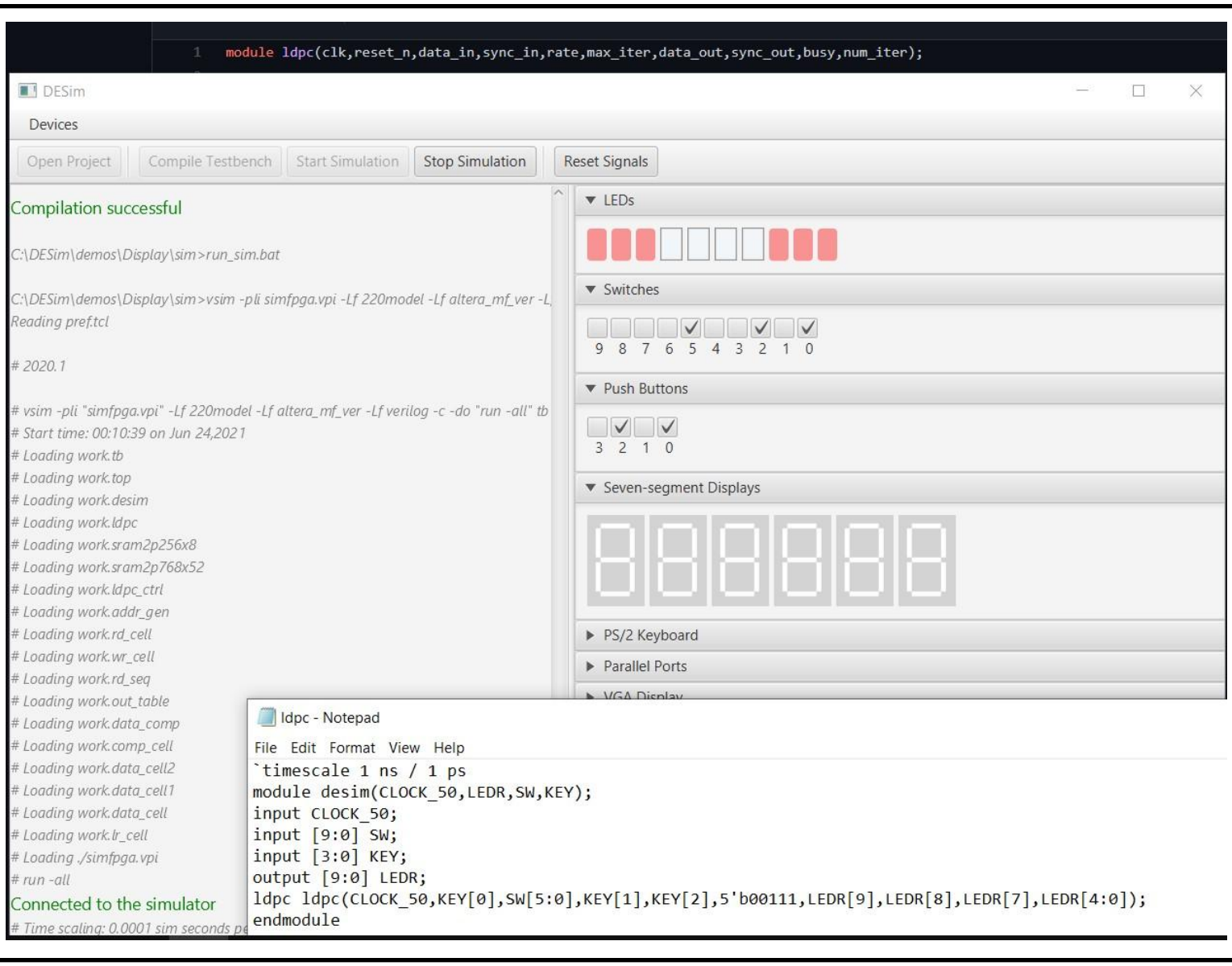


fig 8 DESim simulation of DE10 lite at num. of iterations = 4

Above figure shows the implementation of ldpc in Max 10 fpga DESim emulator for DE10 lite FPGA. The interface looks more like DE1- Soc. Here the no. of iterations has reached to 4. And the busy signal is high.

In the below figure, no. of iterations has reached maximum, that is in this case 7, and the sync_out and busy signals are high. Here the data is being written out.


1 module ldpc(clk,reset_n,data_in,sync_in,rate,max_iter,data_out,sync_out,busy,num_iter);
DESim
Devices
Open Project
Compile Testbench
Start Simulation
Stop Simulation
Reset Signals
Compilation successful
C:\DESim\demos\Display\sim>run_sim.bat
C:\DESim\demos\Display\sim>vsim -pli simfpga.vpi -Lf 220model -Lf altera_mf_ver -L
Reading pref.tcl
2020.1
vsim -pli "simfpga.vpi" -Lf 220model -Lf altera_mf_ver -Lf verilog -c -do "run -all" tb
Start time: 00:10:39 on Jun 24,2021
Loading work.tb
Loading work.top
Loading work.desim
Loading work.ldpc
Loading work.sram2p256x8
Loading work.sram2p768x52
Loading work.ldpc_ctrl
Loading work.addr_gen
Loading work.rd_cell
Loading work.wr_cell
Loading work.rd_seq
Loading work.out_table
Loading work.data_comp
Loading work.comp_cell
Loading work.data_cell2
Loading work.data_cell1
Loading work.data_cell
Loading work.lr_cell
Loading ./simfpga.vpi
run -all
Connected to the simulator
Time scaling: 0.0001 sim seconds pe
LEDs
Switches
9 8 7 6 5 4 3 2 1 0
Push Buttons
3 2 1 0
Seven-segment Displays
PS/2 Keyboard
Parallel Ports
VGA Display
ldpc - Notepad
File Edit Format View Help
`timescale 1 ns / 1 ps
module desim(CLOCK_50,LEDR,SW,KEY);
input CLOCK_50;
input [9:0] SW;
input [3:0] KEY;
output [9:0] LEDR;
ldpc ldpc(CLOCK_50,KEY[0],SW[5:0],KEY[1],KEY[2],5'b00111,LEDR[9],LEDR[8],LEDR[7],LEDR[4:0]);
endmodule

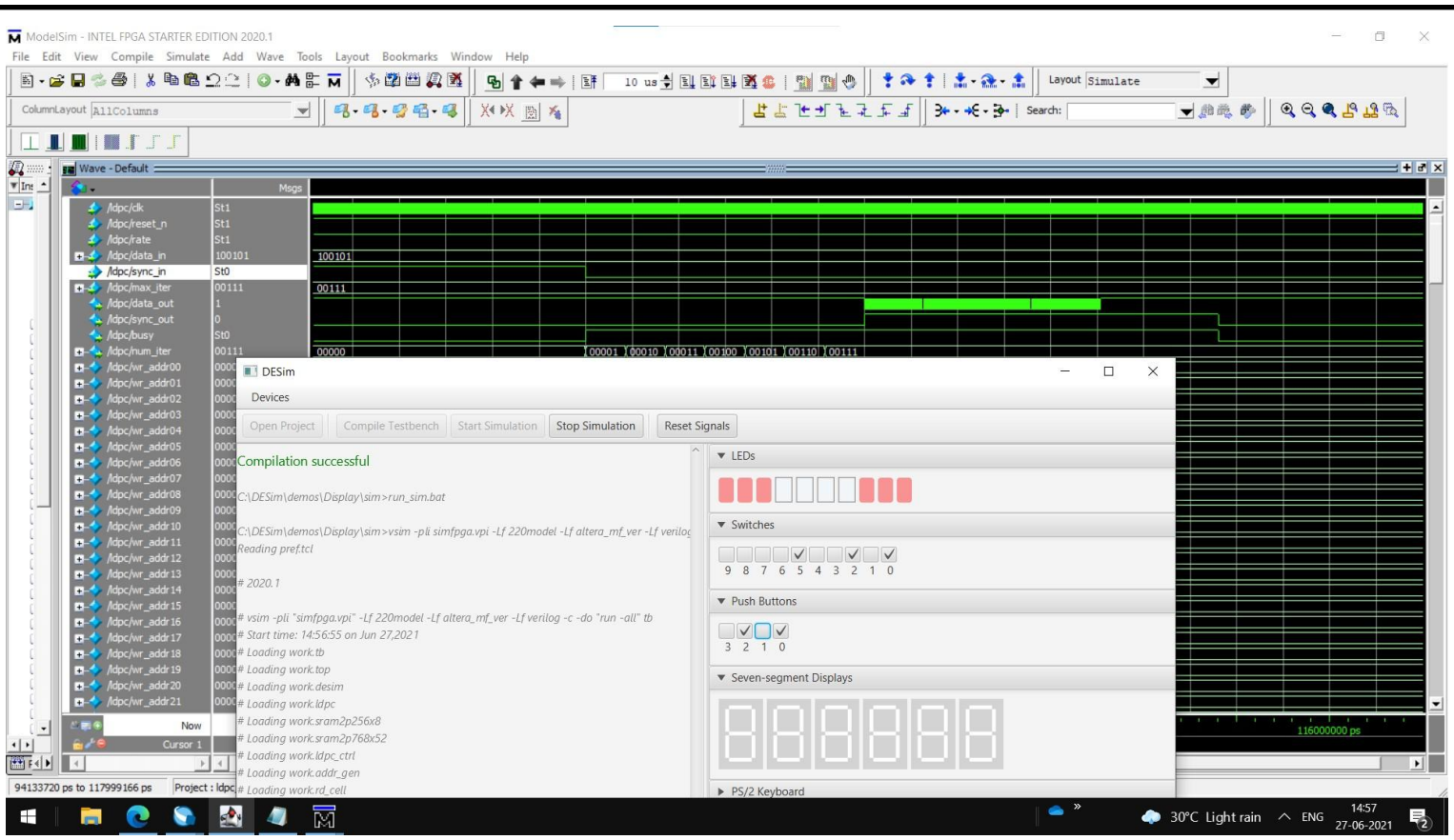


fig 10 DESim output when no. of iterations = 7 and data is being written out along with modelsim output

Above figure shows modelsim output and desim output together so that it could be understood easily.

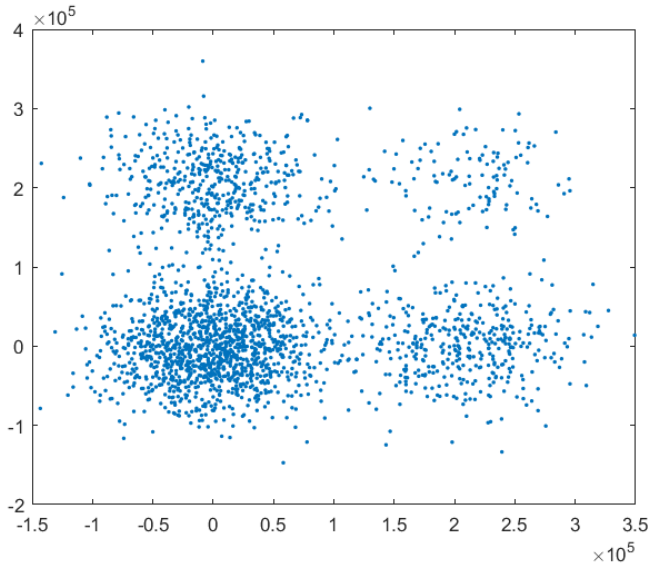


fig 11 16 qam using LDPC Encoding and Decoding

Above figure shows the output simulation of a modulation here 16qam using LDPC. The bit error rate is calculated for min-sum algorithm and hard decision algorithm.

ldpc_encode.m | ldpc_decode.m

```
10 -    clc;
11 -    format compact;
12 -    clear all;
13 -    coderate = 0.5;
14 -    mode = '16qm';
15      % modulate = 'bpsk' 'qpsk' '16qm'
16 -    SNR = 7.7;
17
18 -    if coderate == 0.5
19 -        X=randi(9216*coderate,1);
20          %X=zeros(9216*coderate,1);
21 -        load data\G.mat
22 -        PC= mod((X*X),2);
23 -        MSG(1:4608)=PC';
24 -        MSG(4608+1:4608+4608)=X;
25          %col_order=[0 1 2 3 4 5 9 10 11 13 15 16 17 19 20 22 23 24 26 27 31 32 33 34 36 37 38 39 41 4
26 -        load data\col_order.mat
27 -        for i=1:9216
28 -            C(col_order(i)+1)=MSG(i);
29 -        end
30 -    end
31
32 -    if coderate == 0.75
33 -        X=randint(9216*coderate,1);
```

Command Window

```
Hard Decision BER: 8104
Min-Sum Alogorithm BER: 7752
```

fig 12 BER for HD algorithm and proposed min-sum algorithm

Bit Error Rate for Min Sum Algorithm is better compared to Hard Decision algorithm

CHAPTER 6: CONCLUSION

In this mini-project undertaken by us, we tried to implement LDPC Decoding using Min Sum algorithm in FPGA.

After doing the literature survey we got a detailed understanding of advancements happening in the field of Linear Block Codes, LDPC Codes Basics, its rateless relatives, types of LDPC Encoding and Decoding etc.

DESim is used for the FPGA implementation which is an emulator of DE-10 lite FPGA Kit by FPGAcademy because of unavailability of physical FPGAs in labs.

The RTL simulation is done using Quartus Prime and RTL is obtained , which gives a detailed understanding of verilog implementation at circuit level.

Output is verified using the ModelSim simulation tool.

Min-Sum algorithm and Hard Decision algorithm are compared using Bit Error Rate parameter which shows that Min-Sum algorithm with llr approximation has advantages. This analysis is done using the Matlab tool.

CHAPTER 7:Applications

3GPP

5G NR

5G NR is the mobile broadband standard of the 5th generation. A new rate compatible structure for LDPC codes are employed for channel coding to fulfill the broad applications supported by the standard.

Creonic's 5G LDPC Decoder IP Core provides a perfect solution for this new LDPC structure with high level of flexibility while maintaining high throughput and low latency as required by the standard.

ETSI

DVB-S2X

DVB-S2X is the next generation satellite transmission standard which is an extended version of its well-established predecessor DVB-S2. The new specification allows for spectral efficiency gains of up to 50% by offering lower roll-off factors, higher modulations and a finer code rate granularity compared to DVB-S2.

DVB-S2

In 2005 DVB-S2 became the first standard to adopt LDPC codes. Today it is quite popular and the de-facto standard for high-speed satellite communication. The standard defines four different system configurations and application areas: broadcast services, interactive services, digital satellite news gathering (DSNG), and professional services.

The properties of the LDPC codes in this standard make the hardware implementation of the LDPC decoder quite challenging. With 64800 bits the DVB-x2 series offers the longest LDPC codeword sizes, consuming quite a bit of memory in a hardware realization. Throughputs are typically less than 100 Mbit/s on the air interface. Together with an outer BCH decoder, the forward error correction of the DVB-S2 standard achieves an outstanding error correction performance.

DVB-T2

DVB-T2 is the successor of DVB-T. It was published in 2009 and integrates a subset of the LDPC codes as defined in DVB-S2. Two LDPC codes (block length 16200, code rate 3/5 and block length 64800, code rate 2/3) were, however, replaced. While DVB-S2 uses LDPC and BCH coding only for payload data (so-called baseband frames, BBFrames), DVB-T2 uses two LDPC codes (16200 bits, rate 1/5 and rate 4/9) for the signalling of the current configuration of the DVB-T2 system.

DVB-T2-Lite

The latest version of the DVB-T2 standard (V 1.3.1, Annex I) contains a new lightweight profile. The main objective of DVB-T2-Lite is the reduction of receiver complexity so that applications like mobile broadcasting become feasible. Therefore only the short LDPC frames with 16200 bits are contained within DVB-T2-Lite, resulting in a decreased LDPC/BCH decoder complexity.

DVB-C2

DVB-C2, the successor of DVB-C, contains a subset of the LDPC codes as defined in DVB-S2. A single code is used (64800 bits, code rate 2/3) that was introduced with DVB-T2 only. Since for cable networks high signal-to-noise ratios are common, the lower code rates have been removed allowing for a reduced decoder complexity. The code with the lowest code rate (16200 bits, code rate 4/9) is only used for the sending of signalling information.

GMR-1

GEO-Mobile Radio (GMR) is a standard for satellite telephony that follows the GSM standard in many ways. Only the three lower layers of the OSI model differ between GMR and GSM (for GMPRS only the two lowest layers).

Two versions of the standard exist: GMR-1 (ETSI TS 101 376) and GMR-2 (ETSI TS 101 377). For GMR-1 three releases exist. Release 2 and Release 3 of GMR-1 adopted LDPC codes in 2008 and 2009, respectively. The standard is characterized by low throughput requirements of less than 1 Mbit/s. Puncturing, shortening, and repeating is applied in order to obtain different code rates and block lengths from the parity check matrices.

IEEE

IEEE 802.3 (10G BASE-T)

The IEEE 802.3 standard defines 10 gigabit Ethernet and was first published in 2002. In 2006 the IEEE 802.3an standard was released as an amendment to IEEE 802.3-2005. This amendment (10 GBASE-T) defines the 10 gigabit transmission over shielded or unshielded twisted pair cables for distances of up to 100 m. It uses LDPC codes for forward error correction. The IEEE 802.3an amendment was consolidated into IEEE 802.3-2008.

10 GBASE-T contains a special class of LDPC codes (so-called Reed-Solomon code-based LDPC codes or RS-LDPC codes). A Reed-Solomon code is used to define the generator matrix of the LDPC code. The LDPC code construction method guarantees that no cycles of length four are contained within the Tanner graph. Since the structure of the parity check matrix differs from all other standardized LDPC codes, different decoder architectures become mandatory.

IEEE 802.11 (WiFi)

IEEE 802.11n is the successor of the IEEE 802.11a/b/g standards. It is particularly designed for higher throughputs. In contrast to the previous IEEE 802.11 standards, 11n can use multiple antennas (MIMO) allowing for the transmission of multiple data streams in parallel. The throughput of each data stream can be as high as 150 Mbit/s on the air interface. With a maximum of four antennas up to 600 Mbit/s are defined within the standard.

IEEE 802.11n defines twelve LDPC codes. Convolutional coding is mandatory, usage of LDPC coding is optional. The IEEE 802.11n codes are reused within the IEEE 802.11ac standard that is intended to further increase the transmission speed.

IEEE 802.15.3c (60 GHz PHY)

IEEE 802.15.3-2003 is a standard for high data rate wireless personal area networks (WPAN). The IEEE 802.15.3c-2009 amendment describes an alternative PHY layer to the IEEE 802.15.3-2003 standard. The new mmWave PHY layer operates in the 60 GHz band (57 - 64 GHz) and allows for air throughputs of up to 5 Gbit/s. The standard uses LDPC codes for these high data rate modes. In particular, the single carrier (SC) mode and the high speed interface (HSI) mode use LDPC codes.

The standard defines five LDPC codes with two block lengths. In order to satisfy the high throughput requirements, special decoder architectures with an increased parallelism compared to other standards become mandatory.

IEEE 802.16 (Mobile WiMAX)

Along with DVB-S2 and the drafts of IEEE 802.11n, Mobile WiMAX (Worldwide Interoperability for Microwave Access) was one of the first standards to adopt LDPC codes for forward error correction. Mobile WiMAX was first defined in IEEE 802.16e-2005 as an amendment to IEEE 802.16-2004, and later consolidated into IEEE 802.16-2009. The throughputs of WiMAX systems are typically much less than 100 Mbit/s. Using the LDPC codes is optional.

The standard offers the highest block length flexibility of all standards that apply LDPC codes. Overall 19 block lengths are defined. Each block length comes with four code rates. For two code rates (rate 2/3 and rate 3/4 the standard defines two different LDPC codes with minor differences in error correction performance. All in all, 114 LDPC codes are contained within the WiMAX standard. However, only six parity check matrices are used to derive all other matrices. The usage of LDPC coding is optional, only convolutional coding is mandatory.

The same LDPC codes are used within the IEEE 802.22 and ITU-T G.hn standards, see below.

IEEE 802.22 (WRAN)

IEEE 802.22 is a standard for wireless broadband access that uses the so-called white spaces between occupied channels in the TV frequency spectrum. The aim of the standard is to bring broadband access to low population density areas. The maximum data rate is about 20 Mbit/s. Due to its cognitive radio techniques, it has the potential to be applied in many regions worldwide.

As with ITU-T G.hn the standard uses the WiMAX (IEEE 802.16) LDPC codes as LDPC code basis. Compared to WiMAX two new block lengths are introduced (384 and 480 bits). Furthermore, it no longer contains two different codes for code rate 2/3 and code rate 3/4. Instead it adopted the codes 2/3B and 3/4A only. So despite the new block lengths, the number of LDPC codes decreased from 114 for WiMAX to 84 for IEEE 802.22. LDPC coding is optional, only convolutional coding is mandatory.

ATSC 3.0

Advanced Television Systems Committee (ATSC) standards are a set of standards developed by the Advanced Television Systems Committee for digital television transmission over terrestrial, cable, and satellite networks.

The standard describes 24 LDPC codes that are similar to those of DVB-S2/-T2/-C2. The codes are concatenated with an inner BCH encoder.

DOCSIS 3.1

Data Over Cable Service Interface Specification is an international telecommunications standard that permits the addition of high-bandwidth data transfer to an existing cable TV (CATV) system.

The standard describes six LDPC codes, whereof one is taken from DVB-C2. For some codes puncturing and shortening is applied in order to obtain different block sizes and code rates.

CCSDS

The CCSDS (The Consultative Committee for Space Data Systems) published an "experimental specification" for near-earth and deep space communication in 2007. The document was contributed to CCSDS by NASA (National Aeronautics and Space Administration). In 2011 the LDPC codes were adopted by a blue book as "recommended standard".

The documents describe ten LDPC codes, one optimized for near-earth communication (block length 8176), and all others optimized for deep space communication. The block lengths of the deep space codes were selected such that three lengths of information words exist (1024, 4096, and 16384).

DTMB (DMB-T/H)

Digital Terrestrial Media Broadcast (DTMB) is a Chinese standard for digital broadcasting. Unlike CMMB, it is intended for fixed terminals and supports HDTV transmission. It will replace the analog TV transmission in China. Data rates of up to 32 Mbit/s are supported.

The standard defines three LDPC codes of the same block length. The forward error correction uses an outer BCH decoder. A specialty of the defined codes is the submatrix size of 127. This is a prime number that has some negative influence on an efficient hardware decoder realization.

ITU-T G.hn (G.9960)

G.hn is the name for home grid technologies defined by the International Telecommunication Unit (ITU). The recommendation G.9960 defines physical layer and system architecture while recommendation G.9961 defines the data link level. The standard defines the communication over three different types of wires: coaxial cables (cable networks), telephone lines, and power lines. G.hn systems achieve throughputs of up to 1 Gbit/s.

The standard uses a subset of the WiMAX (IEEE 802.16) LDPC codes in order to derive its own LDPC codes with different block lengths. While the WiMAX codes are defined for a block length of 2304, the G.hn standard defines

seven different block lengths with a total of three different code rates (rate 1/2, rate 2/3, rate 5/6). The shortest block length is used for header information only, while all other block lengths hold payload information. The standard defines puncturing patterns to increase the code rate beyond rate 5/6. By the removal of parity bits from the highest rate codes before transmission, the code rates 16/18 and 20/21 are obtained.

WiMedia 1.5 UWB

The WiMedia Alliance is a non-profit organization that promotes and certifies ultra-wide band (UWB) technologies. In version 1.5 of its physical layer, the WiMedia standard adopted LDPC codes for high data rates (payload throughputs of up to 1 Gbit/s). For lower rates, convolutional codes are used. The standard defines two block lengths: 1200 and 1320. The long blocks are obtained by a re-encoding of the short blocks with a rate 10/11 LDPC code. These additional parity bits are transmitted on the guard tones of an OFDM symbol for throughputs of 640 Mbit/s and above. The receiver, however, is allowed to ignore these 120 additional parity bits for decoding.

DVB-NGH

DVB-NGH is a draft standard for digital broadcasting systems for handheld devices. Parts of the standards are similar to DVB-T2-Lite. Hence, the maximum block length of the LDPC codes is 16200 bits. Seven new LDPC codes were added to the DVB family of standards (16200 bit codewords with rates 4/15, 7/15, 8/15, 9/15; 4320 bit codewords with rates 1/5 and 1/2, 8640 bit codeword with rate 1/4). All other codes have been used before, e.g., in DVB-S2.

DVB-NGH uses two LDPC codes (4320 bits, rate 1/5 and 8640 bits, rate 1/2) for signalling the current configuration of the DVB-NGH system. The 8640 bits code is an extended LDPC code based on a code with 4320 bits and rate 1/2.

IEEE 802.11ac (WiFi)

The main objective of IEEE 802.11ac is to increase the throughputs of the previous IEEE 802.11 standards. Compared to IEEE 802.11n, the draft of IEEE 802.11ac allows for eight antennas (11n: four), 256-QAM modulation (11n: 64-QAM), and channel bandwidths of up to 160 MHz (11n: 40 MHz). The changes in the standard allow for a theoretical throughput of up to 7 Gbit/s. The LDPC codes are the same as in IEEE 802.11n.

IEEE 802.11ad (WiGig)

IEEE 802.11ad is an amendment to IEEE 802.11-2007. Its intention is to modify the physical and MAC layer of the standard to enable a high throughput data transmission in the 60 GHz frequency band.

The standard defines four LDPC codes that are different from the codes defined in IEEE 802.11n and IEEE 802.11ac. LDPC coding is mandatory, no other coding scheme is specified. The increased submatrix size (42) of the parity check matrices relaxes the problem of achieving Gbit throughputs for such small block lengths in comparison to IEEE 802.11ac/n. In those standards the submatrix size is only 27 for a block length of 648 bits.

REFERENCES

[1] Near Shannon Limit Performance of Low Density Parity Check Codes - David J.C. MacKay, Radford M. Neal

[2] Gallager Codes – Recent Results David J. C. MacKay

[3] Comprehensive Algorithmic Review and Analysis of LDPC Codes, Waheed Ullah, University of the Witwatersrand, Abid Yahya, Universiti Malaysia Perlis

[4] Overview of LDPC Codes Zongjie Tu and Shiyong Zhang Department of Computer and Information Technology Fudan University, Shanghai, China

[5] VLSI Implementation for Low Density Parity Check Decoder, W.L.Lee and Angus Wu, Electronics Design Automation Center, Department of Electronic Engineering City University of Hong Kong, Tat Chee Avenue, Koloon Tong, Kowloon, Hong Kong.

[6] Reduced Complexity Iterative Decoding of Low-Density Parity Check Codes Based on Belief Propagation Marc P. C. Fossorier, Member, IEEE, Miodrag Mihaljevic, and Hideki Imai, ´ Fellow, IEEE

[7] Implementation of Near Shannon Limit Error-Correcting Codes Using Reconfigurable Hardware, Benjamin Levine , R Reed Taylor , Herman Schmit

[8] Parallel Decoding Architectures for Low Density Parity Check Codes, C.Howland and A. Blanksby

[9] A 220mW 1Gb/s 1024-Bit Rate-1/2 Low Density Parity Check Decoder , Chris Howland and Ansrew Blanksby, High Speed Communications VLSI Research Department, Agere Systems, Holmdel NJ 07733

[10] Performance Analysis and Code Optimization of Low Density Parity-Check Codes on Rayleigh Fading Channels Jilei Hou, Student Member, IEEE, Paul H. Siegel, Fellow, IEEE, and Laurence B. Milstein, Fellow, IEEE

[11] Performance Comparison of Layered Space Time Codes Ka Leong Lo, Slavica Marinkovic, Zhuo Chen and Branka Vucetic The School of Electrical and Information Engineering, The University of Sydney, NSW 2006, Australia

[12] Low-Density Parity-Check (LDPC) Coded OFDM Systems with M-PSK, Hisashi Futaki, Tomoaki Ohtsuki, Graduate School of Science and Technology, Tokyo University of Science, Faculty of Science and TEchnology, Tokyo University of Science

[13] Reduced-Complexity Decoding of Q-ary LDPC Codes for Magnetic Recording Hongxin Song, Member, IEEE, and J. R. Cruz, Fellow, IEEE

[14] Efficient Encoding of Low-Density Parity-Check Codes Thomas J. Richardson and Rüdiger L. Urbanke

[15] High Throughput Low-Density Parity-Check Decoder Architectures, Engling Yeo, Payam Pakzad, Borivoje Nikolić, and Venkat Anantharam Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720-1770

[16] VLSI Implementation-Oriented (3,k)-Regular Low-Density Parity-Check Codes, Tong Xhang and Keshab K.Parhi,Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455, USA

[17] Low Density Parity Check Codes over GF(q), Matthew C. Davey and David J. C MacKay, Cavendish Laboratory, Cambridge CB3 OHE, England

[18] Design of Low-Density Parity Check Codes for Bandwidth Efficient Modulation , Jilei Hou, Paul H. Siegel, Laurence B. Milstein, and Henry D. Pfister, Dept. of Electrical and Computer Engineering, 0407, University of California, San Diego, LAa Jolla, CA 92093-0407 , USA

[19] Low-Density Parity-Check Codes Based on Finite Geometries: A Rediscovery and New Results Yu Kou, Student Member, IEEE, Shu Lin, Fellow, IEEE, and Marc P. C. Fossorier, Senior Member, IEEE

[20] Joint Code and Decoder Design for Implementation Oriented (3, k)- regular LDPC Codes, Tong Zhang and Keshab K. Parhi, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455, USA

[21] Low Density Parity Check Codes for Magnetic Recording Channels Hongxin Song, Richard M. Todd, and J. R. Cruz

[22] Low-Density Parity-Check Codes for Digital Subscriber Lines E. Eleftheriou and S. Ölçer IBM Research, Zurich Research Laboratory 8803 Rüschlikon, Switzerland

[23] Low-Density Parity-Check Codes and Their Rateless Relatives,Nicholas Bonello, Sheng Chen and Lajos Hanzo