DuckSim

Computer Architecture and Embedded Systems (CAES) Lab

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Core Concept:

DuckSim is a computer architecture simulation tool with modular components and granularity of analysis that can be scaled various time-slice and physical implementation resolutions.

Motivation:

Existing architecture simulation environments (MIT’s *Hornet*, etc.) are over-specified with particular hardware models or research questions in mind, and do not offer value to the researcher exploring completely novel architectures. DuckSim is a novel modeling and simulation platform designed from the ground up to provide lasting value to computer architects by facilitating extensibility, modularity, and appropriate levels of analysis at all phases of design and implementation.

Summary:

In order to provide a robust, efficient, and general-purpose prototyping environment for the design and testing of novel computer architectures, the DuckSim project is being developed by the CAES Lab at the University of Oregon.

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Technical commitments:

Simulator implementation: C++

Module implementation: C++, ...

Minimum Dependencies: Pin, gcc

Target compiler compatibility: GNU’s gcc, Apple’s Clang, Intel’s icc

Operating environment[s]: Linux, Mac OS