**VELLORE INSTITUTE OF TECHNOLOGY, CHENNAI**

**BECE407P – ASIC DESIGN**

**LAB-6**

# PRE AND POST SYNTHESIS FUNCTIONAL VERIFICATION OF 2x2 MULTIPLIER

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Date of Submission: 15-11-2024

## AIM:

To perform the pre-synthesis and post-synthesis functional verification of a 2x2 multiplier and the physical design.

## EDA TOOLS USED:

NCLaunch , Cadence® Genus and Cadence® Innovus.

## PROCEDURE:

### VERILOG CODE

```
`timescale 1ns / 1ns

module mul2b(input [1:0]a,b, input clk, output reg [3:0]p);

reg [1:0]a_reg, b_reg;
wire [3:0]m;
wire x1,x2,x3,x4;

always @(posedge clk)
begin
a_reg <= a;
b_reg <= b;
end

and a1(m[0],a_reg[0],b_reg[0]);
and a2(x1,a_reg[1],b_reg[0]);
and a3(x2,a_reg[0],b_reg[1]);
and a4(x3,a_reg[1],b_reg[1]);
half h1(x1,x2,m[1],x4);
half h2(x3,x4,m[2],m[3]);

always @(posedge clk)
p <= m;

endmodule
```

```
module half(
    input a,
    input b,
    output sum,
    output cy
    );

    assign sum=a^b;
    assign cy=a&b;



endmodule
```

**TCL**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib

set_attr  library slow.lib
read_hdl {mul2b.v half.v}

elaborate
read_sdc mul2b_constraints.g

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > mul2b_netlist.v
write_sdc > mul2b.sdc
gui_show



report_power > mul2b_power.rpt
report_area > mul2b_area.rpt
report_timing > mul21b_timing.rpt
```

**CONSTRAINTS**

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.1 [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "a"]  -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"]  -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "p"] -clock [get_clocks "clk"]
```

**NETLIST GENERATED**

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Nov 14 2024 14:42:05 IST (Nov 14 2024 09:12:05 UTC)

// Verification Directory fv/mul
`timescale 1ns / 1ns
module mul(a, b, clk, p);
  input [1:0] a, b;
  input clk;
  output [3:0] p;
  wire [1:0] a, b;
  wire clk;
  wire [3:0] p;
  wire [1:0] a_reg;
  wire [1:0] b_reg;
  wire UNCONNECTED, n_0, n_1, n_2, n_3, n_4, n_5;
  DFFQXL \p_reg[2] (.CK (clk), .D (n_4), .Q (p[2]));
  DFFQXL \p_reg[1] (.CK (clk), .D (n_5), .Q (p[1]));
  AOI21XL g98__2398(.A0 (n_2), .A1 (n_1), .B0 (n_3), .Y (n_5));
  NOR2XL g97__5107(.A (n_0), .B (n_3), .Y (n_4));
  DFFQXL \p_reg[3] (.CK (clk), .D (n_3), .Q (p[3]));
  NOR2XL g100__6260(.A (n_2), .B (n_1), .Y (n_3));
  DFFTRXL \p_reg[0] (.CK (clk), .D (a_reg[0]), .RN (b_reg[0]), .Q
       (p[0]), .QN (UNCONNECTED));
  NAND2XL g102__4319(.A (a_reg[1]), .B (b_reg[1]), .Y (n_0));
  NAND2XL g103__8428(.A (a_reg[0]), .B (b_reg[1]), .Y (n_2));
  NAND2XL g101__5526(.A (a_reg[1]), .B (b_reg[0]), .Y (n_1));
  DFFQX1 \b_reg_reg[0] (.CK (clk), .D (b[0]), .Q (b_reg[0]));
  DFFQX1 \a_reg_reg[0] (.CK (clk), .D (a[0]), .Q (a_reg[0]));
  DFFQX1 \a_reg_reg[1] (.CK (clk), .D (a[1]), .Q (a_reg[1]));
  DFFQX1 \b_reg_reg[1] (.CK (clk), .D (b[1]), .Q (b_reg[1]));
endmodule
```

**SDC**

```
# ####################################################################

#  Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Nov 14 15:56:41 IST 2024

# ####################################################################

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design mul

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[0]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[0]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {p[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {p[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {p[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {p[0]}]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

**INNOVUS.ENC**

```
####################################################################
#  Generated by:      Cadence Innovus 21.15-s110_1
#  OS:                Linux x86_64(Host ID cad15)
#  Generated on:      Thu Nov 14 16:37:00 2024
#  Design:            mul
#  Command:           saveDesign mul_innovus.enc
####################################################################
if {[is_common_ui_mode]} {
  read_db [file dirname [file normalize [info script]]]/mul_innovus.enc.dat
} else {
  restoreDesign [file dirname [file normalize [info script]]]/mul_innovus.enc.dat mul
}
```

**.SPEF**

```
*SPEF "IEEE 1481-1998"
*DESIGN "mul"
*DATE "Thu Nov 14 16:36:00 2024"
*VENDOR "Cadence Design Systems, Inc."
*PROGRAM "Innovus"
*VERSION "21.15-s110_1"
*DESIGN_FLOW "PIN_CAP NONE" "NAME_SCOPE LOCAL"
*DIVIDER /
*DELIMITER :
*BUS_DELIMITER []
*T_UNIT 1 NS
*C_UNIT 1 PF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

// MMMC spef file for corner 'default_rc_corner'

*NAME_MAP

*1 clk
*2 p[0]
*3 a_reg[1]
*4 a_reg[0]
*5 b_reg[1]
*6 b_reg[0]
*7 UNCONNECTED
*8 n_0
*9 n_1
*10 n_2
*11 n_3
*12 n_4
*13 n_5
*14 g98__2398
*15 g97__5107
*16 g100__6260
*17 p_reg\[0\]
*18 g102__4319
*19 g103__8428
*20 g101__5526


*PORTS

*1 I *C 14.85 0
*2 O *C 6.27 10.64


*D_NET *1 0.000631498

*CONN
*P *1 I *C 14.85 0 *L 0
*I *17:CK I *C 14.85 4.76 *L 0.00224 *D DFFTRXL

*CAP
1 *1 0.000315749
2 *1:1 0.000315749

*RES
1 *1:1 *17:CK 6.4
*END

*D_NET *2 0.000861133

*CONN
*I *17:Q O *C 6.27 7 *L 0 *D DFFTRXL
*P *2 O *C 6.27 10.64 *L 0

*CAP
1 *2:1 0.000430567
2 *2 0.000430567

*RES
1 *2:1 *2 1.04712
2 *17:Q *2:1 6.4
*END

*D_NET *3 0.00222021

*CONN
*I *20:A I *C 16.83 5.88 *L 0.0031 *D NAND2XL
*I *18:A I *C 25.41 5.88 *L 0.0031 *D NAND2XL

*CAP
1 *3:1 0.000191363
2 *3:2 0.000191363
3 *3:3 8.87374e-05
4 *3:4 0.00016403
5 *3:5 0.00047461
6 *3:6 0.00047461
7 *3:7 0.00016403
8 *3:8 8.87374e-05
9 *3:9 0.000191363
10 *3:10 0.000191363

*RES
1 *3:10 *18:A 6.4
2 *3:9 *3:10 0.465386
3 *3:8 *3:9 6.4
4 *3:7 *3:8 0.476149
5 *3:6 *3:7 0.404005
6 *3:5 *3:6 2.14267
7 *3:4 *3:5 0.404005
8 *3:3 *3:4 0.476149
9 *3:2 *3:3 6.4
10 *3:1 *3:2 0.465386
11 *20:A *3:1 6.4
*END

*D_NET *4 0.00201407

*CONN
*I *17:D I *C 13.53 5.88 *L 0.0028 *D DFFTRXL
*I *19:A I *C 27.39 5.88 *L 0.0031 *D NAND2XL

*CAP
1 *4:2 0.000443687
2 *4:3 0.000481333
3 *4:4 0.000436964
4 *4:5 0.000436964
*I *15:A I *C 23.43 5.88 *L 0.00317 *D NOR2XL
*I *18:Y O *C 24.75 6.44 *L 0 *D NAND2XL

*CAP
1 *8:1 4.5107e-05
2 *8:2 0.000121652
3 *8:3 0.000121652
4 *8:4 4.5107e-05

*RES
1 *8:4 *18:Y 6.4
2 *8:3 *8:4 0.109698
3 *8:2 *8:3 0.186154
4 *8:1 *8:2 0.109698
5 *15:A *8:1 6.4
*END

*D_NET *9 0.000586509

*CONN
*I *20:Y O *C 17.49 6.44 *L 0 *D NAND2XL
*I *16:B I *C 18.15 5.32 *L 0.00274 *D NOR2XL
*I *14:A1 I *C 20.13 5.88 *L 0.00314 *D AOI21XL

*CAP
1 *20:Y 4.43687e-05
2 *9:1 0.000119661
3 *9:2 9.0214e-05
4 *16:B 7.52923e-05
5 *9:4 0.000128487
6 *9:5 8.33796e-05
7 *9:6 4.5107e-05

*RES
1 *9:6 *14:A1 6.4
2 *9:5 *9:6 0.109698
3 *9:4 *9:5 0.0930771
4 *9:2 *9:4 0.219396
5 *9:1 *16:B 0.404005
6 *9:1 *9:2 6.4
7 *20:Y *9:1 0.238074
*END

*D_NET *10 0.00155043

*CONN
*I *14:A0 I *C 20.79 5.32 *L 0.00314 *D AOI21XL
*I *16:A I *C 18.81 5.88 *L 0.00317 *D NOR2XL
*I *19:Y O *C 28.05 6.44 *L 0 *D NAND2XL

*CAP
1 *10:0 0.000173594
2 *10:1 0.000135321
3 *10:2 3.82726e-05
4 *10:3 8.87374e-05
5 *10:6 0.000126384
6 *10:7 0.000348227
7 *10:8 0.000348227
8 *10:9 0.000126384
9 *10:10 8.87374e-05
```

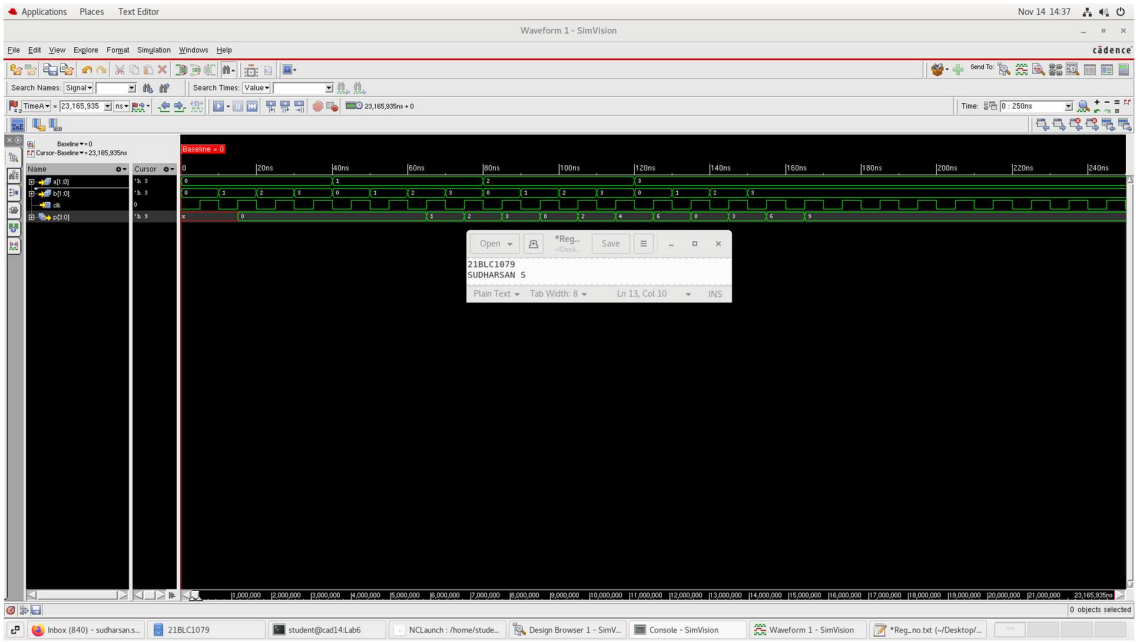
**CCOPT.SPEC**

```
#############################################################
#  Generated by:      Cadence Innovus 21.15-s110_1
#  OS:                Linux x86_64(Host ID cad15)
#  Generated on:      Thu Nov 14 16:32:20 2024
#  Design:            mul
#  Command:           create_ccopt_clock_tree_spec -file ccopt.spec
#############################################################
#-------------------------------------------------------------------------------
# Clock tree setup script - dialect: Innovus
#-------------------------------------------------------------------------------
#-------------------------------------------------------------------------------

if { [get_ccopt_clock_trees] != {} } {
  error {Cannot run clock tree spec: clock trees are already defined.}
}

namespace eval ::ccopt {}
namespace eval ::ccopt::ilm {}
set ::ccopt::ilm::ccoptSpecRestoreData {}
# Start by checking for unflattened ILMs.
# Will flatten if so and then check the db sync.
if { [catch {ccopt_check_and_flatten_ilms_no_restore}] } {
  return -code error
}
# cache the value of the restore command output by the ILM flattening code
set ::ccopt::ilm::ccoptSpecRestoreData $::ccopt::ilm::ccoptRestoreILMState

# The following pins are clock sources
set_ccopt_property cts_is_sdc_clock_root -pin clk true

# Clocks present at pin clk
#   clk (period 10.000ns) in timing_config constraints([mul_sdc.sdc])
create_ccopt_clock_tree -name clk -source clk -no_skew_group
set_ccopt_property target_max_trans_sdc -delay_corner max_delay -early -clock_tree clk 0.100
set_ccopt_property target_max_trans_sdc -delay_corner max_delay -late -clock_tree clk 0.100
# Clock period setting for source pin of clk
set_ccopt_property clock_period -pin clk 10

#############################################################################
##
## Timing connectivity based skew groups: off
##
#############################################################################
set_ccopt_property timing_connectivity_info {}

# Skew group to balance non generated clock:clk in timing_config:constraints (sdc mul_sdc.sdc)
create_ccopt_skew_group -name clk/constraints -sources clk -auto_sinks
set_ccopt_property include_source_latency -skew_group clk/constraints true
set_ccopt_property extracted_from_clock_name -skew_group clk/constraints clk
set_ccopt_property extracted_from_constraint_mode_name -skew_group clk/constraints constraints
set_ccopt_property extracted_from_delay_corners -skew_group clk/constraints {max_delay min_delay}


check_ccopt_clock_tree_convergence
# Restore the ILM status if possible
if { [get_ccopt_property auto_design_state_for_ilms] == 0 } {
  if {$::ccopt::ilm::ccoptSpecRestoreData != {} } {
    eval $::ccopt::ilm::ccoptSpecRestoreData
  }
```

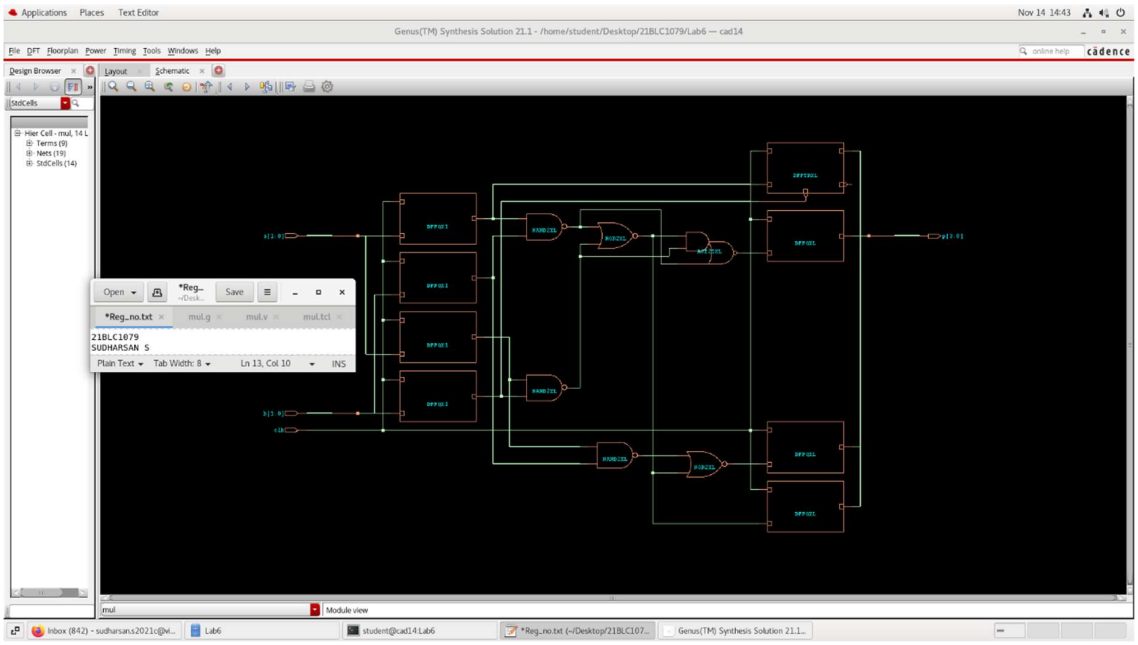
**STREAMOUT.map**

```
Metal1          NET             1               0
Metal1          SPNET           2               0
Metal1          PIN             3               0
Metal1          LEFPIN          4               0
Metal1          FILL            5               0
Metal1          FILLOPC         6               0
Metal1          VIA             7               0
Metal1          VIAFILL         8               0
Metal1          VIAFILLOPC              9               0
Metal1          LEFOBS          10              0
NAME            Metal1/NET              11              0
NAME            Metal1/SPNET            12              0
NAME            Metal1/PIN              13              0
NAME            Metal1/LEFPIN           14              0
Via12           PIN             15              0
Via12           LEFPIN          16              0
Via12           FILL            17              0
Via12           FILLOPC         18              0
Via12           VIA             19              0
Via12           VIAFILL         20              0
Via12           VIAFILLOPC              21              0
Metal2          NET             22              0
Metal2          SPNET           23              0
Metal2          PIN             24              0
Metal2          LEFPIN          25              0
Metal2          FILL            26              0
Metal2          FILLOPC         27              0
Metal2          VIA             28              0
Metal2          VIAFILL         29              0
Metal2          VIAFILLOPC              30              0
Metal2          LEFOBS          31              0
NAME            Metal2/NET              32              0
NAME            Metal2/SPNET            33              0
NAME            Metal2/PIN              34              0
NAME            Metal2/LEFPIN           35              0
Via23           PIN             36              0
Via23           LEFPIN          37              0
Via23           FILL            38              0
Via23           FILLOPC         39              0
Via23           VIA             40              0
Via23           VIAFILL         41              0
Via23           VIAFILLOPC              42              0
Metal3          NET             43              0
Metal3          SPNET           44              0
Metal3          PIN             45              0
Metal3          LEFPIN          46              0
Metal3          FILL            47              0
Metal3          FILLOPC         48              0
Metal3          VIA             49              0
Metal3          VIAFILL         50              0
Metal3          VIAFILLOPC              51              0
Metal3          LEFOBS          52              0
NAME            Metal3/NET              53              0
NAME            Metal3/SPNET            54              0
NAME            Metal3/PIN              55              0
NAME            Metal3/LEFPIN           56              0
Via34           PIN             57              0
Via34           LEFPIN          58              0
Via34           FILL            59              0
Via34           FILLOPC         60              0
Via34           VIA             61              0
Via34           VIAFILL         62              0
Via34           VIAFILLOPC              63              0
Metal4          NET             64              0
Metal4          SPNET           65              0
Metal4          PIN             66              0
Metal4          LEFPIN          67              0
Metal4          FILL            68              0
Metal4          FILLOPC         69              0
Metal4          VIA             70              0
Metal4          VIAFILL         71              0
Metal4          VIAFILLOPC              72              0
Metal4          LEFOBS          73              0
NAME            Metal4/NET              74              0
NAME            Metal4/SPNET            75              0
NAME            Metal4/PIN              76              0
NAME            Metal4/LEFPIN           77              0
Via45           PIN             78              0
Via45           LEFPIN          79              0
Via45           FILL            80              0
Via45           FILLOPC         81              0
Via45           VIA             82              0
Via45           VIAFILL         83              0
Via45           VIAFILLOPC              84              0
Metal5          NET             85              0
Metal5          SPNET           86              0
Metal5          PIN             87              0
Metal5          LEFPIN          88              0
```

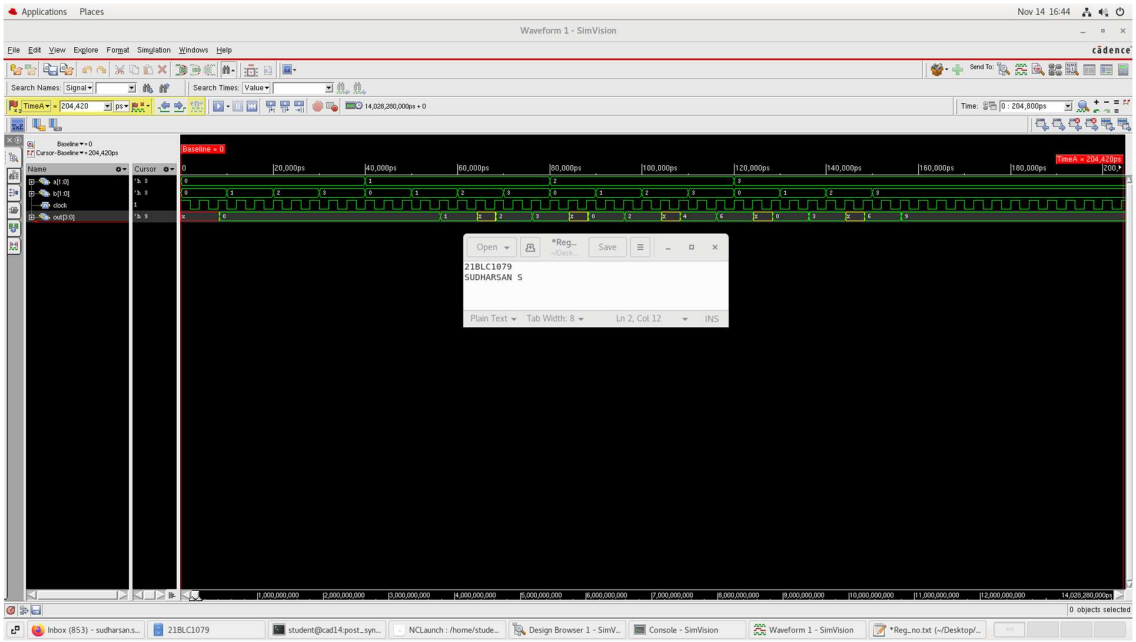
**PRE-SYNTHESIS FUCNTIONAL VERIFICATION:**




## GATE LEVEL NETLIST




## POST SYNTHESIS FUNCTIONAL VERIFICATION:




## PHYSICAL DESIGN