

VELLORE INSTITUTE OF TECHNOLOGY, CHENNAI

BECE407P – ASIC DESIGN

LAB-2

RUNNING THE BASIC SYNTHESIS FLOW USING CADENCE® GENUS

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Date of the Lab: 01-08-2024

AIM:

To run the basic synthesis flow for the following designs: 4-bit Up Counter, 1-bit Half Adder, Full Adder using Half Adder, SR flipflop and D flipflop.

EDA TOOLS USED:

Cadence® Genus: For RTL synthesis and design analysis.

DETAILED DESCRIPTION OF THE DESIGNS:

a) Method of Writing a Script File (.g) for Input Timing Constraints

A script file with a (.g) extension in Cadence is used to define timing constraints for digital circuits. These constraints ensure the circuit meets its required performance specifications. The file includes definitions for the clock period, duty cycle, rise and fall times, and jitter. Additionally, it specifies delays for the input and output ports.

b) Steps to Define Timing Constraints:

1. Clock Definition: Begin by defining the clock port. For example, you can use a line like `create_clock -name CLK -period 10 [get_ports clk]`.
2. Rise and Fall Times: Specify the rise and fall times for the clock signal.
3. Jitter Specification: Define the clock jitter, which measures timing uncertainty.
4. Port Delays: Set the delays for each input and output port, typically relative to the clock signal. This can be repeated for each port as necessary.

```
//21BLC1079
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
set_clock_transition -rise 0.1 [get_clocks "clock"]
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "c"] -clock [get_clocks "clock"]
```

c) Steps to Start Cadence® Genus

1. **Open Terminal:** Navigate to the synthesis directory and open the terminal.
2. **Setup Environment:** source /home/install/cshrc
This will load the necessary environment settings for Cadence tools.
3. **Launch Genus:** genus -legacy_ui
4. **To execute a specific script file :** genus -legacy_ui -f scriptfile.tcl
This will start Genus in legacy user interface mode.

```
[student@cad14 synthesis]$ csh
[student@cad14 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad14 synthesis]$ genus -legacy_ui -f half.tcl
```

d) Steps to Load Libraries, Designs, and Synthesize

```
2024/07/31 12:05:23 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/07/31 12:05:23 For more info, please run checkSysConf in <cdsRoot>/tools.lnx86/bin/checkSysConf <productid>
TMPDIR is being set to /tmp/genus_temp_15168_cad14_student_aAdvrT
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[12:05:24.339314] Configured Lic search path (21.01-s002): 5280@cadence:29000@172.16.77.98

Version: 21.14-s082.1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files half.tcl
Date:   Wed Jul 31 12:05:24 2024
Host:   cad14 (x86_64 w/Linux 4.18.0-477.10.1.e18_8.x86_64+debug) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (27774416KB)
PID:    15168
OS:     Red Hat Enterprise Linux release 8.8 (Ootpa)

[12:05:24.209792] Periodic Lic check successful
[12:05:24.209792] Feature usage summary:
[12:05:24.209793] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
***** Loading tool scripts...
***** Finished loading tool scripts (6 seconds elapsed).

#@ Processing -files option
@genus 1> source half.tcl
Setting attribute of root ''': 'init_lib_search_path' = /home/student/Desktop/21BLC1079/lib/
Setting attribute of root ''': 'init_hdl_search_path' = /home/student/Desktop/21BLC1079/rtl/

Threads Configured:3
Message Summary for Library slow_vdd1v0_basicCells.lib:
*****
```

1. Load Libraries:

Place the required .lib files in a designated folder.

Use the following commands to set the library search path and load the libraries:

```
set_attribute init_lib_search_path
/home/student/Desktop/21BLC1079/lib/
set_attribute library slow_vdd1v0_basicCells.lib
```

2. Load Designs:

Place the design files (e.g., .v files) in the appropriate folder.

Load the designs using:

```
set_attribute init_hdl_search_path  
/home/student/Desktop/21BLC1079/rtl/  
read_hdl top_files>.v
```

```
#@ Processing -files option  
@genus 1> source half.tcl  
Setting attribute of root '' : 'init_lib_search_path' = /home/student/Desktop/21BLC1079/lib/  
Setting attribute of root '' : 'init_hdl_search_path' = /home/student/Desktop/21BLC1079/rtl/  
  
Threads Configured:3  
  
Message Summary for Library slow_vdd1v0_basicCells.lib:  
*****  
  
Library has 324 basic logic and 128 basic sequential cells.  
Info : Elaborating Design. [ELAB-1]  
      : Elaborating top-level block 'half_adder' from file '/home/student/Desktop/21BLC1079/rtl/half_adder.v'.  
Info : Done Elaborating Design. [ELAB-3]  
      : Done elaborating 'half_adder'.  
Checking for analog nets...
```

3. Synthesis Process:

These are the following commands for synthesis:

```
elaborate  
read_sdc constraints.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt
```

```
Stage: post_elab  
-----  
| Trick | Accepts | Rejects | Runtime (ms) |  
-----  
| ume_constant_bmux | 0 | 0 | 0.00 |  
  
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: half_adder, recur: true)  
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)  
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: half.adder, recur: true)  
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)  
  
Stage: post_elab  
-----  
| Transform | Accepts | Rejects | Runtime (ms) |  
-----  
| hlo_clip_mux_input | 0 | 0 | 0.00 |  
| hlo_clip | 0 | 0 | 0.00 |  
  
Statistics for commands executed by read_sdc:  
"create_clock" - successful 1 , failed 0 (runtime 0.00)  
"get_clocks" - successful 6 , failed 0 (runtime 0.00)  
"get_ports" - successful 6 , failed 0 (runtime 0.00)  
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)  
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)  
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)  
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)  
read_sdc completed in 00:00:00 (hh:mm:ss)  
  Setting attribute of root '' : 'syn_generic_effort' = medium  
  
Stage: pre_early_cg  
-----  
| Transform | Accepts | Rejects | Runtime (ms) |  
-----  
  
##Generic Timing Info for library domain: _default_ typical gate delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF  
Starting mux data reorder optimization [v1.0] (stage: pre to gen setup, startdef: half adder, recur: true)
```

```

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |
Info : Deleting instances not driving any primary outputs. [GLO-34]
: Deleting 4 sequential instances.
: Optimizations such as constant propagation or redundancy removal could change the connections so a hierarchical instance does not drive any primary outputs anymore. To see the list of deleted hierarchical instances, set the 'information_level' attribute to 2 or above. If the message is truncated set the message attribute 'truncate' to false to see the complete list. To prevent this message from appearing, set 'delete_unloaded_insts' root/subdesign attribute to 'false' or 'preserve' instance attribute to 'true'.
Info : Deleting instances not driving any primary outputs. [GLO-34]
Info : Deleting 4 hierarchical instances.
Info : Synthesizing. [SYNTH-1]
: Synthesizing 'half_adder' to generic gates using 'medium' effort.
PBS_Generic_Start - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_Generic_Start' being created for table 'pbs_debug'
Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0 ) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic_Start
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: ('N' indicates data that was populated from previously saved time_info database
Info: CPU time includes time spent in parallel regions and threads
TNS Restructuring Config: no_value at stage: generic applied.
Info : Partition Based Synthesis execution skipped. [PHYS-752]
: Design size is less than the partition size '100000' for distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |
Starting mux data reorder optimization [v1.0] (stage: post_to_gen_setup, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |

```

```

Stage: pre_rtlopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_infer_macro | 0 | 2 | 0.00 |
| hlo_decode_mux_sandwich | 0 | 0 | 0.00 |
| hlo_mux_decode | 0 | 0 | 0.00 |
| hlo_chop_mux | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_constant_mux_opt | 0 | 0 | 0.00 |
| hlo_inequality_transform | 0 | 0 | 0.00 |
| hlo_reconv_opt | 0 | 0 | 0.00 |
| hlo_restructure | 0 | 0 | 0.00 |
| hlo_common_select_muxopto | 0 | 0 | 0.00 |
| hlo_identity_transform | 0 | 0 | 0.00 |
| hlo_reduce_operator_chain | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_optimize_datapath | 0 | 0 | 0.00 |
| hlo_datapath_recast | 0 | 0 | 0.00 |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |

Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_hlo_rtlopt
| Trick | Accepts | Rejects | Runtime (ms) |
| ume_runtime | 0 | 0 | 0.00 |

Number of big hc bmuxes before = 0
Info : Pre-processed datapath logic. [DPOPT-6]
: No pre-processing optimizations applied to datapath logic in 'half_adder'.
Info : Skipping datapath optimization. [DPOPT-5]
: There is no datapath logic in 'half_adder'.
Number of big hc bmuxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef: half_adder, recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_rtlopt

```

```

Stage: post_rtlopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_logic_reduction | 0 | 0 | 0.00 |
| hlo_mux_reorder | 0 | 0 | 0.00 |

Starting mux speculation [v1.0] (stage: post_muxopt, startdef: half_adder, recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.001s)

Stage: post_muxopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_speculation | 0 | 0 | 1.00 |

=====
Stage : to_generic
=====
Message Summary
=====
Message Text
=====

| Id | Sev | Count | Message Text
|-----+-----+-----+-----|
| CDFG-372 | Info | 4 | Bitwidth mismatch in assignment.
|           |     |     | |Review and make sure the mismatch is unintentional. Genus can possibly issue bitwidth mismatch warning for explicit assignments present in RTL as-well-as for
implicit assignments |     |     | inferred by the tool. For example, in case of enum declaration without value, the tool will implicitly assign value to the enum variables. It also issues the
warning for any   |     |     | bitwidth mismatch that appears in this implicit assignment.
| DPOPT-5 | Info | 1 | Skipping datapath optimization.
| DPOPT-6 | Info | 1 | Pre-processed datapath logic.
| ELAB-1  | Info | 1 | Elaborating Design.
| ELAB-2  | Info | 2 | Elaborating Subdesign.

```

Category	Flops	Percentage
Total instances	4	100.0
Excluded from State Retention	4	100.0
- Will not convert	4	100.0
- Preserved	0	0.0
- Power intent excluded	4	100.0
- Could not convert	0	0.0
- Scan type	0	0.0
- No suitable cell	0	0.0
State Retention instances	0	0.0

PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 0.9976039999999999
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.0(100.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt-Post

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.0(100.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt-Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic-Postgen HBO Optimizations

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Generic-Logical) =====
##>===== Cadence Confidential (Generic-Logical) =====
##>Main Thread Summary:
##>-----
##>
##>STEP Elapsed WNS TNS Insts Area Memory
##>-----
##>G:Initial 0 - - 10 64 465
##>G:Setup 0 - - - - -
##>G:Launch ST 0 - - - - -
##>G:Design Partition 0 - - - - -
##>G>Create Partition Netlists 0 - - - - -
##>G:Init Power 0 - - - - -
##>G:Budgeting 0 - - - - -
##>G:Derenv-DB 0 - - - - -
##>G:Debug Outputs 0 - - - - -
##>G:ST loading 0 - - - - -
##>G:Distributed 0 - - - - -
##>G:Timer 0 - - - - -
##>G:Assembly 0 - - - - -
##>G:DFT 0 - - - - -
##>G:Const Prop 0 - - 8 48 465

```

Info   : Mapping. [SYNTH-4]
      : Mapping 'half_adder' using 'medium' effort.
Mapper: Libraries have:
      domain _default_: 324 combo usable cells and 128 sequential usable cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.0(100.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
-----+-----+-----+-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Premap HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Premap' HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.0(100.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Info   : Partition Based Synthesis execution skipped. [PHYS-752]
      : Design size is less than the partition size '100000' for distributed mapping optimization to kick in.
Mapper: Libraries have:
      domain _default_: 324 combo usable cells and 128 sequential usable cells
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)
=====
Stage : first_condense
=====
Message Summary
=====
| Id    | Sev  | Count |           Message Text           |
| PHYS-752 | Info |    1 | Partition Based Synthesis execution skipped. |
| SYNTH-2  | Info |    1 | Done synthesizing.                |
| SYNTH-4  | Info |    1 | Mapping.                         |
=====

Global mapping target info

```

```

Target path end-point (Port: half_adder/sum)
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)
Multi-threaded Technology Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping status
=====
          Group
          Tot Wrst
Operation   Total Weighted
global_map    Area Slacks
              26     0

Cost Group      Target  Slack  Diff. Constr.
-----
clock           270    8772   10000

Global incremental target info
=====
Cost Group 'clock' target slack: 180 ps
Target path end-point (Port: half_adder/sum)

Global incremental optimization status
=====
          Group
          Tot Wrst
Operation   Total Weighted
global_incr  Area Slacks
              26     0

Cost Group      Target  Slack  Diff. Constr.
-----
clock           180    8772   10000

State Retention Synthesis Status
=====
Category          Flops Percentage
-----
Total instances      4      100.0
Excluded from State Retention      4      100.0
  - Will not convert      4      100.0
  - Preserved      0      0.0
  - Power intent excluded      4      100.0
  - Could not convert      0      0.0
  - Scan type      0      0.0
  - No suitable cell      0      0.0
State Retention instances      0      0.0
-----

INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed_Time 0, CPU_Time -0.002332000000000007
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
  00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start

```

```

00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | -0.2( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Techmap-Global Mapping
00:00:04(00:00:07) | 00:00:00(00:00:01) | 0.0( 50.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Datapath Postmap Operations
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time -3.79999999998249e-5
stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | -0.2( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Techmap-Global Mapping
00:00:04(00:00:07) | 00:00:00(00:00:01) | 0.0( 50.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Datapath Postmap Operations
00:00:04(00:00:07) | -01:59:57(00:00:00) | -0.0( 0.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Postmap HBO Optimizations
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Doing ConstProp on /designs/half_adder ...
Time taken by ConstProp Step: 00:00:00
PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations

```

00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.2(50.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt_Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Postgen HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Start
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	-0.2(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Techmap_Global Mapping
00:00:04(00:00:07)	00:00:00(00:00:01)	0.0(50.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Datapath Postmap Operations
00:00:04(00:00:07)	-01:59:57(00:00:00)	-0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap HBO Optimizations
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Clock Gating
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Cleanup
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)					
Info: ("N") indicates data that was populated from previously saved time_info database					
Info: CPU time includes time of parent + longest thread					
PBS_Techmap_Post_MBCI - Elapsed_Time 0, CPU_Time 0.0					
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'					
Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.2(50.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt_Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Postgen HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Start
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	-0.2(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Techmap_Global Mapping
00:00:04(00:00:07)	00:00:00(00:00:01)	0.0(50.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Datapath Postmap Operations
00:00:04(00:00:07)	-01:59:57(00:00:00)	-0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap HBO Optimizations
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Clock Gating
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Cleanup
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_Techmap-Post_MBCI
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)					
Info: ("N") indicates data that was populated from previously saved time_info database					
Info: CPU time includes time of parent + longest thread					
#>===== Cadence Confidential (Mapping-Logical) =====					
#>Main Thread Summary:					
#>	##STEP	Elapsed	WNS	TNS	Insts Area Memory
#>	#>M:Initial	0	-	-	8 48 465
#>M:Pre Cleanup	0	-	-	8	48 465

```

##>STEP           Elapsed    WNS      TNS   Insts     Area   Memory
##>-----
##>M:Initial          0       -       -      8     48     465
##>M:Pre Cleanup       0       -       -      8     48     465
##>M:Setup             0       -       -      -      -      -
##>M:Launch ST          0       -       -      -      -      -
##>M:Design Partition    0       -       -      -      -      -
##>M>Create Partition Netlists 0       -       -      -      -      -
##>M:Init Power          0       -       -      -      -      -
##>M:Budgeting           0       -       -      -      -      -
##>M:Derenv-DB           0       -       -      -      -      -
##>M:Debug Outputs        0       -       -      -      -      -
##>M:ST loading           0       -       -      -      -      -
##>M:Distributed          0       -       -      -      -      -
##>M:Timer               0       -       -      -      -      -
##>M:Assembly             0       -       -      -      -      -
##>M:DFT                 0       -       -      -      -      -
##>M:DP Operations         1       -       -      5     25     465
##>M:Const Prop            0     8772      0      5     25     465
##>M:Cleanup              0     8772      0      5     25     465
##>M:MBCI                 0       -       -      5     25     465
##>M:Const Gate Removal    0       -       -      -      -      -
##>M:Misc                  0
##>-----
##>Total Elapsed          1
##>=====
Info  : Done mapping. [SYNTH-5]
      : Done mapping 'half_adder'.
Setting attribute of root '/': 'syn_opt_effort' = medium
Info  : Incrementally optimizing. [SYNTH-7]
      : Incrementally optimizing 'half_adder' using 'medium' effort.

Incremental optimization status
=====
                                         Group
                                         Tot Wrst  Total - - DRC Totals - -
                                         Total Weighted    Neg   Max   Max
Operation      Area   Slacks   Slack  Trans  Cap
init_iopt      26      0       0       0       0
-----
const_prop     26      0       0       0       0

Incremental optimization status
=====
                                         Group
                                         Tot Wrst  Total - - DRC Totals - -
                                         Total Weighted    Neg   Max   Max
Operation      Area   Slacks   Slack  Trans  Cap
init_delay     26      0       0       0       0

Trick      Calls   Accepts  Attempts  Time(secs)
-----
crit_upsz    0 (     0 /     0 )  0.00
plc_bal_star 0 (     0 /     0 )  0.00
drc_buftimb  0 (     0 /     0 )  0.00
plc_st        0 (     0 /     0 )  0.00
plc_st_fence  0 (     0 /     0 )  0.00
plc_star      0 (     0 /     0 )  0.00
plc_laf_st    0 (     0 /     0 )  0.00
plc_laf_st_fence 0 (     0 /     0 )  0.00

```

<u>crit_upsz</u>	0 (0 /	0)	0.00
<u>plc_bal_star</u>	0 (0 /	0)	0.00
<u>drc_buftimb</u>	0 (0 /	0)	0.00
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_st_fence</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>plc_laf_st</u>	0 (0 /	0)	0.00
<u>plc_laf_st_fence</u>	0 (0 /	0)	0.00
<u>drc_buftims</u>	0 (0 /	0)	0.00
<u>plc_laf_lo_st</u>	0 (0 /	0)	0.00
<u>plc_lo_st</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00
<u>setup_dn</u>	0 (0 /	0)	0.00
<u>buf2inv</u>	0 (0 /	0)	0.00
<u>mb_split</u>	0 (0 /	0)	0.00
<u>exp</u>	0 (0 /	0)	0.00
<u>gate_deco</u>	0 (0 /	0)	0.00
<u>gcomp_tim</u>	0 (0 /	0)	0.00
<u>inv_pair_2_buf</u>	0 (0 /	0)	0.00
 <u>init_drc</u>	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>simole_buf</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_buf_so</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>simole_buf</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_buf_so</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 <u>init_tns</u>	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_bal_star</u>	0 (0 /	0)	0.00
<u>drc_buftimb</u>	0 (0 /	0)	0.00
<u>drc_buftims</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
<u>plc_laf_lo_st</u>	0 (0 /	0)	0.00
<u>plc_lo_st</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00

```

crit_upsz      0 (    0 /    0 ) 0.00
plc_bal_star   0 (    0 /    0 ) 0.00
drc_buftimb   0 (    0 /    0 ) 0.00
    plc_st     0 (    0 /    0 ) 0.00
plc_st_fence   0 (    0 /    0 ) 0.00
    plc_star    0 (    0 /    0 ) 0.00
    plc_laf_st   0 (    0 /    0 ) 0.00
plc_laf_st_fence 0 (    0 /    0 ) 0.00
    drc_buftimes 0 (    0 /    0 ) 0.00
plc_laf_lo_st  0 (    0 /    0 ) 0.00
    plc_lo_st    0 (    0 /    0 ) 0.00
        fopt      0 (    0 /    0 ) 0.00
crit_dnsz     0 (    0 /    0 ) 0.00
    dup         0 (    0 /    0 ) 0.00
        fopt      0 (    0 /    0 ) 0.00
setup_dn       0 (    0 /    0 ) 0.00
    buf2inv     0 (    0 /    0 ) 0.00
    mb_split     0 (    0 /    0 ) 0.00
        exp         0 (    0 /    0 ) 0.00
gate_deco     0 (    0 /    0 ) 0.00
gcomp_tim      0 (    0 /    0 ) 0.00
inv_pair_2_buf 0 (    0 /    0 ) 0.00

init_drc          26    0    0    0    0

    Trick   Calls   Accepts  Attempts  Time(secs)
-----
    plc_st     0 (    0 /    0 ) 0.00
    plc_star   0 (    0 /    0 ) 0.00
    drc_bufs   0 (    0 /    0 ) 0.00
    drc_fopt   0 (    0 /    0 ) 0.00
    drc_bufb   0 (    0 /    0 ) 0.00
    simole_buf 0 (    0 /    0 ) 0.00
    dup         0 (    0 /    0 ) 0.00
crit_dnsz     0 (    0 /    0 ) 0.00
crit_upsz      0 (    0 /    0 ) 0.00

    Trick   Calls   Accepts  Attempts  Time(secs)
-----
    plc_st     0 (    0 /    0 ) 0.00
    plc_star   0 (    0 /    0 ) 0.00
    drc_bufs   0 (    0 /    0 ) 0.00
    drc_fopt   0 (    0 /    0 ) 0.00
    drc_bufb   0 (    0 /    0 ) 0.00
    simole_buf 0 (    0 /    0 ) 0.00
    dup         0 (    0 /    0 ) 0.00
crit_dnsz     0 (    0 /    0 ) 0.00
crit_upsz      0 (    0 /    0 ) 0.00

    Trick   Calls   Accepts  Attempts  Time(secs)
-----
    plc_st     0 (    0 /    0 ) 0.00
    plc_star   0 (    0 /    0 ) 0.00
    drc_bufs   0 (    0 /    0 ) 0.00
    drc_fopt   0 (    0 /    0 ) 0.00
    drc_bufb   0 (    0 /    0 ) 0.00
    dup         0 (    0 /    0 ) 0.00
crit_dnsz     0 (    0 /    0 ) 0.00
crit_upsz      0 (    0 /    0 ) 0.00

init_area          26    0    0    0    0

    Trick   Calls   Accepts  Attempts  Time(secs)
-----
    undup      0 (    0 /    0 ) 0.00
    rem_buf    0 (    0 /    0 ) 0.00
    rem_inv    0 (    0 /    0 ) 0.00
    merge.bi   0 (    0 /    0 ) 0.00
    rem_inv_gb 0 (    0 /    0 ) 0.00
    io_phase   0 (    0 /    0 ) 0.00
    gate_como  0 (    0 /    0 ) 0.00
    gcomp_mog  0 (    0 /    0 ) 0.00
    glob_area  2 (    0 /    2 ) 0.00

```

4. To view the GUI:

```
gui_show
```

syn_generic_effort: Controls the optimization level during RTL and datapath transformations into a gate-level netlist. Higher effort results in better quality netlists but takes more time.

syn_map_effort: Manages the mapping of generic gates to specific technology library components, optimizing for the best implementation.

syn_opt_effort: Further optimizes the logic design, applying techniques like Boolean simplification, technology mapping, restructuring, retiming, and clock gating.

e) Cadence® Genus Legacy Terminal After Synthesis

The following commands are to generate and read synthesis ,

1. Generate Reports:

```
report_timing > filename.rep
```

```
=====
Generated by:      Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:     Jul 31 2024 12:05:33 pm
Module:          half_adder
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode:    enclosed
Area mode:       timing library
=====

      Pin           Type      Fanout Load Slew Delay Arrival
                           (fF)   (ps)  (ps)  (ps)
-----+-----+-----+-----+-----+-----+-----+-----+
(clock clock)          launch            000    +0      0 R
df3_uut_Q_reg/CK        DFFQXL      1  0.0   13  +228   228 F
df3_uut_Q_reg/Q          <<< interconnect 13    +0      228 F
sum                   out port          +0      228 F
(half_adder_top.g_line_7) ext delay        +1000  1228 F
-----+-----+-----+-----+-----+-----+-----+-----+
(clock clock)          capture          10000 R
-----+-----+-----+-----+-----+-----+-----+-----+
Cost Group  : 'clock' (path_group 'clock')
Timing slack : 8772ps
Start-point : df3_uut_Q_reg/CK
End-point   : sum
```

```
report_area > filename.rep
```

```

=====
Generated by:          Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:          Jul 31 2024 12:05:33 pm
Module:                half_adder
Technology library:   slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode:         enclosed
Area mode:             timing library
=====

Instance  Module  Cell Count  Cell Area  Net Area  Total Area  Wireload
-----
half_adder      5        25.650    0.000     25.650 <none> (D)
| (D) = wireload is default in technology library

```

report_power > filename.rep

Power Report for /half_adder					
Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	4.07667e-10	7.90551e-07	1.29600e-08	8.03918e-07	88.11%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	9.66040e-11	3.99862e-08	3.64500e-09	4.37278e-08	4.79%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	6.48000e-08	6.48000e-08	7.10%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	5.04271e-10	8.30537e-07	8.14050e-08	9.12446e-07	100.00%
Percentage	0.06%	91.02%	8.92%	100.00%	100.00%

2. **Read Reports:** Review the generated reports to analyze timing, area, and power metrics.

f) Writing the Output Files

The primary output of the synthesis process is the gate-level netlist, which is saved as a .v file. Additionally, a timing constraint file with the .sdc extension is also generated.

1. **Generate Netlist:**

write_hdl filename.v

2. **Generate Timing Constraints:**

write_sdc filename.sdc

HALFADDER:

```

// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Jul 31 2024 12:05:33 IST (Jul 31 2024 06:35:33 UTC)

// Verification Directory fv/half_adder

module half_adder(a, b, c, sum, clock);
    input a, b, clock;
    output c, sum;
    wire a, b, clock;
    wire c, sum;
    wire d1, d3, n_0, n_1;
    DFFQXL df4_uut_Q_reg(.CK (clock), .D (n_0), .Q (c));
    DFFQXL df3_uut_Q_reg(.CK (clock), .D (n_1), .Q (sum));
    ADDHX1 g43_2398(.A (d1), .B (d3), .CO (n_0), .S (n_1));
    DFFHQX1 df2_uut_Q_reg(.CK (clock), .D (b), .Q (d3));
    DFFHQX1 df1_uut_Q_reg(.CK (clock), .D (a), .Q (d1));
endmodule

```

FULL ADDER:

```

// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Jul 31 2024 13:21:02 IST (Jul 31 2024 07:51:02 UTC)

// Verification Directory fv/full_adder

module full_adder(a, b, cin, clock, sum, carry_out);
    input a, b, cin, clock;
    output sum, carry_out;
    wire a, b, cin, clock;
    wire sum, carry_out;
    wire c1, c2, ha1_d1, ha1_d3, ha2_d1, ha2_d3, n_0, n_1;
    wire n_2, n_3, s1;
    OR2XL g63_2398(.A (c2), .B (c1), .Y (carry_out));
    DFFQXL ha2_df4_uut_Q_reg(.CK (clock), .D (n_2), .Q (c2));
    DFFQXL ha2_df3_uut_Q_reg(.CK (clock), .D (n_3), .Q (sum));
    ADDHX1 g66_5107(.A (ha2_d3), .B (ha2_d1), .CO (n_2), .S (n_3));
    DFFQXL ha2_df1_uut_Q_reg(.CK (clock), .D (s1), .Q (ha2_d1));
    DFFQXL ha1_df4_uut_Q_reg(.CK (clock), .D (n_0), .Q (c1));
    DFFHQX1 ha1_df3_uut_Q_reg(.CK (clock), .D (n_1), .Q (s1));
    ADDHX1 g70_6260(.A (ha1_d1), .B (ha1_d3), .CO (n_0), .S (n_1));
    DFFHQX1 ha1_df2_uut_Q_reg(.CK (clock), .D (b), .Q (ha1_d3));
    DFFHQX1 ha2_df2_uut_Q_reg(.CK (clock), .D (cin), .Q (ha2_d3));
    DFFHQX1 ha1_df1_uut_Q_reg(.CK (clock), .D (a), .Q (ha1_d1));
endmodule

```

SR_Flip_Flop:

```
|  
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1  
// Generated on: Jul 31 2024 12:23:49 IST (Jul 31 2024 06:53:49 UTC)  
  
// Verification Directory fv/sr_flip_flop  
  
module sr_flip_flop(S, R, clk, Q, Qn);  
    input S, R, clk;  
    output Q, Qn;  
    wire S, R, clk;  
    wire Q, Qn;  
    wire n_0, n_1, n_2;  
    DFFQXL Q_reg(.CK (clk), .D (n_2), .Q (Q));  
    DFFQXL Qn_reg(.CK (clk), .D (n_1), .Q (Qn));  
    NAND2BXL g122_2398(.AN (S), .B (n_0), .Y (n_2));  
    AOI2BB1XL g123_5107(.A0N (R), .A1N (Qn), .B0 (S), .Y (n_1));  
    NAND2BX1 g124_6260(.AN (R), .B (Q), .Y (n_0));  
endmodule
```

D_FLIP_FLOP:

```
|  
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1  
// Generated on: Jul 31 2024 12:36:11 IST (Jul 31 2024 07:06:11 UTC)  
  
// Verification Directory fv/d_flip_flop  
  
module d_flip_flop(D, Q, Qn, clk);  
    input D, clk;  
    output Q, Qn;  
    wire D, clk;  
    wire Q, Qn;  
    wire n_0;  
    DFFQXL uut_Qn_reg(.CK (clk), .D (n_0), .Q (Qn));  
    DFFQXL uut_Q_reg(.CK (clk), .D (D), .Q (Q));  
    INVX1 g24(.A (D), .Y (n_0));  
endmodule
```

COUNTER

```

// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Jul 31 2024 12:45:29 IST (Jul 31 2024 07:15:29 UTC)

// Verification Directory fv/counter

module counter(clk, reset, count);
    input clk, reset;
    output [3:0] count;
    wire clk, reset;
    wire [3:0] count;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8;
    DFFQXL \count_reg[3] (.CK (clk), .D (n_8), .Q (count[3]));
    NOR2X1 g81_2398(.A (reset), .B (n_7), .Y (n_8));
    DFFQXL \count_reg[2] (.CK (clk), .D (n_6), .Q (count[2]));
    DFFHQX1 \count_reg[1] (.CK (clk), .D (n_4), .Q (count[1]));
    XNOR2X1 g83_5107(.A (count[3]), .B (n_5), .Y (n_7));
    AOI211XL g84_6260(.A0 (n_1), .A1 (n_2), .B0 (reset), .C0 (n_5), .Y
        (n_6));
    NOR2X1 g87_4319(.A (reset), .B (n_3), .Y (n_4));
    OAI21X1 g89_8428(.A0 (count[0]), .A1 (count[1]), .B0 (n_2), .Y
        (n_3));
    NOR2X1 g86_5526(.A (n_1), .B (n_2), .Y (n_5));
    DFFHQX1 \count_reg[0] (.CK (clk), .D (n_0), .Q (count[0]));
    NOR2X1 g90_6783(.A (reset), .B (count[0]), .Y (n_0));
    NAND2X1 g91_3680(.A (count[1]), .B (count[0]), .Y (n_2));
    INVX1 g92(.A (count[2]), .Y (n_1));
endmodule

```

g) Method of Writing a Script File (.tcl) for Synthesis

TCL script files automate the synthesis process, enabling consistent and efficient design flows.

1. Set Library and HDL Paths:

```

set_attribute init_lib_search_path
/home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path
/home/student/Desktop/21BLC1079/lib/

```

2. Load Library and Design:

```

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl design-file>.v

```

3. Synthesize the Design:

```

elaborate
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt

```

4. Generate Reports and Output Files:

```

report_timing > filename.rep
report_area > filename.rep

```

```
report_power > filename.rep  
write_hdl filename.v  
write_sdc filename.sdc
```

HALFADDER:

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
  
read_hdl {half_adder.v d_flip_flop.v sr_flip_flop.v}  
elaborate  
  
read_sdc half_adder_top.g  
  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
  
gui_show  
  
write_hdl > halfgate.v  
write_sdc > halvesdc.sdc  
  
report_timing > halftime.rep  
report_area > halfarea.rep  
report_power > halfpower.rep
```

FULLADDER:

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
  
read_hdl {full_adder.v half_adder.v d_flip_flop.v sr_flip_flop.v}  
elaborate  
  
read_sdc fulladder.g  
  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
  
gui_show  
  
write_hdl > fulladder_gate.v  
write_sdc > fulladder_sdc.sdc  
  
report_timing > fulladder_time.rep  
report_area > fulladder_area.rep  
report_power > fulladder_power.rep
```

SR_FLIP_FLOP:

```
|set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
|set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
|set_attribute library slow_vdd1v0_basicCells.lib

read_hdl {sr_flip_flop.v}
elaborate

read_sdc srff.g

set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt

gui_show

write_hdl > srff_gate.v
write_sdc > srff_sdc.sdc

report_timing > srff_time.rep
report_area > srff_area.rep
report_power > srff_power.rep
```

D_FLIP_FLOP:

```
|set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
|set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
|set_attribute library slow_vdd1v0_basicCells.lib

read_hdl {d_flip_flop.v sr_flip_flop.v}
elaborate

read_sdc dff.g

set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt

gui_show

write_hdl > dff_gate.v
write_sdc > dff_sdc.sdc

report_timing > dff_time.rep
report_area > dff_area.rep
report_power > dff_power.rep
```

COUNTER:

```

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib

read_hdl {counter.v}
elaborate

read_sdc counter_top.g

set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt

gui_show

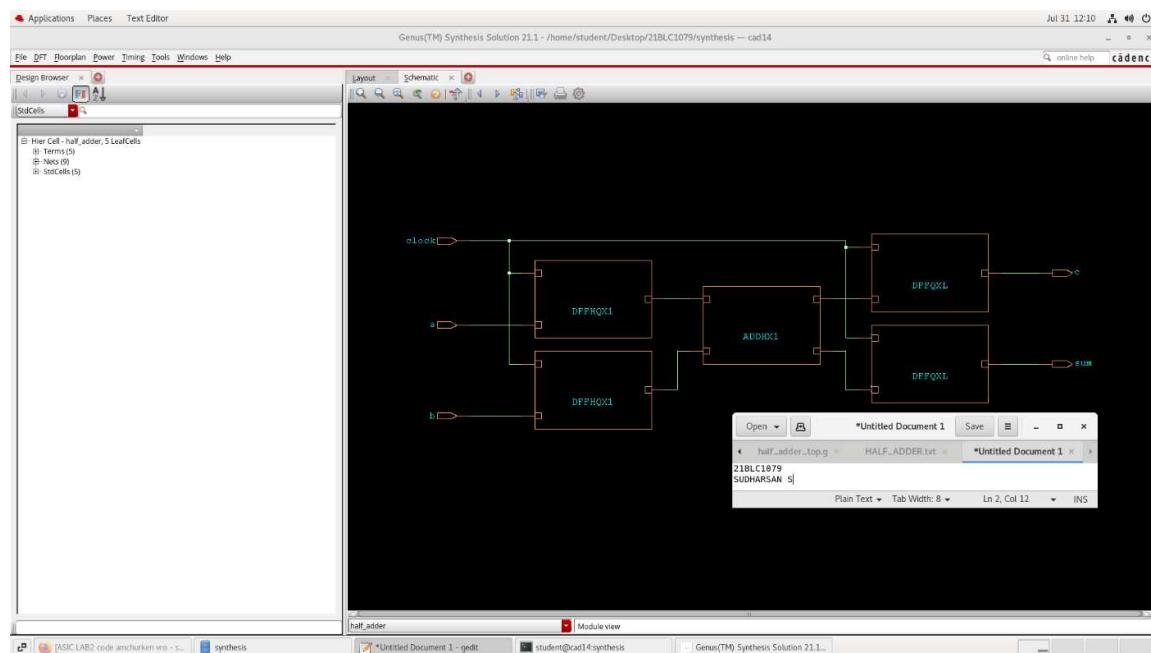
write_hdl > counter_gate.v
write_sdc > counter_sdc.sdc

report_timing > counter_time.rep
report_area > counter_area.rep
report_power > counter_power.rep

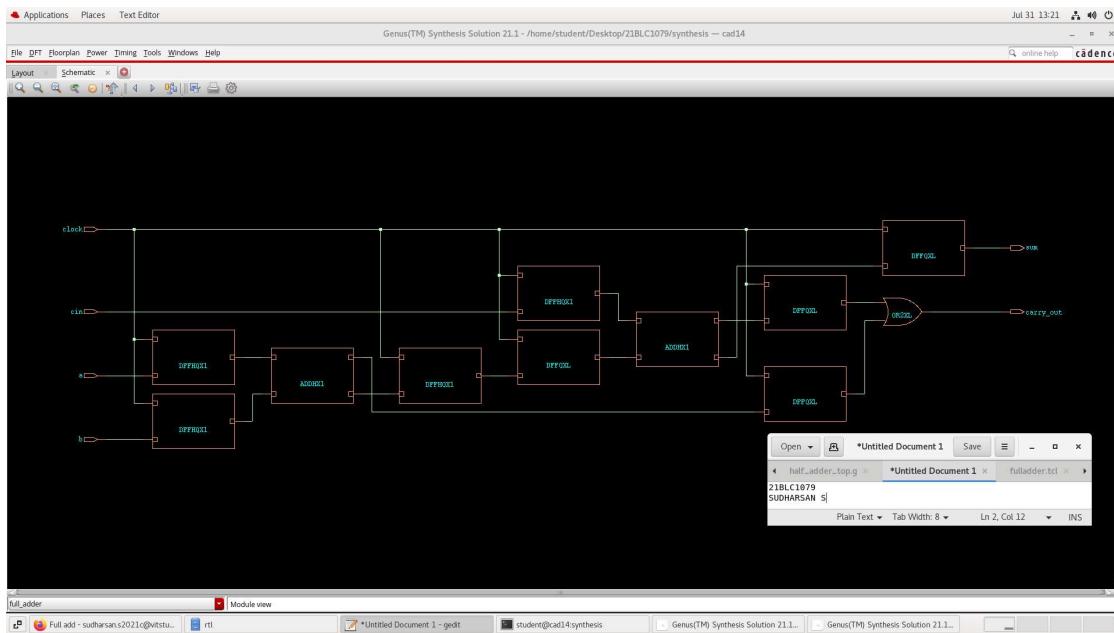
```

SCHEMATIC:

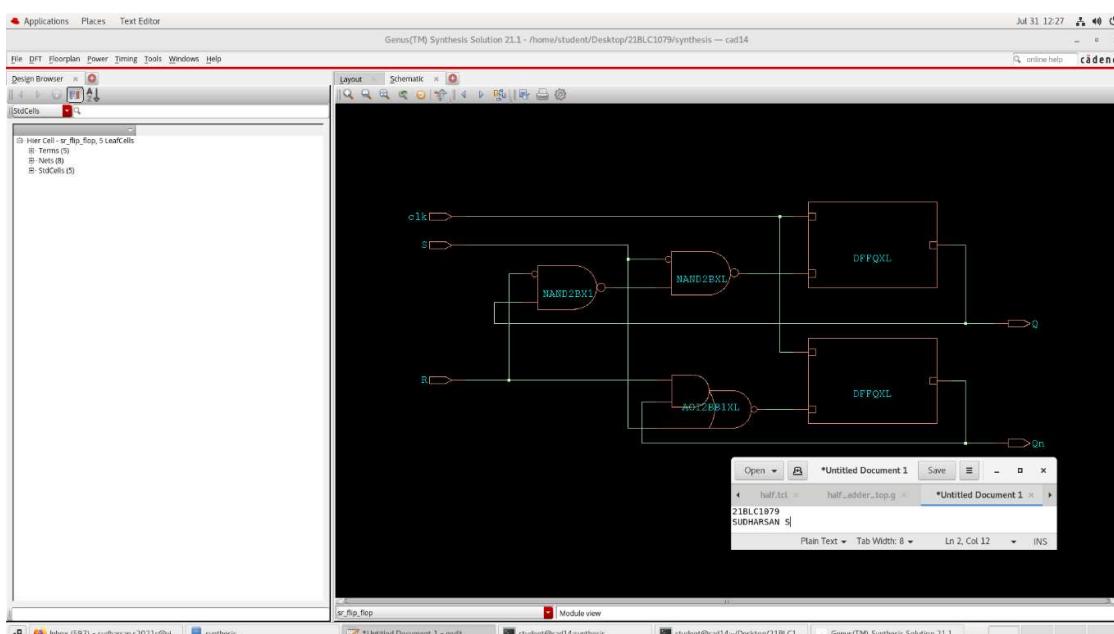
HALFADDER:



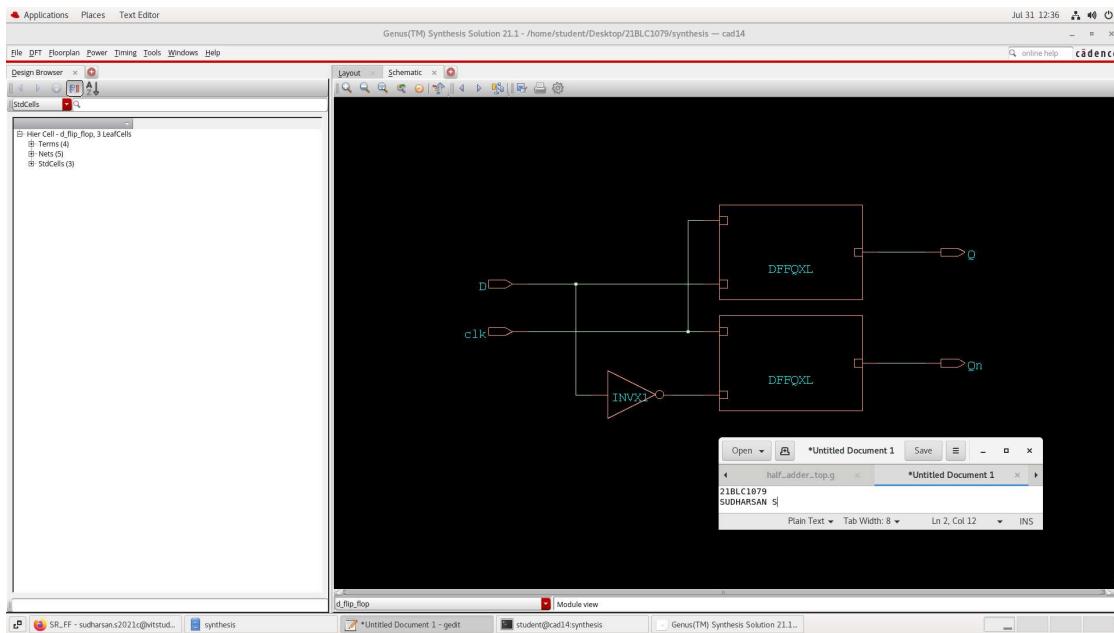
FULL ADDER:



SR_FLIP_FLOP:



D_FLIP_FLOP:



COUNTER:



INFERENCE:

This lab report explains how to use Cadence® Genus for synthesizing digital circuits. It covers setting up timing constraints, loading necessary libraries and designs, and automating the synthesis process with scripts. The report also highlights how to optimize the design by adjusting effort settings.