

VELLORE INSTITUTE OF TECHNOLOGY, CHENNAI

BECE407P – ASIC DESIGN

LAB-3

DESIGN AND SIMULATION OF CIRCUITS USING CADENCE NCLaunch AND RUNNING THE BASIC SYNTHESIS FLOW USING CADENCE® GENUS

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Date of the Lab: 05-09-2024

AIM:

To do functional verification and synthesis for the following designs.

EDA TOOLS USED:

Cadence® Genus: For RTL synthesis and design analysis.

DETAILED DESCRIPTION OF THE DESIGNS:

a) Method of Writing a Script File (.g) for Input Timing Constraints

A script file with a (.g) extension in Cadence is used to define timing constraints for digital circuits. These constraints ensure the circuit meets its required performance specifications. The file includes definitions for the clock period, duty cycle, rise and fall times, and jitter. Additionally, it specifies delays for the input and output ports.

b) Steps to Define Timing Constraints:

1. Clock Definition: Begin by defining the clock port. For example, you can use a line like `create_clock -name CLK -period 10 [get_ports clk]`.
2. Rise and Fall Times: Specify the rise and fall times for the clock signal.
3. Jitter Specification: Define the clock jitter, which measures timing uncertainty.
4. Port Delays: Set the delays for each input and output port, typically relative to the clock signal. This can be repeated for each port as necessary.

```
//21BLC1079
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
set_clock_transition -rise 0.1 [get_clocks "clock"]
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "c"] -clock [get_clocks "clock"]
```

c) Steps to Start Cadence® Genus

1. **Open Terminal:** Navigate to the synthesis directory and open the terminal.
2. **Setup Environment:** source /home/install/cshrc
This will load the necessary environment settings for Cadence tools.
3. **Launch Genus:** genus -legacy_ui
4. **To execute a specific script file :** genus -legacy_ui -f scriptfile.tcl
This will start Genus in legacy user interface mode.

```
[student@cad14 synthesis]$ csh
[student@cad14 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad14 synthesis]$ genus -legacy_ui -f half.tcl
2024/07/31 12:05:23 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/07/31 12:05:23 For more info, please run checkSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus_temp_15168_cad14_student_advrT
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[12:05:24.339314] Configured Lic search path (21.01-s002): 5280@cadence:29000@172.16.77.98

Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files half.tcl
Date:   Wed Jul 31 12:05:24 2024
Host:   cad14 (x86_64 w/Linux 4.18.0-477.10.1.el8_8.x86_64+debug) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (27774416KB)
PID:    15168
OS:     Red Hat Enterprise Linux release 8.8 (Ootpa)

[12:05:24.209792] Periodic Lic check successful
[12:05:24.209792] Feature usage summary:
[12:05:24.209793] Genus Synthesis
Checking out license: Genus_Synthesis

*****
```

```
Loading tool scripts...
Finished loading tool scripts (6 seconds elapsed).

#@ Processing -files option
@genus 1> source half.tcl
  Setting attribute of root '//': 'init_lib_search_path' = /home/student/Desktop/21BLC1079/lib/
  Setting attribute of root '//': 'init_hdl_search_path' = /home/student/Desktop/21BLC1079/rtl/
Threads Configured:3
Message Summary for Library slow_vdd1v0_basicCells.lib:
*****
```

1. Load Libraries:

Place the required .lib files in a designated folder.

Use the following commands to set the library search path and load the libraries:

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute library slow_vdd1v0_basicCells.lib
```

2. Load Designs:

Place the design files (e.g., .v files) in the appropriate folder.

Load the designs using:

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
read_hdl top_files>.v
```

```
#@ Processing -files option
@genus 1> source half.tcl
Setting attribute of root ''': 'init_lib_search_path' = /home/student/Desktop/21BLC1079/lib/
Setting attribute of root ''': 'init_hdl_search_path' = /home/student/Desktop/21BLC1079/rtl/

Threads Configured:3

Message Summary for Library slow_ydd1v0_basicCells.lib:
*****
Library has 924 double logic and 120 double sequential lib cells.

Info   : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'half_adder' from file '/home/student/Desktop/21BLC1079/rtl/half_adder.v'.
Info   : Done Elaborating Design. [ELAB-3]
        : Done elaborating 'half_adder'.
Checking for analog nets...
```

3. Synthesis Process:

These are the following commands for synthesis:

```
elaborate
read_sdc constraints.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
```

```
Stage: post_elab
| Trick      | Accepts | Rejects | Runtime (ms) |
| ume_constant_bmux |    0 |     0 |      0.00 |

Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: half_adder, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: half_adder, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
-----
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_clip_mux_input |    0 |     0 |      0.00 |
| hlo_clip |    0 |     0 |      0.00 |

Statistics for commands executed by read_sdc:
"create_clock"          - successful    1 , failed      0 (runtime  0.00)
"get_clocks"            - successful    6 , failed      0 (runtime  0.00)
"get_ports"              - successful    6 , failed      0 (runtime  0.00)
"set_clock_transition"  - successful    2 , failed      0 (runtime  0.00)
"set_clock_uncertainty" - successful    1 , failed      0 (runtime  0.00)
"set_input_delay"       - successful    2 , failed      0 (runtime  0.00)
"set_output_delay"      - successful    2 , failed      0 (runtime  0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root ''': 'syn_generic_effort' = medium

Stage: pre_early_cg
-----
| Transform | Accepts | Rejects | Runtime (ms) |

##Generic Timing Info for library domain: _default_ typical gate delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre to gen setup, startdef: half adder, recur: true)
```

```

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |
Info : Deleting instances not driving any primary outputs. [GLO-34]
: Deleting 4 sequential instances.
: Optimizations such as constant propagation or redundancy removal could change the connections so a hierarchical instance does not drive any primary outputs anymore. To see the list of deleted hierarchical instances, set the 'information_level' attribute to 2 or above. If the message is truncated set the message attribute 'truncate' to false to see the complete list. To prevent this optimization from deleting unloaded Insts' root/subdesign attribute to 'false' or 'preserve' instance attribute to 'true'.
Info : Deleting instances not driving any primary outputs. [GLO-34]
Info : Deleting 4 hierarchical instances.
Info : Synthesizing. [SYNTH-1]
: Synthesizing 'half_adder' to generic gates using 'medium' effort.
PBS_Generic_Start - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_Generic_Start' being created for table 'pbs_debug'
Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0 ) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic_Start
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: ('N' indicates data that was populated from previously saved time_info database
Info: CPU time includes time spent in parallel regions and threads
TNS Restructuring Config: no_value at stage: generic applied.
Info : Partition Based Synthesis execution skipped. [PHYS-752]
: Design size is less than the partition size '100000' for distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |
Starting mux data reorder optimization [v1.0] (stage: post_to_gen_setup, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |

```

```

Stage: pre_rtlopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_infer_macro | 0 | 2 | 0.00 |
| hlo_decode_mux_sandwich | 0 | 0 | 0.00 |
| hlo_mux_decode | 0 | 0 | 0.00 |
| hlo_chop_mux | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_constant_mux_opt | 0 | 0 | 0.00 |
| hlo_inequality_transform | 0 | 0 | 0.00 |
| hlo_reconv_opt | 0 | 0 | 0.00 |
| hlo_restructure | 0 | 0 | 0.00 |
| hlo_common_select_muxopto | 0 | 0 | 0.00 |
| hlo_identity_transform | 0 | 0 | 0.00 |
| hlo_reduce_operator_chain | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_optimize_datapath | 0 | 0 | 0.00 |
| hlo_datapath_recast | 0 | 0 | 0.00 |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |

Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_hlo_rtlopt
| Trick | Accepts | Rejects | Runtime (ms) |
| ume_runtime | 0 | 0 | 0.00 |

Number of big hc bmuxes before = 0
Info : Pre-processed datapath logic. [DPOPT-6]
: No pre-processing optimizations applied to datapath logic in 'half_adder'.
Info : Skipping datapath optimization. [DPOPT-5]
: There is no datapath logic in 'half_adder'.
Number of big hc bmuxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef: half_adder, recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_rtlopt

```

```

Stage: post_rtlopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_logic_reduction | 0 | 0 | 0.00 |
| hlo_mux_reorder | 0 | 0 | 0.00 |

Starting mux speculation [v1.0] (stage: post_muxopt, startdef: half_adder, recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.001s)

Stage: post_muxopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_speculation | 0 | 0 | 1.00 |

=====
Stage : to_generic
=====
Message Summary
=====
Message Text
=====

| Id | Sev | Count | Message Text
|-----+-----+-----+-----|
| CDFG-372 | Info | 4 | Bitwidth mismatch in assignment.
|           |     |     | |Review and make sure the mismatch is unintentional. Genus can possibly issue bitwidth mismatch warning for explicit assignments present in RTL as-well-as for
implicit assignments |     |     | inferred by the tool. For example, in case of enum declaration without value, the tool will implicitly assign value to the enum variables. It also issues the
warning for any   |     |     | bitwidth mismatch that appears in this implicit assignment.
| DPOPT-5 | Info | 1 | Skipping datapath optimization.
| DPOPT-6 | Info | 1 | Pre-processed datapath logic.
| ELAB-1  | Info | 1 | Elaborating Design.
| ELAB-2  | Info | 2 | Elaborating Subdesign.

```

Category	Flops	Percentage
Total instances	4	100.0
Excluded from State Retention	4	100.0
- Will not convert	4	100.0
- Preserved	0	0.0
- Power intent excluded	4	100.0
- Could not convert	0	0.0
- Scan type	0	0.0
- No suitable cell	0	0.0
State Retention instances	0	0.0

PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 0.9976039999999999
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.0(100.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt-Post

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.0(100.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt-Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic-Postgen HBO Optimizations

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Generic-Logical) =====
##>===== Cadence Confidential (Generic-Logical) =====
##>Main Thread Summary:
##>-----
##>
##>STEP Elapsed WNS TNS Insts Area Memory
##>-----
##>G:Initial 0 - - 10 64 465
##>G:Setup 0 - - - - -
##>G:Launch ST 0 - - - - -
##>G:Design Partition 0 - - - - -
##>G>Create Partition Netlists 0 - - - - -
##>G:Init Power 0 - - - - -
##>G:Budgeting 0 - - - - -
##>G:Derenv-DB 0 - - - - -
##>G:Debug Outputs 0 - - - - -
##>G:ST loading 0 - - - - -
##>G:Distributed 0 - - - - -
##>G:Timer 0 - - - - -
##>G:Assembly 0 - - - - -
##>G:DFT 0 - - - - -
##>G:Const Prop 0 - - 8 48 465

```

Info : Mapping. [SYNTH-4]
: Mapping 'half_adder' using 'medium' effort.
Mapper: Libraries have:
domain _default : 324 combo usable cells and 128 sequential usable cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.0(100.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
+-----+-----+-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: ("N") indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Premap HBO Optimizations - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_TechMap-Premap HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.0(100.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
+-----+-----+-----+-----+-----+
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
+-----+-----+-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: ("N") indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Info : Partition Based Synthesis execution skipped. [PHYS-752]
: Design size is less than the partition size '100000' for distributed mapping optimization to kick in.
Mapper: Libraries have:
domain _default : 324 combo usable cells and 128 sequential usable cells
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)
Stage : first_condense
=====
Message Summary
=====
| Id | Sev | Count | Message Text |
|-----+-----+-----+-----|
| PHYS-752 | Info | 1 | Partition Based Synthesis execution skipped. |
| SYNTH-2 | Info | 1 | Done synthesizing. |
| SYNTH-4 | Info | 1 | Mapping. |
=====

Global mapping target info

```

```

Target path end-point (Port: half_adder/sum)
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)
Multi-threaded Technology Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping status
=====
          Group
          Tot Wrst
Operation    Total  Weighted
global_map     Area   Slacks
                26      0

Cost Group      Target  Slack  Diff. Constr.
-----
clock           270    8772   10000

Global incremental target info
=====
Cost Group 'clock' target slack: 180 ps
Target path end-point (Port: half_adder/sum)

Global incremental optimization status
=====
          Group
          Tot Wrst
Operation    Total  Weighted
global_incr   Area   Slacks
                26      0

Cost Group      Target  Slack  Diff. Constr.
-----
clock           180    8772   10000

State Retention Synthesis Status
=====
Category        Flops Percentage
-----
Total instances      4      100.0
Excluded from State Retention      4      100.0
  - Will not convert      4      100.0
  - Preserved      0      0.0
  - Power intent excluded      4      100.0
  - Could not convert      0      0.0
  - Scan type      0      0.0
  - No suitable cell      0      0.0
State Retention instances      0      0.0
-----

INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed_Time 0, CPU_Time -0.002332000000000007
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
  00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start

```

```

00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | -0.2( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Techmap-Global Mapping
00:00:04(00:00:07) | 00:00:00(00:00:01) | 0.0( 50.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Datapath Postmap Operations
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time -3.79999999998249e-5
stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | -0.2( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Techmap-Global Mapping
00:00:04(00:00:07) | 00:00:00(00:00:01) | 0.0( 50.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Datapath Postmap Operations
00:00:04(00:00:07) | -01:59:57(00:00:00) | -0.0( 0.0) | 12:05:33 (Jul31) | 465.5 MB | PBS_TechMap-Postmap HBO Optimizations
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Doing ConstProp on /designs/half_adder ...
Time taken by ConstProp Step: 00:00:00
PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:31 (Jul31) | 465.5 MB | PBS_Generic-Start
00:00:04(00:00:06) | 00:00:00(00:00:01) | 100.2( 50.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic_Opt-Post
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Start
00:00:04(00:00:06) | 00:00:00(00:00:00) | 0.0( 0.0) | 12:05:32 (Jul31) | 465.5 MB | PBS_TechMap-Premap HBO Optimizations

```

00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.2(50.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt_Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Postgen HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Start
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	-0.2(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Techmap_Global Mapping
00:00:04(00:00:07)	00:00:00(00:00:01)	0.0(50.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Datapath Postmap Operations
00:00:04(00:00:07)	-01:59:57(00:00:00)	-0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap HBO Optimizations
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Clock Gating
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Cleanup
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)					
Info: ("N") indicates data that was populated from previously saved time_info database					
Info: CPU time includes time of parent + longest thread					
PBS_Techmap_Post_MBCI - Elapsed_Time 0, CPU_Time 0.0					
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'					
Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:04(00:00:05)	00:00:00(00:00:00)	0.0(0.0)	12:05:31 (Jul31)	465.5 MB	PBS_Generic_Start
00:00:04(00:00:06)	00:00:00(00:00:01)	100.2(50.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Opt_Post
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Generic_Postgen HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Start
00:00:04(00:00:06)	00:00:00(00:00:00)	0.0(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:06)	00:00:00(00:00:00)	-0.2(0.0)	12:05:32 (Jul31)	465.5 MB	PBS_Techmap_Global Mapping
00:00:04(00:00:07)	00:00:00(00:00:01)	0.0(50.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Datapath Postmap Operations
00:00:04(00:00:07)	-01:59:57(00:00:00)	-0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap HBO Optimizations
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Clock Gating
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_TechMap_Postmap Cleanup
00:00:04(00:00:07)	00:00:00(00:00:00)	0.0(0.0)	12:05:33 (Jul31)	465.5 MB	PBS_Techmap-Post_MBCI
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)					
Info: ("N") indicates data that was populated from previously saved time_info database					
Info: CPU time includes time of parent + longest thread					
#>===== Cadence Confidential (Mapping-Logical) =====					
#>Main Thread Summary:					
#>	##STEP	Elapsed	WNS	TNS	Insts Area Memory
#>	#>M:Initial	0	-	-	8 48 465
#>M:Pre Cleanup	0	-	-	8	48 465

```

##>STEP          Elapsed    WNS      TNS   Insts     Area   Memory
##>-----
##>M:Initial          0       -       -      8     48     465
##>M:Pre Cleanup       0       -       -      8     48     465
##>M:Setup             0       -       -      -      -      -
##>M:Launch ST          0       -       -      -      -      -
##>M:Design Partition    0       -       -      -      -      -
##>M>Create Partition Netlists 0       -       -      -      -      -
##>M:Init Power          0       -       -      -      -      -
##>M:Budgeting           0       -       -      -      -      -
##>M:Derenv-DB           0       -       -      -      -      -
##>M:Debug Outputs        0       -       -      -      -      -
##>M:ST loading           0       -       -      -      -      -
##>M:Distributed          0       -       -      -      -      -
##>M:Timer               0       -       -      -      -      -
##>M:Assembly             0       -       -      -      -      -
##>M:DFT                 0       -       -      -      -      -
##>M:DP Operations         1       -       -      5     25     465
##>M:Const Prop            0     8772      0      5     25     465
##>M:Cleanup              0     8772      0      5     25     465
##>M:MBCI                 0       -       -      5     25     465
##>M:Const Gate Removal    0       -       -      -      -      -
##>M:Misc                  0
##>-----
##>Total Elapsed          1
##>=====
Info  : Done mapping. [SYNTH-5]
      : Done mapping 'half_adder'.
Setting attribute of root '/': 'syn_opt_effort' = medium
Info  : Incrementally optimizing. [SYNTH-7]
      : Incrementally optimizing 'half_adder' using 'medium' effort.

Incremental optimization status
=====
                                         Group
                                         Tot Wrst  Total - - DRC Totals - -
                                         Total Weighted    Neg   Max   Max
Operation      Area   Slacks   Slack  Trans  Cap
init_iopt      26      0       0       0       0
-----
const_prop     26      0       0       0       0

Incremental optimization status
=====
                                         Group
                                         Tot Wrst  Total - - DRC Totals - -
                                         Total Weighted    Neg   Max   Max
Operation      Area   Slacks   Slack  Trans  Cap
init_delay     26      0       0       0       0

Trick   Calls   Accepts  Attempts  Time(secs)
-----
crit_upsz      0 (     0 /     0 )  0.00
plc_bal_star   0 (     0 /     0 )  0.00
drc_buftimb   0 (     0 /     0 )  0.00
plc_st         0 (     0 /     0 )  0.00
plc_st_fence   0 (     0 /     0 )  0.00
plc_star       0 (     0 /     0 )  0.00
plc_laf_st     0 (     0 /     0 )  0.00
plc_laf_st_fence 0 (     0 /     0 )  0.00

```

<u>crit_upsz</u>	0 (0 /	0)	0.00
<u>plc_bal_star</u>	0 (0 /	0)	0.00
<u>drc_buftimb</u>	0 (0 /	0)	0.00
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_st_fence</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>plc_laf_st</u>	0 (0 /	0)	0.00
<u>plc_laf_st_fence</u>	0 (0 /	0)	0.00
<u>drc_buftims</u>	0 (0 /	0)	0.00
<u>plc_laf_lo_st</u>	0 (0 /	0)	0.00
<u>plc_lo_st</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00
<u>setup_dn</u>	0 (0 /	0)	0.00
<u>buf2inv</u>	0 (0 /	0)	0.00
<u>mb_split</u>	0 (0 /	0)	0.00
<u>exp</u>	0 (0 /	0)	0.00
<u>gate_deco</u>	0 (0 /	0)	0.00
<u>gcomp_tim</u>	0 (0 /	0)	0.00
<u>inv_pair_2_buf</u>	0 (0 /	0)	0.00
 <u>init_drc</u>	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>simole_buf</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_buf_so</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>simole_buf</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_st</u>	0 (0 /	0)	0.00
<u>plc_star</u>	0 (0 /	0)	0.00
<u>drc_buf_so</u>	0 (0 /	0)	0.00
<u>drc_bufs</u>	0 (0 /	0)	0.00
<u>drc_fopt</u>	0 (0 /	0)	0.00
<u>drc_bufb</u>	0 (0 /	0)	0.00
<u>dup</u>	0 (0 /	0)	0.00
<u>crit_dnsz</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
 <u>init_tns</u>	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)
<u>plc_bal_star</u>	0 (0 /	0)	0.00
<u>drc_buftimb</u>	0 (0 /	0)	0.00
<u>drc_buftims</u>	0 (0 /	0)	0.00
<u>crit_upsz</u>	0 (0 /	0)	0.00
<u>plc_laf_lo_st</u>	0 (0 /	0)	0.00
<u>plc_lo_st</u>	0 (0 /	0)	0.00
<u>fopt</u>	0 (0 /	0)	0.00

crit_upsz	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
plc_st	0 (0 /	0)	0.00
plc_st_fence	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
plc_laf_st	0 (0 /	0)	0.00
plc_laf_st_fence	0 (0 /	0)	0.00
drc_buftimes	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
 init_drc	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time(secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 init_area	26	0	0	0
 Trick	Calls	Accepts	Attempts	Time(secs)

undup	0 (0 /	0)	0.00
rem_buf	0 (0 /	0)	0.00
rem_inv	0 (0 /	0)	0.00
merge.bi	0 (0 /	0)	0.00
rem_inv_gb	0 (0 /	0)	0.00
io_phase	0 (0 /	0)	0.00
gate_como	0 (0 /	0)	0.00
gcomp_mog	0 (0 /	0)	0.00
glob_area	2 (0 /	2)	0.00

4. To view the GUI:

```
gui_show
```

syn_generic_effort: Controls the optimization level during RTL and datapath transformations into a gate-level netlist. Higher effort results in better quality netlists but takes more time.

syn_map_effort: Manages the mapping of generic gates to specific technology library components, optimizing for the best implementation.

syn_opt_effort: Further optimizes the logic design, applying techniques like Boolean simplification, technology mapping, restructuring, retiming, and clock gating.

e) Cadence® Genus Legacy Terminal After Synthesis

The following commands are to generate and read synthesis ,

1. Generate Reports:

```
report_timing > filename.rep
```

```
=====
Generated by:      Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:     Jul 31 2024 12:05:33 pm
Module:          half_adder
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode:    enclosed
Area mode:        timing library
=====

      Pin           Type      Fanout Load Slew Delay Arrival
                           (fF)   (ps)  (ps)  (ps)
-----
(clock clock)          launch
df3_uut_Q_reg/CK          DFFQXL      1  0.0   13  +228   228 F
df3_uut_Q_reg/Q          <<< interconnect
sum                      out port
(half_adder_top.g_line_7) ext delay
                           capture
Cost Group  : 'clock' (path_group 'clock')
Timing slack :  8772ps
Start-point : df3_uut_Q_reg/CK
End-point   : sum
```

```
report_area > filename.rep
```

```

=====
Generated by:          Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:          Jul 31 2024 12:05:33 pm
Module:                half_adder
Technology library:   slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode:         enclosed
Area mode:             timing library
=====

Instance  Module  Cell Count  Cell Area  Net Area  Total Area  Wireload
-----
half_adder      5        25.650    0.000     25.650 <none> (D)
| (D) = wireload is default in technology library

```

report_power > filename.rep

```

Instance: /half_adder
Power Unit: W
PDB Frames: /stim#0/frame#0

Category      Leakage      Internal      Switching      Total      Row%
-----
memory        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
register     4.07667e-10  7.90551e-07  1.29600e-08  8.03918e-07  88.11%
latch         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
logic         9.66040e-11  3.99862e-08  3.64500e-09  4.37278e-08  4.79%
bbox           0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
clock          0.00000e+00  0.00000e+00  6.48000e-08  6.48000e-08  7.10%
pad            0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
pm             0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%

Subtotal      5.04271e-10  8.30537e-07  8.14050e-08  9.12446e-07  100.00%
Percentage    0.06%       91.02%       8.92%       100.00%  100.00%
-----
```

2. **Read Reports:** Review the generated reports to analyze timing, area, and power metrics.

f) Writing the Output Files

The primary output of the synthesis process is the gate-level netlist, which is saved as a .v file. Additionally, a timing constraint file with the .sdc extension is also generated.

1. **Generate Netlist:**

write_hdl filename.v

2. **Generate Timing Constraints:**

write_sdc filename.sdc

1) Verilog Code:**• Half Adder**

```
module halfadder(a,b,c,sum);
    input a,b;
    output reg c, sum;
    always@(*)
        begin
            sum = a^b;
            c = a&b;
        end
    endmodule
```

• Full Adder

```
module fulladder(a,b,cin,cout,sum);
    input a , b , cin;
    output reg cout,sum;
    always@*
        begin
            {cout,sum} = a+b+cin;
        end
    endmodule
```

• Half subtractor

```
module halfsubtractor(a,b,diff,borrow);
    input a,b;
    output reg diff,borrow;
    always@*
        {borrow,diff} = a-b;
    endmodule
```

• Full subtractor

```
module fullsubtractor(a,b,c,diff,borrow);
    input a,b,c;
```

```

output reg diff,borrow;

always@*
{borrow,diff} = c-a-b;

endmodule

```

- **4 bit full adder**

```

module fourbit_full_adder(input [3:0]a,b,input c,
output [3:0]sum,
output carry);
assign {carry,sum}=a+b+c;
endmodule

```

- **4 bit full subtractor**

```

module four_bit_subractor(input [3:0]a,b,
input c,output [3:0]difference,output borrow};
assign {difference,borrow}=a-b-c;
endmodule

```

- **4 bit adder and subtractor**

```

module fourbitaddersubtractor(a,b,o,add);
input [3:0] a , b;
output reg [4:0] o;
input add
always@*
begin
if(add ==1'b1) o = a+b;
else o = a-b;
end
endmodule

```

- **Subtraction using 2s complement addition**

```

module subr_using2s_complement(input [3:0]a,b,
output [3:0]difference,output borrow);
wire [3:0] b1;
wire carry_out;

```

```
assign b1 = (~b) + 1;
assign {carry_out, difference} = a + b1;
assign borrow = ~carry_out;
endmodule
```

- **4 bit adder and subtractor**

```
module fourbitaddersubtractor(a,b,o,add);
input [3:0] a , b;
output reg [4:0] o;
input add;
always@*
begin
if(add ==1'b1) o = a+b;
else o = a-b;
end
endmodule
```

- **Parity detector**

```
module paritydetector(a,b,p,o);
input a,b,p;
output o;
assign o = ~(a^b^p);
endmodule
```

- **Binary to gray code converter**

```
module binarytogramay(bin,gray);
input [2:0] bin;
output [2:0] gray;
assign gray[2] = bin[2];
assign gray[1] = bin[2]^bin[1];
assign gray[0] = bin[1]^bin[0];
endmodule
```

- **Gray to binary converter**

```
module graytobinary(bin,gray);
    output [2:0] bin;
    input [2:0] gray;
    assign bin[2] = gray[2];
    assign bin[1] = gray[2]^gray[1];
    assign bin[0] = gray[1]^gray[0];
endmodule
```

- **2:1 Mux**

```
module twomux(a,b,sel,out);
    input a , b, sel;
    output out;
    assign out = (sel)? b:a;
endmodule
```

- **2:1 Mux using if else**

```
module twomuxifelse(a,b,sel,out);
    input a,b,sel;
    output reg out;
    always@*
        begin
            if(sel == 1'b1) out = b;
            else out = a;
        end
endmodule
```

- **2:1 Mux using case**

```
module twomuxcase(a,b,sel,out);
    input a,b,sel;
    output reg out;
    always@*
        begin
            case(sel)
                1'b0: out = a;
```

```
1'b1: out = b;  
default: out = 1'bx;  
endcase  
end  
endmodule
```

- **4:1 Mux**

```
module fourmux(a,b,c,d,s1,s0,out);  
input a , b,c,d,s0,s1;  
output out;  
assign out = s1&s0&d | s1&(~s0)&c | (~s1)&s0&b | (~s1)&(~s0)&a;  
endmodule
```

- **4:1 Mux if else**

```
module fourmuxcase(a,b,c,d,s1,s0,out);  
input a,b,c,d,s0,s1;  
output reg out;  
always@*  
begin  
case({s1,s0})  
2'b11: out = d;  
2'b11: out = c;  
2'b11: out = b;  
2'b11: out = a;  
default: out = 1'bx;  
endcase  
end  
endmodule
```

- **4:1 Mux using case**

```
module fourmuxcase(a,b,c,d,s1,s0,out);

input a,b,c,d,s0,s1;
output reg out;
always@*
begin
  case({s1,s0})
    2'b11: out = d;
    2'b11: out = c;
    2'b11: out = b;
    2'b11: out = a;
    default: out = 1'bx;
  endcase
end
endmodule
```

- **4:1 Mux using 2:1 Mux**

```
module fourmuxtwomux(a,b,c,d,s1,s0,out);

input a,b,c,d,s1,s0;
wire w1,w2;
output out;
twomux t1(a,c,s1,w1);
twomux t2(b,d,s1,w2);
twomux t3(w1,w2,s0,out);
endmodule
```

- **Addition and subtraction using if else**

```
module addsubifelse(a,b,o1,o2,control);
input a,b,control;
output reg o1,o2;
always@*
begin
if(control == 1'b1)
begin
o2 = a&b;
o1 = a^b;
end
else if(control == 1'b0)
begin
o2 = ~a&b;
o1 = a^b;
end
end
endmodule
```

- **3:8 Decoder**

```
module threetoeightdecoder(a,b);
input [2:0] a;
output [7:0] b;
assign b[7] = a[2]&a[1]&a[0];
assign b[6] = a[2]&a[1]&(~a[0]);
assign b[5] = a[2]&(~a[1])&a[0];
assign b[4] = a[2]&(~a[1])&(~a[0]);
assign b[3] = (~a[2])&a[1]&a[0];
assign b[2] = (~a[2])&a[1]&(~a[0]);
assign b[1] = (~a[2])&(~a[1])&a[0];
assign b[0] = (~a[2])&(~a[1])&(~a[0]);
endmodule
```

- **1:2 Decoder using case**

```
module onetotwodecoder(a,b);
```

```
input a;
output reg [1:0]b;
always@*
begin
case(a)
1'b0: b = 2'b01;
1'b1: b = 2'b10;
default: b = 2'bzz;
endcase
end
endmodule
```

- **1:2 Decoder having enable**

```
module onetotwodecoderenable(a,b,enable);
input a,enable;
output reg [1:0]b;
always@*
begin
if(enable == 1'b1)
begin
if(a == 1'b1) b = 2'b10;
else if(a == 1'b0) b = 2'b01;
end
else b = 2'b00;
end
endmodule
```

- **2:4 Decoder using enable**

```
module twotofourdecodercaseenable(a,b,enable);
input [1:0]a;
input enable;
output reg[3:0] b;
always@*
begin
case(enable)
```

```

1'b1:begin
  case(a)
    2'b00: b = 4'b0001;
    2'b01: b = 4'b0010;
    2'b10: b = 4'b0100;
    2'b11: b = 4'b1000;
    default: b = 4'bxxxx;
  endcase
end
1'b0: b = 4'bxxxx;
default: b = 4'bxxxx;
endcase
end
endmodule

```

- **2:4 Decoder using enable and case**

```

module twotofourdecodercaseenable(a,b,enable);
  input [1:0]a;
  input enable;
  output reg[3:0] b;
  always@*
  begin
    case(enable)
      1'b1:begin
        case(a)
          2'b00: b = 4'b0001;
          2'b01: b = 4'b0010;
          2'b10: b = 4'b0100;
          2'b11: b = 4'b1000;
          default: b = 4'bxxxx;
        endcase
      end
      1'b0: b = 4'bxxxx;
      default: b = 4'bxxxx;
    endcase
  end
endmodule

```

```
    end
```

```
  endmodule
```

- **2:4 Decoder with continuous assignment**

```
module twotofourdecoderassign(a,b);  
  
  input [1:0]a;  
  
  output[3:0]b;  
  
  assign b[3] = a[1]&a[0];  
  
  assign b[2] = a[1]&(~a[0]);  
  
  assign b[1] = (~a[1])&a[0];  
  
  assign b[0] = (~a[1])&(~a[0]);  
  
endmodule
```

- **Decoder using shift operator**

```
module decoderusingshift(a,b);  
  
  input [1:0] a;  
  
  output reg [3:0]b;  
  
  always@*  
  
    b <= 4'b0001<<a;  
  
endmodule
```

- **4:2 Encoder**

```
module fourtotwoencoder(a,b);  
  
  input [3:0]a;  
  
  output [1:0]b;  
  
  assign b[1] = a[3]|a[2];  
  
  assign b[0] = a[3]|a[1];  
  
endmodule
```

- **4:2 Priority Encoder**

```
module priorityencoder(a,b);  
  
input [3:0] a;  
  
output [1:0] b;  
  
assign b[1] = a[3]|a[2];  
  
assign b[0] = a[3] | (~a[2])&a[1];  
  
endmodule
```

- **Positive Level D latch**

```
module posdlatch(d,q,enable);  
  
input d,enable;  
  
output reg q;  
  
always@*  
  
begin  
  
if(enable == 1'b1) q <= d;  
  
end  
  
endmodule
```

- **Negative Level D Latch**

```
module negdlatch(d,q,enable);  
  
input d,enable;  
  
output reg q;  
  
always@*  
  
begin  
  
if(enable == 1'b0) q <= d;  
  
end
```

```
endmodule
```

- **Positive Level Sensitive D Flip Flop**

```
module posdff(d,q,clock);  
input d,clock;  
output reg q;  
always@(posedge clock)  
q <= d;  
endmodule
```

- **Negative Level Sensitive D Flip Flop**

```
module negdff(d,q,clock);  
input d,clock;  
output reg q;  
always@(negedge clock)  
q <= d;  
endmodule
```

- **D FF having synchronous reset**

```
module synchresetdff(d,q,clock,reset);  
input d,clock , reset;  
output reg q;  
always@(posedge clock)  
if(~reset)q<=1'b0;  
else q <= d;  
endmodule
```

- **D FF having asynchronous reset**

```
module asynchresetdff(d,q,clock,reset);  
  input d,clock , reset;  
  output reg q;  
  always@(posedge clock or negedge reset)  
    if(~reset)q<=1'b0;  
    else q <= d;  
endmodule
```

- **D FF having synchronous load and asynchronous reset**

```
module asynchresetdff(d,q,clock,reset,load);  
  input d,clock,reset,load;  
  output reg q;  
  always@(posedge clock or negedge reset)  
    if(~reset)q<=1'b0;  
    else if(load) q<= 1'b1;  
    else q <= d;  
endmodule
```

- **D FF having synchronous load and synchronous reset**

```
module synchresetdff(d,q,clock,reset,load);  
  input d,clock,reset,load;  
  output reg q;  
  always@(posedge clock)  
    if(~reset)q<=1'b0;  
    else if(load) q<= 1'b1;  
    else q <= d;
```

```
endmodule
```

- **Three bit up counter**

```
module threebitupcounter(reset,clock,count);  
  
input reset , clock;  
  
output reg [2:0] count;  
  
always@(posedge clock)  
  
begin  
  
if(reset) count <= 3'b0;  
  
else  
  
begin  
  
if(count == 3'b111) count <= 3'b0;  
  
else count <= count + 1;  
  
end  
  
end  
  
endmodule
```

- **Three bit down counter**

```
module threebitdowncounter(reset,clock,count);  
  
input reset , clock;  
  
output reg [2:0] count;  
  
always@(posedge clock)  
  
begin  
  
if(reset) count <= 3'b000;  
  
else  
  
begin
```

```
if(count == 3'b000) count <= 3'b111;  
else count <= count - 1;  
end  
end  
endmodule
```

- **Three bit up down counter**

```
module threebitupdowncounter(reset,clock,count,up);  
input reset , clock , up;  
output reg [2:0] count;  
always@(posedge clock)  
begin  
if(reset) count <= 3'b000;  
else  
begin  
if(up)  
begin  
if(count == 3'b111) count <= 3'b0;  
else count <= count + 1;  
end  
else  
begin  
if(count == 3'b000) count <= 3'b111;  
else count <= count - 1;  
end
```

```
end  
end  
endmodule
```

- **Two bit gray counter**

```
module twoabitgraycounter(inp , out , reset , clock);  
input [1:0] inp;  
output [1:0] out;  
input reset , clock;  
always@(posedge clock)  
begin  
if(reset) out <= 2'b00;  
else begin  
out[1] <= inp[0];  
out[0] <= ~inp[1];  
end  
end  
endmodule
```

- **Parameterized binary and gray counter**

```
module parameterizedgrayandbinary(clock,reset, gray_out, binary_out);  
input clock , reset;  
output reg [3:0] gray_out , binary_out;  
always@(posedge clock , negedge reset)  
begin  
if(~reset) {binary_out,gray_out} = 8'b00000000;
```

```
else
begin
binary_out <= binary_out + 1;
gray_out <= (binary_out>>1)^binary_out;
end
end
endmodule
```

- **Four bit Ring Counter**

```
module ringcounter( clock , reset , count);
input clock, reset;
output reg [3:0] count;
always@(posedge clock , negedge reset)
begin
if(~reset) count <= 4'b0000;
else count <= {count[0],count[3:1]};
end
endmodule
```

- **Four bit Johnson Counter**

```
module johnsoncounter( clock , reset , count);
input clock, reset;
output reg [3:0] count;
always@(posedge clock , negedge reset)
begin
if(~reset) count <= 4'b0000;
```

```
else count <= {~count[0],count[3:1]};
```

```
end
```

```
endmodule
```

- **Four bit BCD up-down counter**

```
module threebitupdowncounter(reset,clock,count,up);
```

```
input reset , clock , up;
```

```
output reg [2:0] count;
```

```
always@(posedge clock)
```

```
begin
```

```
if(reset) count <= 3'b000;
```

```
else
```

```
begin
```

```
if(up)
```

```
begin
```

```
if(count == 3'b111) count <= 3'b0;
```

```
else count <= count + 1;
```

```
end
```

```
else
```

```
begin
```

```
if(count == 3'b000) count <= 3'b111;
```

```
else count <= count - 1;
```

```
end
```

```
end
```

```
end
```

```
endmodule
```

- **4 bit PIPO register**

```
module fourbitpipe(inp,out,clock,load);  
  
input [3:0] inp;  
  
input clock,load;  
  
output reg [3:0] out;  
  
always@(posedge clock)  
  
begin  
  
if(load == 1'b1) out<= in;  
  
end  
  
endmodule
```

- **SISO register**

```
module siso ( clock , reset , in , out);  
  
reg t1 , t2 , t3;  
  
  
always@(posedge clock , negedge reset)  
  
begin  
  
if(~reset) {out,t3,t2,t1} <= 4'b0000;  
  
else  
  
begin  
  
out <= t3;  
  
t3 <= t2;  
  
t2 <= t1;  
  
t1 <= in;
```

```
end  
end  
endmodule
```

- **Right/Left Shift Register**

```
module left_right(right_left , clock ,reset, in , out);  
input right_left , clock , in , reset;  
output reg [3:0] out;  
always@(posedge clock , negedge reset);  
begin  
if (~reset) out <=4'b0000;  
else  
begin  
if(right_left) out <= {in,out[3:1]};  
else out <= {out[2:0],in};  
end  
end  
endmodule
```

- **4:1 Mux having registered output**

```
module registeredmux(a,b,c,d,out,select,clock);  
input [3:0] a,b,c,d;  
output reg [3:0] out;  
input [1:0]select;  
input clock;  
always@(posedge clock)
```

```
begin  
  case(select)  
    2'b00: out <= a;  
    2'b01: out <= b;  
    2'b10: out <= c;  
    2'b11: out <= d;  
  default: out <= 4'b0000;  
  endcase  
end  
endmodule
```

- **4-bit ripple up counter**

```
module rippleup( clock , toggle_in , reset, count);  
  input clock, toggle_in, reset  
  output reg [3:0] count;  
  wire c0, c1, c2;  
  assign c0 = count[0];  
  assign c1 = count[1];  
  assign c2 = count[2];  
  always @ (posedge clock , negedge reset )  
  begin  
    if (reset == 1'b0)  
      count[0] <= 1'b0;  
    else if (toggle_in == 1'b1)  
      count[0] <= ~count[0];
```

```
end

always @ (negedge c0, negedge reset )

begin

if (reset == 1'b0)

count[1] <= 1'b0;

else if (toggle_in == 1'b1)

count[1] <= ~count[1];

end

always @ (negedge c1, negedge reset )

begin

if (reset == 1'b0)

count[2] <= 1'b0;

else if (toggle_in == 1'b1)

count[2] <= ~count[2];

end

always @ (negedge c2, negedge reset )

begin

if (reset == 1'b0)

count[3] <= 1'b0;

else if (toggle_in == 1'b1)

count[3] <= ~count[3];

end

endmodule
```

- **Read write Memory**

```

module readwrite(input clk,cs,read_write,[4:0]data_in,[4:0]address,
output [4:0]data_out);
reg[4:0]memory[0:10];
always@(posedge clk)
if(read_write && cs)
memory[address]<=data_in;
always@(posedge clk)
if(~read_write && cs)
data_out<=memory[address];
endmodule

```

- **Parameterized Read Write Memory used in the FIFO having 8 location depth**

```

module para_mem #(parameter data_size = 8, parameter ad-
dress_size = 3)
(
input [data_size-1:0] write_data,
input [address_size-1:0] write_address, read_address,
input write_clk_en, write_full, write_clk,
output [data_size-1:0] read_data);
localparam FIFO_depth = 1<<address_size;
reg [data_size-1:0] mem [0:FIFO_depth-1];
assign read_data = mem[read_address];
always @(posedge write_clk)
if (write_clk_en && !write_full) mem[write_address] <= write_data;
endmodule

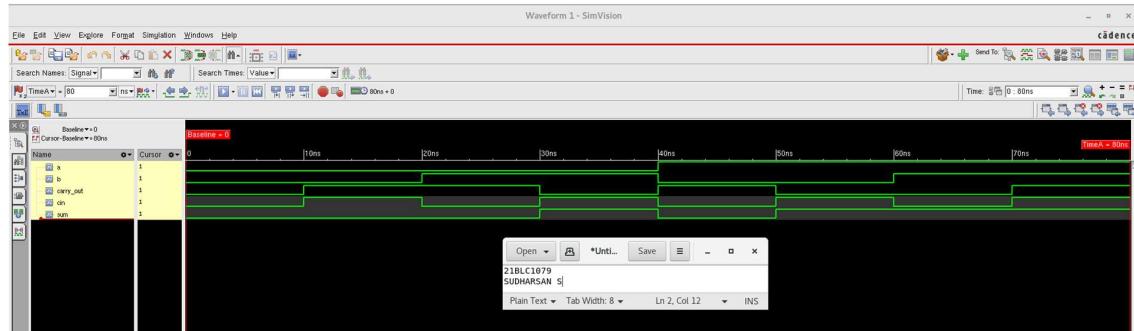
```

2) Test benches

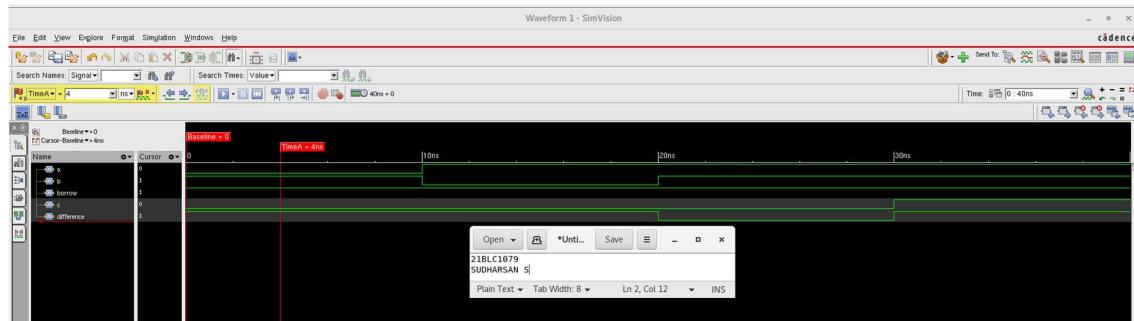
- Half Adder



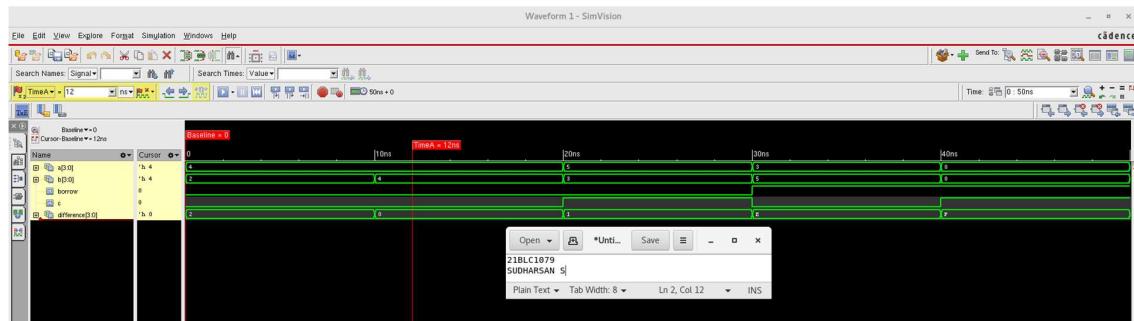
- Full Adder



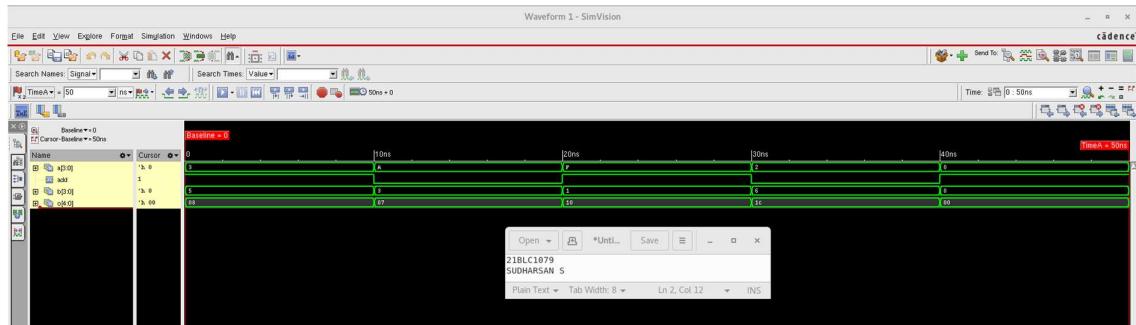
- Full subtractor



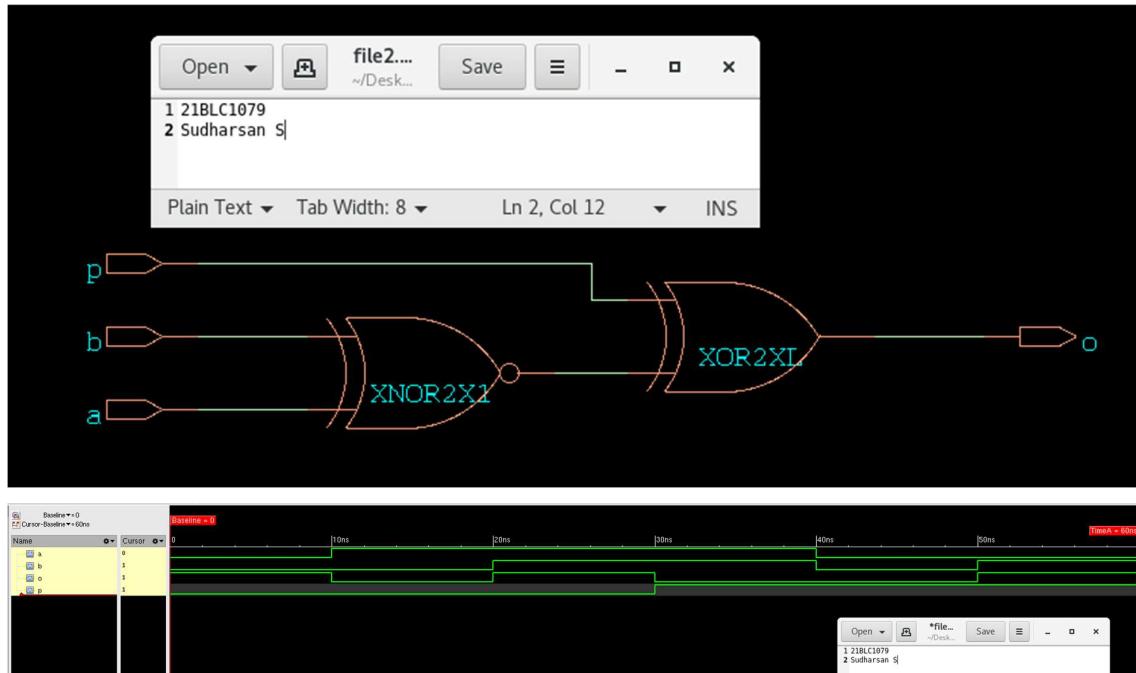
- 4 bit full subtractor



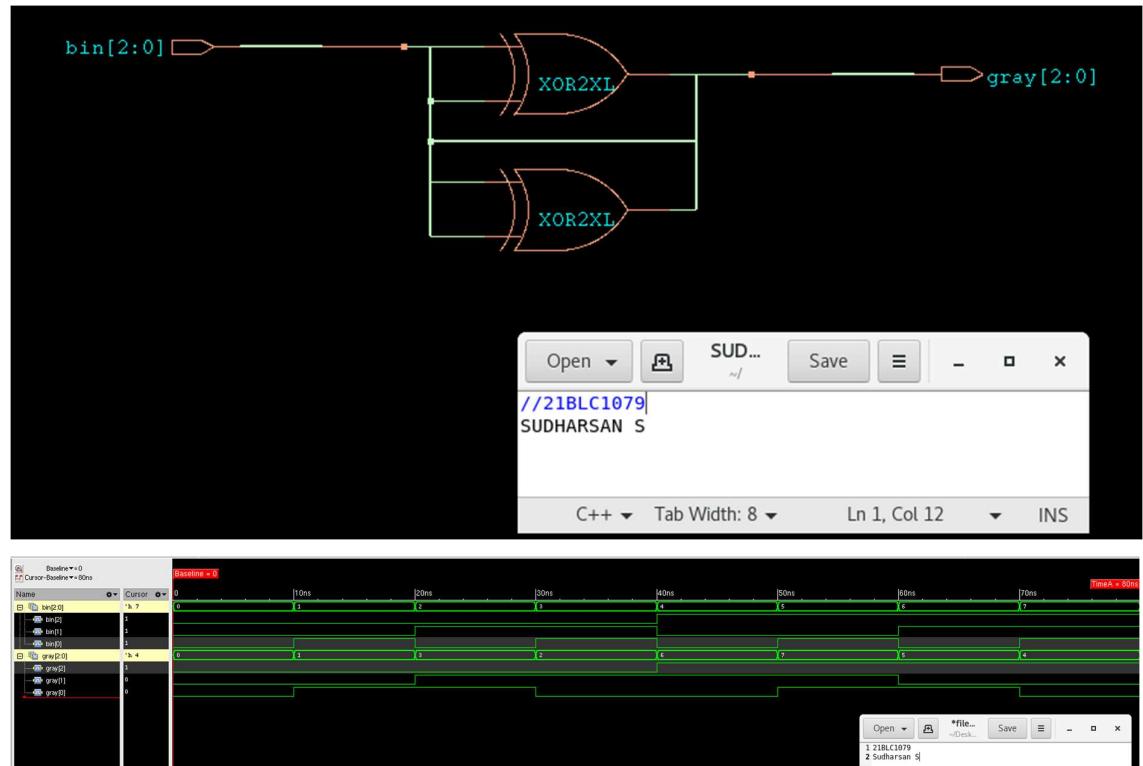
- 4 bit adder and subtractor



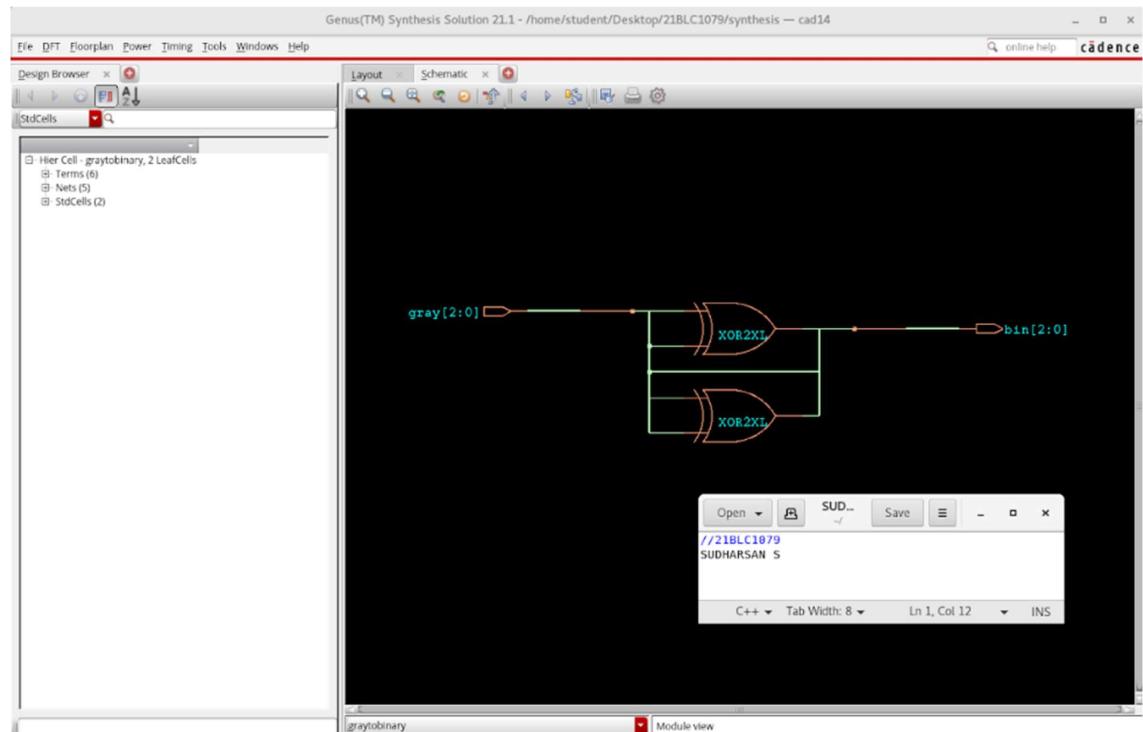
- Parity detector

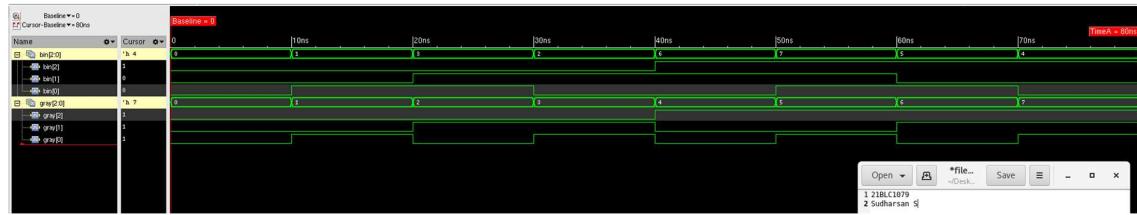


- Binary to gray code converter

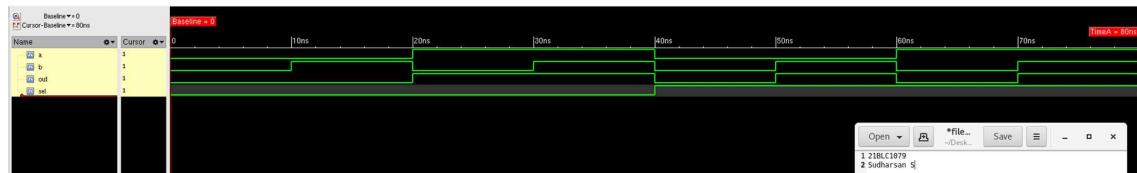
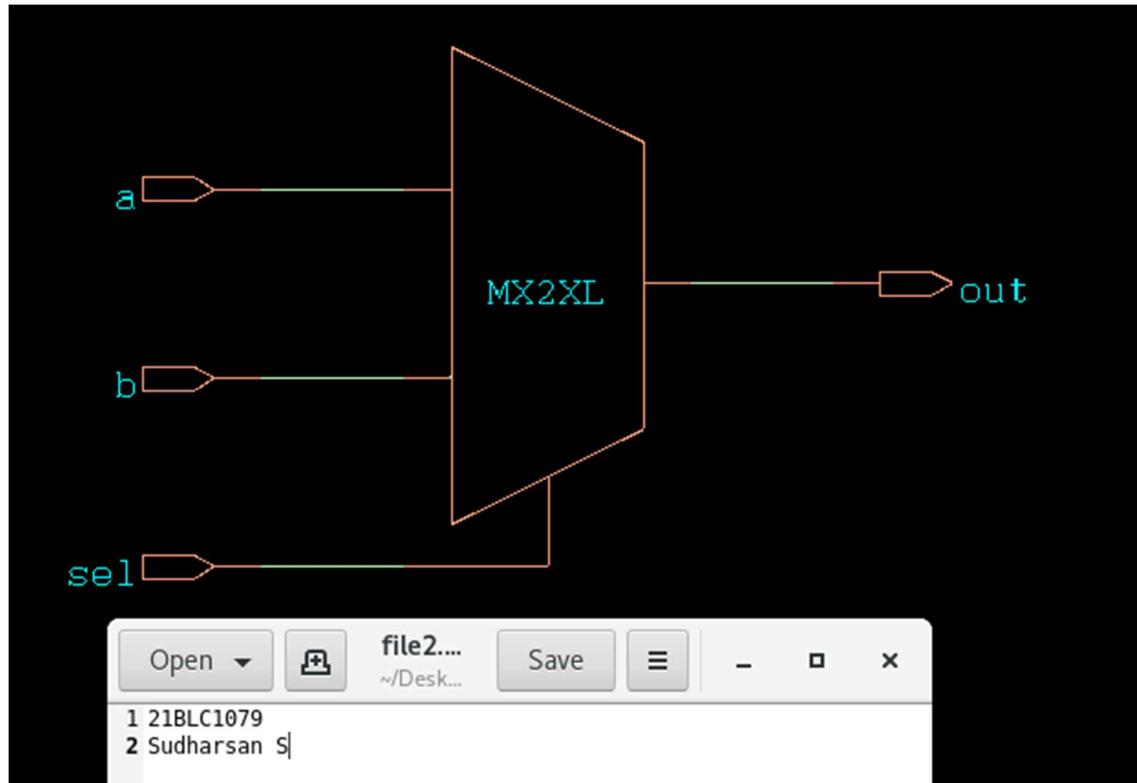


- Gray to binary converter

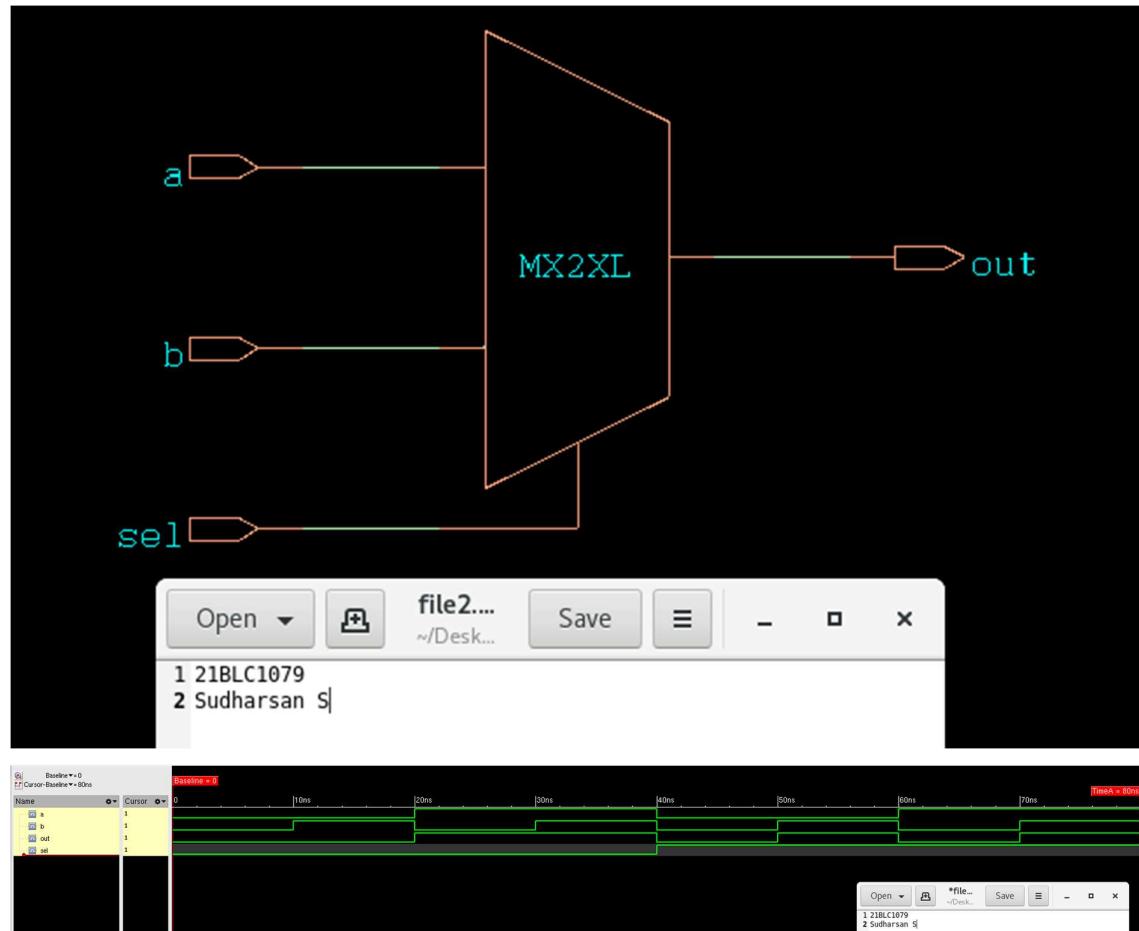




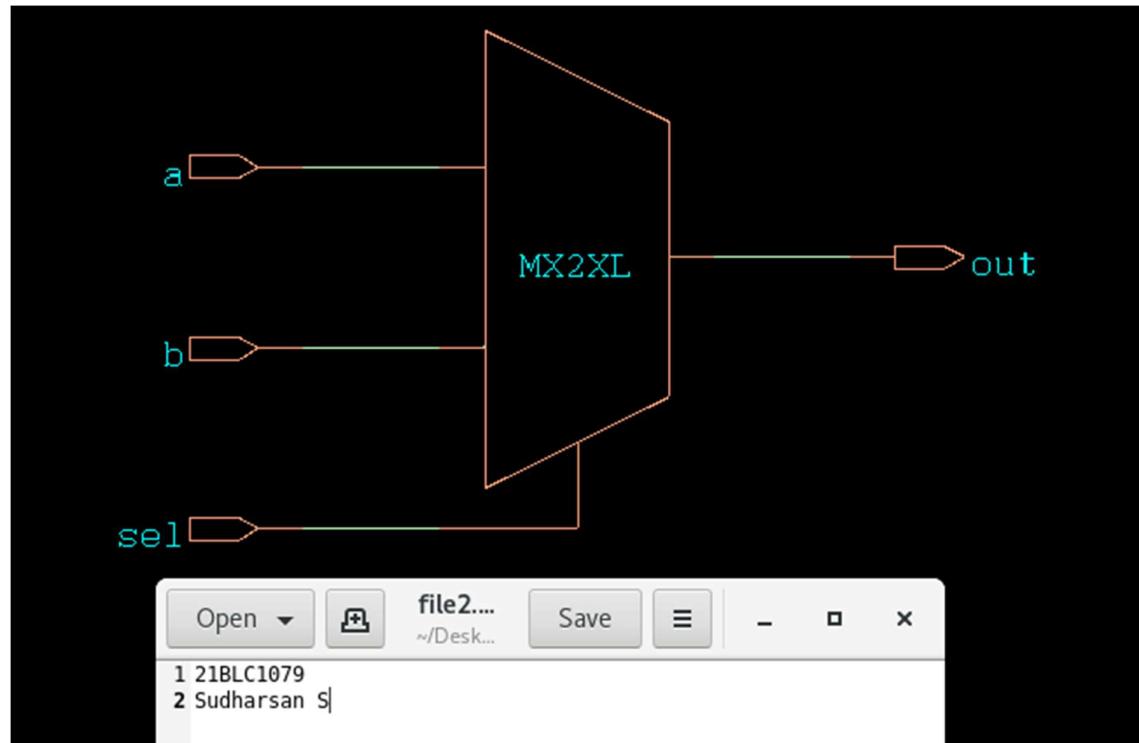
- 2:1 Mux

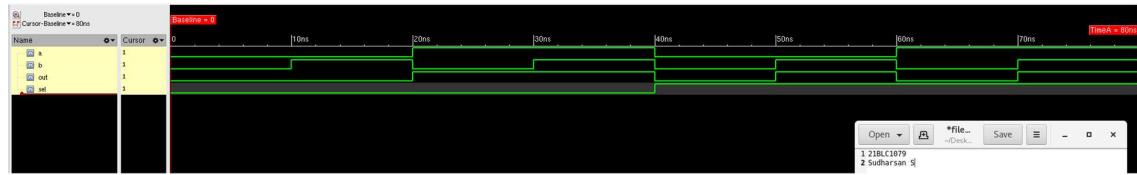


- 2:1 Mux using if else

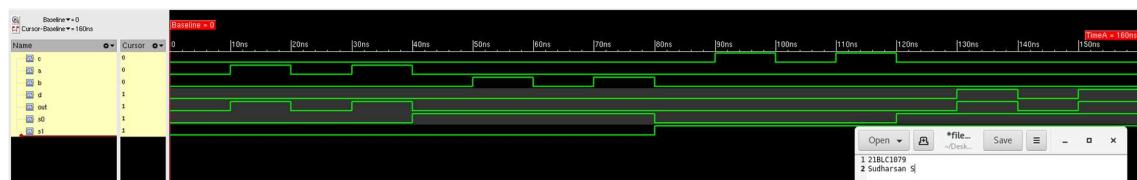
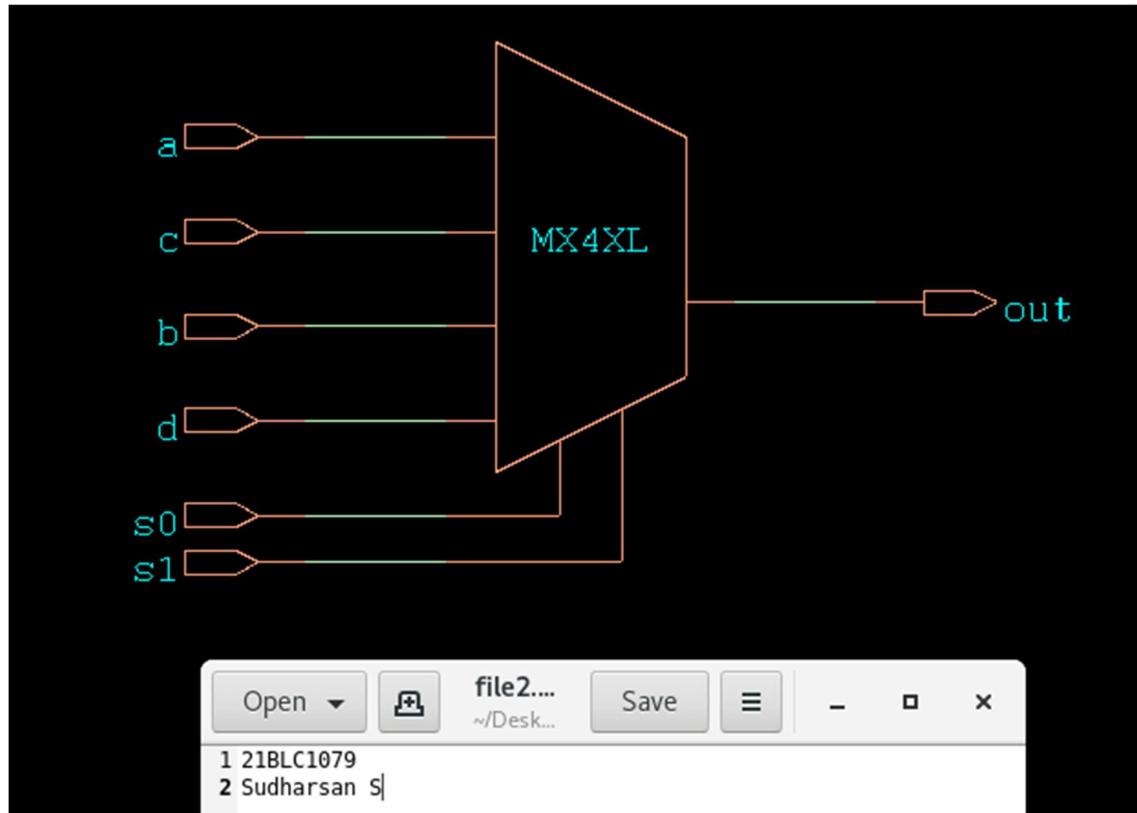


- 2:1 Mux using case

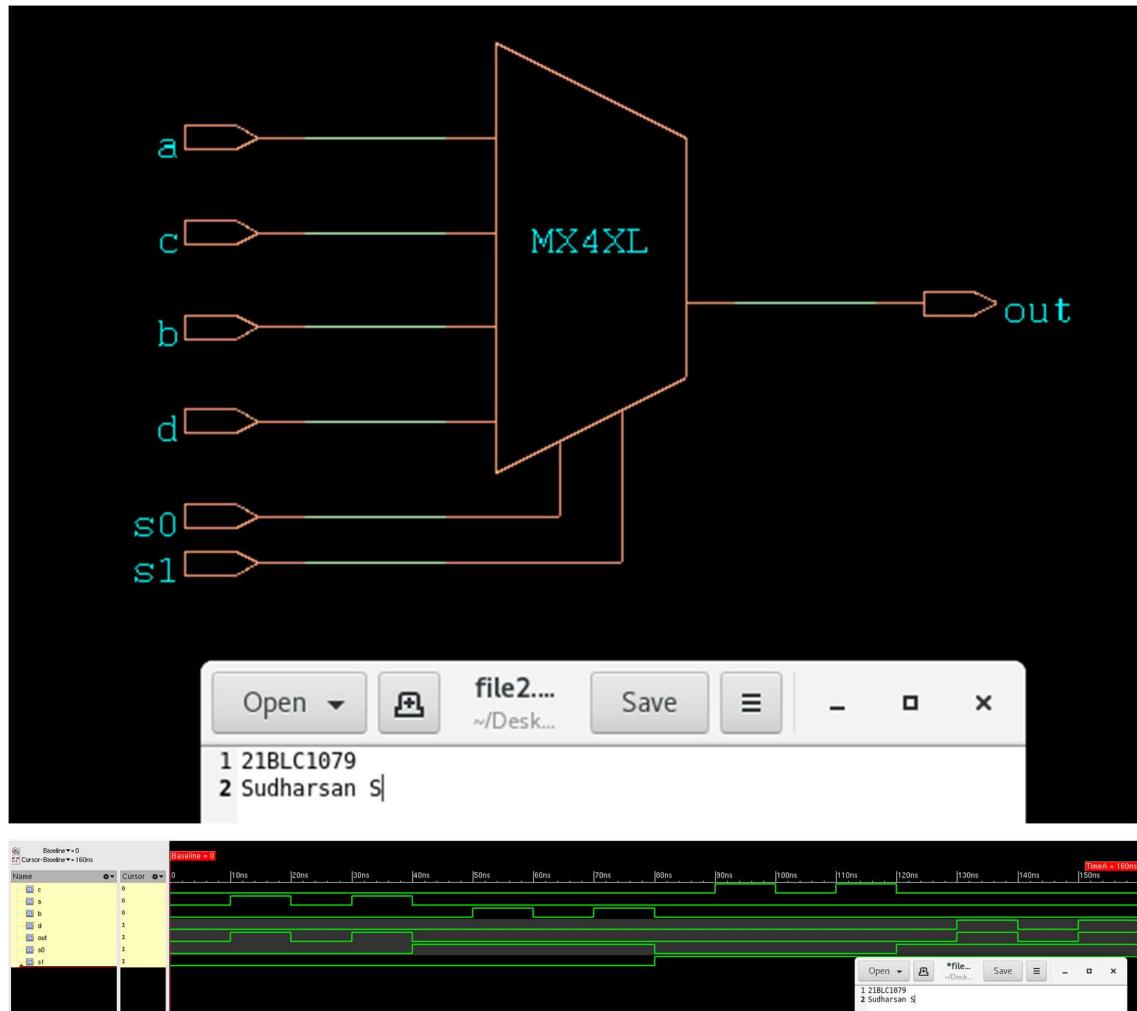




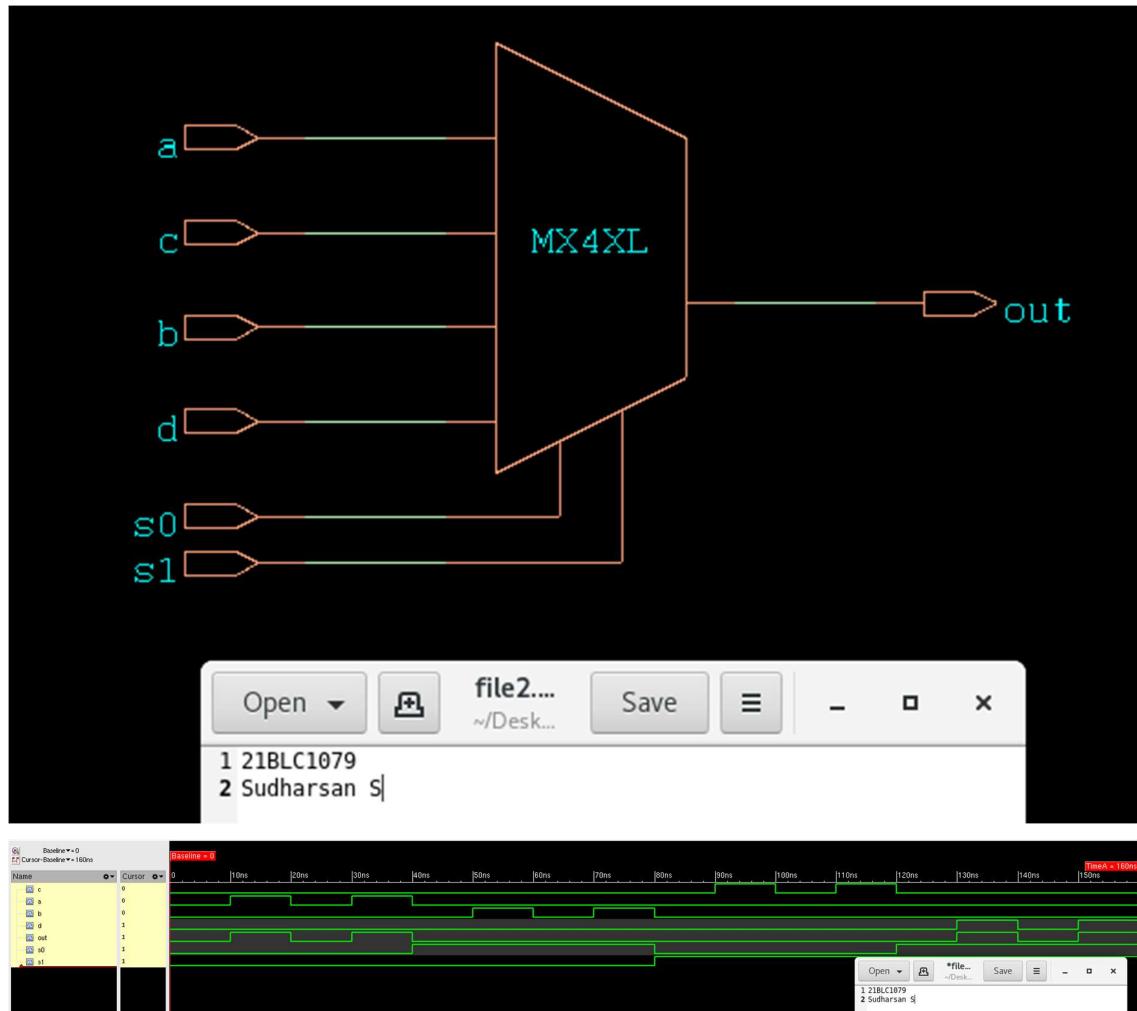
- 4:1 Mux



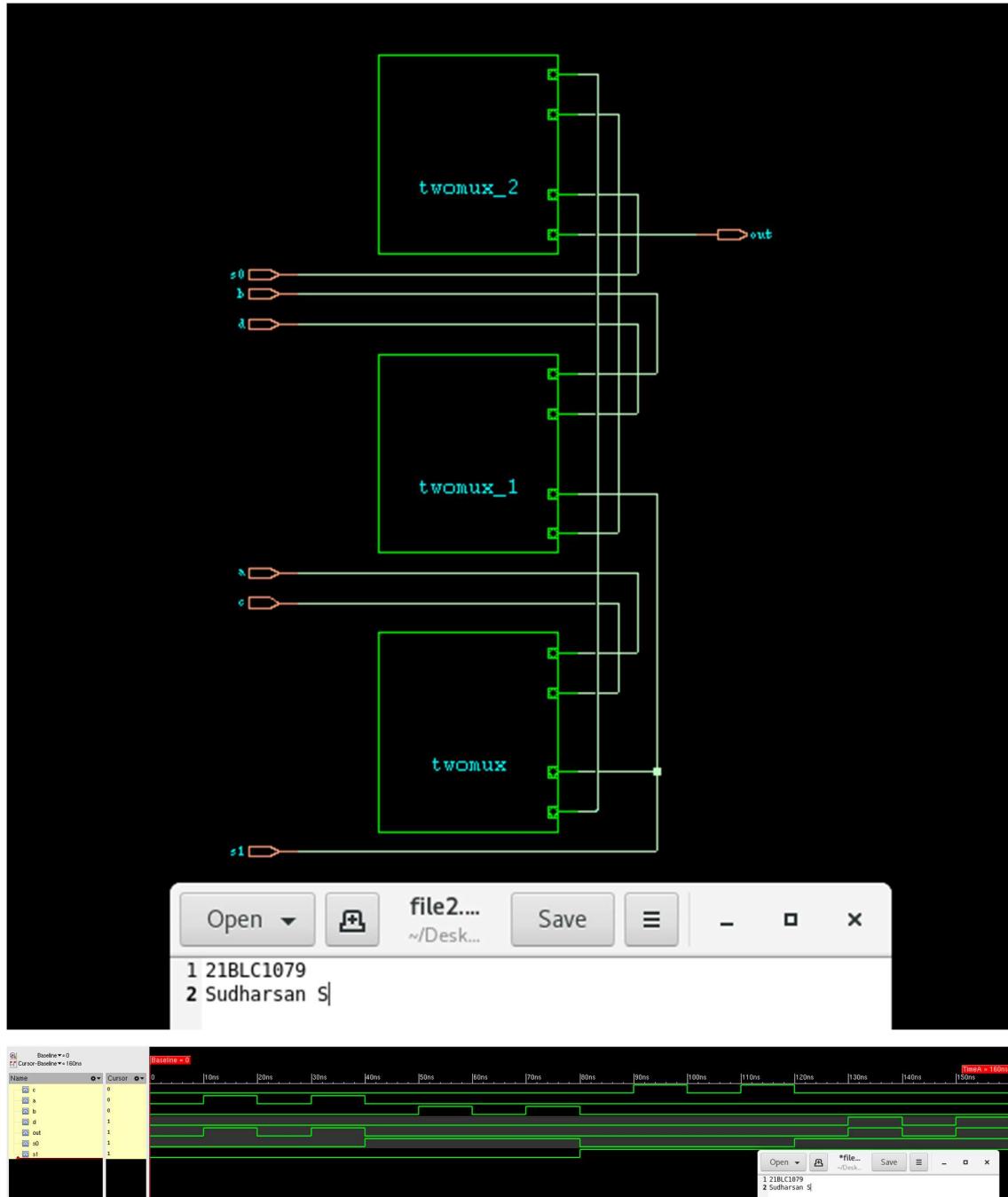
- 4:1 Mux if else



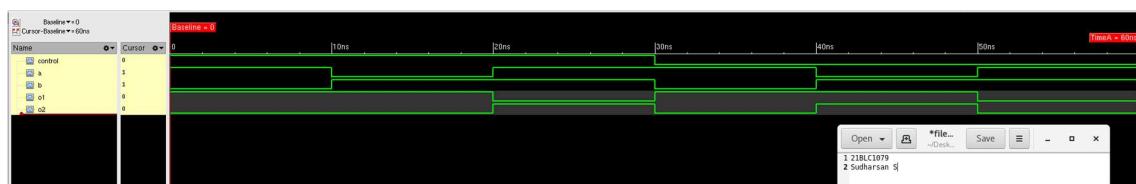
- 4:1 Mux using case



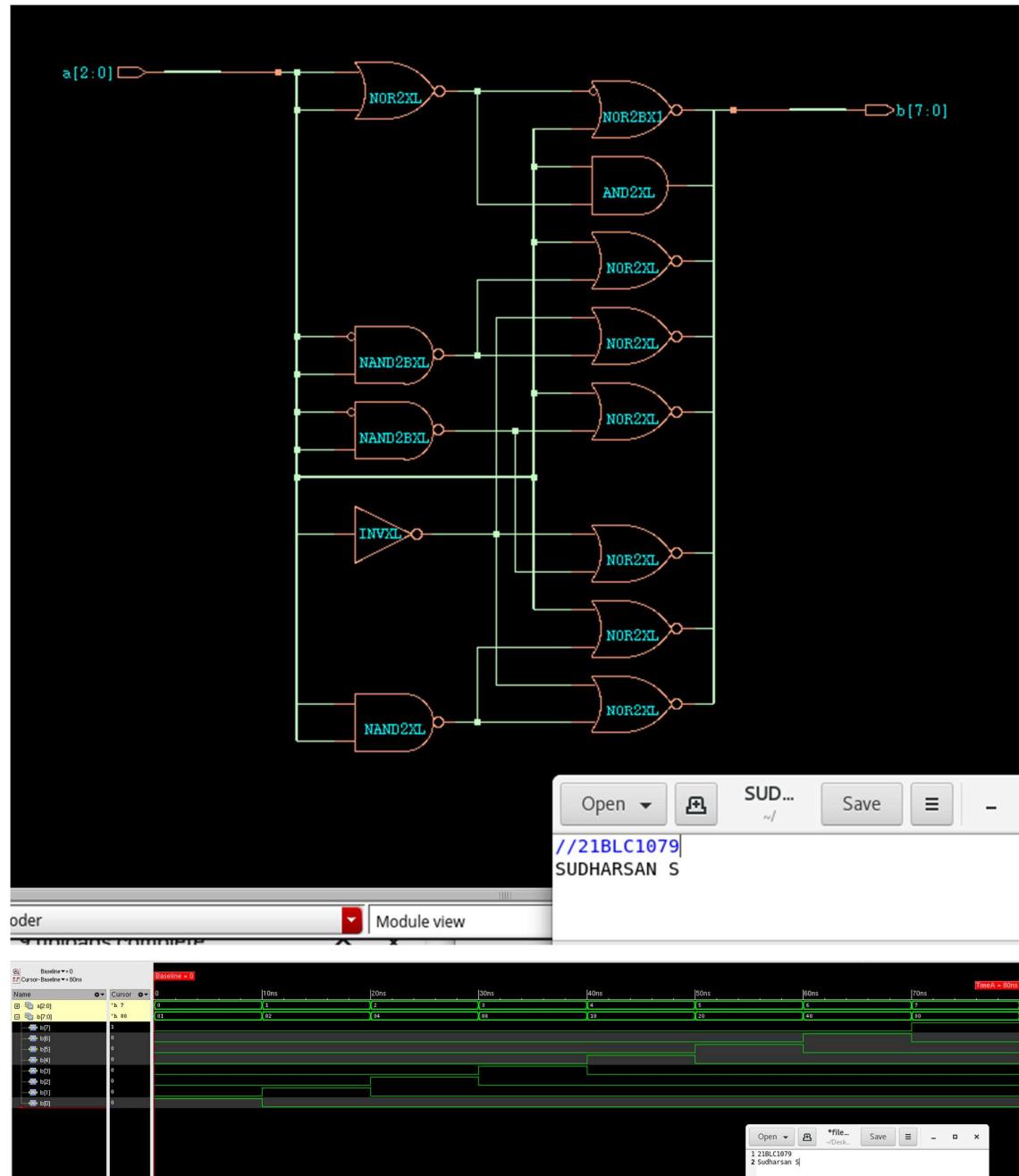
- 4:1 Mux using 2:1 Mux



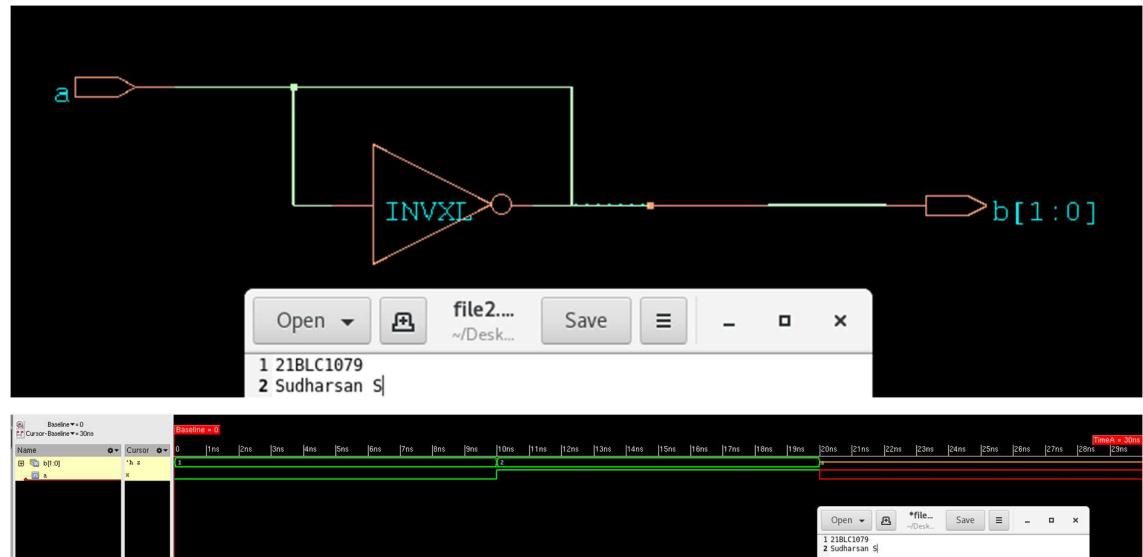
- Addition and subtraction using if else



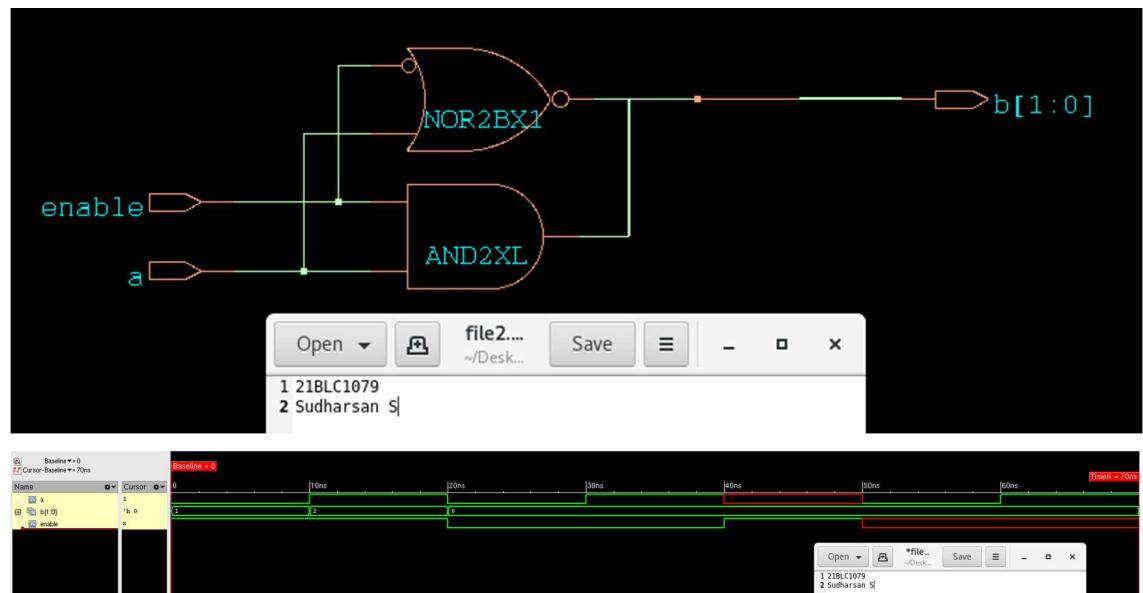
- 3:8 Decoder



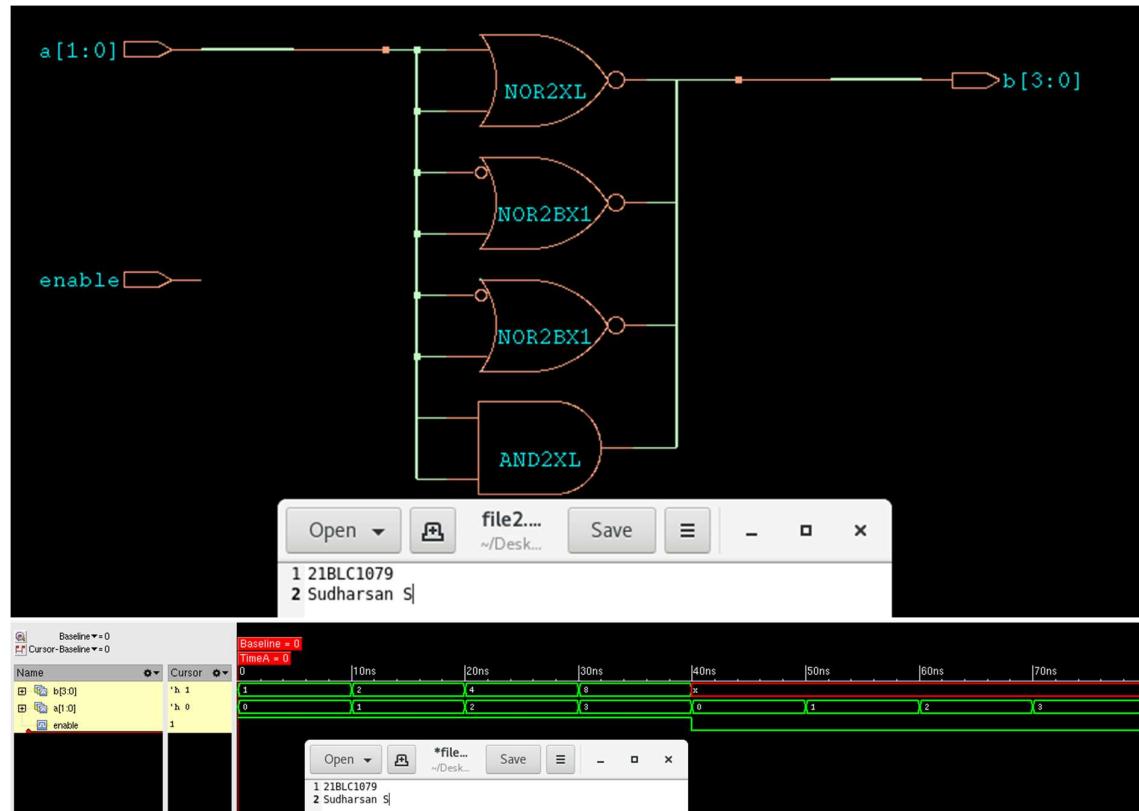
- 1:2 Decoder using case



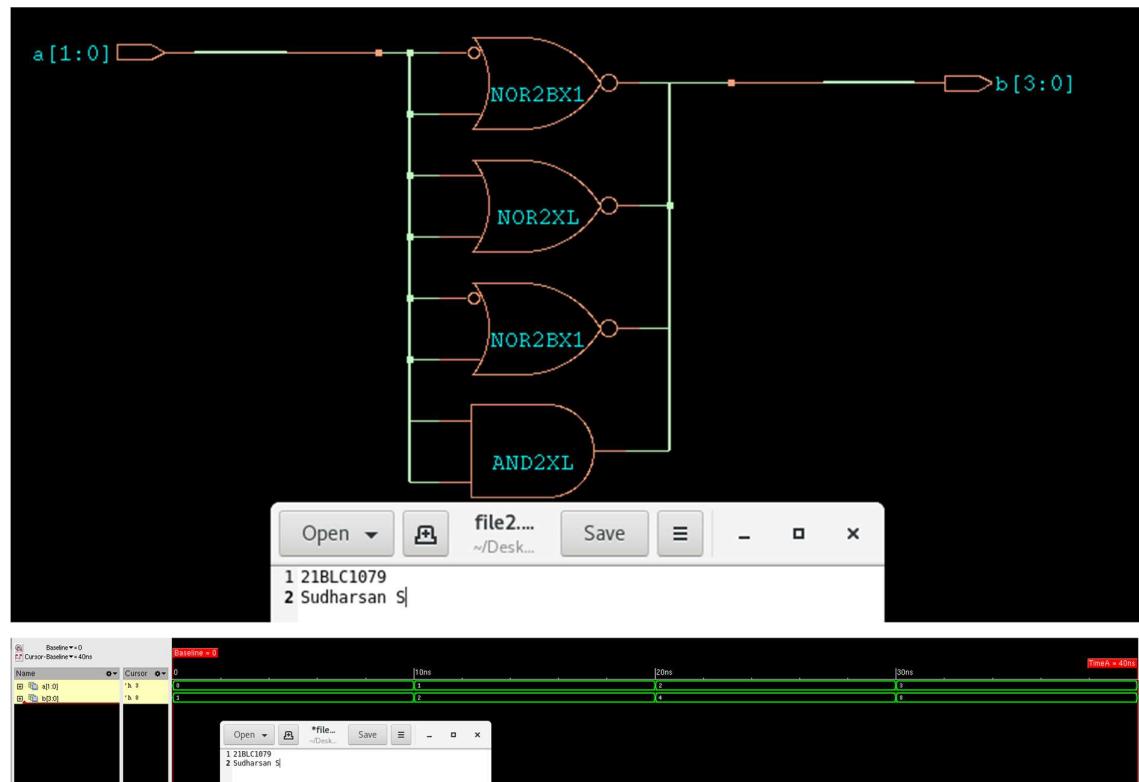
- **1:2 Decoder having enable**



- **2:4 Decoder with case enable**



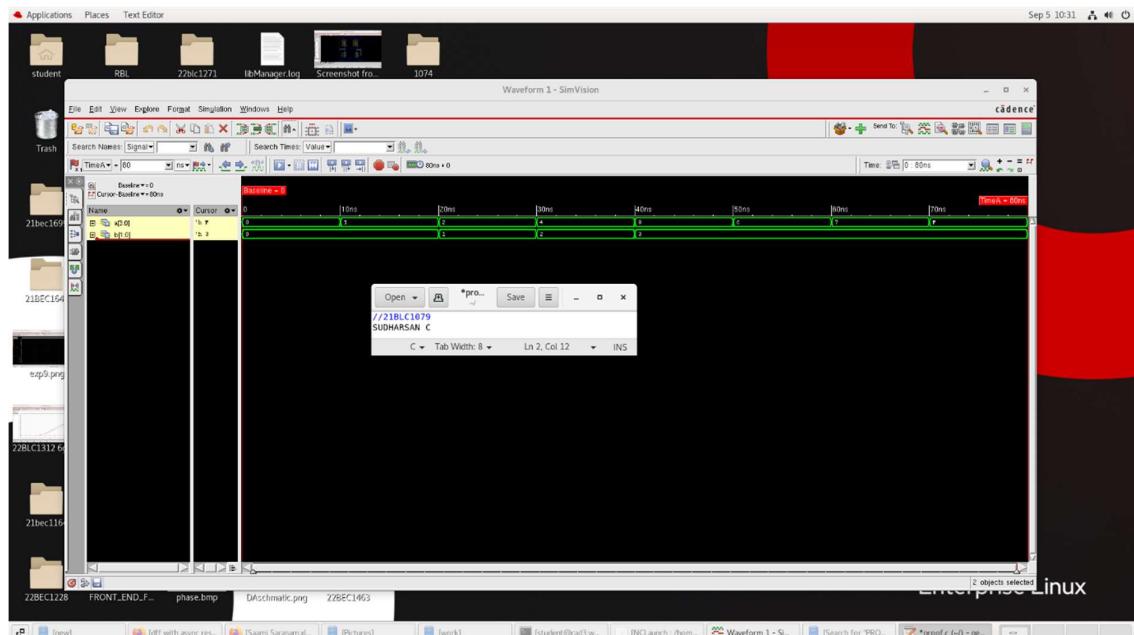
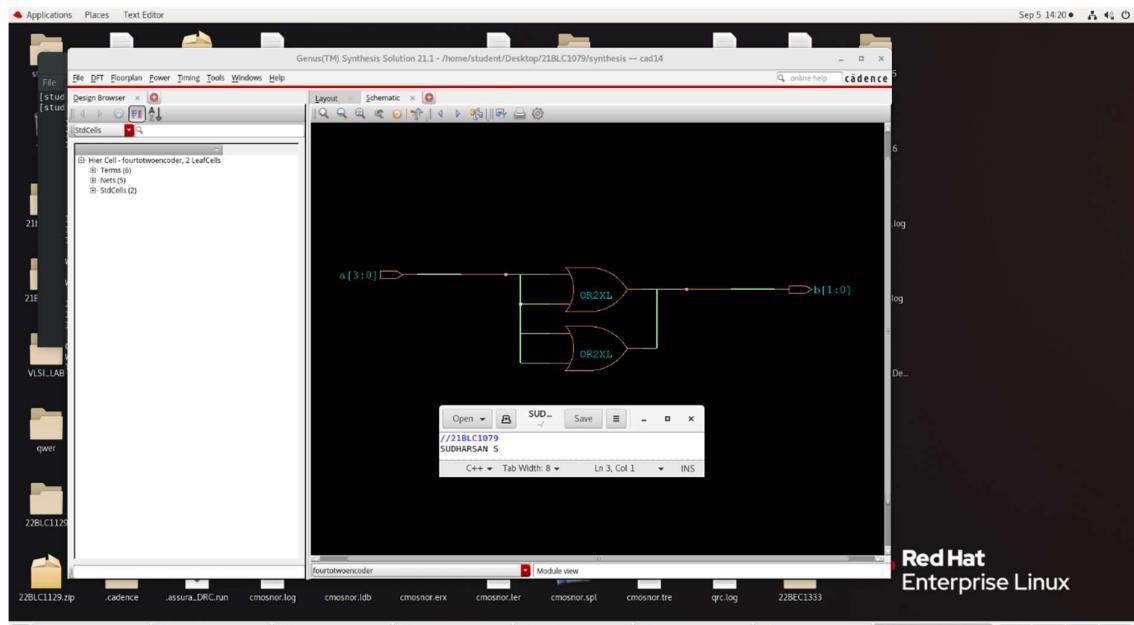
- 2:4 Decoder with continuous assignment



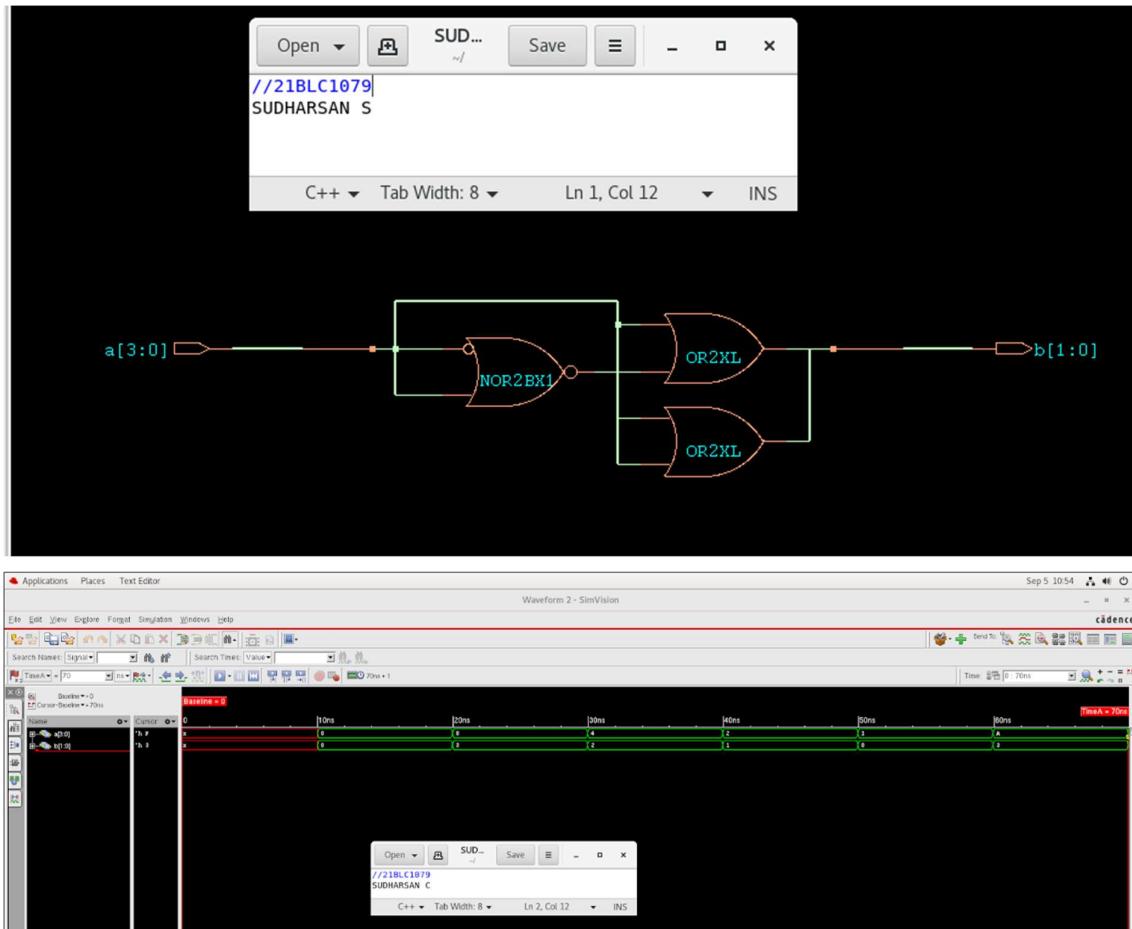
- Decoder using shift operator



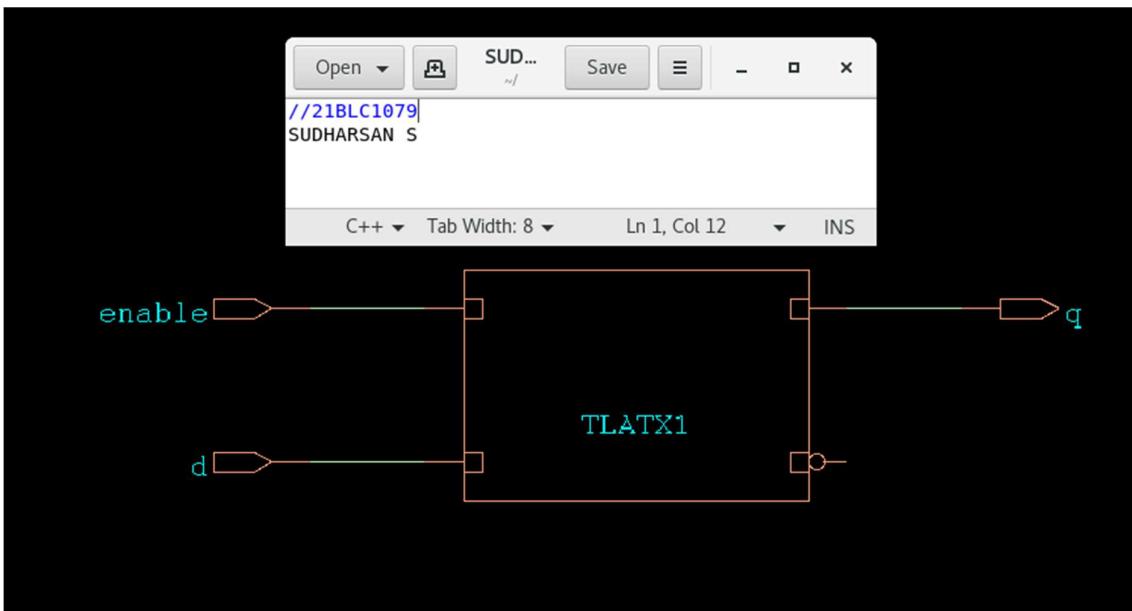
- 4:2 Encoder

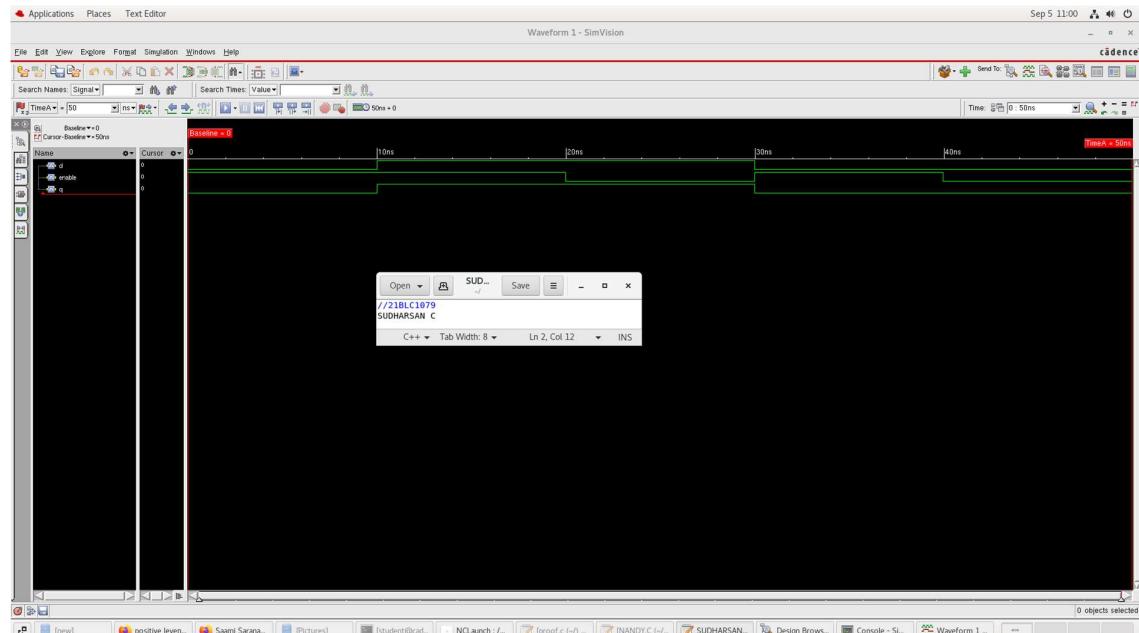


- 4:2 Priority Encoder

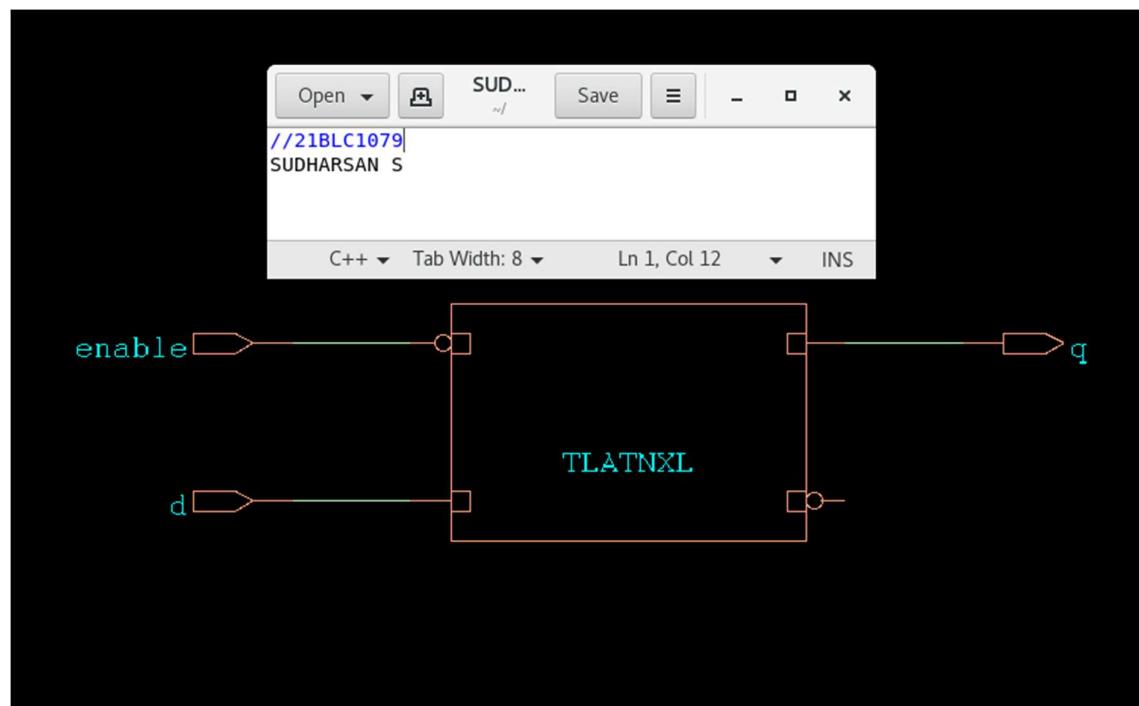


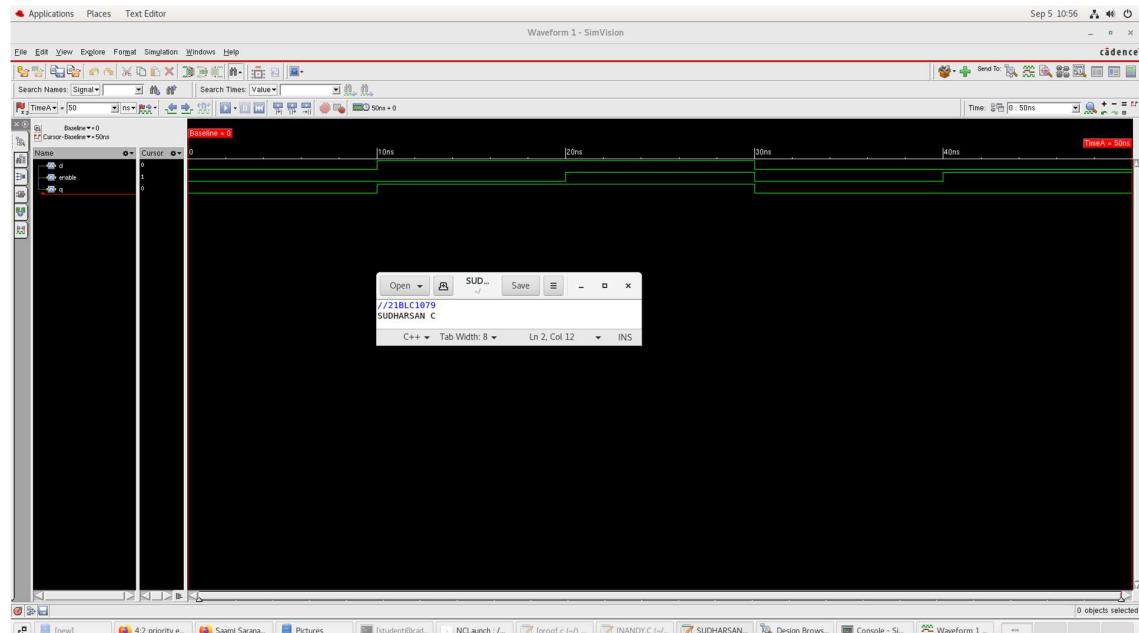
- Positive Level Sensitive D Flip Flop



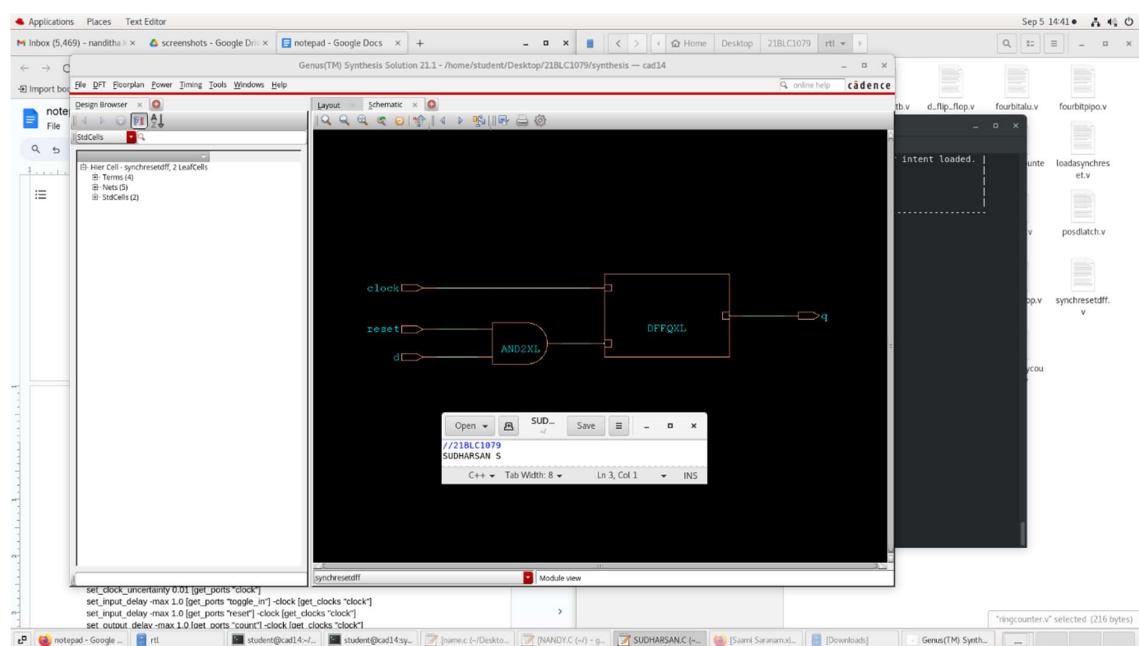


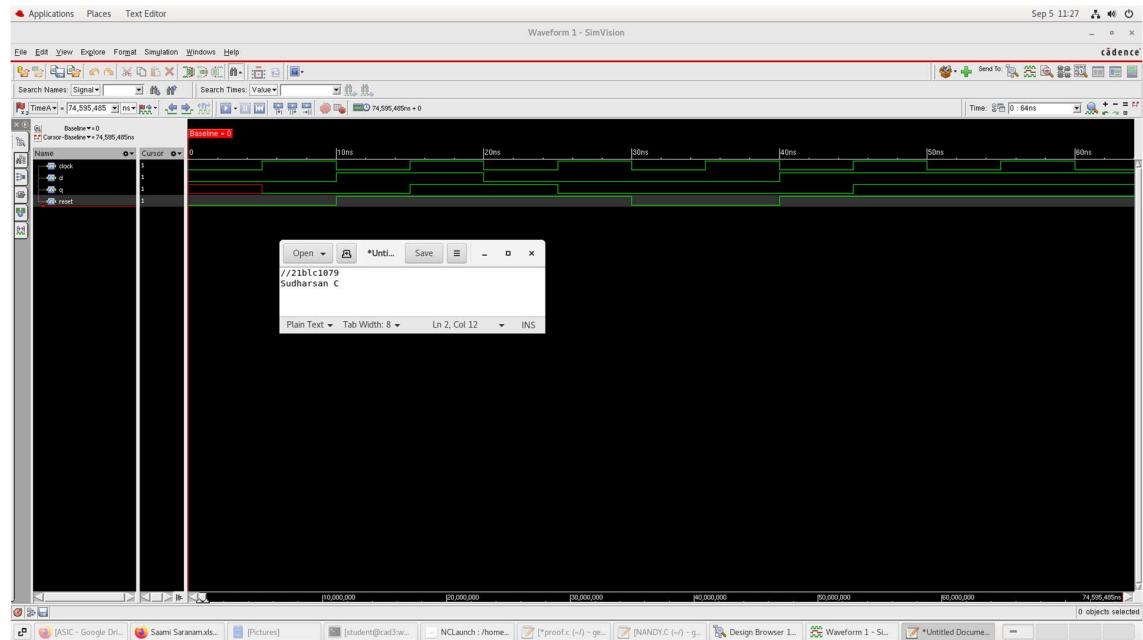
- **Negative Level Sensitive D Flip Flop**



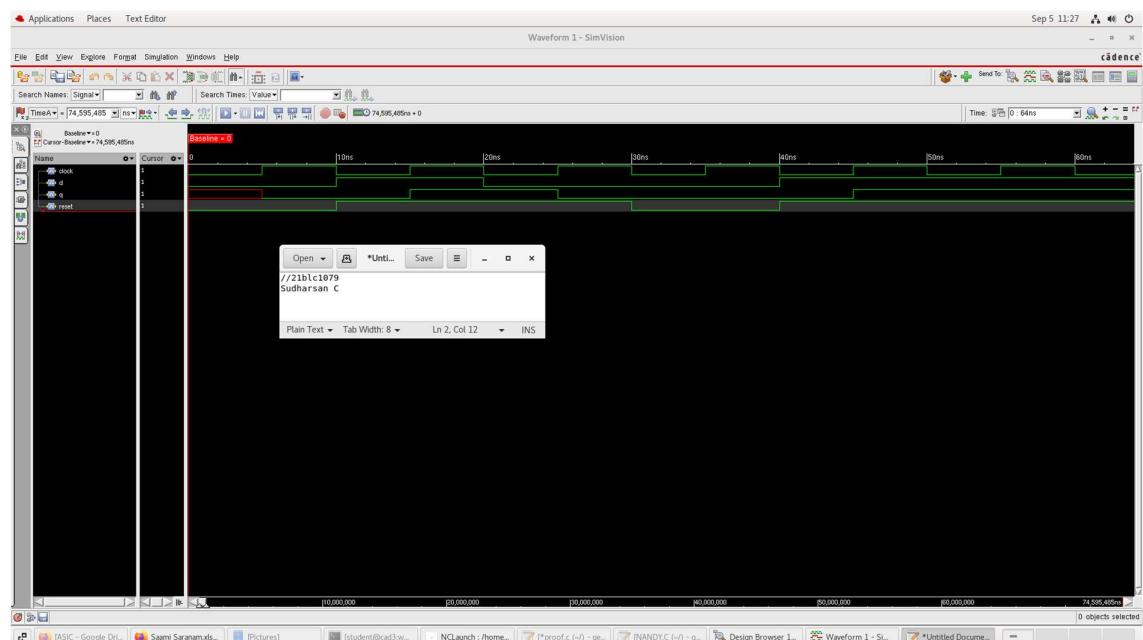


- **D FF having synchronous reset**

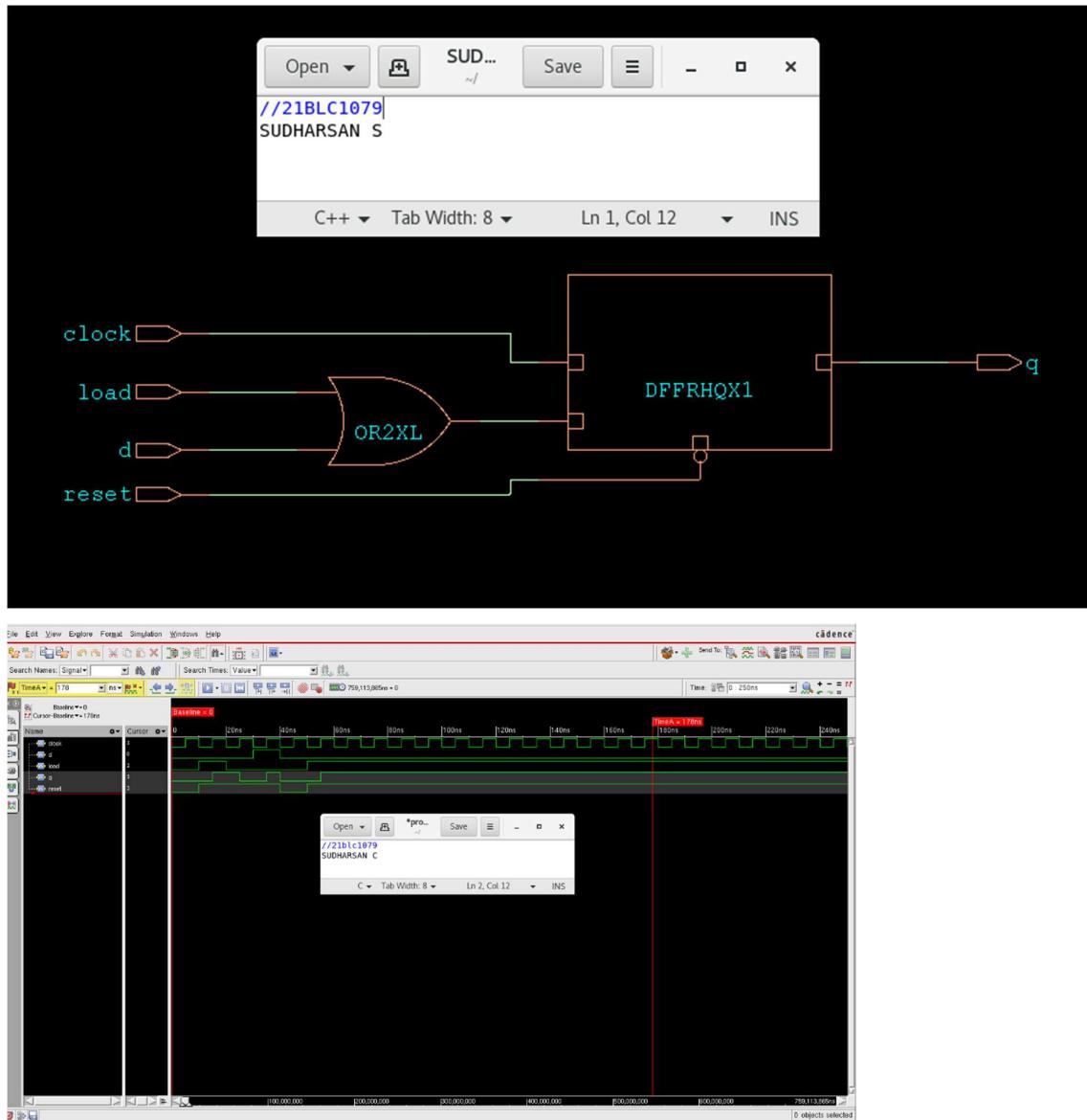




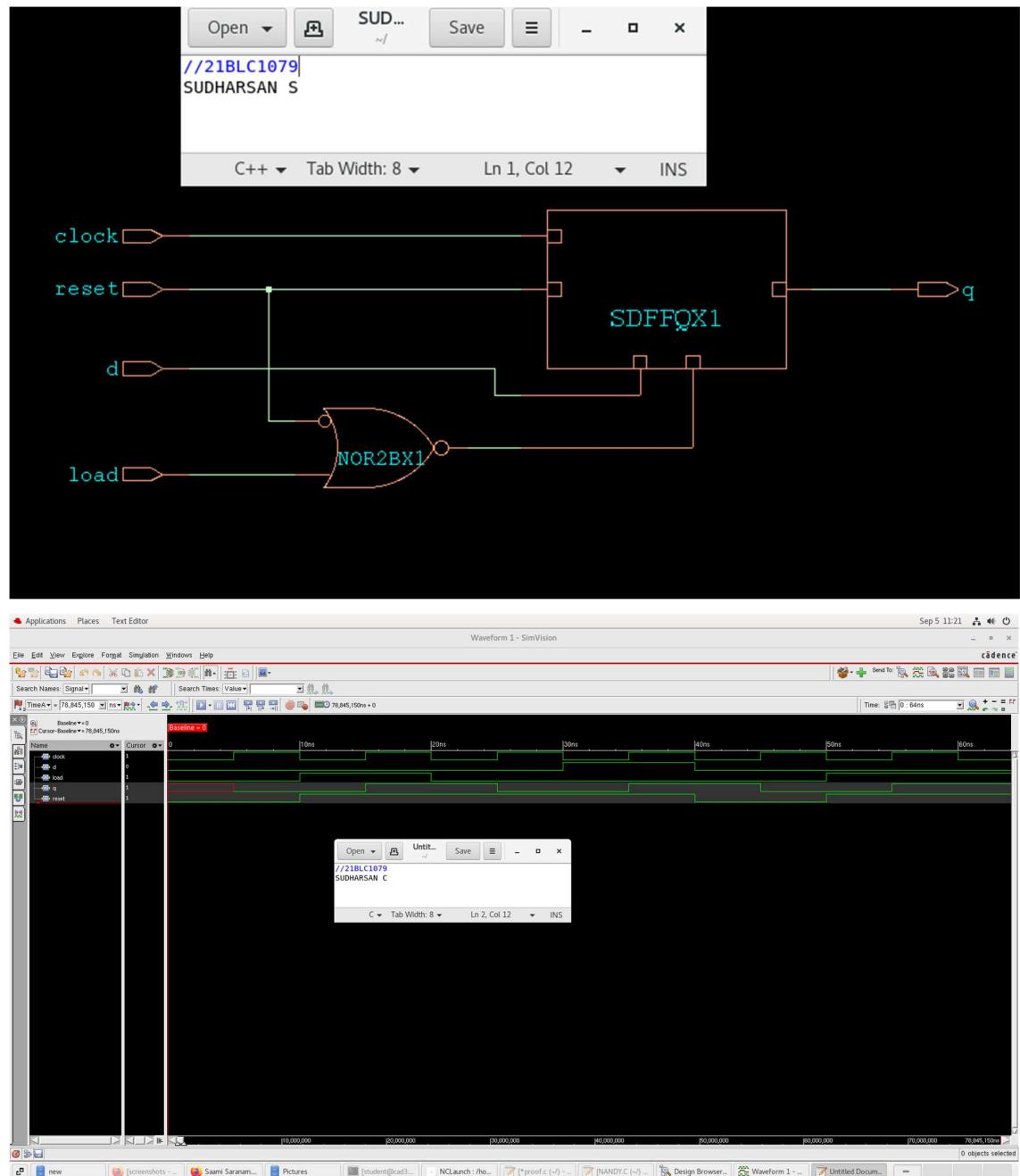
- **D FF having asynchronous reset**



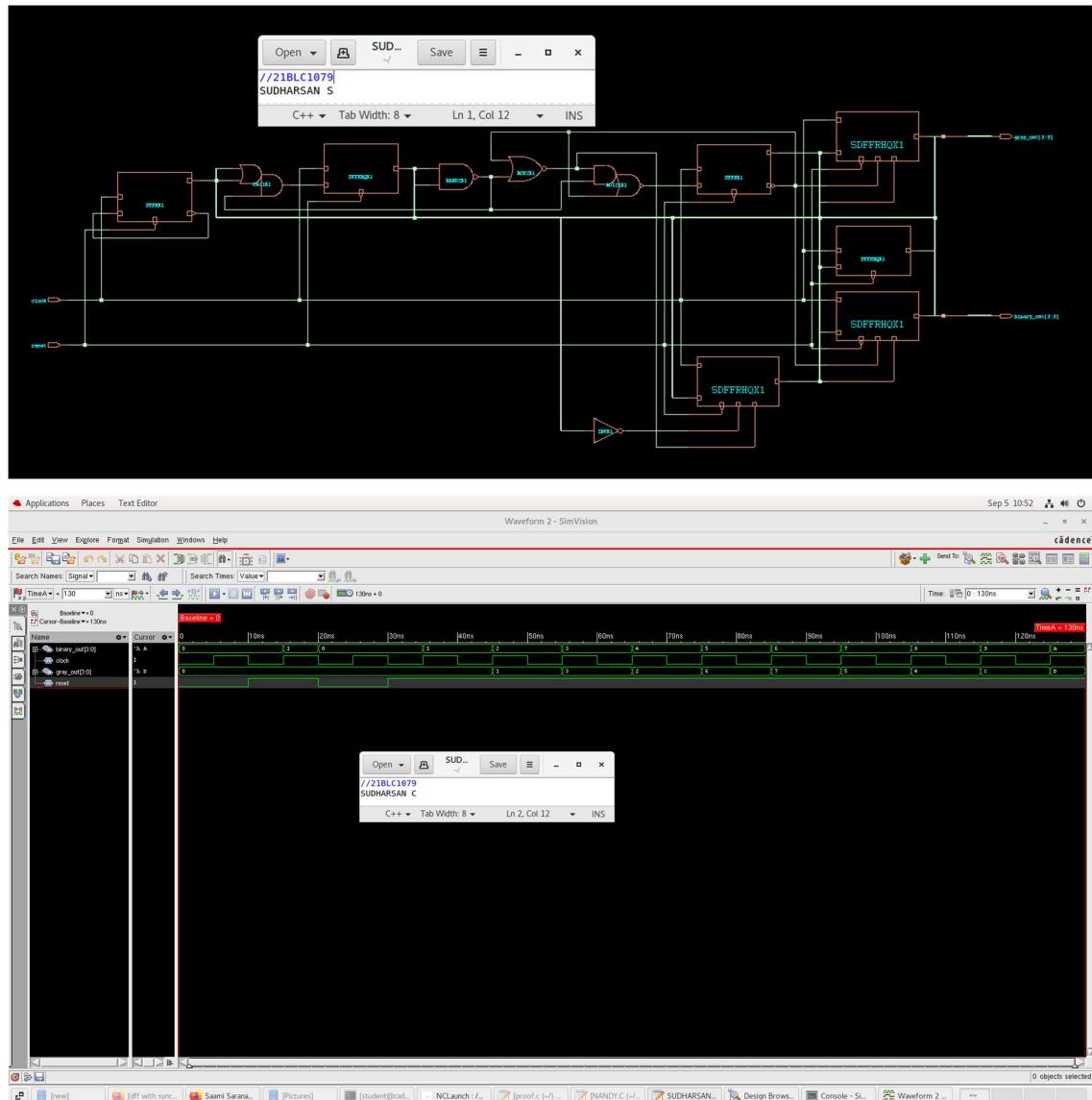
- **D FF having synchronous load and asynchronous reset**



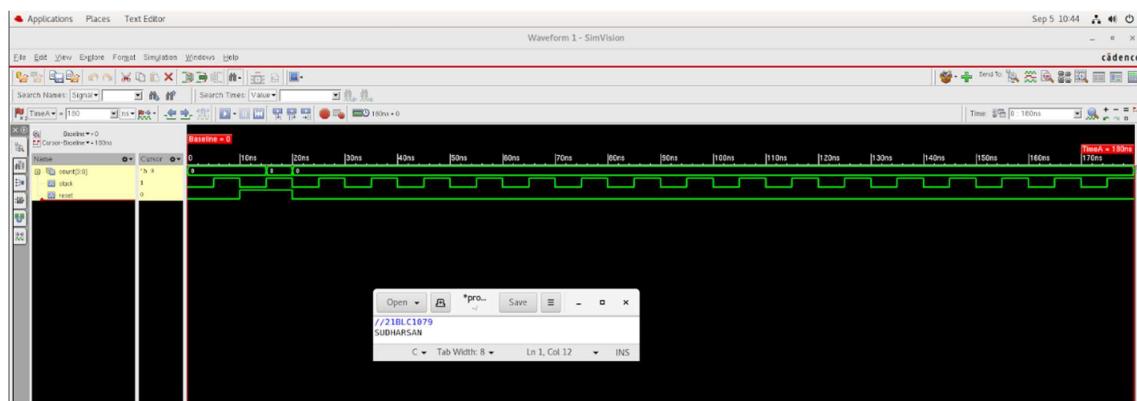
- **D FF having synchronous load and synchronous reset**

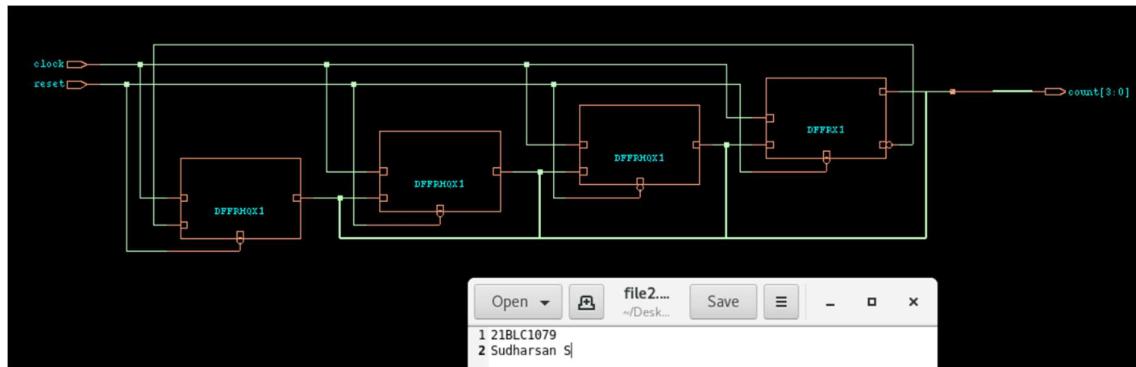


- Parameterized binary and gray counter

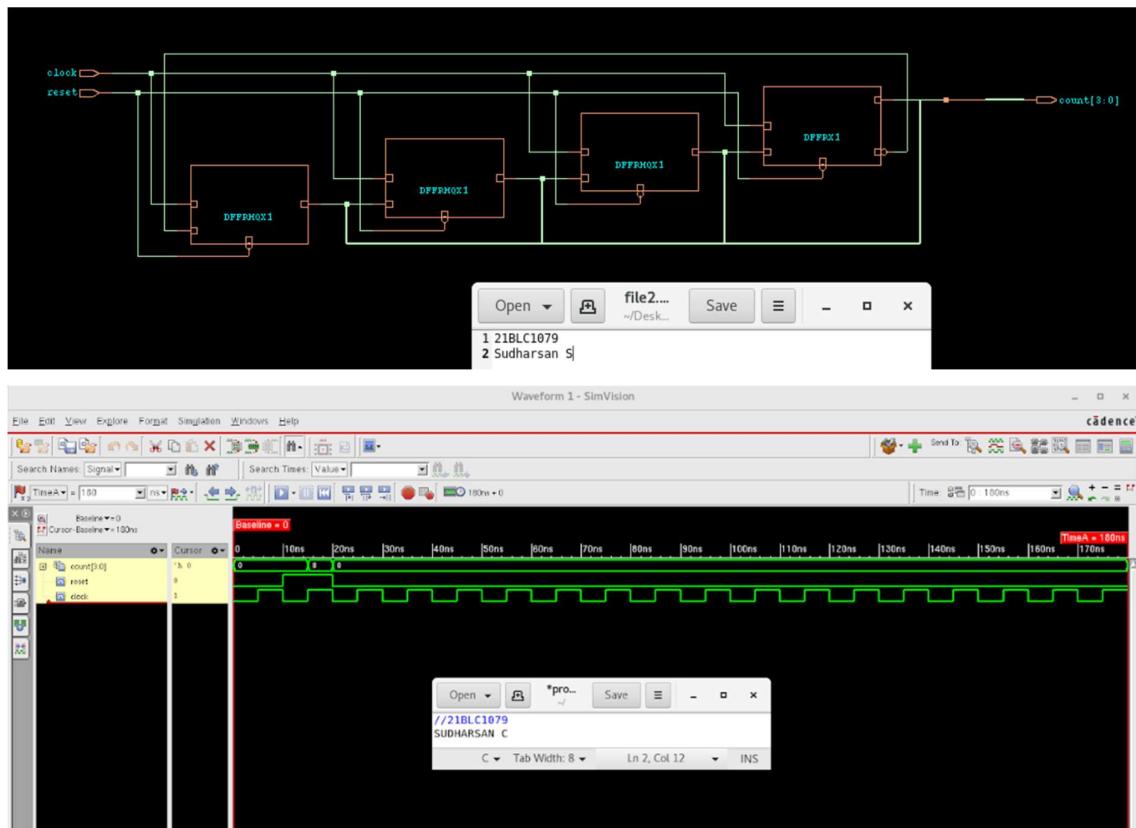


- **Four bit Ring Counter**





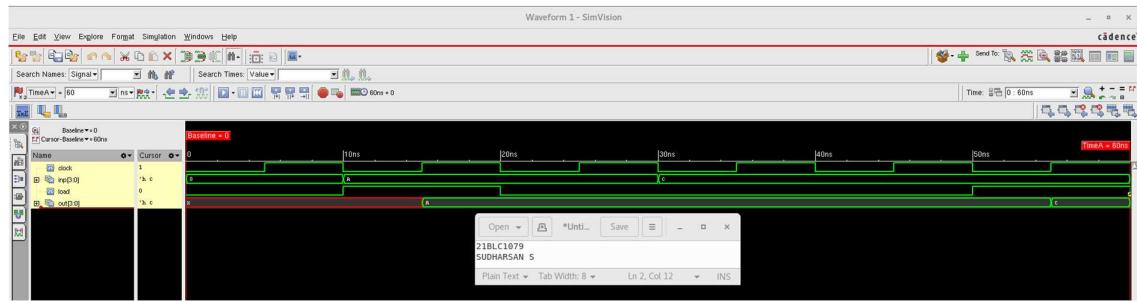
- Four bit Johnson Counter



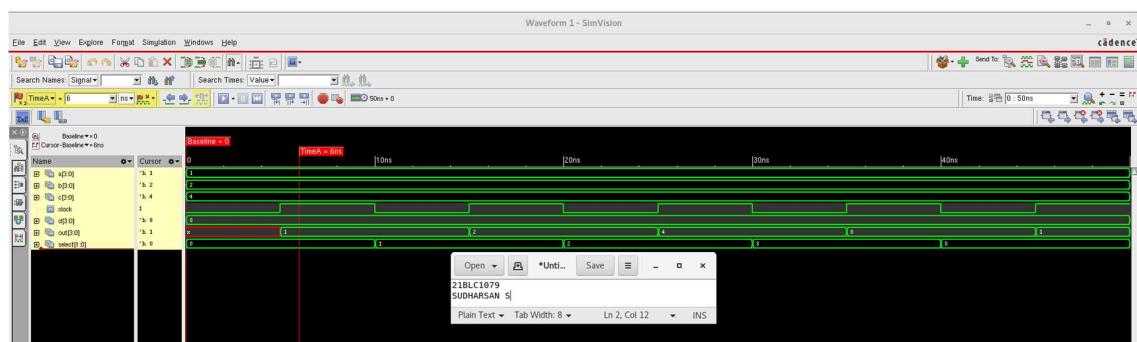
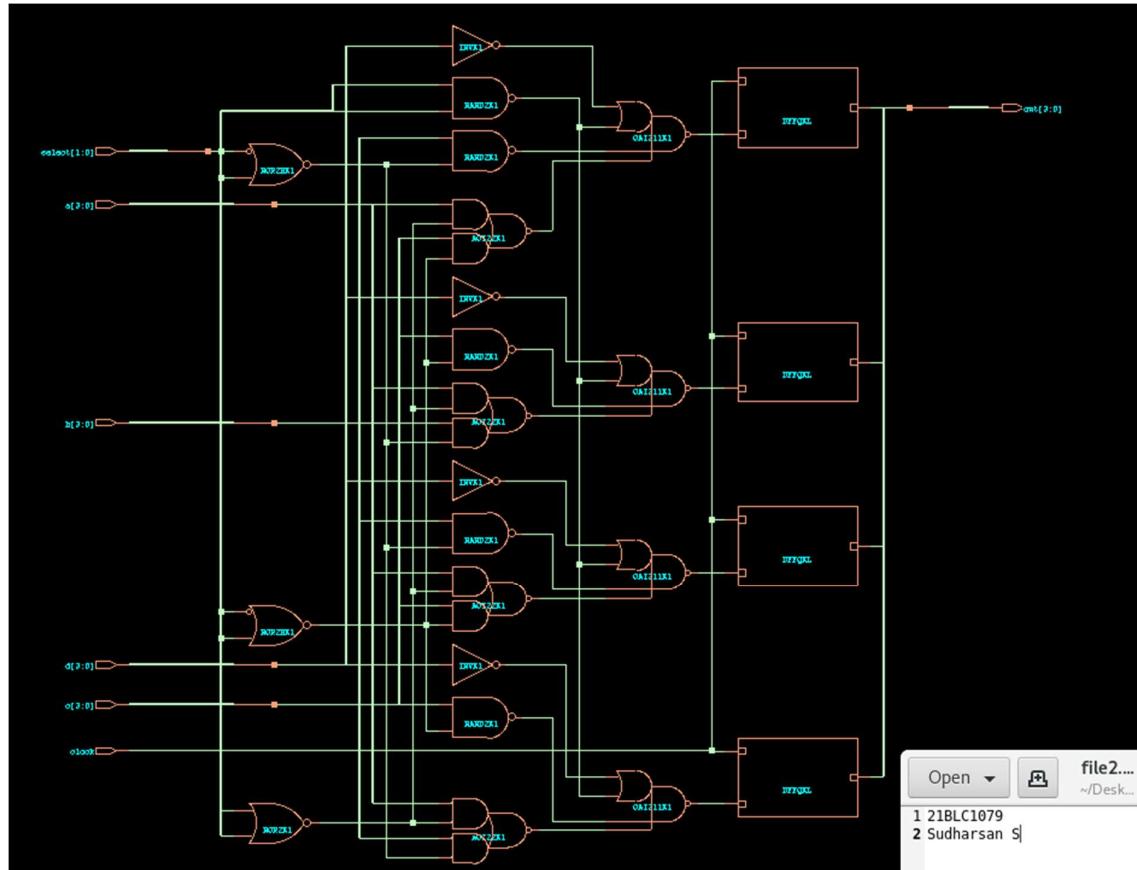
- Four bit BCD up-down counter



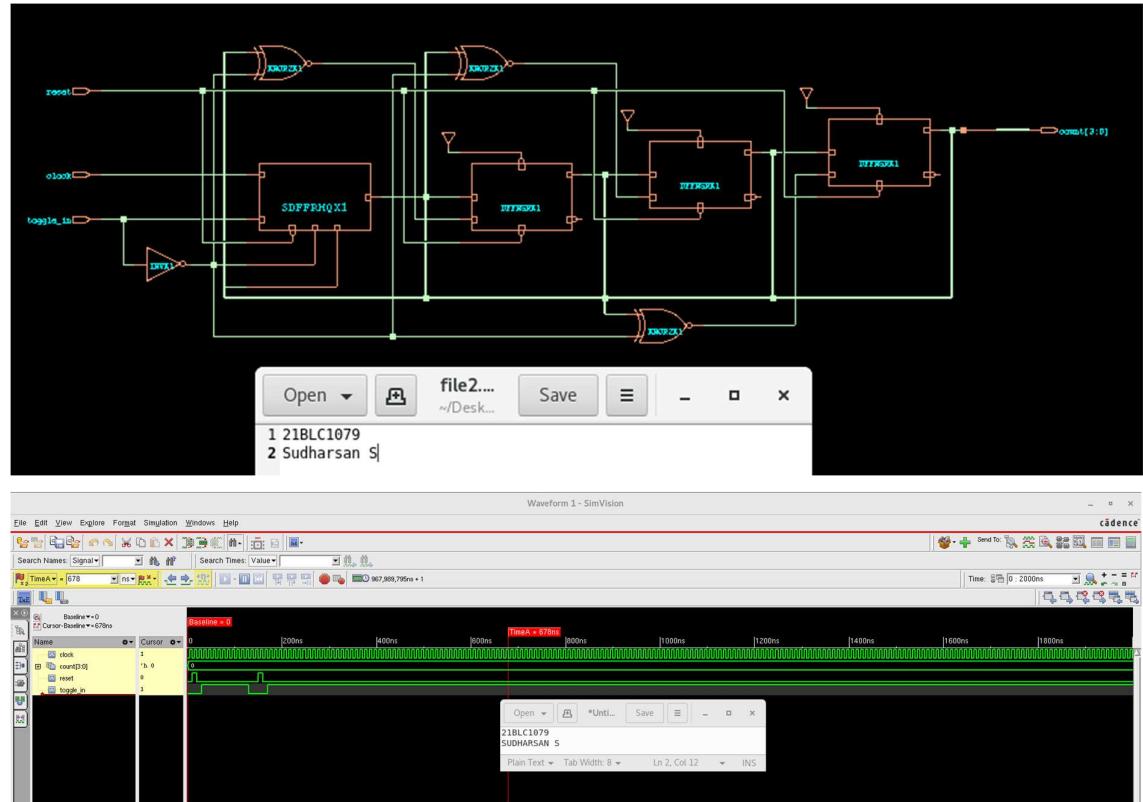
- 4 bit PIPO register



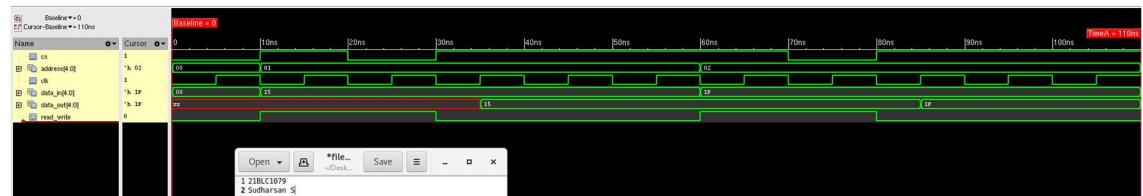
- 4:1 Mux having registered output



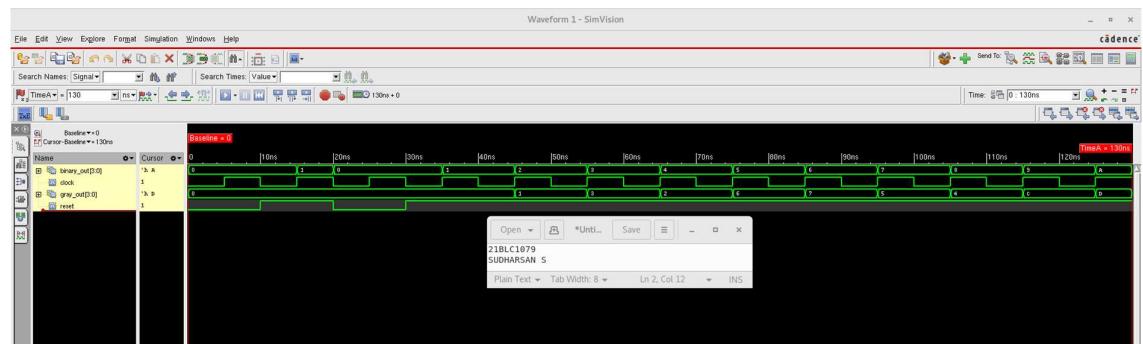
- 4-bit ripple up counter



- **Read write Memory**



- **Parameterized Read Write Memory used in the FIFO having 8 location depth**



3) Timing Constraint File

- **Half Adder**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_output_delay -max 1.0 [get_ports "cout"]
set_output_delay -max 1.0 [get_ports "sum"]
```

- **Full Adder**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "cin"]
set_output_delay -max 1.0 [get_ports "cout"]
set_output_delay -max 1.0 [get_ports "sum"]
```

- **Half subtractor**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_output_delay -max 1.0 [get_ports "diff"]
set_output_delay -max 1.0 [get_ports "borrow"]
```

- **Full subtractor**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "cin"]
set_output_delay -max 1.0 [get_ports "diff"]
set_output_delay -max 1.0 [get_ports "borrow"]
```

- **4 bit full adder**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "c"]
set_output_delay -max 1.0 [get_ports "sum"]
set_output_delay -max 1.0 [get_ports "carry"]
```

- **4 bit full subtractor**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "c"]
set_output_delay -max 1.0 [get_ports "difference"]
set_output_delay -max 1.0 [get_ports "borrow"]
```

- **4 bit adder and subtractor**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "add"]
set_output_delay -max 1.0 [get_ports "o"]
```

- **Subtraction using 2s complement addition**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_output_delay -max 1.0 [get_ports "difference"]
set_output_delay -max 1.0 [get_ports "borrow"]
```

- **4 bit adder and subtractor**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "add"]
set_output_delay -max 1.0 [get_ports "o"]
```

- **Parity detector**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "p"]
set_output_delay -max 1.0 [get_ports "o"]
```

- **Binary to gray code converter**

```
set_output_delay -max 1.0 [get_ports "gray"]
set_input_delay -max 1.0 [get_ports "bin"]
```

- **Gray to binary converter**

```
set_input_delay -max 1.0 [get_ports "gray"]
set_output_delay -max 1.0 [get_ports "bin"]
```

- **2:1 Mux**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "sel"]
set_output_delay -max 1.0 [get_ports "out"]
```

- **2:1 Mux using if else**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "b"]
set_input_delay -max 1.0 [get_ports "sel"]
```

```
set_output_delay -max 1.0 [get_ports "out"]
```

- **2:1 Mux using case**

```
set_input_delay -max 1.0 [get_ports "a"]
```

```
set_input_delay -max 1.0 [get_ports "b"]
```

```
set_input_delay -max 1.0 [get_ports "sel"]
```

```
set_output_delay -max 1.0 [get_ports "out"]
```

- **4:1 Mux**

```
set_input_delay -max 1.0 [get_ports "a"]
```

```
set_input_delay -max 1.0 [get_ports "b"]
```

```
set_input_delay -max 1.0 [get_ports "c"]
```

```
set_input_delay -max 1.0 [get_ports "d"]
```

```
set_input_delay -max 1.0 [get_ports "s1"]
```

```
set_input_delay -max 1.0 [get_ports "s0"]
```

```
set_output_delay -max 1.0 [get_ports "out"]
```

- **4:1 Mux if else**

```
set_input_delay -max 1.0 [get_ports "a"]
```

```
set_input_delay -max 1.0 [get_ports "b"]
```

```
set_input_delay -max 1.0 [get_ports "c"]
```

```
set_input_delay -max 1.0 [get_ports "d"]
```

```
set_input_delay -max 1.0 [get_ports "s1"]
```

```
set_input_delay -max 1.0 [get_ports "s0"]
```

```
set_output_delay -max 1.0 [get_ports "out"]
```

- **4:1 Mux using case**

```
set_input_delay -max 1.0 [get_ports "a"]
```

```
set_input_delay -max 1.0 [get_ports "b"]  
set_input_delay -max 1.0 [get_ports "c"]  
set_input_delay -max 1.0 [get_ports "d"]  
set_input_delay -max 1.0 [get_ports "s1"]  
set_input_delay -max 1.0 [get_ports "s0"]  
set_output_delay -max 1.0 [get_ports "out"]
```

- **4:1 Mux using 2:1 Mux**

```
set_input_delay -max 1.0 [get_ports "a"]  
set_input_delay -max 1.0 [get_ports "b"]  
set_input_delay -max 1.0 [get_ports "c"]  
set_input_delay -max 1.0 [get_ports "d"]  
set_input_delay -max 1.0 [get_ports "s1"]  
set_input_delay -max 1.0 [get_ports "s0"]  
set_output_delay -max 1.0 [get_ports "out"]
```

- **Addition and subtraction using if else**

```
set_input_delay -max 1.0 [get_ports "a"]  
set_input_delay -max 1.0 [get_ports "b"]  
set_input_delay -max 1.0 [get_ports "control"]  
set_output_delay -max 1.0 [get_ports "o1"]  
set_output_delay -max 1.0 [get_ports "o2"]
```

- **3:8 Decoder**

```
set_input_delay -max 1.0 [get_ports "a"]  
set_output_delay -max 1.0 [get_ports "b"]
```

- **1:2 Decoder using case**

```
set_input_delay -max 1.0 [get_ports "a"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **1:2 Decoder having enable**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "enable"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **2:4 Decoder using enable**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "enable"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **2:4 Decoder using enable and case**

```
set_input_delay -max 1.0 [get_ports "a"]
set_input_delay -max 1.0 [get_ports "enable"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **2:4 Decoder with continuous assignment**

```
set_input_delay -max 1.0 [get_ports "a"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **Decoder using shift operator**

```
set_input_delay -max 1.0 [get_ports "a"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **4:2 Encoder**

```
set_input_delay -max 1.0 [get_ports "a"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **4:2 Priority Encoder**

```
set_input_delay -max 1.0 [get_ports "a"]
set_output_delay -max 1.0 [get_ports "b"]
```

- **Positive Level D latch**

```
set_input_delay -max 1.0 [get_ports "enable"]
set_input_delay -max 1.0 [get_ports "d"]
set_output_delay -max 1.0 [get_ports "q"]
```

- **Negative Level D Latch**

```
set_input_delay -max 1.0 [get_ports "enable"]
set_input_delay -max 1.0 [get_ports "d"]
set_output_delay -max 1.0 [get_ports "q"]
```

- **Positive Level Sensitive D Flip Flop**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
set_clock_transition -rise 0.1 [get_clocks "clock"]
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **Negative Level Sensitive D Flip Flop**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
set_clock_transition -rise 0.1 [get_clocks "clock"]
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **D FF having synchronous reset**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **D FF having asynchronous reset**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **D FF having synchronous load and asynchronous reset**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "load"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **D FF having synchronous load and synchronous reset**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "load"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clock"]
```

- **Three bit up counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clock"]
```

- **Three bit down counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clock"]
```

- **Three bit up down counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
```

```
set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "up_down"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clock"]
```

- **Two bit gray counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "inp"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clock"]
```

- **Parameterized binary and gray counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "gray_out"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "binary_out"] -clock [get_clocks "clock"]
```

- **Four bit Ring Counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
```

```
set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks] "clock"]
```

- **Four bit Johnson Counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks] "clock"]
```

- **Four bit BCD up-down counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "up"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clock"]
```

- **4 bit PIPO register**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]
```

```
set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "inp"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "load"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clock"]
```

- **SISO register**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "in"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clock"]
```

- **Right/Left Shift Register**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]

set_clock_transition -fall 0.1 [get_clocks "clock"]

set_clock_uncertainty 0.01 [get_ports "clock"]

set_input_delay -max 1.0 [get_ports "right_left"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]

set_input_delay -max 1.0 [get_ports "in"] -clock [get_clocks "clock"]

set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clock"]
```

- **4:1 Mux having registered output**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]

set_clock_transition -rise 0.1 [get_clocks "clock"]
```

```
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "c"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "d"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "select"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clock"]
```

- **4-bit ripple up counter**

```
create_clock -name clock -period 10 -waveform {0 5} [get_ports "clock"]
set_clock_transition -rise 0.1 [get_clocks "clock"]
set_clock_transition -fall 0.1 [get_clocks "clock"]
set_clock_uncertainty 0.01 [get_ports "clock"]
set_input_delay -max 1.0 [get_ports "toggle_in"] -clock [get_clocks "clock"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clock"]
set_output_delay -max 1.0 [get_ports "count"] -clock [get_clocks "clock"]
```

- **Read write Memory**

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "cs"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "read_write"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "data_in"] -clock [get_clocks "clk"]
```

```
set_input_delay -max 1.0 [get_ports "address"] -clock [get_clocks "clk"]
```

```
set_output_delay -max 1.0 [get_ports "data_out"] -clock [get_clocks "clk"]
```

- **Parameterized Read Write Memory used in the FIFO having 8 location depth**

```
create_clock -name write_clk -period 10 -waveform {0 5} [get_ports "write_clk"]
```

```
set_clock_transition -rise 0.1 [get_clocks "write_clk"]
```

```
set_clock_transition -fall 0.1 [get_clocks "write_clk"]
```

```
set_clock_uncertainty 0.01 [get_ports "write_clk"]
```

```
set_input_delay -max 1.0 [get_ports "write_data"] -clock [get_clocks "write_clk"]
```

```
set_input_delay -max 1.0 [get_ports "write_address"] -clock [get_clocks "write_clk"]
```

```
set_input_delay -max 1.0 [get_ports "read_address"] -clock [get_clocks "write_clk"]
```

```
set_input_delay -max 1.0 [get_ports "write_clk_en"] -clock [get_clocks "write_clk"]
```

```
set_input_delay -max 1.0 [get_ports "write_full"] -clock [get_clocks "write_clk"]
```

```
set_output_delay -max 1.0 [get_ports "read_data"] -clock [get_clocks "write_clk"]
```

4) Constraint File

- **Half Adder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl halfadder.v
elaborate
read_sdc halfadder.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > halfadder_gate.v
write_sdc > halfadder_sdc.sdc
report_timing >halfadder_time.rep
report_area > halfadder_area.rep
report_power > halfadder_power.rep
```

- **Full Adder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl fulladder.v
```

```
elaborate
```

```
read_sdc fulladder.g
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic
```

```
set_attribute syn_map_effort medium
```

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > fulladder_gate.v
```

```
write_sdc > fulladder_sdc.sdc
```

```
report_timing >fulladder_time.rep
```

```
report_area > fulladder_area.rep
```

```
report_power > fulladder_power.rep
```

- **Half subtractor**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl halfsubtractor.v
```

```
elaborate
```

```
read_sdc halfsubtractor.g
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > halfsubtractor_gate.v  
write_sdc > halfsubtractor_sdc.sdc  
report_timing >halfsubtractor_time.rep  
report_area > halfsubtractor_area.rep  
report_power > halfsubtractor_power.rep
```

- **Full subtractor**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl fullsubtractor.v  
elaborate  
read_sdc fullsubtractor.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt
```

```
gui_show  
write_hdl > fullsubtractor_gate.v  
write_sdc > fullsubtractor_sdc.sdc  
report_timing >fullsubtractor_time.rep  
report_area > fullsubtractor_area.rep  
report_power > fullsubtractor_power.rep
```

- **4 bit full adder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl fourbit_full_adder.v  
elaborate  
read_sdc fourbit_full_adder.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > fourbit_full_adder_gate.v  
write_sdc > fourbit_full_adder_sdc.sdc  
report_timing > fourbit_full_adder_time.rep  
report_area > fourbit_full_adder_area.rep
```

```
report_power > fourbit_full_adder_power.rep
```

- **4 bit full subtractor**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl fullsubtractor.v
```

```
elaborate
```

```
read_sdc fullsubtractor.sdc
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic
```

```
set_attribute syn_map_effort medium
```

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > fullsubtractor_gate.v
```

```
write_sdc > fullsubtractor_sdc.sdc
```

```
report_timing >fullsubtractor_time.rep
```

```
report_area > fullsubtractor_area.rep
```

```
report_power > fullsubtractor_power.rep
```

- **4 bit adder and subtractor**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl fourbit_full_adder.v
elaborate
read_sdc fourbit_full_adder.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > fourbit_full_adder_gate.v
write_sdc > fourbit_full_adder_sdc.sdc
report_timing > fourbit_full_adder_time.rep
report_area > fourbit_full_adder_area.rep
report_power > fourbit_full_adder_power.rep
```

- **Subtraction using 2s complement addition**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl subr_using2s_complement.v
elaborate
read_sdc subr_using2s_complement.g
set_attribute syn_generic_effort medium
syn_generic
```

```
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > subr_using2s_complement_gate.v  
write_sdc > subr_using2s_complement_sdc.sdc  
report_timing > subr_using2s_complement_time.rep  
report_area > subr_using2s_complement_area.rep  
report_power > subr_using2s_complement_power.rep
```

- **4 bit adder and subtractor**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl fourbit_full_adder.v  
elaborate  
read_sdc fourbit_full_adder.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show
```

```
write_hdl > fourbit_full_adder_gate.v  
write_sdc > fourbit_full_adder_sdc.sdc  
report_timing > fourbit_full_adder_time.rep  
report_area > fourbit_full_adder_area.rep  
report_power > fourbit_full_adder_power.rep
```

- **Parity detector**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl paritydetector.v  
elaborate  
read_sdc paritydetector.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > paritydetector_gate.v  
write_sdc > paritydetector_sdc.sdc  
report_timing > paritydetector_time.rep  
report_area > paritydetector_area.rep  
report_power > paritydetector_power.rep
```

- **Binary to gray code converter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl binarytogram.v
elaborate
read_sdc binarytogram.sdc
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > binarytogram_gate.v
write_sdc > binarytogram_sdc.sdc
report_timing >binarytogram_time.rep
report_area > binarytogramarea.rep
report_power > binarytogram_power.rep
```

- **Gray to binary converter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl graytobinary.v
```

elaborate

read_sdc graytobinary.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > graytobinary_gate.v

write_sdc > graytobinary_sdc.sdc

report_timing >graytobinary_time.rep

report_area > graytobinaryarea.rep

report_power > graytobinary_power.rep

- **2:1 Mux**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl twomux.v

elaborate

read_sdc twomux.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > twomux_gate.v
```

```
write_sdc > twomux_sdc.sdc
```

```
report_timing > twomux_time.rep
```

```
report_area > twomux_area.rep
```

```
report_power > twomux_power.rep
```

- **2:1 Mux using if else**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl twomuxifelse.v
```

```
elaborate
```

```
read_sdc twomuxifelse.g
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic
```

```
set_attribute syn_map_effort medium
```

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > twomuxifelse_gate.v
```

```
write_sdc > twomuxifelse_sdc.sdc  
report_timing > twomuxifelse_time.rep  
report_area > twomuxifelse_area.rep  
report_power > twomuxifelse_power.rep
```

- **2:1 Mux using case**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl twomuxcase.v  
elaborate  
read_sdc twomuxcase.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > twomuxcase_gate.v  
write_sdc > twomuxcase_sdc.sdc  
report_timing > twomuxcase_time.rep  
report_area > twomuxcase_area.rep  
report_power > twomuxcase_power.rep
```

- **4:1 Mux**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl fourmux.v
elaborate
read_sdc fourmux.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > fourmux_gate.v
write_sdc > fourmux_sdc.sdc
report_timing > fourmux_time.rep
report_area > fourmux_area.rep
report_power > fourmux_power.rep
```

- **4:1 Mux if else**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl fourmuxifelse.v
```

elaborate

read_sdc fourmuxifelse.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > fourmuxifelse_gate.v

write_sdc > fourmuxifelse_sdc.sdc

report_timing > fourmuxifelse_time.rep

report_area > fourmuxifelse_area.rep

report_power > fourmuxifelse_power.rep

- **4:1 Mux using case**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl fourmuxcase.v

elaborate

read_sdc fourmuxcase.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

```
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > fourmuxcase_gate.v  
write_sdc > fourmuxcase_sdc.sdc  
report_timing > fourmuxcase_time.rep  
report_area > fourmuxcase_area.rep  
report_power > fourmuxcase_power.rep
```

- **4:1 Mux using 2:1 Mux**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl fourmuxtwomux.v  
elaborate  
read_sdc fourmuxtwomux.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > fourmuxtwomux_gate.v
```

```
write_sdc > fourmuxtwomux_sdc.sdc  
report_timing >fourmuxtwomux_time.rep  
report_area > fourmuxtwomux_area.rep  
report_power > fourmuxtwomux_power.rep
```

- **Addition and subtraction using if else**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl addsubifelse.v  
elaborate  
read_sdc addsubifelse.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > addsubifelse_gate.v  
write_sdc > addsubifelse_sdc.sdc  
report_timing >addsubifelse_time.rep  
report_area > addsubifelse_area.rep  
report_power > addsubifelse_power.rep
```

- **3:8 Decoder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl threetoeightdecoder.v
elaborate
read_sdc threetoeightdecoder.sdc
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > threetoeightdecoder_gate.v
write_sdc > threetoeightdecoder_sdc.sdc
report_timing > threetoeightdecoder_time.rep
report_area > threetoeightdecoder_area.rep
report_power > threetoeightdecoder_power.rep
```

- **1:2 Decoder using case**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl onetotwodecoder.v
elaborate
```

```
read_sdc onetotwodecoder.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > onetotwodecoder_gate.v  
write_sdc > onetotwodecoder_sdc.sdc  
report_timing > onetotwodecoder_time.rep  
report_area > onetotwodecoder_area.rep  
report_power > onetotwodecoder_power.rep
```

- **1:2 Decoder having enable**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl onetotwodecoderenable.v  
elaborate  
read_sdc onetotwodecoderenable.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map
```

```
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > onetotwodecoderenable_gate.v  
write_sdc > onetotwodecoderenable_sdc.sdc  
report_timing > onetotwodecoderenable_time.rep  
report_area > onetotwodecoderenable_area.rep  
report_power > onetotwodecoderenable_power.rep
```

- **2:4 Decoder using enable**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl twotofourdecoderenable.v  
elaborate  
read_sdc twotofourdecoderenable.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > twotofourdecoderenable_gate.v  
write_sdc > twotofourdecoderenable_sdc.sdc
```

```
report_timing > twotofourdecoderenable_time.rep
```

```
report_area > twotofourdecoderenable_area.rep
```

```
report_power > twotofourdecoderenable_power.rep
```

- **2:4 Decoder using enable and case**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl twotofourdecodercaseenable.v
```

```
elaborate
```

```
read_sdc twotofourdecodercaseenable.sdc
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic
```

```
set_attribute syn_map_effort medium
```

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > twotofourdecodercaseenable_gate.v
```

```
write_sdc > twotofourdecodercaseenable_sdc.sdc
```

```
report_timing > twotofourdecodercaseenable_time.rep
```

```
report_area > twotofourdecodercaseenable_area.rep
```

```
report_power > twotofourdecodercaseenable_power.rep
```

- **2:4 Decoder with continuous assignment**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl twotofourdecoderassign.v  
elaborate  
read_sdc twotofourdecoderassign.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > twotofourdecoderassign_gate.v  
write_sdc > twotofourdecoderassign_sdc.sdc  
report_timing > twotofourdecoderassign_time.rep  
report_area > twotofourdecoderassign_area.rep  
report_power > twotofourdecoderassign_power.rep
```

- **Decoder using shift operator**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl decoderusingshift.v  
elaborate  
read_sdc decoderusingshift.g
```

```
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > decoderusingshift_gate.v  
write_sdc > decoderusingshift_sdc.sdc  
report_timing > decoderusingshift_time.rep  
report_area > decoderusingshift_area.rep  
report_power > decoderusingshift_power.rep
```

- **4:2 Encoder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl fourtotoencoder.v  
elaborate  
read_sdc fourtotoencoder.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium
```

```
syn_opt  
gui_show  
write_hdl > fourtwoencoder_gate.v  
write_sdc > fourtwoencoder_sdc.sdc  
report_timing > fourtwoencoder_time.rep  
report_area > fourtwoencoder_area.rep  
report_power > fourtwoencoder_power.rep
```

- **4:2 Priority Encoder**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl priorityencoder.v  
elaborate  
read_sdc priorityencoder.sdc  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > priorityencoder_gate.v  
write_sdc > priorityencoder_sdc.sdc  
report_timing > priorityencoder_time.rep
```

report_area > priorityencoder_area.rep

report_power > priorityencoder_power.rep

- **Positive Level D latch**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl posdlatch.v

elaborate

read_sdc posdlatch.sdc

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > posdlatch_gate.v

write_sdc > posdlatch_sdc.sdc

report_timing > posdlatch_time.rep

report_area > posdlatch_area.rep

report_power > posdlatch_power.rep

- **Negative Level D Latch**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

```
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl negdlatch.v  
elaborate  
read_sdc negdlatch.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > negdlatch_gate.v  
write_sdc > negdlatch_sdc.sdc  
report_timing > negdlatch_time.rep  
report_area > negdlatch_area.rep  
report_power > negdlatch_power.rep
```

- **Positive Level Sensitive D Flip Flop**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl posdff.v  
elaborate  
read_sdc posdff.g  
set_attribute syn_generic_effort medium
```

```
syn_generic  
set_attribute syn_map_effort medium  
  
syn_map  
set_attribute syn_opt_effort medium  
  
syn_opt  
  
gui_show  
  
write_hdl > posdff_gate.v  
  
write_sdc > posdff_sdc.sdc  
  
report_timing > posdff_time.rep  
  
report_area > posdff_area.rep  
  
report_power > posdff_power.rep
```

- **Negative Level Sensitive D Flip Flop**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
  
set_attribute library slow_vdd1v0_basicCells.lib  
  
read_hdl negdff.v  
  
elaborate  
  
read_sdc negdff.g  
  
set_attribute syn_generic_effort medium  
  
syn_generic  
set_attribute syn_map_effort medium  
  
syn_map  
set_attribute syn_opt_effort medium  
  
syn_opt
```

```
gui_show  
write_hdl > negdff_gate.v  
write_sdc > negdff_sdc.sdc  
report_timing > negdff_time.rep  
report_area > negdff_area.rep  
report_power > negdff_power.rep
```

- **D FF having synchronous reset**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl synchresetdff.v  
elaborate  
read_sdc synchresetdff.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > synchresetdff_gate.v  
write_sdc > synchresetdff_sdc.sdc  
report_timing > synchresetdff_time.rep  
report_area > synchresetdff_area.rep
```

```
report_power > synchresetdff_power.rep
```

- **D FF having asynchronous reset**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl asynchresetdff.v
```

```
elaborate
```

```
read_sdc asynchresetdff.sdc
```

```
set_attribute syn_generic_effort medium
```

```
syn_generic
```

```
set_attribute syn_map_effort medium
```

```
syn_map
```

```
set_attribute syn_opt_effort medium
```

```
syn_opt
```

```
gui_show
```

```
write_hdl > asynchresetdff_gate.v
```

```
write_sdc > asynchresetdff_sdc.sdc
```

```
report_timing > asynchresetdff_time.rep
```

```
report_area > asynchresetdff_area.rep
```

```
report_power > asynchresetdff_power.rep
```

- **D FF having synchronous load and asynchronous reset**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
```

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
```

```
set_attribute library slow_vdd1v0_basicCells.lib
```

```
read_hdl loadsynchreset.v
elaborate
read_sdc loadsynchreset.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > loadsynchreset_gate.v
write_sdc > loadsynchreset_sdc.sdc
report_timing > loadsynchreset_time.rep
report_area > loadsynchreset_area.rep
report_power > loadsynchreset_power.rep
```

- **D FF having synchronous load and synchronous reset**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl loadasynchreset.v
```

elaborate

```
read_sdc loadasynchreset.g
set_attribute syn_generic_effort medium
syn_generic
```

```
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > loadasynchreset_gate.v  
write_sdc > loadasynchreset_sdc.sdc  
report_timing > loadasynchreset_time.rep  
report_area > loadasynchreset_area.rep  
report_power > loadasynchreset_power.rep
```

- **Three bit up counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl threebitupcounter.v  
elaborate  
read_sdc threebitupcounter.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show
```

```
write_hdl > threebitupcounter_gate.v  
write_sdc > threebitupcounter_sdc.sdc  
report_timing > threebitupcounter_time.rep  
report_area > threebitupcounter_area.rep  
report_power > threebitupcounter_power.rep
```

- **Three bit down counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_ydd1v0_basicCells.lib  
read_hdl threebitdowncounter.v  
elaborate  
read_sdc threebitdowncounter.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > threebitdowncounter_gate.v  
write_sdc > threebitdowncounter_sdc.sdc  
report_timing > threebitdowncounter_time.rep  
report_area > threebitdowncounter_area.rep  
report_power > threebitdowncounter_power.rep
```

- **Three bit up down counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl threebitupdowncounter.v  
elaborate  
read_sdc threebitupdowncounter.sdc  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > threebitupdowncounter_gate.v  
write_sdc > threebitupdowncounter_sdc.sdc  
report_timing > threebitupdowncounter_time.rep  
report_area > threebitupdowncounter_area.rep  
report_power > threebitupdowncounter_power.rep
```

- **Two bit gray counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl twobitgraycounter.v
```

elaborate

read_sdc twobitgraycounter.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > twobitgraycounter_gate.v

write_sdc > twobitgraycounter_sdc.sdc

report_timing > twobitgraycounter_time.rep

report_area > twobitgraycounter_area.rep

report_power > twobitgraycounter_power.rep

- **Parameterized binary and gray counter**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl parameterizedgrayandbinary.v

elaborate

read_sdc parameterizedgrayandbinary.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

```
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > parameterizedgrayandbinary_gate.v  
write_sdc > parameterizedgrayandbinary_sdc.sdc  
report_timing > parameterizedgrayandbinary_time.rep  
report_area > parameterizedgrayandbinary_area.rep  
report_power > parameterizedgrayandbinary_power.rep
```

- **Four bit Ring Counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl ringcounter.v  
elaborate  
read_sdc ringcounter.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > ringcounter_gate.v
```

```
write_sdc > ringcounter_sdc.sdc  
report_timing > ringcounter_time.rep  
report_area > ringcounter_area.rep  
report_power > ringcounter_power.rep
```

- **Four bit Johnson Counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl johnsoncounter.v  
elaborate  
read_sdc johnsoncounter.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > johnsoncounter_gate.v  
write_sdc > johnsoncounter_sdc.sdc  
report_timing > johnsoncounter_time.rep  
report_area > johnsoncounter_area.rep  
report_power > johnsoncounter_power.rep
```

- **Four bit BCD up-down counter**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl bcdropdown.v
elaborate
read_sdc bcdropdown.g
set_attribute syn_generic_effort medium
syn_generic
set_attribute syn_map_effort medium
syn_map
set_attribute syn_opt_effort medium
syn_opt
gui_show
write_hdl > bcdropdown_gate.v
write_sdc > bcdropdown_sdc.sdc
report_timing > bcdropdown_time.rep
report_area > bcdropdown_area.rep
report_power > bcdropdown_power.rep
```

- **4 bit PIPO register**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl pipo.v
elaborate
```

```
read_sdc pipo.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > pipo_gate.v

write_sdc > pipo_sdc.sdc

report_timing > pipo_time.rep

report_area > pipo_area.rep

report_power > pipo_power.rep
```

- **SISO register**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl siso.v

elaborate

read_sdc siso.g

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map
```

```
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > siso_gate.v  
write_sdc > siso_sdc.sdc  
report_timing > siso_time.rep  
report_area > siso_area.rep  
report_power > siso_power.rep
```

- **Right/Left Shift Register**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl left_right.v  
elaborate  
read_sdc left_right.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > left_right_gate.v  
write_sdc > left_right_sdc.sdc
```

report_timing >left_right_time.rep

report_area > left_right_area.rep

report_power > left_right_power.rep

- **4:1 Mux having registered output**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/

set_attribute library slow_vdd1v0_basicCells.lib

read_hdl registeredmux.v

elaborate

read_sdc registeredmux.sdc

set_attribute syn_generic_effort medium

syn_generic

set_attribute syn_map_effort medium

syn_map

set_attribute syn_opt_effort medium

syn_opt

gui_show

write_hdl > registeredmux_gate.v

write_sdc > registeredmux_sdc.sdc

report_timing > registeredmux_time.rep

report_area > registeredmux_area.rep

report_power > registeredmux_power.rep

- **4-bit ripple up counter**

set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/

```
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl rippleup.v  
elaborate  
read_sdc rippleup.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > rippleup_gate.v  
write_sdc > rippleup_sdc.sdc  
report_timing > rippleup_time.rep  
report_area > rippleup_area.rep  
report_power > rippleup_power.rep
```

- **Read write Memory**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl readwrite.v  
elaborate  
read_sdc readwrite.g
```

```
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > readwrite_gate.v  
write_sdc > readwrite_sdc.sdc  
report_timing > readwrite_time.rep  
report_area > readwrite_area.rep  
report_power > readwrite_power.rep
```

- **Parameterized Read Write Memory used in the FIFO having 8 location depth**

```
set_attribute init_lib_search_path /home/student/Desktop/21BLC1079/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BLC1079/rtl/  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl para_mem.v  
elaborate  
read_sdc para_mem.g  
set_attribute syn_generic_effort medium  
syn_generic  
set_attribute syn_map_effort medium  
syn_map  
set_attribute syn_opt_effort medium  
syn_opt  
gui_show  
write_hdl > para_mem_gate.v
```

```
write_sdc > para_mem_sdc.sdc  
report_timing > para_mem_time.rep  
report_area > para_mem_area.rep  
report_power > para_mem_power.rep
```