Design of a 2.4GHz Low Noise Amplifier

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***Abstract*—This work presents the design and analysis of a 2.4 GHz Low Noise Amplifier (LNA) using the CMOS 180nm technique optimized for high gain, low noise figure, and improved linearity. The proposed LNA is implemented using cascode and folded cascode topologies with inductive source degeneration to enhance impedance matching and noise performance. Additionally, Modified Derivative Superposition (MDS) is employed to improve linearity by suppressing third-order intermodulation distortion (IMD3). The design achieves a noise figure below 0.6 dB, open-loop gain exceeding 30 dB, and ensures stability across operating conditions. Performance metrics like IIP3, OIP3, and P1dB are analyzed to validate linearity, while S-parameters are examined to evaluate impedance matching, gain, and stability across the operating frequency. The simulation results demonstrate significant improvements in gain, noise performance, and power efficiency, making the proposed LNA a promising solution for modern wireless communication systems.**

***Index Terms*—Low Noise Amplifier, CMOS, Cascode Topology, Folded-Cascode LNA, Inductive Source Degenerated LNA, Modified Derivative Superposition, Linearity, Noise Figure, S-parameters**

I. Introduction

Low Noise Amplifiers (LNAs) serve as crucial components in wireless communication systems, directly impacting the sensitivity of the receiver and overall system performance. The primary function of LNAs is to amplify weak signals received from the antenna while minimizing noise contribution from subsequent circuit stages [14]. However, designing an LNA that simultaneously provides high gain, a low noise figure (NF), proper input-output impedance matching, and high linearity presents significant challenges due to trade-offs between circuit parameters [10].

The cascode structure is one of the most widely used LNA configurations due to its inherent advantages, such as increased gain and improved input-output isolation, which reduces the Miller effect [9]. Despite these benefits, conventional cascode LNAs exhibit a trade-off between gain and linearity [11]. To address this, this study proposes two LNA topologies: Cascode with Modified Derivative Superposition (MDS) and Folded Cascode with MDS, implemented in 180nm CMOS technology. The MDS technique enhances gain while improving linearity by distributing voltage stress across multiple stacked transistors [15].

Impedance matching is achieved using an inductor-capacitor (LC) network to optimize power transfer and minimize reflections, while source degeneration inductance is incorporated to enhance linearity and stability by controlling internal impedance [13]. Additionally, an active biasing technique ensures stable performance despite temperature and process variations [12]. One of the key challenges in LNA design is balancing gain and linearity. Higher gains often lead to reduced linearity due to increased distortion at higher power levels [16].

In this work, linearity enhancement techniques such as Derivative Superposition (DS) and Modified Derivation Superposition (MDS) are employed to achieve an optimal trade-off. Performance evaluation is conducted in terms of gain, noise figure, and stability factor (K), along with linearity metrics such as third-order input intercept point (IIP3) and 1 dB compression point (P1dB) [10].

A complete design methodology for 2.4 GHz CMOS LNAs is presented in this study, with a focus on comparing cascode-MDS and folded cascode-MDS architectures. Simulation results validate the proposed design approach by demonstrating balanced gain, linearity, and noise performance [11].

II. Linearity

An ideal amplifier should reproduce a scaled version of the input signal, a property known as linearity. In practice, perfect linearity is unachievable due to physical limitations, biasing, and power constraints [17]. As input strength increases, amplifiers deviate from ideal behavior, especially in high-frequency designs where parasitic effects in transistors, PCB traces, and packaging cause further non-linearity and distortion [18].

This non-linearity affects signal integrity and system performance [3], causing issues such as Gain Compression, Harmonic Distortion, Clipping, and Intermodulation Distortion (IMD) [**?**]. IMD results from multiple signal interactions, creating additional unwanted signals that disrupt operation.

P1dB is the point where gain drops by 1 dB from the linear value due to the active device entering saturation, leading to signal compression and distortion [22] [23]. It marks the maximum usable output power before significant non-linearity occurs.

IP3 evaluates susceptibility to IMD when multiple signals are present. Third-order intermodulation products, particularly at (2f1 - f2) and (2f2 - f1), are problematic as they lie close to the original signals and are hard to filter out [3]. IP3 is a theoretical point where third-order product power intersects the extrapolated linear output. Though actual saturation occurs earlier, a higher IP3 indicates better linearity and distortion resistance [24]. Relationship between P1dB and IP3:

$$P_{1\text{dB}} \approx IIP_3 - 10\,\text{dB} \tag{1}$$

III. Methodology

The Third-order intermodulation distortion (IM3) occurs when signals with different frequencies, apart from the desired frequency, are amplified. The products of IM3 2f1 - f2 and 2f2 - f1 are close to the parent signal and thus reduces the performance of an LNA. The second-order intermodulation distortion is usually outside of the band of interest and therefore less important [2]. To cancel out IM3 of an LNA, Derivative Superposition technique is proposed [2] [3]. This proposed method consists of two parallel transistors which are biased in different regions of operations such that the third order derivative of transconductance of M1 and M2 are equal and opposite. Thus, reducing the third-order nonlinearity [5] [10]. For this specific VGS the circuit provides high value of IIP3 and 1 dB compression point [6]. However, DS technique is susceptible to second-order non linearity. To counter the effects for second order non-linearity an alternate technique is proposed known as Modified Derivative Superposition which improves the linearity of the LNA.

A. Architecture

Fig.1 shows the MDS technique proposed on a folded-cascode LNA[10]. M1 and M2 represent the parallel transistors (NMOS) configured in Common Source and Common Gate stages respectively, which is connected to a PMOS M3 forming a folded cascode LNA. M1 operates in moderate inversion region and M2 operates in strong inversion region. Lt and Ct contribute to the LC tank which is used to supply the bias current. The LC is realized to resonant at the desired frequency [6].
LC tuning can be expressed as:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

The inductor and capacitor at the input side and output side are used for input and output matching. Coupling capacitors are used at the input stage to block the DC signal and to allow AC signal. The nonlinear components in the incremental drain current is given by [10]

$$i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \tag{3}$$

where,

$$g_{m1} = \frac{\partial i_d}{\partial v_{gs}}, \quad g_{m2} = \frac{\partial^2 i_d}{2\partial v_{gs}^2}, \quad g_{m3} = \frac{\partial^3 i_d}{6\partial v_{gs}^3} \tag{4}$$

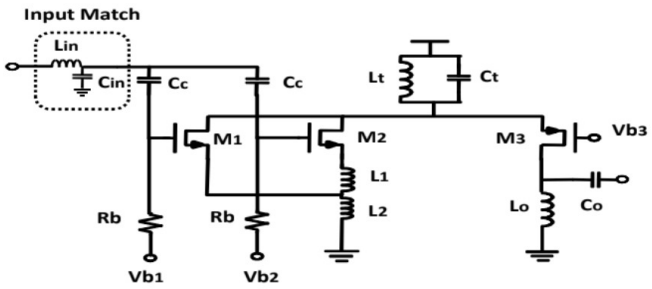

Fig.1: Folded Cascode LNA with MDS [10]

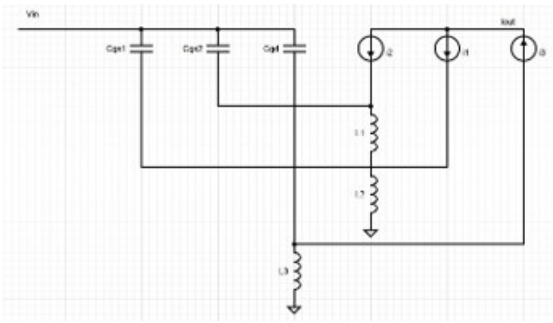

Fig.2: Small Signal Analysis

Impedance matching is significant for maximum power transfer and as reduction of signal reflections at the input and output of the LNA. In this work, impedance matching for both the input and output stage is done using L and C components. For the input matching, an LC network is used; and for the output matching, an LC tank circuit with an additional capacitor will be applied to act as an output matching circuit. For the input stage, the gate-source capacitance and series inductive reactance determines the impedance. The matching network consists of L and C components that will match the antenna impedance (typically 50ohm) to the input impedance of the LNA.
[10]Input matching is given by :

$$Z_{\text{in}} \approx j\omega L_g + \frac{1}{g_m} + j\omega L_s \tag{5}$$

Zin is the input impedance of the LNA
Lg is the gate inductance
gm is the transconductance of the input transistor
Ls is the source degeneration inductance

A source degeneration inductor (L) to improve the linearity and stability by controlling the internal impedance is also added.
The degenerative inductance, used to improve the noise performance and stability [7], is split into L1 and L2. By choosing the right value for L1, the contribution of second order derivative of transconductance to non-linearity is reduced. The third order derivative of transconductance of M1 and M2, gm31 and gm32 are equal but not opposite in phase. Instead, they are opposite to gm22 which is the second order derivative of transconductance. Thus, improving the linearity [6].

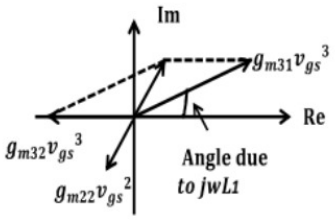

Fig.3: Nonlinearity cancellation [10]

B. Schematic

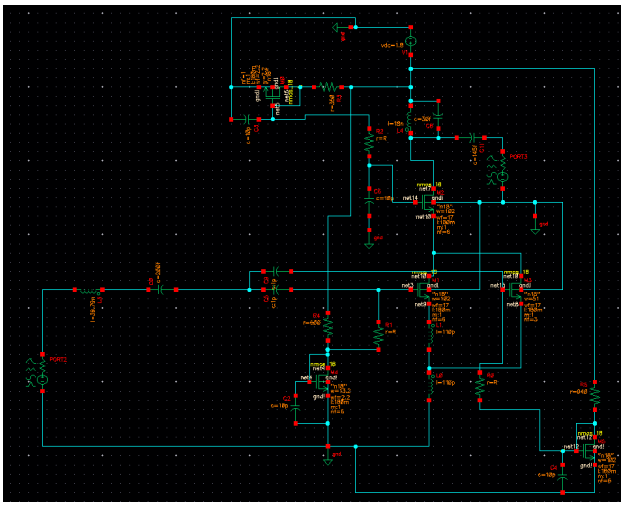

Fig.4: 180nm Schematic for Cascode LNA with MDS

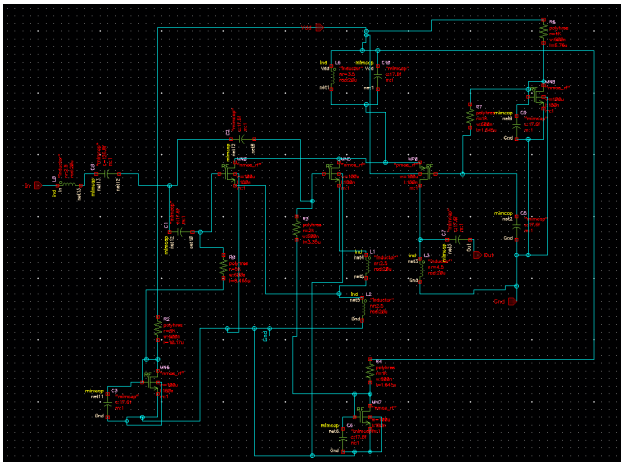

Fig.5: 180nm Schematic for Folded Cascode LNA with MDS

IV. Results

A cascode Low Noise Smplifier adapting MDS technique and A Folded Cascode Low Noise Amplifier have been implemented using the 180nm CMOS technology. The corresponding values for Gain, Stability, Noise Figure, IIP3 and P1dB are recorded.

A. Gain, Stability and Noise Figure

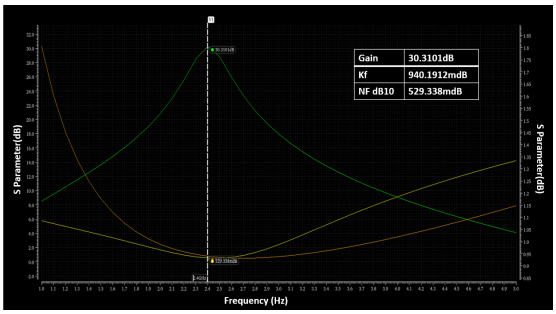

Fig.6: For Cascode

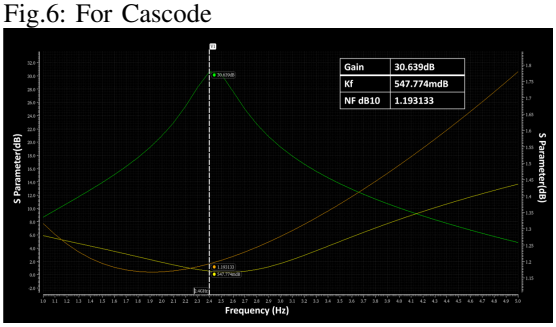

Fig.7: For Folded-Cascode

Comparison Table

Parameters	Cascode MDS	Folded-Cascode MDS
Gain(dB)	30.31	30.369
Noise Figure(mdB)	529.338	547.774
Stability Factor	0.9401	1.19313
P1dB(dBm)	-1.90672	-22.6776
IIP3(dBm)	9.20838	24.6909

Table.1 Comparative Analysis of Cascode MDS and Folded-Cascode MDS Architectures

From the table, we can conclude that Folded Cascode with MDS technqiue has better gain, stabilty and IIP3. However, there has to be some trade off to achieve this. Thus, the P1dB for the folded cascode circuit decreases.

V. Conclusion

In this work, we designed and analyzed a 2.4 GHz CMOS Low Noise Amplifier (LNA) that balances high gain, low noise, and improved linearity. By leveraging cascode and folded cascode topologies with the Modified Derivative Superposition (MDS) technique, we successfully minimized third-order intermodulation distortion (IMD3) while maintaining strong performance in impedance matching and noise reduction. Our simulations showed that the folded cascode architecture, combined with MDS, delivers higher gain and improved linearity (IIP3), although it comes with a slight trade-off in P1dB. Ultimately, this study contributes to the ongoing efforts to enhance LNA performance in modern wireless communication systems. The techniques explored

here could help improve receiver sensitivity and overall system efficiency, making them valuable for next-generation wireless networks.

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