IIT BHUBANESWAR

Wissenaire'21

Test Name: Analog Circuit Design

Test Duration: 150 minutes (2 hr 30 min)

Maximum points:100 points

Instructions:

1. Answer all the questions.

2.Answer all parts of a question together.

3.No question number before any solution will not be considered for evaluation.

4.There will be no negative marking.

5.Marking scheme for each part of every question is specified at end of the question.

6.Answer very concisely for the theory questions.

7.In the schematic diagram of Lt-spice please write you Name before you took screenshot and attach in the final report.

8.All the simulation graphs should be taken on a white background in Lt-spice. Do not use black background while taking screenshots of graphs at all.

9.In the circuit diagram please label all the required nodes.

10.Always plot different quantities of a question in different pane.

11.Please utilize the time properly. No extra time is provided and no one is allowed to appear for the exam again.

Q1: Design a circuit in LT-spice with the following characteristics:

- It should have 3 ideal Op-Amps.
- It should be given a single input source (Vin).
- It should have 3 outputs namely V1 V2 and V3, one at each Op-Amp.
- V1(jw)/Vin(jw) should be a high-pass response.
- V2(jw)/Vin(jw) should be a band pass response.
- V3(jw)/Vin(jw) should be a low-pass response.

Specifications:

- You should use only Resistors and capacitors and you are free to choose any value of R and C.
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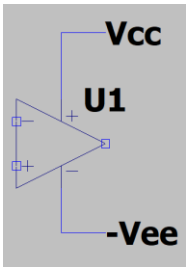


Take V_{CC}=+15V and V_{EE}=+15V while doing simulation in Lt-spice as shown above.

a) Attach the screenshot of the LT-spice schematic diagram of the constructed circuit? (**5 points**)

b) Attach the screenshots of all the high pass, low pass and band pass responses by performing a DC sweep simulation? (**15 points**)

c)The above-mentioned circuit is one of the filter circuits? Name it? (**1Point**)?

d)Write the formula of second order low pass, high pass and band pass responses? (**3Points**)

e) Why are the 3dB cut-off frequencies of low-pass response and high-pass response that you obtain from simulation are same? (**1Point**)

Hint: Out of three Op-Amp circuits that you cascade together, two are integrator circuits.

Q2. Using only **One Op-Amp**, devise a circuit to realize the following function utilizing three voltage inputs (V_1, V_2 and V_3)?

$$V(out)=5V_1-3V_2-7V_3$$

Specifications:

- Use universal Op-Amp(ideal).
- Take saturation voltages as V_{CC}=+15V and -V_{EE}=-15V.
- Take feedback resistance (R_f)=21kΩ.
- Take all the V1, V2 and V3 inputs as sinusoidal sources with frequency 100Hz and amplitudes 5V,3V,4V respectively.

a) Attach the screenshot of the LT-spice schematic diagram of the designed circuit? (**4 points)**

b) What are the gains of an inverting amplifier and non-inverting amplifier with source resistance R1 and feedback resistance Rf? (**2points**)

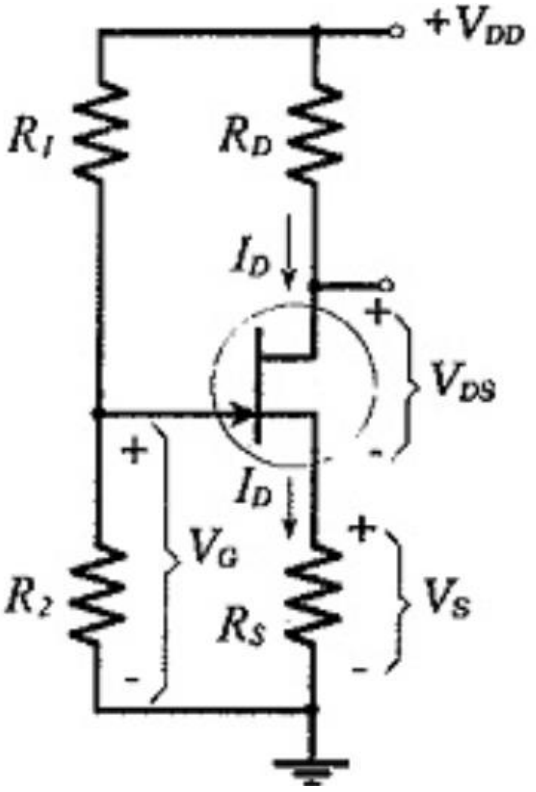
c)Attach the screenshot of plot containing V1, V2 and V3 by performing a transient simulation**?** (**3 points**)

d)The circuit designed is one of the types of amplifiers? Name it?

(**1 point**)

e) Attach the screenshot of plot containing (5V1-3V2-7V3) and V(out) **in different pane** by performing a transient simulation**?** (**10 points**)

Q3) Consider the NMOS circuit below:



Take V_{DD}=10V

R1=R2=10MΩ

R_D=R_s=6kΩ

V_t(threshold)=1V

μ_n Cox (w/L) =1mA/V^2

Specifications:

- Use ‘nmos4’ instead of inbuilt MOSFET ‘nmos’

- Name the nmos4 MOSFET as N_1u
- N_1u details can be provided in Spice directive as shown

```
.MODEL N_1u NMOS LEVEL  = 3
+ KP    = 1000E-6    VTO=1
```

- Length and width of N_1u may be left unspecified

Perform the simulation with given specifications and verify whether theoretical results are matching with experimental results.

a) Solve the above circuit to find V_G, V_D, V_s and I_D theoretically with the knowledge of working of NMOS? Attach the photocopy of solved problem? (**10 points**)

b) Attach the screenshot of schematic consisting designed circuit?

(**5 points**)

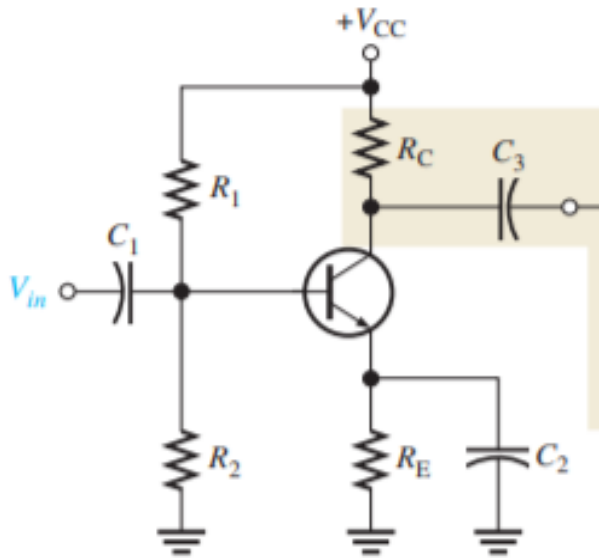
c)Attach the screenshot of voltages and currents obtained by performing DC Op simulation? (**5 points**)

d)Why the current through gate of MOSFET is zero? Explain briefly? (**2 points**)

e) Name the bias employed for the given circuit? **(1 point**)

f) What is the significance of threshold voltage in MOSFET? (**2 points**)

Q4) Design a common-emitter amplifier shown below with the following characteristics:



Specifications:

- Take V_{CC}=24V
- A_V(OC)= -100
- I_C=4mA
- V_{CE}=12V,
- I_C (sat)=8mA
- DC current gain(β)=100
- Take $R_2 \leq (\beta R_E)/10$

Perform the simulation with these specifications given above.

While doing the simulation with any model change the value of β to 100 from it's original value by imposing the model data onto spice-directive. Consider V_{BE}=0.7V as diode cut-in voltage for obtaining resistance values.

a) How you obtain the values of R_1 , R_2, R_c and R_E from the given specifications? Attach the scanned copy of the theoretical solution for this? (**10 points)**

b) Attach the screenshot of the LT-spice schematic diagram of the designed circuit? (**5 points)**

c) Attach the screenshot of voltages and currents obtained by performing DC Op simulation? (**5 points**)

d)How does capacitors behave in DC-operation? (**2 points**)

e) Comment on the specification given as "$R_2 \leq (\beta R_E)/10$"? (**3 points**)

f) How do you justify the statement "BJT is operating in active mode" from the simulation results? (**2 points**)

g) Draw the frequency response of a CE amplifier and explain why does it look like that? (**3 points**)

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