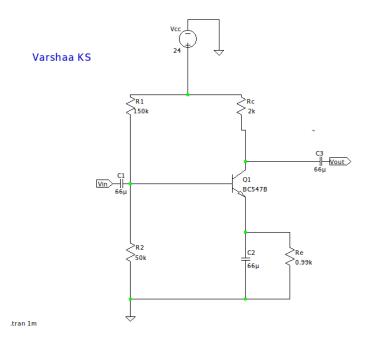
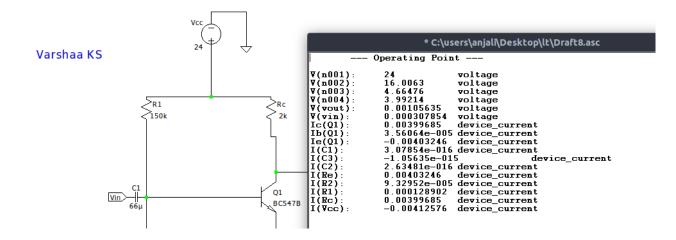
a) How you obtain the values of R1, R2, Rc and RE from the given specifications? Attach the scanned copy of the theoretical solution for this?

Select	ing the value of Rc = 2 K =>
Ulai	ing a equation from collector to smills
Vcc -	IcRc · Vie - IeRe : D
24-	4m×21×-12-4m×10] × RE = 0
	100
RE	- 0.991<
From	equation: IE - VBB - VBE
	RE+RB/B+1
Ass	uming VBB = 1 & VC C => R2 = 1 R,
	4 4
=> 1	B = 32510 => R1=150K and R2=50K

b)Attach the screenshot of the LT-spice schematic diagram of the designed circuit?



c)Attach the screenshot of voltages and currents obtained by performing DC Op simulation?



d) How does capacitors behave in DC-operation?

At DC operation, the frequency of the signal is 0 and hence the capacitor acts as open circuits.

e) Comment on the specification given as $R2 \le (\beta RE)/10$?

This is done so as to decrease Ib as much as possible. Because of this, the current through the collector is nearly identical to the current through the emitter.

f) How do you justify the statement "BJT is operating in active mode" from the simulation results?

From the operating point table we obtained via the simulation, we can see that Ic/lb (beta) is nearly 100. If the BJT was operating in the saturation mode, the beta value or Ic/lb will be far less than 100.

E) Draw the frequency response of a CE amplifier and explain why does it look like that?

At low frequencies of operation, the gain falls off due to the effects of the coupling and bypass capacitors. At high frequencies of operation, the gain falls due to internal parasitic capacitances of the BJT. There is a set of frequencies from FI to Fh where the effects of both of these capacitances are minimal and the gain remains more or less constant.

