ANALOG CIRCUIT DESIGN

WISSENAIRE

Simulation Report

And Solutions

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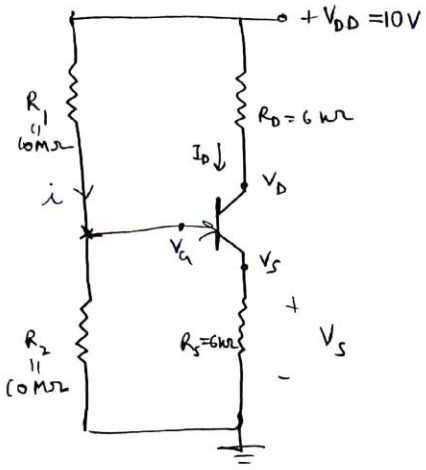
Solution No. 3

a) Solved the given circuit theoretically,



$V_t = 1V \qquad \mu_n C_{ox}\left(\frac{W}{L}\right) = 1mA/V^2$

In MOSFET, no current going in gate.

$$i = \frac{10}{10M\Omega + 10M\Omega} = 0.5\,\mu A.$$

$$V_G = V_{TH} = \frac{10}{2} = 5V.$$

$\Rightarrow \boxed{V_G = 5V}$

$V_D = 10 - I_D(6M\Omega) \qquad V_S = 0 + I_D \cdot (6M\Omega)$

assuming transistor to be in saturation,

$V_{GS} = 5 - I_D\,6M\Omega.$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 1mA/V^2 \times (4 - 6I_D)^2.$$

$\therefore I_D = 0.88mA$ and $0.5mA$.

also verify,

$V_S = 5.28$ when $I_D = 0.88mA$.

$V_{GS} = -0.28$

$\Rightarrow V_{GS} < V_t$ Cutoff

✗ wrong assumption

for $I_D = 0.88mA$ not possible.

Now, for $I_D = 0.5mA$

$\boxed{V_S = 3V}$

$\boxed{V_D = 7V}$

$V_{DS} = 4V \qquad V_{GS} = 2V$

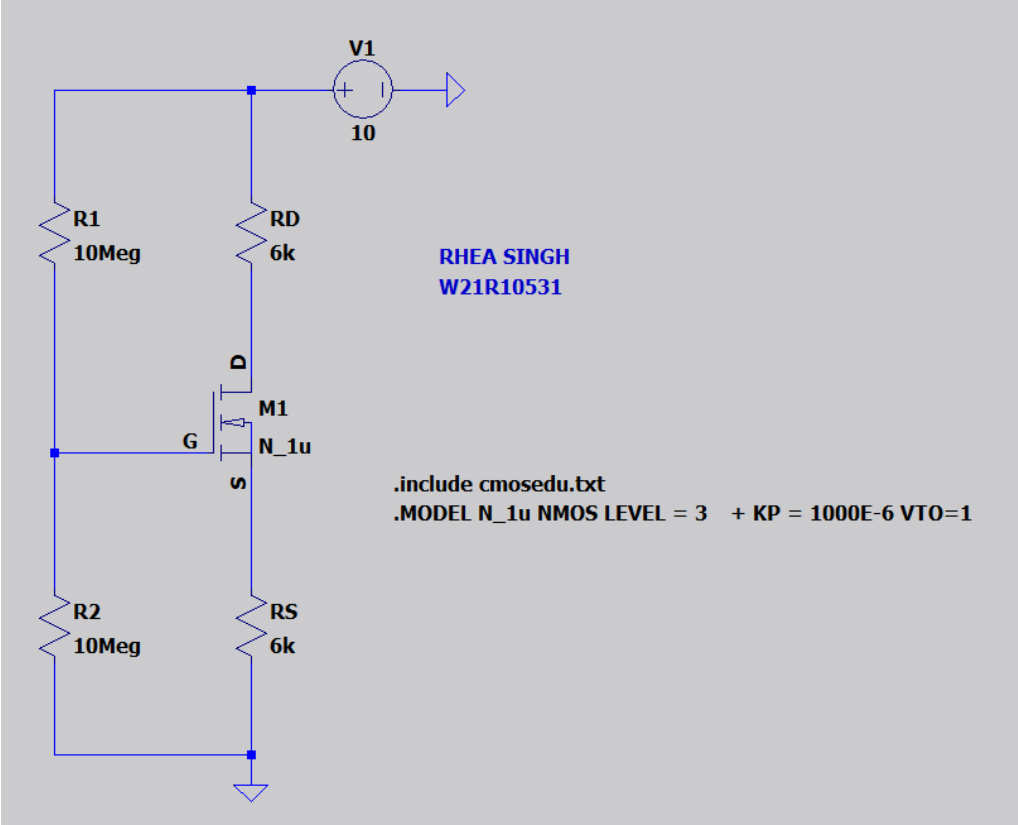
&

$V_{DS} > V_{GS} - V_t$

✓ correct assumption.

$\therefore \boxed{I_D = 0.5mA.}$

b) The screenshot of schematic consisting designed circuit :



c) The screenshot of voltages and currents obtained by performing DC Op simulation :

* C:\Users\rhea8\OneDrive\Desktop\Analog_Circuit_Design\Draft5.asc

--- Operating Point ---

V(d):	7	voltage
V(g):	5	voltage
V(s):	3	voltage
V(n002):	3.15305	voltage
V(n001):	10	voltage
Id(M1):	0.0005	device_current
Ig(M1):	0	device_current
Ib(M1):	1.9871e-016	device_current
Is(M1):	-0.0005	device_current
I(Rd):	0.0005	device_current
I(Rs):	0.0005	device_current
I(R2):	5e-007	device_current
I(R1):	5e-007	device_current
I(V1):	-0.0005005	device_current

d) The current through gate of MOSFET is zero because it is insulated with the oxide layer so the current cannot pass through it.
e) The bias employed for the given circuit is that the transistor is in saturation.
f) The significance of threshold voltage in MOSFET is that as threshold voltage is the minimum gate-to-source voltage VGS (th) that is needed to create a conducting path between the source and drain terminals so it is an important scaling factor to maintain power efficiency.