PBL PROJECT REPORT

DIGITAL ELECTRONICS AND LOGIC SYSTEM DESIGN

(PBEOT304)

PROJECT TITLE:

4-BIT ALU

TEAM MEMBERS:

GOWRIKRISHNA V [29]

GOWTHAM KRISHNA P K [30]

HARIKRISHNAN SANTHOSH [31]

HARIKRISHNA S [32]

SUDHEESH [64]

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COLLEGE OF ENGINEERING, TRIVANDRUM

SEMESTER: S3EL

ACADEMIC YEAR: 2025-26 (ODD)

Contents

BASIC INFORMATION

College Name	College of Engineering, Trivandrum
Department	Electrical and Electronics Engineering
Course	Digital Electronics and Logic System Design (PBEOT304)
Semester	S3EL
Academic Year	2025-26 (Odd)
Project Title	4-BIT ALU
Team Members	GOWRIKRISHNA V (29) GOWTHAM KRISHNA P K (30) HARIKRISHNAN SANTHOSH (31) HARIKRISHNA S (32) SUDHEESH (64)

Chapter 1

ABSTRACT

Problem Statement: Modern computing relies fundamentally on the Arithmetic Logic Unit (ALU) for all data processing. This project addressed the need to practically realize and demonstrate the core operational and architectural principles of a processor's central component, starting from the most basic digital building blocks.

Objectives: The primary objective was to design and implement a comprehensive 4-bit ALU using discrete digital components, specifically basic logic gates and flip-flops. The unit was designed to execute essential arithmetic operations (addition, subtraction, multiplication, and division) and foundational bitwise logical operations (AND, OR, XOR). The project also explicitly aimed to enhance the understanding of digital logic design by showcasing the internal structure of these data manipulation circuits.

Methodology: The design utilized a modular approach. Sub-circuits, such as the 4-bit ripple-carry adder (for addition and subtraction via two's complement) and dedicated multiplication/division logic, were constructed using AND, OR, and XOR gates. Flip-flops were integrated for control and state management. A control unit, built with multiplexers and decoders, governed the selection of the desired operation. Rigorous testing was employed via simulation to verify the functionality and accuracy of all implemented operations against the required truth tables.

Key Results: The project successfully delivered a functioning, modular 4-bit ALU prototype. The implementation validated core principles of digital logic design, demonstrating how simple gates are combined into complex, functional processing units capable of fundamental data manipulation. This work serves as an essential foundation for understanding CPU internal architecture.

Chapter 2

INTRODUCTION

The project is motivated by the fundamental role of the Arithmetic Logic Unit (ALU) in all digital computing. The ALU is essentially the "brain" of a Central Processing Unit (CPU) because it performs all the calculations and logical decisions needed to execute software instructions.

An ALU is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers. Understanding how an ALU works at the gate level provides invaluable insight into computer architecture and digital system design. This project aims to bridge theoretical knowledge with practical implementation by constructing a fully functional 4-bit ALU from basic digital components.

Chapter 3

OBJECTIVES

List the main objectives of your project:

1. **Design and Implementation:** To successfully design and construct a functional 4-bit ALU using fundamental digital components, including basic logic gates (AND, OR, NOT, XOR) and flip-flops (for control and state).
2. **Operational Capability:** To ensure the implemented ALU is capable of performing a defined set of fundamental operations, which must include:
   - **Arithmetic:** Addition, subtraction, multiplication, and division.
   - **Logic:** Bitwise AND, OR, and XOR.
3. **Demonstrate Working Principle:** To demonstrate the practical working of an ALU by showing how it manipulates 4-bit data inputs according to a control signal that selects the desired operation.
4. **Educational Outcome:** To enhance the understanding of digital logic design principles and showcase the internal architecture of complex data manipulation circuits, thereby providing a foundational understanding of CPU operation.

Chapter 4

METHODOLOGY

The project followed a four-stage, structured design methodology, ensuring that all functional and timing requirements were met before proceeding to physical construction.

4.1 Problem Analysis

The primary objective is to design and implement a comprehensive 4-bit Arithmetic Logic Unit (ALU) using discrete digital components (basic logic gates and flip-flops) to execute essential arithmetic and bitwise logical operations.

Key considerations during the problem analysis phase included:

- Identifying the required arithmetic operations (addition, subtraction, multiplication, division)
- Defining the logical operations (AND, OR, XOR)
- Determining the control signal requirements for operation selection
- Establishing the modular architecture for the ALU design

4.2 Circuit Design

The circuit design phase involved creating detailed schematics for each functional block of the ALU. The design was modular, consisting of:

- Arithmetic Unit (AU): Implementing addition, subtraction, multiplication, and division circuits
- Logic Unit (LU): Implementing bitwise AND, OR, and XOR operations
- Control Unit: Multiplexer-based operation selector
- Output Stage: Result propagation and flag generation

4.3 Simulation

Tools used: Logisim, Proteus, etc.

Before physical implementation, comprehensive simulation was performed to verify the logical correctness of the design. This phase included:

- Truth table verification for all operations
- Timing analysis to ensure proper signal propagation
- Edge case testing to identify potential design flaws
- Iterative refinement based on simulation results

4.4 Hardware Implementation

After successful verification through circuit simulation, the 4-bit Arithmetic Logic Unit (ALU) was realized as a physical, functional prototype. The implementation utilized a breadboard environment to facilitate easy assembly, modification, and debugging.

4.4.1 Components List

Sl. No	Component	Specification / Description
1		
2		
3		
4		
5		

Table 4.1: Components used in hardware implementation

4.5 Testing and Troubleshooting

Verification of circuit operation was performed through systematic testing procedures, including:

- Functional testing of individual modules
- Integration testing of the complete ALU
- Comparison of hardware results with simulation results
- Debugging and corrective measures for any discrepancies

Chapter 5

IMPLEMENTATION

5.1 Circuit Diagram

5.1.1 Simulation Diagram

ALU

MULTIPLIER

DIVIDER

5.2 Simulation Results

Add simulation screenshots and explain outcomes.

- Addition Operation Results
- Subtraction Operation Results
- Multiplication Operation Results
- Division Operation Results
- Logic Operations Results (AND, OR, XOR)

5.3 Hardware Implementation

Add photos and discuss results.

Chapter 6

RESULTS

The validation phase of the 4-bit ALU project involved comparing results obtained from two critical environments: software simulation (ideal logic) and physical hardware implementation (real-world performance). This comparison was essential for certifying the design's functional correctness and stability.

6.1 Simulation Result

The circuit was first simulated using Proteus Design Suite to validate the logical operation of each subsystem. Key findings include:

- All arithmetic operations (addition, subtraction, multiplication, division) functioned correctly according to their respective truth tables
- Logic operations (AND, OR, XOR) produced expected outputs for all input combinations
- Control signals properly selected the desired operation
- No timing violations or race conditions were observed

6.2 Hardware Results

The physical implementation validated the simulation results with the following observations:

- Functional correctness matched simulation for all tested input combinations
- Minor timing delays observed due to real-world propagation delays
- All operations executed reliably within acceptable tolerances

Chapter 7

INNOVATION AND APPLICATION

7.1 Unique Features

The project's innovation lies in the ground-up realization and comprehensive functional integration of the 4-bit ALU. It is unique because it:

1. Integrated the MULTIPLIER AND DIVIDER CIRCUIT which made the circuit much cost effective.
2. Employs a modular design (AU, LU, Control) that directly reflects the VLSI architecture used in commercial processors, providing a scalable blueprint.

7.2 Real-World Applications

The 4-bit ALU serves as a fundamental model for all digital electronics, with direct applications in:

- **Microprocessor Architecture:** It is the conceptual core of every CPU and GPU, teaching the basics of the data path, control logic, and flag management.
- **Embedded Systems:** Its principles are used in low-power microcontrollers and digital sensors.
- **Hardware Design Skills:** The process validates skills necessary for designing custom digital logic using Hardware Description Languages (HDL) for FPGAs and ASICs.

Chapter 8

CHALLENGES AND TROUBLESHOOTING

During the implementation phase, several challenges were encountered:

- **Component Availability:** Faced difficulties in sourcing specific IC components required for the implementation.
- **Timing Issues:** Initial circuit exhibited timing mismatches that were resolved through careful signal routing.
- **Debugging Complexity:** Identifying faults in the integrated circuit required systematic isolation testing.

Each challenge was systematically addressed through collaborative problem-solving and iterative design refinement.

Chapter 9

CONCLUSION

This project successfully demonstrated the design and implementation of a functional 4-bit Arithmetic Logic Unit using fundamental digital components. The key achievements include:

- Successful integration of arithmetic and logic operations in a single modular unit
- Validation of theoretical concepts through practical hardware implementation
- Enhanced understanding of digital logic design and computer architecture principles
- Development of troubleshooting and debugging skills in digital systems

Future Improvements:

- Expanding to 8-bit or 16-bit ALU for more complex operations
- Implementation using programmable logic devices (FPGAs)
- Addition of more advanced operations (shift, rotate, comparison)
- Integration of status flags (carry, overflow, zero, sign)
- Performance optimization for faster operation

This project serves as a foundation for understanding modern processor architectures and provides valuable hands-on experience in digital system design.

Chapter 10

REFERENCES

[1] Floyd, T. L. (2015). *Digital Fundamentals* (11th Edition). Pearson Education.

[2] Malvino, A. P., & Leach, D. P. (2017). *Digital Principles and Applications* (8th Edition). McGraw-Hill Education.

[3] Boylestad, R. L. (2016). *Electronic Devices and Circuit Theory* (11th Edition). Pearson Education.

[4] Datasheet – 74LS86 Quad 2-Input XOR Gate, Texas Instruments

- Used for bitwise XOR operations and as a core component in the Full Adder and Subtractor circuits.

[5] Datasheet – 74LS32 Quad 2-Input OR Gate, Texas Instruments

- Used for bitwise OR operations and general combinatorial logic.

[6] Datasheet – 74LS08 Quad 2-Input AND Gate, Texas Instruments

- Used for bitwise AND operations and general combinatorial logic.

[7] Datasheet – 74LS151 8-to-1 Line Data Selector/Multiplexer, Texas Instruments

- Essential for the ALU's output stage to select the result from the correct functional unit (Arithmetic or Logic).

[8] Datasheet – 74LS83 4-Bit Binary Full Adder, Texas Instruments

- If utilizing a pre-packaged adder IC, this datasheet details pinouts and ripple-carry functionality.

Chapter 11

APPENDIX

Include datasheets, code snippets, or additional figures if required.

11.1 Additional Circuit Diagrams

11.2 Truth Tables

11.3 Test Results

11.4 Component Datasheets