[Digital Logic] Homework 2
Sudarshana Jagadeeshi
CS 4341.206/502

Problem 1
I worked alone.

Problem 2
I used the textbook.

Problem 3
1.

w	x	y	z	f	index
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	x	2
0	0	1	1	0	3
0	1	0	0	0	4
0	1	0	1	x	5
0	1	1	0	0	6
0	1	1	1	x	7
1	0	0	0	x	8
1	0	0	1	0	9
1	0	1	0	1	10
1	0	1	1	0	11
1	1	0	0	x	12
1	1	0	1	1	13

1	1	1	0	x	14
1	1	1	1	1	15

k-map

VV wx >> yz	00	01	11	10
00	1 (0)	0 (1)	0 (3)	X (2)
01	0 (4)	X (5)	X (7)	0 (6)
11	X (12)	1 (13)	1 (15)	X (14)
10	X (8)	0 (9)	0 (11)	1 (10)

3.2

$w'x'y'z' + wx'yz' + wxz$

The two 1s in the corners are the first two terms. For the group of two, only the c changes.

3.3

There is one group of four, and 1 group of two.

$f' = (xz + w'xz')'$

$f= (x+z') (wx'z)$

3.4

There is one central group of four, and then the four corners

$xz+ x'z'$

3.5

There is one wrap group of 4. The other group of four is one the second row

$(w'x + x'z)'= (w+x')(xz)$

3.6

	Equation	#literals	#and	#or	#not	total
3.2	w’x’y’z’ + wx’yz’ + wxz	11	8	2	6	27
3.3	(x+z’) (wx’z)	5	3	1	2	11
3.4	xz+ x’z’	4	2	1	2	9
3.5	(w+x’)(xz)	4	2	1	1	8

3.7

Yes, the first two with w/o dont care were 27 and 11. This went down to 9 and 8 after doing the dont care.

Problem 4

4.1 Half-adder

Row_index	A_0	B_0		C_1	S_1
0	0	0		0	0
1	0	1		0	1
2	1	0		0	1
3	1	1		1	0

4.2 Full-adder

Row_index	A_0	B_0	C_0		C_1	S_1
0	0	0	0		0	0
1	0	0	1		0	1
2	0	1	0		0	1
3	0	1	1		1	0

4	1	0	0		0	1
5	1	0	1		1	0
6	1	1	0		1	0
7	1	1	1		1	1

4.4 One-hot decoder

Row_index	I_1	I_0		O_3	O_2	O_1	O_0
0	0	0		0	0	0	1
1	0	1		0	0	1	0
2	1	0		0	1	0	0
3	1	1		1	0	0	0

4.5 One-hot encoder

Row_index	I_3	I_2	I_1	I_0	Enable		O_0	O_1
0	0	0	0	1	1		0	0
1	0	0	1	0	1		0	1
2	0	1	0	0	1		1	0
3	1	0	0	0	1		1	1
4	x	x	x	x	0		x	x

4.6 4-bit Right Arbiter

Row_inde	I_3	I_2	I_1	I_0		O_0	O_1	O_2	O_3

x									
0	0	0	0	0		0	0	0	0
1	0	0	0	1		0	0	0	1
2	0	0	1	0		0	0	1	0
3	0	0	1	1		0	0	0	1
4	0	1	0	0		0	1	0	0
5	0	1	0	1		0	0	0	1
6	0	1	1	0		0	0	1	0
7	0	1	1	1		0	0	0	1
8	1	0	0	0		1	0	0	0
9	1	0	0	1		0	0	0	1
10	1	0	1	0		0	0	1	0
11	1	0	1	1		0	0	0	1
12	1	1	0	0		0	1	0	0
13	1	1	0	1		0	0	0	1
14	1	1	1	0		0	0	1	0
15	1	1	1	1		0	0	0	1

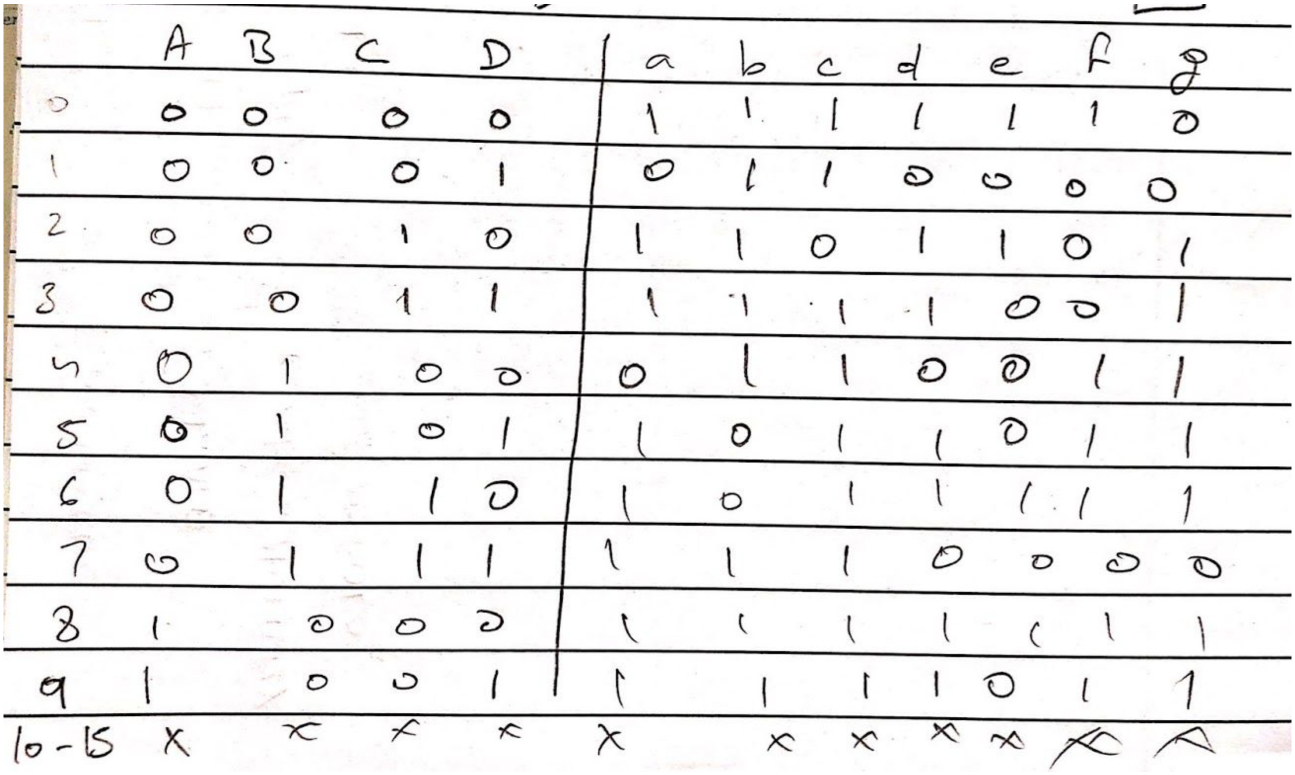
4.7 Mux

Row_index	Select_1	Select_0	Channel_1	Channel_2		d3	d2	d1	d0
0									
1									

2										
3										
4										
5										
6										
7										
8										

Problem 5

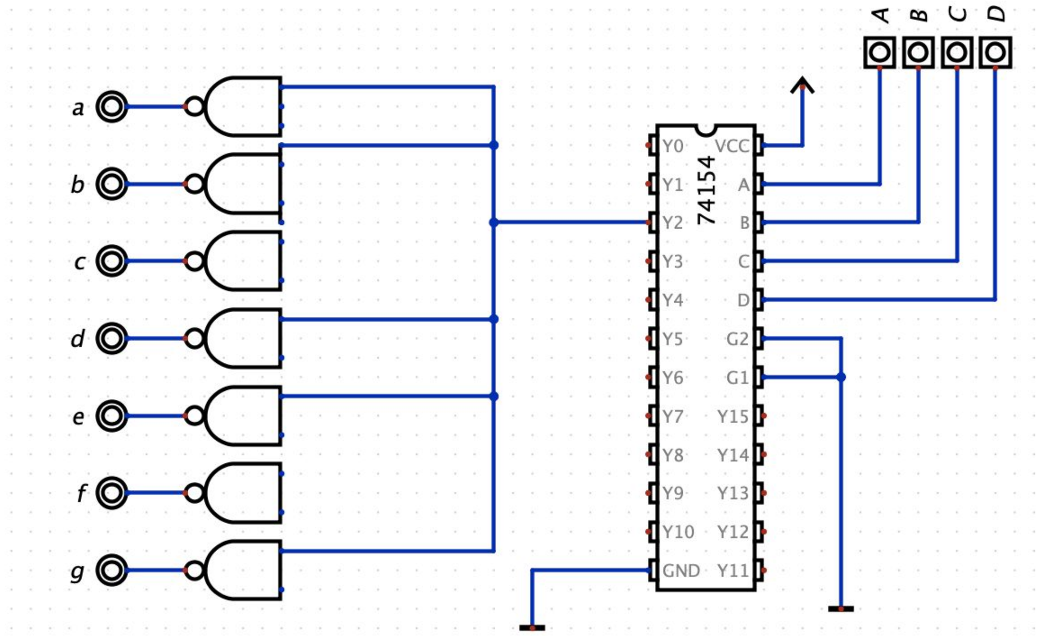
The circuit will be a 74154 decoder. There will be 4 inputs fed in, A B C and D. There will also be 7 NAND gates, each feeding into outputs a-g. Then wach Y0-Y9 will be sent to their respective NAND gates as follows:



	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10-15	X	x	x	x	X	x	x	x	x	x	x

Here, the Y2 output is sent to a, b, d, e, and g nand gates.

The circuit should look something like this, but I have only filled Y2 in.


a
b
c
d
e
f
g
A
B
C
D
74154
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
GND
VCC
A
B
C
D
G2
G1
Y15
Y14
Y13
Y12
Y11