EW-2 Report
Project 1: Audio Amplifier

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Note: All project files are saved in the **github repository**.

Aim & Objectives

1 Differential Amplifier- Pre-Gain Stage

Considering we have a maximum input of 10 mV amplitude, with $V_{CC} = \pm 5V$, we can get a maximum output voltage of $10\,\text{mV} \times 500 = 5V$. Hence, we aim for a gain of 500. The stage gains must be split as follows:

- Given the information that the CE Amplifier works for small signals, we aim to pass a signal $\leq 100\,\text{mV}$.
- In order to amplify a 10 mV signal to 100 mV, we need a gain of 10 in the differential amplifier.

Basic Operation

- Amplifies the difference between two input signals V_{in1} and V_{in2}.
- Comprises two matched BJTs (Q_1 and Q_2) sharing a common emitter via a constant current source.
- Output: Voltage difference between collector resistors (R_C).

Working Principle

- If $V_{in1} > V_{in2}$: Q_1 conducts more current, Q_2 less. This creates a voltage difference at the collectors.
- If $V_{in2} > V_{in1}$: Q_2 conducts more current, Q_1 less.
- If $V_{in1} = V_{in2}$ (common-mode input): Both transistors share the current equally, resulting in no differential output.

Noise Cancellation

Noise often affects both inputs similarly as a common-mode signal. The differential amplifier rejects this common-mode noise. It responds only to the difference between the inputs, effectively canceling the noise and amplifying the difference.

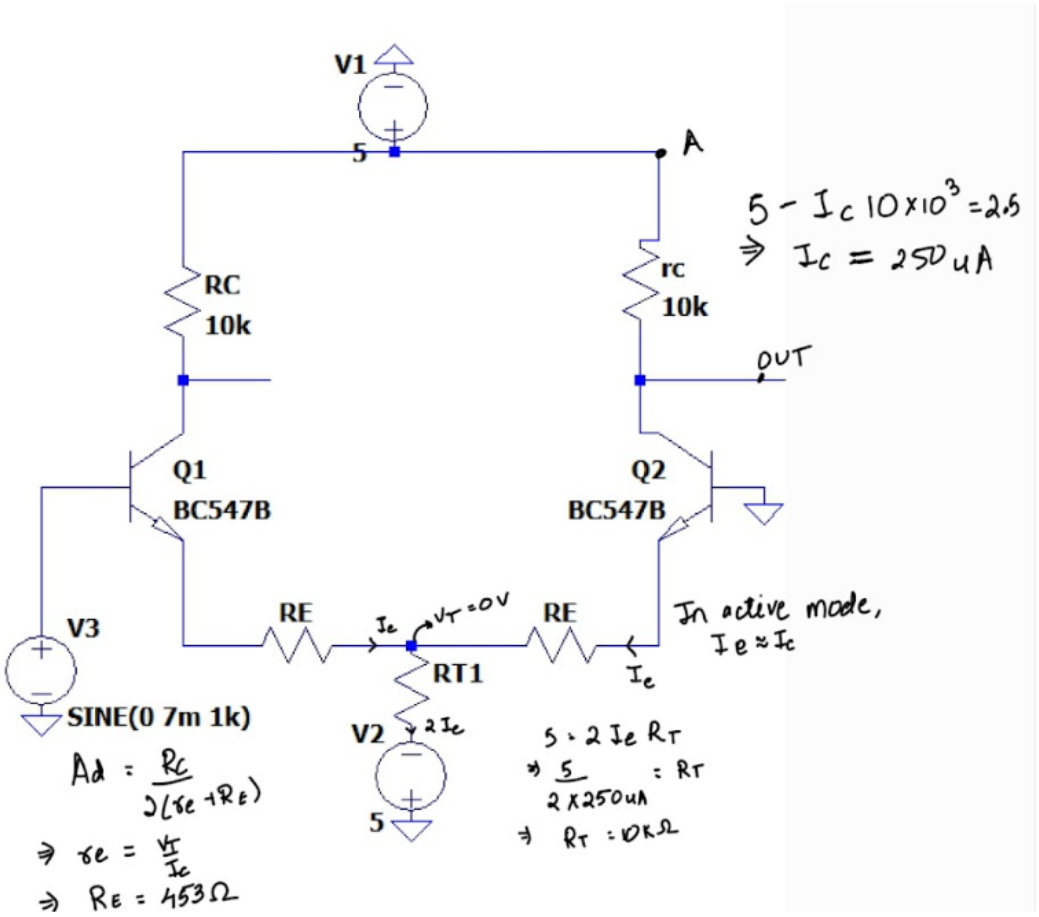

Figure 1: Rough Calculation, Differential Amplifier

Gain derivation of Differential Amplifier

$$\begin{aligned} i_{C1}(AC+DC) &= \frac{I}{2} + \Delta i_c \\ &= \frac{I}{2} + i_c \quad \text{(AC)} \\ &= \frac{I}{2} + g_m\,(V_{i2}) \\ &= \frac{I}{2} + g_m\,(-V_{id}) \\ &= \frac{I}{2} - \frac{g_m V_{id}}{2} \end{aligned}$$

$$\begin{aligned} v_{out} &= V_{CC} - I_{AC+DC} R_C \quad \text{(AC only taken)} \\ &= V_{CC} - \frac{I}{2} R_C + \frac{g_m V_{id} R_C}{2} \end{aligned}$$

$$\begin{aligned} \frac{V_{out}\ \text{(differential)}}{V_{in}} &= \frac{g_m V_{id} R_C}{2 V_{id}} \\ &= \frac{g_m R_C}{2} \end{aligned}$$

$$\text{Gain} = \frac{R_C}{2(r_e + R_E)}$$

where an external R_e is added with r_e.

Parameter Calculations

As we work with ±5 V, we make a few initial assumptions *(these shall be substantiated by our calculations).*

$$V_T = 0V$$

$$I_C \approx I_E \ (Active\ BJTs)$$

$$R_C = 10k\ \Omega$$

To calculate I_C, we simplify the following **Voltage Equation**:

$$V_{cc} - R_2 \cdot I_C = 2.5V$$

$$I_C \cdot 10k = (2.5 - 5) \cdot (-1)$$

$$I_C = 2.5 \cdot 10^{-4}$$

$$\therefore I_C = 250\mu A$$

As I_C is symmetric between both Emitter Branches,

$$I_T = 2 \cdot I_C$$

Using Ohm's Law (V = I· R):

$$5 = 2 \cdot I_C$$

$$5 = 5 \cdot 10^{-4} \cdot R_{tail}$$

$$\therefore R_{tail} = 10k\ \Omega$$

To account for **Non-Ideal Conditions**, we assume a gain $G_1 = 11$

$$A_d = \frac{R_C}{2 \cdot (r_e + R_E)}$$

$$A_d = \frac{R_C}{2 \cdot (r_e + R_E)}$$

$$r_e = \frac{V_T}{I_C}$$

Substituting $V_T = 26mV$ & $I_C = 2.5 \cdot 10^{-4}$:

$$r_e = 104\ \Omega$$

Solving for R_E:

$$11 = \frac{10 \cdot 10^3}{104 + R_E}$$

$$\therefore R_E = 453\ \Omega$$

To account for our assumption of $G_1 = 11, R_E = 453\ \Omega$ is considered as a starting value, after which it is lowered until the appropriate gain is achieved.
In conclusion, we arrive at $R = 354\ \Omega$ for the desired gain specification, i.e. $G_1 \approx 10$.

LTSpice Plots

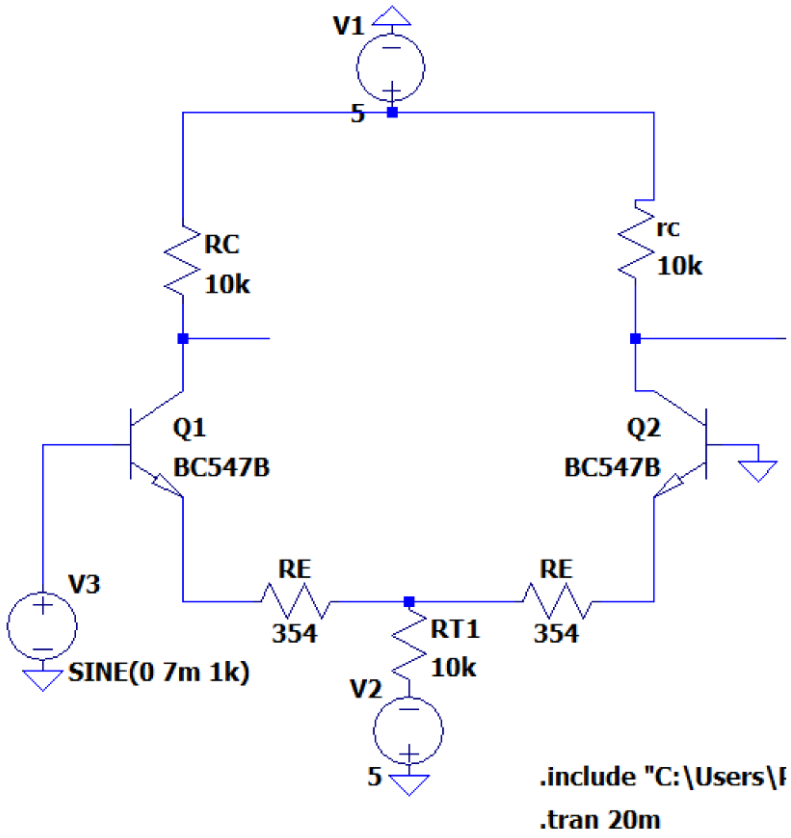

Figure 2: Entire Differential Amplifier Circuit

Input and output signals

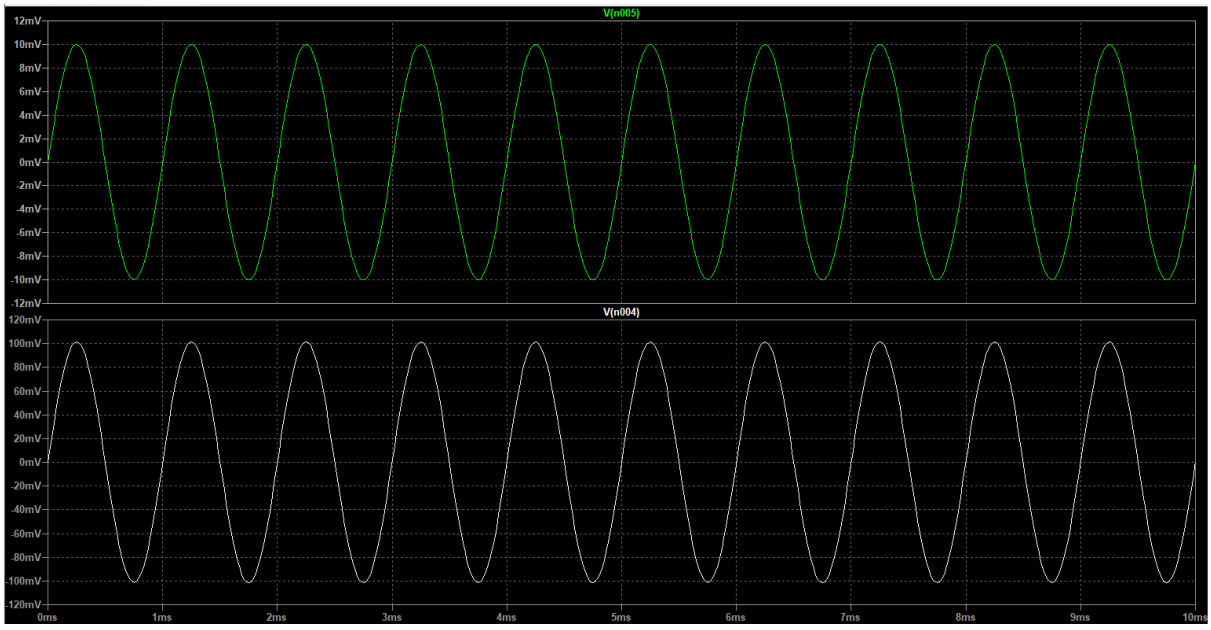

Figure 3: Plots of differential Amplifier

CMRR, Input & Output Resistances

- **Common Mode Rejection Ratio** is the ability of a differential amplifier to reject common-mode signals (signals present equally on both inputs) while amplifying differential signals (difference between inputs).
- **High CMRR** indicates better noise rejection and improved signal fidelity.

$$CMRR = 20 \cdot log(\frac{A_d}{A_c})$$

Calculating A_C, we give 10mV to both BJTs of our differential amplifier, we get the following gain:

$$A_c = 0.5$$

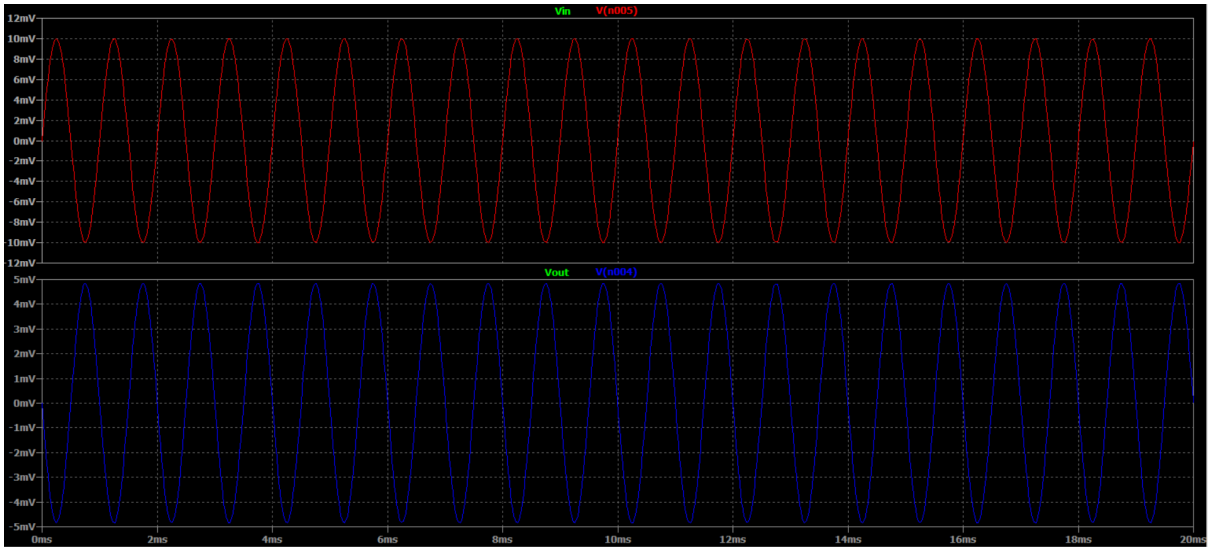

Figure 4: $A_C Relation$; V_{in} & V_{out}

Substituting Gains to get CMRR:

$$CMRR = 20 \cdot log(\frac{10}{0.5})$$

$$\therefore CMRR \approx 26$$

Input Resistance Grounding output and giving $V_{DC} = 1V$, we get current of 57μ A. $R_{in} = 17543\ \Omega$.

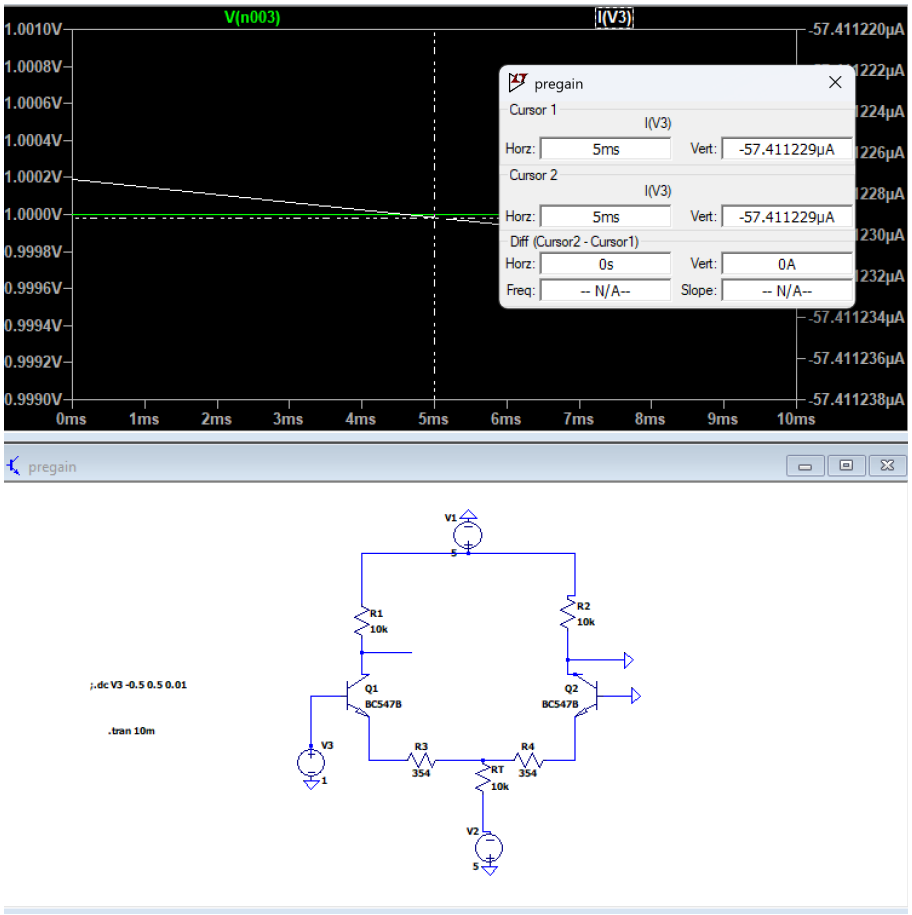

Figure 5: Rin

Output resistance We give output voltage 1V, and ground the input, we have resistance of 5kΩ.

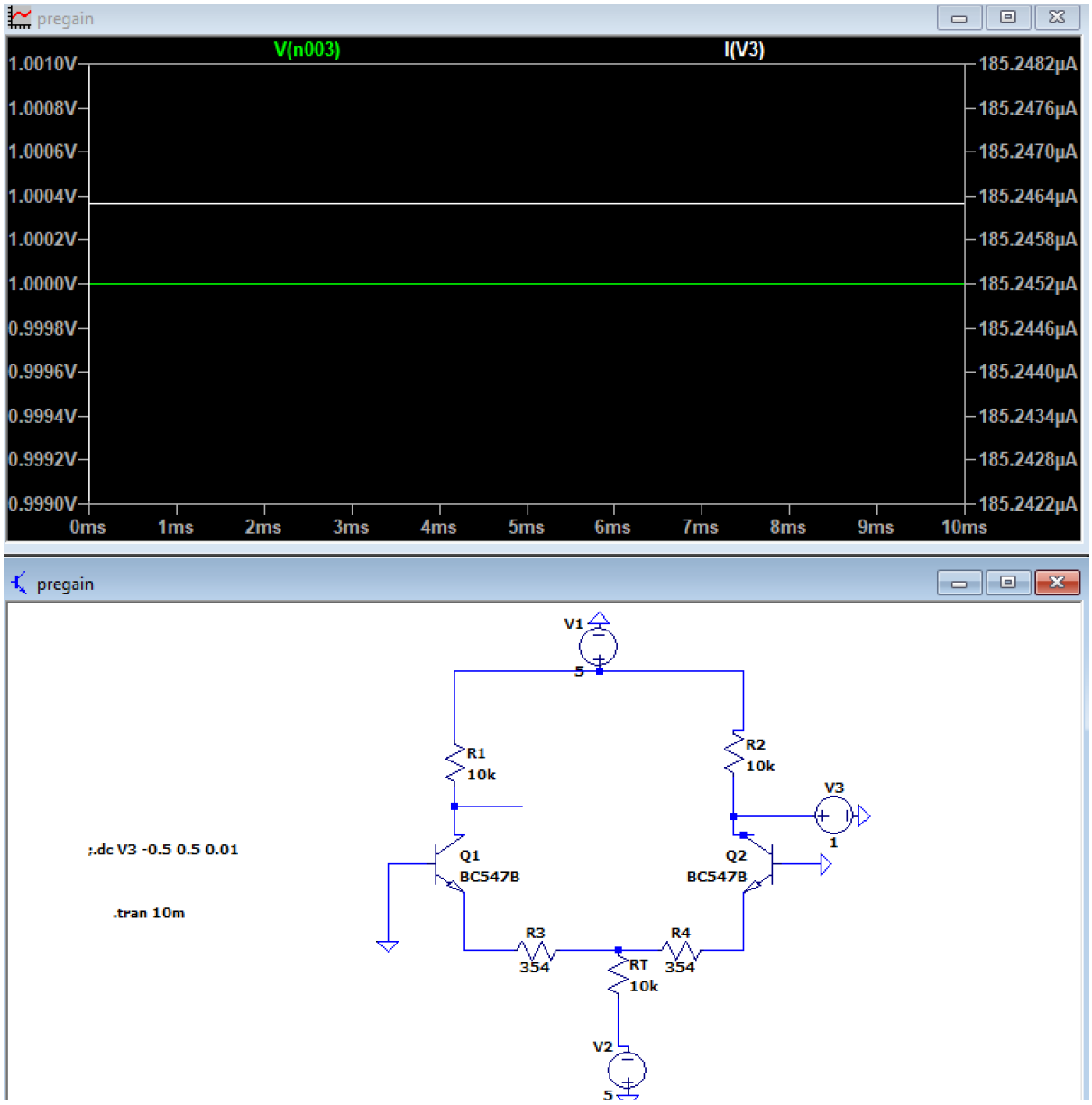

Figure 6: Ouput Resistance

2 Common Emitter (CE) Amplifier

- **Purpose:** Provides voltage amplification with phase inversion.
- **Configuration:** Input is applied at the base, output is taken from the collector, and the emitter is connected to ground through a resistor.
- **Key Features:** High voltage gain, moderate input impedance, low output impedance, and an inverted output signal.
- **Working Principle:**
  - Small increases in base-emitter voltage (V_{BE}) (a few mV) significantly increase base current (I_B).
  - Current gain (β) amplifies I_B, causing larger changes in collector current (I_C).

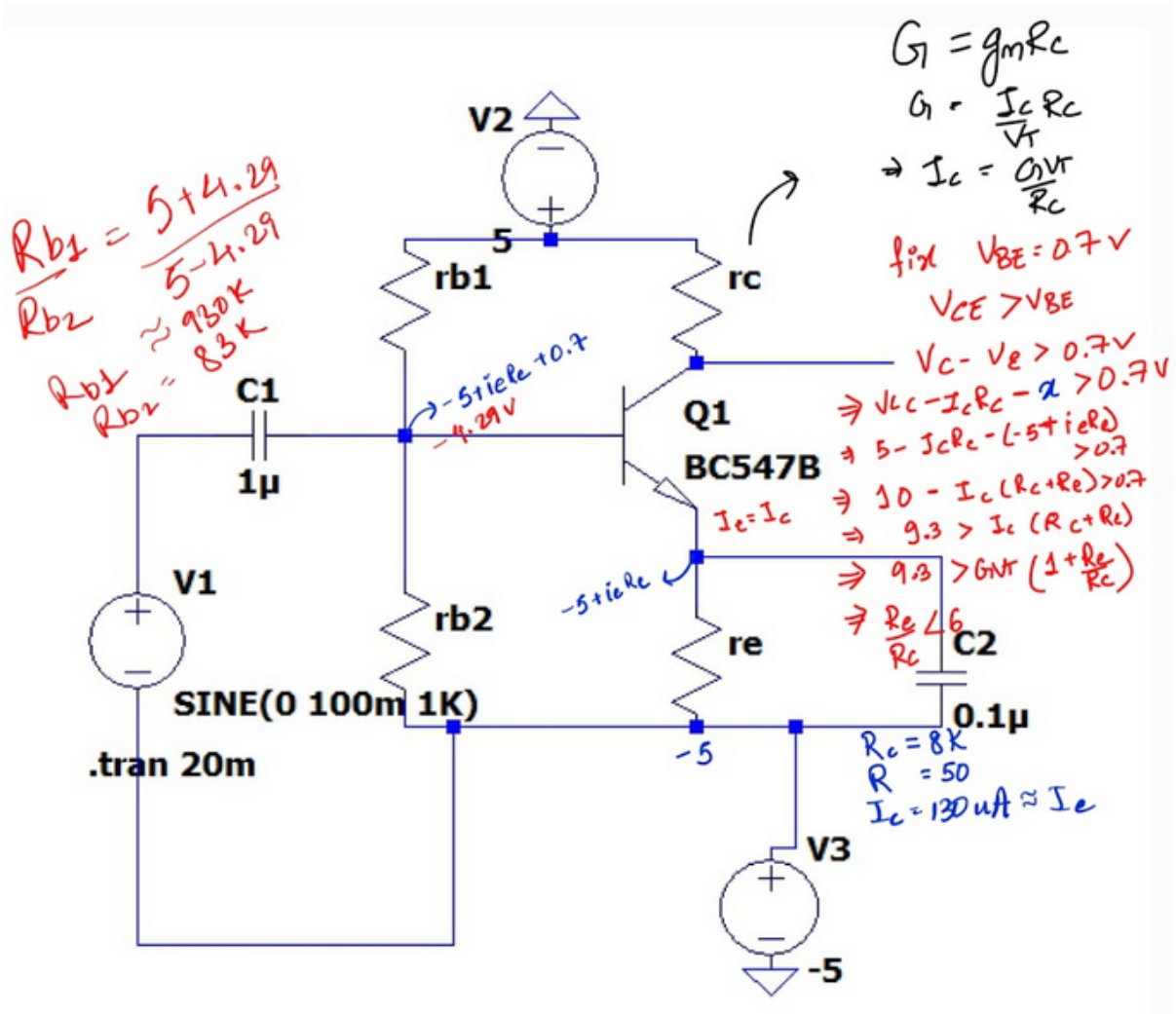

Figure 7: Parameter Calculations, CE Amplifier

Gain derviation of CE amplifier

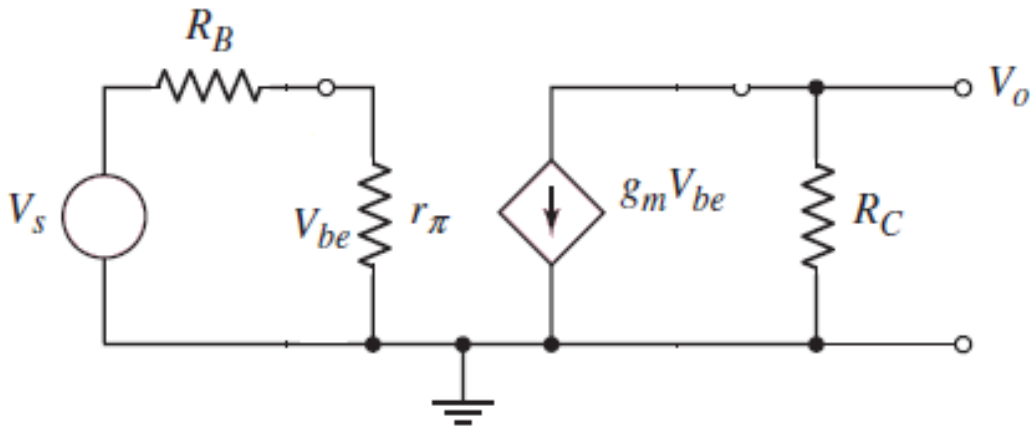

Figure 8: Small signal model of CE amplifer

form the above figure, We start with Ohm's Law:

$$V = IR$$

For the output voltage:

$$V_{out} = g_m V_{be}(R_C \parallel R_L)$$

The voltage gain is given by:

$$\frac{V_{out}}{V_{in}} = g_m R_C$$

where we assume $R_L = 0$.

Parameter Calculations

For a CE amplifier,we fix G=60 and calculate the values.

$$G = g_m \cdot R_C$$

$$g_m = \frac{I_C}{V_T}$$

$$I_C = \frac{G \cdot V_T}{R_C}$$

$$Fixing\ V_{BE} = 0.7V$$

$$V_C - V_E > 0.7V$$

$$V_{CC} - I_C \cdot R_C - x > 0.7V$$

$$Where\ x = -5 + I_E \cdot R_E$$

$$10 - I_C \cdot (R_C + R_E) > 0.7V$$

$$\therefore G \cdot V_T(1 + \frac{R_E}{R_C}) < 9.3$$

Substituting values, we get:

$$\frac{R_E}{R_C} < 6$$

To ensure **active BJTs**, we calculate R_{b1} & R_{b2} using Current Law as follows, with $V_B = -4.29V$

$$\frac{R_{b1}}{R_{b2}} = \frac{5 + 4.29}{5 - 4.29}$$

$$\therefore R_{b1} \approx 930k\ \Omega,\ R_{b2} \approx 78k\ \Omega$$

Our final values are:

$$R_C = 8k\ \Omega$$

$$R = 50\ \Omega$$

$$I_C \approx I_E = 130\,\mu A$$

LTSpice Plots

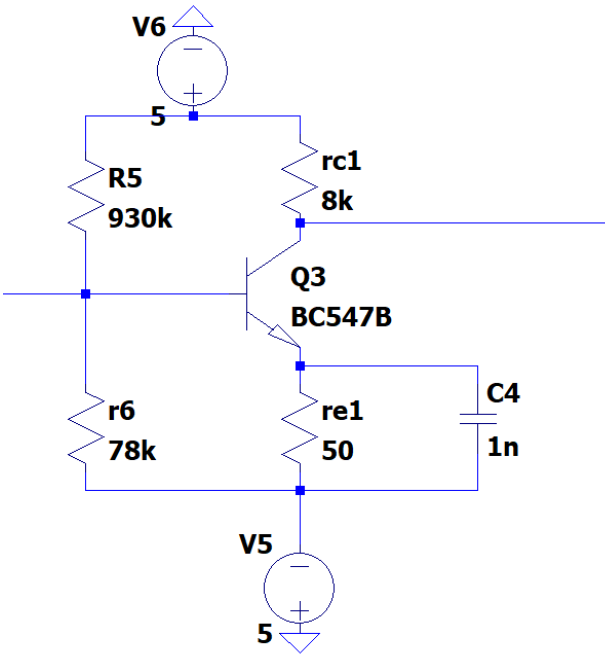

Figure 9: LTSpice CE amplifier

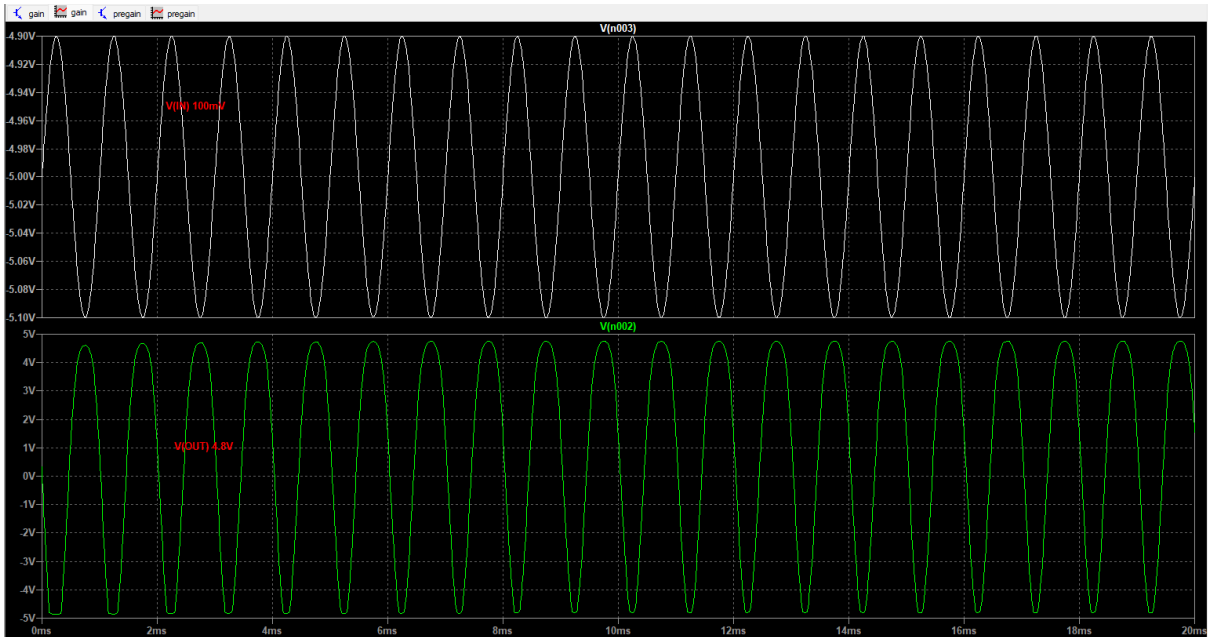

Figure 10: Plots of differential Amplifier

Notes

- The input and the output voltage are 180 degrees out of phase.
- $$\text{Gain comes out to be: } \frac{9.56V\text{ (pk-pk)}}{200\,\text{mV (pk-pk)}}$$

  $$\text{Gain} = \frac{9.56}{0.2} = 47.8$$
- Joining the first and second stages together, we observe that $G_1 \cdot G_2 < 500$. By tweaking R_c and R_e values slightly, we can achieve a net gain of

  $$\approx 460, \quad \text{with } G_1 = 7 \text{ and } G_2 = 65.$$

  This is verified for various small signal inputs.

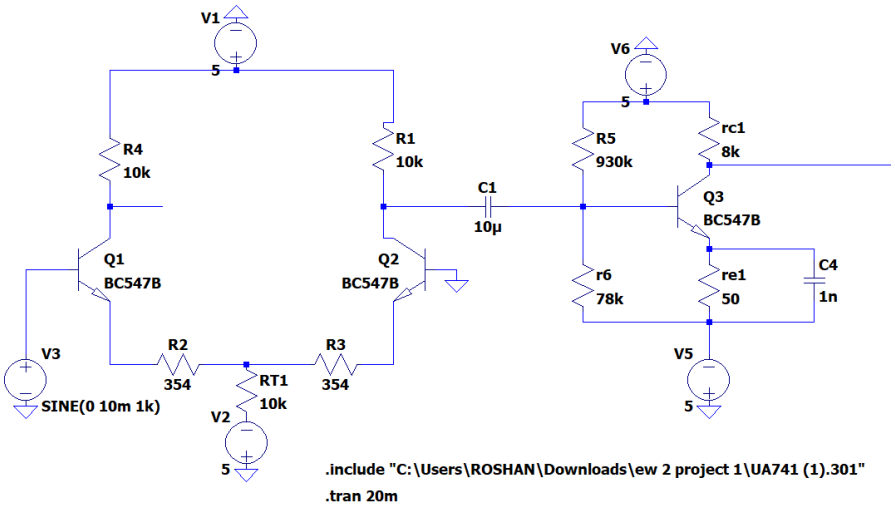

Figure 11: 2 stages joined

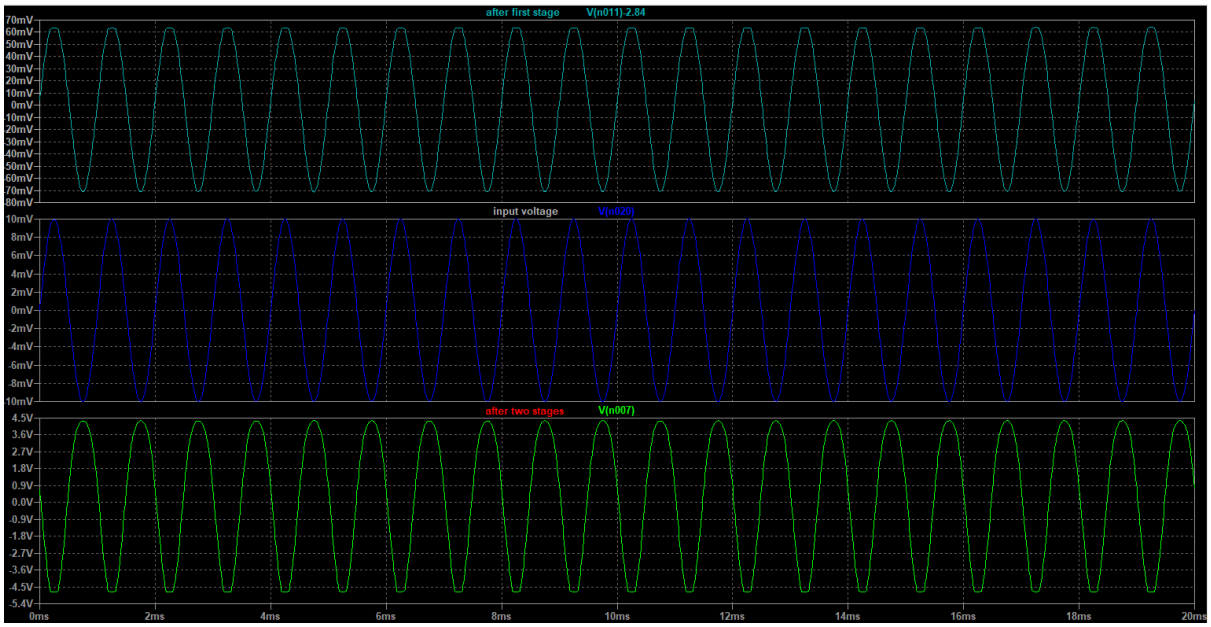

Figure 12: Signals at different stages

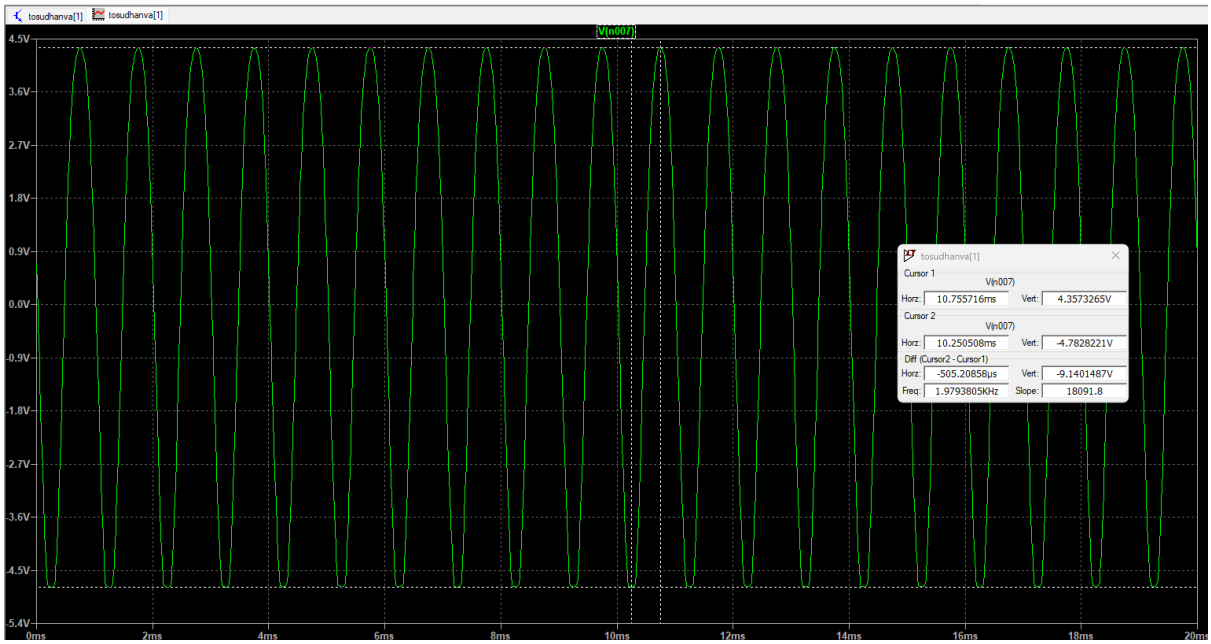

Figure 13: Signal has a gain of 460(9.14/0.02) gain after passing the input signal of 10mV into two stages.

Bandpass filter

We use a filter stage to eliminate freq. components other than 20Hz-kHz.
We make an active bandpass filter by connecting an HPF and an LPF with voltage followers in between.A active filter is a filter that has a voltage supply to it.

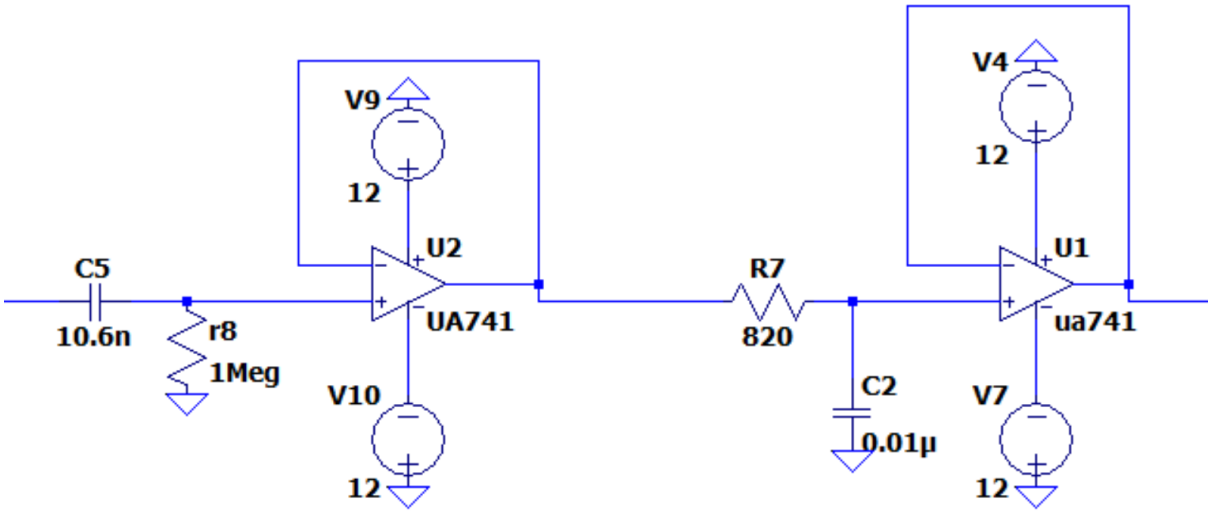

Figure 14: Bandpass is a combination of a lowpass and a highpass

High-Pass Filter (HPF):
The cutoff frequency for the HPF is given by:

$$f_{\text{HPF}} = \frac{1}{2\pi R_1 C_1}$$

Substituting $R_1 = 1\,\text{M}\Omega$ and $C_1 = 8\,\text{nF}$:

$$f_{\text{HPF}} = \frac{1}{2\pi(1 \times 10^6)(10.6 \times 10^{-9})} \approx 20\,\text{Hz}$$

we have taken a high-value resistance so that the loading effects to the CE amplifier [$Rc||R_l$] will be approximated to R_C.

Low-Pass Filter (LPF): The cutoff frequency for the LPF is given by:

$$f_{\text{LPF}} = \frac{1}{2\pi R_1 C_1}$$

Substituting $R_1 = 820\,\Omega$ and $C_1 = 0.01\,\mu\text{F}$:

$$f_{\text{LPF}} = \frac{1}{2\pi(820)(1 \times 10^{-8})} \approx 20\,\text{kHz}$$

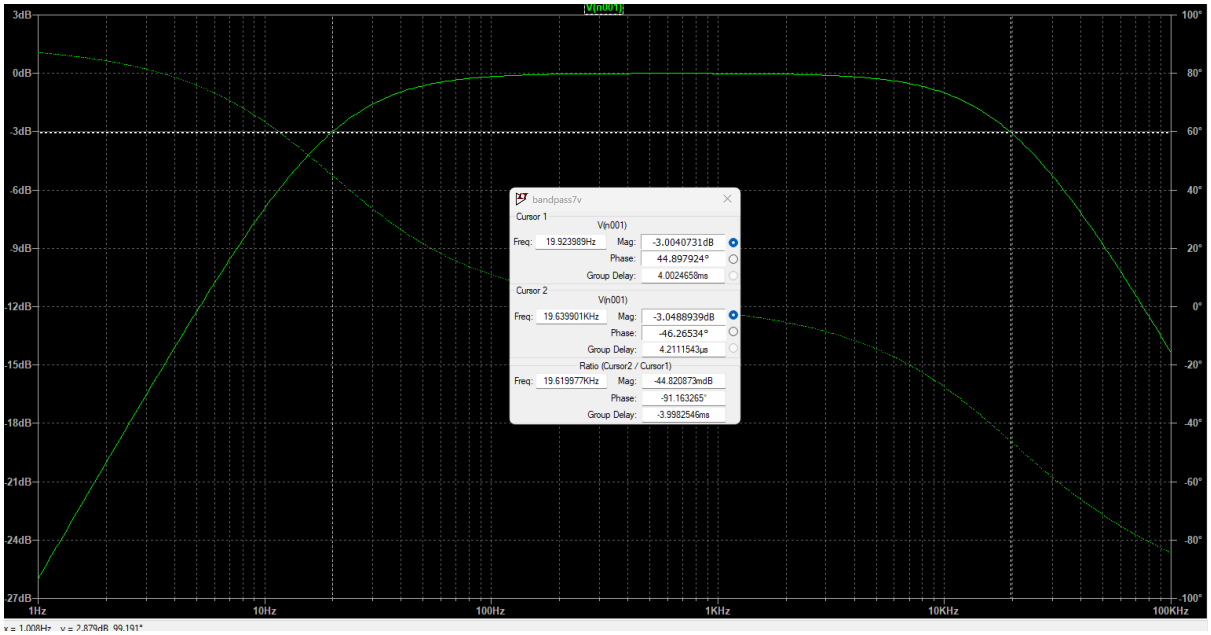

Figure 15: AC analysis of bandpass filter

Note:
There is a $-3\,\text{dB}$ gain at approximately $15\,\text{Hz}$ and $20\,\text{kHz}$.

Power Amplifiers

Power amplifiers are designed to deliver significant power to a load (e.g., a speaker) and operate efficiently at high output levels. They are typically used in the final stages of amplification in audio systems.

Class AB Design

- Combines the efficiency of Class B amplifiers with the low distortion of Class A amplifiers.
- Operates with both transistors conducting slightly during the crossover point, reducing crossover distortion.
- Biasing Using Diodes
  - Diodes are used to set the biasing voltage for transistors in the Class AB amplifier.
  - Typically, two diodes are placed in series with the base-emitter junctions of the output transistors.
  - The forward voltage drop of the diodes ensures a small quiescent current through the transistors, minimizing crossover distortion.

$$V_{\text{bias}} = 2V_f \quad \text{(where } V_f \text{ is the forward voltage of each diode).}$$

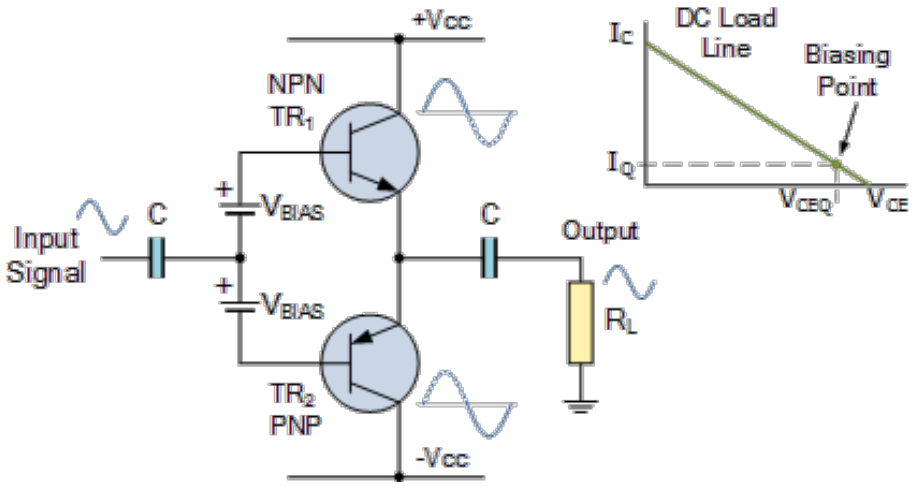

Figure 16: Class AB power amplifier

Estimating values

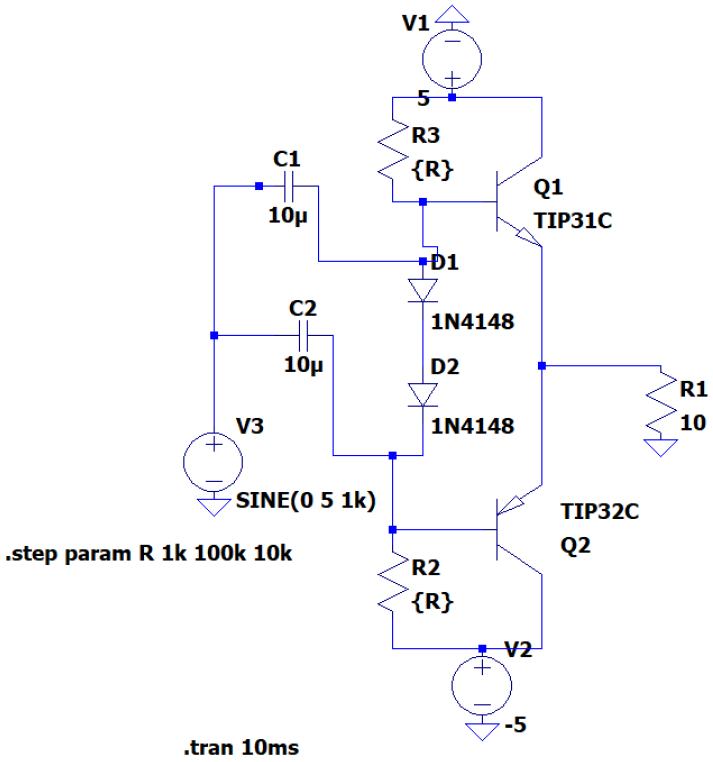

Figure 17: AB power Amplifier in LTspice

We parameterize the resistors above and below and plot the output voltage across R_{load} and take that value of R with least beadbound region) Here, R=1 kΩ.

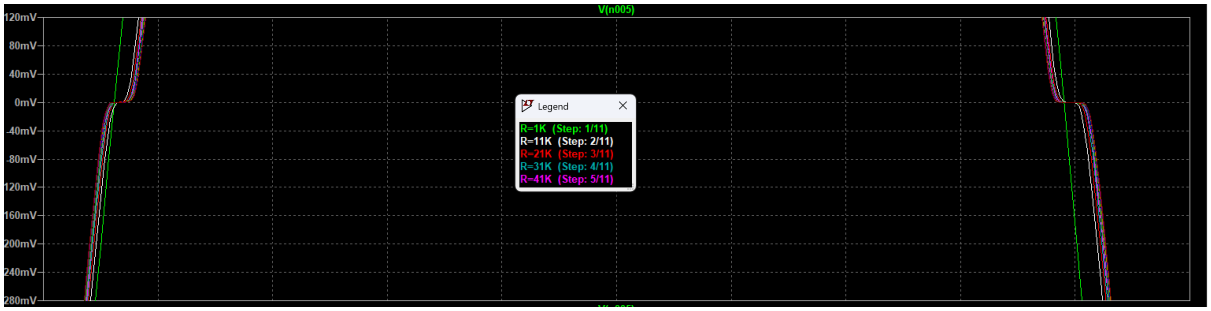

Figure 18: Analyzing output for various resistances

There will be a potential drop in output accounting for V_{BE}.

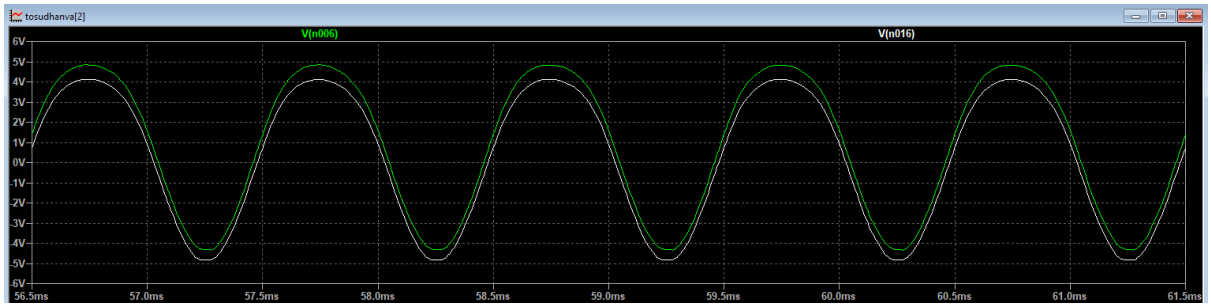

Figure 19: The positive half cycle has a voltage drop and negative half cycle has a increase in neagtive sense

Power Calculation

Given:

- Peak Current ($I_{\max}$) = 0.45 A
- Peak Voltage ($V_{\max}$) = 4.5 V

To calculate the power, we use the formula for the RMS values derived from the peak values:

$$V_{\text{rms}} = \frac{V_{\max}}{\sqrt{2}}, \quad I_{\text{rms}} = \frac{I_{\max}}{\sqrt{2}}$$

Then, the power P is given by:

$$P = V_{\text{rms}} \cdot I_{\text{rms}} = \frac{V_{\max} \cdot I_{\max}}{2}$$

Substituting the values:

$$P = \frac{4.5 \cdot 0.45}{2} = 1.025\,\text{W}$$

Thus, the power is $P = 1.025\,\text{W}$.

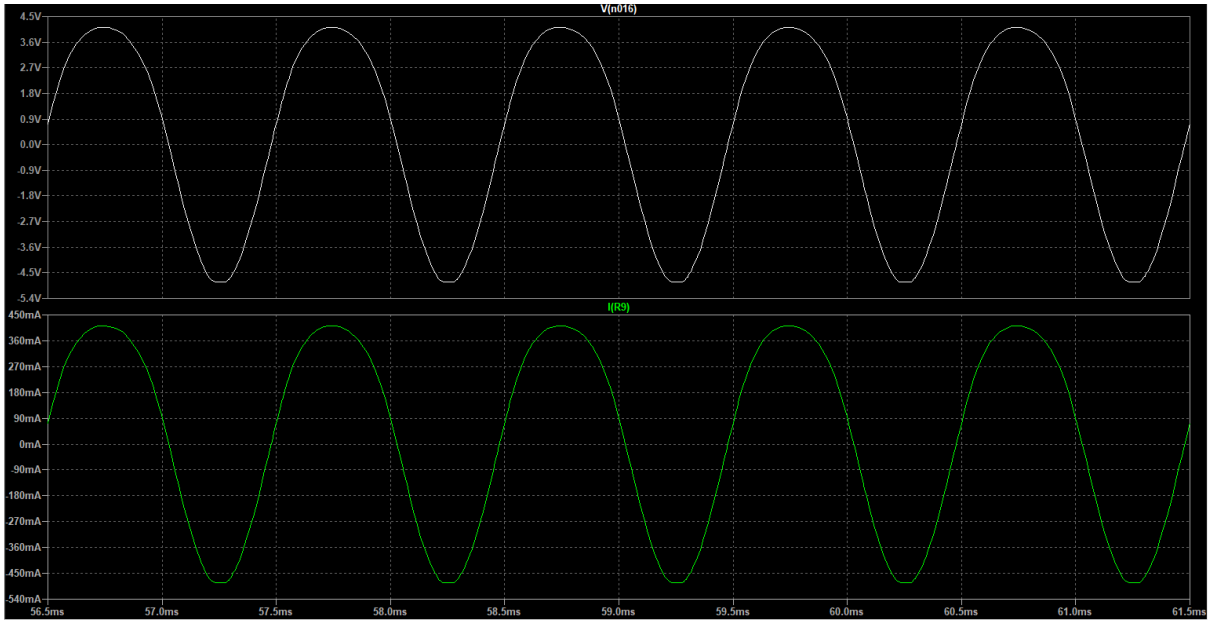

Figure 20: Power Calculation

Complete Circuital Analysis

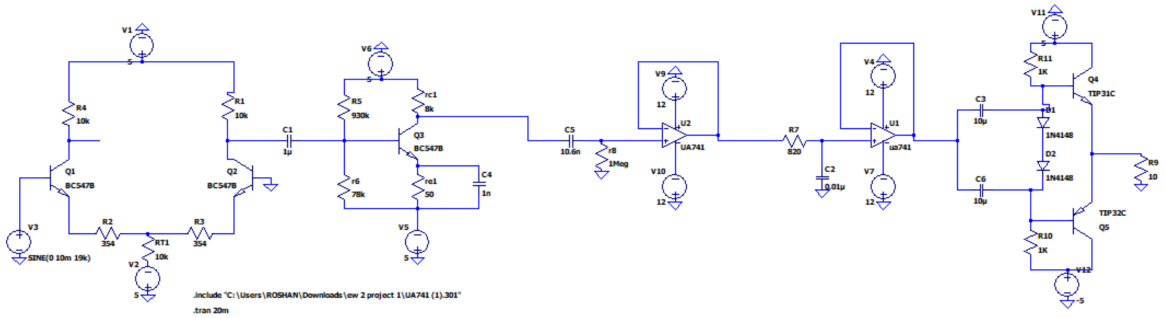

Figure 21: Entire circuit

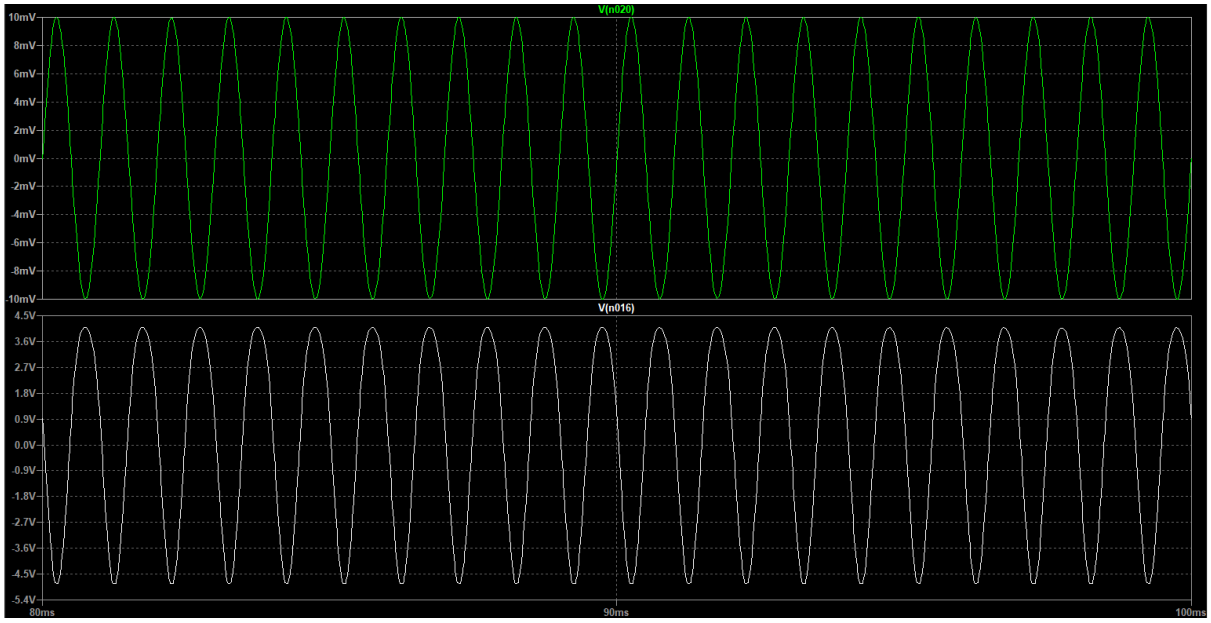

Figure 22: V_{in} & V_{out}

Total Harmonic Distortion

A Total Harmonic Distortion (THD) audio amplifier is designed to amplify an audio signal while minimizing unwanted distortions. THD refers to the harmonic components that are added to the original signal due to imperfections in the amplifier's circuitry. It is defined as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n,\text{rms}}^2}}{V_{f\_rms}}$$

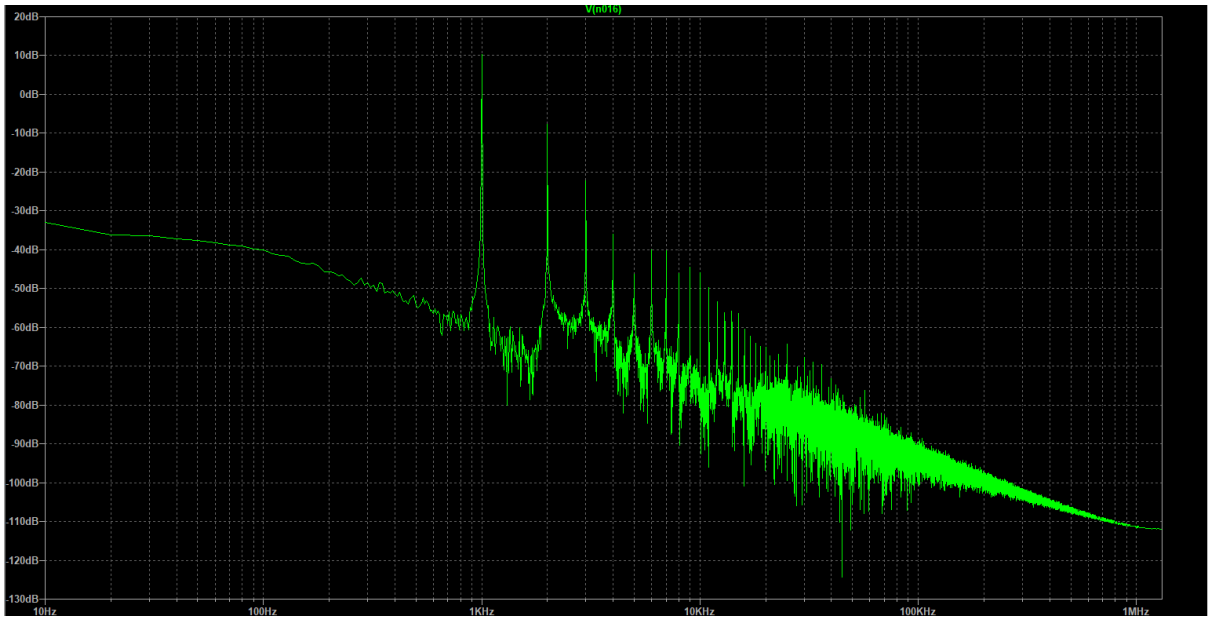

Figure 23: FFT, Output Wave

After applying **FFT** to our Output Wave, we consider the *first five harmonics* as a reasonable estimate.

Frequency(Hz)	Voltage(RMS)
1kHz	3.26V
2kHz	0.417V
3kHz	0.076V
4kHz	0.015V
5kHz	0.003V

Table 1: Harmonic Values

We get our final THD reading by substituting the observations as follows:

$$\therefore THD \approx 0.1301$$

Slew rate

Slew Rate refers to the rate at which the output voltage of an amplifier changes over time. It is typically measured in volts per microsecond (V/us) and is an important parameter for audio amplifiers, as it determines how quickly the amplifier can respond to rapid changes in the input signal. $S.R. = max(\frac{\delta V_{out}}{\delta t})$

From LTSpice, by plotting $\frac{\delta V_{\text{out}}}{\delta t}$, it has a maximum **Slew Rate** $\approx 0.35\,\text{V}/\mu\text{s}$.

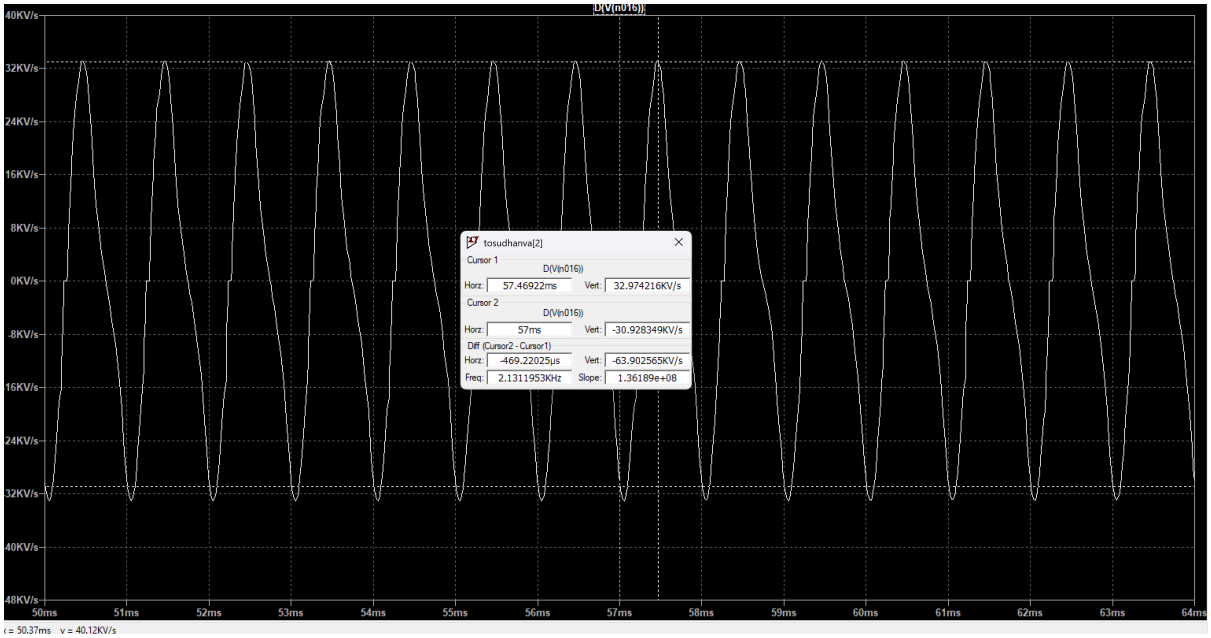

Figure 24: Slew rate

Hardware Observations

The hardware implementation employs a few practical changes in component values that detract from our original simulation to account for non-idealities.

- *(Input/Output Impedances, Heat etc)* necessitate adjustmenets in resistance and capacitance values being used in all stages.
- The **Frequency Response** of bandpass stage requires the *cutoff frequencies (20Hz-20kHz)* to be at 0dB gain; The true -3dB cutoffs must considered further away from our initially calculated values for f_c.

Readings with the final circuit are given below.

Reference

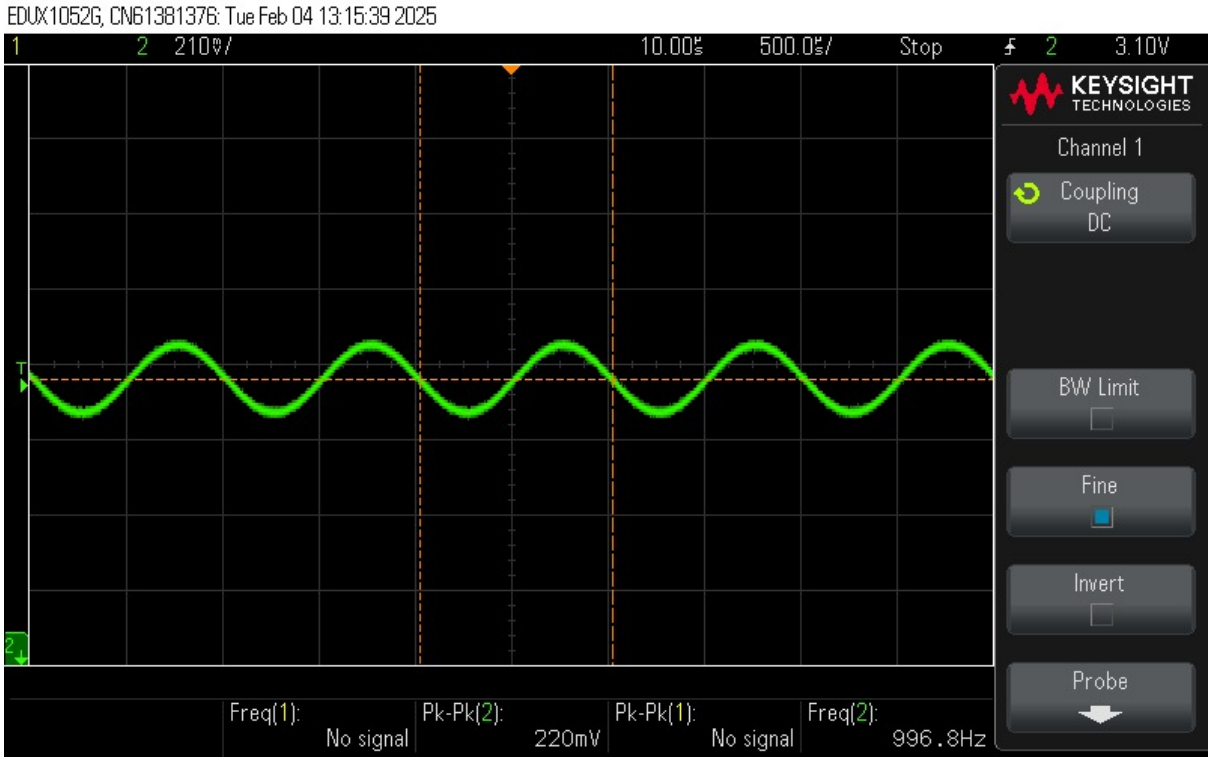

Figure 25: Amplification 10 after first stage

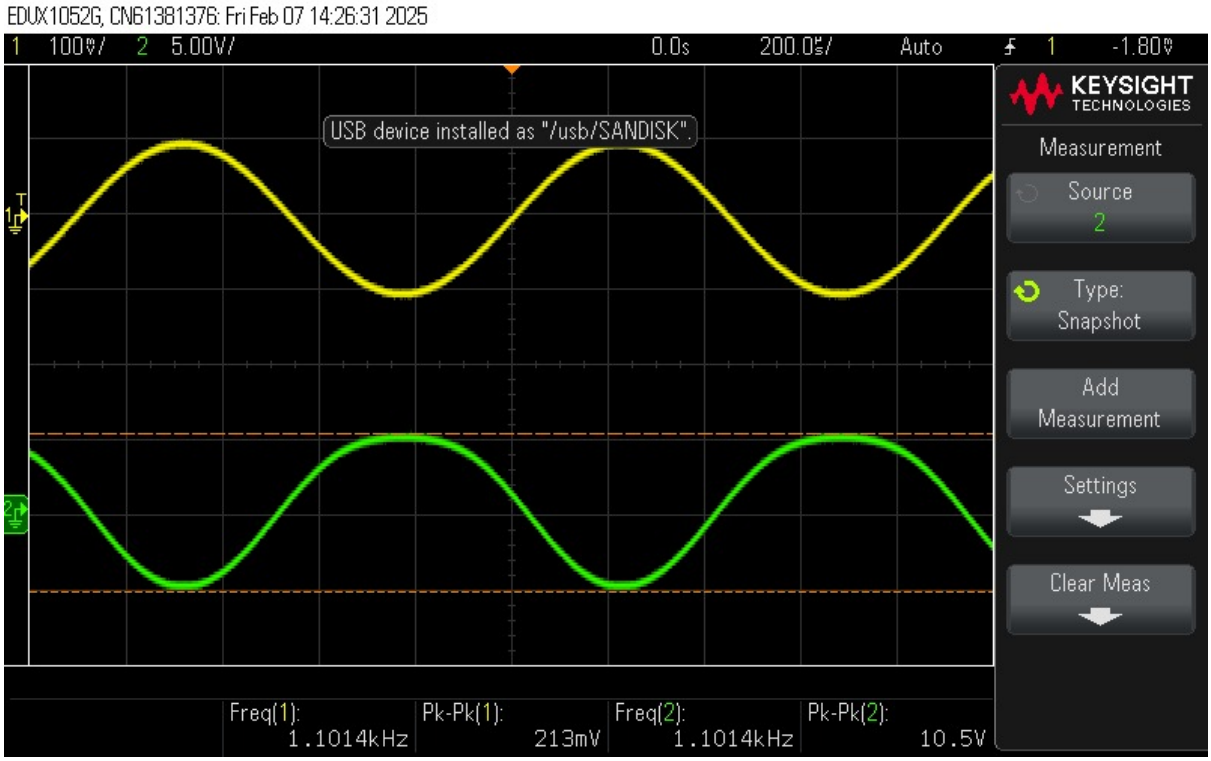

Figure 26: Amplification 50 after two stages

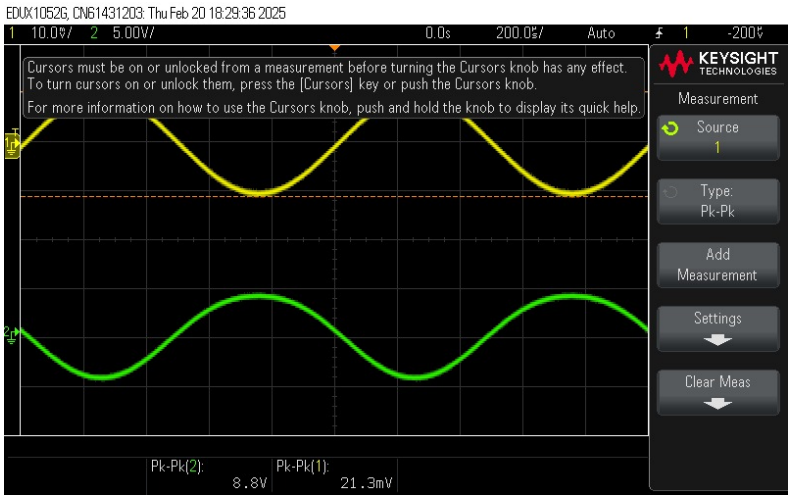

Figure 27: I/O Waveforms

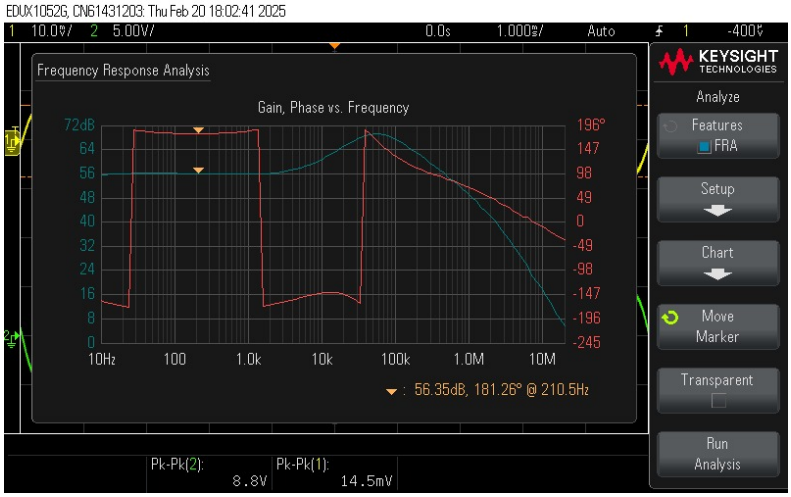

Figure 28: Gain, Differential + CE Stage

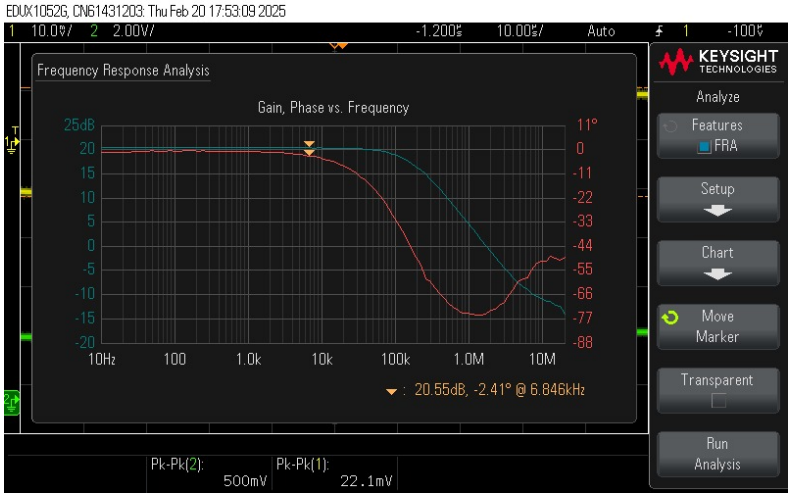

Figure 29: Differential Amplifier Gain

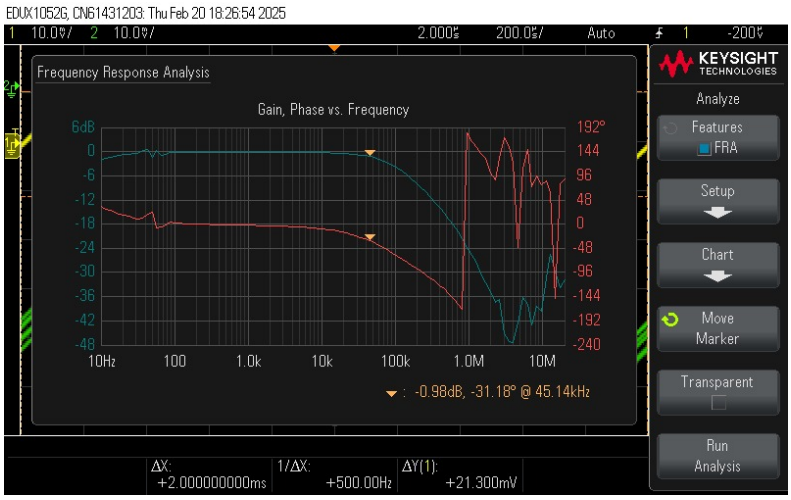

Figure 30: Frequency Analysis, Bandpass Filter

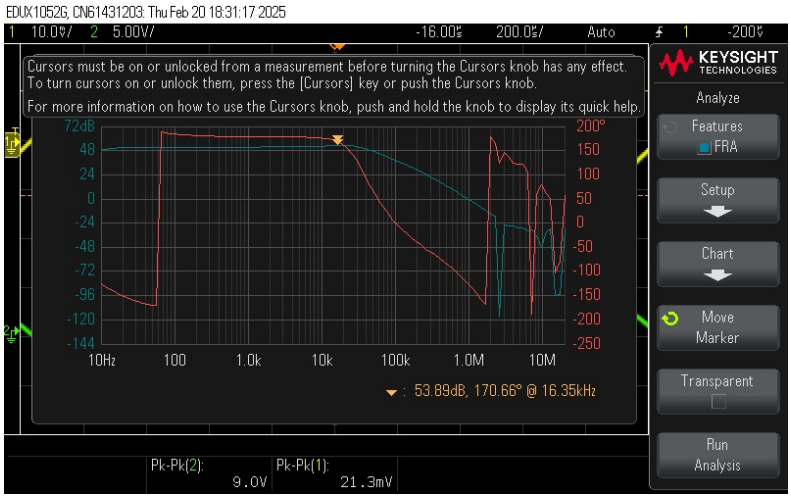

Figure 31: Final Circuit, 4 Stages Attached *(Observe Reduced Gain)*

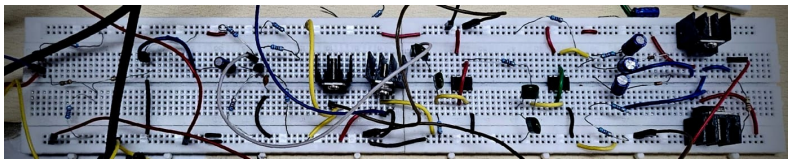

Figure 32: Breadboard Implementation

The following link showcases the practical exhibition of our amplifier.

Acknowledgement

We would like to sincerely thank the professors, TAs and lab assistants for their unending support and guidance throughout the course of this project. section*References

- YouTube Playlist 1
- YouTube Playlist 2