

Mode of Data Transfer

The binary information that is received from an external device is usually stored in the memory unit. The information that is transferred from the CPU to the external device is originated from the memory unit. Data transfer between CPU and I/O devices may be done in different modes.

Data transfer to and from the peripherals may be done in any of the three possible ways.

(i) Programmed I/O :

It is due to the result of I/O instructions that are written in the computer program. Each data transfer is initiated by an instruction in the program. In this case it requires constant monitoring by the CPU of the Peripheral devices. In this method, the I/O device does not have direct access to the memory unit. A transfer from I/O device to memory requires the execution of several instructions by the CPU. In Programmed I/O, the CPU stays in the program loop until the I/O unit indicates that it is ready for data transfer. This is a time consuming process as it needlessly keeps the CPU busy. This situation can be avoided by using an interrupt facility. Programmed data transfer schemes are employed when small amount of data are to be transferred.

(ii) Interrupt-Driven I/O :-

In this scheme the CPU initiates an I/O device to get ready and then it executes its main program instead of remaining in a program loop to check the

status of the I/O device. When I/O device becomes ready to transfer data, it sends a high signal to the CPU through a special input line called interrupt line. In other words, it interrupts the normal processing sequence of the CPU. On receiving an interrupt, the CPU completes the current instruction at hand, and then attends the I/O device. It saves the contents of the program counter on the stack first, and then handle the I/O device. After completing the data transfer, the CPU returns back to the main program which it was executing before the interrupt occurred.

Both the methods programmed I/O and interrupt-driven I/O require the active intervention of the processor to transfer data between memory and I/O, and any data transfer must traverse a path through the processor. Thus, both these forms of I/O suffer from the two drawbacks:

- (a) ~~I/O~~ The I/O transfer rate is limited by the speed with which the processor can test and service a device.
- (b) The processor is tied up in managing an I/O transfer; a number of instructions must be executed.

(iii) Direct Memory Access (DMA):

In DMA data transfer scheme, CPU does not participate. Data are directly transferred from an I/O device to memory or vice versa. The data transfer is controlled by the I/O device or a DMA controller. This scheme is employed when large amount of data are to be transferred. If the bulk data are transferred through the CPU, it takes appreciable time and the process become slow.

An I/O device which wants to send data using DMA technique, sends the HOLD signal to the CPU.

On receiving HOLD signal from an I/O device, the CPU gives up the control of buses as soon as the current machine cycle is completed. The CPU sends a hold acknowledge signal to the I/O device to indicate that it has received the HOLD request and it has released the buses. The I/O device takes over the control of buses and directly transfers data to the memory or reads the data from memory. When data transfer is over, the CPU regains the control over the buses.

DMA data transfer scheme is faster than ~~Programmed~~ or interrupt driven data transfer scheme.

DMA data transfer scheme are of two types.

(i) Burst Mode of DMA Data Transfer:-

A scheme of DMA data transfer, in which the I/O ~~device~~ device withdraws the DMA request only after all the data bytes have been transferred, is called burst mode of data transfer. By this technique a block of data is transferred. This technique is employed by magnetic disk drives.

(ii) Cycle Stealing Technique:-

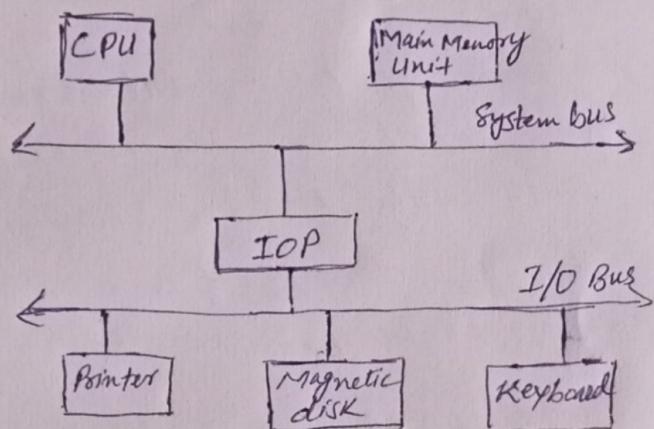
In this technique, a long block of data is transferred by a sequence of DMA cycles. In this method, after transferring one byte or several bytes, the I/O devices withdraws DMA request. This method reduces interference in CPU's activities. The interference can be eliminated completely by designing an interfacing circuitry which can steal bus cycle for DMA data transfer only when CPU is not using system bus.

Input-Output Processor (IOP) :-

The input output Processor (IOP) is just like a CPU that handles the details of I/O operations. It is more equipped with facilities than those are available in a typical DMA controller. The IOP can fetch and execute its own instructions that are specifically designed to

characterize I/O transfer. In addition to the I/O-related tasks, it can perform other processing tasks like arithmetic, logic, branching and code translation.

Block Diagram of Input-Output Process (IOP) :-



The input output processor is a specialized processor which loads and stores data into memory along with the execution of I/O instruction.

External Communication Interface :-

The external communication interface refers to the different communication channel/buses used by system to communicate with external world. The various interfaces for external communication are

- (i) RS-232C & RS -485
- (ii) Universal Serial Bus (USB)
- (iii) Infra red
- (iv) Bluetooth
- (v) Wi-Fi
- (vi) ZigBee