

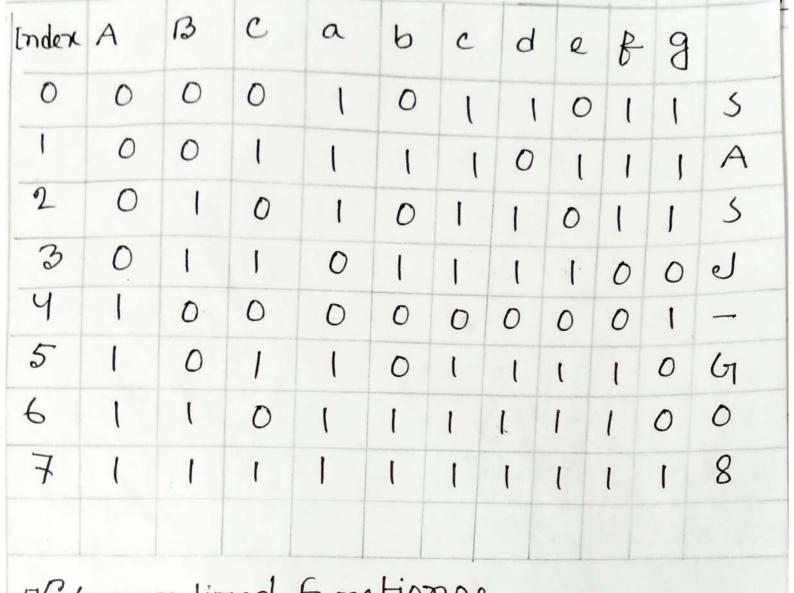
Project Report CSE 231

Digital Logic Design Section 11 Workstation-08

Using combinational circuit print: **SASJ-G08** in 7 segment display

Spring 2020 North South University Submitted To: Tanjila Farah(TnF)

| SL. | NAME: | Student ID: |
|-----|---------------------------|-------------|
| 1. | S M Gazzali Arafat Nishan | 1831513642 |
| 2. | Rofiqul Alam Shehab | 1831185042 |
| 3. | Sudipta Bhatta | 1731194042 |



$$=\Sigma(0,1,2,5,6,7)$$

$$b = ABC + ABC + ABC + ABC = \Sigma(1,3,6,7)$$

 $c = ABC + ABC +$

$$d = ABC + ABC + ABC + ABC + ABC + ABC$$

$$= \sum (0,2,3,5,6,7)$$

$$= \sum (0,2,3,5,6,7)$$

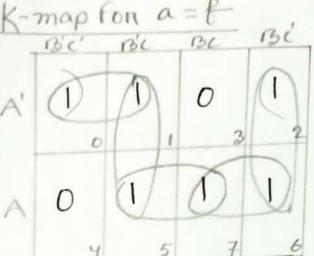
$$e = \sum_{i=1}^{n} (0,2,3,3,0,1)$$

$$= \sum_{i=1}^{n} (1,3,5,6,7)$$

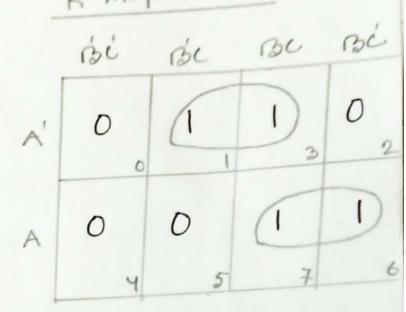
$$= \sum_{i=1}^{n} (1,3,5,6,7)$$

2 = ABC+ABC+ABC+ABC+ABC K-map for

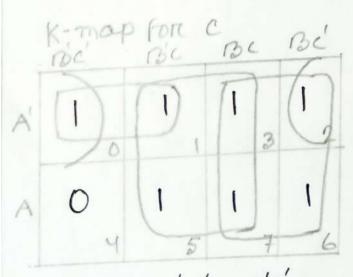
 $= \sum (0,1,2,4,7)$



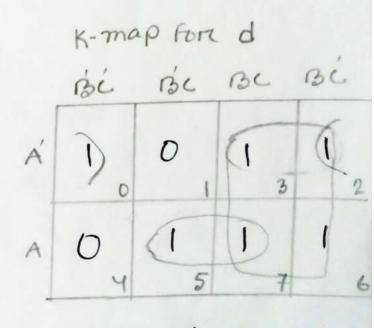
F=AB+BC+AC+AB+BC



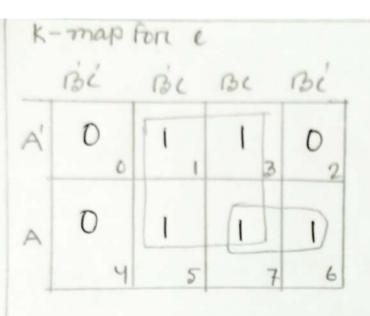
F=A'C+AB

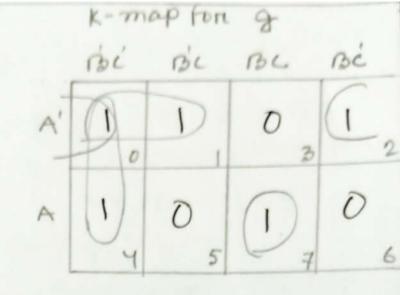


F=C+B+AB+A'C'



F=B+AC+A'C'





Hi simplification Bon 200

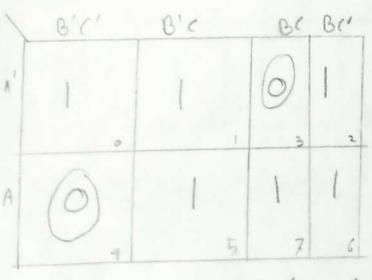
He Generalized POS Function:

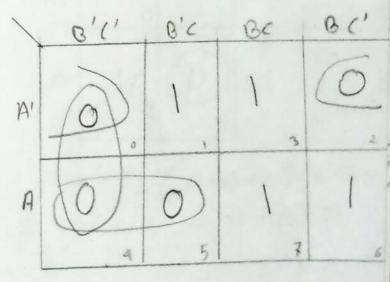
$$A = ABC' + ABC = (A'+B+e)(A+B'+C') = OTT(3,9)$$
 $b = ABC' + ABC' + ABC' + ABC' + ABC = (A+B+e)(A+B'+C)$
 $(A'+B+c)(A'+B+C')$
 $= (TT(0,2,4,5)$

C = AB'C' = A'+B+C = TT (4)

k-map for a=f

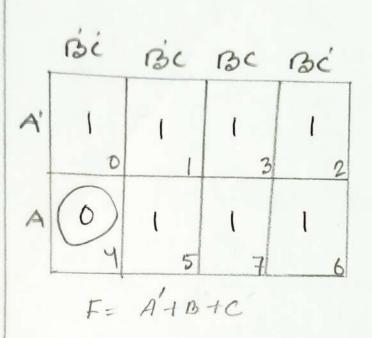
x-map sorz b



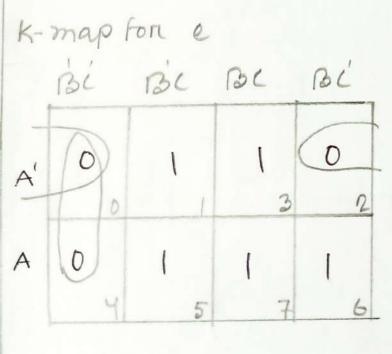


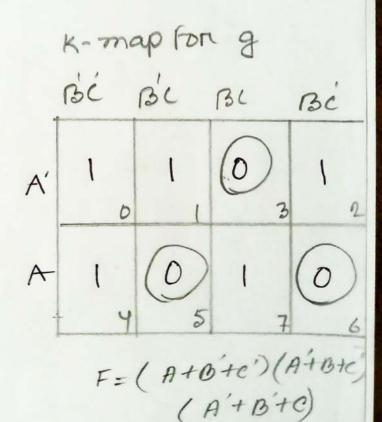
K-map for c

K-map For d



| | Bic | Bic | BC | BC | |
|----|-----|-------|--------|------|----|
| A' | 1 | 0 | 1 3 | 1 | 2 |
| A | 0 | 1 | 1 7 | | 6 |
| | F | = (A- | + B+C) | A+B+ | c) |





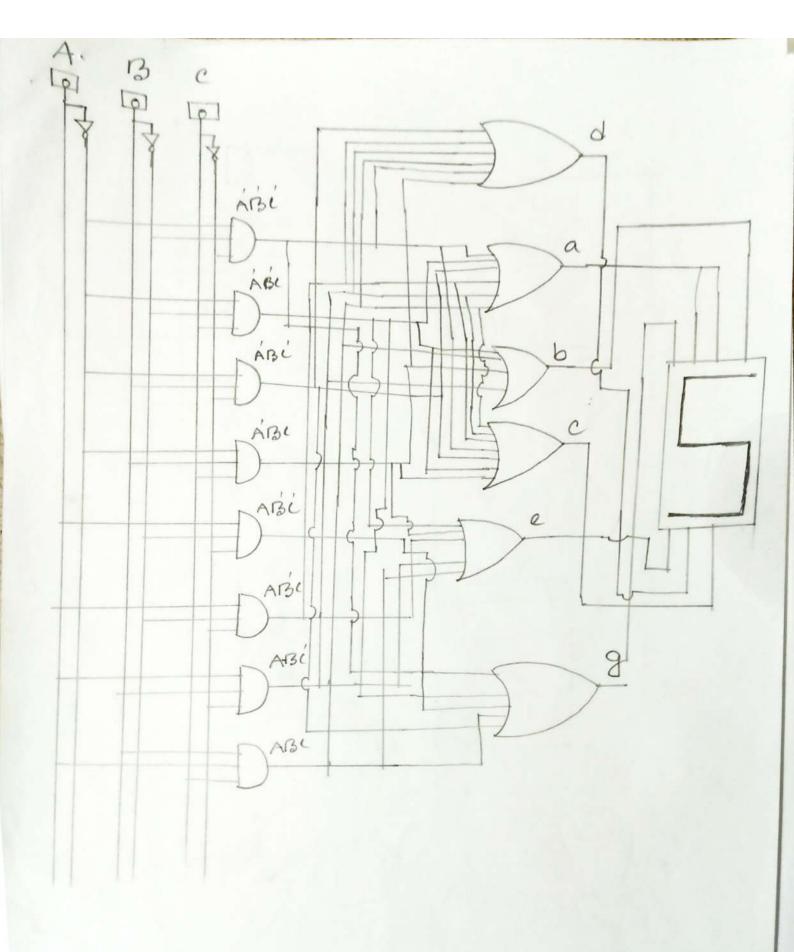
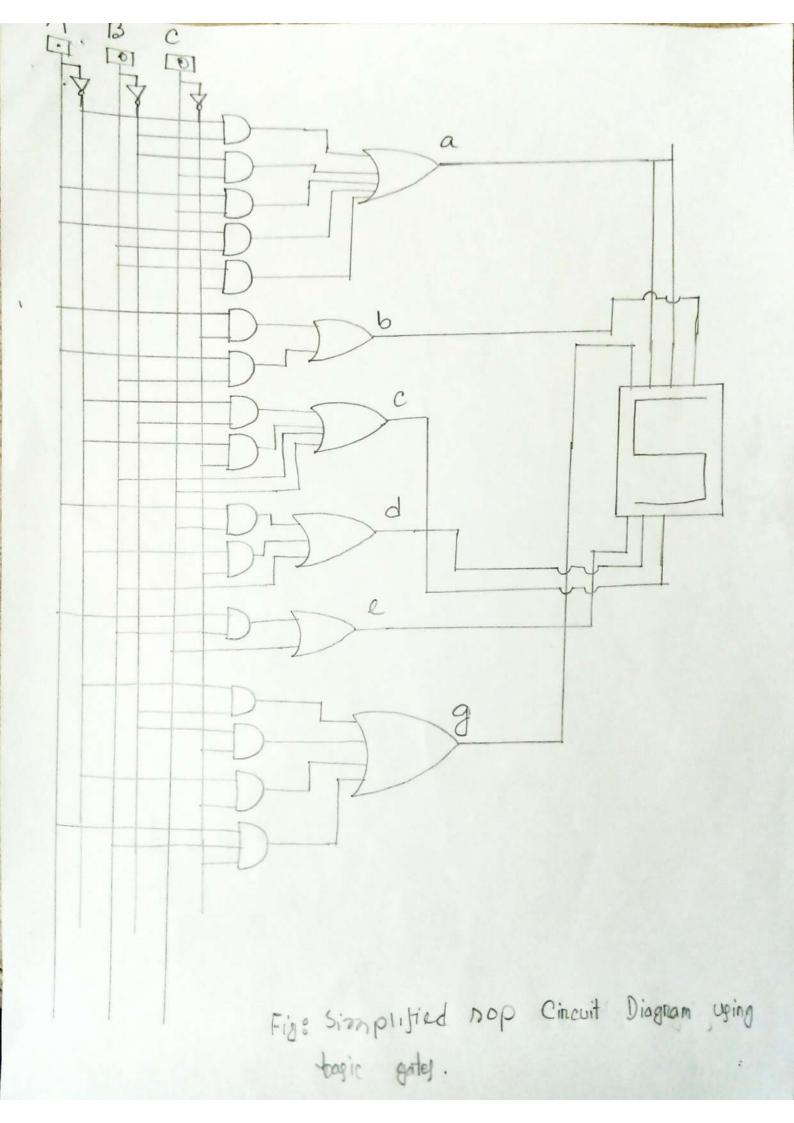


Fig: Greneralized sop Cincuit Diagram Using
Basic gates.



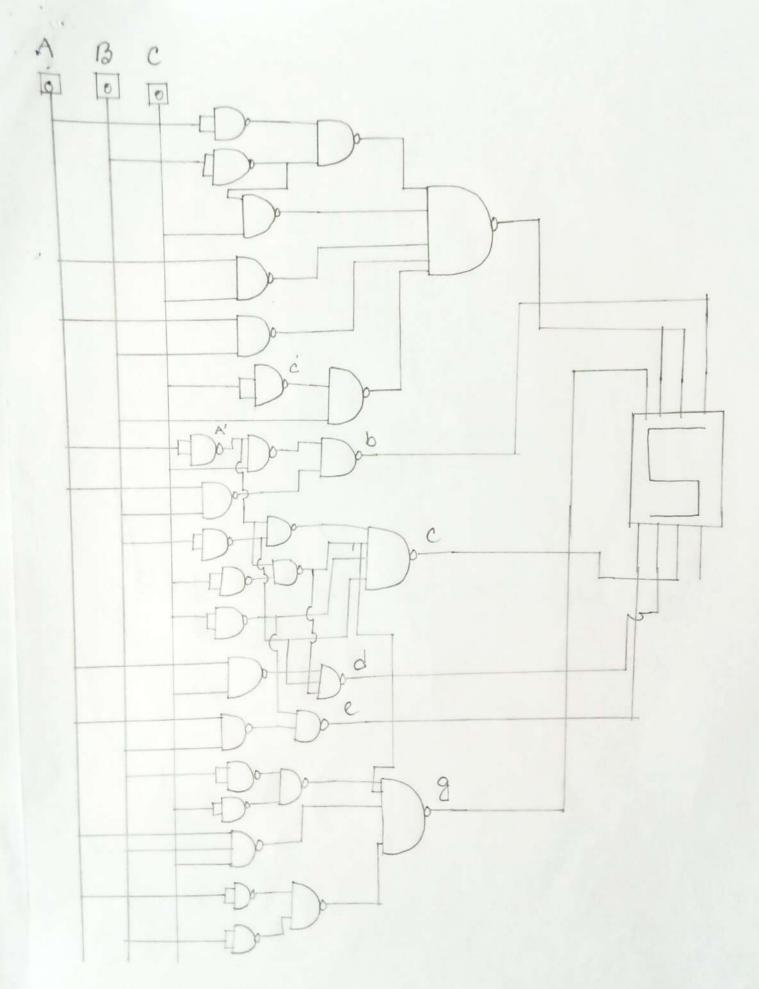


Fig: Simplified SOP Cincuit Diagram you're NAND gates.

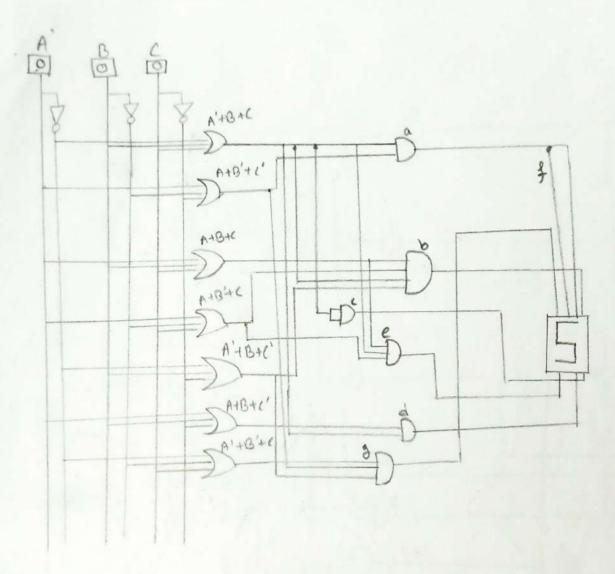
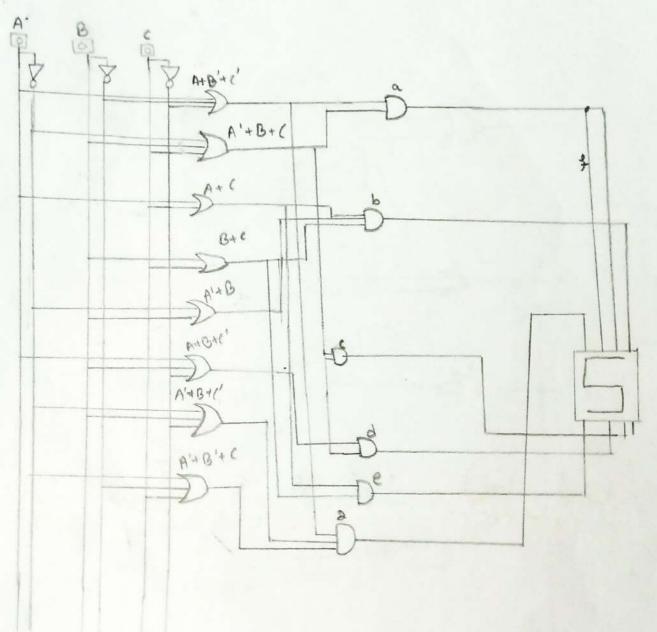
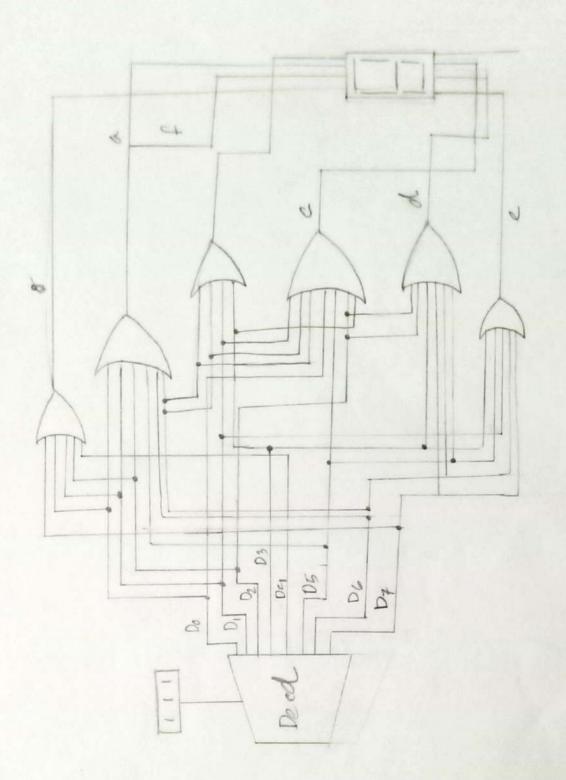


Fig: Cheveralized pos cincuit diagram ying togic gotes.



Figo Simplified por unewit Diagram wring basic gates

Fig: Simplified POS using only NOR dates A B C (A+B+C) (n'+B+c) (A+B+() 100) (1/10 rc) | 2d (A+B'+(*)' (A+B+L) (A'+B+C')



Fg. Greneralized SOF Cincuit Diagram uping Decader and OR gate.

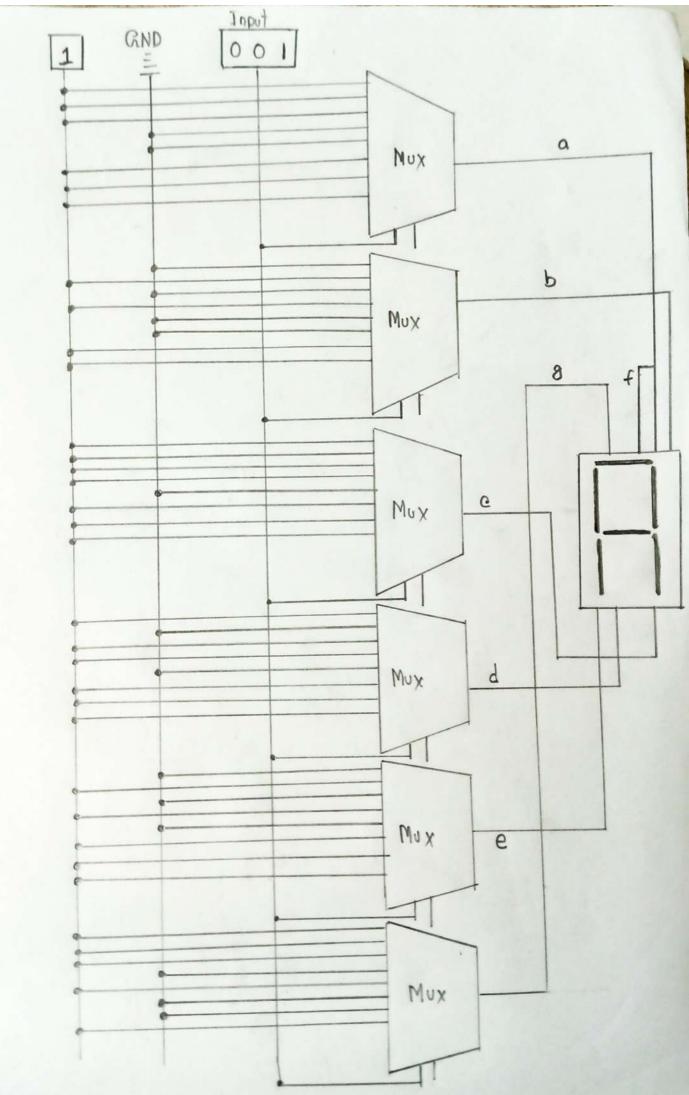


Fig: Generalized SOP Multiplexer

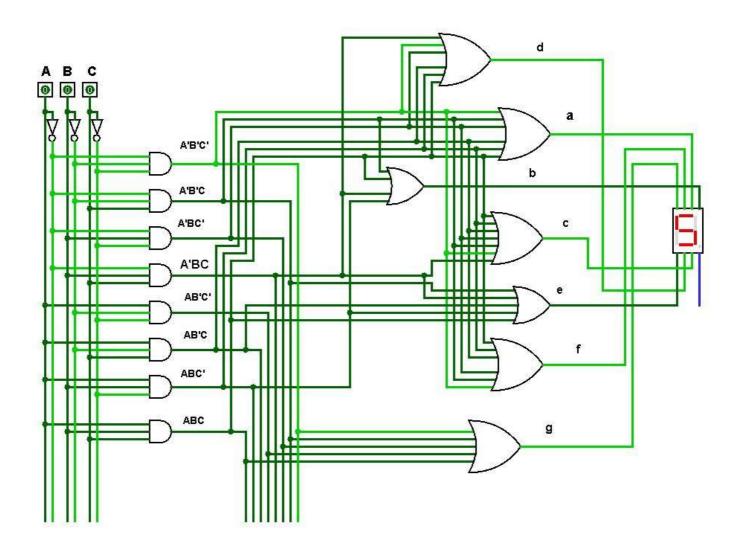


Fig. Circuit Diagram For Generalized SOP Equation

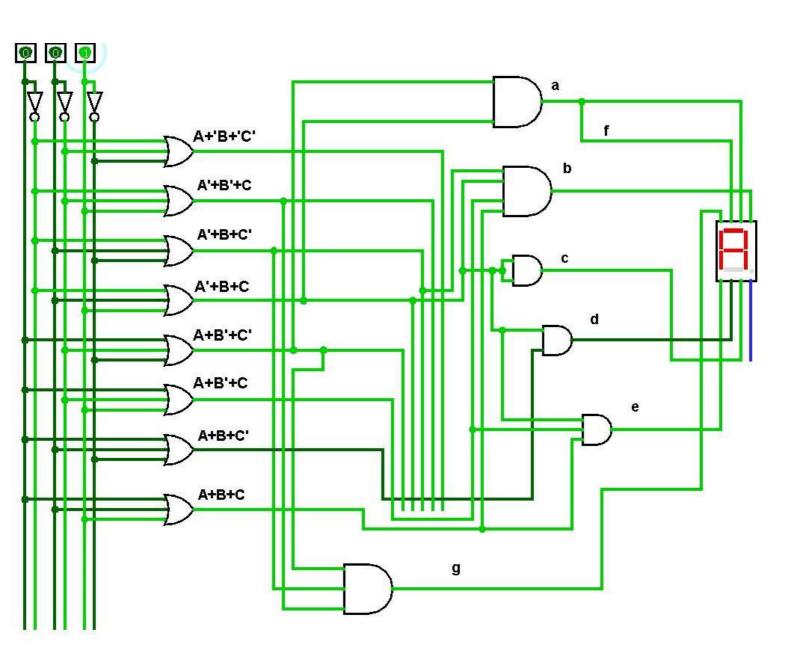


Fig. Circuit Diagram for Simplified SOP Using Basic Gates

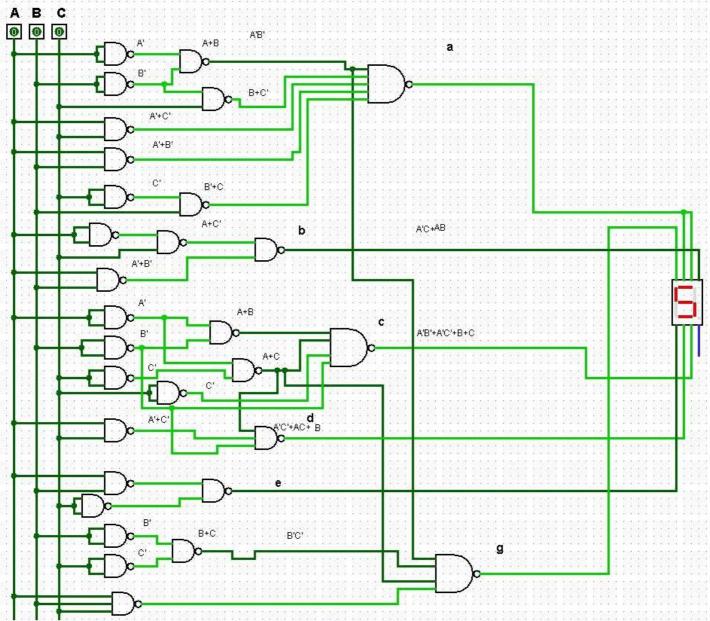


Fig. Circuit Diagram of SOP using only NAND Gates

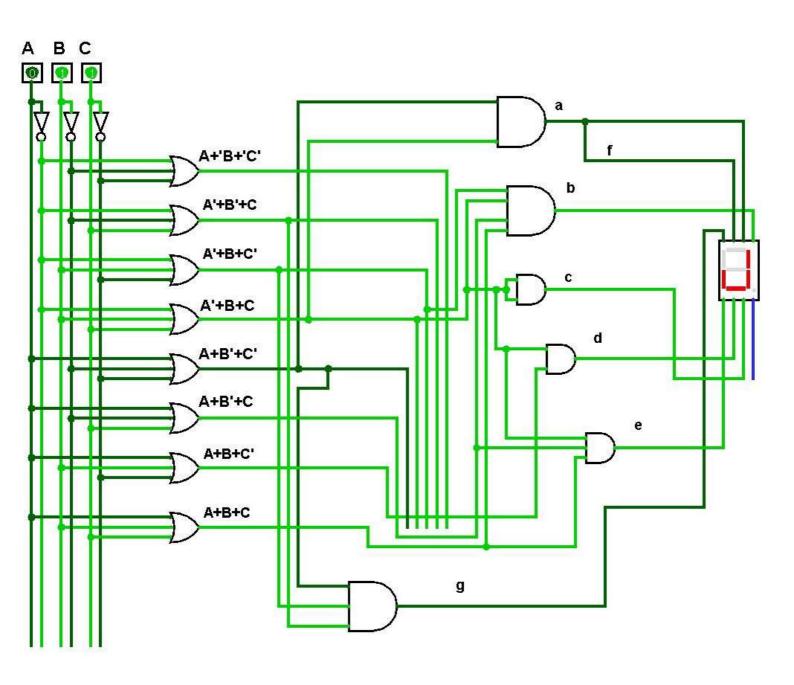


Fig. Circuit Diagram of Generalized POS

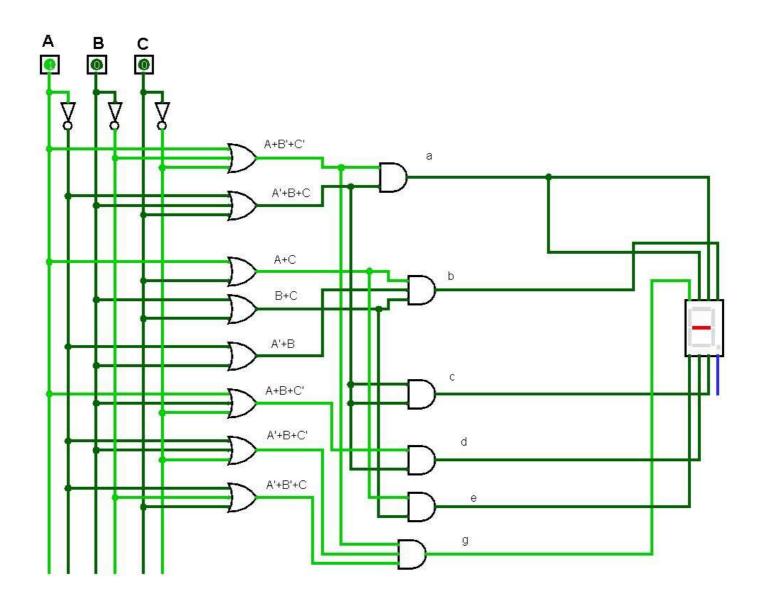
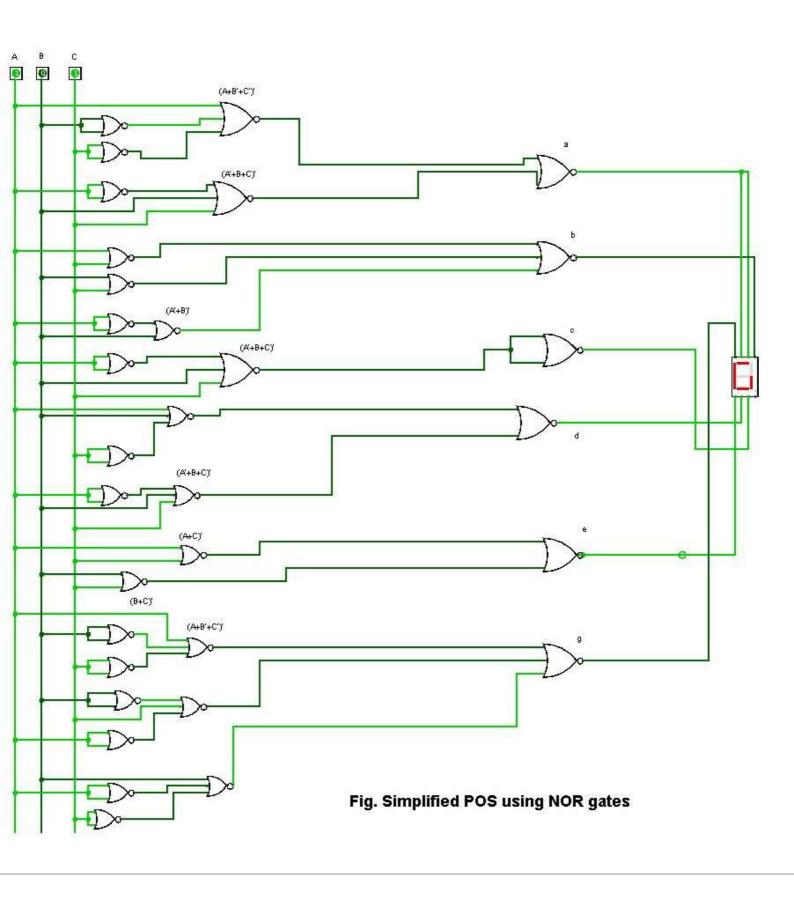


Fig.Circuit Diagram for Simplified POS Using Basic Gates



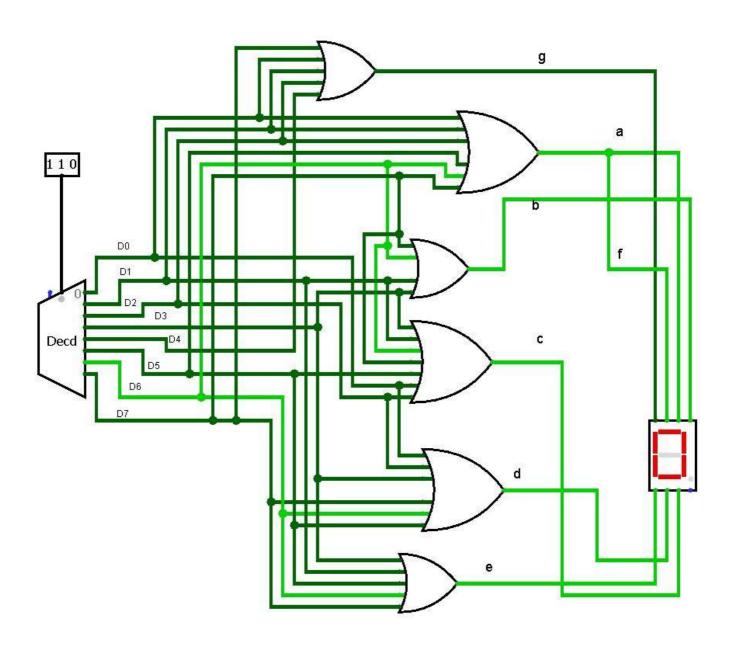


Fig. Generalized SOP Using Decoder and OR Gates

