Project Report
CSE 231

Digital Logic Design
Section 11
Workstation-08

Using combinational circuit print: **SASJ-G08** in 7 segment display

Spring 2020
North South University
Submitted To: Tanjila Farah(TnF)

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Index	A	B	C	a	b	c	d	e	f	g	
0	0	0	0	1	0	1	1	0	1	1	S
1	0	0	1	1	1	1	0	1	1	1	A
2	0	1	0	1	0	1	1	0	1	1	S
3	0	1	1	0	1	1	1	1	0	0	J
4	1	0	0	0	0	0	0	0	0	1	-
5	1	0	1	1	0	1	1	1	1	0	G
6	1	1	0	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	1	1	1	8

Generalized Functions:

$a = \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B}C + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + A\acute{B}C + ABC$

$= \Sigma(0,1,2,5,6,7)$

$b = \acute{A}\acute{B}C + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + A\acute{B}C + ABC = \Sigma(1,3,6,7)$

$c = \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B}C + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + A\acute{B}C + AB\acute{C} + ABC = \Sigma(0,1,2,3,5,6,7)$

$d = \acute{A}\acute{B}\acute{C} + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + A\acute{B}C + AB\acute{C} + ABC$

$= \Sigma(0,2,3,5,6,7)$

$e = \acute{A}\acute{B}\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + A\acute{B}C + AB\acute{C} + ABC$

$= \Sigma(1,3,5,6,7)$

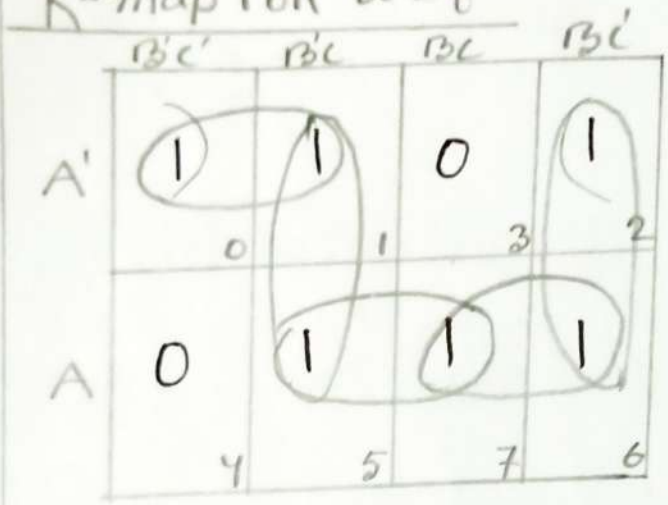
$f = \acute{A}\acute{B}\acute{C} + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}C + AB\acute{C} + ABC$

$\sum(0,1,2,5,6,7)$

$g = \acute{A}\acute{B}\acute{C} + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}\acute{C} + ABC$

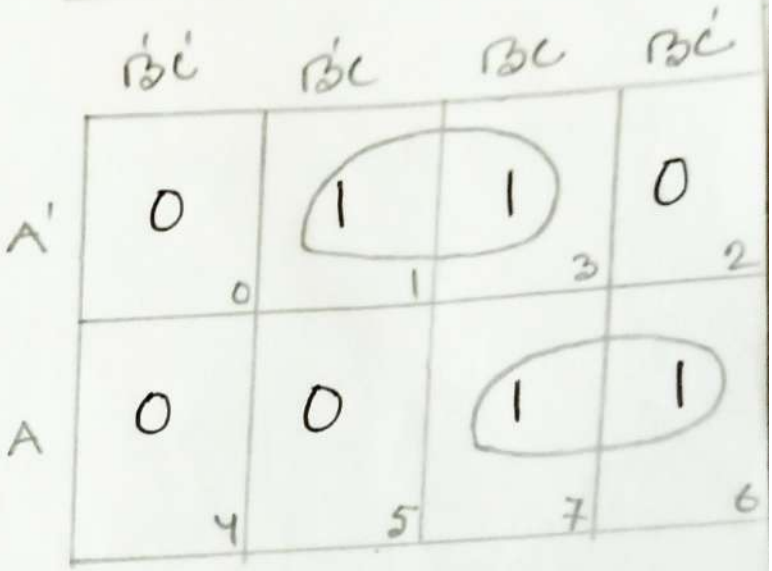
$= \sum(0,1,2,4,7)$

K-map for a = f



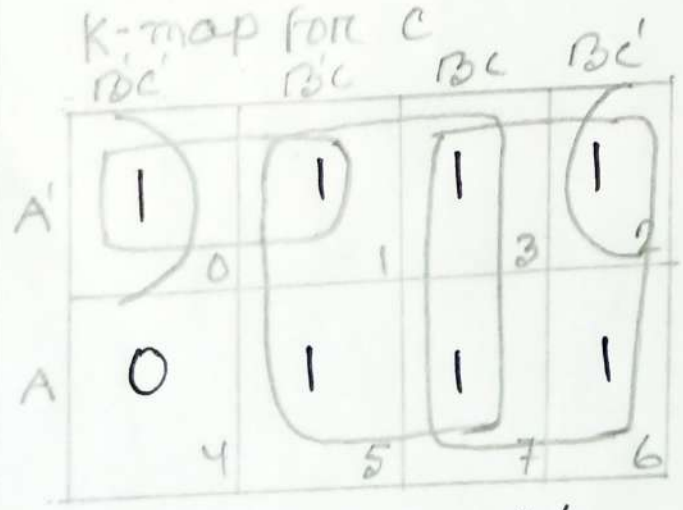
$F = \acute{A}\acute{B} + B\acute{C} + AC + AB + B\acute{C}$

K-map for b



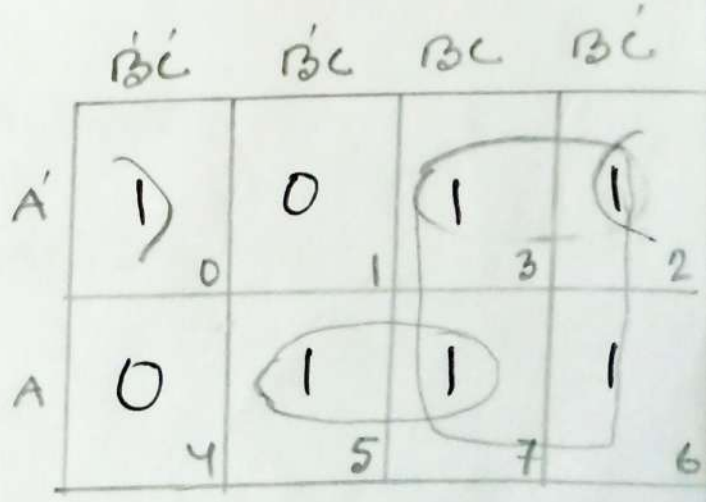
$F = A\acute{C} + AB$

K-map for c



$F = C + B + A\acute{B} + A\acute{C}$

K-map for d



$F = B + AC + A\acute{C}$

K-map for e

	$B'C'$	$B'C$	BC	BC'
A'	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = e + AB$

K-map for g

	$B'C'$	$B'C$	BC	BC'
A'	1 (0)	1 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	1 (7)	0 (6)

$F = A'B' + B'C' + A'C' + ABC$

Simplification for sop

i) $a = A'B' + B'C + AC + AB + BC'$

ii) $b = A'C + AB$

iii) $c = c + B + A'B' + A'C'$

iv) $d = B + AC + A'C'$

v) $e = c + AB$

vi) $f = A'B' + B'C + AC + AB + BC'$

vii) $g = A'B' + B'C' + A'C' + ABC$

Generalized POS Function :

$a = AB'C' + A'BC = (A'+B+C)(A+B'+C') = \Pi(3,4)$

$b = A'B'C' + A'BC' + AB'C' + AB'C = (A+B+C)(A+B'+C)$
$(A'+B+C)(A'+B+C')$
$= \Pi(0,2,4,5)$

$c = AB'C' = A'+B+C = \Pi(4)$

$d = A'B'C + AB'C' = (A+B+C')(A'+B+C) = \Pi(1,4)$

$e = A'B'C' + A'BC' + AB'C' = (A+B+C)(A+B'+C)$
$(A'+B+C) = \Pi(0,2,4)$

$f = AB'C' + A'BC = (A'+B+C)(A+B'+C') = \Pi(3,4)$

$g = A'BC + AB'C + ABC' = (A+B'+C')(A'+B+C')$
$(A'+B'+C) = \Pi(3,5,6)$

k-map for a=f

	B'C'	B'C	BC	BC'
A'	1 (0)	1 (1)	0 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = (A+B'+C')(A'+B+C)$

k-map for b

	B'C'	B'C	BC	BC'
A'	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	0 (5)	1 (7)	1 (6)

$F = (A+C)(B+C)(A'+B)$

K-map for c

	$B'C'$	$B'C$	BC	BC'
A'	1 (0)	1 (1)	1 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = A' + B + C$

K-map for d

	$B'C'$	$B'C$	BC	BC'
A'	1 (0)	0 (1)	1 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = (A + B + C')(A' + B + C)$

K-map for e

	$B'C'$	$B'C$	BC	BC'
A'	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = (A + C)(B + C)$

K-map for g

	$B'C'$	$B'C$	BC	BC'
A'	1 (0)	1 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	1 (7)	0 (6)

$F = (A + B' + C')(A' + B + C)(A' + B' + C)$

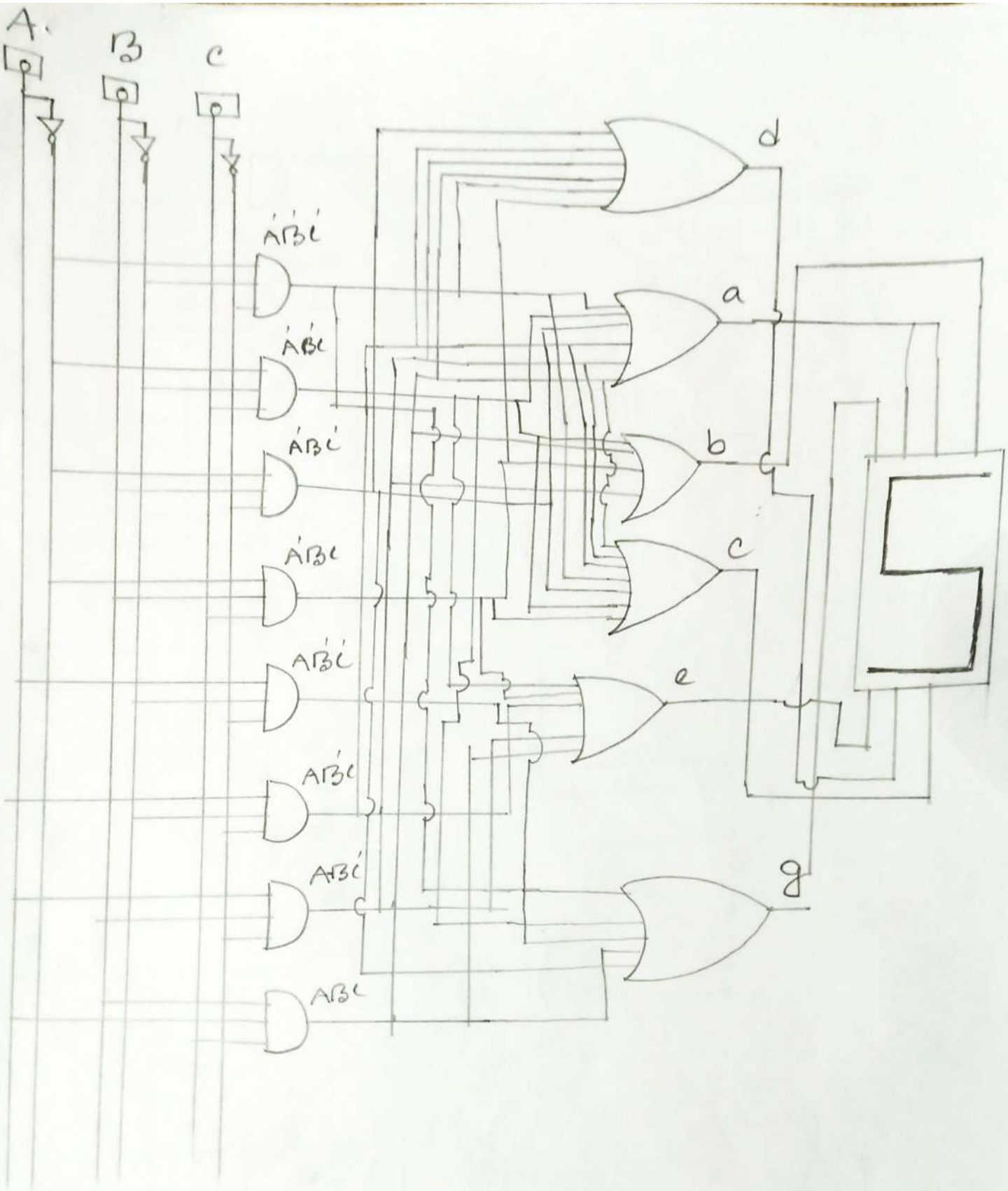


Fig: Generalized SOP Circuit Diagram Using Basic gates.

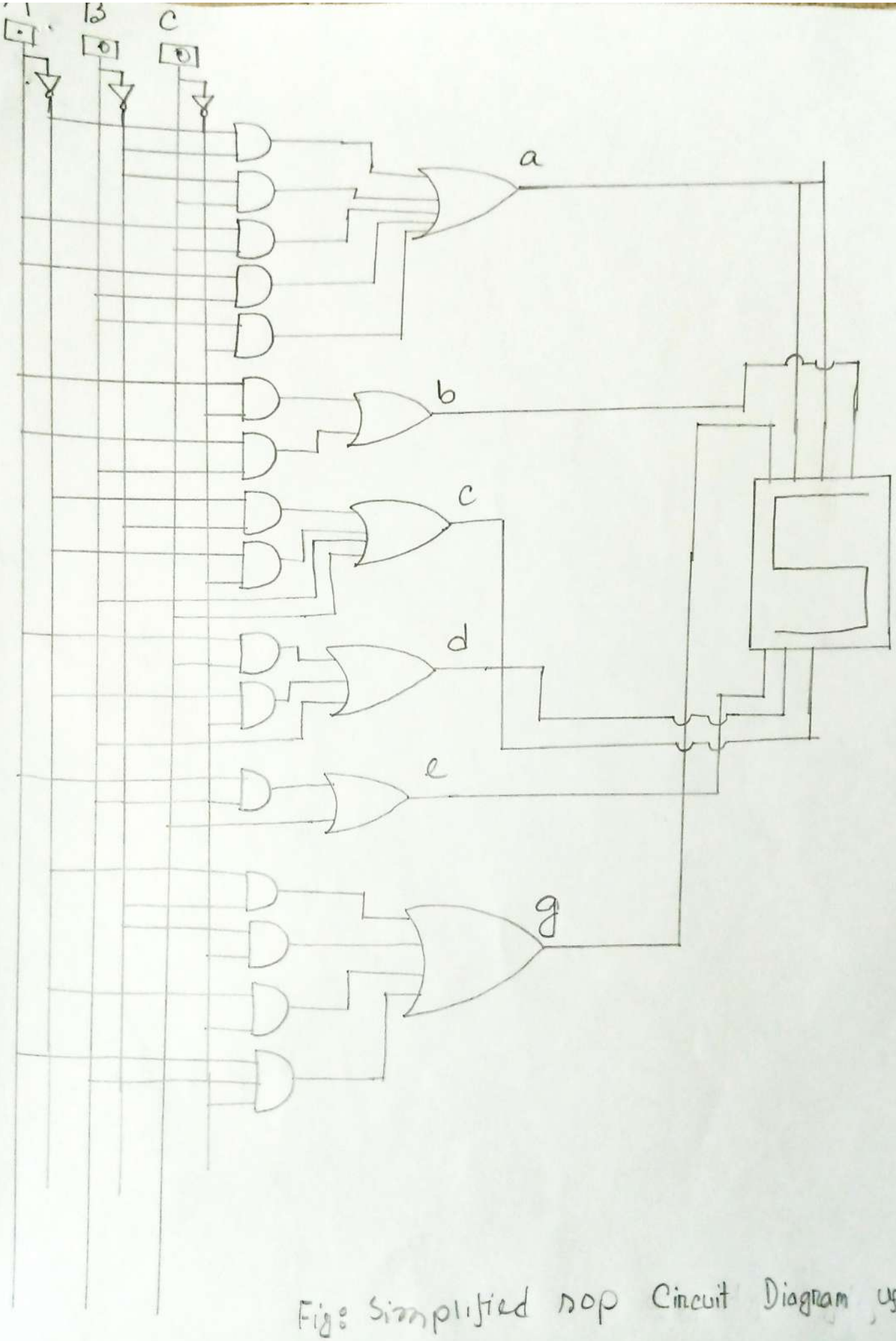


Fig: Simplified SOP Circuit Diagram using basic gates.

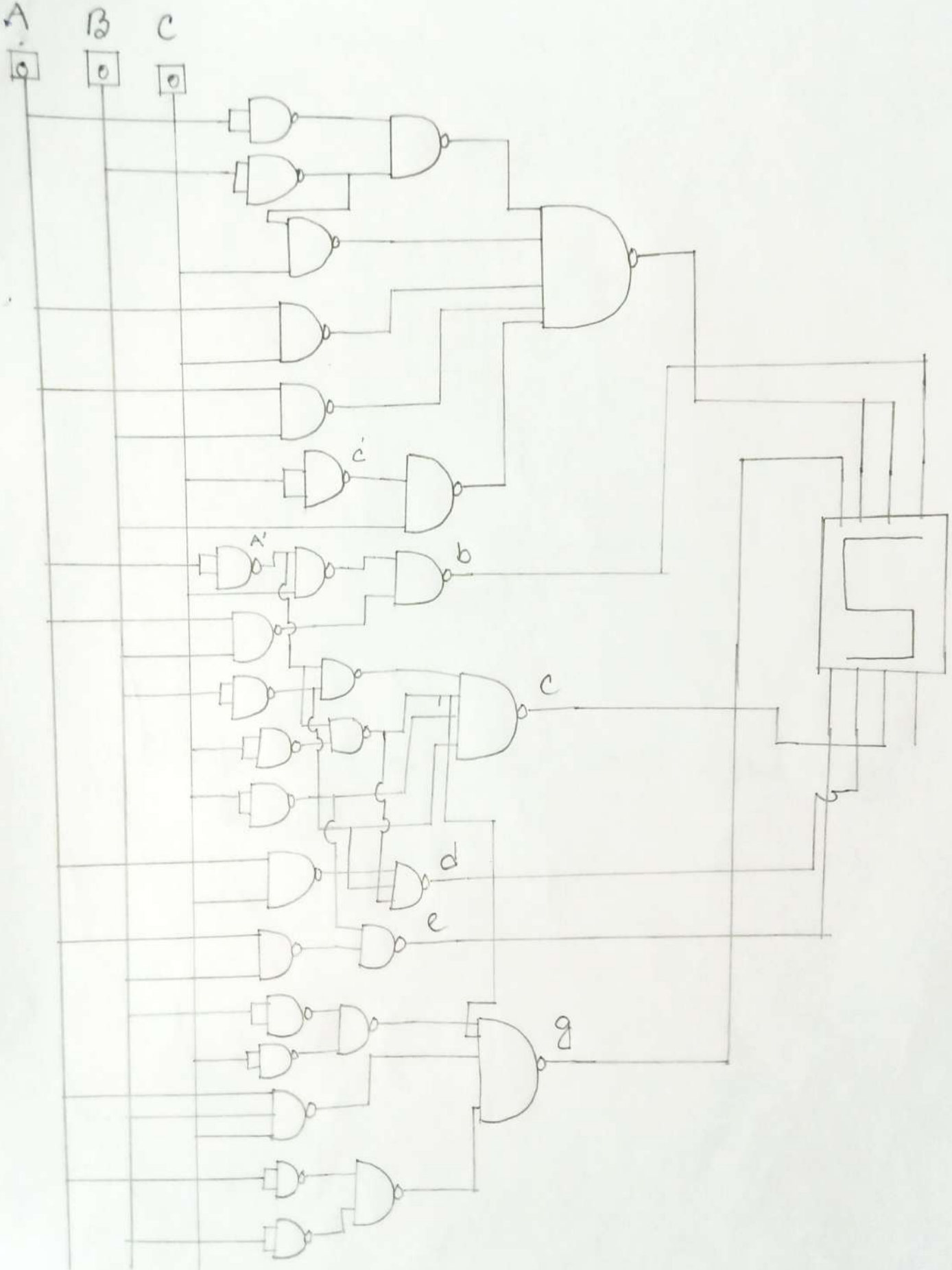


Fig: Simplified SOP Circuit Diagram using NAND gates.

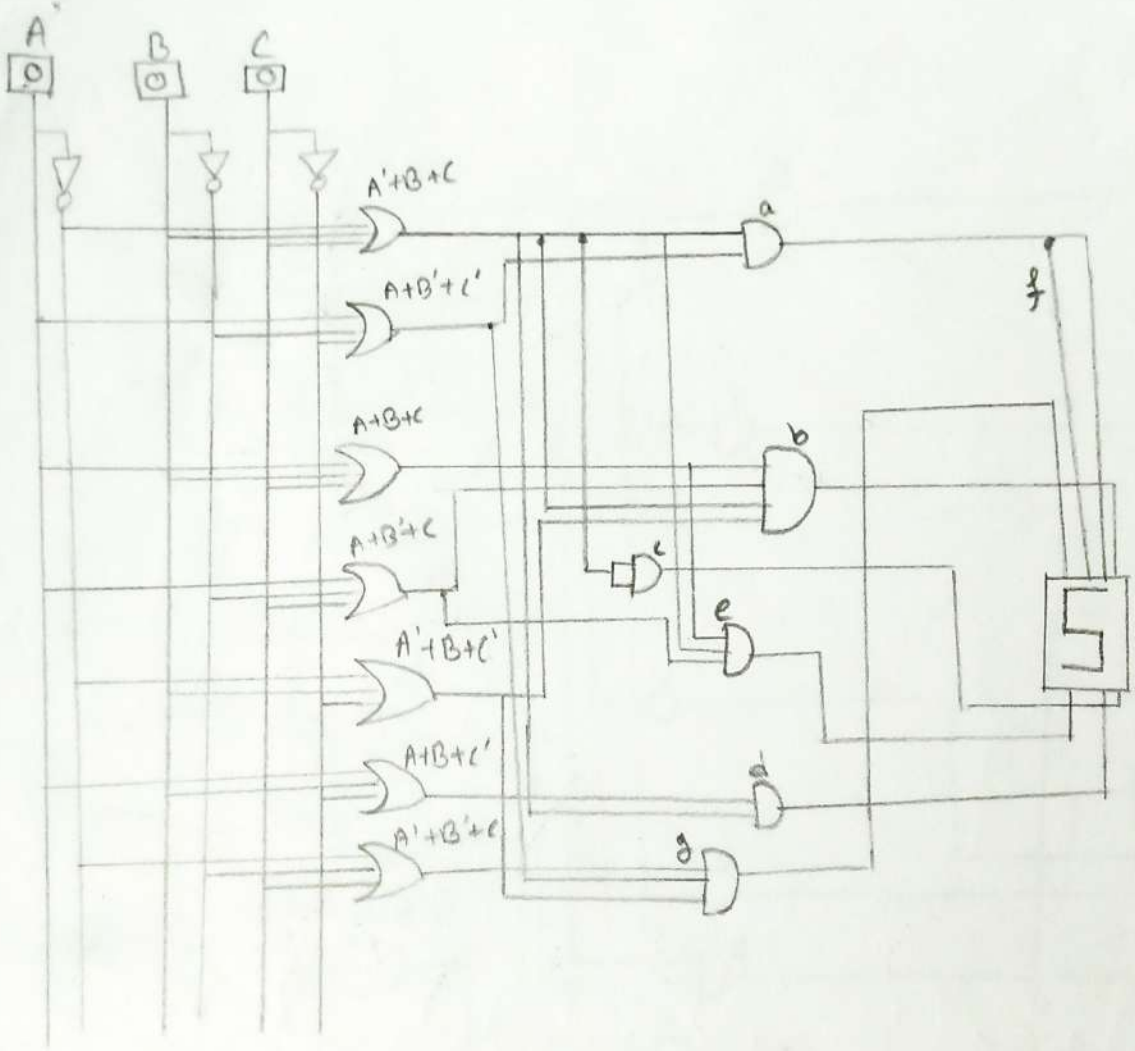


Fig: Generalized POS circuit diagram using basic gates.

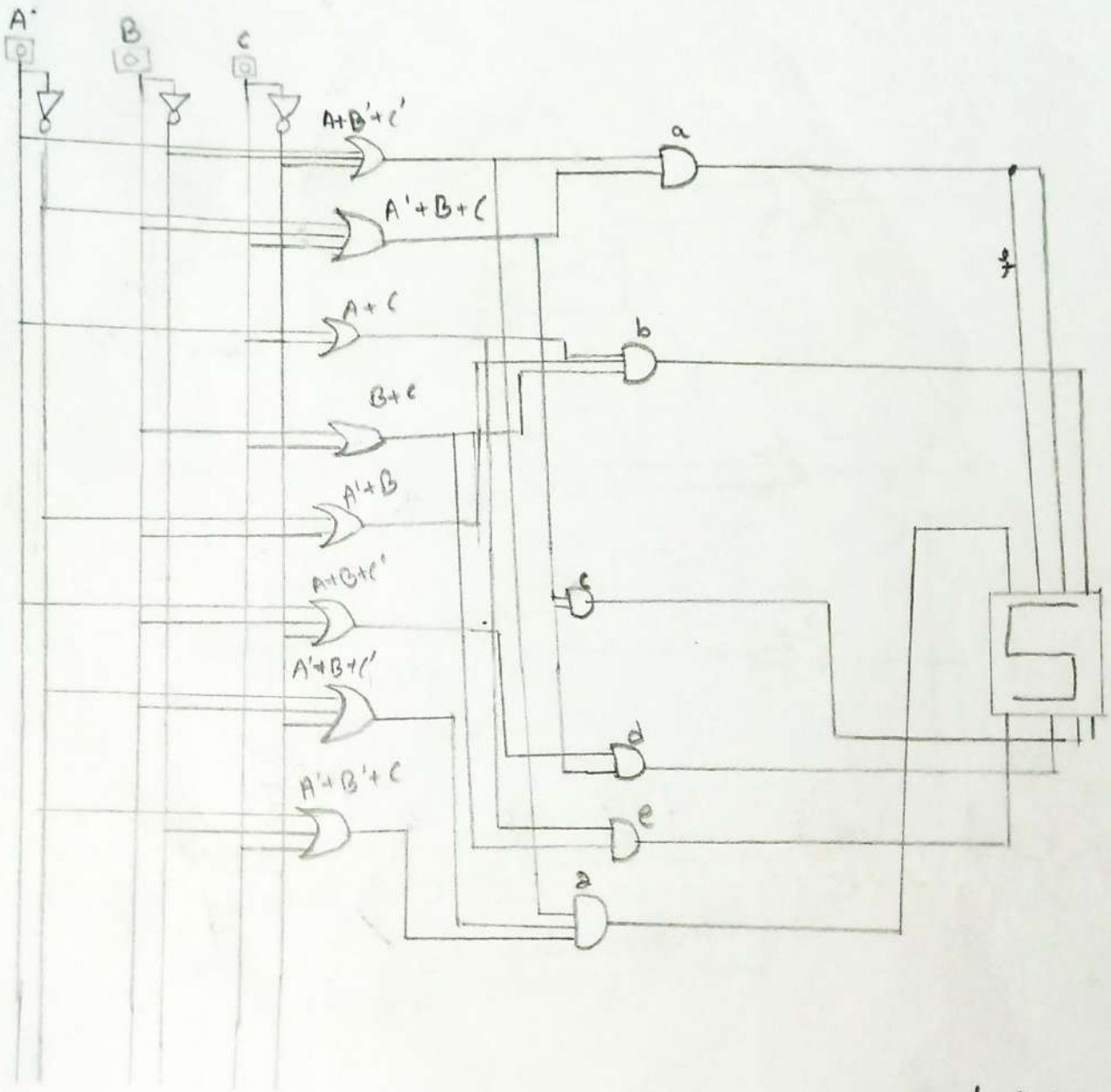
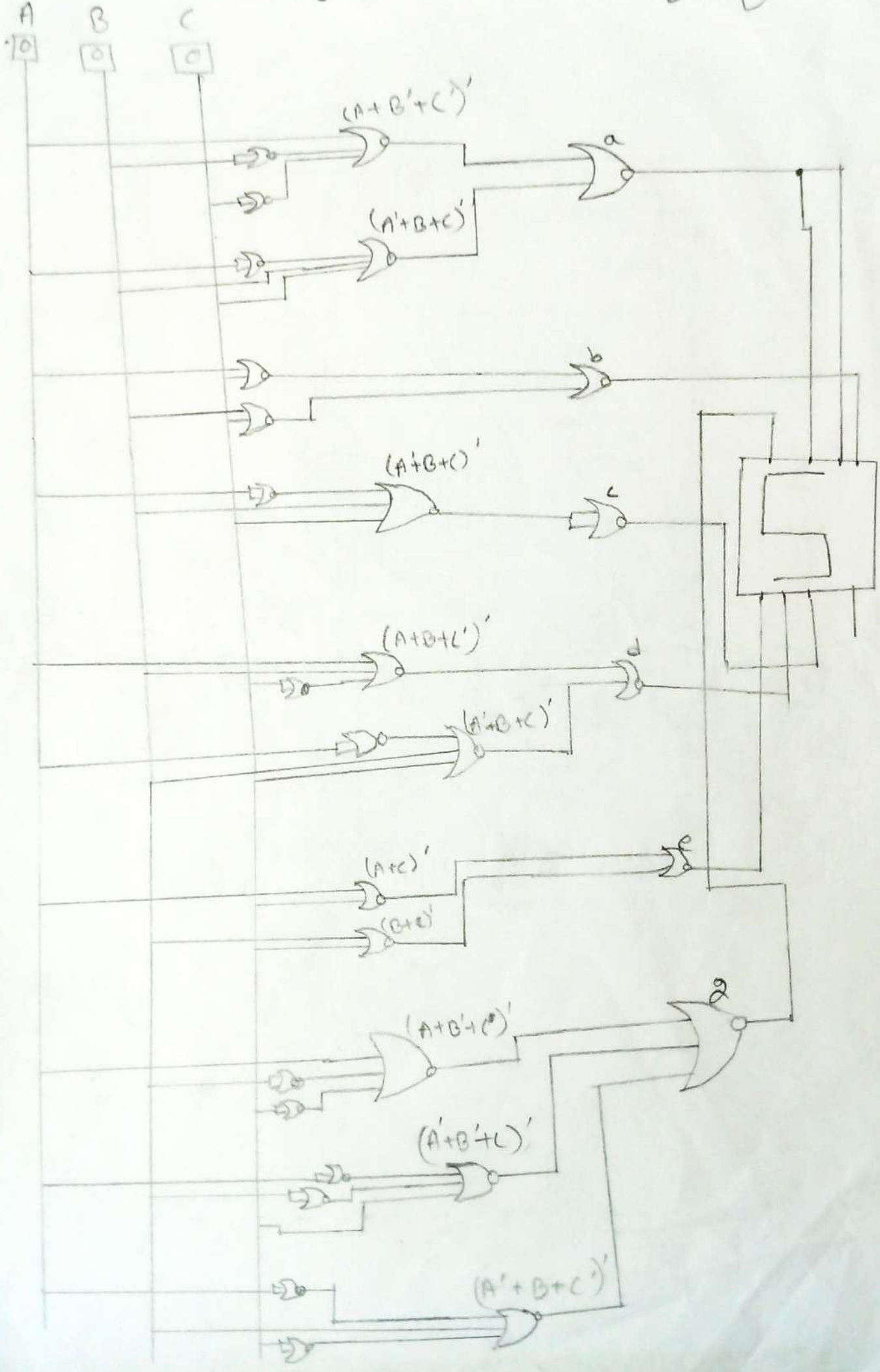


Fig: Simplified pos circuit Diagram using basic gates

Fig: Simplified POS using only NOR gates



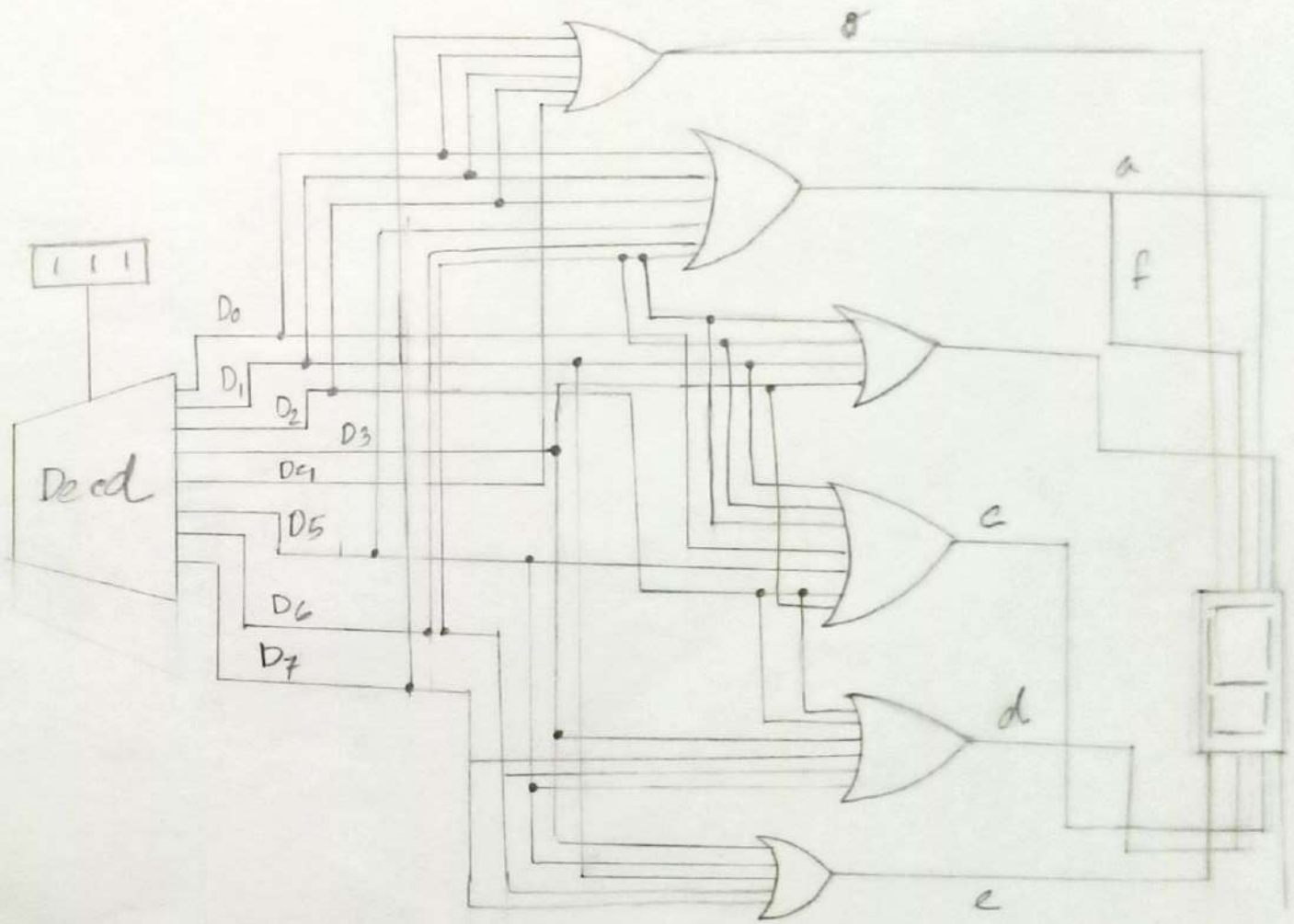


Fig: Generalized SOP Circuit Diagram using Decoder and OR gate.

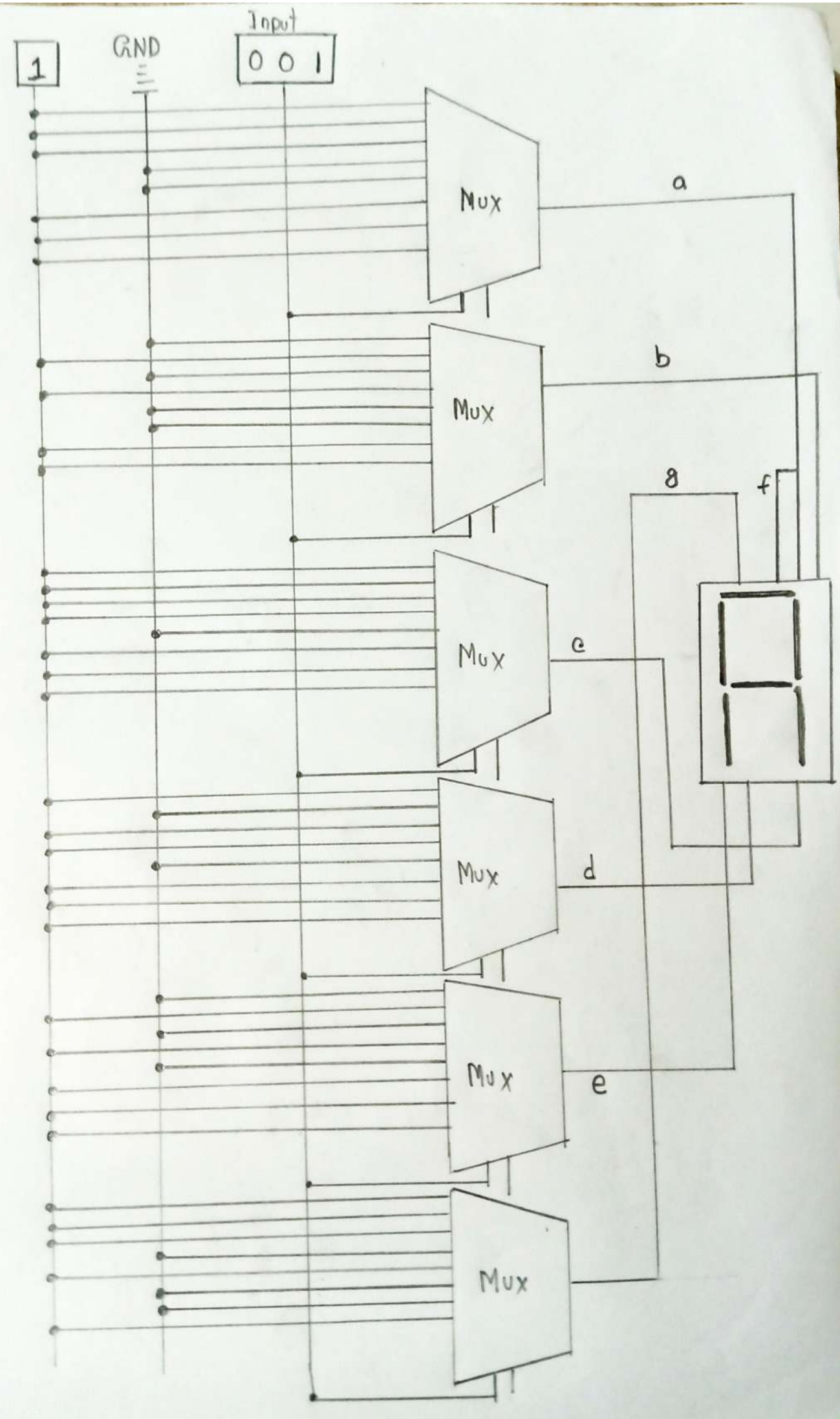


Fig:- Generalized SOP Multiplexer

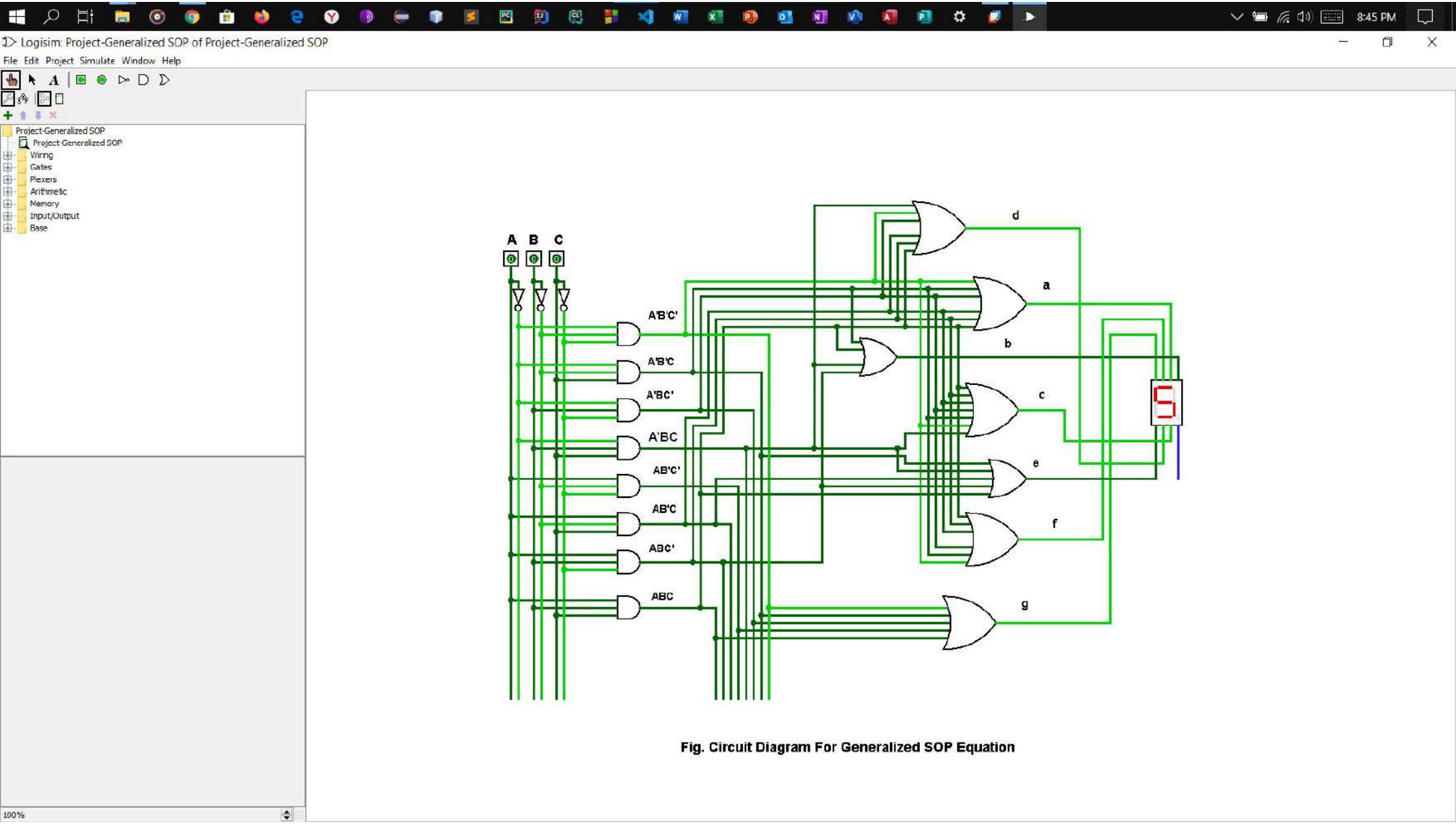


Fig. Circuit Diagram For Generalized SOP Equation

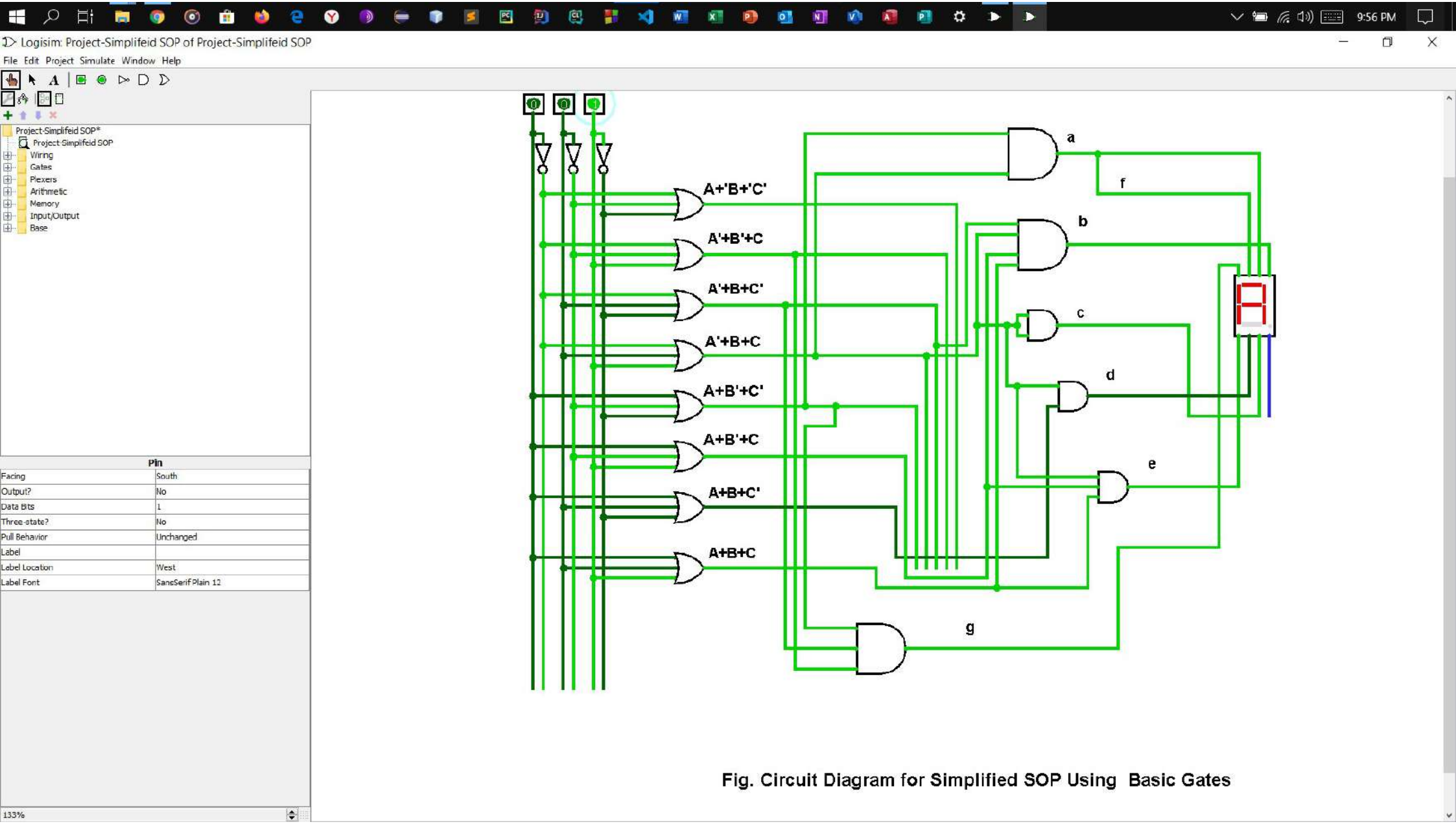


Fig. Circuit Diagram for Simplified SOP Using Basic Gates

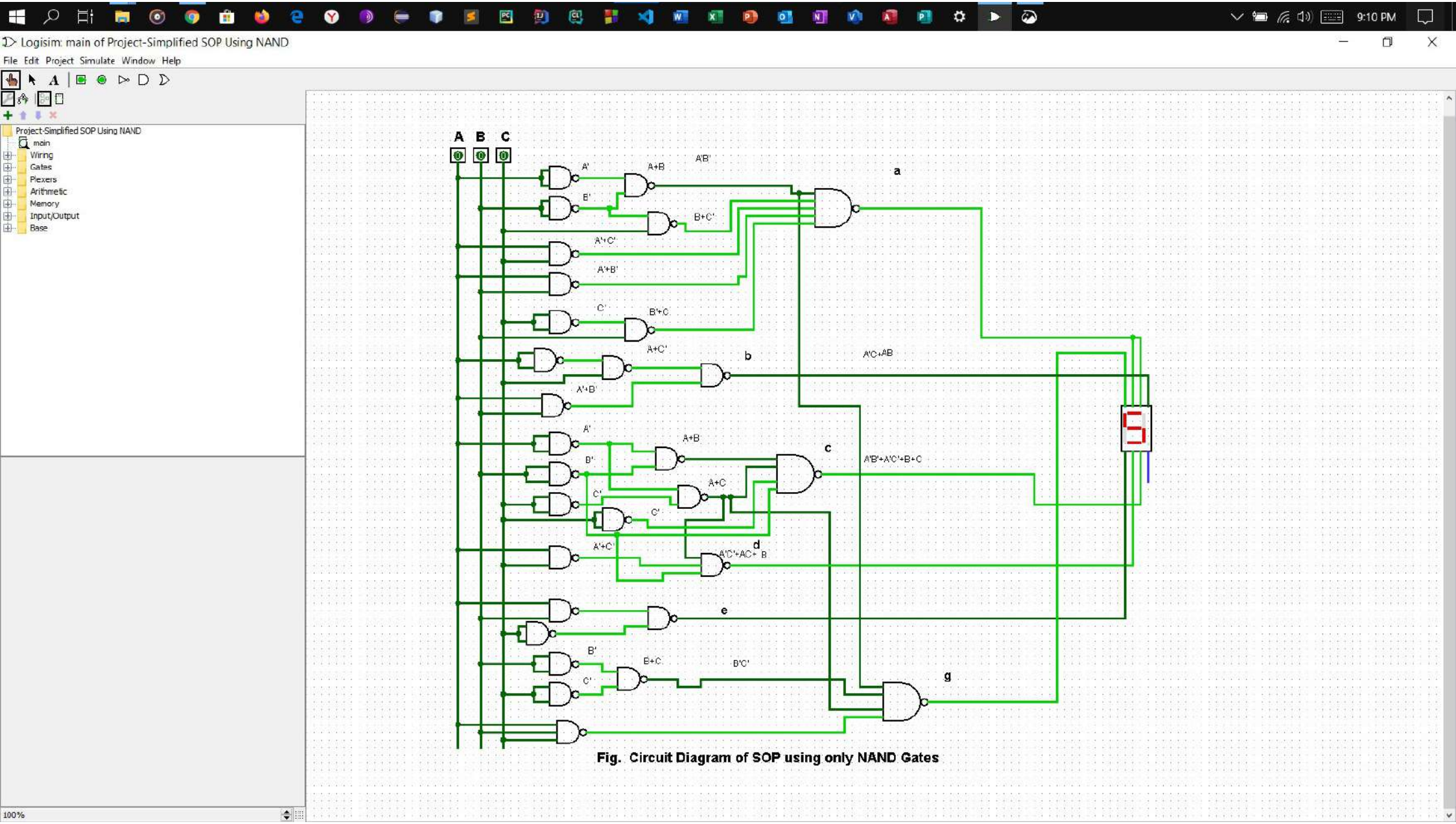


Fig. Circuit Diagram of SOP using only NAND Gates

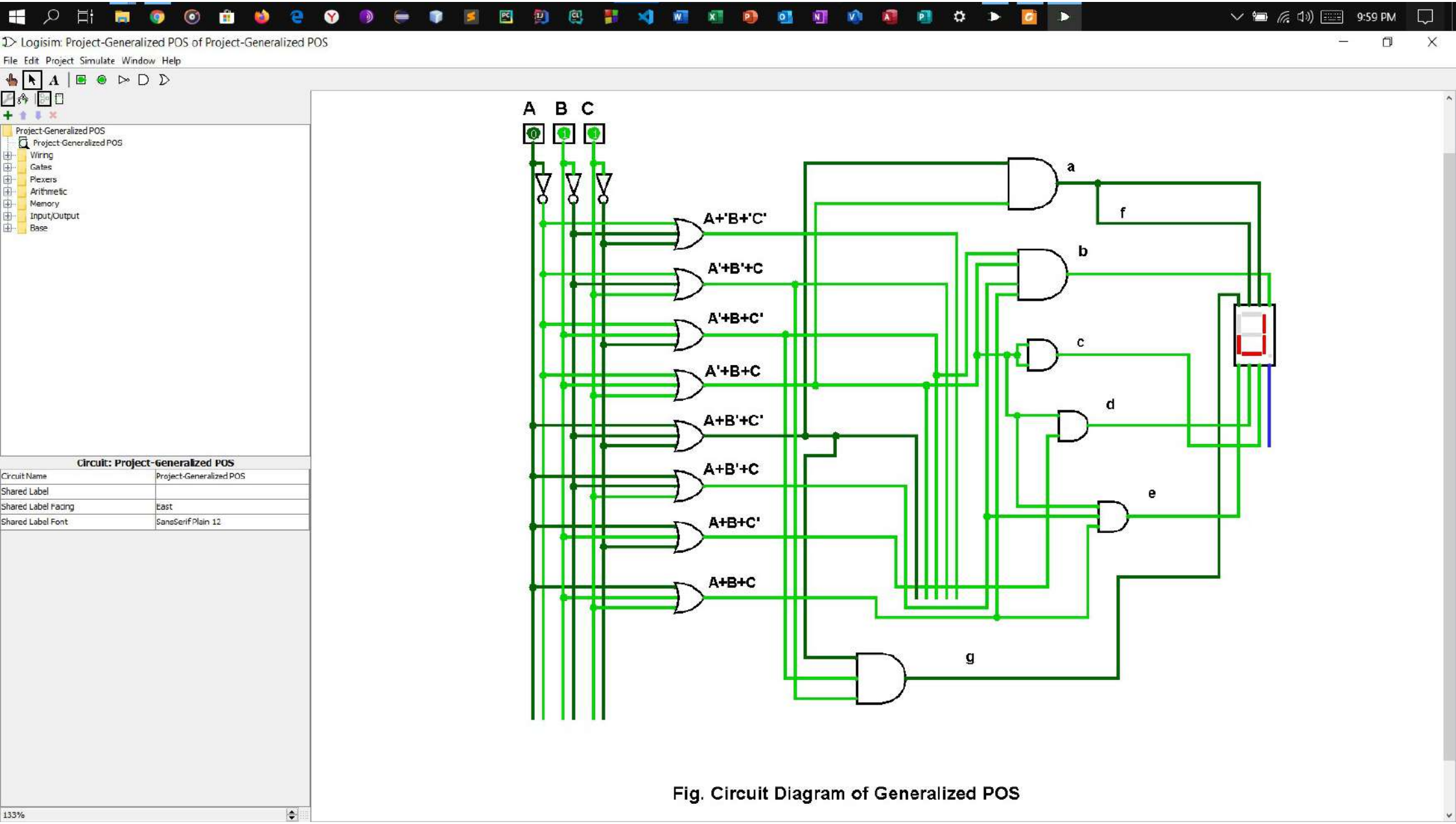


Fig. Circuit Diagram of Generalized POS

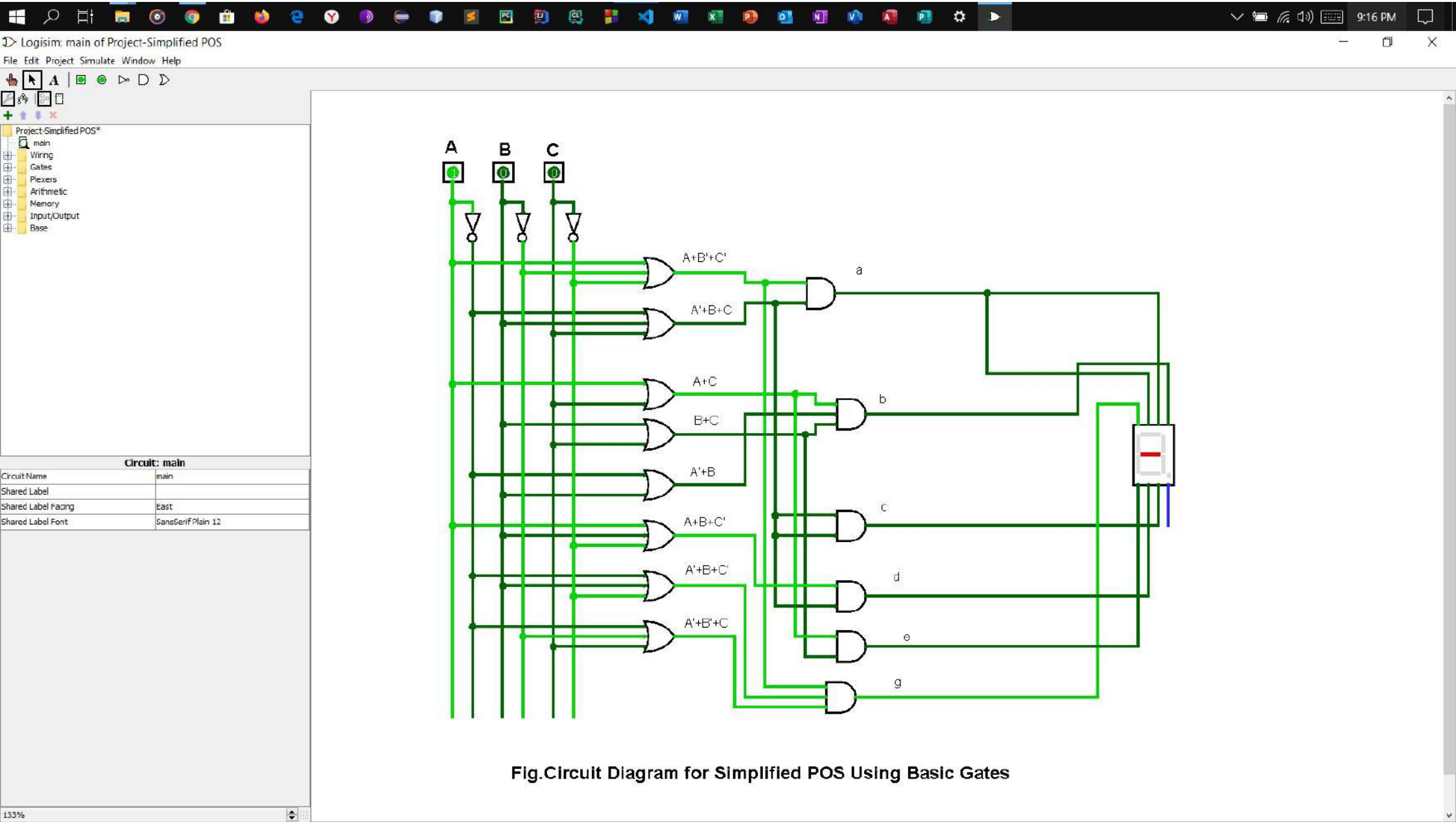


Fig.Circuit Diagram for Simplified POS Using Basic Gates

Logisim: Fig. Simplified POS using NOR gates of simple POS for only NOR

File Edit Project Simulate Window Help

simple POS for only NOR*

Circuit: Fig. Simplified POS using NOR gates

Circuit Name	Fig. Simplified POS using NOR gates
Shared Label	
Shared Label Facing	East
Shared Label Font	SansSerif Plain 12

75%

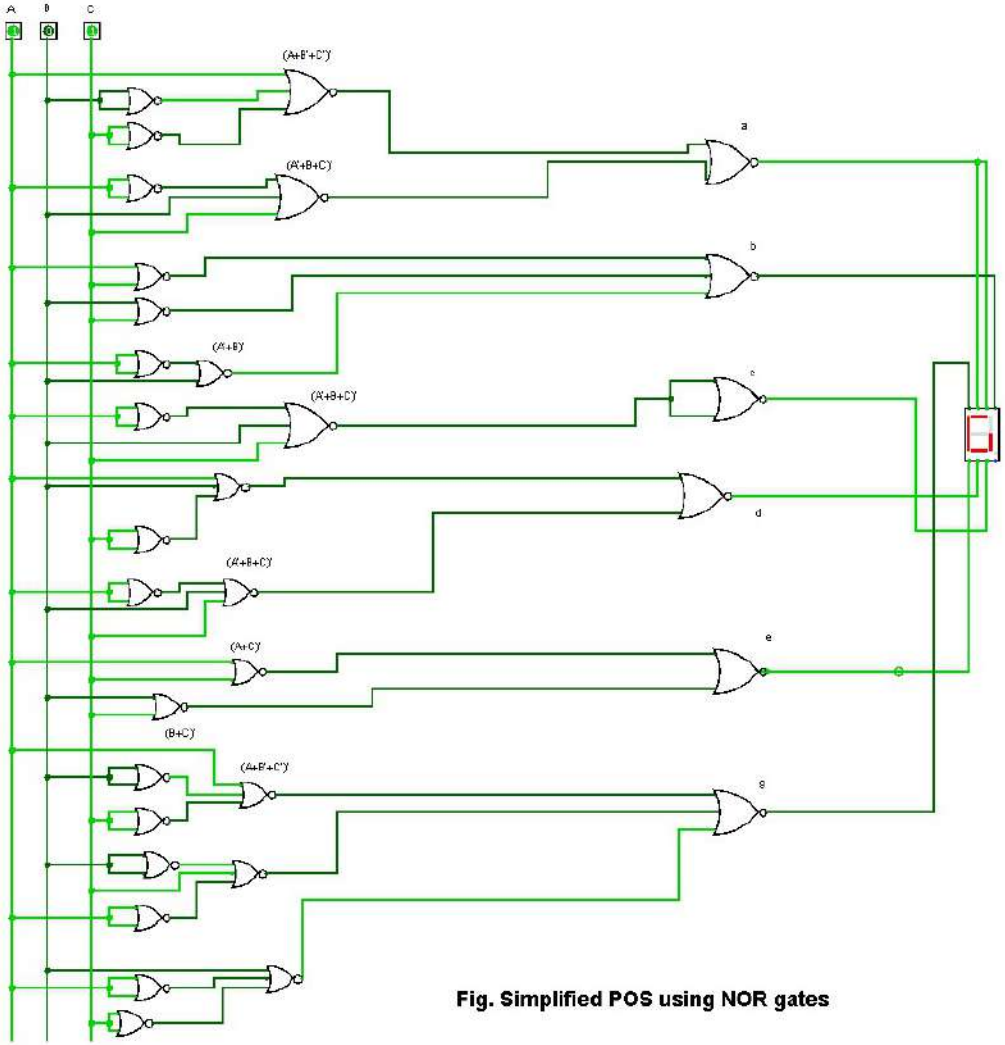


Fig. Simplified POS using NOR gates

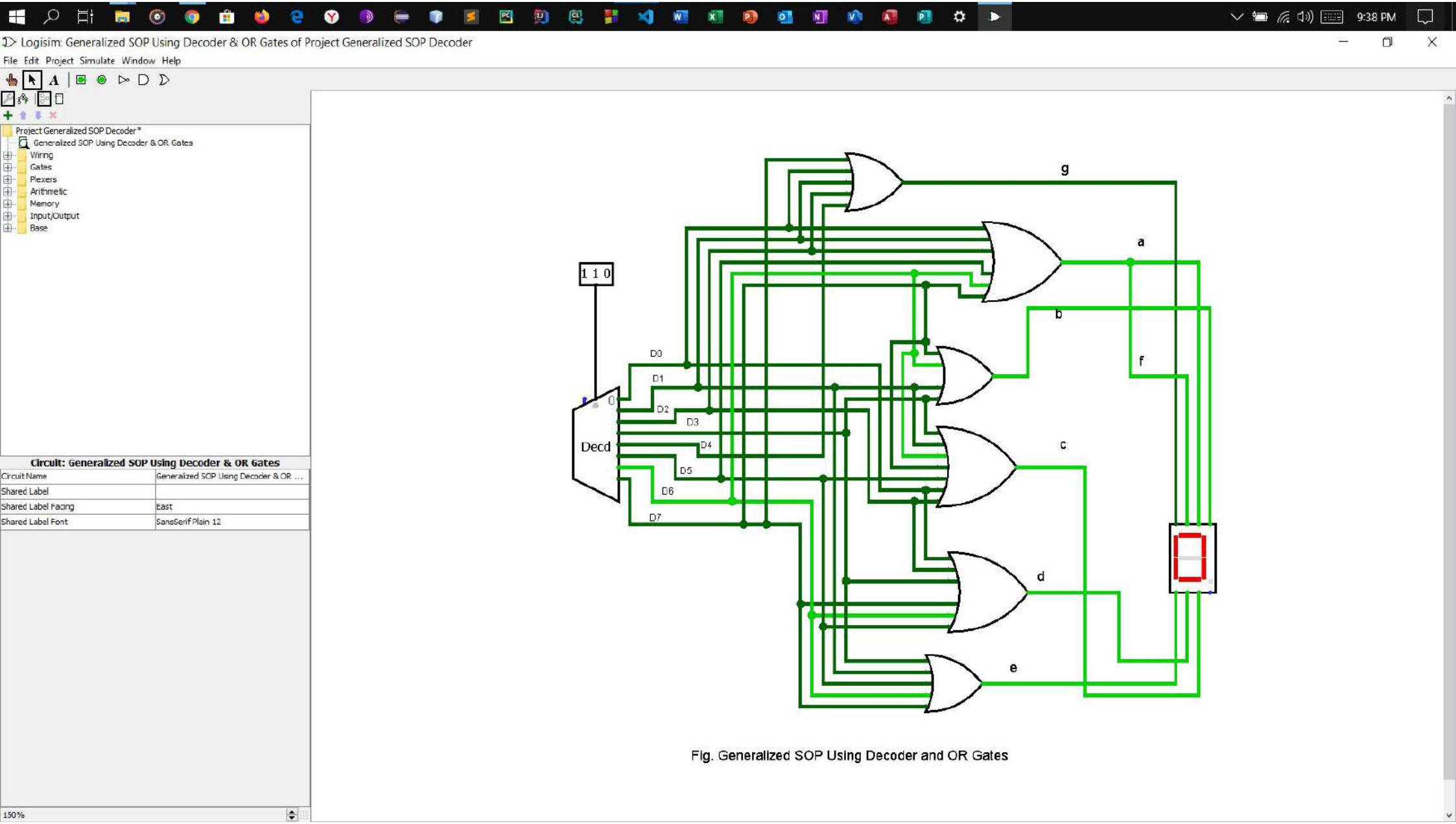
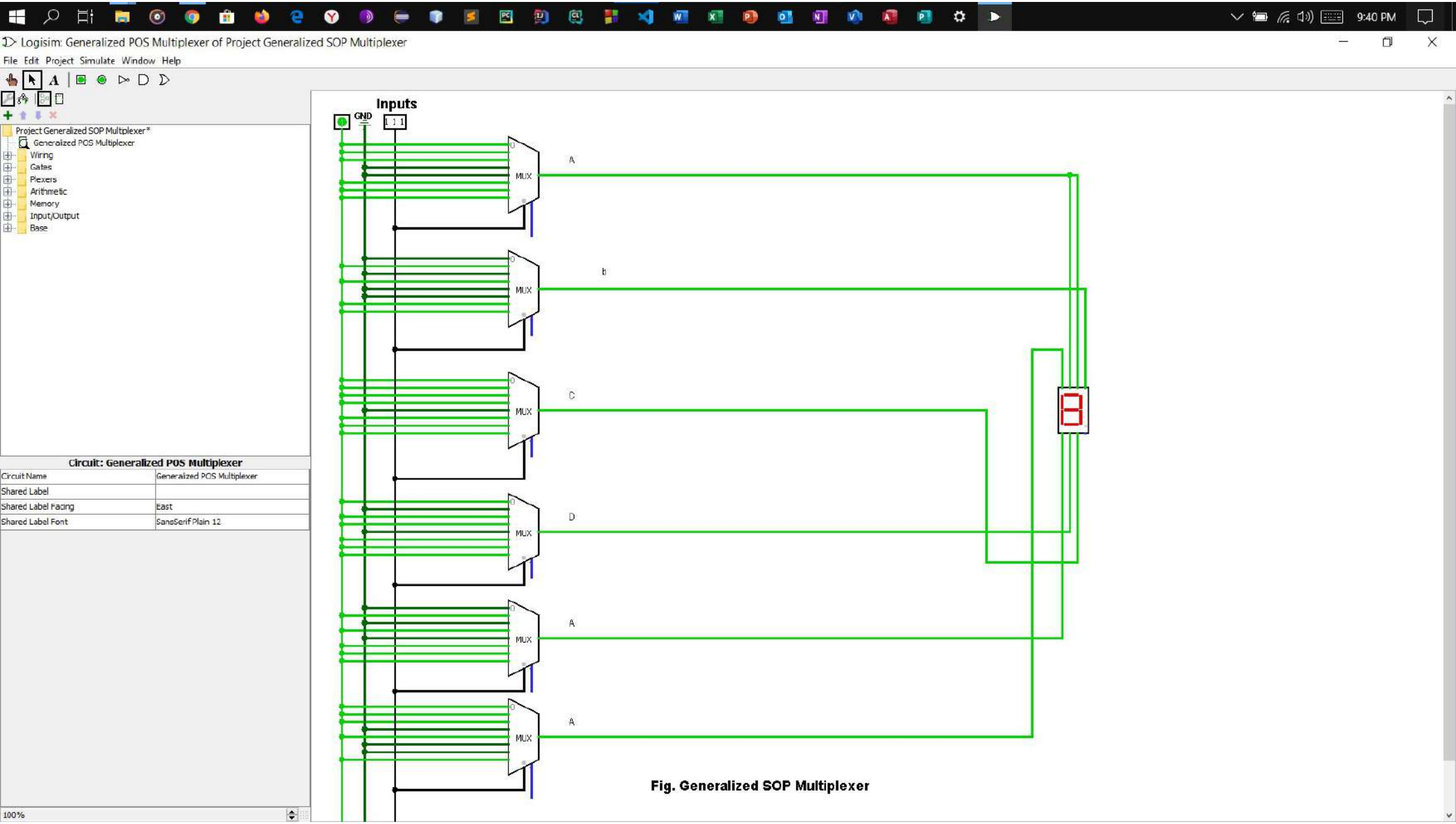
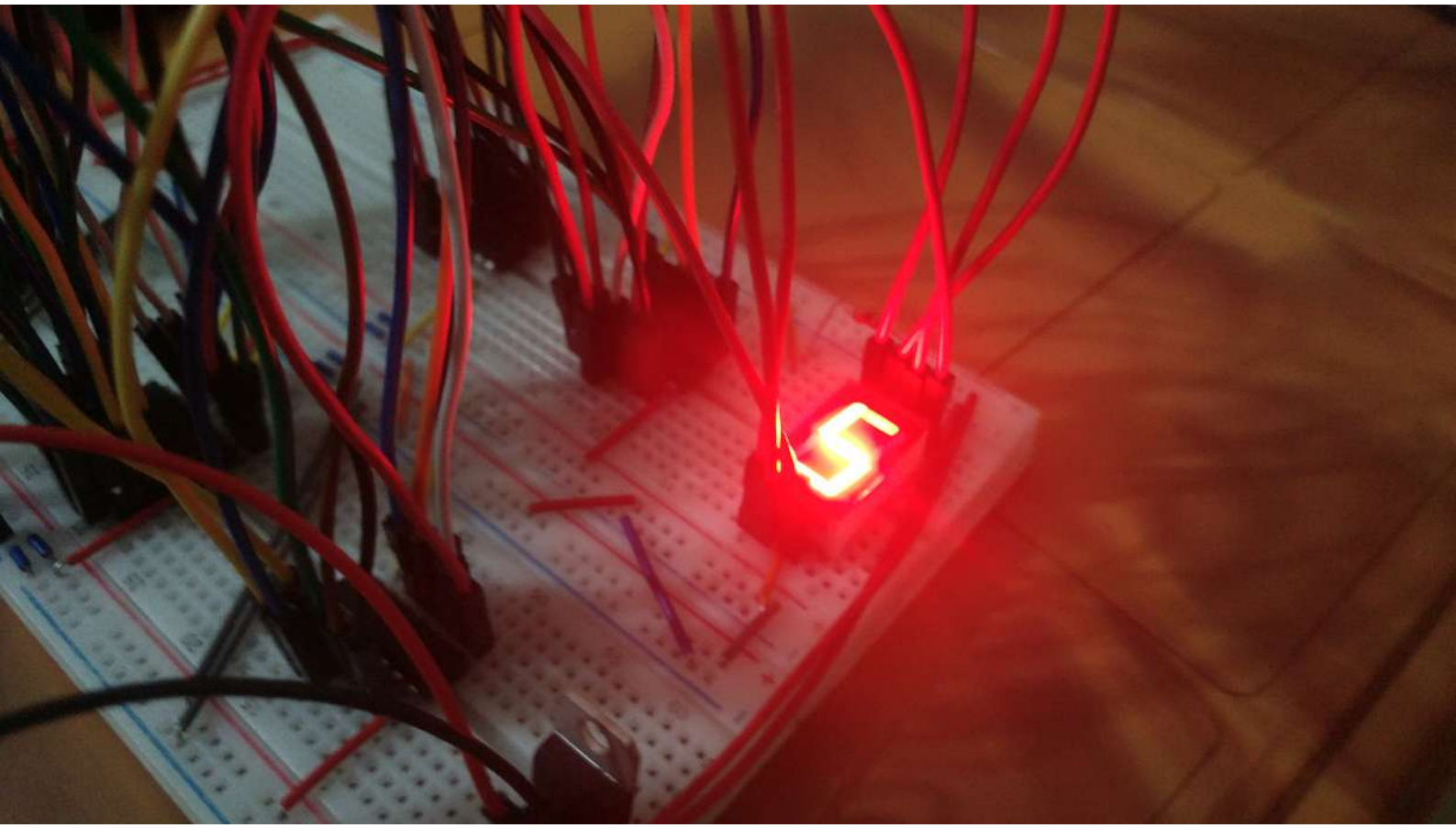
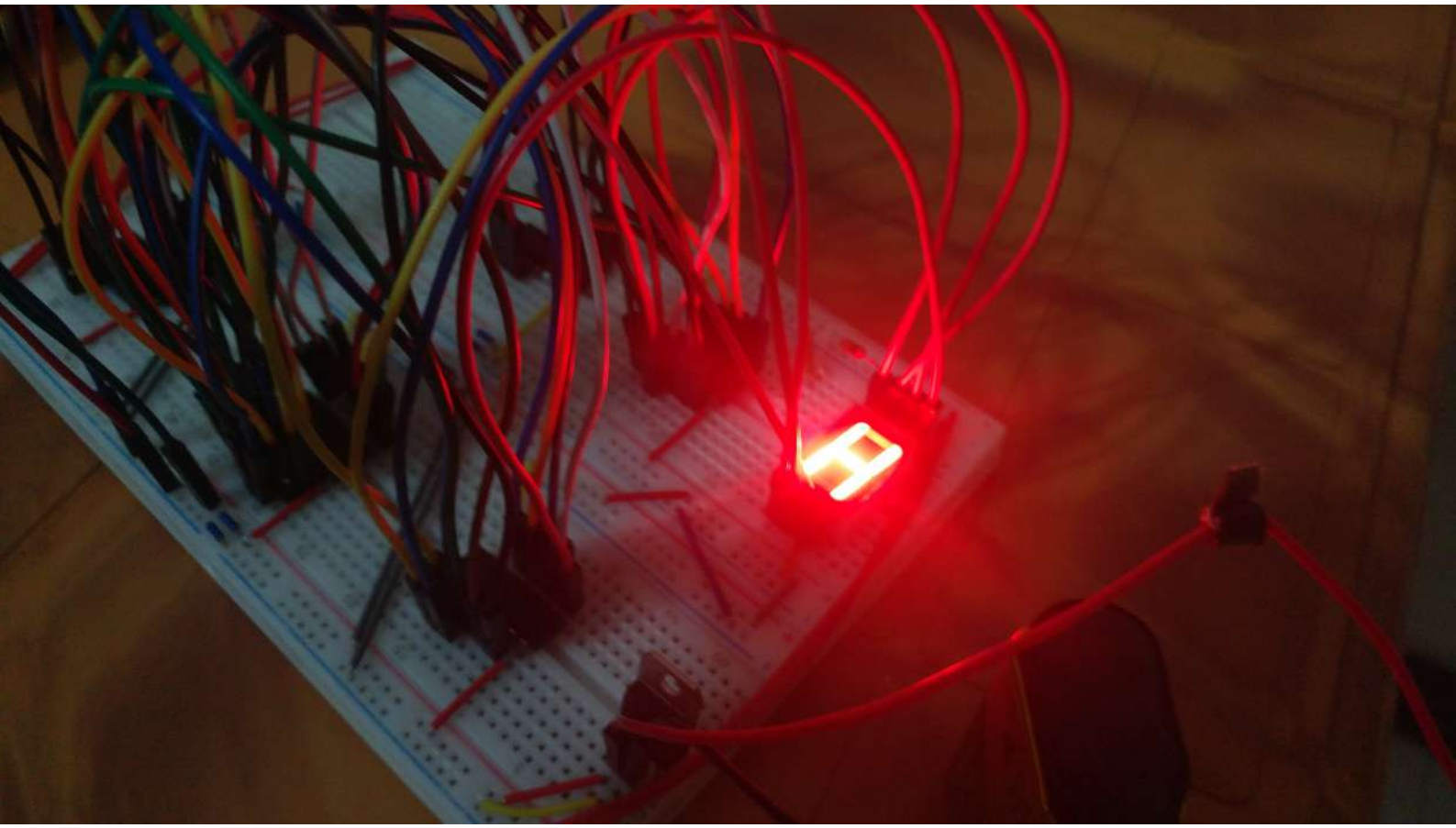
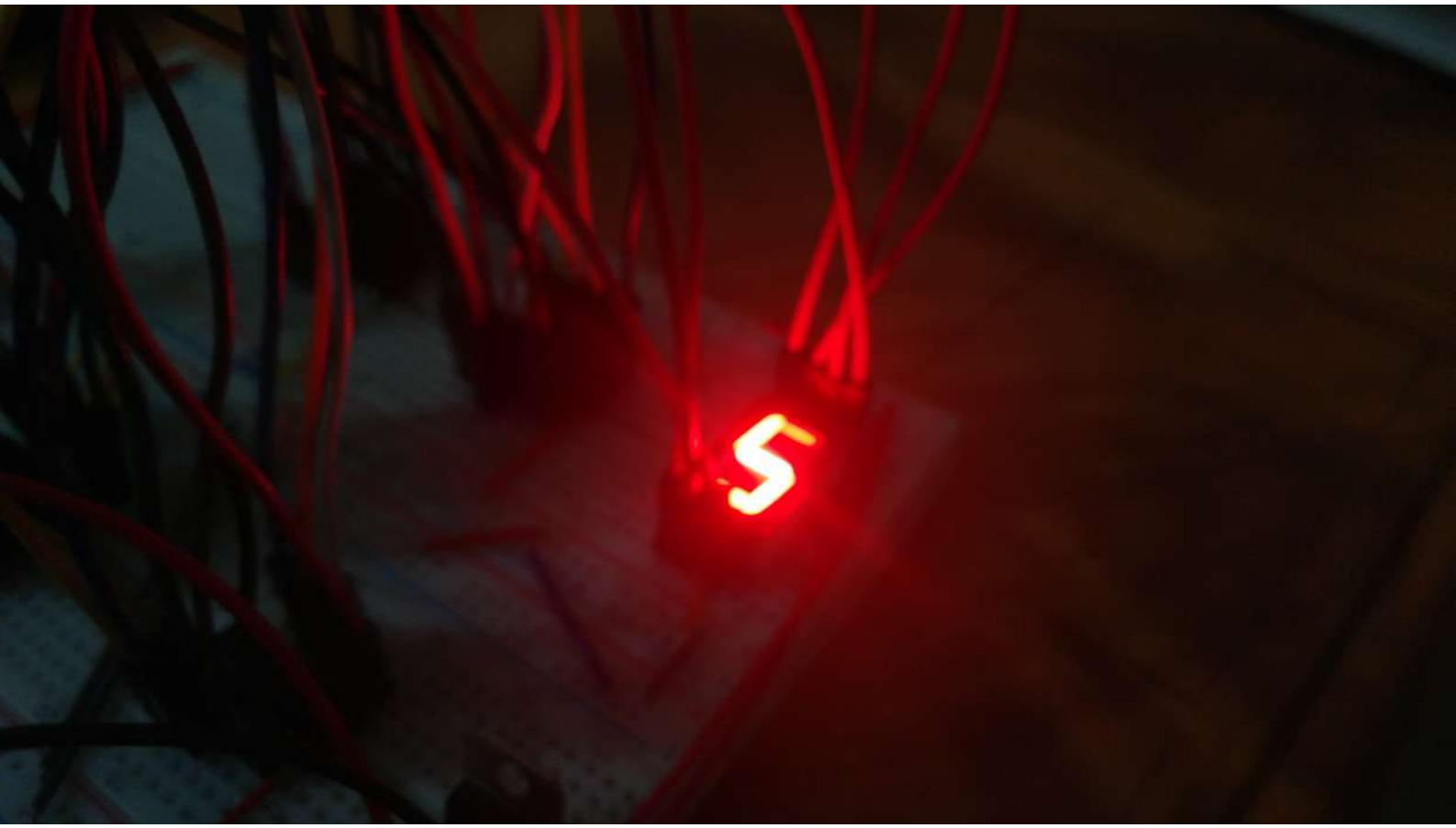


Fig. Generalized SOP Using Decoder and OR Gates


Logisim: Generalized POS Multiplexer of Project Generalized SOP Multiplexer
File Edit Project Simulate Window Help
Project Generalized SOP Multiplexer*
Generalized POS Multiplexer
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: Generalized POS Multiplexer
Circuit Name
Generalized POS Multiplexer
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
100%
Inputs
GND
MUX
A
b
C
D
A
A
Fig. Generalized SOP Multiplexer



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