Project Final Report
CSE 231

Digital Logic Design
Section 11
Workstation-08

Using sequential circuit print: **SASJ-G08** in 7 segment display

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North South University
Submitted To: Tanjila Farah(TnF)

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Sequential part of the project

Characteristic Table:

present State			Next State			T Flip-flop		
A(t)	B(t)	C(t)	A(t+1)	B(t+1)	C(t+1)	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Excitation table: T-Flipflop:

Q	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

K-map:

$T_A = B(t)C(t)$

	B'(t)C'(t)	B'(t)C(t)	B(t)C(t)	B(t)C'(t)
A'(t)	0 (0)	0 (1)	1 (3)	0 (2)
A(t)	0 (4)	0 (5)	1 (7)	0 (6)

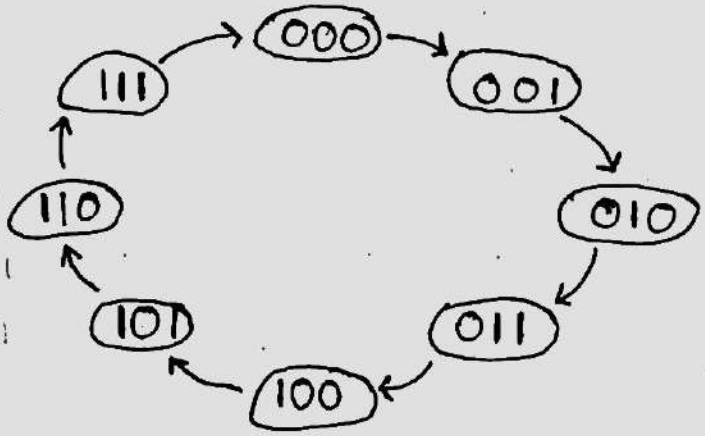
$T_B = C(t)$

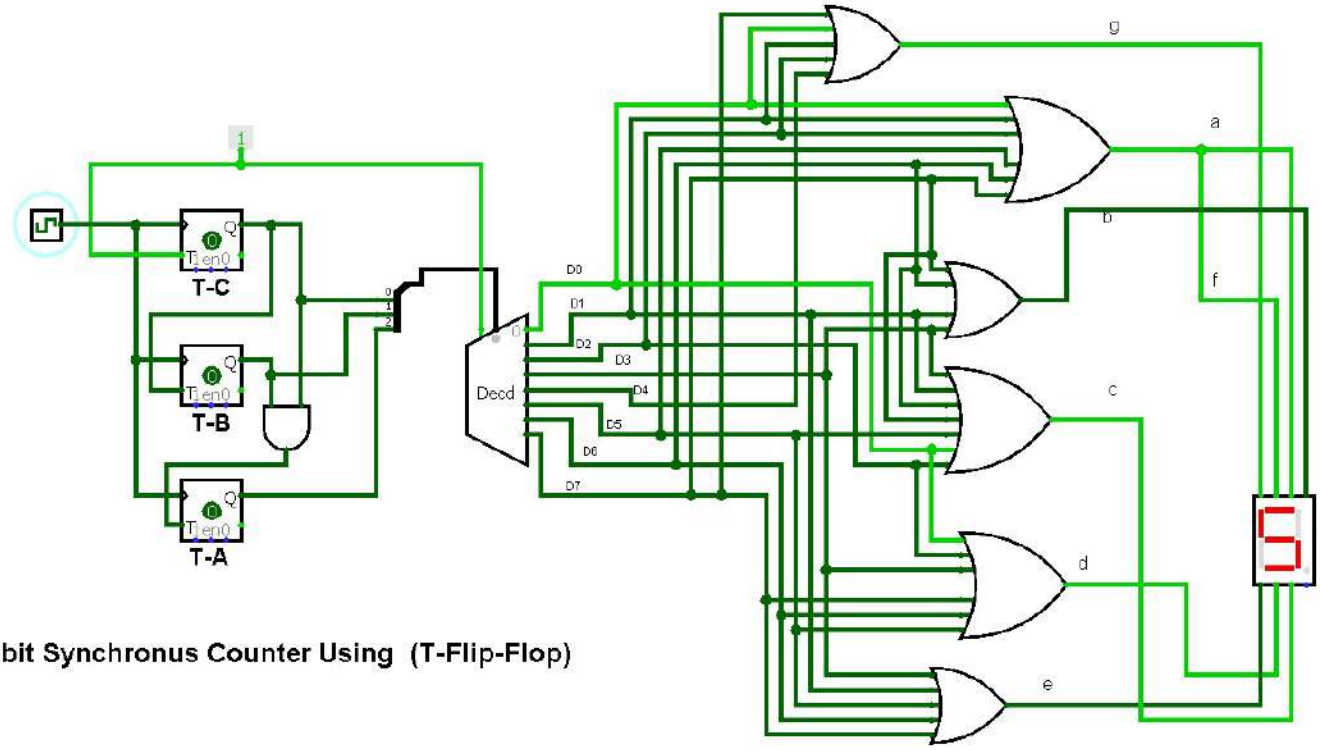
	B'(t)C'(t)	B'(t)C(t)	B(t)C(t)	B(t)C'(t)
A'(t)	0 (0)	1 (1)	1 (3)	0 (2)
A(t)	0 (4)	1 (5)	1 (7)	0 (6)

$T_C = 1$

	$B'(t)C'(t)$	$B'(t)C(t)$	$B(t)C(t)$	$B(t)C'(t)$
$A'(t)$	1 (0)	1 (1)	1 (3)	1 (2)
$A(t)$	1 (4)	1 (5)	1 (7)	1 (6)

State Diagram:





MEMORY-3bit Synchronus Counter Using (T-Flip-Flop)

Fig. Generalized SOP Sequential Circuit Using Decoder,AND gate,OR gates,T-flip-flops

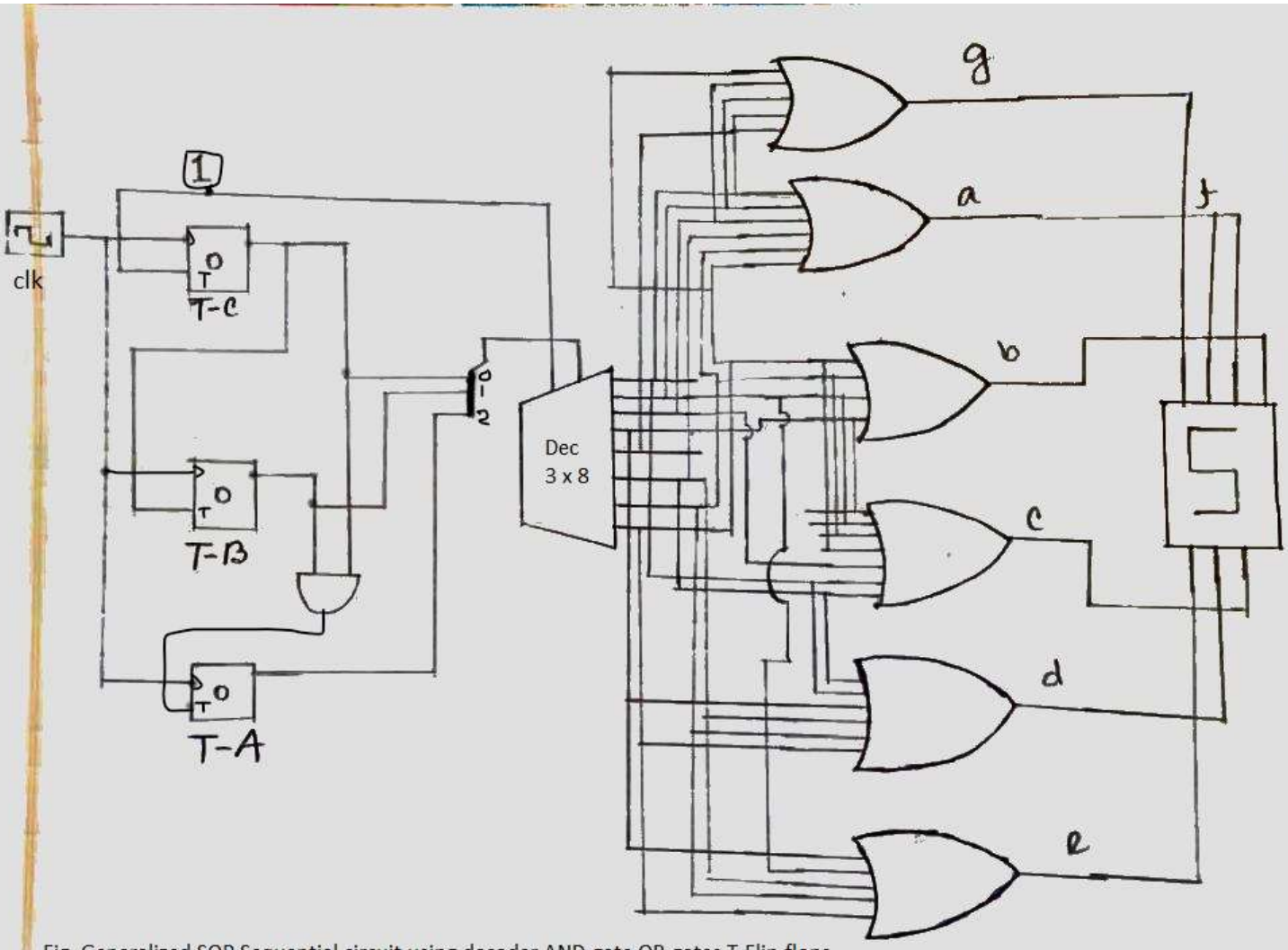
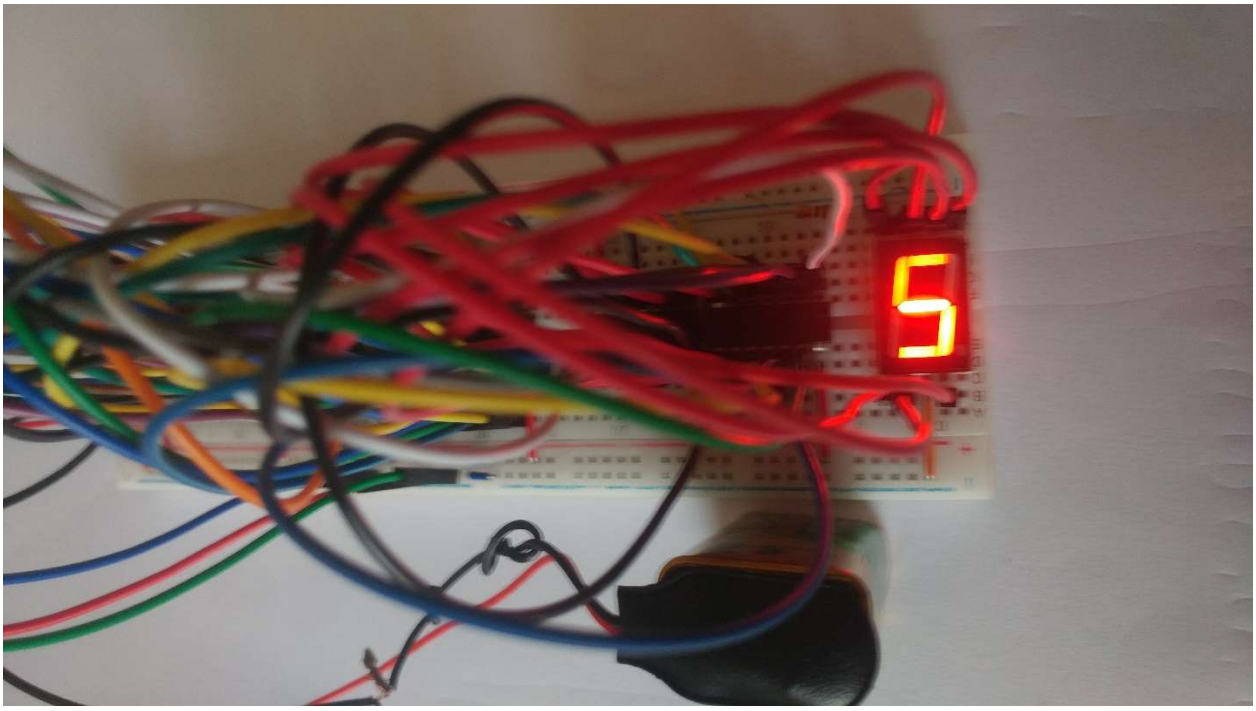
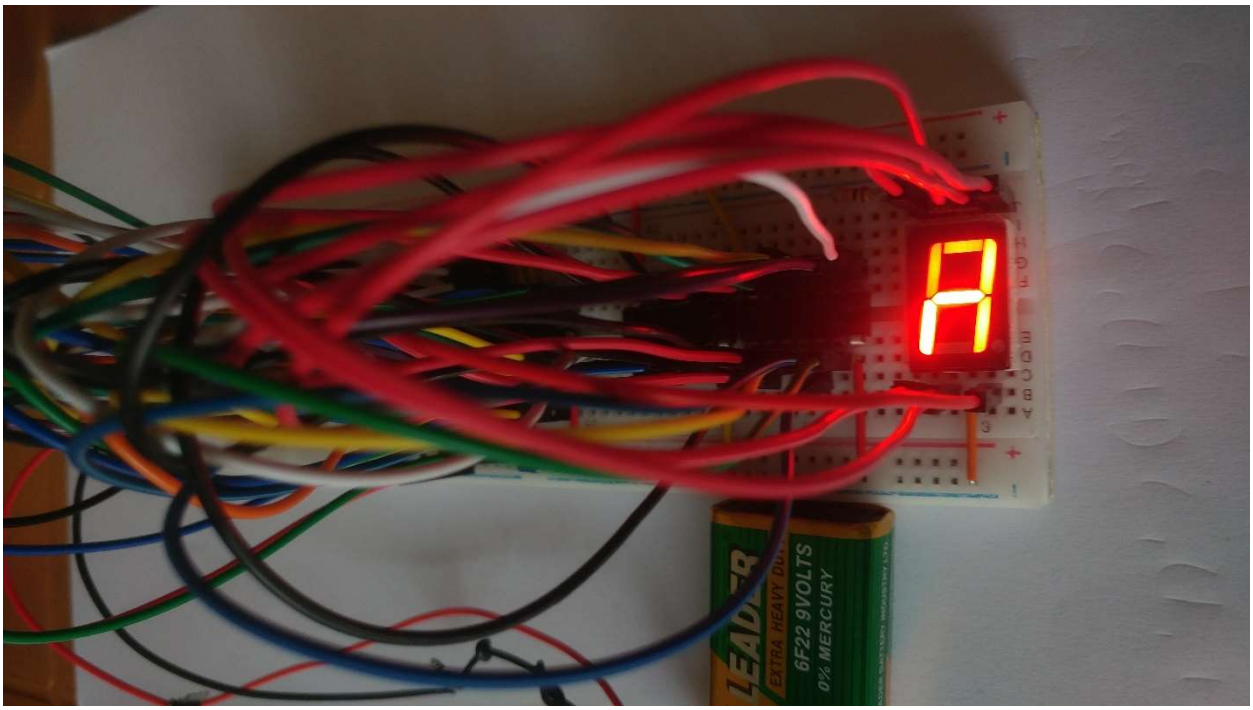


Fig. Generalized SOP Sequential circuit using decoder,AND-gate,OR-gates,T-Flip-flops

“”””” Pictures of Hardware Part “””””

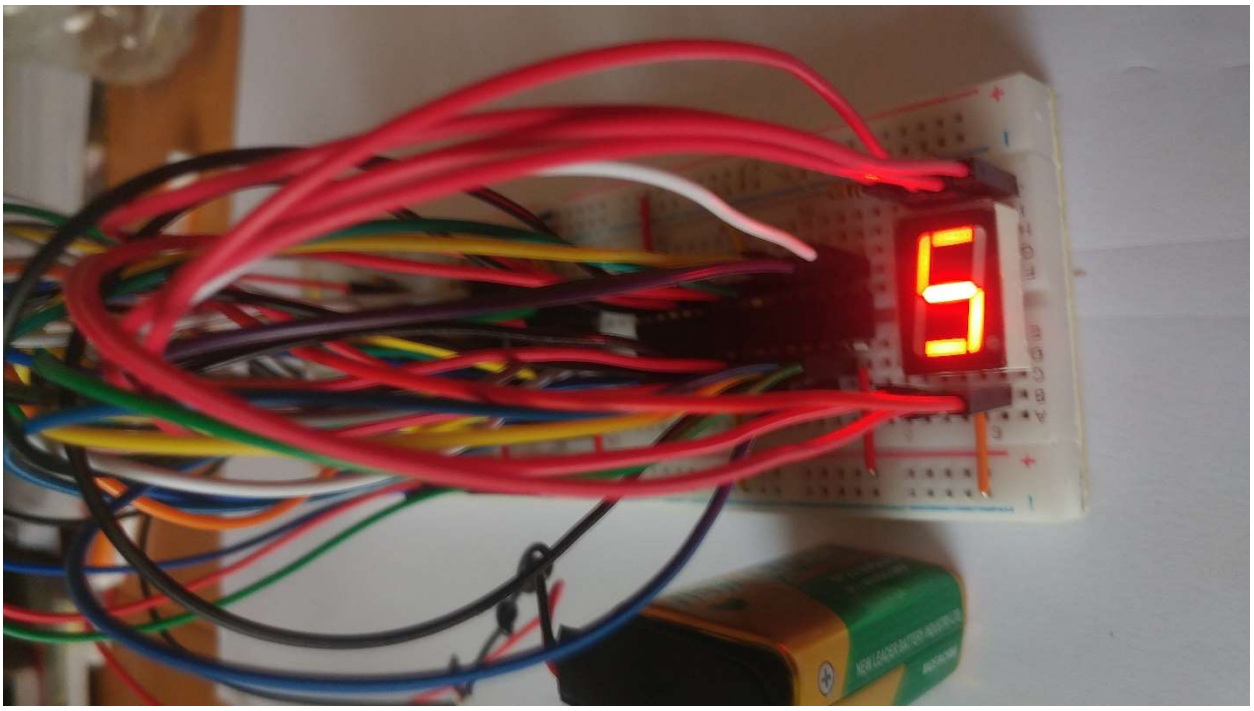


Input-: 0 0 0

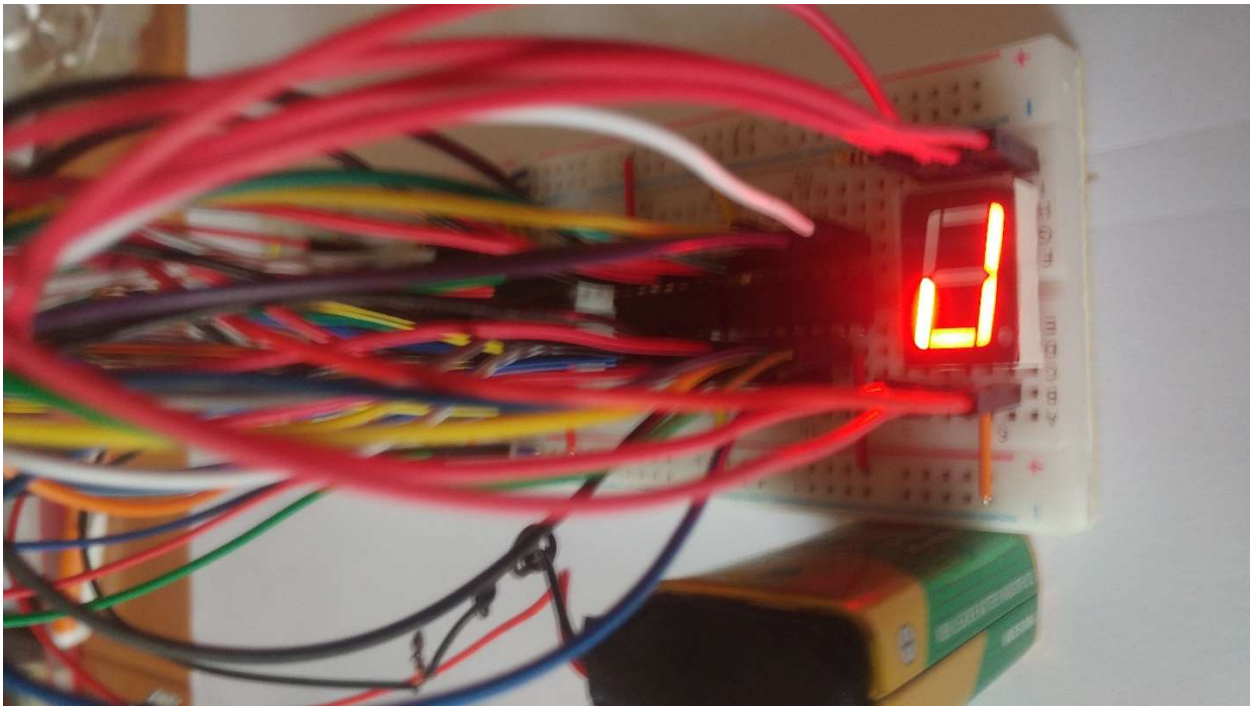


Input-: 0 0 1

“”””” Pictures of Hardware Part “””””

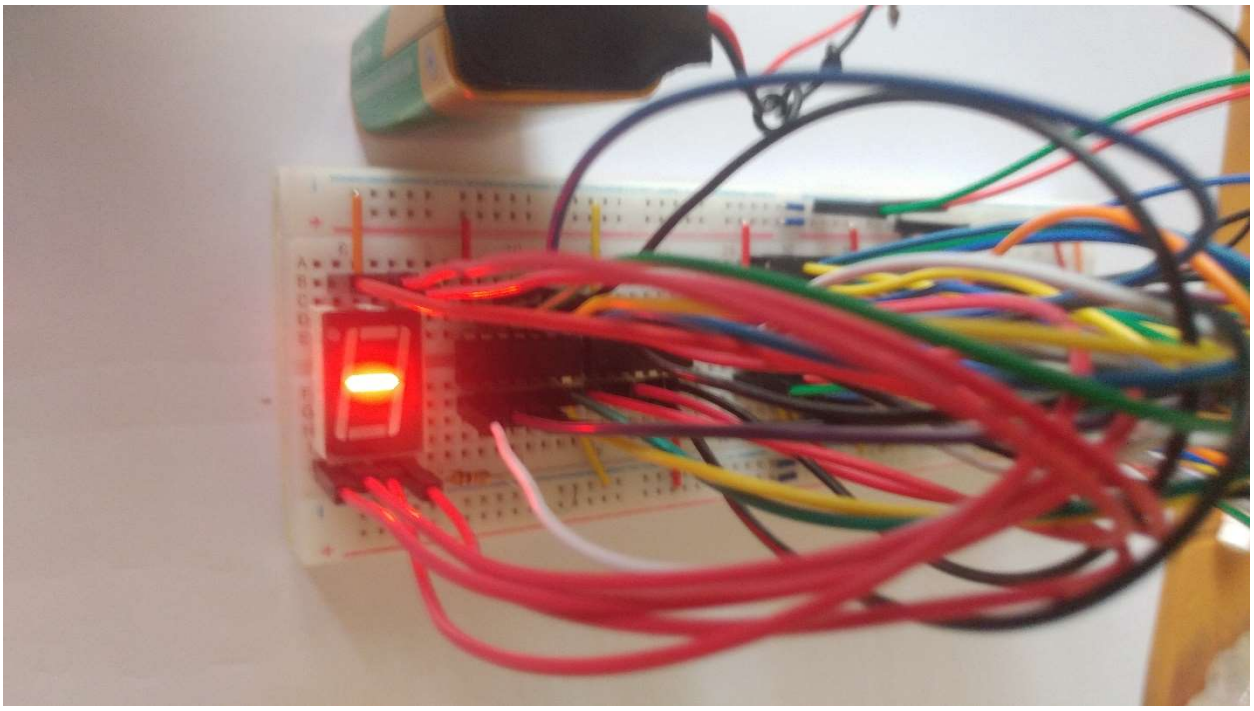


Input-: 0 1 0

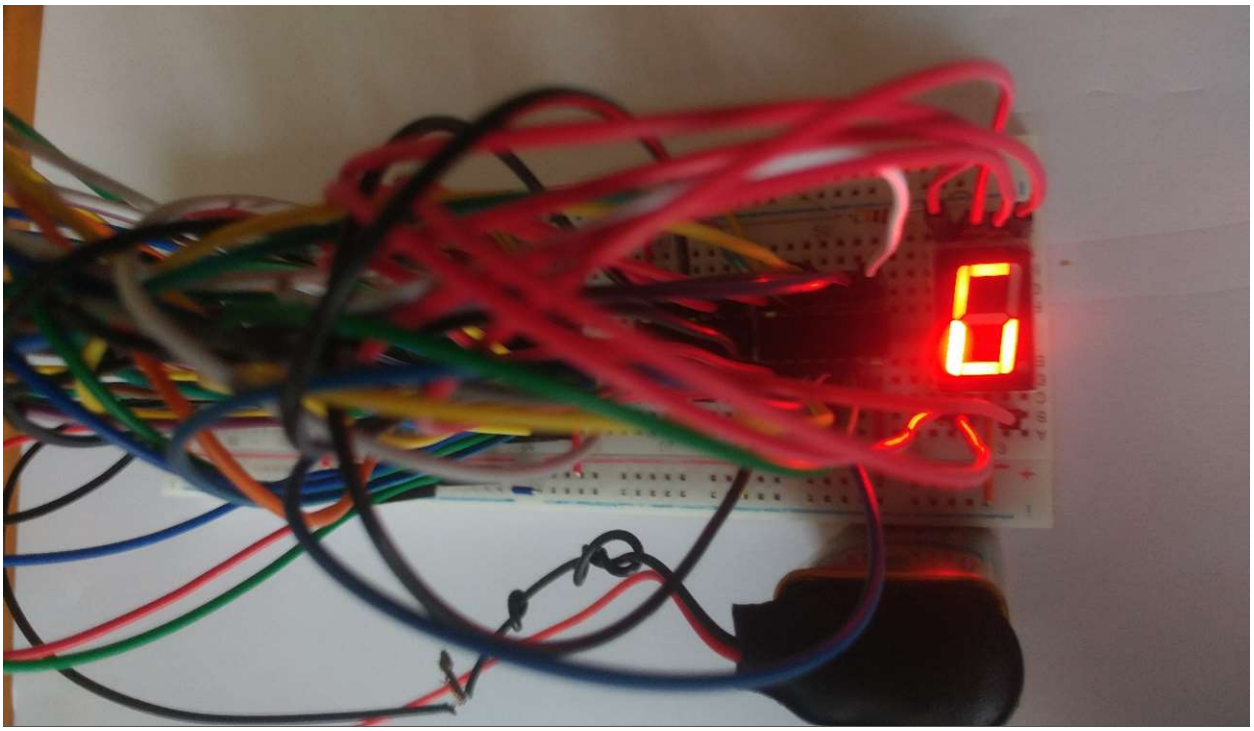


Input-: 0 1 1

“”””” Pictures of Hardware Part “””””

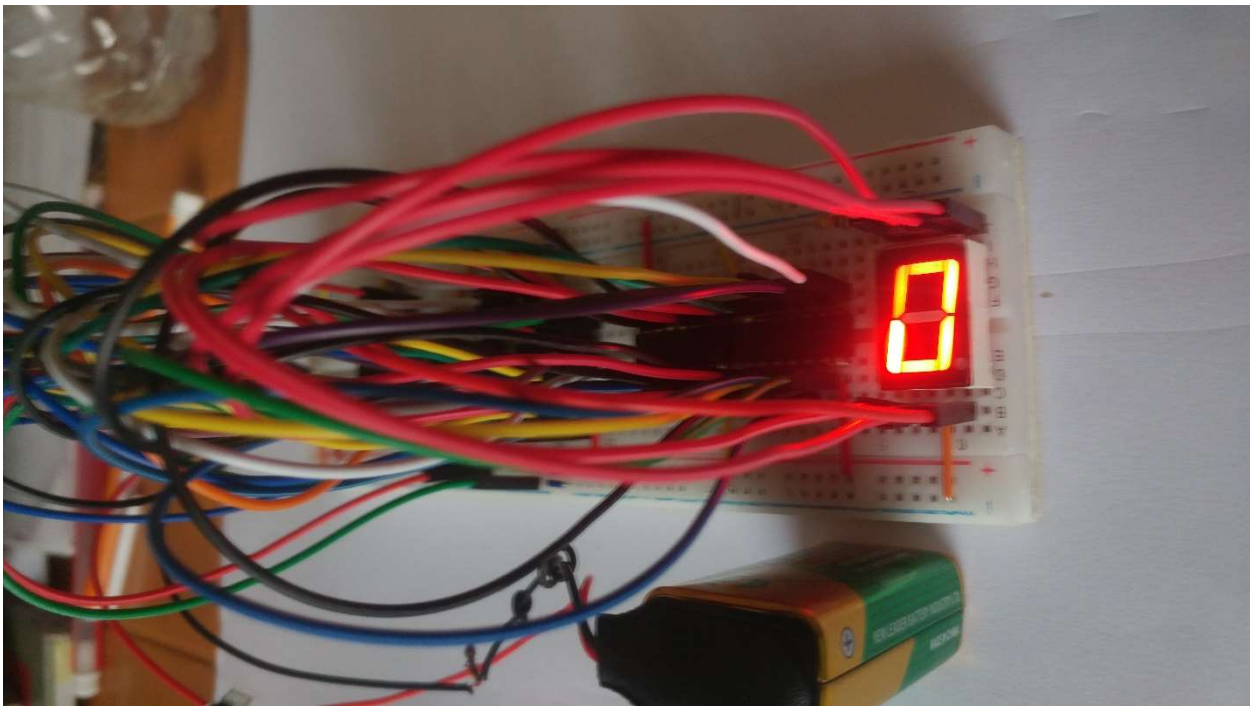


Input-: 1 0 0

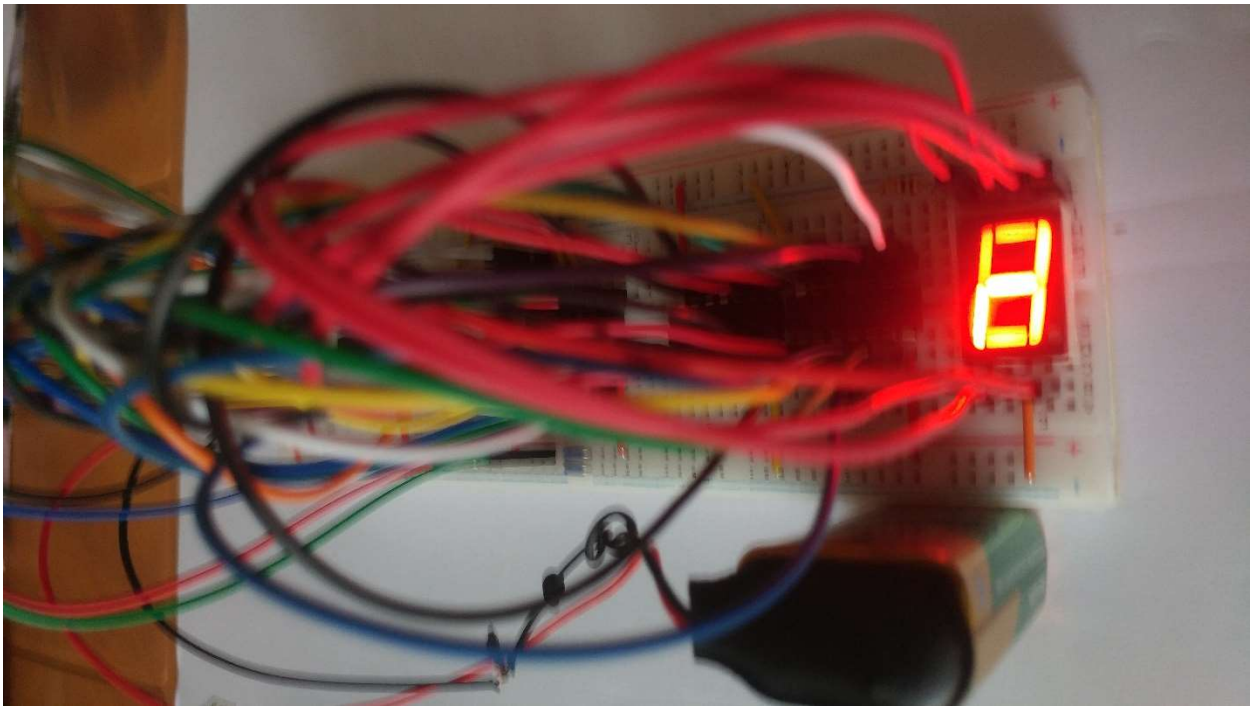


Input-: 1 0 1

“”””” Pictures of Hardware Part “”””



Input-: 1 1 0



Input-: 1 1 1