Project Report
CSE 231

Digital Logic Design
Section 11
Workstation-08

Using combinational circuit print: **SASJ-G08** in 7 segment display

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North South University
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Index	A	B	C	a	b	c	d	e	f	g	
0	0	0	0	1	0	1	1	0	1	1	S
1	0	0	1	1	1	1	0	1	1	1	A
2	0	1	0	1	0	1	1	0	1	1	S
3	0	1	1	0	1	1	1	1	0	0	J
4	1	0	0	0	0	0	0	0	0	1	-
5	1	0	1	1	0	1	1	1	1	0	G
6	1	1	0	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	1	1	1	8

Generalized functions:

$a = \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B}C + \acute{A}B\acute{C} + A\acute{B}C + AB\acute{C} + ABC$

$= \Sigma(0,1,2,5,6,7)$

$b = \acute{A}\acute{B}C + \acute{A}BC + AB\acute{C} + ABC = \Sigma(1,3,6,7)$

$c = \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B}C + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}C + AB\acute{C} +$
$ABC = \Sigma(0,1,2,3,5,6,7)$

$d = \acute{A}\acute{B}\acute{C} + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}C + AB\acute{C} + ABC$

$= \Sigma(0,2,3,5,6,7)$

$e = \acute{A}\acute{B}\acute{C} + \acute{A}BC + A\acute{B}C + AB\acute{C} + ABC$

$= \Sigma(1,3,5,6,7)$

$f = \acute{A}\acute{B}\acute{C} + \acute{A}B\acute{C} + \acute{A}BC + A\acute{B}C + AB\acute{C} + ABC$

$\sum(0,1,2,5,6,7)$

$g = \acute{A}\acute{B}\acute{C} + \acute{A}\acute{B}C + \acute{A}B\acute{C} + A\acute{B}\acute{C} + ABC$

$= \sum(0,1,2,4,7)$

K-map for a = f

	$\acute{B}\acute{C}$	$\acute{B}C$	BC	$B\acute{C}$
$\acute{A}$	1 (0)	1 (1)	0 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = \acute{A}\acute{B} + \acute{B}C + AC + AB + B\acute{C}$

K-map for b

	$\acute{B}\acute{C}$	$\acute{B}C$	BC	$B\acute{C}$
$\acute{A}$	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	0 (5)	1 (7)	1 (6)

$F = \acute{A}C + AB$

K-map for c

	$\acute{B}\acute{C}$	$\acute{B}C$	BC	$B\acute{C}$
$\acute{A}$	1 (0)	1 (1)	1 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = C + B + \acute{A}\acute{B} + \acute{A}\acute{C}$

K-map for d

	$\acute{B}\acute{C}$	$\acute{B}C$	BC	$B\acute{C}$
$\acute{A}$	1 (0)	0 (1)	1 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = B + AC + \acute{A}\acute{C}$

K-map for e

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

$F = e + AB$

K-map for g

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	1 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	1 (7)	0 (6)

$F = \bar{A}\bar{B} + B\bar{C}' + \bar{A}\bar{C}' + ABC$

Simplification for rop

i) $a = \bar{A}\bar{B} + B\bar{C} + AC + AB + B\bar{C}$

ii) $b = \bar{A}C + AB$

iii) $c = c + B + \bar{A}\bar{B} + \bar{A}\bar{C}$

iv) $d = B + AC + \bar{A}\bar{C}$

v) $e = c + AB$

vi) $f = \bar{A}\bar{B} + B\bar{C} + AC + AB + B\bar{C}$

vii) $g = \bar{A}\bar{B} + B\bar{C}' + \bar{A}\bar{C}' + ABC$

Generalized POS Function :

$a = AB'C' + A'BC = (A'+B+C)(A+B'+C') = \Pi(3,4)$

$b = A'B'C' + A'BC' + AB'C' + AB'C = (A+B+C)(A+B'+C)$
$(A'+B+C)(A'+B+C')$
$= \Pi(0,2,4,5)$

$c = AB'C' = A'+B+C = \Pi(4)$

$d = A'B'C + AB'C' = (A+B+C')(A'+B+C) = \Pi(1,4)$

$e = A'B'C' + A'BC' + AB'C' = (A+B+C)(A+B'+C)$
$(A'+B+C) = \Pi(0,2,4)$

$f = AB'C' + A'BC = (A'+B+C)(A+B'+C') = \Pi(3,4)$

$g = A'BC + AB'C + ABC' = (A+B'+C')(A'+B+C')$
$(A'+B'+C) = \Pi(3,5,6)$

k-map for a=f

	B'C'	B'C	BC	BC'
A'	1 (0)	1 (1)	0 (3)	1 (2)
A	0 (4)	1 (5)	1 (7)	1 (6)

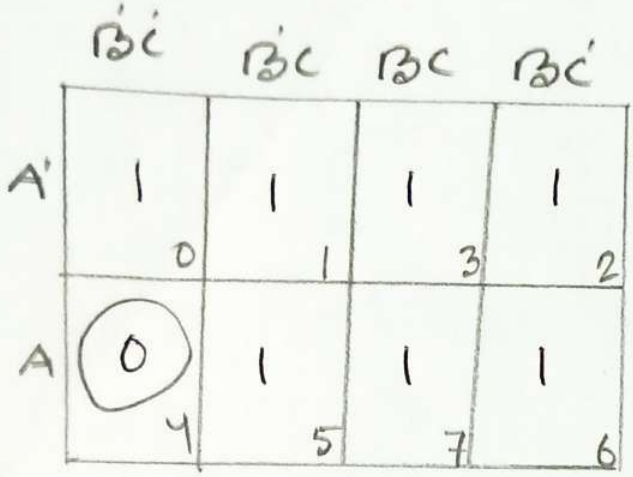
$F = (A+B'+C')(A'+B+C)$

k-map for b

	B'C'	B'C	BC	BC'
A'	0 (0)	1 (1)	1 (3)	0 (2)
A	0 (4)	0 (5)	1 (7)	1 (6)

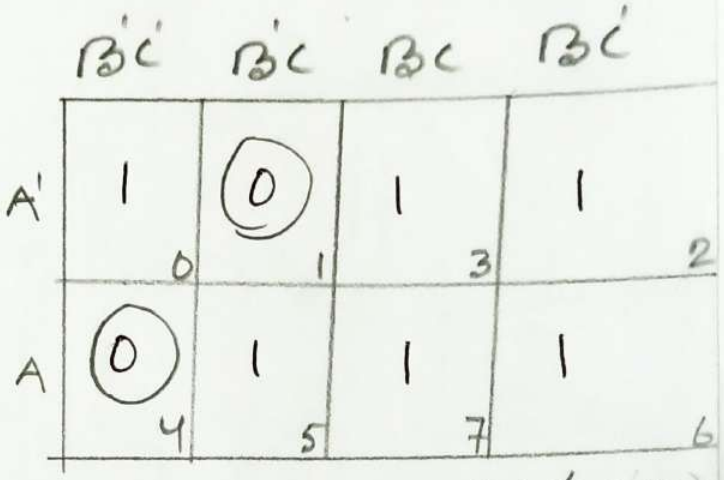
$F = (A+C)(B+C)(A'+B)$

K-map for c



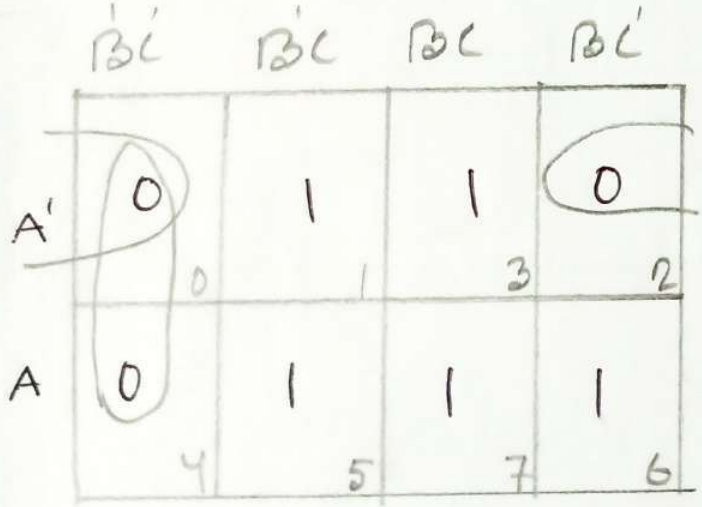
$F = A' + B + C$

K-map for d



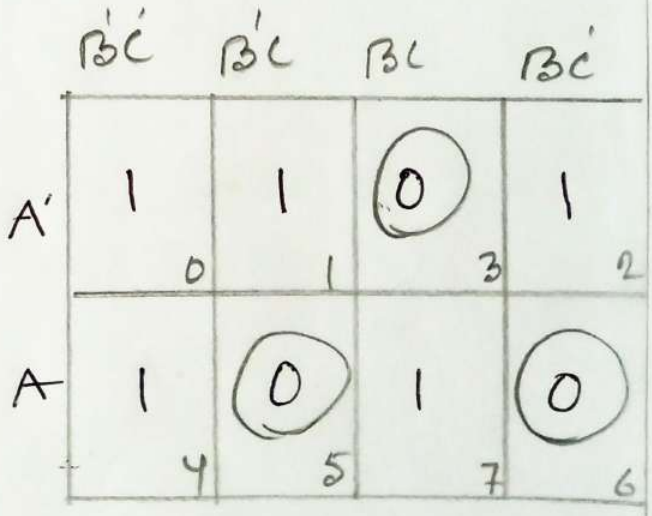
$F = (A + B + C')(A' + B + C)$

K-map for e



$F = (A + C)(B + C)$

K-map for g



$F = (A + B' + C')(A' + B + C)(A' + B' + C)$

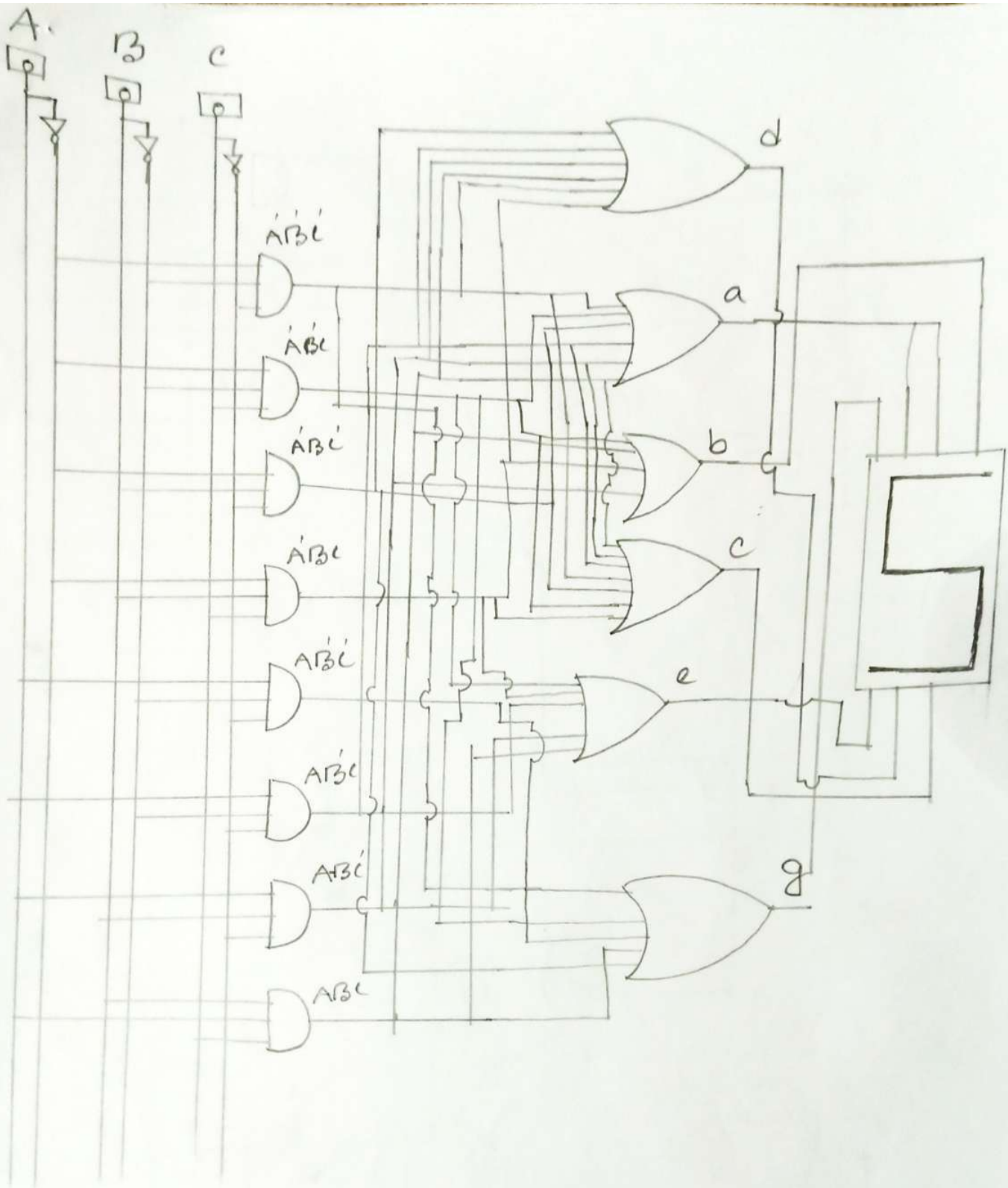


Fig: Generalized SOP Circuit Diagram Using Basic gates.

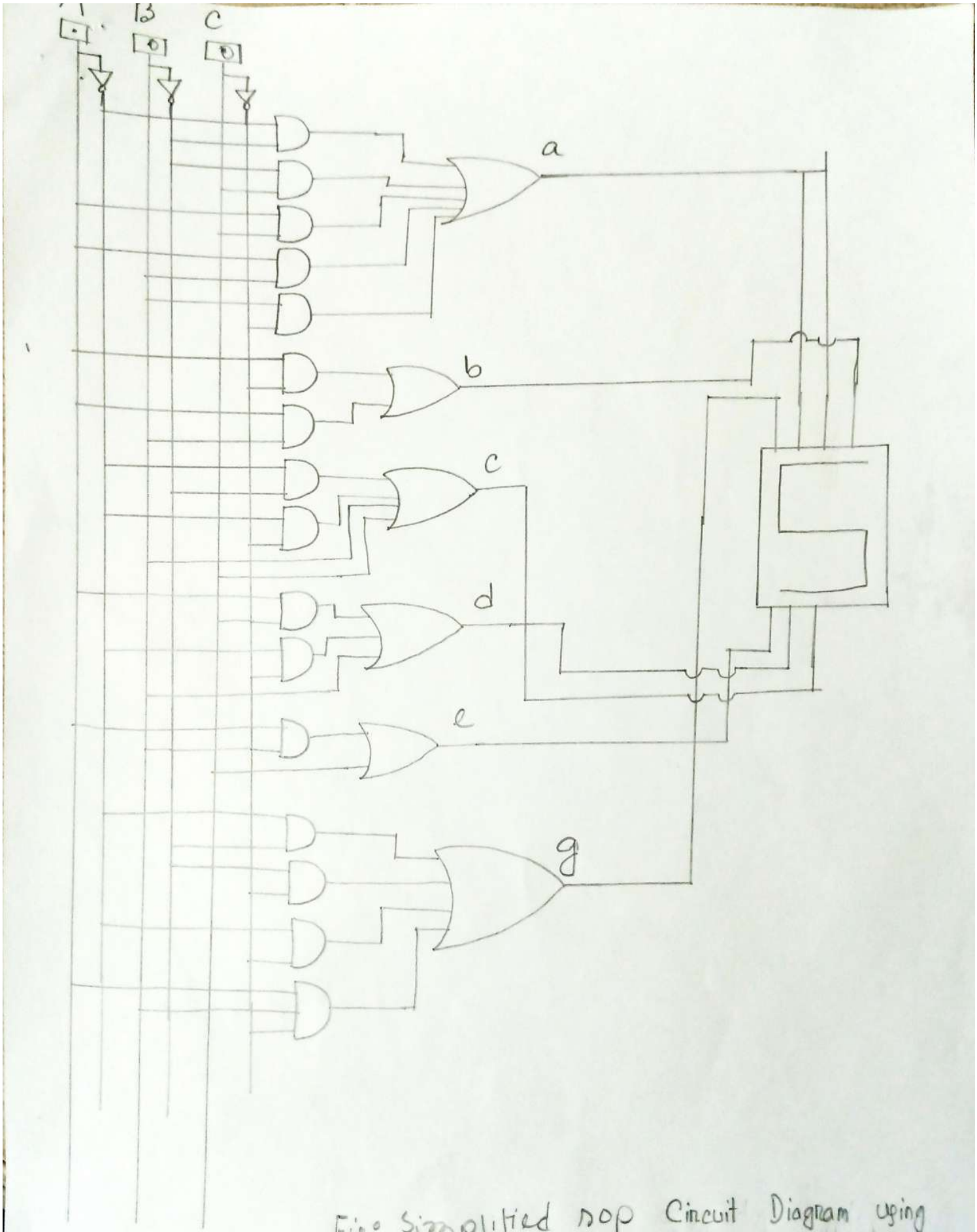


Fig: Simplified POP Circuit Diagram using basic gates.

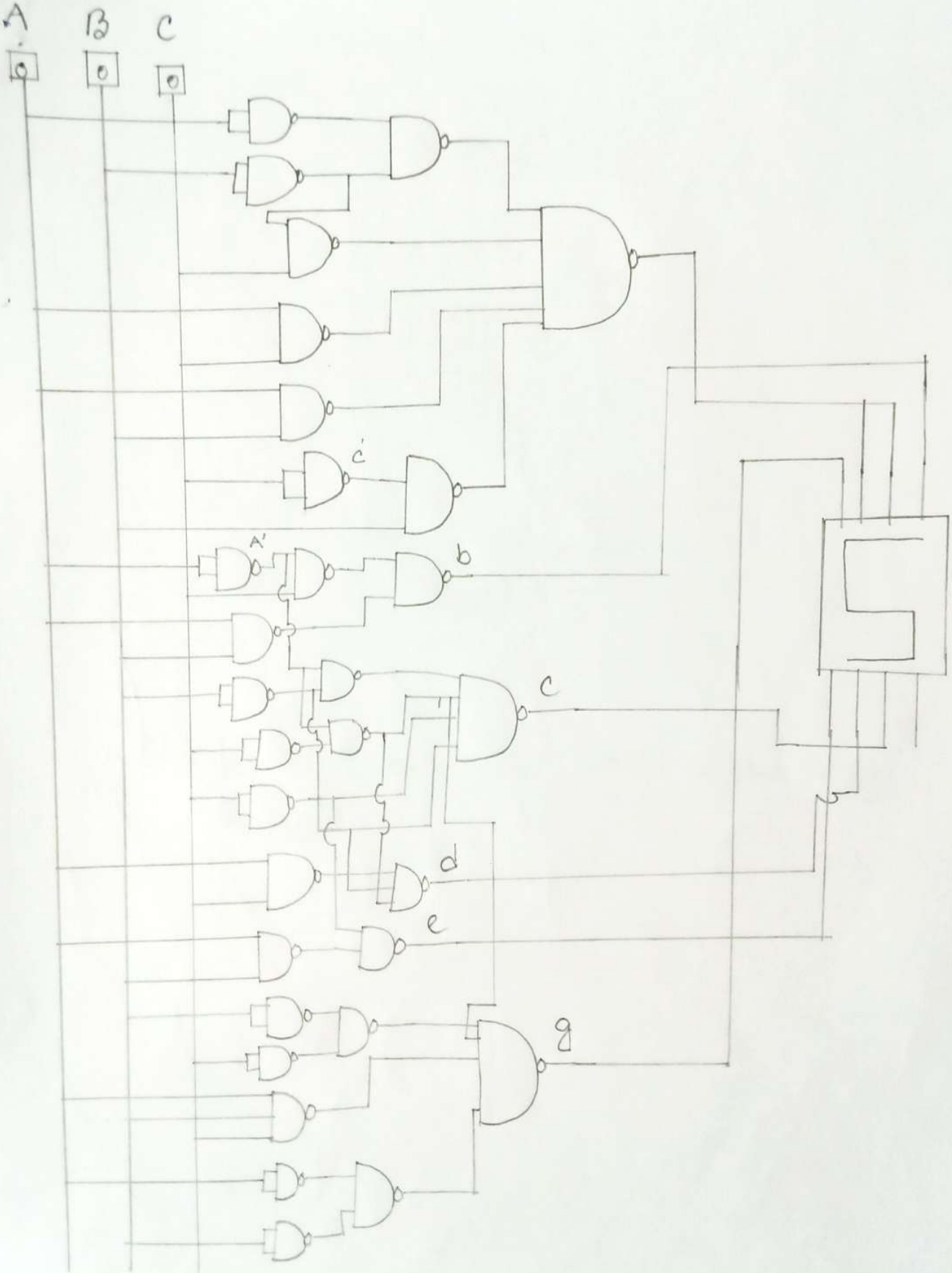


Fig: Simplified SOP Circuit Diagram using NAND gates.

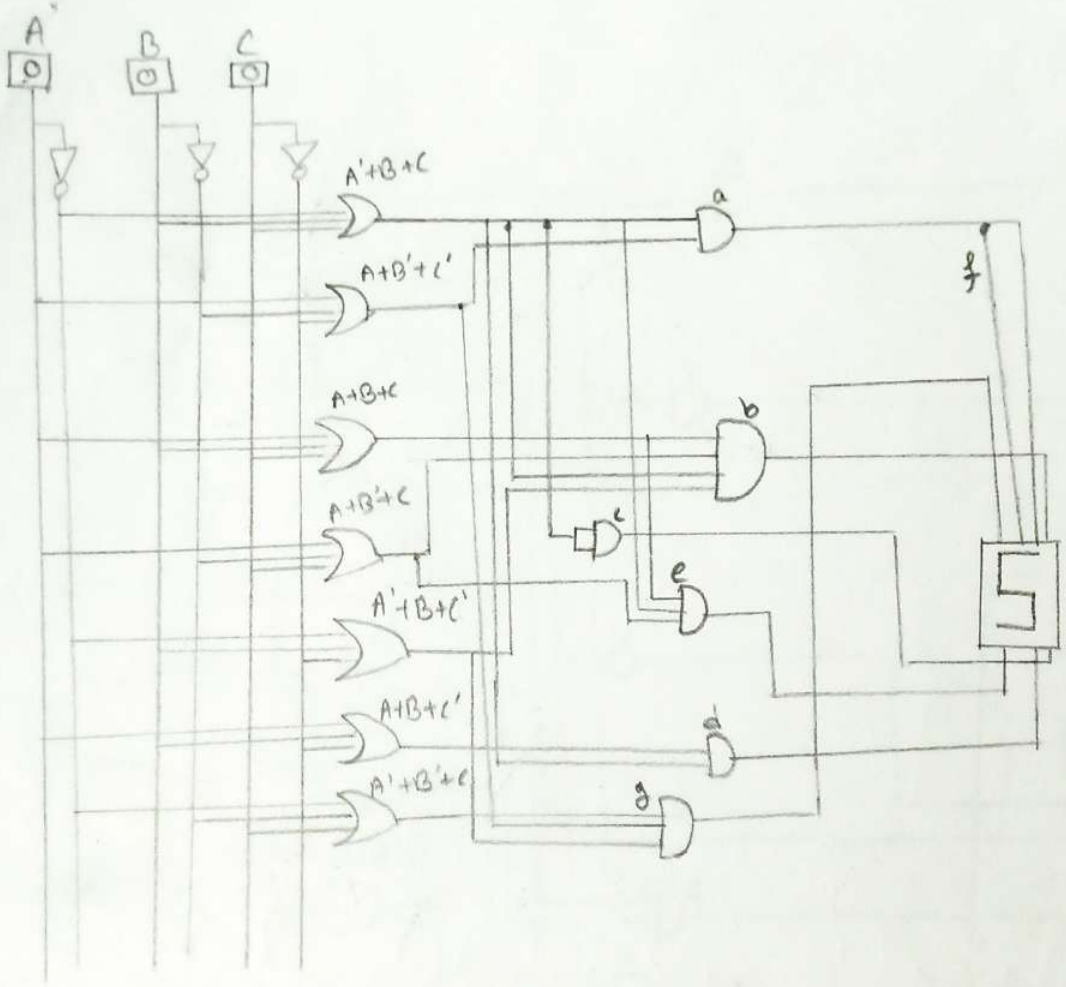


Fig: Generalized POS circuit diagram using basic gates.

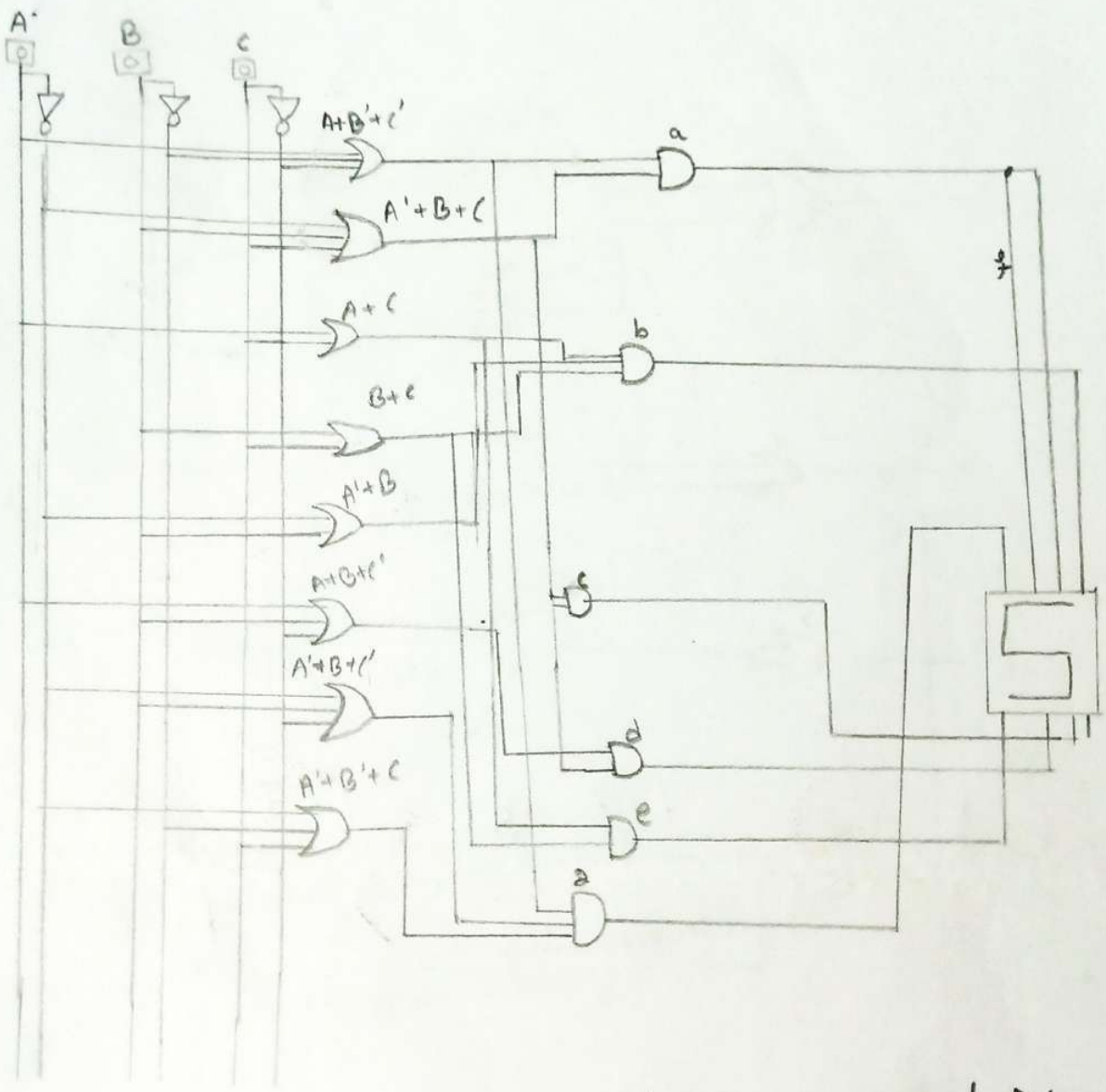
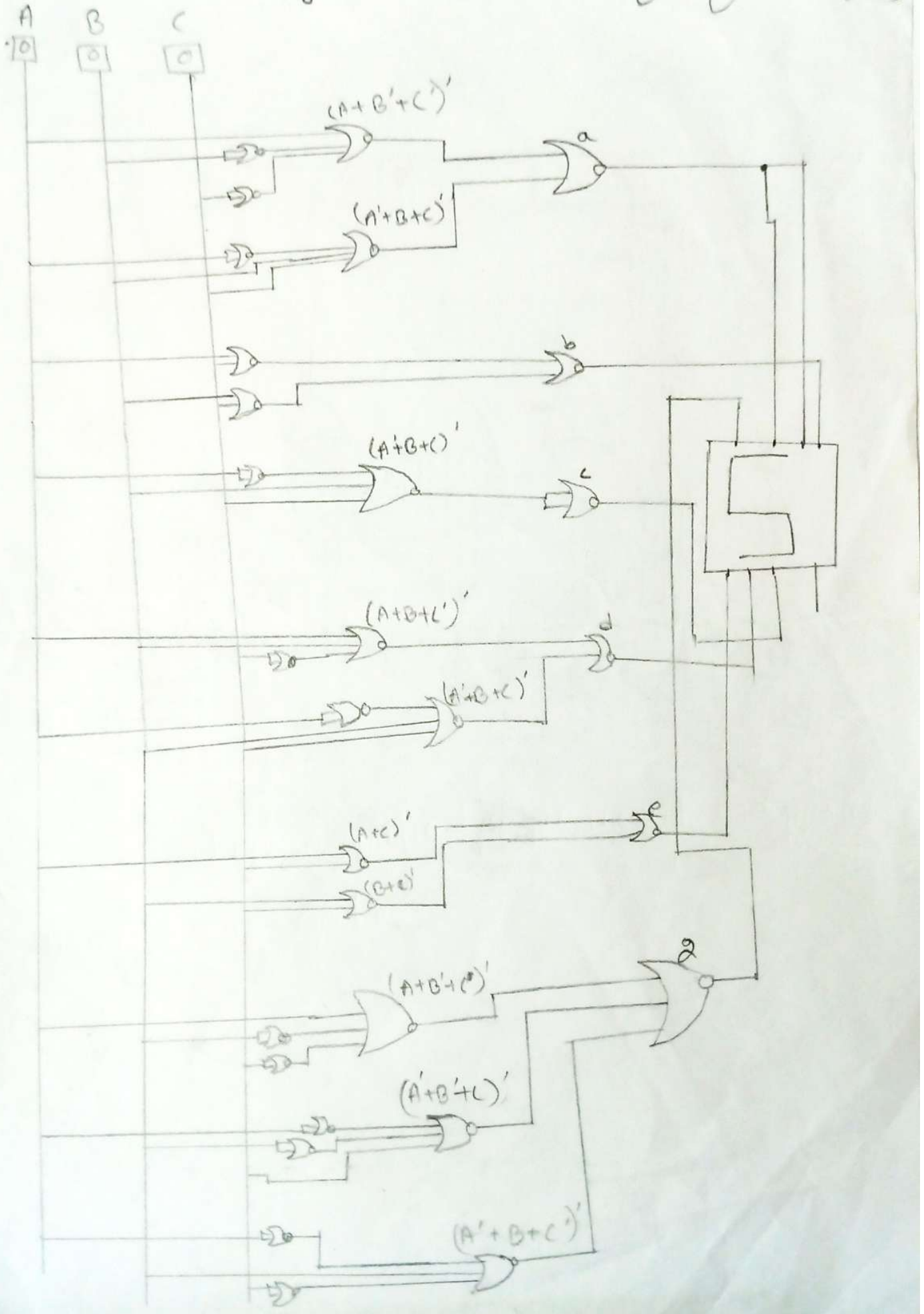


Fig: Simplified pos circuit Diagram using basic gates

Fig: Simplified POS using only NOR gates



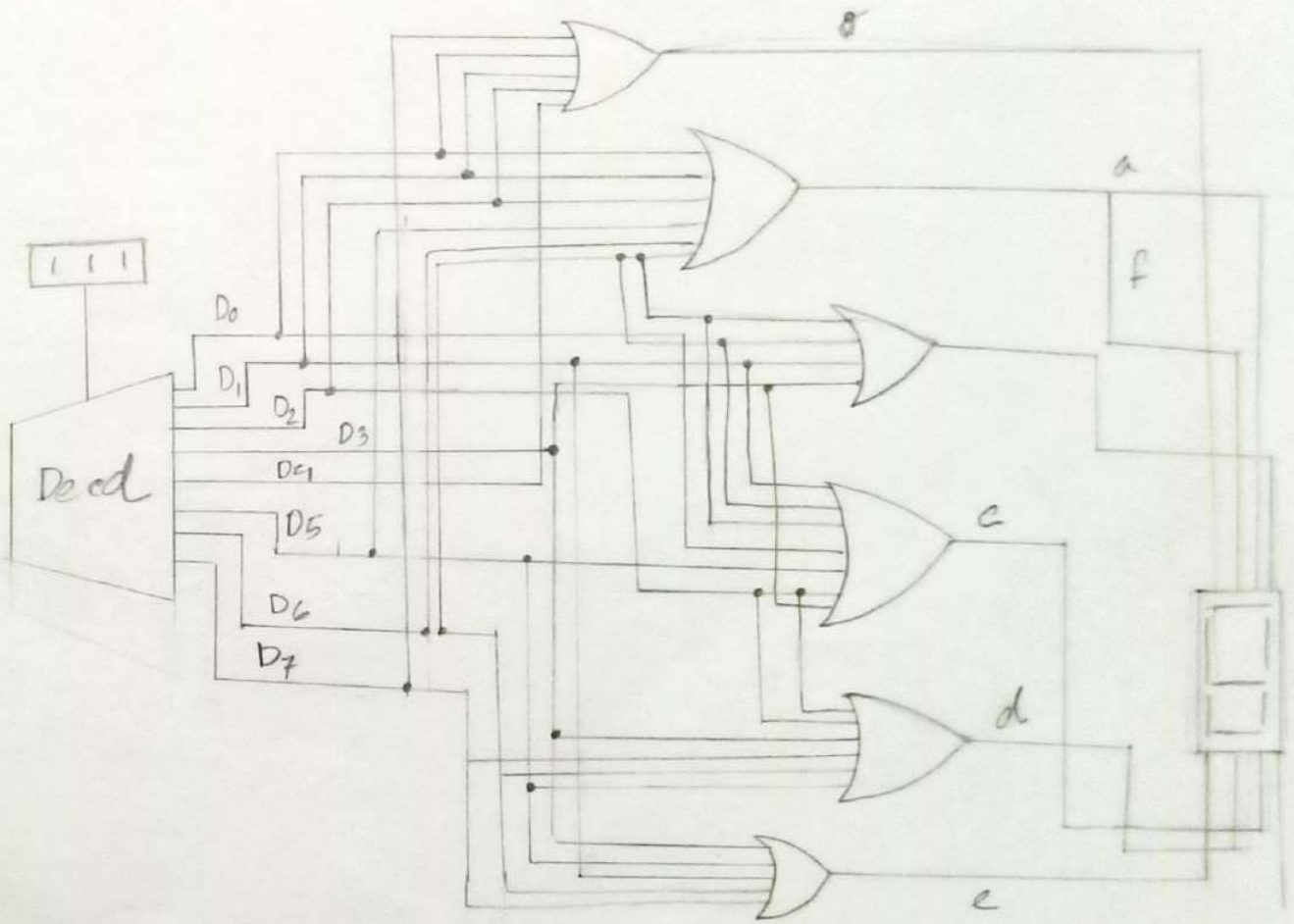


Fig: Generalized SOP Circuit Diagram using Decoder and OR gate.

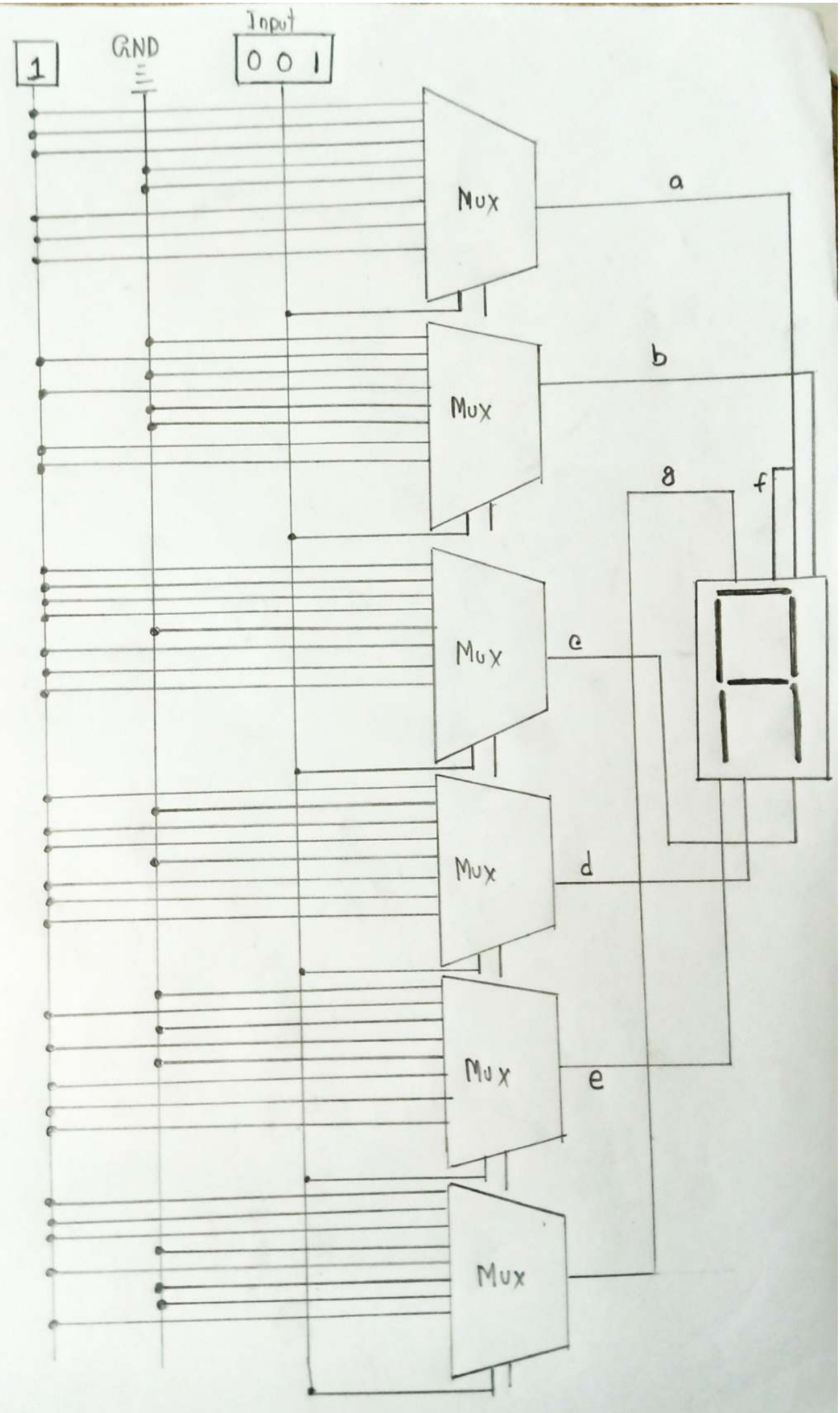


Fig: Generalized SOP Multiplexer

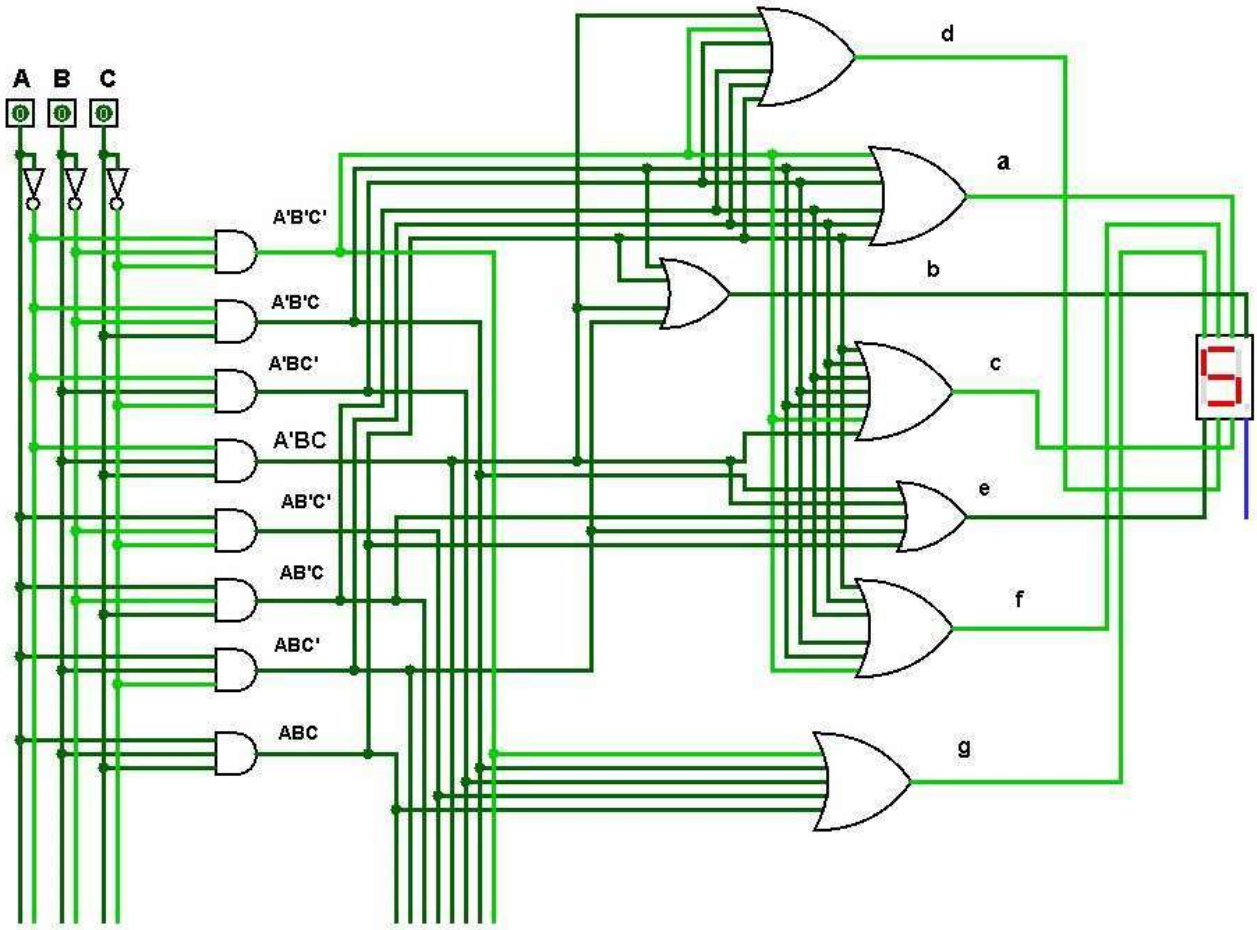


Fig. Circuit Diagram For Generalized SOP Equation

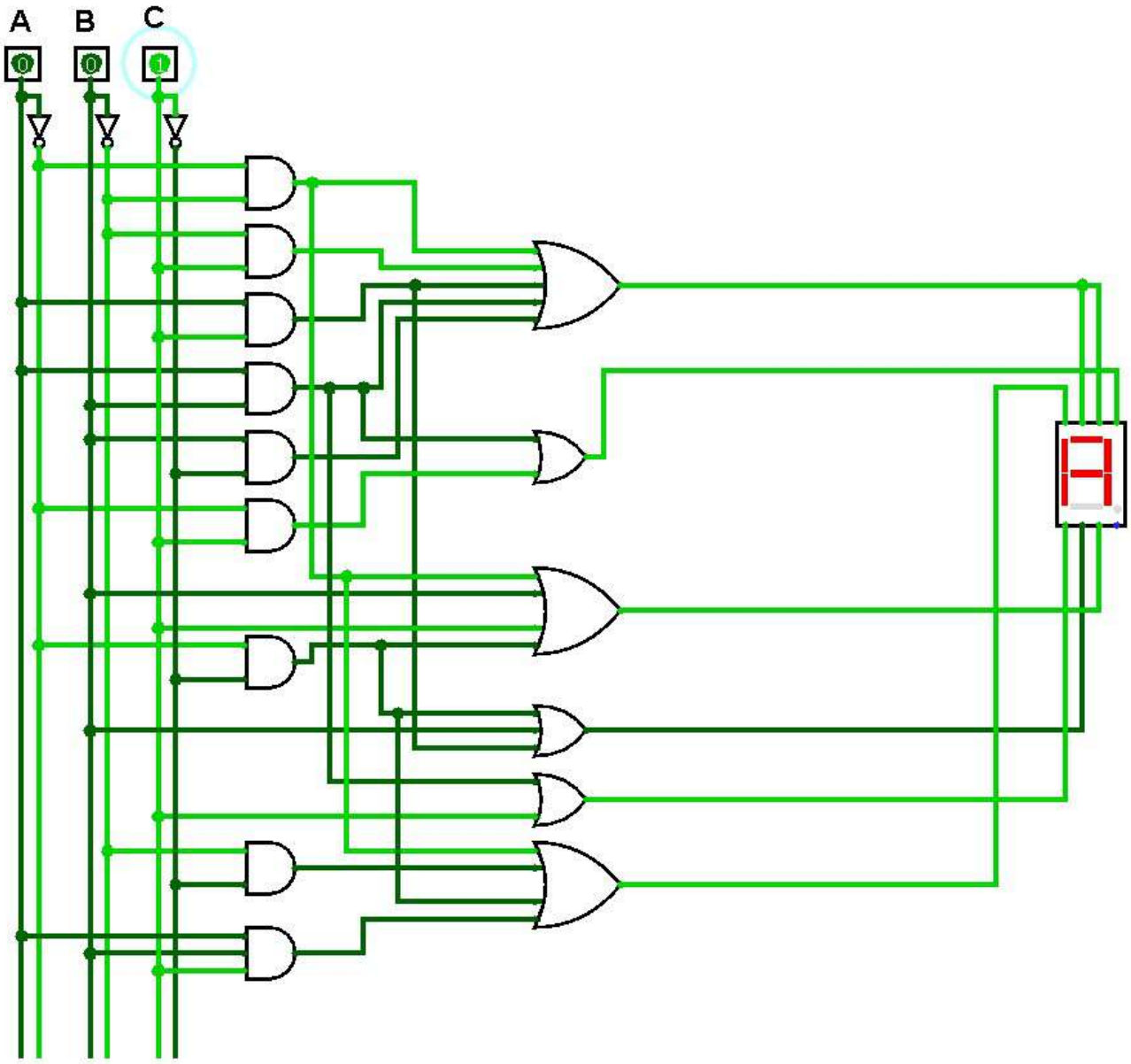


Fig. Project-Simplifeid SOP Circuit Diagram using basic gates

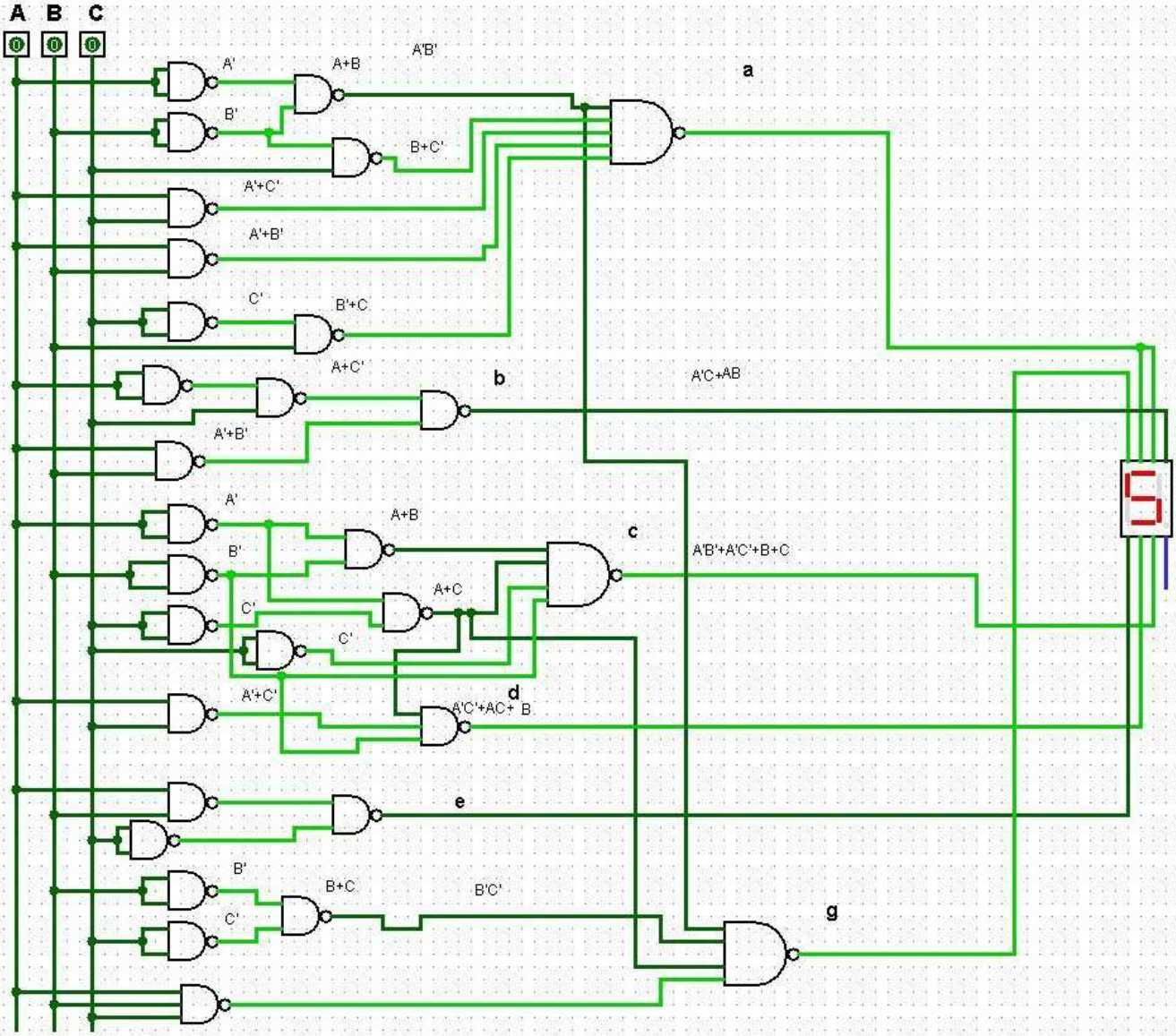


Fig. Circuit Diagram of SOP using only NAND Gates

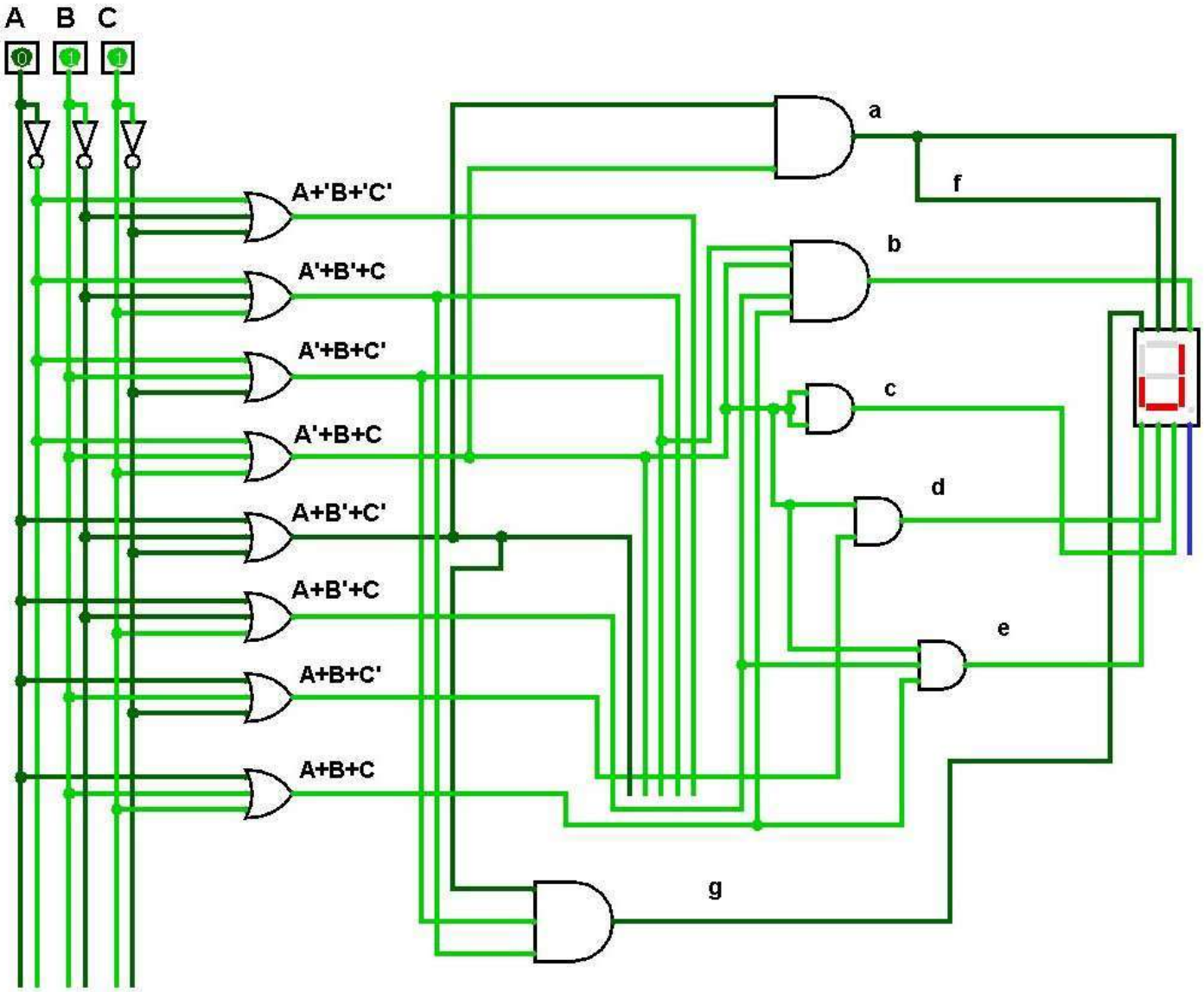


Fig. Circuit Diagram of Generalized POS

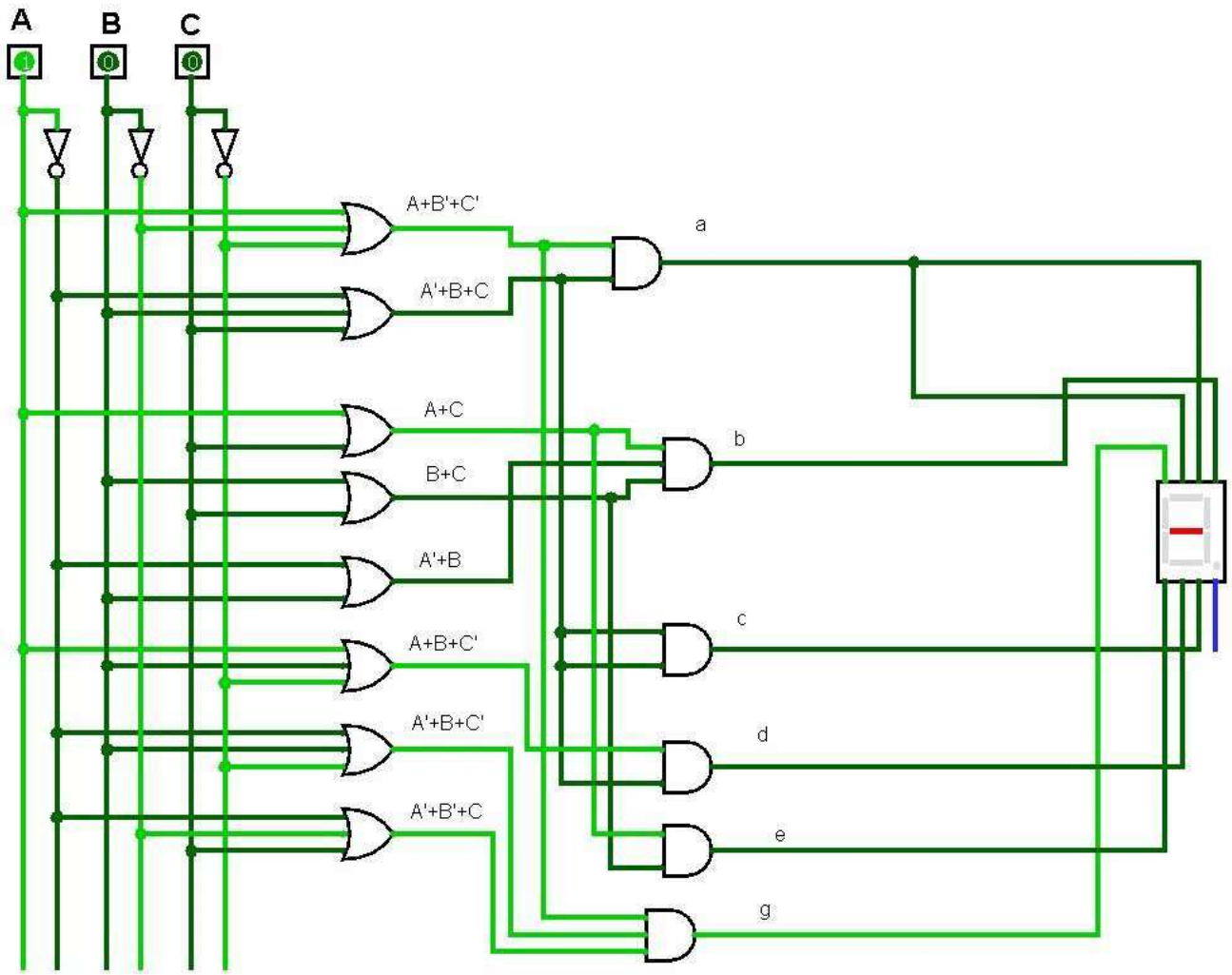


Fig.Circuit Diagram for Simplified POS Using Basic Gates

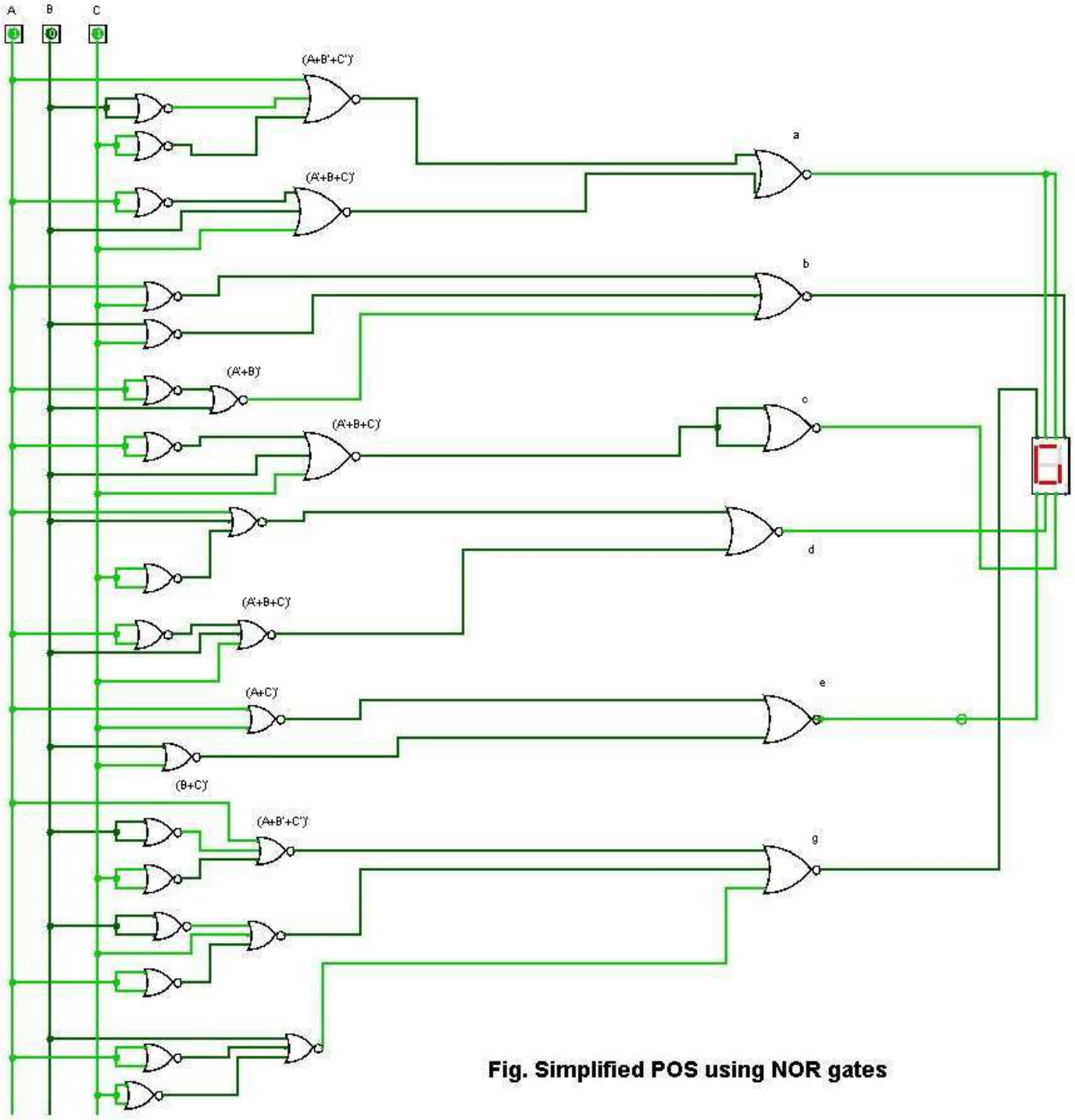


Fig. Simplified POS using NOR gates

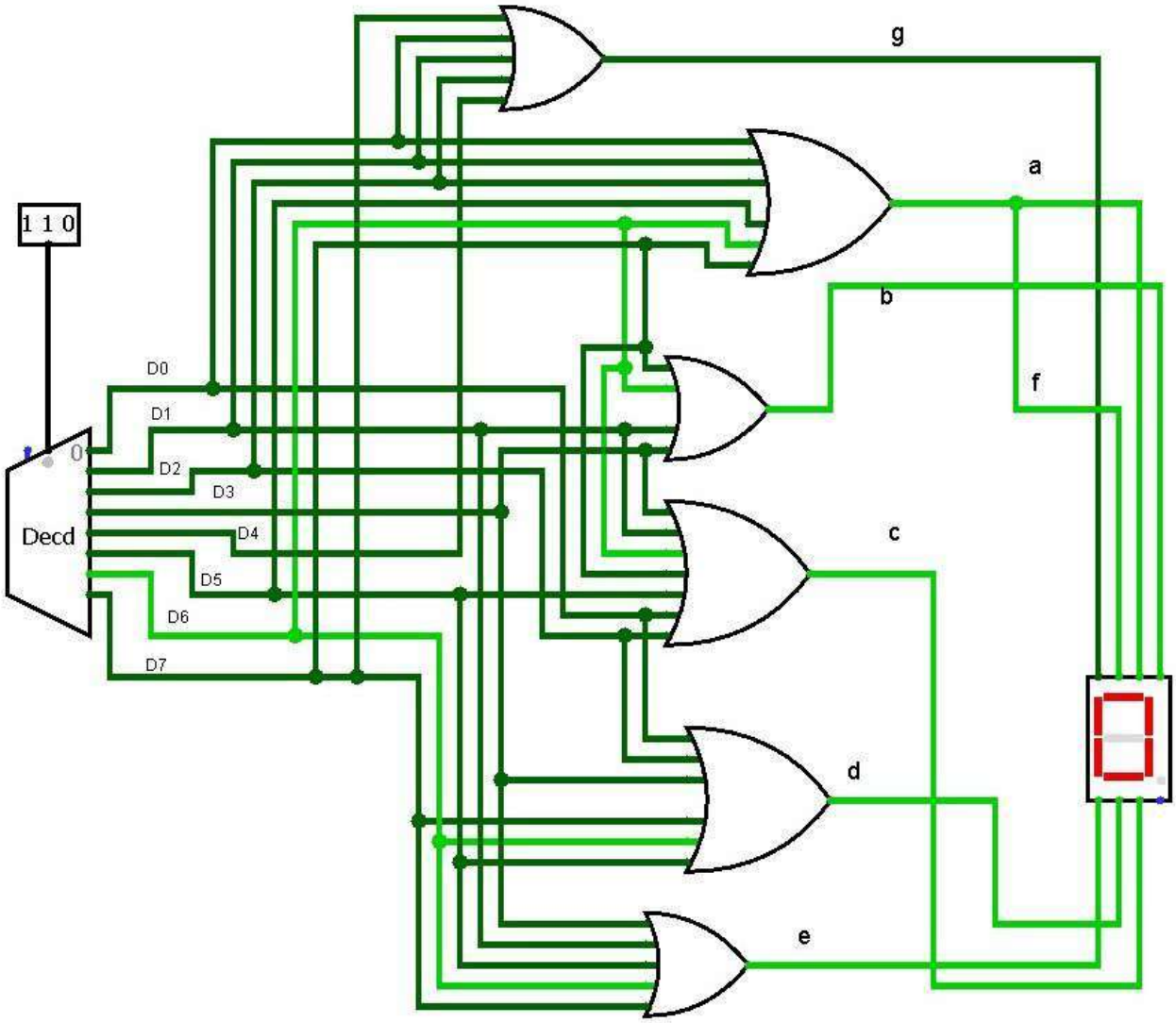


Fig. Generalized SOP Using Decoder and OR Gates

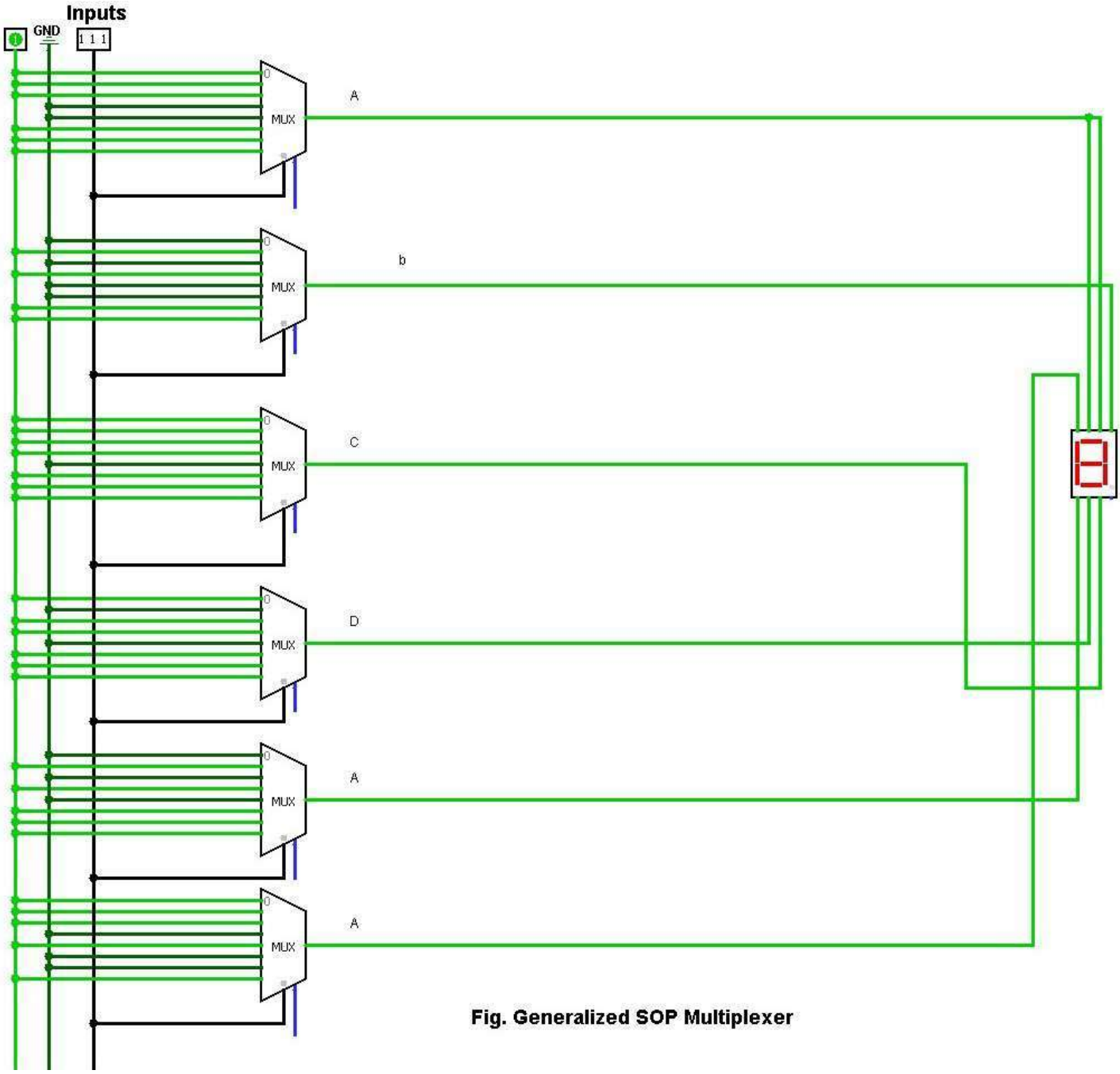
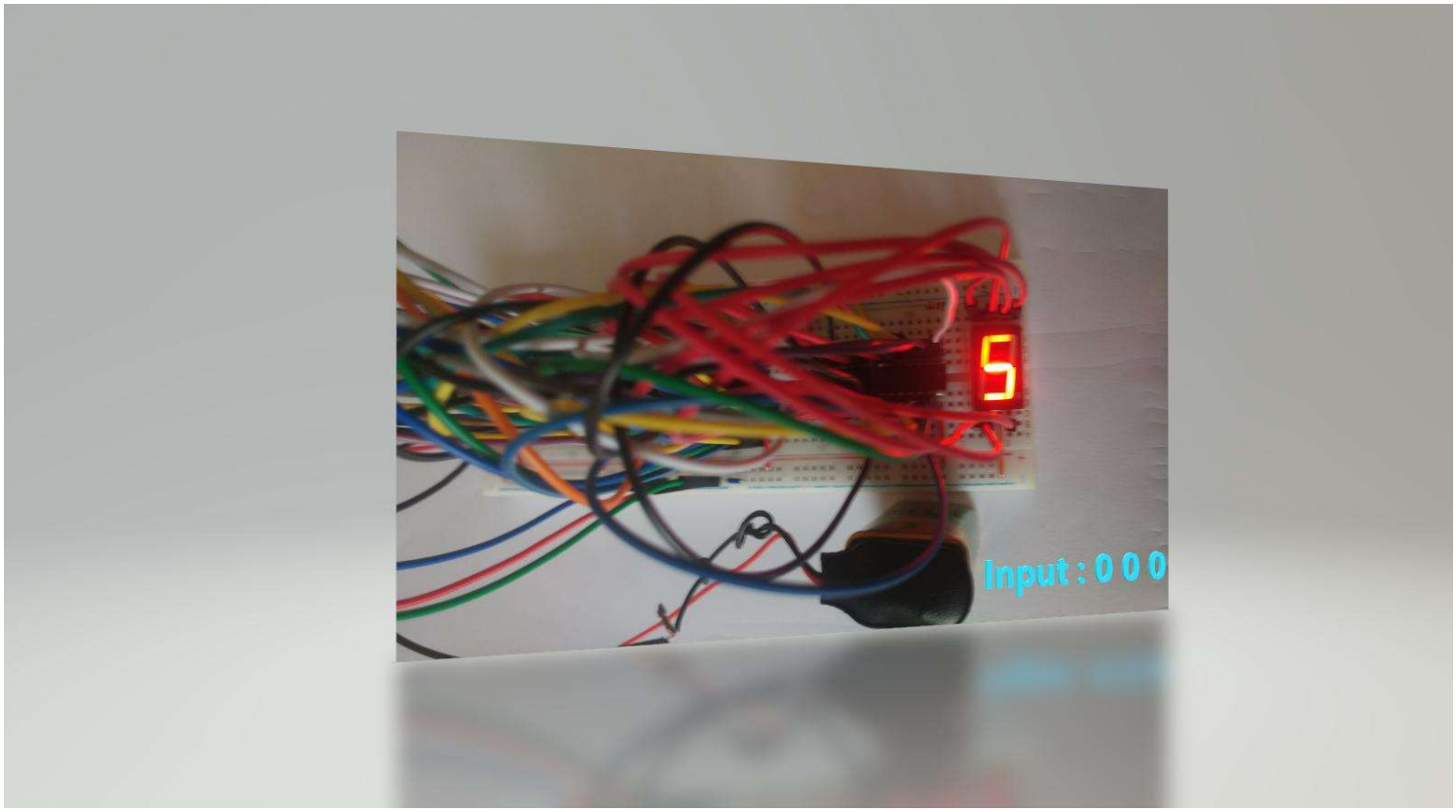


Fig. Generalized SOP Multiplexer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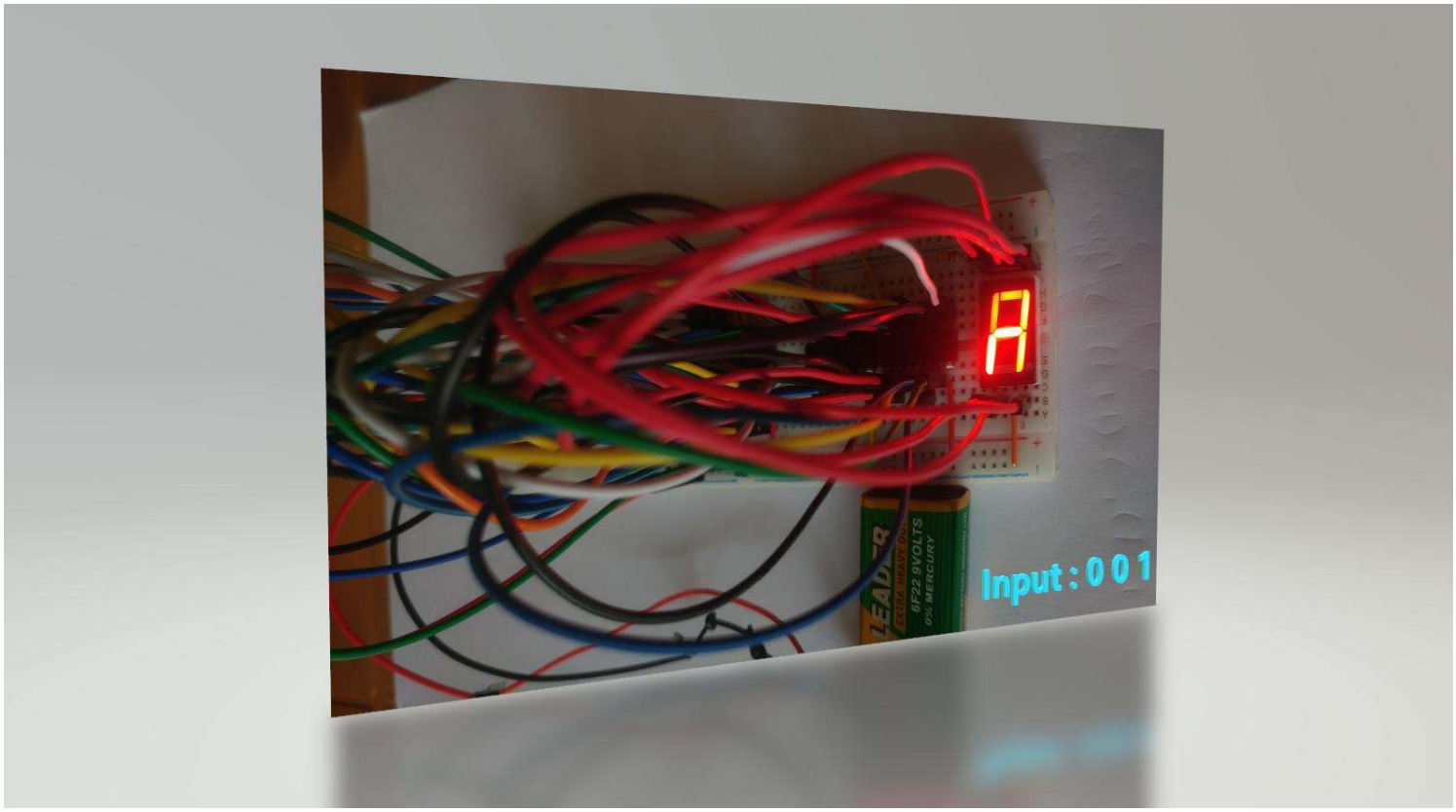
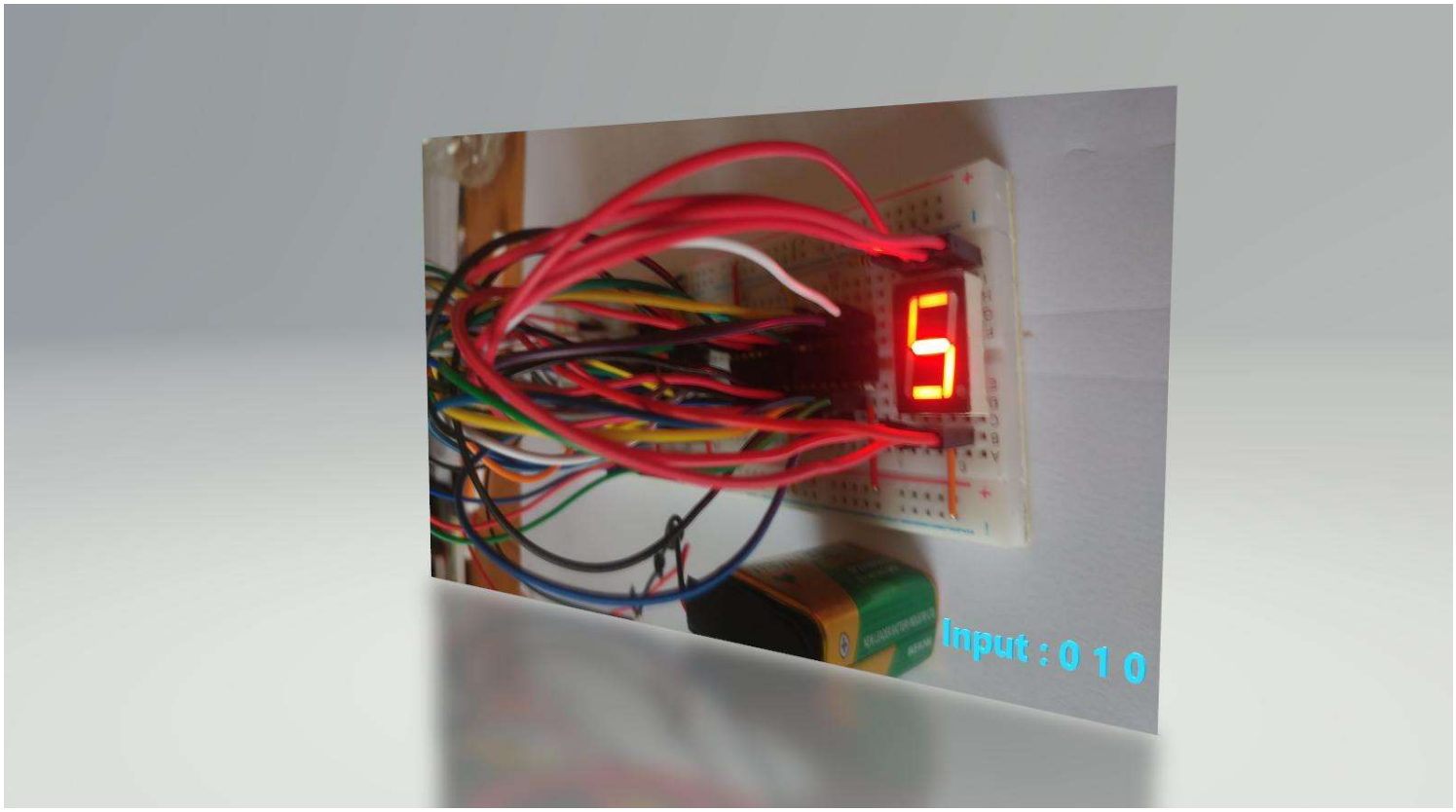
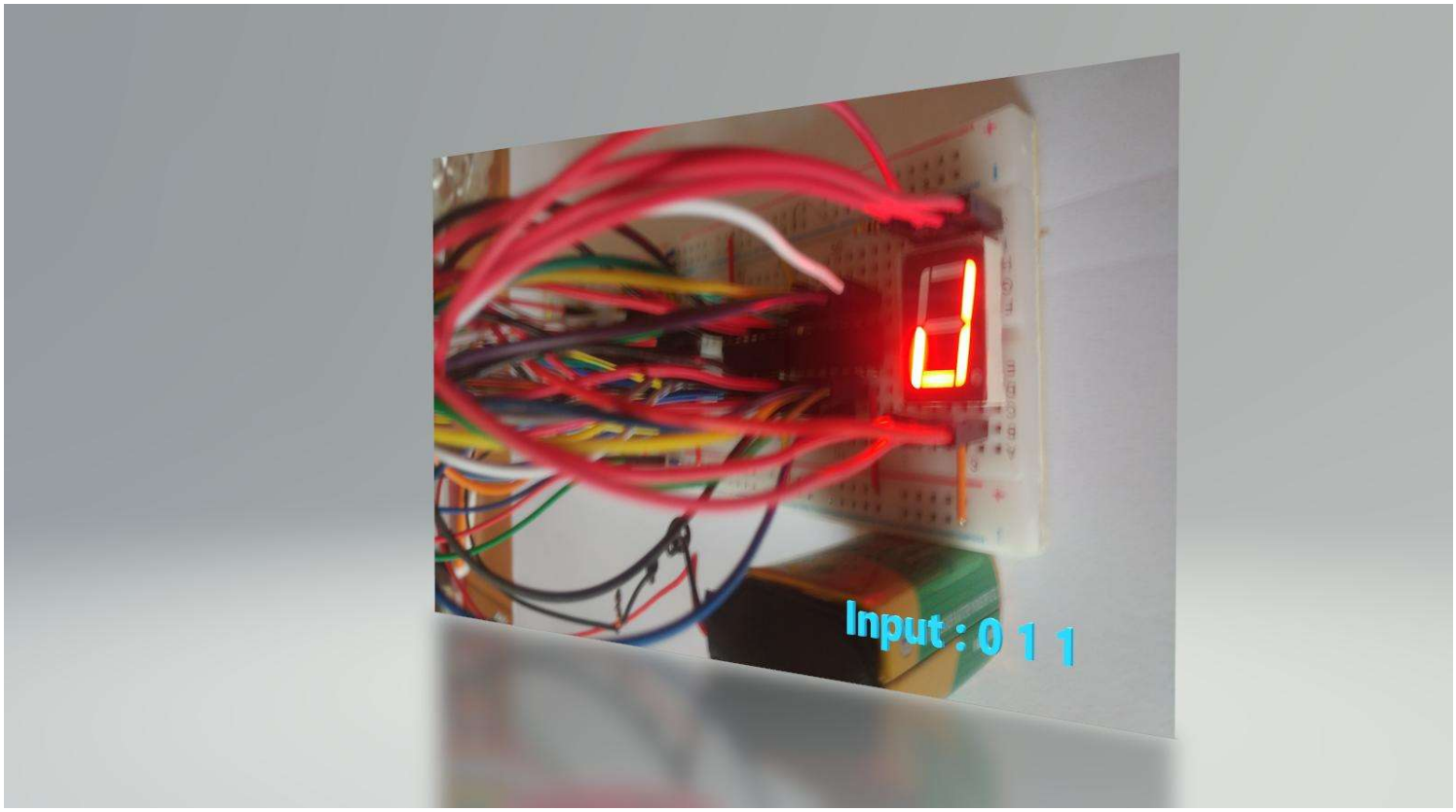
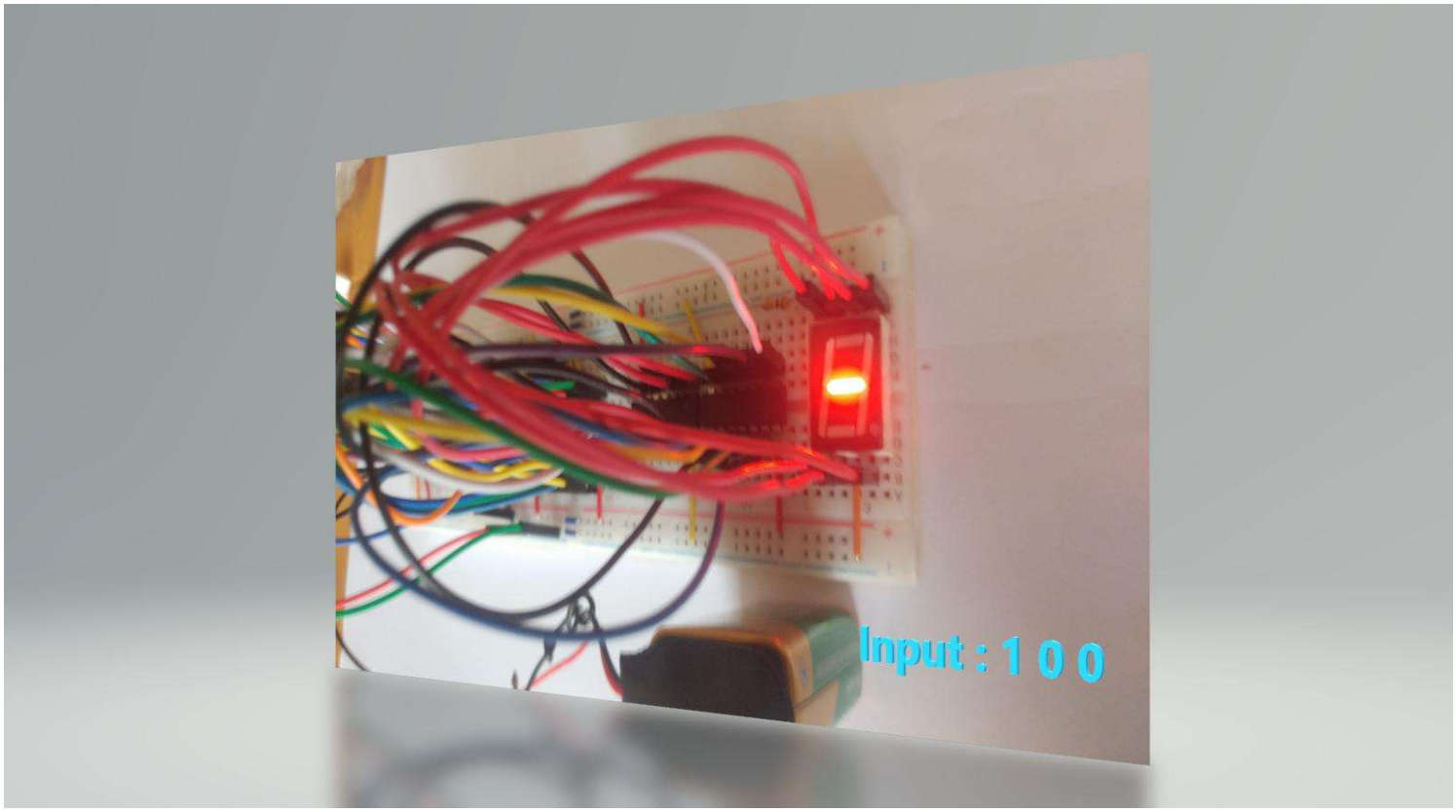

A
Input : 0 0 1
6F22 9VOLTS
0% MERCURY


5
Input : 0 1 0


Input : 0 1 1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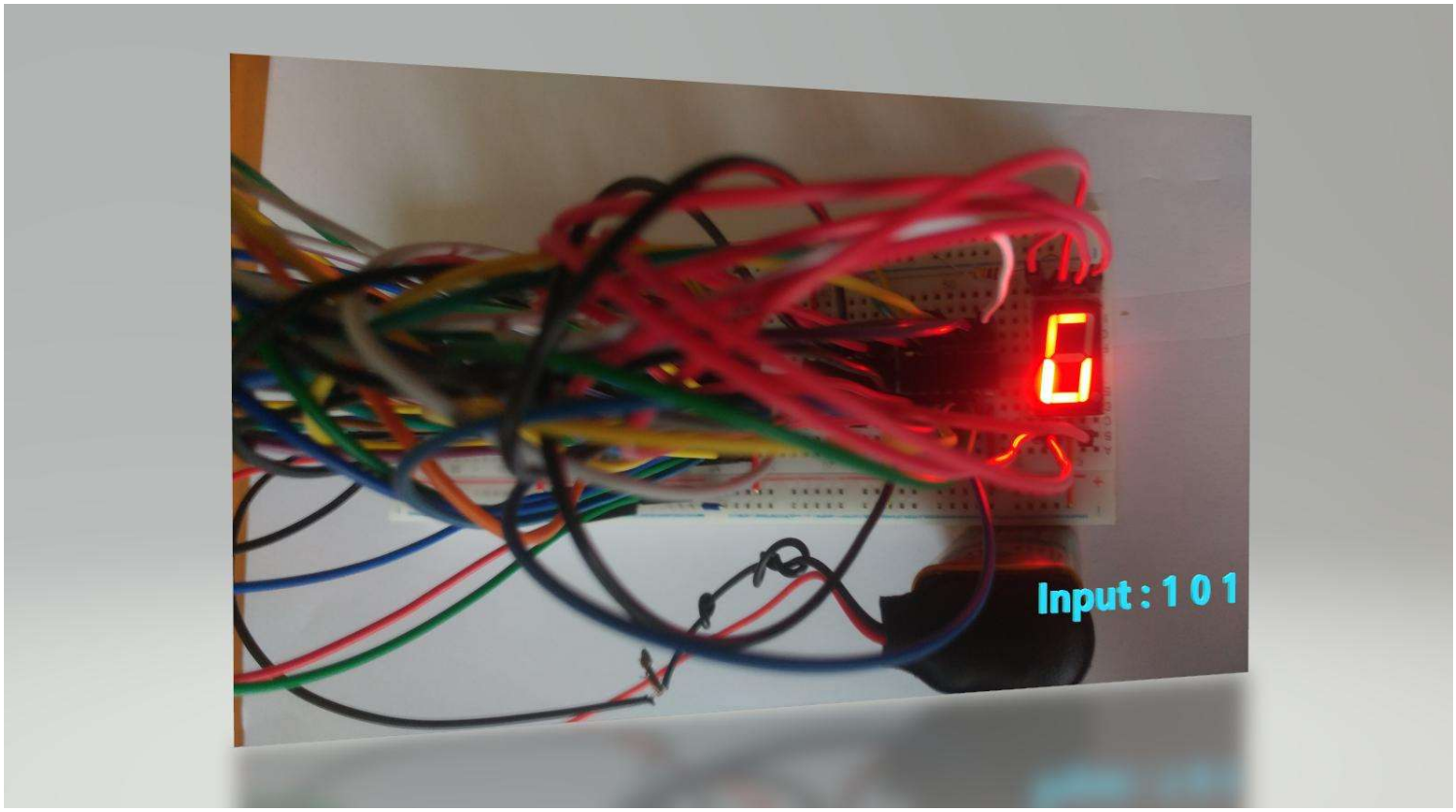
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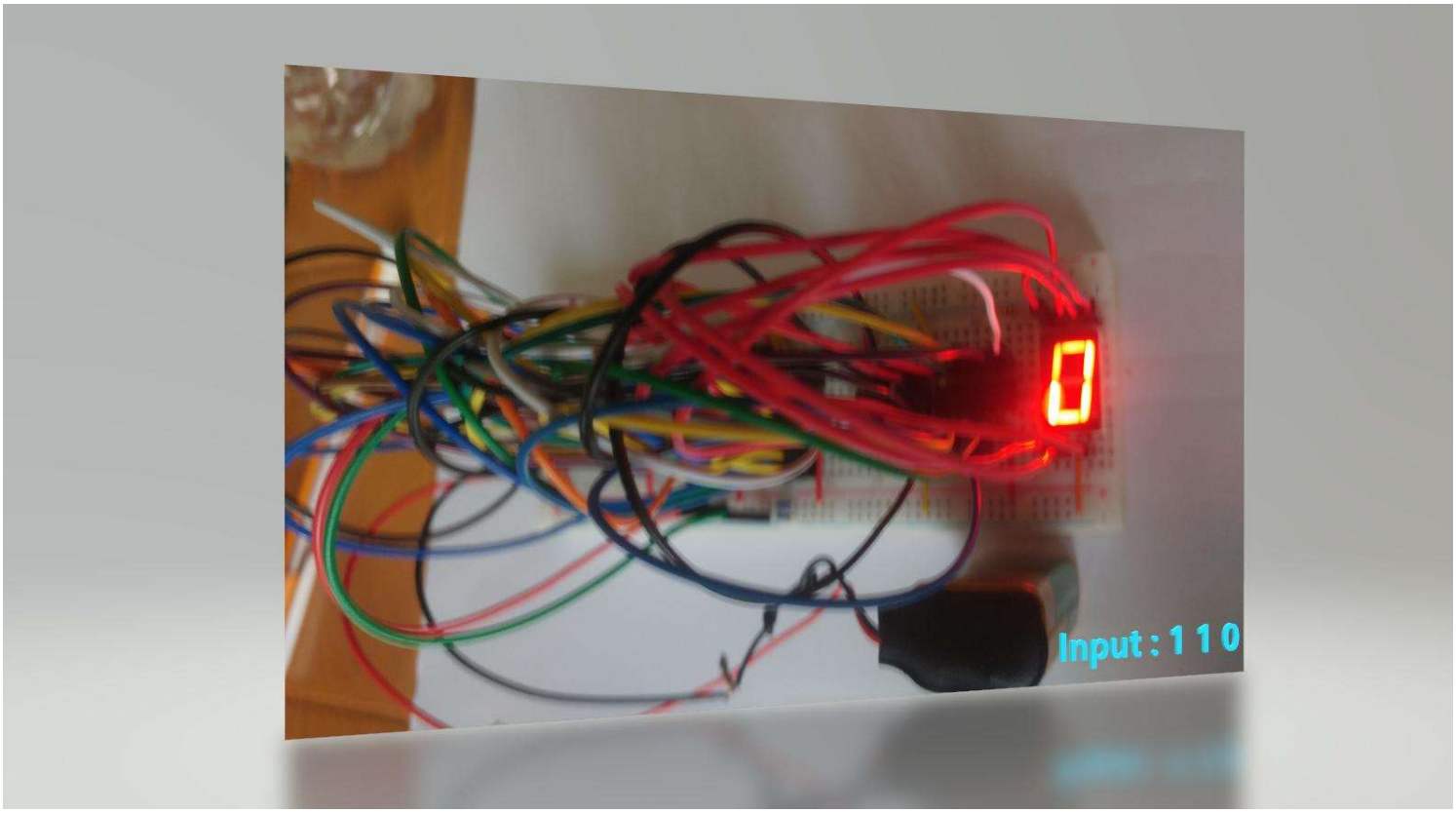
Input : 1 0 1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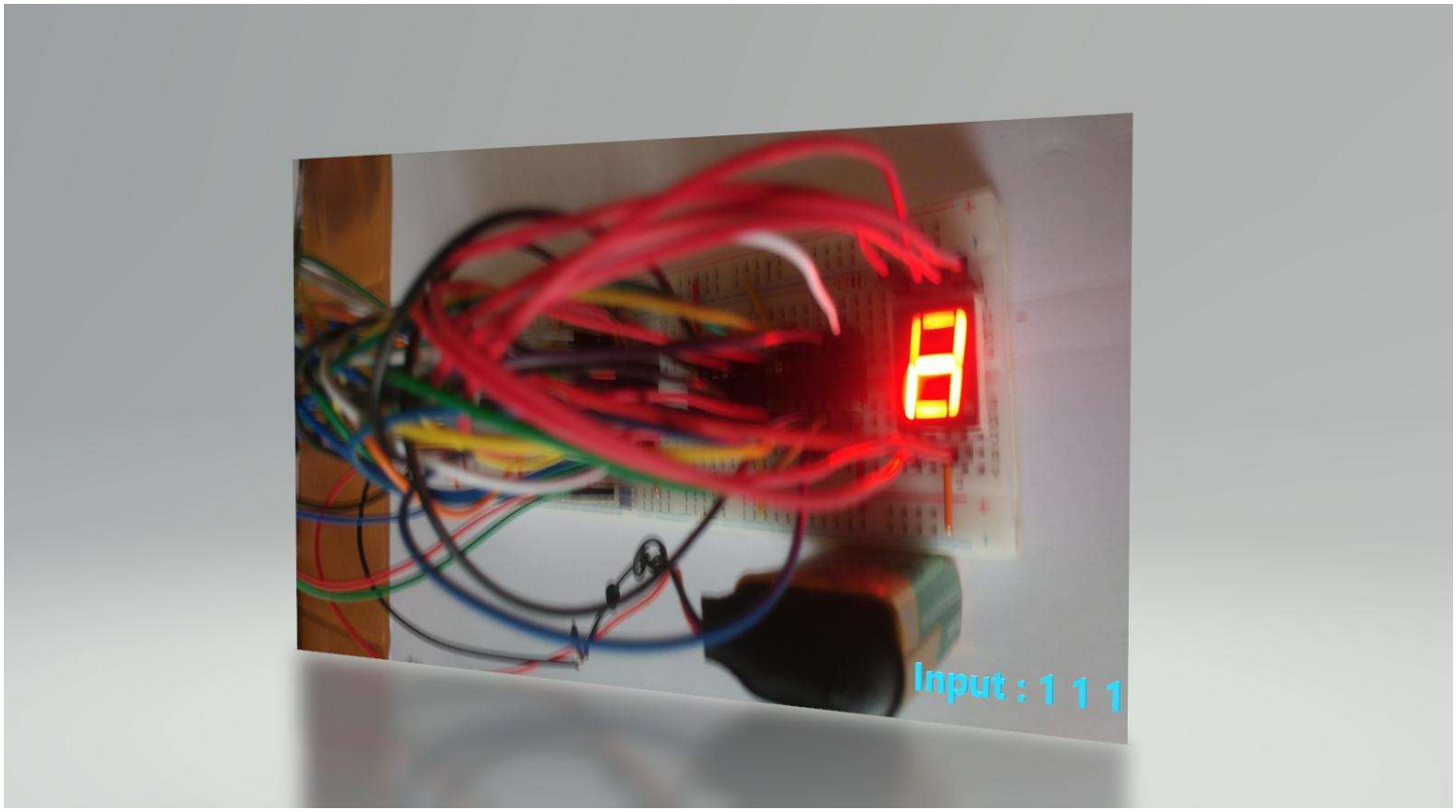
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