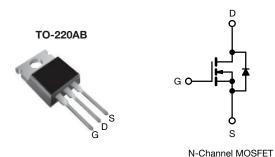
Vishay Siliconix

COMPLIANT

HALOGEN

FREE

E Series Power MOSFET



PRODUCT SUMMARY				
V_{DS} (V) at T_J max.	650			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V	0.137		
Q _g max. (nC)	36			
Q _{gs} (nC)	10			
Q _{gd} (nC)	6			
Configuration	Single			

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP150N60E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)							
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-source voltage			V_{DS}	600	V		
Gate-source voltage			V_{GS}	± 30	V		
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 100 ^{\circ}\text{C}$	- I _D	22			
	VGS at 10 V	T _C = 100 °C		14	Α		
Pulsed drain current ^a			I _{DM}	43			
Linear derating factor				1.42	W/°C		
Single pulse avalanche energy b			E _{AS}	111	mJ		
Maximum power dissipation			P_{D}	179	W		
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C		
Drain-source voltage slope	e slope $T_J = 125 ^{\circ}\text{C}$		-1/-14	100	1//20		
Reverse diode dv/dt ^d			dv/dt	5	- V/ns		
Soldering recommendations (peak temperature	e) ^c	For 10 s		260	°C		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 2.8 A
- c. 1.6 mm from case
- d. $I_{SD} \le I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R_{thJA}	=	62	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	-	0.7	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		-					
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA		-	0.62	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		-	5.0	V
Onto anima lankana		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-source leakage	I_{GSS}	,	V _{GS} = ± 30 V		-	± 1	μA
7		V _{DS} =	V _{DS} = 600 V, V _{GS} = 0 V		-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μΑ
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.137	0.158	Ω
Forward transconductance	9 _{fs}	V _{DS} = 10 V, I _D = 10 A		-	5.1	-	S
Dynamic		-					
Input capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ f = 100 KHz		-	1514	-	pF
Output capacitance	C _{oss}			-	60	-	
Reverse transfer capacitance	C _{rss}			-	2	-	
Effective output capacitance, energy related	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	58	-	
Effective output capacitance, time related	C _{o(tr)}			-	322	-	
Total gate charge	Qg			-	24	36	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 10 \text{ A}, V_{DS} = 480 \text{ V}$		10	-	nC
Gate-drain charge	Q _{gd}	1			6	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 10 A,		-	20	40	- ns
Rise time	t _r			-	27	54	
Turn-off delay time	t _{d(off)}	V _{GS} =	$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$		28	56	
Fall time	t _f	1		-	17	34	
Gate input resistance	R_g	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	22	
Pulsed diode forward current	I _{SM}			-	-	43	A
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 10 \text{A},$ $di/dt = 100 \text{A/}\mu\text{s}, V_R = 25 \text{V}$		-	291	582	ns
Reverse recovery charge	Q _{rr}			-	3.5	7.0	μC
Reverse recovery current	I _{RRM}			_	21	-	Α



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

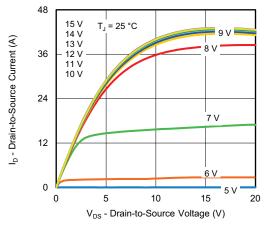


Fig. 1 - Typical Output Characteristics

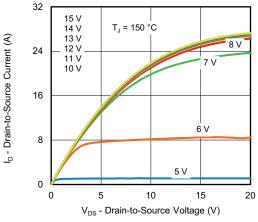


Fig. 2 - Typical Output Characteristics

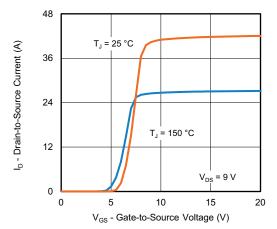


Fig. 3 - Typical Transfer Characteristics

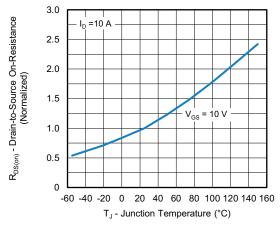


Fig. 4 - Normalized On-Resistance vs. Temperature

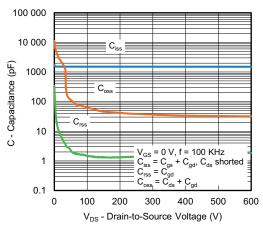


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

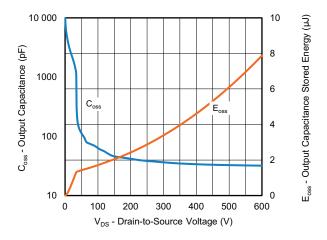


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



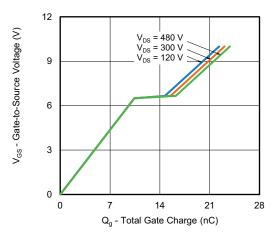


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

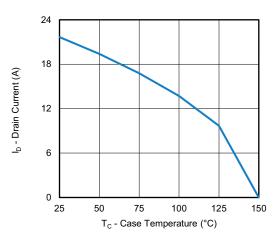


Fig. 9 - Maximum Drain Current vs. Case Temperature

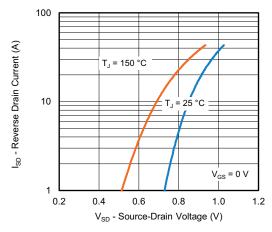


Fig. 8 - Typical Source-Drain Diode Forward Voltage

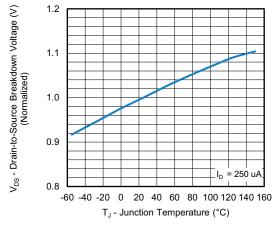


Fig. 10 - Temperature vs. Drain-to-Source Voltage

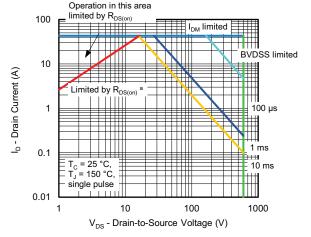


Fig. 11 - Maximum Safe Operating Area

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



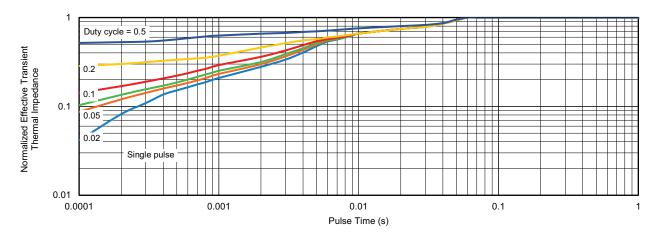


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

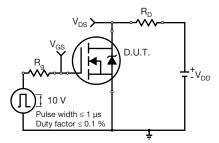


Fig. 13 - Switching Time Test Circuit

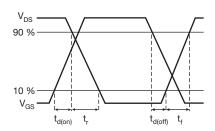


Fig. 14 - Switching Time Waveforms

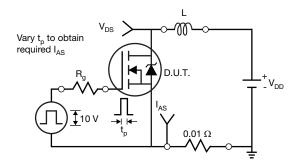


Fig. 15 - Unclamped Inductive Test Circuit

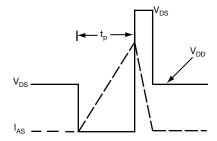


Fig. 16 - Unclamped Inductive Waveforms

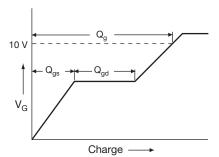


Fig. 17 - Basic Gate Charge Waveform

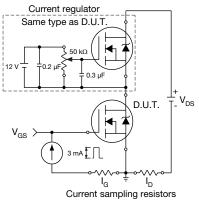
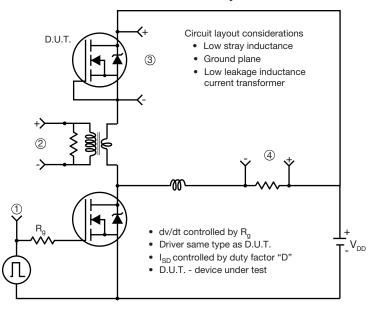


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



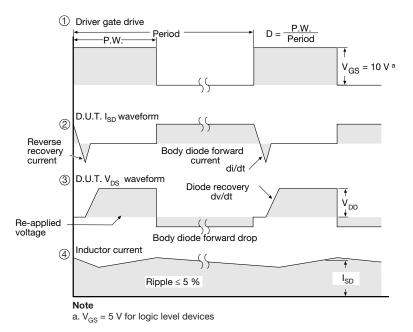


Fig. 19 - For N-Channel

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