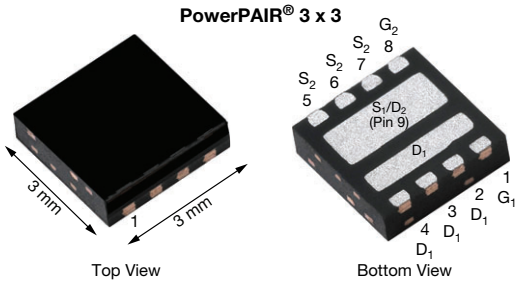
Dual N-Channel 30 V (D-S) MOSFETs



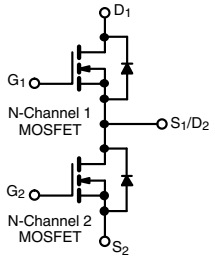
FEATURES

- TrenchFET® Gen IV power MOSFETs
- 100 % R_g and UIS tested
- PowerPAIR® integrated half-bridge MOSFET power stage
- Optimized Q_{gd}/Q_{gs} ratio improves switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY

	CHANNEL-1	CHANNEL-2
V_{DS} (V)	30	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00856	0.00431
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.01403	0.00670
Q_g typ. (nC)	3.7	8.4
I_D (A) [a]	36	69.3
Configuration	Dual	

ORDERING INFORMATION

Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ340BDT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT
Drain-source voltage		V_{DS}	30	30	V
Gate-source voltage		V_{GS}	+20, -16	+20, -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	36	69.3	A
	T_C = 70 °C		28.8	55.4	
	T_A = 25 °C		16.9 [b, c]	25.3 [b, c]	
	T_A = 70 °C		13.5 [b, c]	20.2 [b, c]	
Pulsed drain current (100 µs pulse width)		I_{DM}	100	150	
Continuous source drain diode current	T_C = 25 °C	I_S	13.9	25.8	
	T_A = 25 °C		3.1 [b, c]	3.5 [b, c]	
Single pulse avalanche current	L = 100 mH	I_{AS}	10	15	
Single pulse avalanche energy		E_{AS}	5	11	mJ
Maximum power dissipation	T_C = 25 °C	P_D	16.7	31	W
	T_C = 70 °C		10.7	20	
	T_A = 25 °C		3.7 [b, c]	4.2 [b, c]	
	T_A = 70 °C		2.4 [b, c]	2.7 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	27	34	24	30	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	6	7.5	3.2	4	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch-1	30	-	-	V
		V_{GS} = 0 V, I_D = 250 µA	Ch-2	30	-	-	
V_{DS} Temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 10 mA	Ch-1	-	25.1	-	mV/°C
		I_D = 10 mA	Ch-2	-	24.3	-	
$V_{GS(th)}$ Temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	Ch-1	-	4.0	-	
		I_D = 250 µA	Ch-2	-	4.6	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1.1	-	2.4	V
		V_{DS} = V_{GS}, I_D = 250 µA	Ch-2	1.1	-	2.4	
Gate source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V / -16 V	Ch-1	-	-	100	nA
		V_{DS} = 0 V, V_{GS} = +20 V / -16 V	Ch-2	-	-	100	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch-1	-	-	1	µA
		V_{DS} = 30 V, V_{GS} = 0 V	Ch-2	-	-	1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1	-	-	10	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-2	-	-	10	
On-state drain current [b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	Ch-1	15	-	-	A
		V_{DS} ≥ 5 V, V_{GS} = 10 V	Ch-2	15	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	Ch-1	-	0.00713	0.00856	Ω
		V_{GS} = 10 V, I_D = 20 A	Ch-2	-	0.00359	0.00431	
		V_{GS} = 4.5 V, I_D = 7 A	Ch-1	-	0.01122	0.01403	
		V_{GS} = 4.5 V, I_D = 15 A	Ch-2	-	0.00529	0.00670	
Forward transconductance [b]	g_{fs}	V_{GS} = 10 V, I_D = 10 A	Ch-1	-	30	-	S
		V_{GS} = 10 V, I_D = 10 A	Ch-2	-	60	-	
Dynamic [a]							
Input capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 10 V, f = 1 MHz Channel-2 V_{DS} = 15 V, V_{GS} = 10 V, f = 1 MHz	Ch-1	-	550	-	pF
			Ch-2	-	1065	-	
Output capacitance	C_{oss}		Ch-1	-	235	-	
			Ch-2	-	440	-	
Reverse transfer capacitance	C_{rss}		Ch-1	-	30	-	
			Ch-2	-	33	-	
C_{rss}/C_{iss} ratio			Ch-1	-	0.052	0.103	
			Ch-2	-	0.031	0.062	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 15 A	Ch-1	-	8.4	12.6	nC
		V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	Ch-2	-	15.7	23.5	
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A	Ch-1	-	4.0	6.0	
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-2	-	7.3	11	
Gate-source charge	Q_{gs}	Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-1	-	2.2	-	
			Ch-2	-	3.9	-	
Gate-drain charge	Q_{gd}		Ch-1	-	1.0	-	
			Ch-2	-	1.7	-	
Output charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	Ch-1	-	0.9	-	
			Ch-2	-	1.4	-	
Gate resistance	R_g	f = 1 MHz	Ch-1	0.2	1	2	Ω
			Ch-2	0.2	1	2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Dynamic [a]							
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1	-	8	20	ns
			Ch-2	-	12	24	
Rise time	t_r		Ch-1	-	6	12	
			Ch-2	-	7	14	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	18	36	
			Ch-2	-	22	33	
Fall time	t_f		Ch-1	-	5	10	
			Ch-2	-	7	14	
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 1.5 Ω, $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1	-	15	25	
			Ch-2	-	20	40	
Rise time	t_r		Ch-1	-	450	675	
			Ch-2	-	230	345	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	10	20	
			Ch-2	-	20	40	
Fall time	t_f		Ch-1	-	14	28	
			Ch-2	-	13	26	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	Ch-1	-	-	13.9	A
			Ch-2	-	-	25.8	
Pulse diode forward current (t = 100 µs)	I_{SM}		Ch-1	-	-	100	
			Ch-2	-	-	150	
Body diode voltage	V_{SD}	I_S = 8 A, V_{GS} = 0 V	Ch-1	-	0.83	1.2	V
		I_S = 10 A, V_{GS} = 0 V	Ch-2	-	0.80	1.2	
Body diode reverse recovery time	t_{rr}	Channel-1 I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C Channel-2 I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C	Ch-1	-	21	42	ns
			Ch-2	-	15	68	
Body diode reverse recovery charge	Q_{rr}		Ch-1	-	11	22	nC
			Ch-2	-	5	10	
Reverse recovery fall time	t_a		Ch-1	-	11	-	ns
			Ch-2	-	7	-	
Reverse recovery rise time	t_b		Ch-1	-	10	-	
			Ch-2	-	8	-	

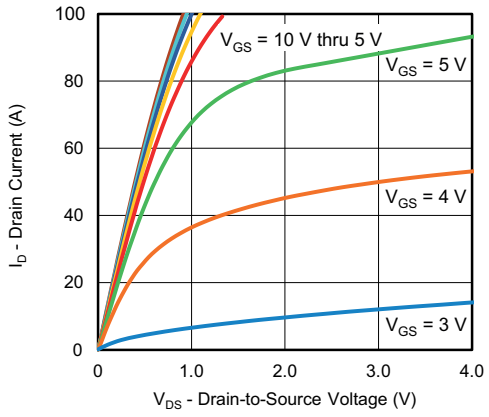
Notes

a. Guaranteed by design, not subject to production testing

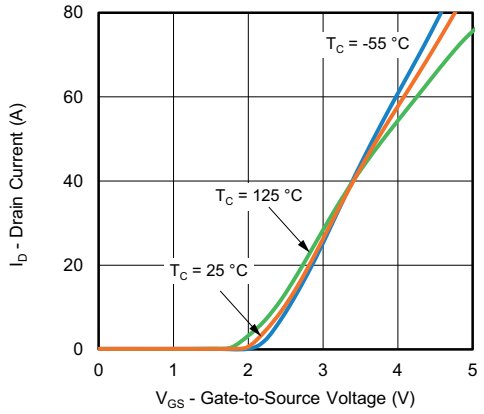
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

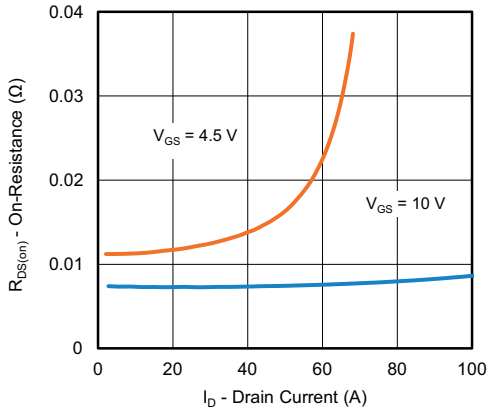
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



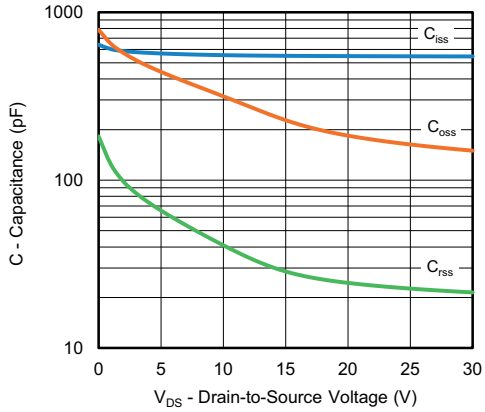
Output Characteristics



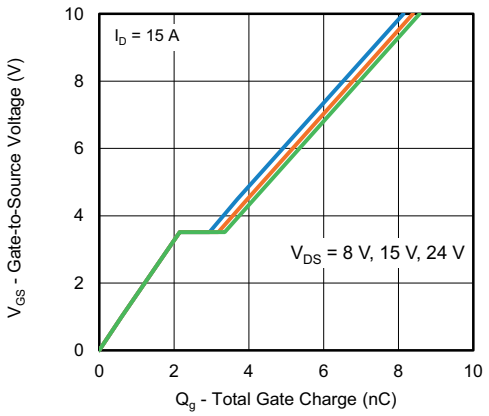
Transfer Characteristics



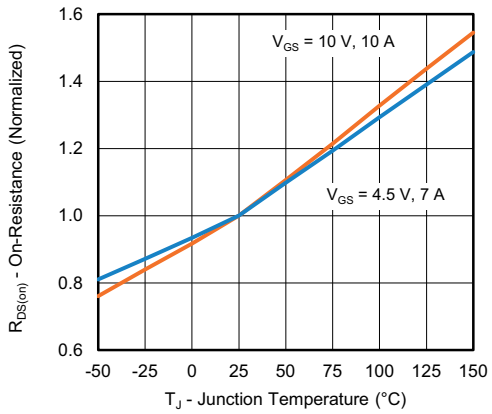
On-Resistance vs. Drain Current



Capacitance

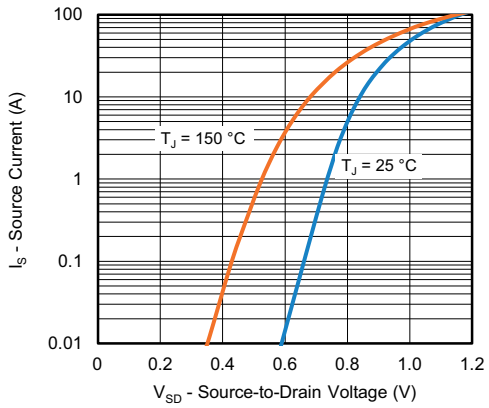


Gate Charge

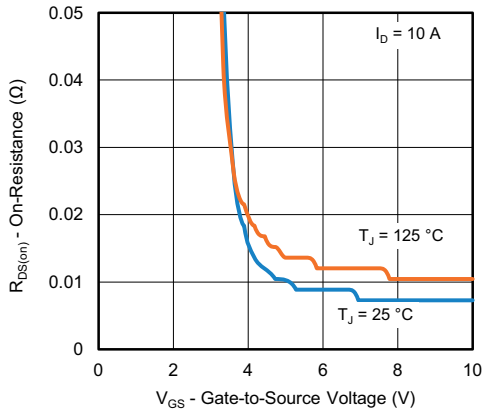


On-Resistance vs. Junction Temperature

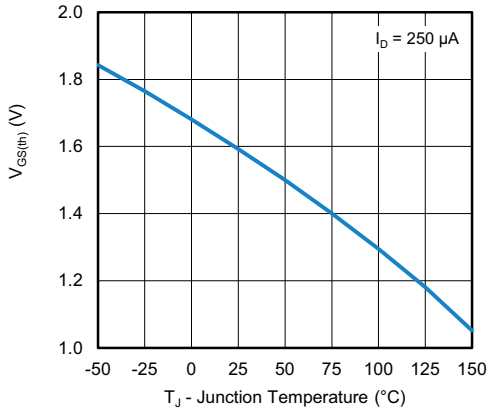
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



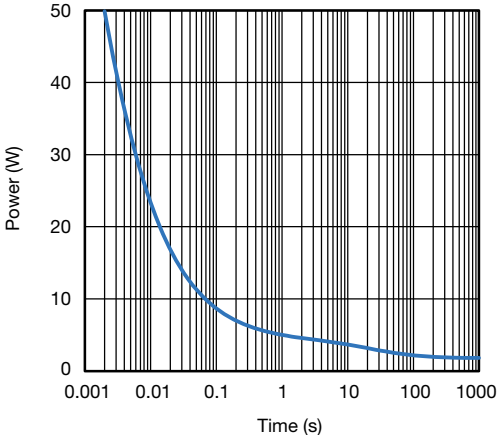
Source-Drain Diode Forward Voltage



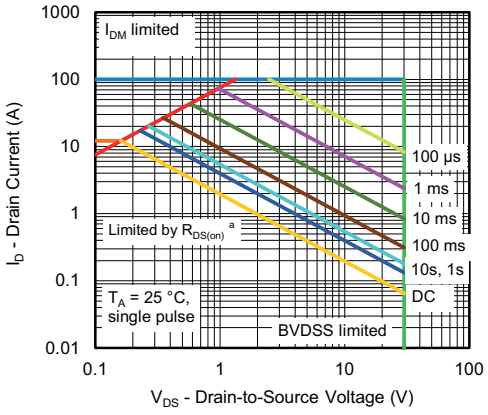
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

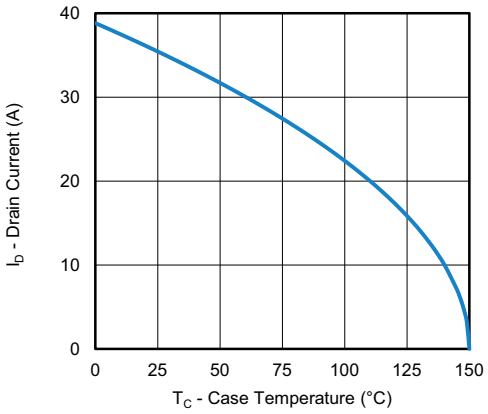


Safe Operating Area, Junction-to-Ambient

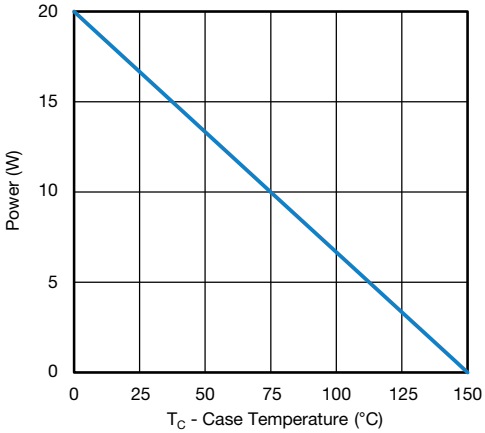
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

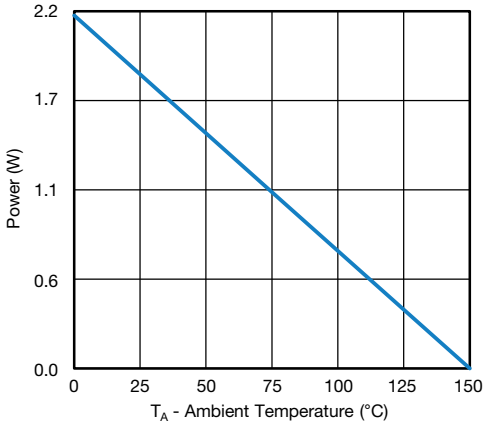
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

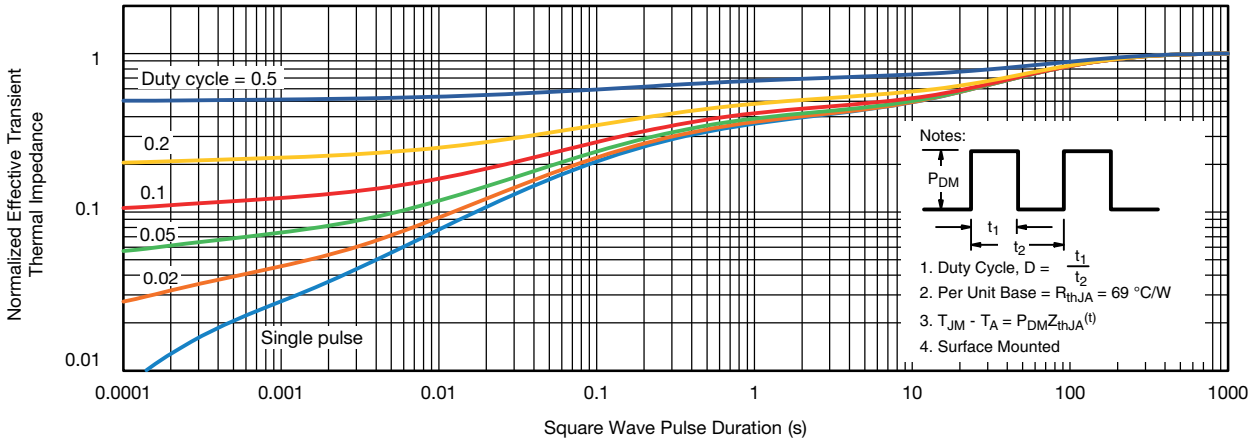


Power, Junction-to-Ambient

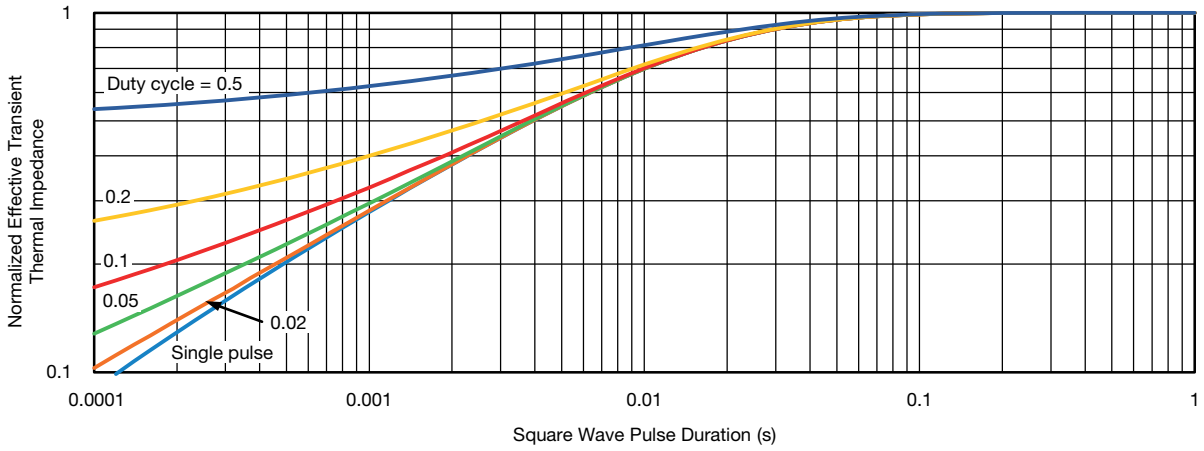
Note

b. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

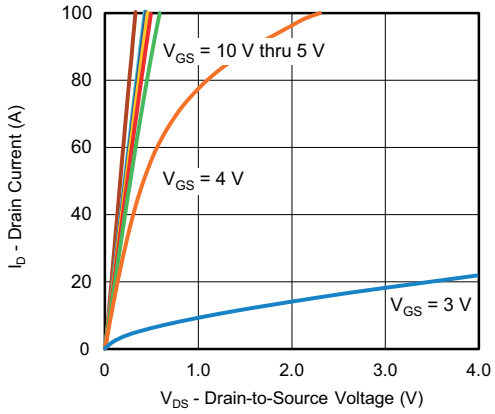


Normalized Thermal Transient Impedance, Junction-to-Ambient

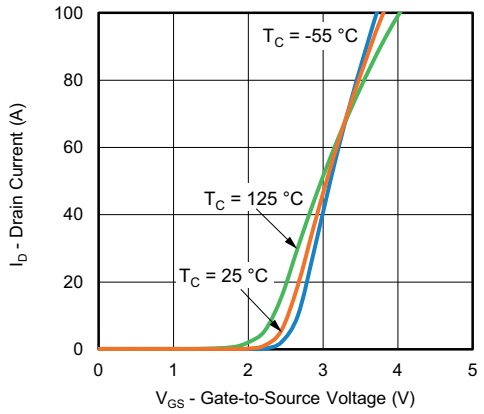


Normalized Thermal Transient Impedance, Junction-to-Case

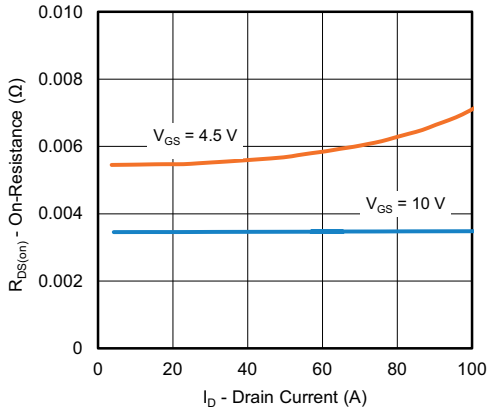
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



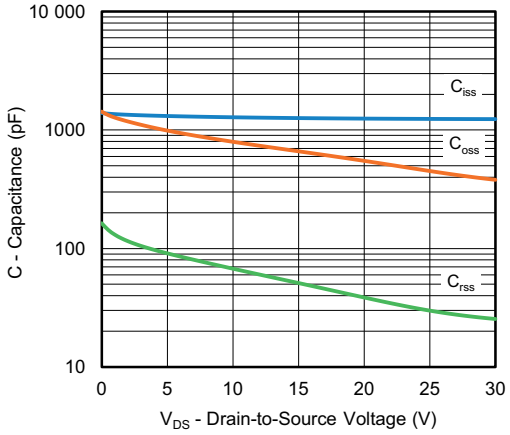
Output Characteristics



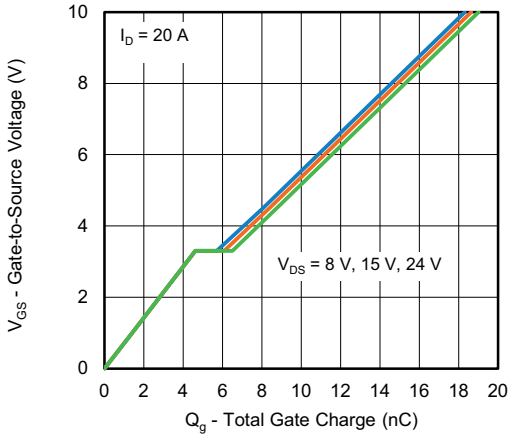
Transfer Characteristics



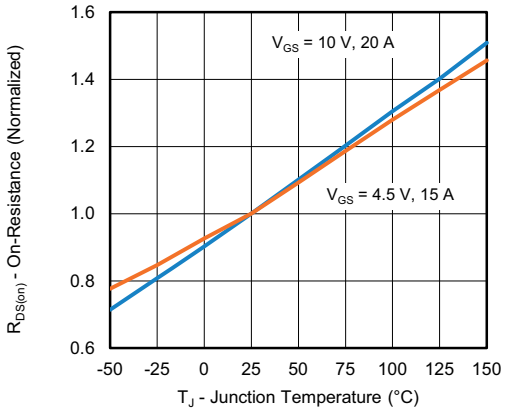
On-Resistance vs. Drain Current



Capacitance

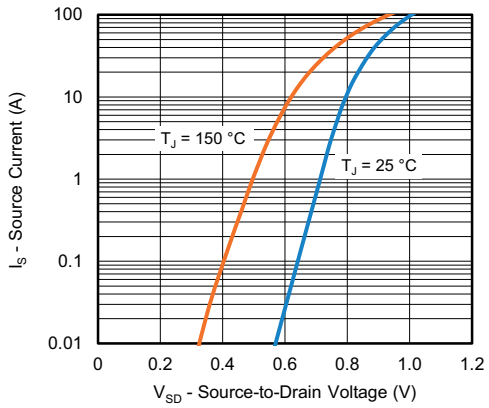


Gate Charge

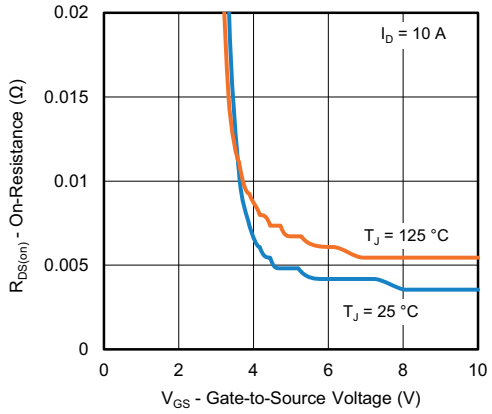


On-Resistance vs. Junction Temperature

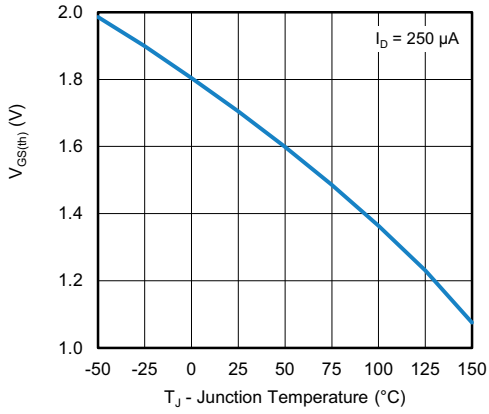
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



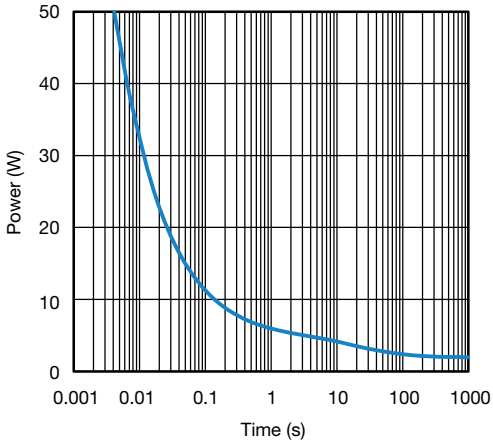
Source-Drain Diode Forward Voltage



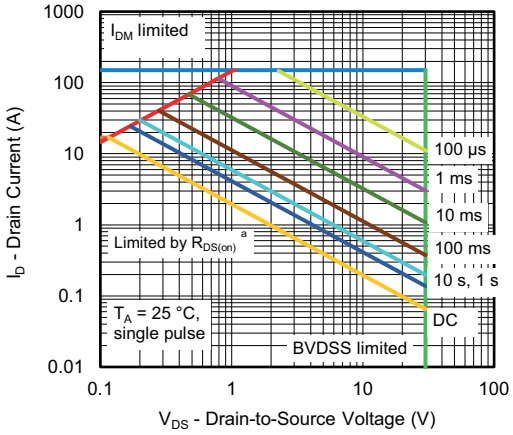
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

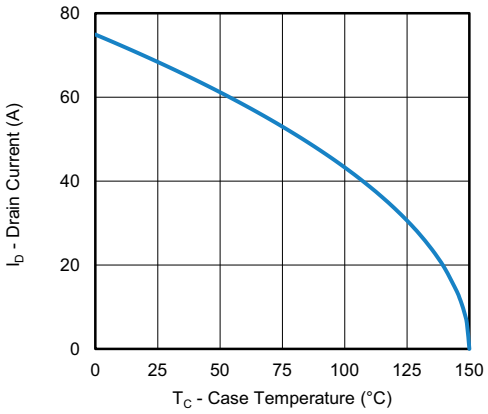


Safe Operating Area, Junction-to-Ambient

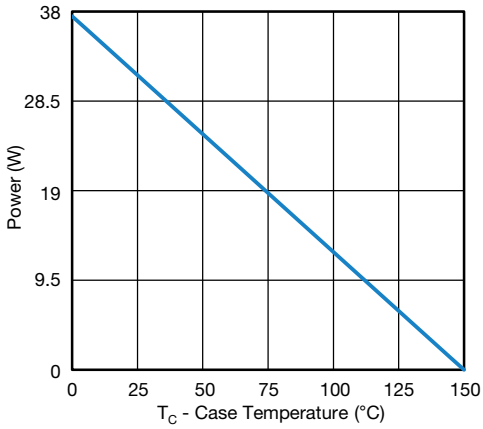
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

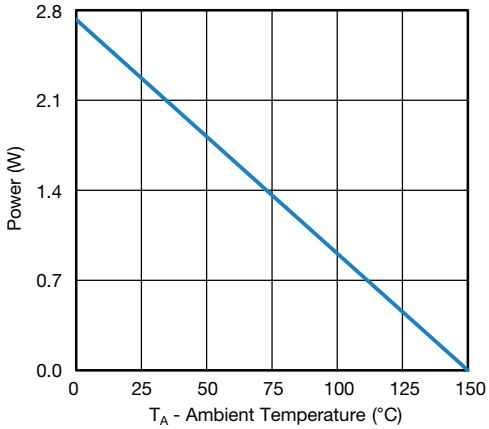
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

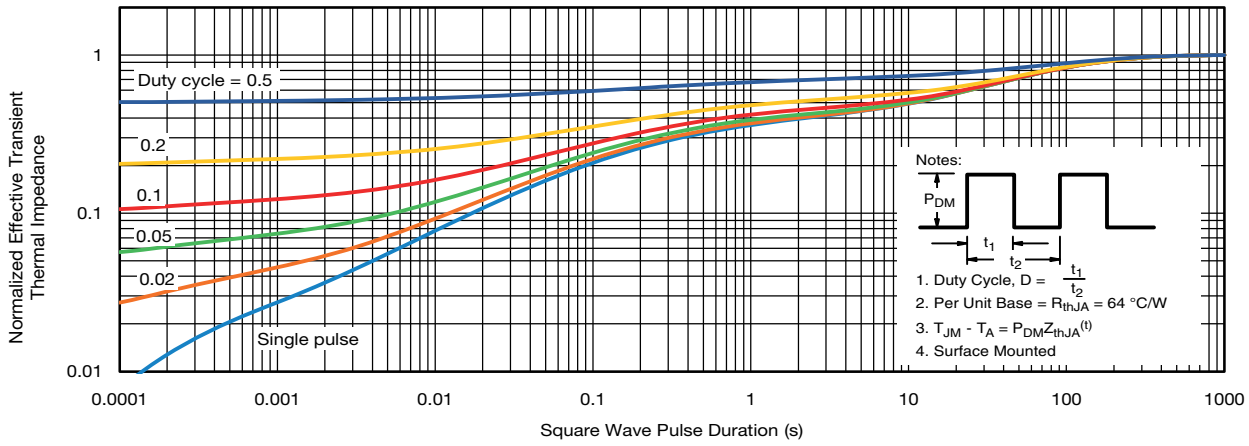


Power, Junction-to-Ambient

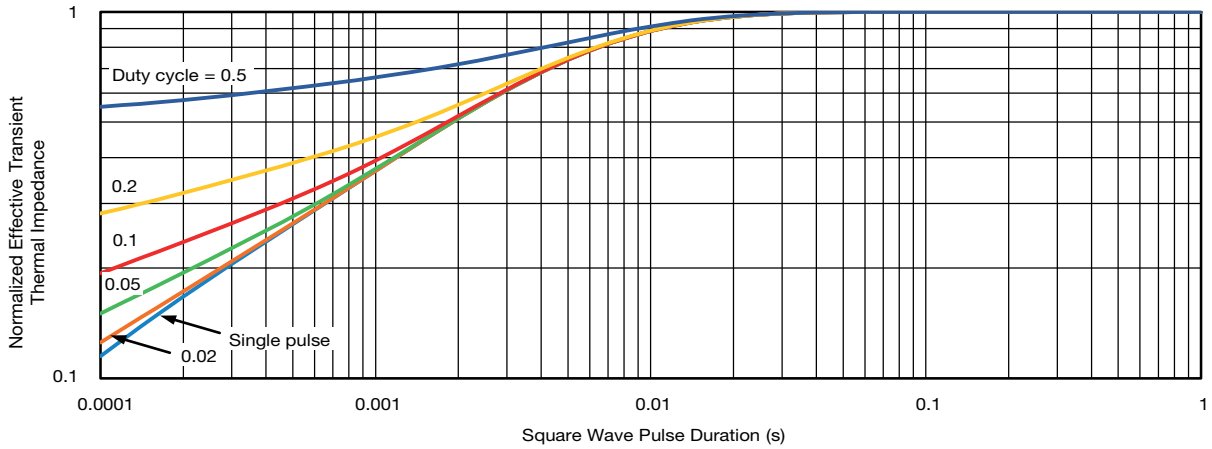
Note

a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



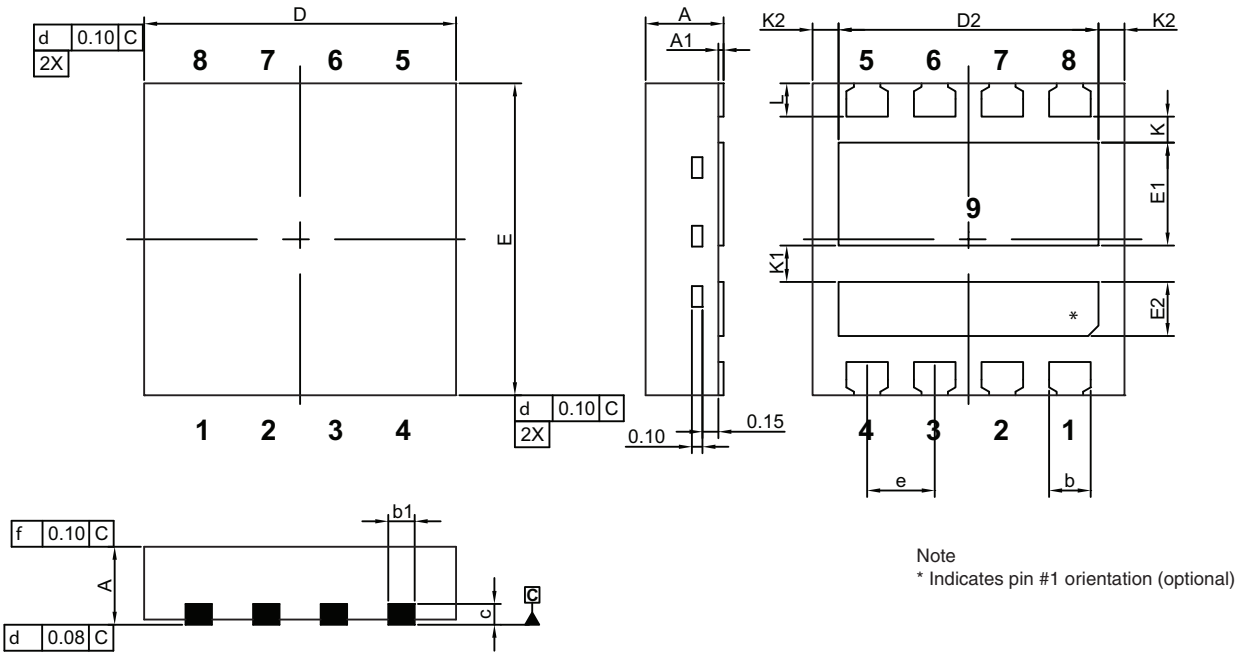
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78132.

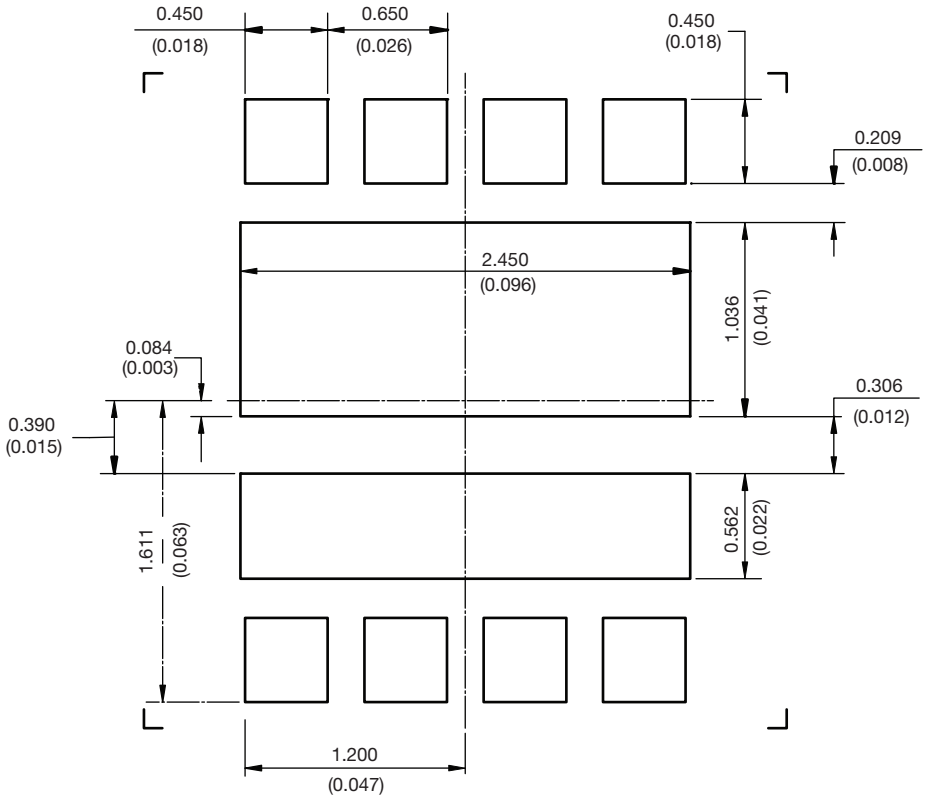
PowerPAIR® 3 x 3 Case Outline



Note
* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12 DWG: 5998						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces

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