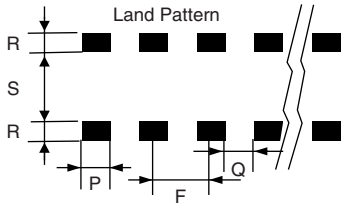
ESCC 4001/025 (e) Qualified High Precision Thin Film Chip Resistor Arrays

LINKS TO ADDITIONAL RESOURCES

3D Models

Vishay Sfernice Thin Film division holds ESCC QML qualification (ESCC technology flow qualification). PRA Hi-Rel arrays can be used in most applications requiring a matched pair (or set) of resistor elements. The networks provide 3 ppm/°C TCR tracking, a ratio tolerance as tight as 0.05 % and outstanding stability. They are available in 1 mm, 1.35 mm, and 1.82 mm pitch.

DIMENSIONS



DIM.	PRA HR 100		PRA HR 135		PRA HR 182	
	mm	mil	mm	mil	mm	mil
A	1.6 $^{+0.2}_{-0.1}$	63	1.85 $^{+0.2}_{-0.1}$	72	3.0 $^{+0.2}_{-0.1}$	118
B	0.34 ± 0.17	13	0.34 ± 0.17	13	0.34 ± 0.17	13
C	0.65 $^{+0.15}_{-0.15}$	25.5	1.05 $^{+0.15}_{-0.15}$	41	1.3 $^{+0.35}_{-0.15}$	51
D	0.25	10	0.25	10	0.25	10
E (1)	E = (N x F) ± 0.2 mm		E = (N x F) ± 8 mil			
F	1	40	1.35	53.1	1.82	72
G	0.38 $^{+0.2}_{-0}$	15	0.38 $^{+0.2}_{-0}$	15	0.38 $^{+0.2}_{-0}$	15
P	0.7	27.5	1.05	41.3	1.52	59.8
Q	0.3	12	0.3	12	0.3	12
R	1	40	1	40	1	40
S	0.6	23.5	0.8	31.5	1.8	70.8

Note

(1) E depends on number of resistors

FEATURES

HALOGEN FREE

- Thin film technology
- High stability passivated nichrome resistive layer 0.02 % on ratio, 1000 h at Pn at +70 °C
- Tight TCR (10 ppm/°C) and TCR tracking (3 ppm/°C)
- Very low noise < -35 dB and voltage coefficient < 0.01 ppm/V
- Ratio tolerance to 0.01 % ($R \geq 200R$)
- Pre-tinned terminations over nickel barrier
- ESA/ESCC qualified
- ESCC 4001 (generic specification)
- ESCC 4001/025 (detailed specification)
- SMD wraparound chip resistor array
- Up to eight different ohmic values (CNW HR)
- Suitable for military use
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

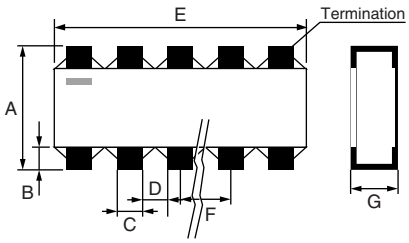
TYPICAL PERFORMANCE

	ABSOLUTE	TRACKING
TCR	10 ppm/°C	3 ppm/°C
	ABSOLUTE	RATIO
TOL.	0.1 %	0.05 %

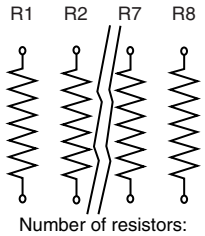
TC tracking: 3 ppm/°C if all resistors of the array are: Rn > 250 Ω

TC tracking: 5 ppm/°C if one or more resistors of the array is in the range: 100 Ω to 250 Ω included

I: Independent resistors

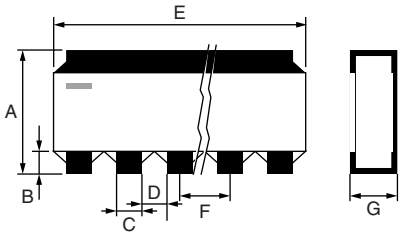


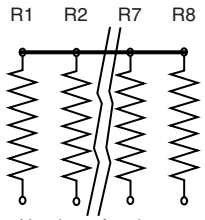
Electrical diagram



Number of resistors: 2 to 8
R1 = R2 = ... R8

C: One common point N resistors





Number of resistors: 2 to 8
R1 = R2 = ... R8

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: PRAHR100I4-10K2BWBT

P	R	A	H	R	1	0	0	I	4	-	1	0	K	2	B	W	B	T

GLOBAL MODEL	CONFIGURATION	NUMBERS OF RESISTORS	OHMIC VALUE IN CLEAR (1)	ABS. TOL.	RATIO TOL.	TERMINATION	PACKAGING
PRA HR 100 **PRA HR 135** **PRA HR 182**	**I**: Independent	**2** to **8**	Decimal R, K or M	**B** = 0.1 % **D** = 0.5 % **F** = 1 %	**W** = 0.05 % **B** = 0.1 %	SnPb over nickel barrier	For more information see “Codification of packaging” table

For different ohmic values on a given network a specific number is used

CNW HR	1368	T
GLOBAL MODEL	CUSTOM NETWORK REFERENCE	For more information see “Codification of packaging” table

Notes

- Part number is limited to 18 digits, so packing must be omitted and mentioned in comment on order. Otherwise ESCC code should be used for ordering

(1) When the last digit(s) of the ohmic value is (are) 0, it (they) must be omitted.
E.g.:PRAHR100I4-2K20BWN → must be ordered under PRAHR100I4-2K2BWN
PRAHR100I4-2K00BWN → must be ordered under PRAHR100I4-2KBWN

ESCC CODE

4	0	0	1	0	2	5	0	1	1	0	0	1	B	W	1

DETAILED SPEC. NUMBER	VARIANT NUMBER	RESISTANCE VALUE	ABSOLUTE TOLERANCE	RATIO TOLERANCE	ABSOLUTE TCR
	01 to **21**	The first three digits are significant figures and the last digit specifies the number of zeros to follow. Example: **3901** = 3900 Ω **1004** = 1 MΩ	**B** = 0.1 % **D** = 0.5 % **F** = 1 %	**W** = 0.05 % **B** = 0.1 %	**1** = 10 ppm/°C

4	0	0	1	0	2	5	2	2	1	2	2	9	B	W	1

DETAILED SPEC. NUMBER	VARIANT NUMBER	CUSTOM NETWORK REFERENCE	ABSOLUTE TOLERANCE	RATIO TOLERANCE	ABSOLUTE TCR
	22 to **42**	Four digits number defined per Vishay Sfernice	**B** = 0.1 % **D** = 0.5 % **F** = 1 %	**W** = 0.05 % **B** = 0.1 %	**1** = 10 ppm/°C

CODIFICATION OF PACKAGING

CODE 18	PACKAGING
WAFFLE PACK	
W	25 min., 1 mult.
PLASTIC TAPE (Standard for all sizes.)	
T	50 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)

EXAMPLES OF CROSS REFERENCE BETWEEN ESA PART NUMBER AND VISHAY PART NUMBER						
ESA PART NUMBER	VISHAY PART NUMBER	EXPLANATIONS				
4001025011001BW1	PRAHR100I2-1K00BWB	4001025 = PRAHR or CNWHR	01 = 100I2 with 2 identical values and B termination	1001 = 1K00	BW = BW	1 = TCR 10 ppm abs: not mentioned in Vishay P/N
4001025221229BW1	CNWHR1229	4001025 = PRAHR or CNWHR	22 = 100I2 with 2 different values, B terminations	1229 = Vishay custom reference number	BW = Tolerances mentioned in custom file	1 = TCR 10 ppm abs: not mentioned in Vishay P/N

CROSS REFERENCE ESA PART NUMBER AND PRAHR PART NUMBER								
VARIANT ESA	VISHAY MODELS		VARIANT ESA	VISHAY MODELS		VARIANT ESA	VISHAY MODELS
01	PRAHR100I2 same value		15	PRAHR182I2 same value		29	PRAHR135I2 different value
02	PRAHR100I3 same value		16	PRAHR182I3 same value		30	PRAHR135I3 different value
03	PRAHR100I4 same value		17	PRAHR182I4 same value		31	PRAHR135I4 different value
04	PRAHR100I5 same value		18	PRAHR182I5 same value		32	PRAHR135I5 different value
05	PRAHR100I6 same value		19	PRAHR182I6 same value		33	PRAHR135I6 different value
06	PRAHR100I7 same value		20	PRAHR182I7 same value		34	PRAHR135I7 different value
07	PRAHR100I8 same value		21	PRAHR182I8 same value		35	PRAHR135I8 different value
08	PRAHR135I2 same value		22	PRAHR100I2 different value		36	PRAHR182I2 different value
09	PRAHR135I3 same value		23	PRAHR100I3 different value		37	PRAHR182I3 different value
10	PRAHR135I4 same value		24	PRAHR100I4 different value		38	PRAHR182I4 different value
11	PRAHR135I5 same value		25	PRAHR100I5 different value		39	PRAHR182I5 different value
12	PRAHR135I6 same value		26	PRAHR100I6 different value		40	PRAHR182I6 different value
13	PRAHR135I7 same value		27	PRAHR100I7 different value		41	PRAHR182I7 different value
14	PRAHR135I8 same value		28	PRAHR100I8 different value		42	PRAHR182I8 different value

TRACEABILITY DEFINITIONS

The two major traceability elements are defined as:

- The primary process lot number named Front End lot (FE lot). One “FE lot” is composed of several wafers issued from the same thin film deposition sequence.
- The date code named Batch Number (BN). The “BN” is defined after completion of the end of production testing sequence.

The lot homogeneity is given by the “FE lot” and not by the “BN”.

According to the applied rules validated by the ESCC through the product qualification, the following situations are agreed:

- Parts coming from different “FE lost” might have the same “BN”.
- A maximum of two different “BN” might be applied to the same “FE lot” to enable the use of overruns from a previous PO.
- Unless requested / approved by the customer the “BN” will be 2 years old maximum.

SPECIFIC TRACEABILITY REQUIREMENTS

The following specific requirements have to be treated as:

- A customer who requires “Lot Homogeneity” has to mention it on the PO as “SINGLE PRODUCTION LOT”.
- A customer who requires “Lot Homogeneity” in addition to a “Single Batch Number” has to mention it on the PO as “SINGLE PRODUCTION LOT AND OPTION R0101”.

END OF PRODUCTION TESTING

Mandatory testing performed at the end of the production process:

- 100 % overload: voltage $\sqrt{(6.25\ P_n \times R_n)}$ or 2 UL whichever is less - duration 2 s
- 100 % burn in: 168 h at P_n at 70 °C

OPTIONS

LOT VALIDATION TESTING

For procurement of qualified components, lot validation testing is not required and shall only be performed if specifically stipulated in the purchase order.

For procurement of unqualified components, lot validation testing shall be performed as stipulated in the purchase order. The need for lot validation testing shall be determined by the orderer.

When lot validation testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of chart F4 indicated in the ESA Generic Specification ESCC 4001. The testing to be performed and the sample size shall be as stipulated in the purchase order. When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the purchase order.

Lot validation testing will be composed of one LVT charges and LVT samples:
Lot validation test charges has to be ordered separately on purchase order.
Lot validation samples have to be ordered separately on purchase order.

FINAL INSPECTION

If requested by the orderer a final inspection can be performed on site.
Final inspection has to be stipulated separately on purchase order.

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE Ω	POWER RATING (1) W	ABSOLUTE TOLERANCE ± %	RATIO TOLERANCE %	ABSOLUTE TCR (2) ± ppm/°C	RATIO TCR (3) ± ppm/°C
PRA HR 100	100	100 to 200K	0.100	0.1, 0.5, 1	0.05, 0.1	10	3
PRA HR 135	135	100 to 250K	0.100	0.1, 0.5, 1	0.05, 0.1	10	3
PRA HR 182	182	100 to 1M	0.100	0.1, 0.5, 1	0.05, 0.1	10	3

Notes

(1) Per resistor at +70 °C
(2) At -40 °C +155 °C
(3) If all resistors of the array are: Rn > 250 Ω at -40 °C to +155 °C

PEFORMANCES

TEST		SPECIFICATIONS	CONDITION
Soldering temperature		260 °C	Max.
Limiting voltage	**PRA HR 100**	35 V	
	PRA HR 135	75 V	
	PRA HR 182	100 V	
Insulation voltage	**PRA HR 100**	70 V_{RMS}	
	PRA HR 135	150 V_{RMS}	
	PRA HR 182	200 V_{RMS}	

CLIMATIC SPECIFICATIONS

Operating temperature range	-65 °C to +155 °C
Storage temperature range	-65 °C to +155 °C

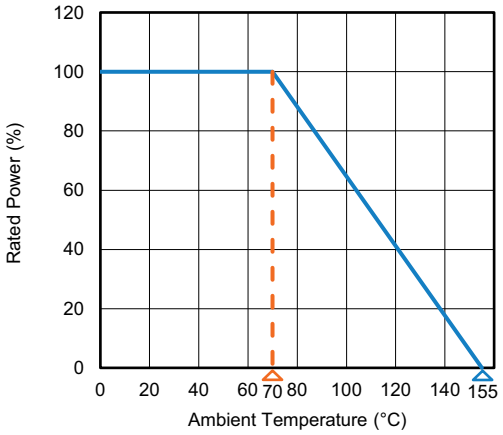
MECHANICAL SPECIFICATIONS

Substrate	Alumina
Technology	Thin Film
Film	Nickel chromium with mineral passivation
Terminations	**B type**: SnPb over nickel barrier

SPECIAL FEATURES

Resistance values can be different on a given network (*R* max./*R* min. as high as 300). Tooling charges might be required depending on the ohmic values in the same network. Please, consult Vishay Sfernice for ohmic values, tolerances and also temperature coefficient outside the standard range.

POWER RATING



PACKAGING

Several types of packaging are available: Waffle-pack and tape and reel.

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE		
		WAFFLE PACK MAX. QUANTITY PER BOX	TAPE AND REEL (1)	
			MIN.	MAX.
PRA100 x 2	25 in waffle pack 50 in tape and reel	100	50	4000
PRA100 x 3		140	50	4000
PRA100 x 4		60	50	4000
PRA100 x 5		50		
PRA100 x 6		50	50	3000
PRA100 x 7		50		
PRA100 x 8		28	50	4000
PRA135 x 2	25 in waffle pack 50 in tape and reel	140	50	4000
PRA135 x 3		60		
PRA135 x 4		60	50	2500
PRA135 x 5		50		
PRA135 x 6		28	50	4000
PRA135 x 7		24		
PRA135 x 8		24		
PRA182 x 2	25 in waffle pack 50 in tape and reel	60	50	2000
PRA182 x 3		60	50	4000
PRA182 x 4		50	50	2000
PRA182 x 5		21	50	1500
PRA182 x 6		24		
PRA182 x 7		24		
PRA182 x 8		20		

Note

(1) Other sizes upon request

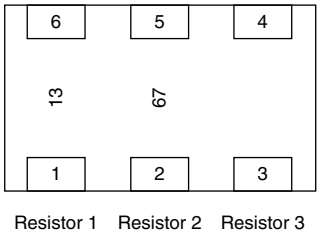
MARKING

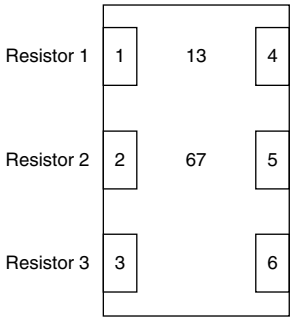
The marking of all components delivered to this specification shall be in accordance with the requirements of ESCC Basic Specifications No. 21700. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany each component in its primary package.

The information to be marked and the order of precedence, shall be as follows:

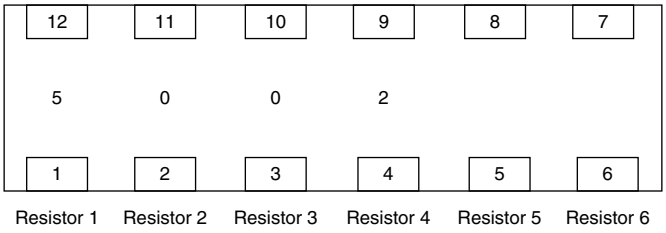
- Rated Resistance (for variants 01 to 21); Terminal identification and array reference code (for variants 22 to 42) (see Physical Dimensions and Terminal Identification)
- The ESCC qualified components symbol (for ESCC qualified components only)
- The ESCC component number
- Traceability information

Terminal identification shall be by means of the location of the marking. Due to the size of the component only the 4 digit resistance value code or array reference code, as applicable (see the ESCC component number), shall be marked on the component.
For symmetrical marking using reversible figures such as 0, 6 or 9, the first resistor of the array, R1, shall be identified by a dot. For arrays with 2 or 3 resistors, the marking shall be located adjacent to the first 2 resistors of the array. The first resistor, R1, of the array is the upper resistor whilst reading the marking, as follows:





For arrays with 4 to 8 resistors, the marking shall be located adjacent to the first 4 resistors of the array. The first resistor, R1, of the array is on the left hand end of the array whilst reading the marking, as follows:



PERFORMANCE			
TESTS	CONDITIONS CECC REQUIREMENTS	DRIFTS	
		ABSOLUTE PER (TYPICAL VALUES)	RATIO
Overload	2.5 Un/2 s	0.05 % Rn + 0.05 Ω	0.01 % Rn
Climatic sequences	-55 °C to +155 °C/5 moisture cycles	0.1 % Rn + 0.05 Ω	0.01 % Rn
Thermal shock	-55 °C to +155 °C/5 cycles 30'	0.05 % Rn + 0.05 Ω	0.01 % Rn
Load life	1000 h/Pn at +70 °C	0.1 % Rn + 0.05 Ω	0.02 % Rn
	2000 h	0.15 % Rn + 0.05 Ω	
Resistance to solder heat	260 °C/10 s	0.05 % Rn + 0.05 Ω	0.01 % Rn
Moisture resistance	0.01 Pn at 40 °C 93 % RH	0.1 % Rn + 0.05 Ω	0.01 % Rn
High temperature storage	1000 h/no load at +155 °C	0.1 % Rn + 0.05 Ω	0.02 % Rn

Note
- Rn: nominal resistance

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