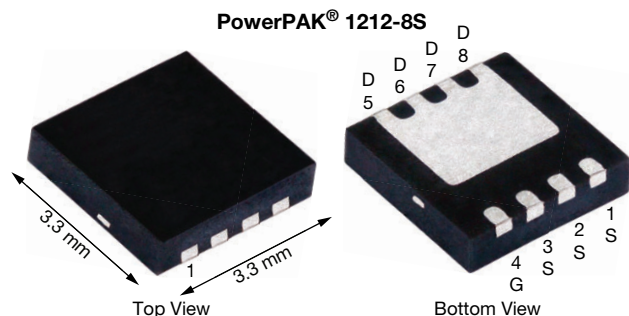


# N-Channel 40 V (D-S) MOSFET



| PRODUCT SUMMARY                                    |        |
|--|--------|
| $V_{DS}$ (V)                                       | 40     |
| $R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V  | 0.0022 |
| $R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V | 0.0032 |
| $Q_g$ typ. (nC)                                    | 21.5   |
| $I_D$ (A) <sup>a</sup>                             | 128    |
| Configuration                                      | Single |

## FEATURES

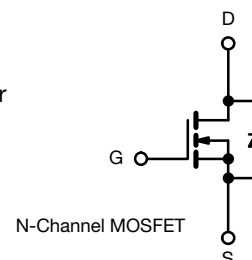
- TrenchFET® Gen IV power MOSFET
- Very low  $Q_g$  and  $Q_{oss}$  reduce power loss and improve efficiency
- Optimized  $Q_g$ ,  $Q_{gd}$ , and  $Q_{gd}/Q_{gs}$  ratio reduces switching related power loss
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
FREE

## APPLICATIONS

- Synchronous rectification
- Synchronous buck converter
- High power density DC/DC
- Load switching



| ORDERING INFORMATION                         |                   |
|--|-------------------|
| Package                                      | PowerPAK 1212-8S  |
| Lead (Pb)-free and halogen-free              | SiSS4402DN-T1-GE3 |
| Lead (Pb)-free and halogen-free, BLR and IOL | SiSS4402DN-T1-UE3 |

| ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted) |                |                      |      |  |
|---|----------------|----------------------|------|--|
| PARAMETER   | SYMBOL         | LIMIT                | UNIT |  |
| Drain-source voltage  | $V_{DS}$       | 40                   | V    |  |
| Gate-source voltage   | $V_{GS}$       | +20 / -16            | V    |  |
| Continuous drain current ( $T_J = 150$ °C)                        | $T_C = 25$ °C  | 128                  | A    |  |
|   | $T_C = 70$ °C  | 103                  |      |  |
|   | $T_A = 25$ °C  | 35.5 <sup>b, c</sup> |      |  |
|   | $T_A = 70$ °C  | 28 <sup>b, c</sup>   |      |  |
| Pulsed drain current ( $t = 100$ $\mu$ s)                         | $I_{DM}$       | 300                  |      |  |
| Continuous source-drain diode current                             | $T_C = 25$ °C  | 59.8                 |      |  |
|   | $T_A = 25$ °C  | 4.5 <sup>b, c</sup>  |      |  |
| Single pulse avalanche current                                    | $I_{AS}$       | 25                   |      |  |
| Single pulse avalanche energy                                     | $E_{AS}$       | 31.25                | mJ   |  |
| Maximum power dissipation   | $T_C = 25$ °C  | 65.7                 | W    |  |
|   | $T_C = 70$ °C  | 42                   |      |  |
|   | $T_A = 25$ °C  | 5 <sup>b, c</sup>    |      |  |
|   | $T_A = 70$ °C  | 3.2 <sup>b, c</sup>  |      |  |
| Operating junction and storage temperature range                  | $T_J, T_{stg}$ | -55 to +150          | °C   |  |
| Soldering recommendations (peak temperature) <sup>c</sup>         |                | 260                  |      |  |

| THERMAL RESISTANCE RATINGS               |               |            |         |         |      |
|--|---------------|------------|---------|---------|------|
| PARAMETER                                |               | SYMBOL     | TYPICAL | MAXIMUM | UNIT |
| Maximum junction-to-ambient <sup>b</sup> | $t \leq 10$ s | $R_{thJA}$ | 20      | 25      | °C/W |
| Maximum junction-to-case (drain)         | Steady state  | $R_{thJC}$ | 1.5     | 1.9     |      |

### Notes

- Based on  $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 63 °C/W



| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                      |   |      |        |        |       |
|---|--------------------------------------|---|------|--------|--------|-------|
| PARAMETER   | SYMBOL                               | TEST CONDITIONS   | MIN. | TYP.   | MAX.   | UNIT  |
| Static  |                                      |   |      |        |        |       |
| Drain-source breakdown voltage                                  | V <sub>DS</sub>                      | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA  | 40   | -      | -      | V     |
| V <sub>DS</sub> temperature coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub>     | I <sub>D</sub> = 250 μA   | -    | 25     | -      | mV/°C |
| V <sub>GS(th)</sub> temperature coefficient                     | ΔV <sub>GS(th)</sub> /T <sub>J</sub> |   | -    | -5.2   | -      |       |
| Gate-source threshold voltage                                   | V <sub>GS(th)</sub>                  | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA   | 1    | -      | 2.5    | V     |
| Gate-source leakage   | I <sub>GSS</sub>                     | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20, -16 V   | -    | -      | ± 100  | nA    |
| Zero gate voltage drain current                                 | I <sub>DSS</sub>                     | V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V   | -    | -      | 1      | μA    |
|   |                                      | V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C   | -    | -      | 10     |       |
| Drain-source on-state resistance <sup>a</sup>                   | R <sub>DS(on)</sub>                  | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A   | -    | 0.0018 | 0.0022 | Ω     |
|   |                                      | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A  | -    | 0.0024 | 0.0032 |       |
| Forward transconductance <sup>a</sup>                           | g <sub>fs</sub>                      | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A   | -    | 98     | -      | S     |
| Dynamic <sup>b</sup>  |                                      |   |      |        |        |       |
| Input capacitance   | C <sub>iss</sub>                     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz  | -    | 3850   | -      | pF    |
| Output capacitance  | C <sub>oss</sub>                     |   | -    | 655    | -      |       |
| Reverse transfer capacitance                                    | C <sub>rss</sub>                     |   | -    | 75     | -      |       |
| Total gate charge   | Q <sub>g</sub>                       | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A   | -    | 46.7   | 70     | nC    |
|   |                                      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A  | -    | 21.5   | 32     |       |
| Q <sub>gs</sub>   | -                                    |   | 9.3  | -      |        |       |
| Q <sub>gd</sub>   | -                                    |   | 4    | -      |        |       |
| Output charge   | Q <sub>oss</sub>                     | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V   | -    | 24.5   | -      |       |
| Gate resistance   | R <sub>g</sub>                       | f = 1 MHz   | 0.5  | 1.1    | 1.8    | Ω     |
| Turn-on delay time  | t <sub>d(on)</sub>                   | V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1 Ω<br>I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω  | -    | 15     | 30     | ns    |
| Rise time   | t <sub>r</sub>                       |   | -    | 6      | 12     |       |
| Turn-off delay time   | t <sub>d(off)</sub>                  |   | -    | 30     | 60     |       |
| Fall time   | t <sub>f</sub>                       |   | -    | 6      | 12     |       |
| Turn-on delay time  | t <sub>d(on)</sub>                   | V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1 Ω<br>I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω | -    | 26     | 52     |       |
| Rise time   | t <sub>r</sub>                       |   | -    | 63     | 126    |       |
| Turn-off delay time   | t <sub>d(off)</sub>                  |   | -    | 33     | 66     |       |
| Fall time   | t <sub>f</sub>                       |   | -    | 10     | 20     |       |
| Drain-Source Body Diode Characteristics                         |                                      |   |      |        |        |       |
| Continuous source-drain diode current                           | I <sub>S</sub>                       | T <sub>C</sub> = 25 °C  | -    | -      | 59.8   | A     |
| Pulse diode forward current (t <sub>p</sub> = 100 μs)           | I <sub>SM</sub>                      |   | -    | -      | 300    |       |
| Body diode voltage  | V <sub>SD</sub>                      | I <sub>S</sub> = 5 A  | -    | 0.73   | 1.1    | V     |
| Body diode reverse recovery time                                | t <sub>rr</sub>                      | I <sub>F</sub> = 10 A, di/dt = 100 A/μs,<br>T <sub>J</sub> = 25 °C  | -    | 29     | 58     | ns    |
| Body diode reverse recovery charge                              | Q <sub>rr</sub>                      |   | -    | 23     | 46     | nC    |
| Reverse recovery fall time                                      | t <sub>a</sub>                       |   | -    | 15     | -      | ns    |
| Reverse recovery rise time                                      | t <sub>b</sub>                       |   | -    | 14     | -      |       |

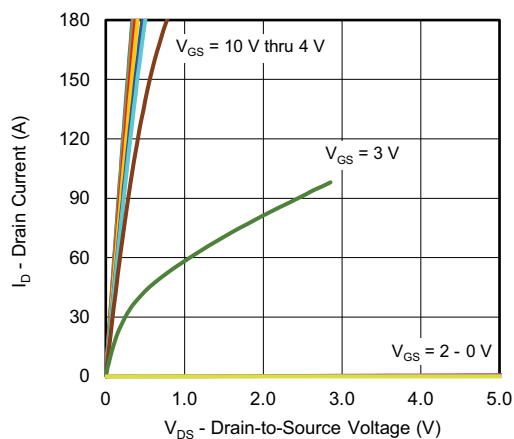
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

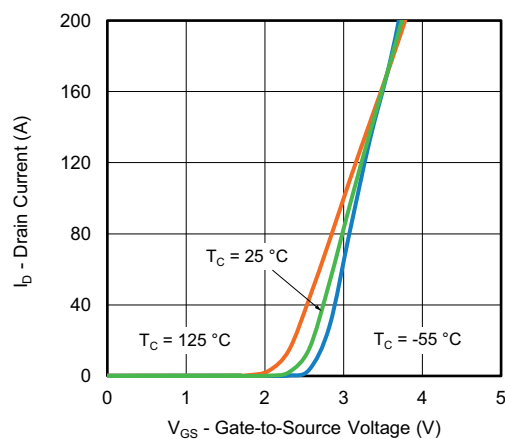
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



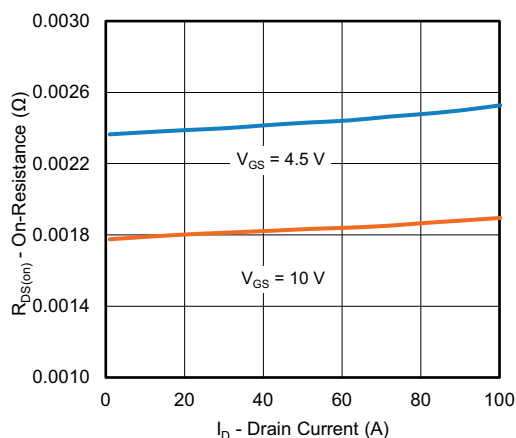
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



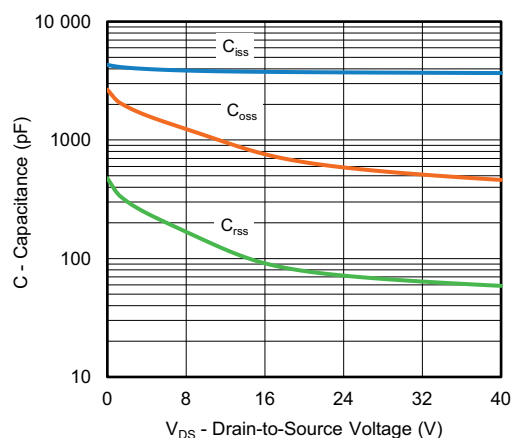
**Output Characteristics**



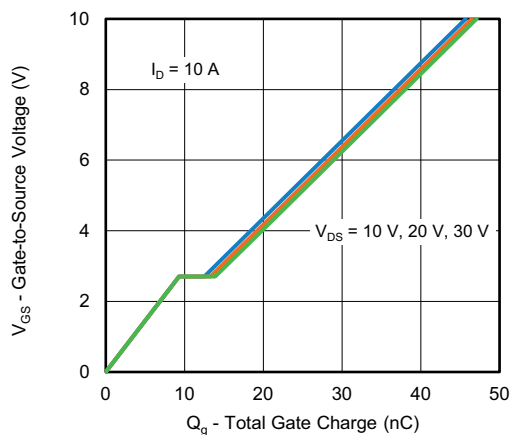
**Transfer Characteristics**



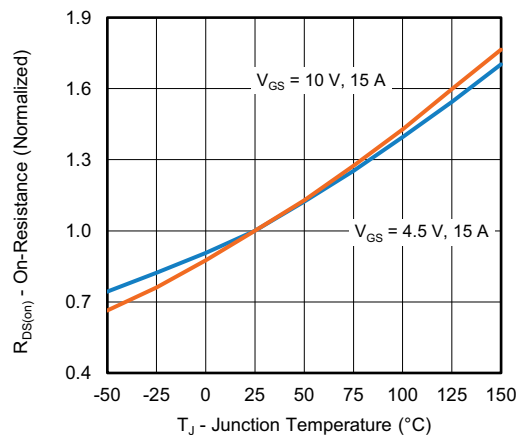
**On-Resistance vs. Drain Current**



**Capacitance**



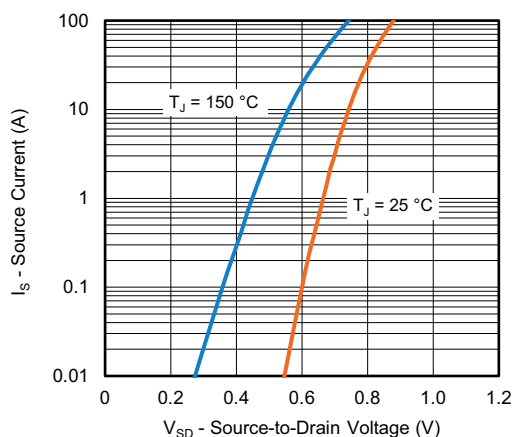
**Gate Charge**



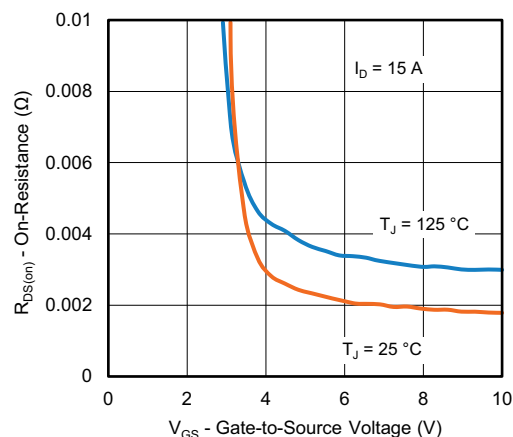
**On-Resistance vs. Junction Temperature**



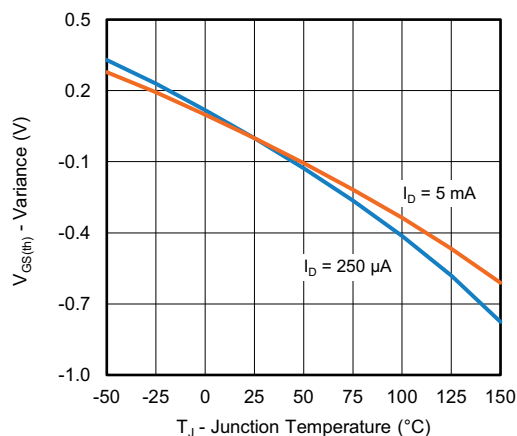
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



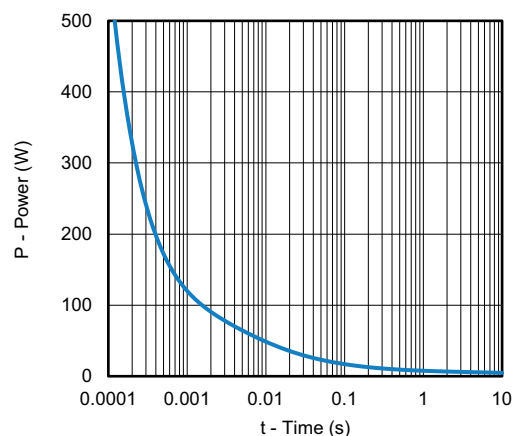
**Source-Drain Diode Forward Voltage**



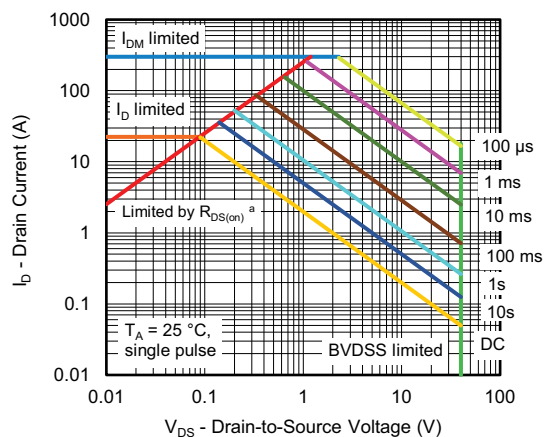
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



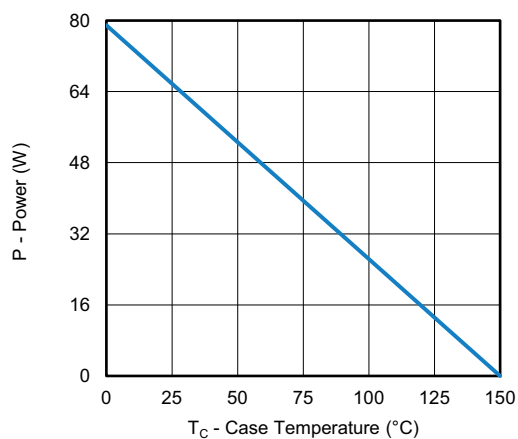
**Safe Operating Area**

**Note**

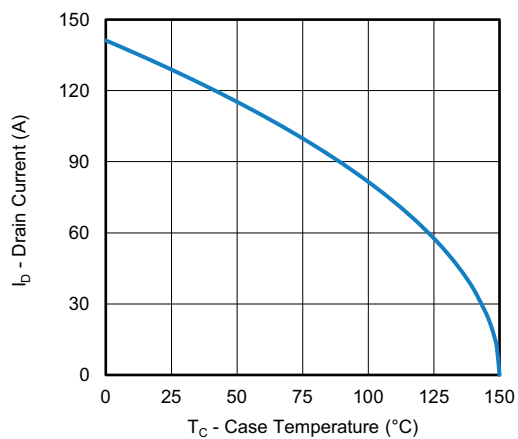
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



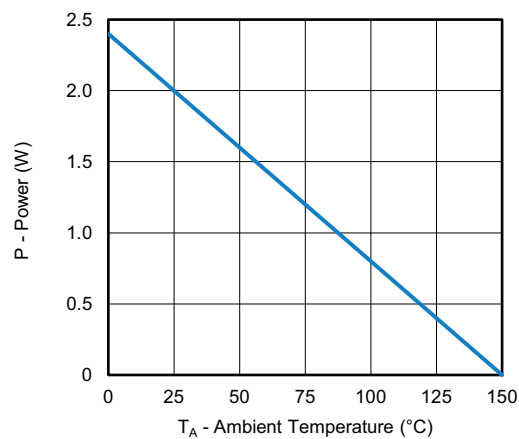
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Power, Junction-to-Case**



**Current Derating <sup>a</sup>**



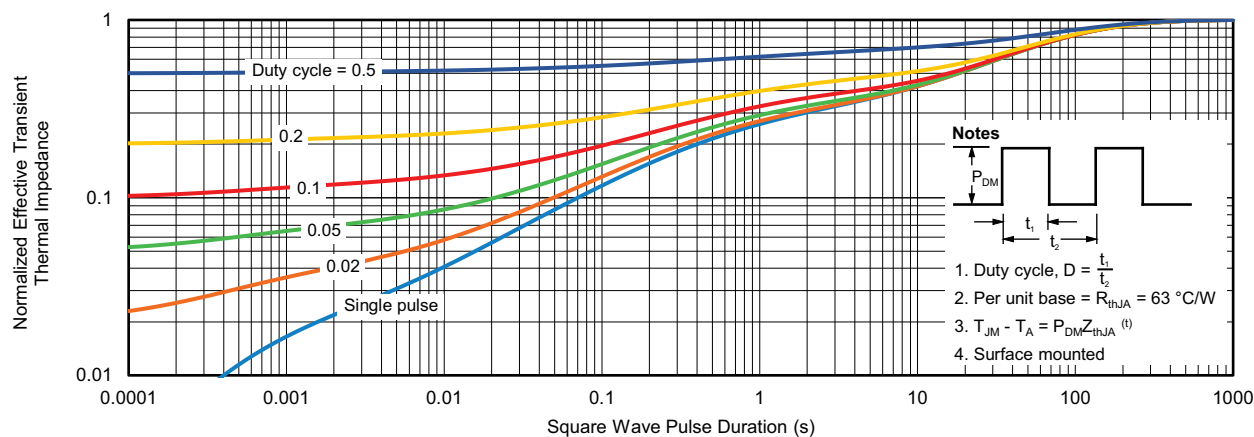
**Power, Junction-to-Ambient**

**Note**

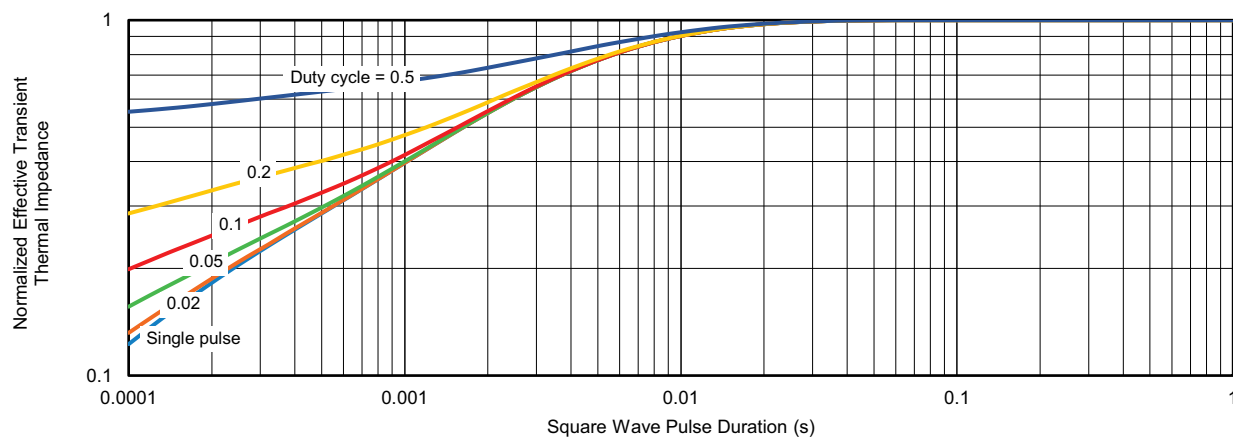
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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