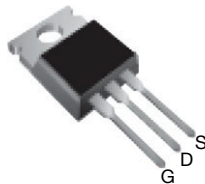


Power MOSFET

TO-220AB

N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.55
Q_g (Max.) (nC)	36	
Q_{gs} (nC)	9.9	
Q_{gd} (nC)	16	
Configuration	Single	

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche, and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback Xfmr. reset
- Single transistor forward Xfmr. reset (both for US line input only)

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF740APbF
Lead (Pb)-free and halogen-free	IRF740APbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	400	V
Gate-source voltage			V _{GS}	± 30	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	I _D	10	A
		T _C = 100 °C		6.3	
Pulsed drain current ^a			I _{DM}	40	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy ^b			E _{AS}	630	mJ
Repetitive avalanche current ^a			I _{AR}	10	A
Repetitive avalanche energy ^a			E _{AR}	12.5	mJ
Maximum power dissipation	T _C = 25 °C		P _D	125	W
Peak diode recovery dV/dt ^c			dV/dt	5.9	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	- 55 to + 150	°C
Soldering recommendations (peak temperature) ^d	For 10 s			300 ^d	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 12.6\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 10\text{ A}$ (see fig. 12)
- $I_{SD} \leq 10\text{ A}$, $dV/dt \leq 330\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

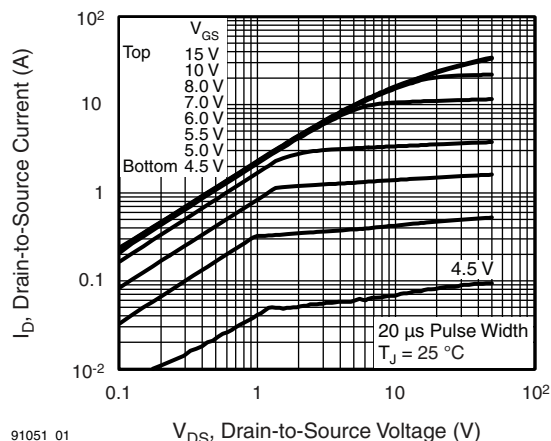
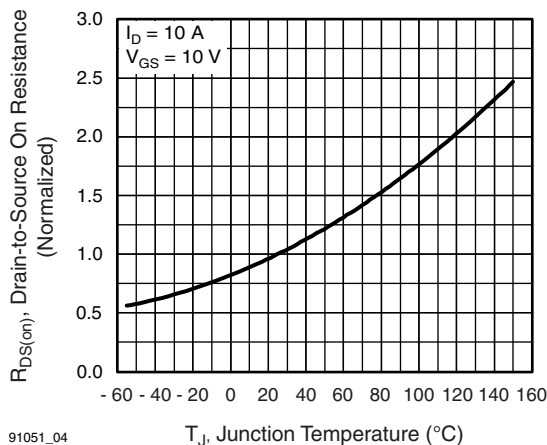
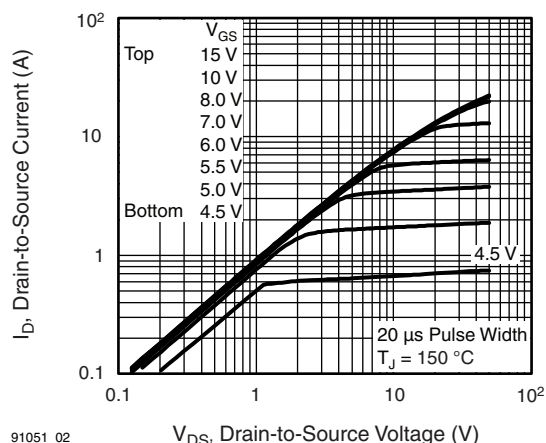
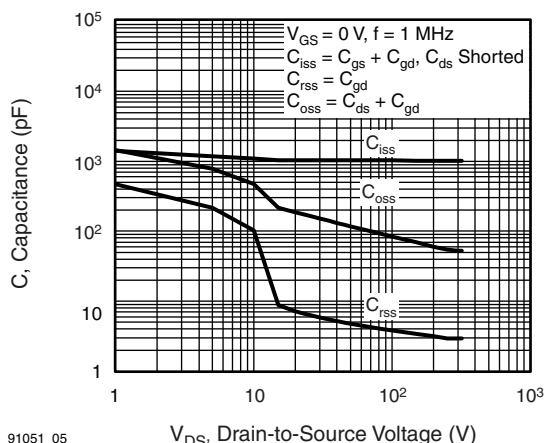
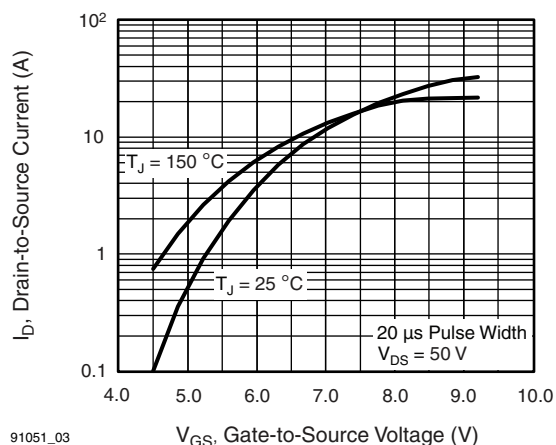
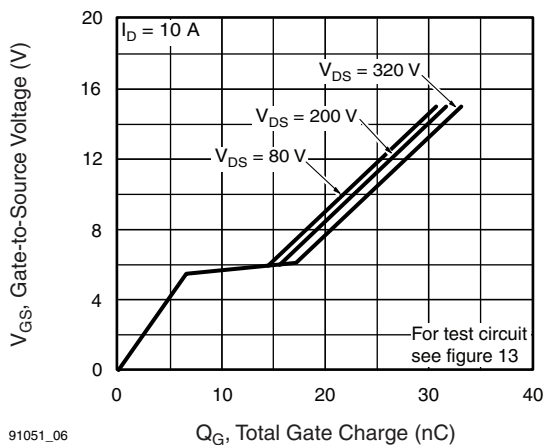
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

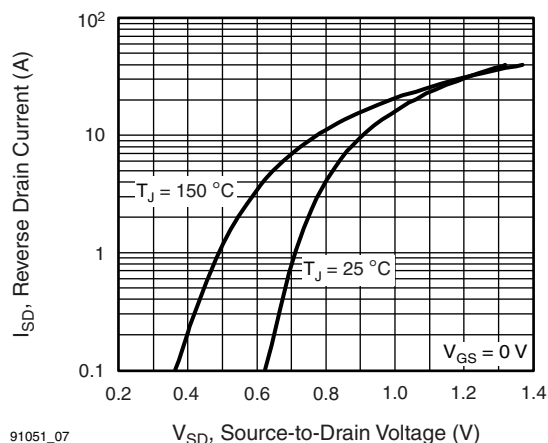
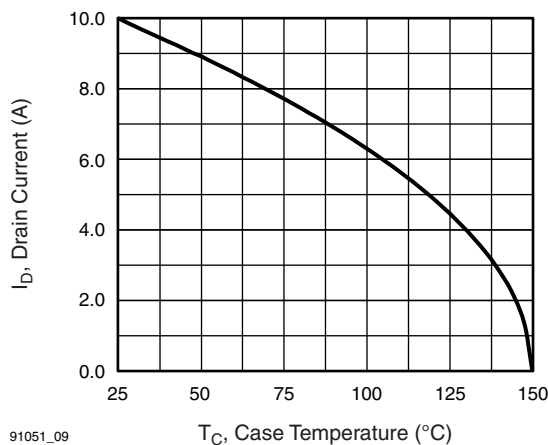
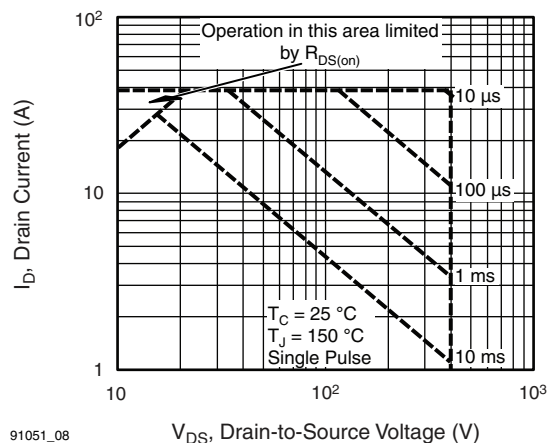
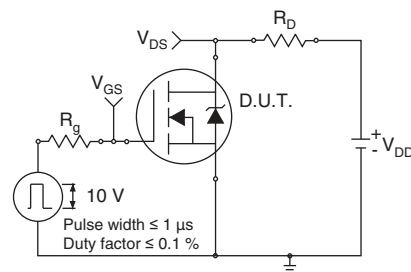
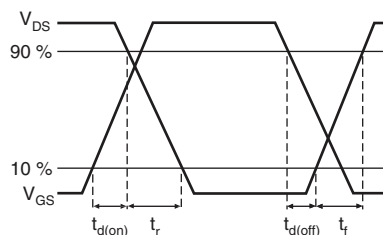
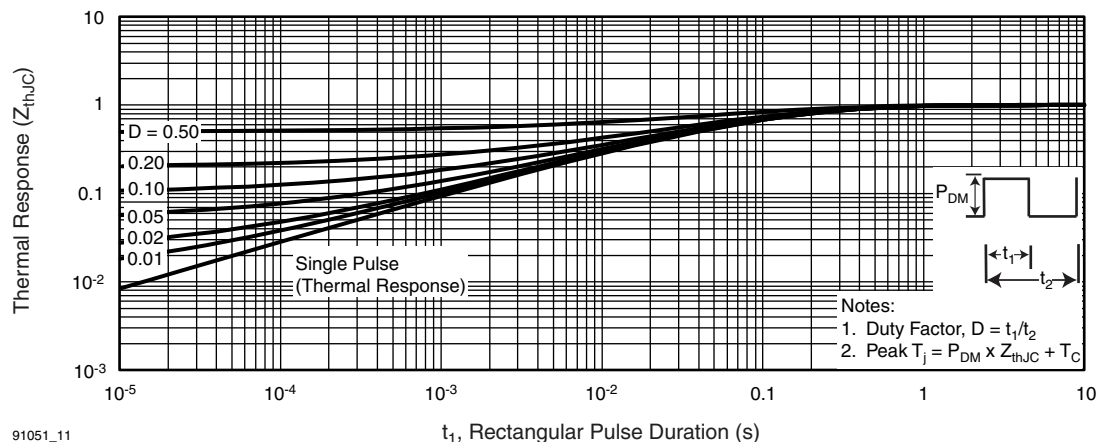
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		400	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.48	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6.0 A ^b	-	-	0.55	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 6.0 A ^b		4.9	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1030	-	pF
Output capacitance	C _{oss}			-	170	-	
Reverse transfer capacitance	C _{rss}			-	7.7	-	
Output capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = 1.0 V, f = 1.0 MHz		-	1490	-	
		V _{GS} = 0 V, V _{DS} = 320 V, f = 1.0 MHz		-	52	-	
Effective output capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = 0 V to 320 V		-	61	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 10 A, V _{DS} = 320 V, see fig. 6 and 13 ^b	-	-	36	nC
Gate-source charge	Q _{gs}			-	-	9.9	
Gate-drain charge	Q _{gd}			-	-	16	
Turn-on delay time	t _{d(on)}	V _{DD} = 200 V, I _D = 10 A, R _g = 10 Ω, R _D = 19.5 Ω, see fig. 10 ^b		-	10	-	ns
Rise time	t _r			-	35	-	
Turn-off delay time	t _{d(off)}			-	24	-	
Fall time	t _f			-	22	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10	A
Pulsed diode forward current ^a	I _{SM}			-	-	40	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 10 A, dI/dt = 100 A/μs ^b		-	240	360	ns
Body diode reverse recovery charge	Q _{rr}			-	1.9	2.9	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

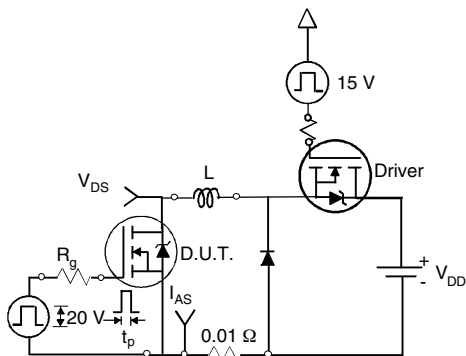
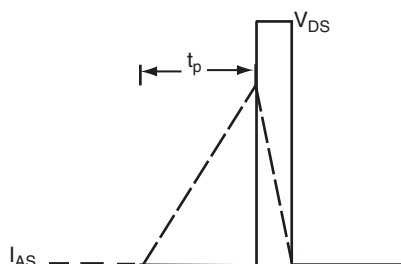
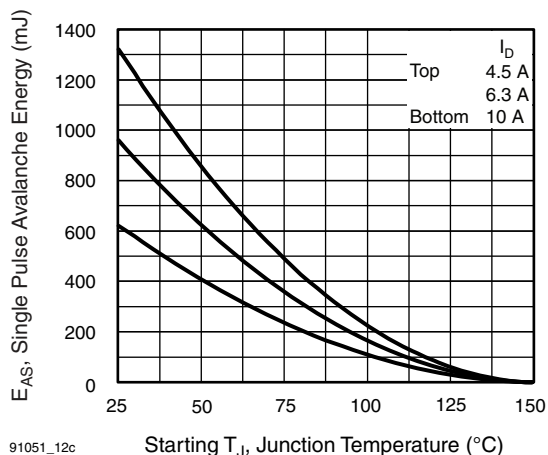
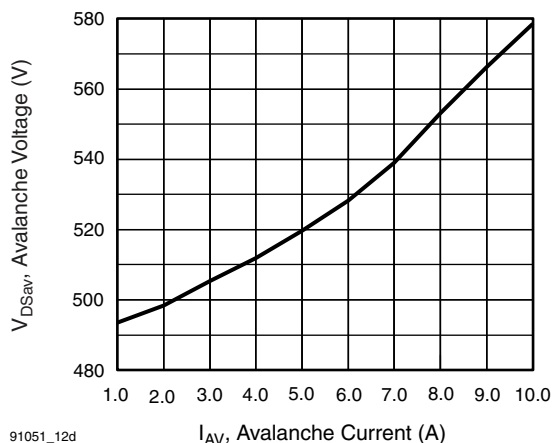
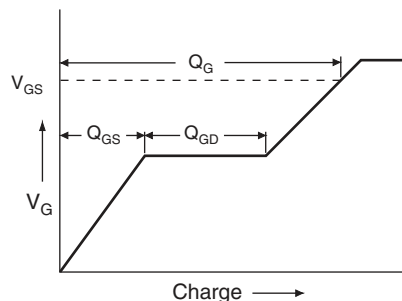
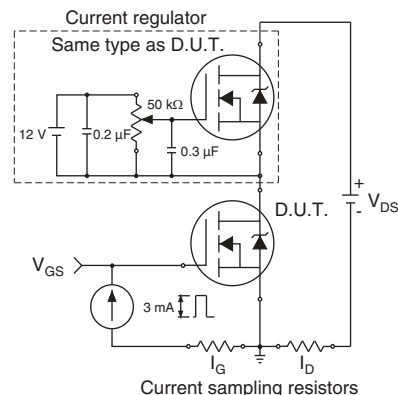
Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

Fig. 3 - Normalized On-Resistance vs. Temperature

Fig. 1 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 2 - Typical Transfer Characteristics

Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 6 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Drain Current vs. Case Temperature

Fig. 7 - Maximum Safe Operating Area

Fig. 9 - Switching Time Test Circuit

Fig. 10 - Switching Time Waveforms


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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12 - Unclamped Inductive Test Circuit

Fig. 13 - Unclamped Inductive Waveforms

Fig. 14 - Maximum Avalanche Energy vs. Drain Current

Fig. 15 - Typical Drain-to-Source Voltage vs. Avalanche Current

Fig. 16 - Basic Gate Charge Waveform

Fig. 17 - Gate Charge Test Circuit

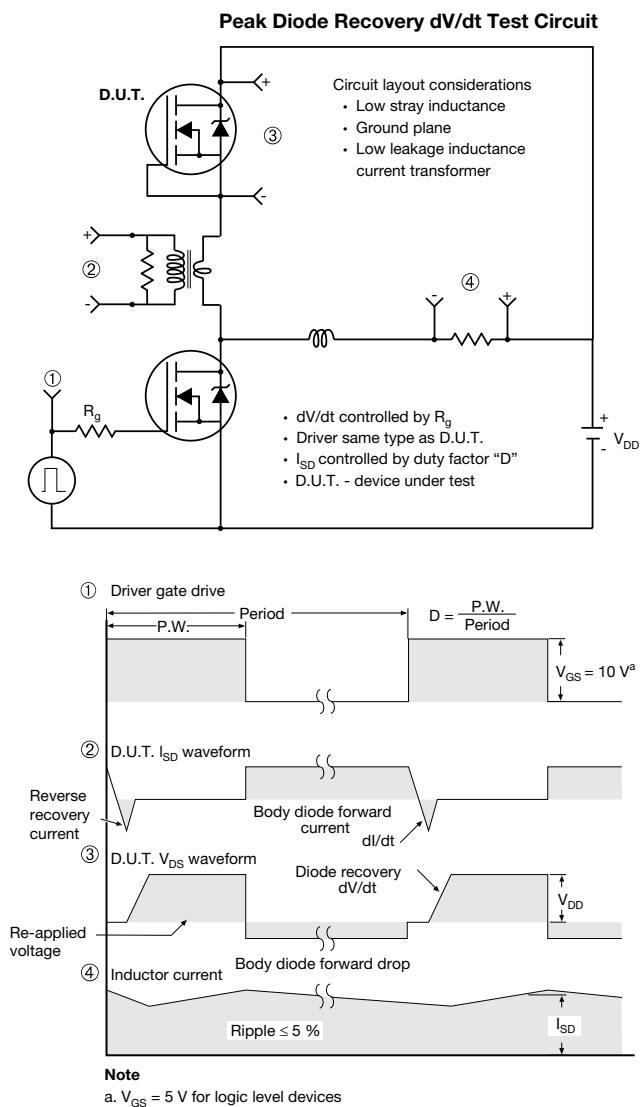


Fig. 18 - For N-Channel

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