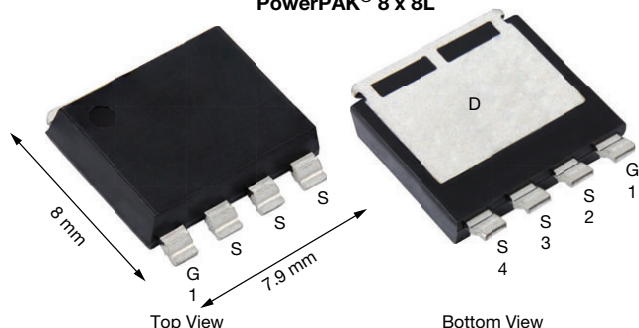


N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L



FEATURES

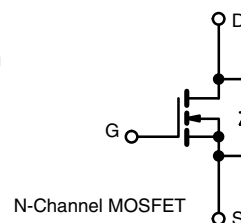
- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device
- Optimized Q_g , Q_{gd} , and Q_{gd}/Q_{gs} ratio reduces switching related power loss
- Up to 200 A maximum continuous drain current
- 50 % smaller footprint than D²PAK (TO-263)
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



PRODUCT SUMMARY

V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0028
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0036
Q_g typ. (nC)	106
I_D (A) ^a	225
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SiJH112E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	225
		$T_C = 70$ °C	188
		$T_A = 25$ °C	23 ^b
		$T_A = 70$ °C	19 ^b
Pulsed drain current ($t = 100$ μ s)	I_{DM}	300	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	303
		$T_A = 25$ °C	3 ^b
Single pulse avalanche current	I_{AS}	60	
Single pulse avalanche energy	E_{AS}	180	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	333
		$T_C = 70$ °C	233
		$T_A = 25$ °C	3.3 ^b
		$T_A = 70$ °C	2.3 ^b
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	36	45	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.36	0.45	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

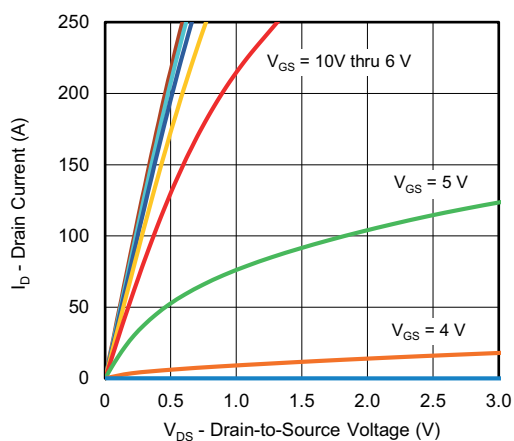
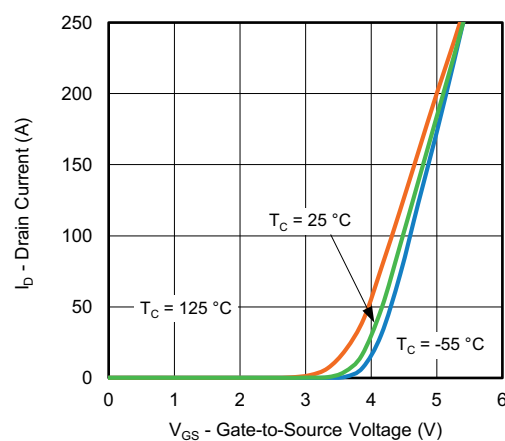
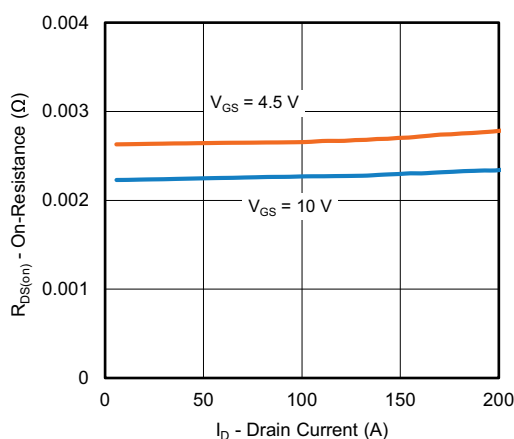
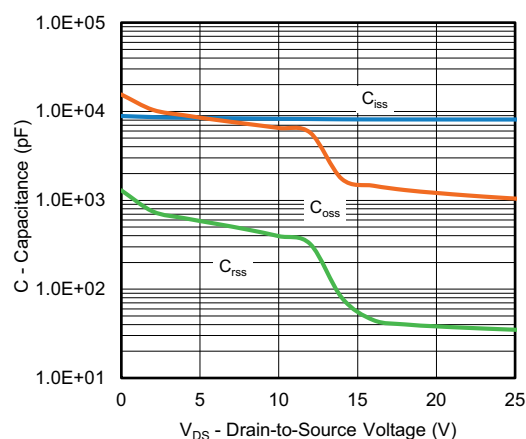
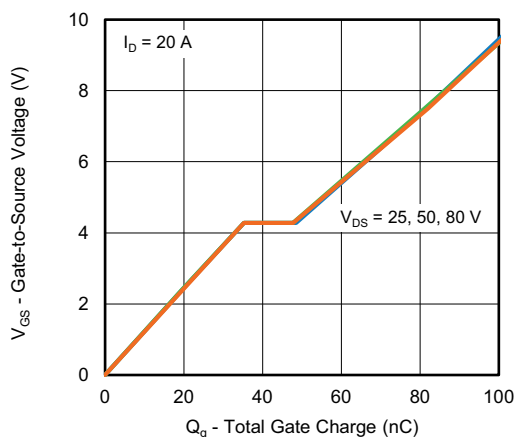
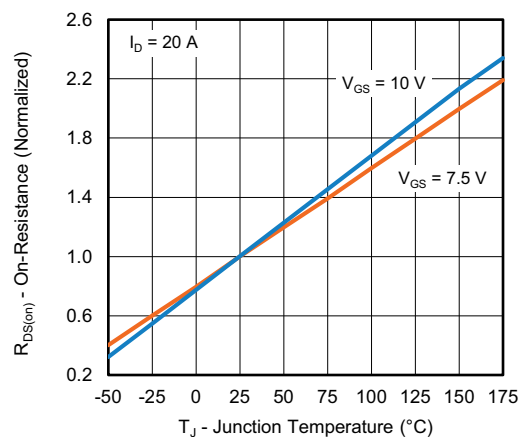


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	70	-	mV/°C	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-8.9	-		
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 μA	2	-	4	V	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20	-	-	100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} =0 V	-	-	1	μA	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15		
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} =10 V	40	-	-	A	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.0023	0.0028	Ω	
		V _{GS} = 7.5 V, I _D = 20 A	-	0.0026	0.0036		
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 50 A	-	135	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	8050	-	pF	
Output capacitance	C _{oss}		-	730	-		
Reverse transfer capacitance	C _{rss}		-	29	-		
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	-	106	160	nC	
		V _{DS} = 20 V, V _{GS} = 7.5 V, I _D =20 A	-	81	122		
Gate-source charge	Q _{gs}		-	36	-		
Gate-drain charge	Q _{gd}		-	23	-		
Gate resistance	R _g	f = 1 MHz	0.3	1.3	2.6	Ω	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 10 Ω, I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	-	21	40	ns	
Rise time	t _r		-	29	60		
Turn-off delay time	t _{d(off)}		-	44	90		
Fall time	t _f		-	11	20		
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 10 Ω, I _D ≅ 5 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	29	60		
Rise time	t _r		-	87	175		
Turn-off delay time	t _{d(off)}		-	40	80		
Fall time	t _f		-	13	25		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	303	A	
Pulse diode forward current	I _{SM}		-	-	300		
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.7	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	-	65	130	ns	
Body diode reverse recovery charge	Q _{rr}		-	150	300	nC	
Reverse recovery fall time	t _a		-	65	-	ns	
Reverse recovery rise time	t _b		-	20	-		

Notes

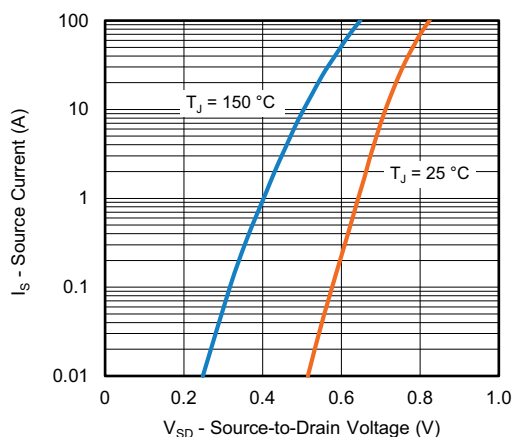
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

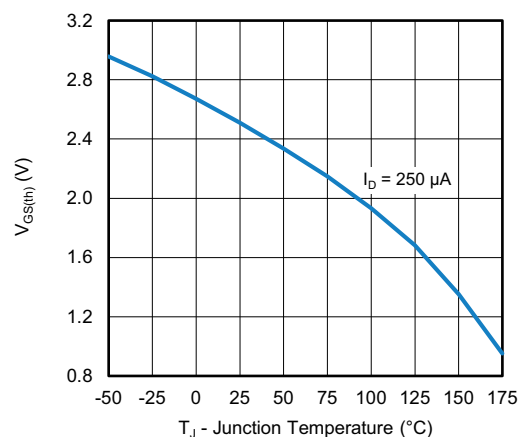
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



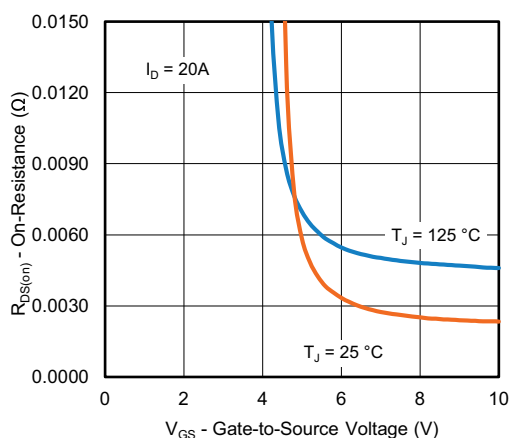
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



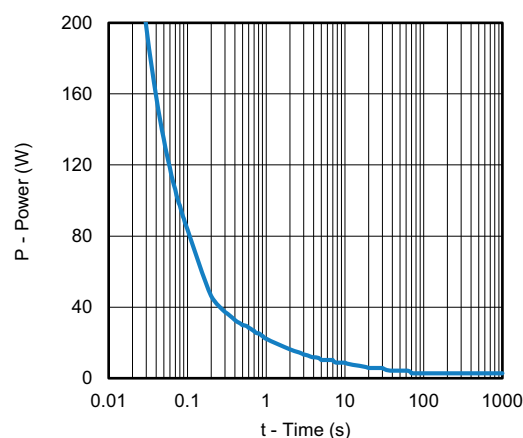
Source-Drain Diode Forward Voltage



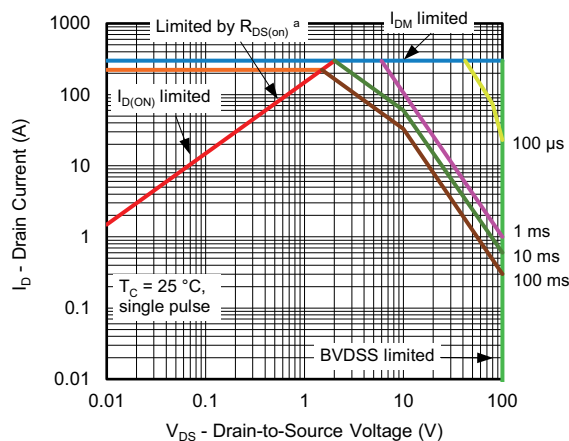
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



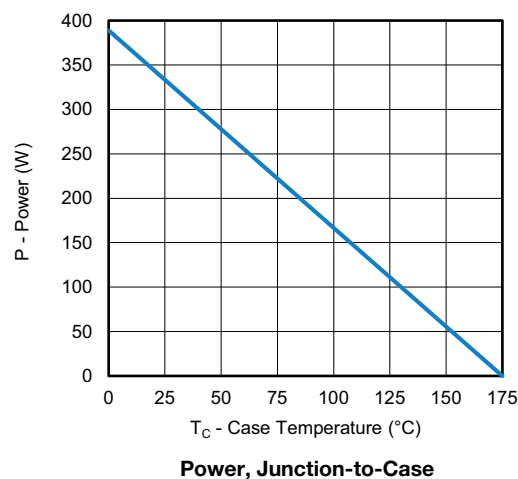
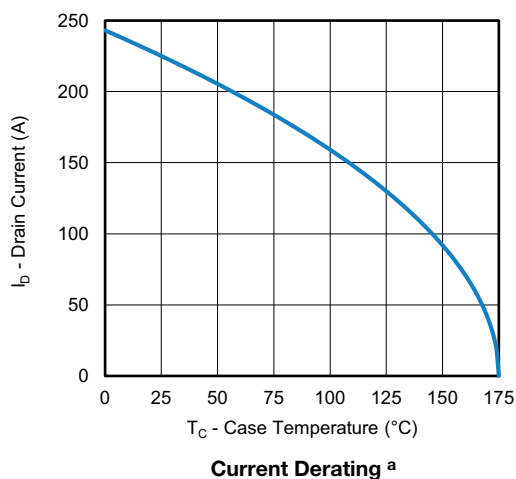
Safe Operating Area, Junction-to-Ambient

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

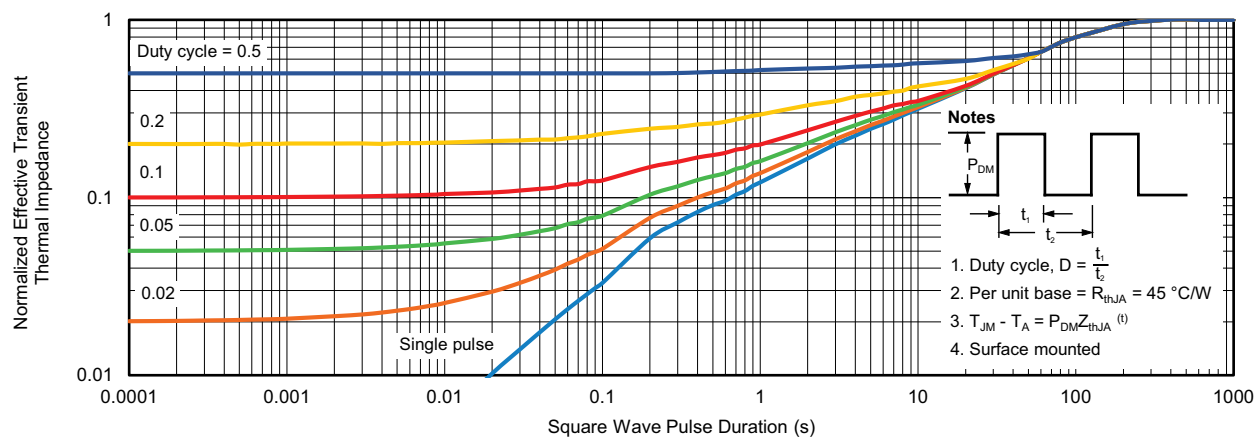


Note

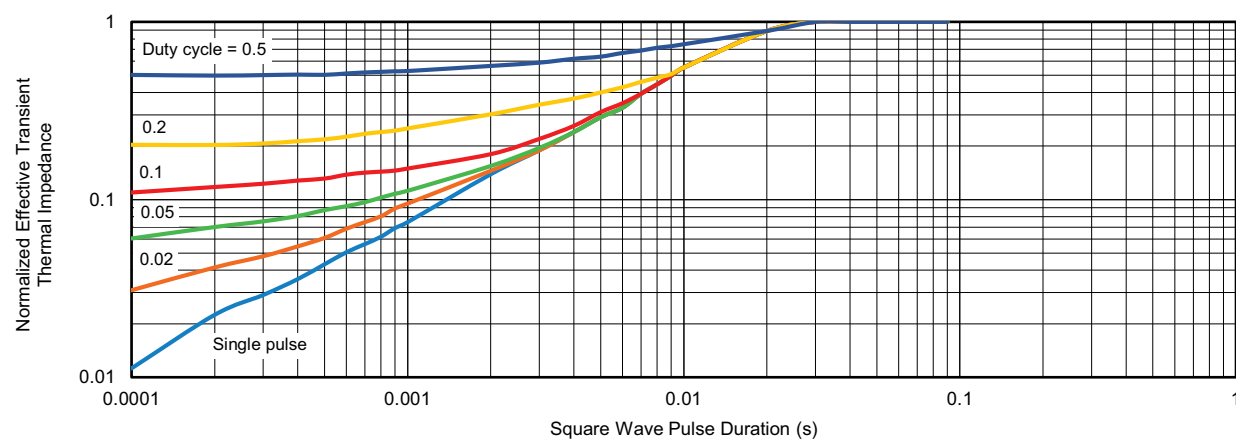
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



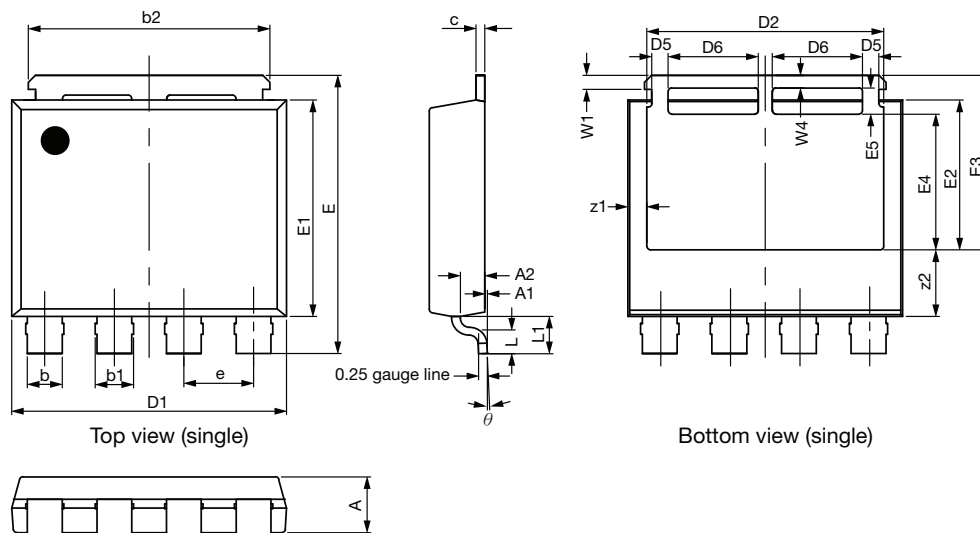
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78023.

PowerPAK® 8 x 8L BWL Case Outline 2

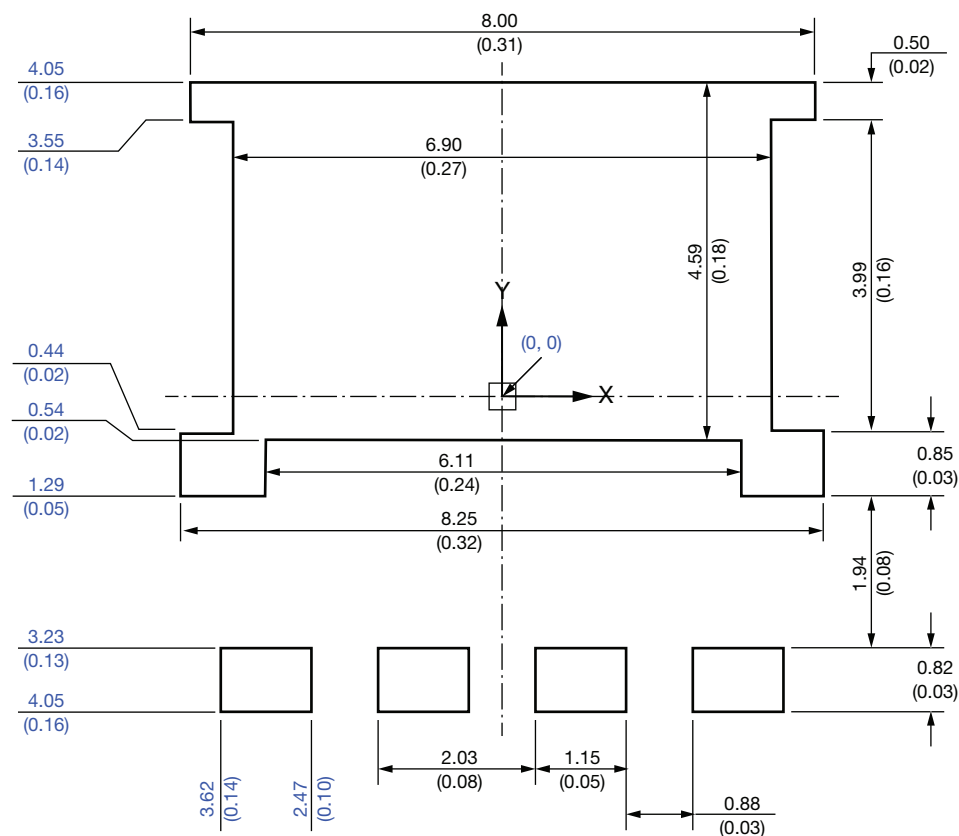


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°
ECN: S19-0643-Rev. B, 05-Aug-2019 DWG: 6073						

Note

- Millimeter will govern

Recommended Minimum PADS for PowerPAK® 8 x 8L Single



Dimensions in millimeters (inches)

Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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