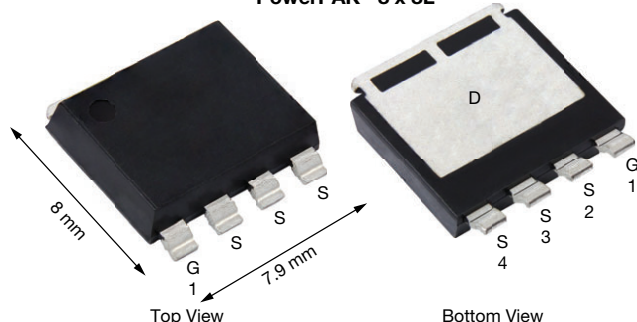


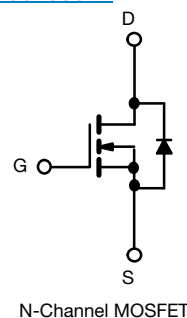
# Automotive N-Channel 30 V (D-S) 175 °C MOSFET

**PowerPAK® 8 x 8L**


## FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


## PRODUCT SUMMARY

$V_{DS}$ (V)	30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.00052
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0007
$I_D$ (A)	445
Configuration	Single
Package	PowerPAK 8 x 8L

## ORDERING INFORMATION

Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SQJQ130EL (for detailed order number please see <a href="http://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Continuous source current (diode conduction)	$I_S$	545	
Pulsed drain current <sup>b</sup>	$I_{DM}$	445	
Single pulse avalanche current	$I_{AS}$	86	
Single pulse avalanche energy	$E_{AS}$	374	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 125$ °C	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	44	°C/W
Junction-to-case (drain)	$R_{thJC}$	0.25	

### Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

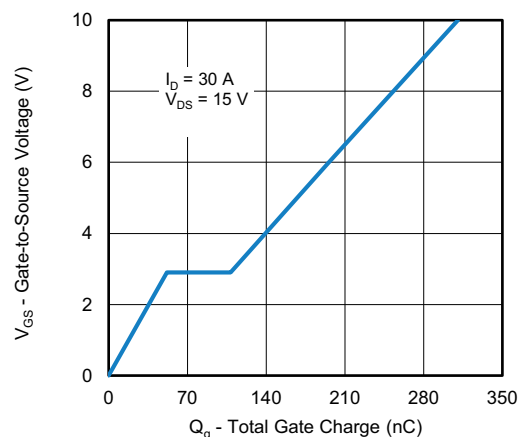
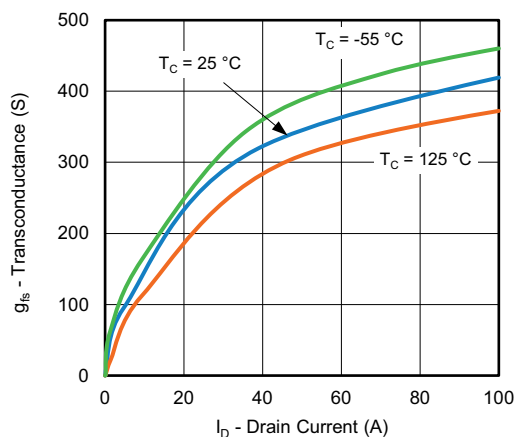
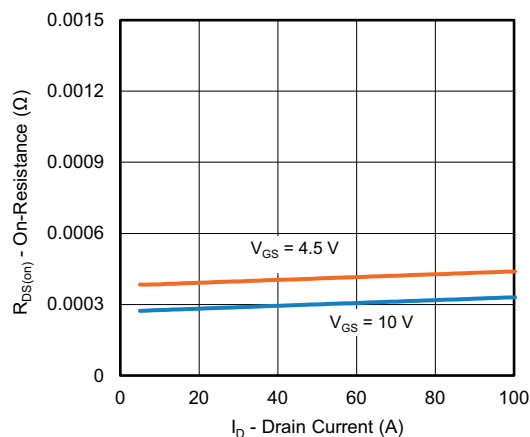
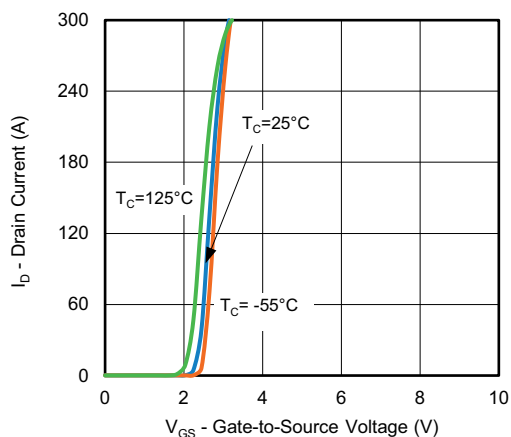
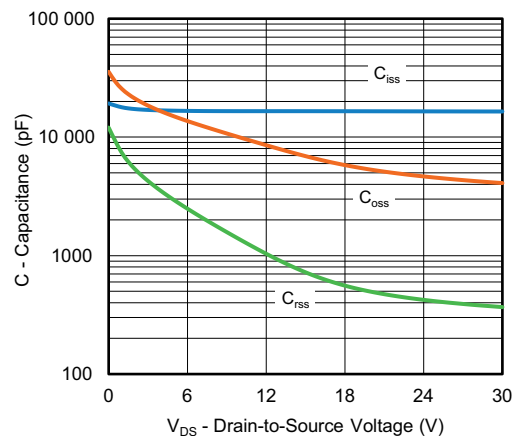
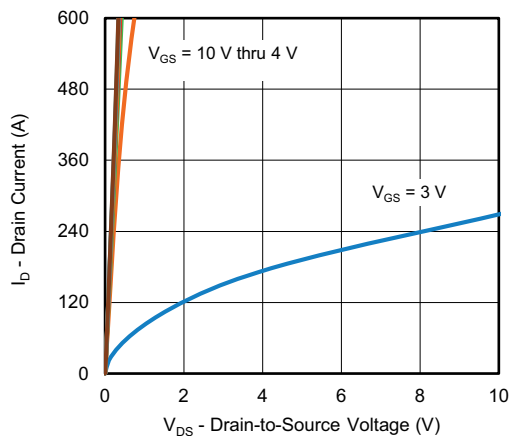


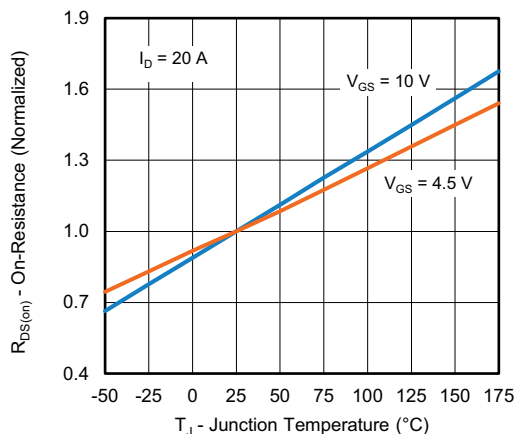
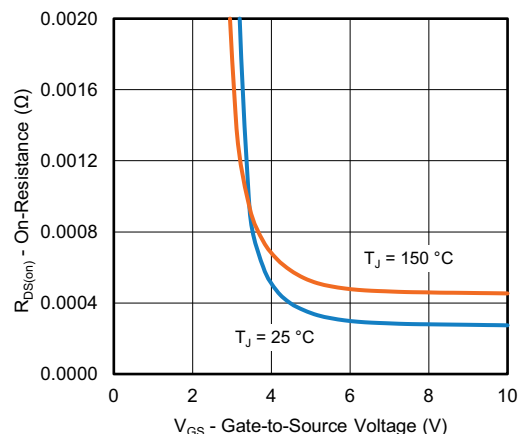
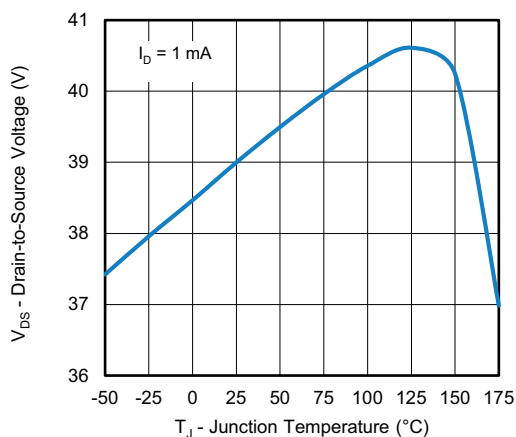
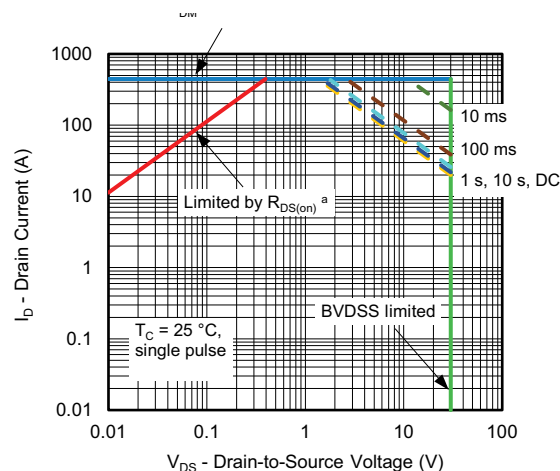
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		30	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 125 °C	-	-	200	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 175 °C	-	-	330	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.00045	0.00052	Ω
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	-	0.0006	0.0007	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0008	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0009	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 60 A		-	360	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	16 675	23 345	pF
Output capacitance	C <sub>oss</sub>			-	6850	9560	
Reverse transfer capacitance	C <sub>rss</sub>			-	715	1000	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	310	455	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	53	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	56	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.9	1.9	2.9	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.5 Ω I <sub>D</sub> ≅ 30 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	22	33	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	30	45	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	109	164	
Fall time <sup>c</sup>	t <sub>f</sub>			-	57	86	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Reverse recovery time	t <sub>rr</sub>	V <sub>DD</sub> = 24 V, I <sub>FM</sub> = 20 A, di/dt = 100 A/μs		-	40	-	ns
	t <sub>a</sub>			-	44	-	
	t <sub>b</sub>			-	83	166	
Reverse recovery charge	Q <sub>rr</sub>			-	156	312	nC
Reverse recovery current	I <sub>RM</sub>			-	-	3.4	A
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	1600	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0		-	0.8	1.1	V

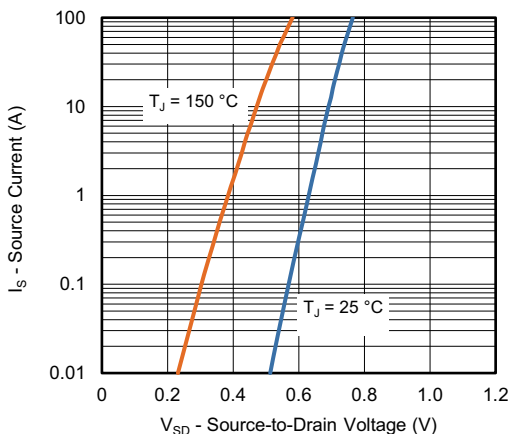
**Notes**

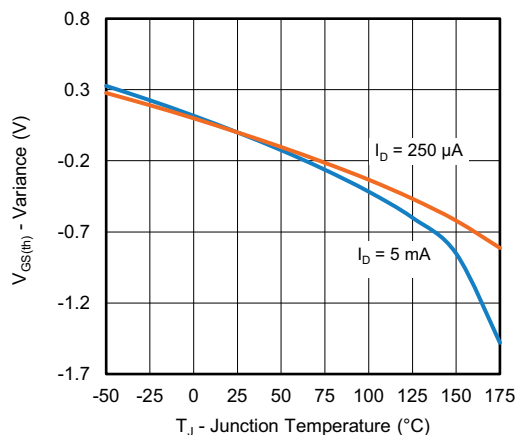
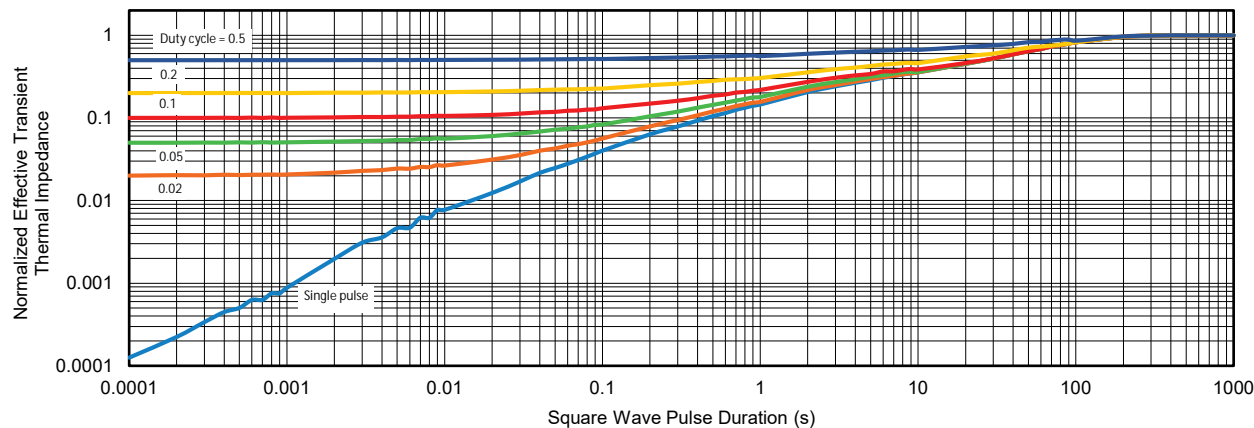
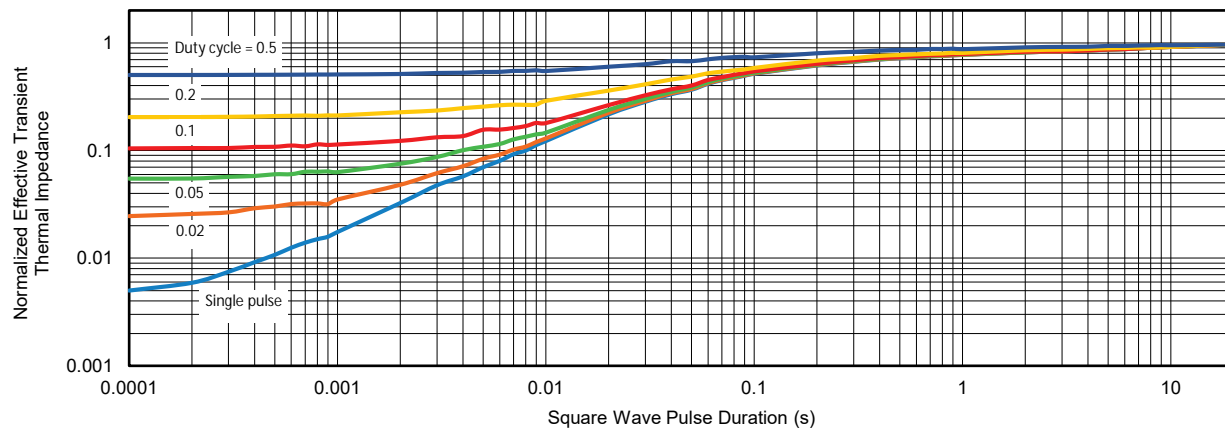
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)


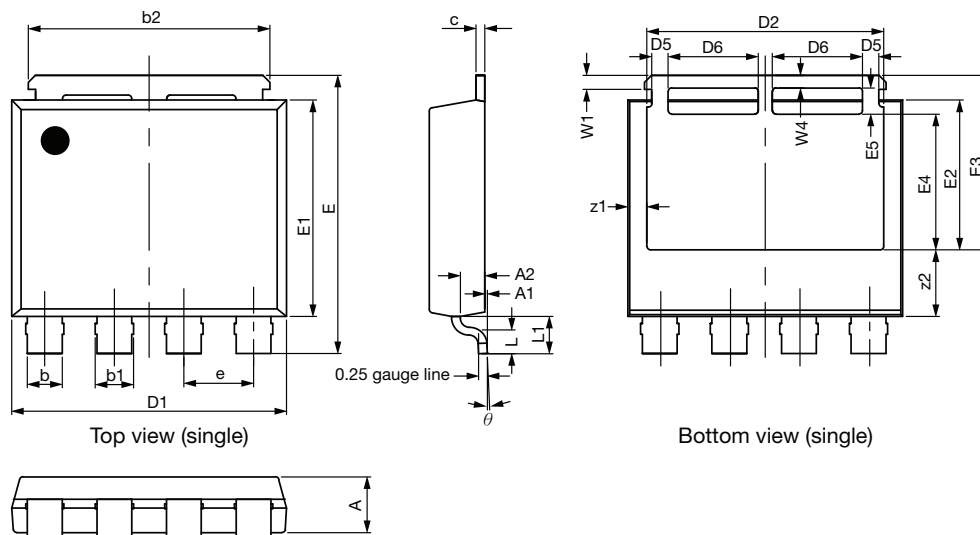
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Fig. 7 - On-Resistance vs. Junction Temperature**

**Fig. 10 - On-Resistance vs. Gate-to-Source Voltage**

**Fig. 8 - Drain Source Breakdown vs. Junction Temperature**

**Fig. 11 - Safe Operating Area**
**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Fig. 9 - Source Drain Diode Forward Voltage**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Fig. 12 - Threshold Voltage**

**Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Fig. 14 - Normalized Thermal Transient Impedance, Junction-to-Case**

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## PowerPAK® 8 x 8L BWL Case Outline 2



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°

ECN: S19-0643-Rev. B, 05-Aug-2019  
DWG: 6073

### Note

- Millimeter will govern



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