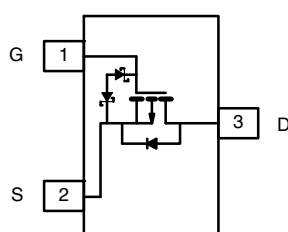


# P-Channel 20 V (D-S) MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 20	0.0320 at $V_{GS} = - 4.5$ V	- 5.9	13.8 nC
	0.0410 at $V_{GS} = - 2.5$ V	- 5.2	
	0.0675 at $V_{GS} = - 1.8$ V	- 4.3	

TO-236  
(SOT-23)



Top View

Si2365EDS (H5)\*

\* Marking Code

### Ordering Information:

Si2365EDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

## FEATURES

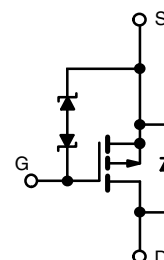
- TrenchFET® Power MOSFET
- 100 %  $R_g$  Tested
- Built-in ESD Protection
- Typical ESD Performance 3000 V
- Material categorization:  
For definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Power Management for Portable and Consumer
- Load Switches
- DC/DC Converters



P-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current ( $t = 300$ $\mu$ s)	$I_{DM}$	- 20	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	- 1 <sup>b, c</sup>
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	100	130	°C/W
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	60	75	

Notes:

a.  $T_C = 25$  °C.

b. Surface mounted on 1" x 1" FR4 board.

c.  $t = 5$  s.

d. Maximum under steady state conditions is 175 °C/W.

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 20			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 14		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			2.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 0.4		- 1	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 10	μA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 4.5 V			± 1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	- 15			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 4 A		0.0265	0.0320	Ω
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 4 A		0.0340	0.0410	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 2 A		0.0465	0.0675	
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 4.5 A		23.8	36	nC
		V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 4.5 A		13.8	21	
Gate-Source Charge	Q <sub>gs</sub>			1.9		
Gate-Drain Charge	Q <sub>gd</sub>			3		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	2.2	11	22	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 2.8 Ω I <sub>D</sub> ≅ - 3.6 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		22	33	ns
Rise Time	t <sub>r</sub>			21	32	
Turn-Off Delay Time	t <sub>d(off)</sub>			62	93	
Fall Time	t <sub>f</sub>			14	21	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 2.8 Ω I <sub>D</sub> ≅ - 3.6 A, V <sub>GEN</sub> = - 8 V, R <sub>g</sub> = 1 Ω		9	18	
Rise Time	t <sub>r</sub>			6	12	
Turn-Off Delay Time	t <sub>d(off)</sub>			65	98	
Fall Time	t <sub>f</sub>			15	23	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 1.4	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 20	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3.6 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 3.6 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		13	20	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			5	10	nC
Reverse Recovery Fall Time	t <sub>a</sub>			8		ns
Reverse Recovery Rise Time	t <sub>b</sub>			5		

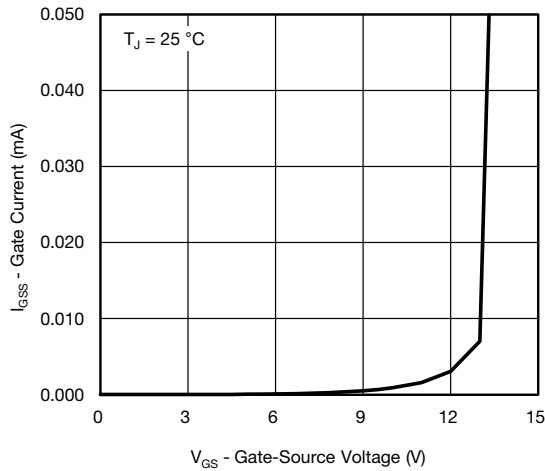
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

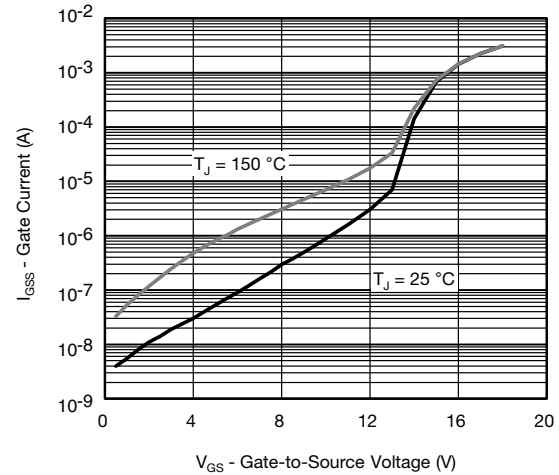
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

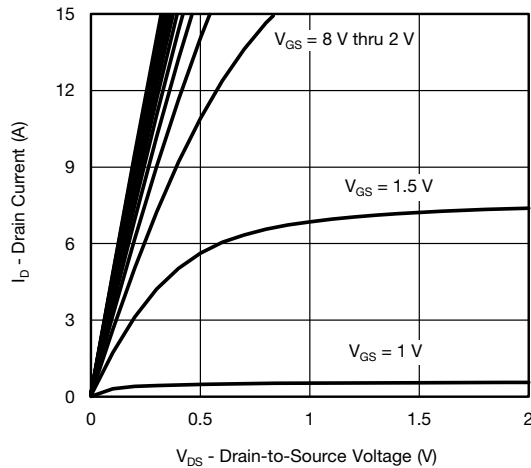
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



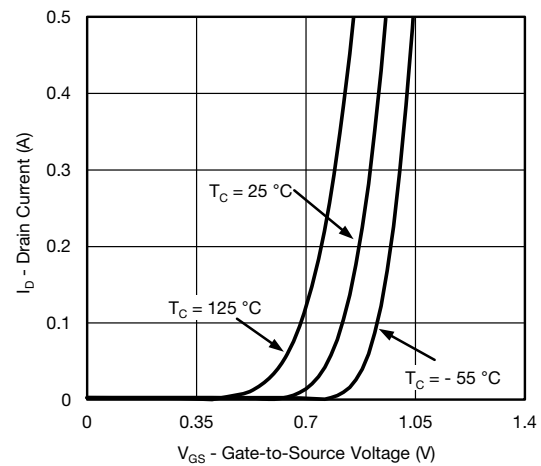
Gate Current vs. Gate-Source Voltage



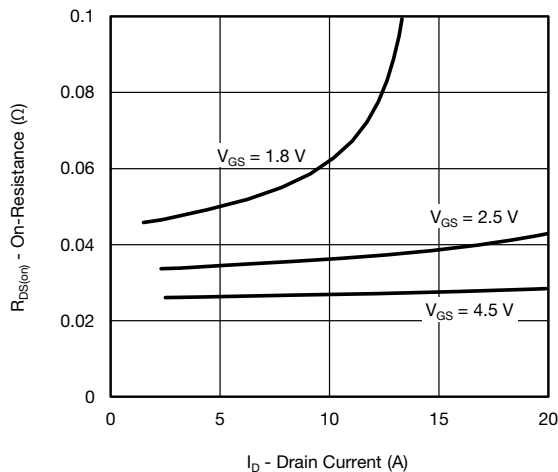
Gate Current vs. Gate-Source Voltage



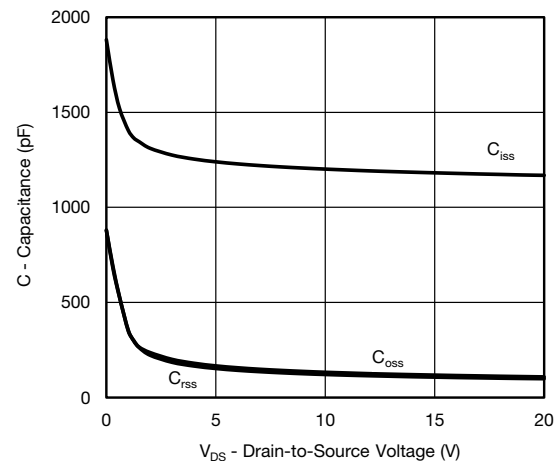
Output Characteristics



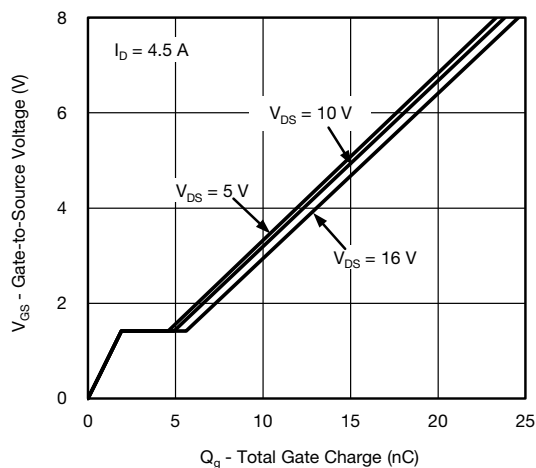
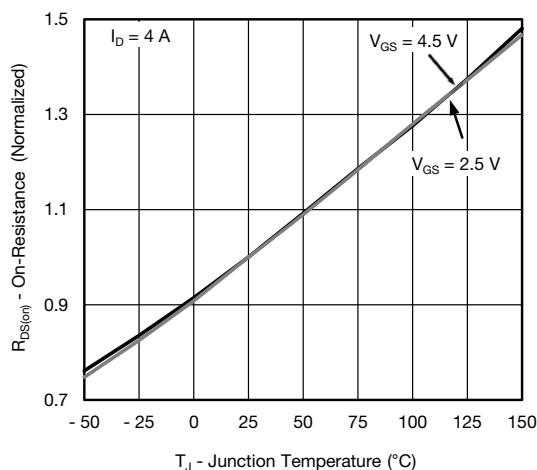
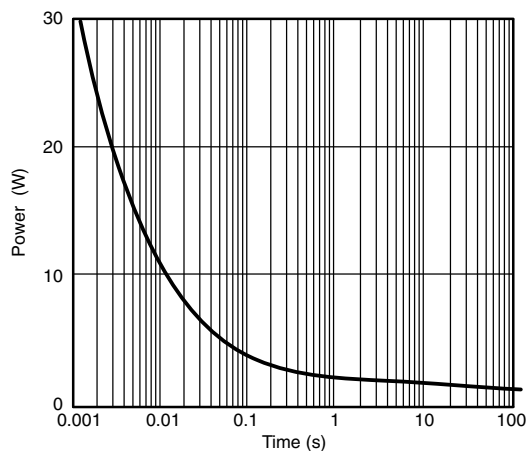
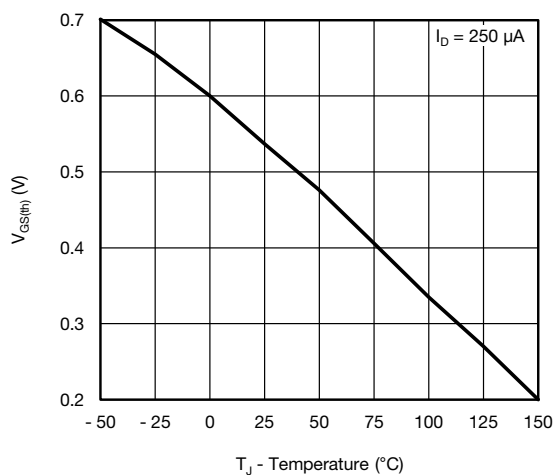
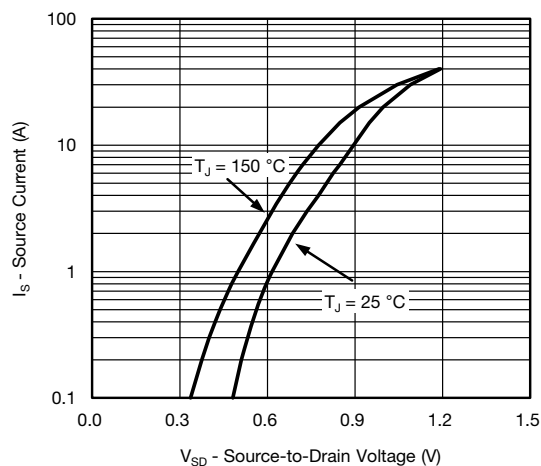
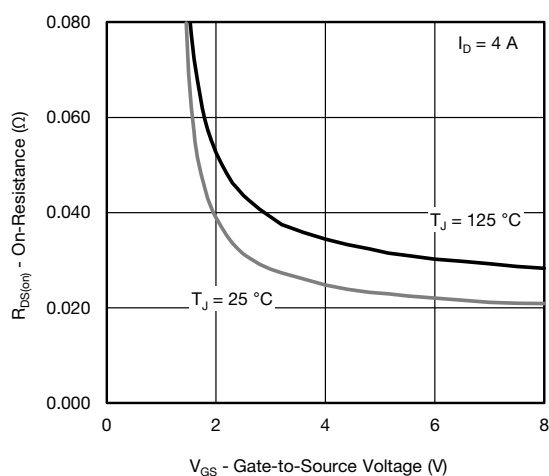
Transfer Characteristics



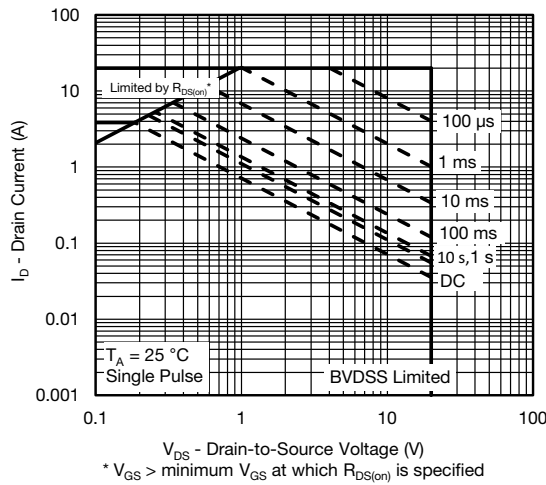
On-Resistance vs. Drain Current



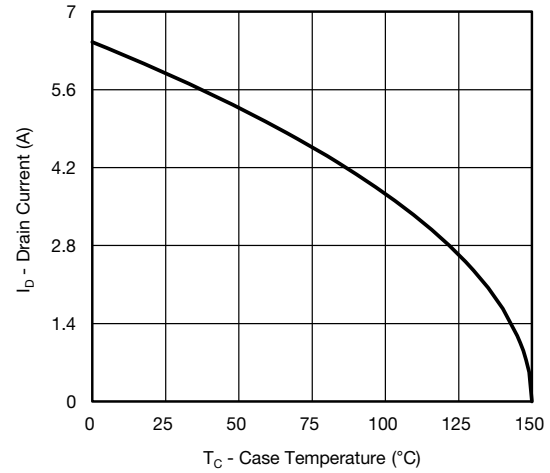
Capacitance

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Gate Charge****On-Resistance vs. Junction Temperature****Single Pulse Power, Junction-to-Ambient****Threshold Voltage****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage**

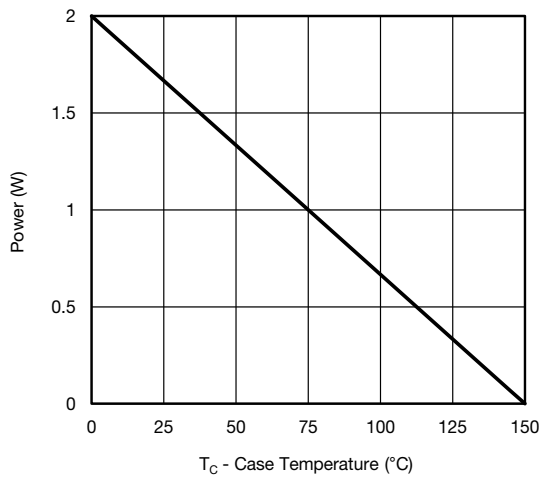
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



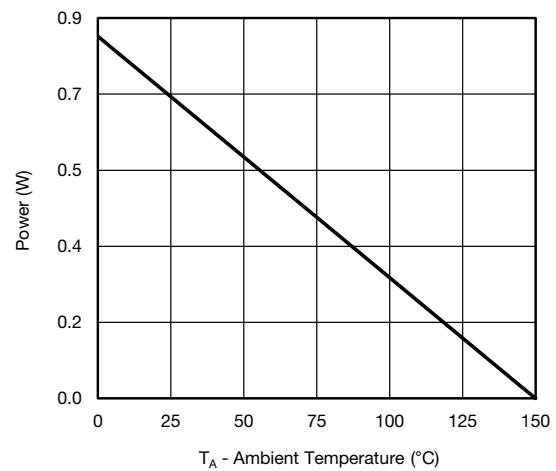
**Safe Operating Area, Junction-to-Ambient**



**Current Derating\***

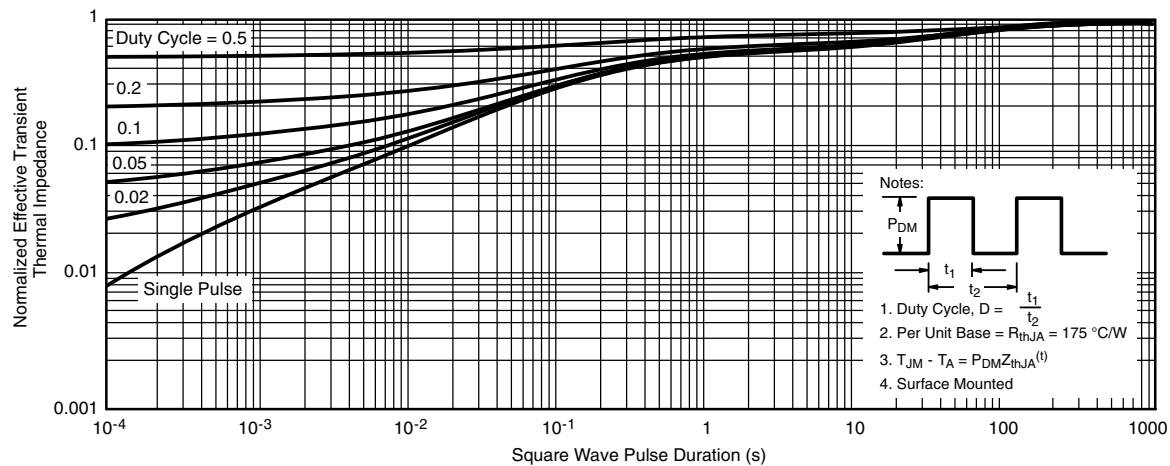
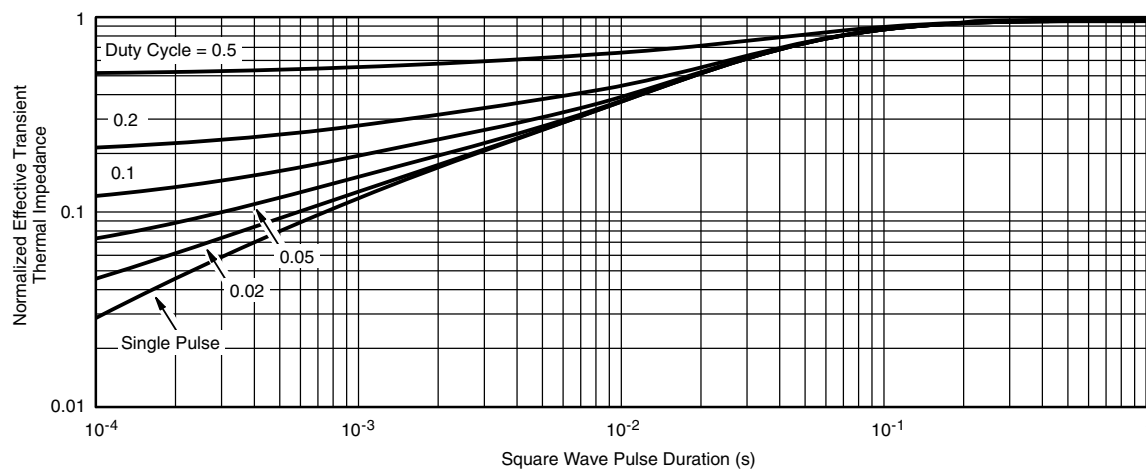


**Power Junction-to-Case**



**Power Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

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## SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A <sub>1</sub>	0.01	0.10	0.0004	0.004
A <sub>2</sub>	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E <sub>1</sub>	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e <sub>1</sub>	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L <sub>1</sub>	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01 DWG: 5479				

## RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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