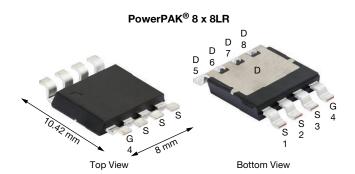


www.vishay.com

Vishay Siliconix

Automotive N-Channel 60 V (D-S) 175 °C MOSFET



FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Thin 1.6 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.00080			
I _D (A) ^e	363			
Configuration	Single			

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N-Channel MOSFET	o s

ORDERING INFORMATION	
Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ160ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	60	V		
Gate-source voltage		V _{GS}	± 20	V		
Continuous drain current e	T _C = 25 °C	- I _D	363			
	T _C = 125 °C		209			
Continuous source current (diode conduction)		I _S	194	Α		
Pulsed drain current ^a , e		I _{DM}	802			
Single pulse avalanche current	L = 0.1 mH	I _{AS}	80			
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	320	mJ		
Maximum power dissipation e	T _C = 25 °C	В	214	W		
	T _C = 125 °C	- P _D	71			
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C		
Soldering recommendations (peak temperature) ^c			260			

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount b	R_{thJA}	44	°C/W	
Junction-to-case (drain) ^d		R_{thJC}	0.7	C/VV	

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (www.vishay.com/doc?73257)
- d. As per JESD51-14
- e. Values based on RthJC and TC of 25 °C- Actual values achievable will be dependent on the thermal characteristics of the complete system



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		60	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2	2.8	3.5	V	
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
Zero gate voltage drain current		V _{GS} = 0 V	V _{DS} = 60 V	-	-	1		
	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 60 V, T _J = 175 °C	-	-	500		
On-state drain current ^a	I _{D(on)}	$V_{GS} = 10 \text{ V}$	$V_{DS} \ge 5 V$	50	-	-	Α	
		$V_{GS} = 10 \text{ V}$	I _D = 20 A	-	0.00056	0.00080		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}$	I _D = 20 A, T _J = 125 °C	-	-	0.0014	Ω	
		$V_{GS} = 10 \text{ V}$	I _D = 20 A, T _J = 175 °C	-	-	0.0017		
Forward transconductance b	9 _{fs}	V _{DS} = 15 V, I _D = 40 A		-	220	-	S	
Dynamic ^b								
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	10 944	15 322	pF	
Output capacitance	Coss			-	4486	6281		
Reverse transfer capacitance	C _{rss}			-	266	373		
Total gate charge ^c	Q_g			-	169	254		
Gate-source charge ^c	Q_{gs}	$V_{GS} = 10 \text{ V}$ $V_{DS} = 30 \text{ V}, I_D = 50 \text{ A}$	-	48	=	nC		
Gate-drain charge ^c	Q_{gd}			-	34		-	
Gate resistance	R_g	f = 1 MHz		0.4	1.6	3.2	Ω	
Turn-on delay time ^c	t _{d(on)}	$V_{DD} = 30 \text{ V, } R_L = 0.6 \Omega,$ $I_D \cong 50 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	20	30	- ns	
Rise time ^c	t _r			-	19	29		
Turn-off delay time ^c	t _{d(off)}			-	57	86		
Fall time ^c	t _f			-	18	27		
Source-Drain Diode Ratings and Charact	teristics ^b							
Pulsed current ^a	I _{SM}			-	-	802	Α	
Forward voltage	V_{SD}	I _F = 40 A, V _{GS} = 0 V		-	0.7	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 50 A, di/dt = 100 A/μs		-	86	172	ns	
Body diode reverse recovery charge	Q _{rr}			-	154	308	nC	
Reverse recovery fall time	t _a			-	49	-	ns	
Reverse recovery rise time	t _b			-	34	-		
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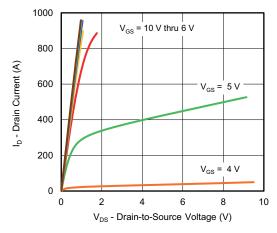
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

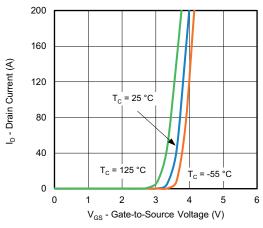
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



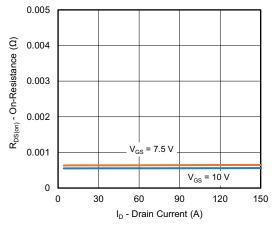
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



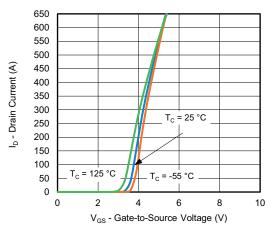
Output Characteristics



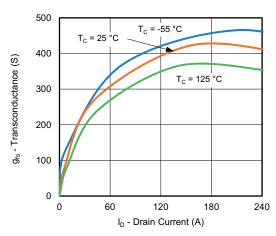
Transfer Characteristics



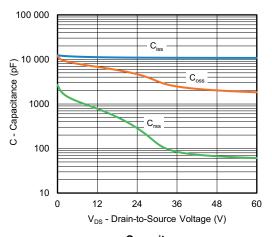
On-Resistance vs. Drain Current



Transfer Characteristics

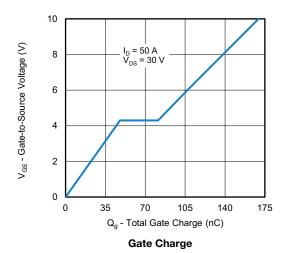


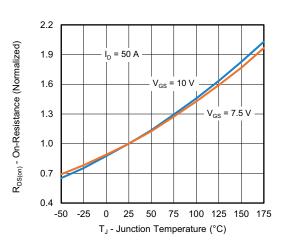
Transconductance



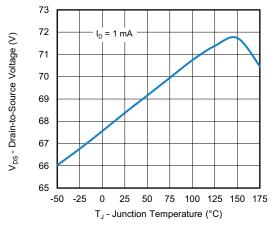


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

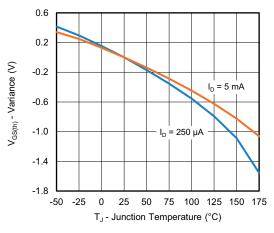




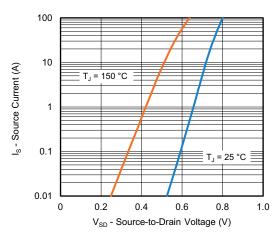
On-Resistance vs. Junction Temperature



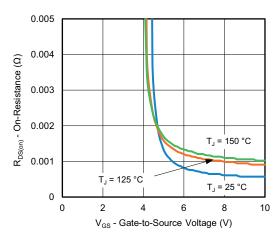
Drain Source Breakdown vs. Junction Temperature



Threshold Voltage



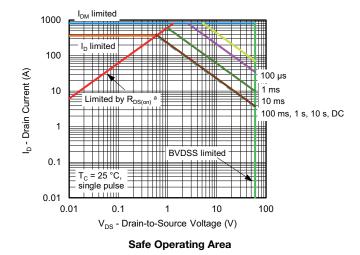
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

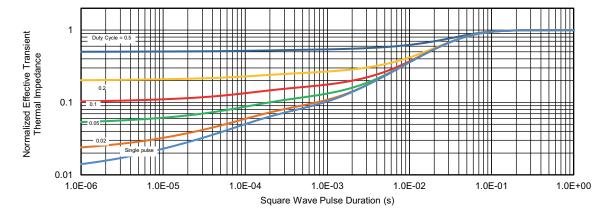


THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)

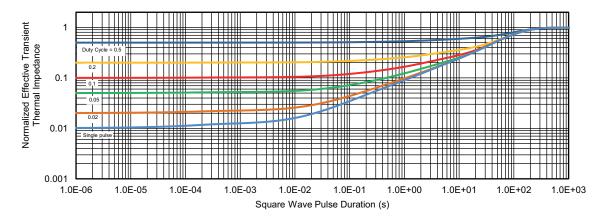


Note

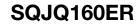
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



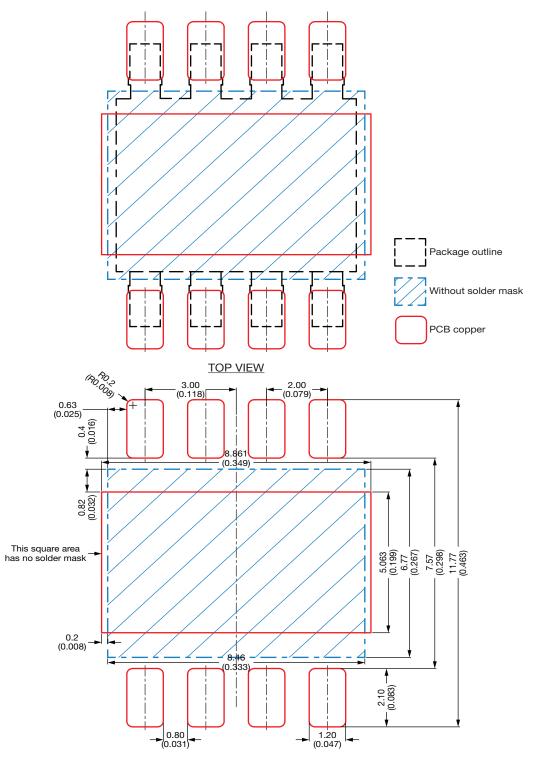


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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm All dimensions are in millimeter (inches)

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DWG: 3002

Revision: 17-Apr-2023

Document Number: 63166



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