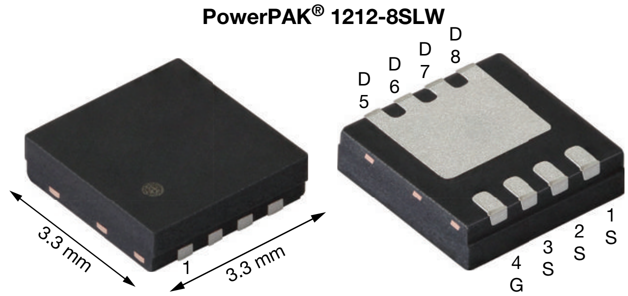
Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8SLW



Top View   Bottom View

Marking code: Q047

PRODUCT SUMMARY	
V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0115
I_D (A) [e]	47
Configuration	Single

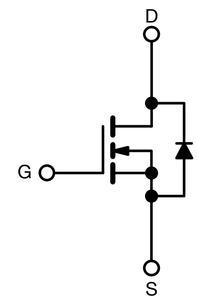
FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Wettable flank terminals
- Low thermal resistance with 0.75 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK® 1212-8SLW
Lead (Pb)-free and halogen-free	SQS186ENW (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-source voltage		V_{DS}	80	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [e]	T_C = 25 °C	I_D	47	A
	T_C = 125 °C		27	
Continuous source current (diode conduction) [e]		I_S	71	
Pulsed drain current [a, e]		I_{DM}	66	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	22	
Single pulse avalanche energy		E_{AS}	24	mJ
Maximum power dissipation [a]	T_C = 25 °C	P_D	79	W
	T_C = 125 °C		26	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Junction-to-ambient	PCB mount [b]	R_{thJA}	54	°C/W
Junction-to-case (drain) [e]		R_{thJC}	1.9	

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. When mounted on 1" square PCB (FR4 material)
c. See solder profile (www.vishay.com/doc?73257). A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. As per on JESD51-14
e. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

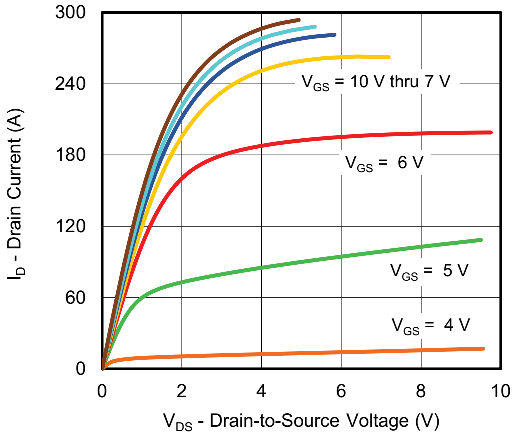
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA		80	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.2	2.8	3.5	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 80 V	-	-	1	μA
		V_{GS} = 0 V	V_{DS} = 80 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 80 V, T_J = 175 °C	-	-	150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	15	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A	-	0.0090	0.0115	Ω
		V_{GS} = 10 V	I_D = 10 A, T_J = 125 °C	-	-	0.0230	
		V_{GS} = 10 V	I_D = 10 A, T_J = 175 °C	-	-	0.0300	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		-	65	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	1470	2058	pF
Output capacitance	C_{oss}			-	338	474	
Reverse transfer capacitance	C_{rss}			-	19	27	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 40 V, I_D = 3 A	-	26	39	nC
Gate-source charge [c]	Q_{gs}			-	7	-	
Gate-drain charge [c]	Q_{gd}			-	6	-	
Gate resistance	R_g	f = 1 MHz		0.4	0.9	2.0	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 13 Ω I_D ≅ 3 A, V_{GEN} = 10 V, R_g = 1 Ω		-	11	17	ns
Rise time [c]	t_r			-	4	8	
Turn-off delay time [c]	$t_{d(off)}$			-	21	32	
Fall time [c]	t_f			-	7	11	
Source-Drain Diode Ratings and Characteristic [b]							
Pulsed current [a]	I_{SM}			-	-	220	A
Forward voltage	V_{SD}	I_F = 10 A, V_{GS} = 0 V		-	0.82	1.1	V
Body diode reverse recovery time	t_{rr}	V_{DD} = 64 V, I_F = 3 A, di/dt = 100 A/μs, R = 10 Ω, L = 0.1 mH, pulse width = 2 μs		-	31	62	ns
Body diode reverse recovery charge	Q_{rr}			-	39	78	nC
Reverse recovery fall time	t_a			-	26	-	ns
Reverse recovery rise time	t_b			-	5	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-2.2	-	A

Notes

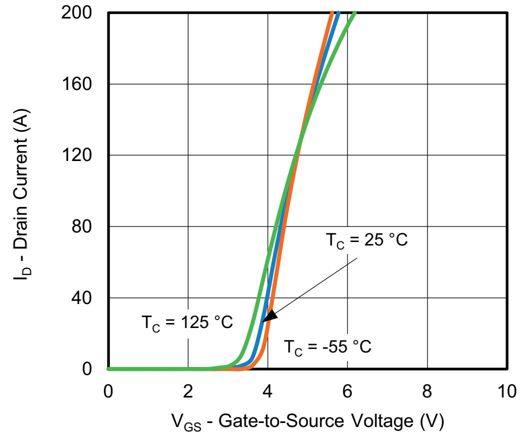
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

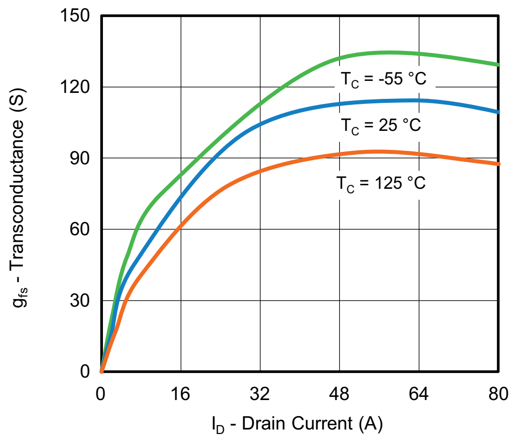
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



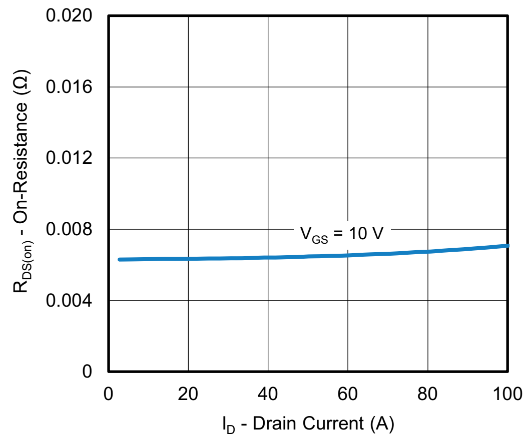
Output Characteristics



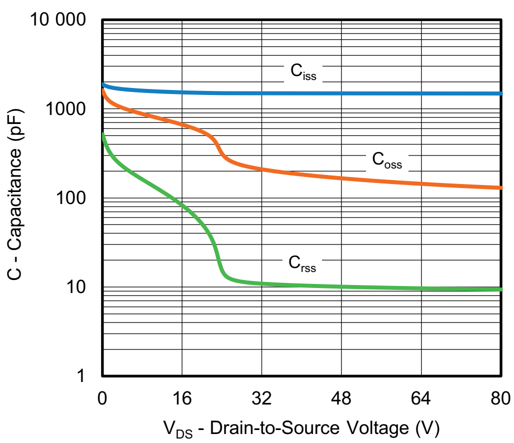
Transfer Characteristics



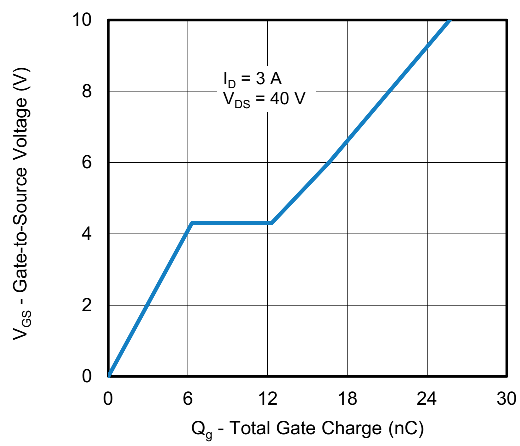
Transconductance



On-Resistance vs. Drain Current

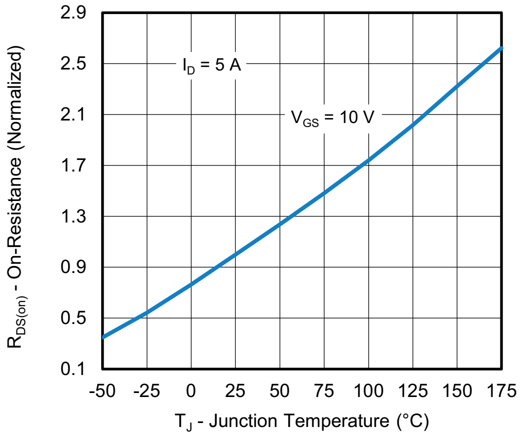


Capacitance

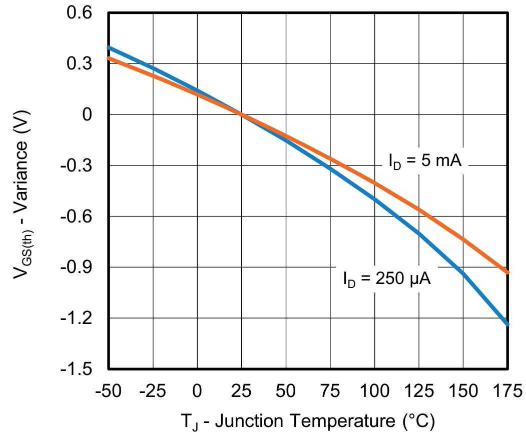


Gate Charge

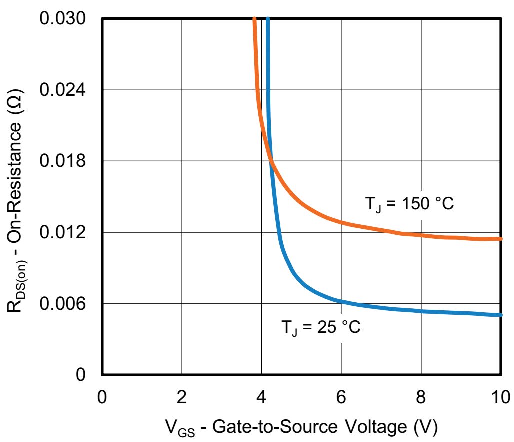
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



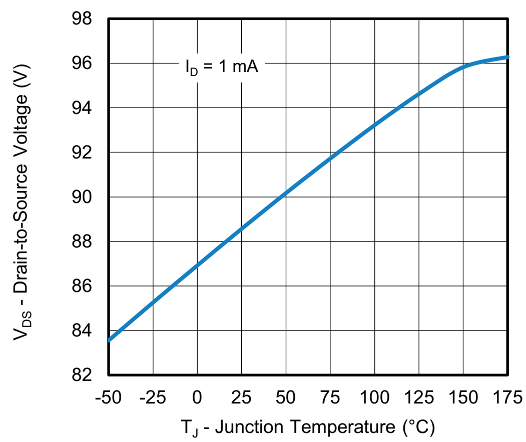
On-Resistance vs. Junction Temperature



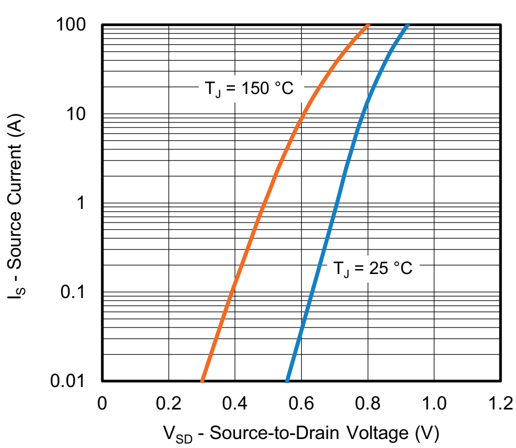
Threshold Voltage



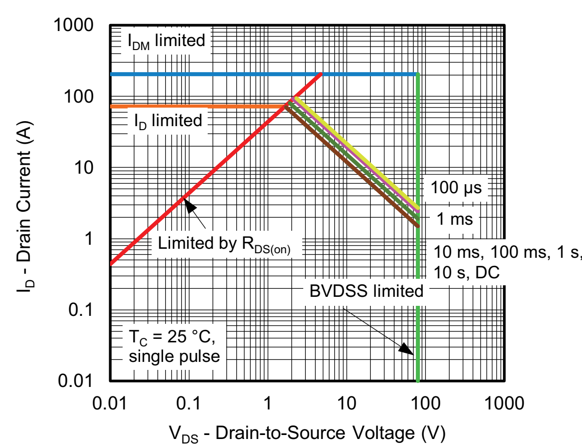
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage

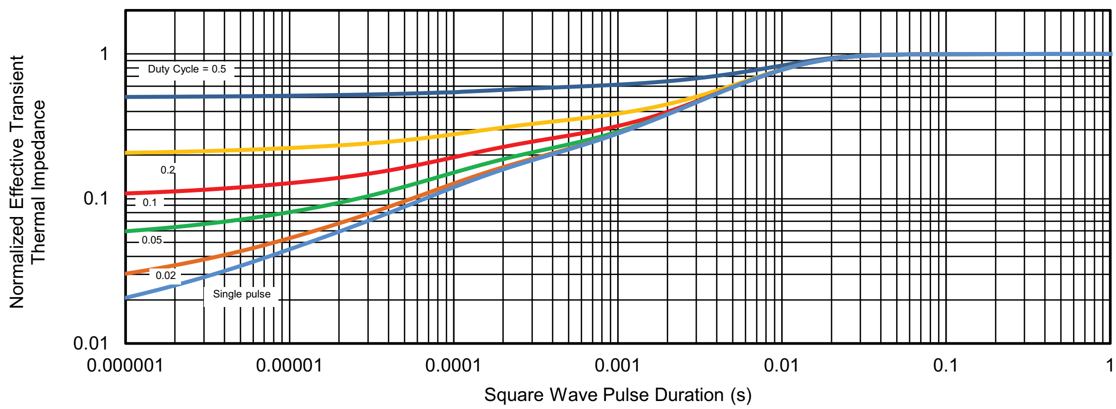


Safe Operating Area

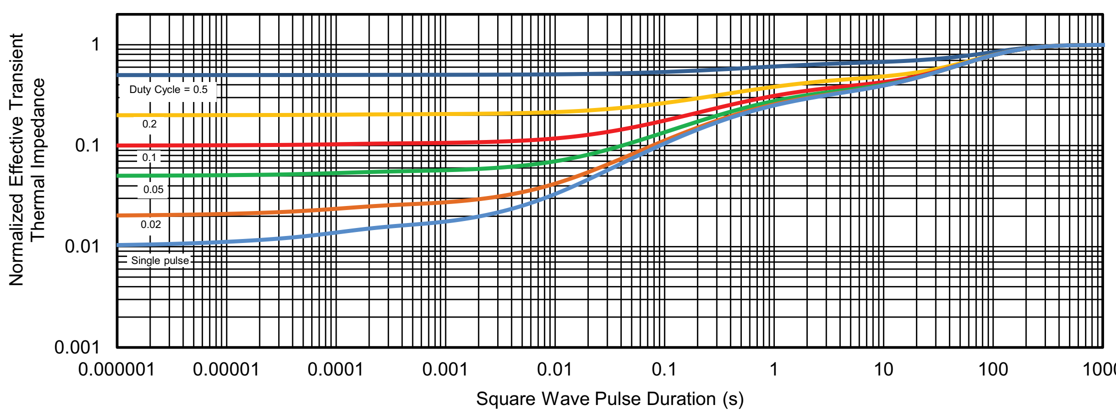
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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