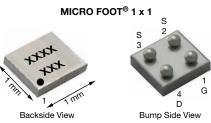




N-Channel 20 V (D-S) MOSFET



8410 Marking code: xxx = Date / lot traceability code

PRODUCT SUMMARY	
V _{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.037
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5 \text{ V}$	0.041
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.8 \text{ V}$	0.047
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.5 \text{ V}$	0.068
Q _g typ. (nC)	5.9
I _D (A) ^a	5.7
Configuration	Single

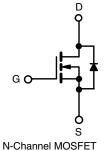
FEATURES

- TrenchFET® power MOSFET
- Ultra small 1 mm x 1 mm maximum outline
- Ultra-thin 0.548 mm maximum height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- · Load switch
- · Power management
- High speed switching



ORDERING INFORMATION	
Package	MICRO FOOT 1 x 1
Lead (Pb)-free and halogen-free	Si8410DB-T2-E1

PARAMETER Drain-source voltage		SYMBOL	LIMIT	UNIT	
		V _{DS}	20	V	
Gate-source voltage		V _{GS}	± 8	v	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C		5.7 ^a		
	T _A = 70 °C		4.5 ^a		
	T _A = 25 °C	I _D	3.8 ^c		
	T _A = 70 °C		3 c	А	
Pulsed drain current (t = 100 μs)	·	I _{DM}	20		
	T _C = 25 °C		1.5 ^a		
Continuous source-drain diode current	T _A = 25 °C	I _S	0.65 ^c		
Maximum power dissipation	T _A = 25 °C		1.8 ^a		
	T _A = 70 °C		1.1 ^a	W	
	T _A = 25 °C	P _D	0.78 ^c		
	T _A = 70 °C		0.5 ^c		
Operating junction and storage temperature ra	nge	T _J , T _{stg}	-55 to +150		
	VPR		260	°C	
Package reflow conditions e	IR/convection		260		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient a, b	t = 10 s	В	55	70	°C/W	
Maximum junction-to-ambient c, d	t = 10 s	R _{thJA}	125	160	C/VV	

- a. Surface mounted on 1" x 1" FR4 board with full copper, t = 10 s, T_A = 25 °C
- b. Maximum under steady state conditions is 100 °C/W
- c. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 10 s
- d. Maximum under steady state conditions is 190 °C/W
- e. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering
- f. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$. OFO A	-	17	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_{D} = 250 \ \mu A$	-	-2.6	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.4	-	0.85	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 100	nA	
Zero esta esta esta esta esta esta esta esta		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	1				
Zero gate voltage drain current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10	μΑ	
On-state drain current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10	-	-	Α	
		V _{GS} = 4.5 V, I _D = 1.5 A	-	0.030	0.037	†	
Duning and the second of the s	Б	V _{GS} = 2.5 V, I _D = 1 A	-	0.033	0.041		
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 1.8 V, I _D = 1 A	-	0.038	0.047	Ω	
		$V_{GS} = 1.5 \text{ V}, I_D = 0.5 \text{ A}$	-	0.044	0.068		
Forward transconductance a	g _{fs}	$V_{DS} = 10 \text{ V}, I_D = 1.5 \text{ A}$	-	17	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	620	-	pF	
Output capacitance	Coss	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	110	-		
Reverse transfer capacitance	C _{rss}		-	40	-		
Table de de co	0	$V_{DS} = 10 \text{ V}, V_{GS} = 8 \text{ V}, I_D = 1.5 \text{ A}$	-	10.4	16	nC	
Total gate charge	Q_g		-	5.9	9		
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.5 \text{ A}$	-	0.7	-		
Gate-drain charge	Q_{gd}		-	0.66	-		
Gate resistance	Rg	V _{GS} = 0.1 V, f = 1 MHz	-	5.3	-	Ω	
Turn-on delay time	t _{d(on)}		-	5	10		
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_{L} = 6.7 \Omega$	-	25	50		
Turn-off delay time	t _{d(off)}	$I_D \cong 1.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	26	50		
Fall time	t _f		-	10	20		
Turn-on delay time	t _{d(on)}		-	5	10	- ns - -	
Rise time	t _r	V_{DD} = -10 V, R_L = 6.7 Ω	-	22	45		
Turn-off delay time	t _{d(off)}	$I_D \cong -1.5 \text{ A}, V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$	-	23	45		
Fall time	t _f		-	10	20		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _A = 25 °C	-	-	1.5	^	
Pulse diode forward current	I _{SM}		-	-	20	Α	
Body diode voltage	V _{SD}	$I_S = 1.5 \text{ A}, V_{GS} = 0$	-	0.7	1.2	V	
Body diode reverse recovery time	t _{rr}		-	15	30	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 1.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	6	15	nC	
Reverse recovery fall time	ta	$T_J = 25 ^{\circ}C$	-	8.5	-	ur -	
Reverse recovery rise time	t _b		-	6.5	-	ns	

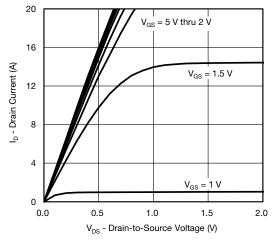
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

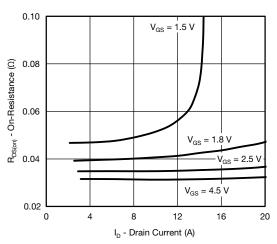
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



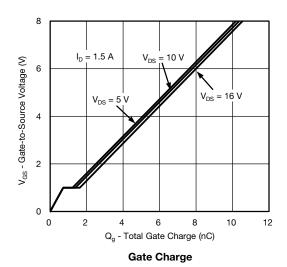
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

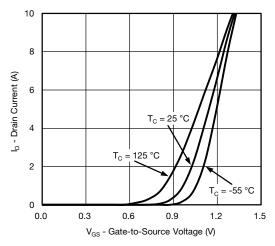


Output Characteristics

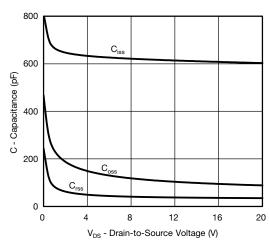


On-Resistance vs. Drain Current and Gate Voltage

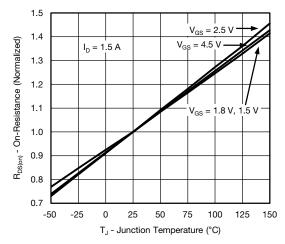




Transfer Characteristics



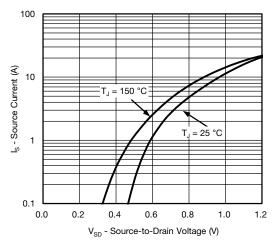
Capacitance



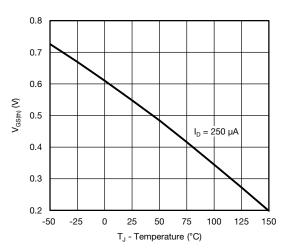
On-Resistance vs. Junction Temperature



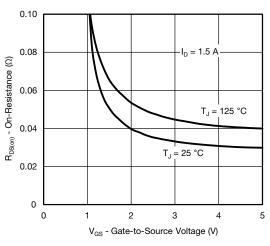
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



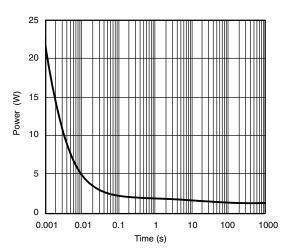
Source-Drain Diode Forward Voltage



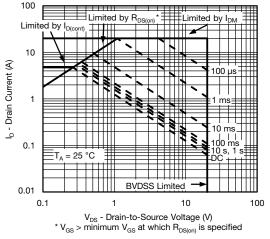
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



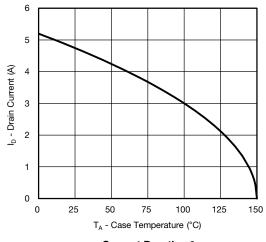
Single Pulse Power, Junction-to-Ambient

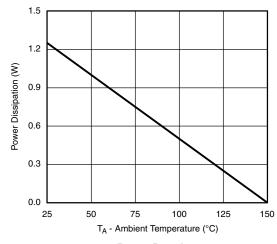


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Current Derating ^a

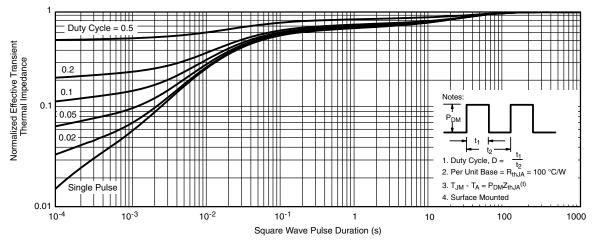
Power Derating

Note

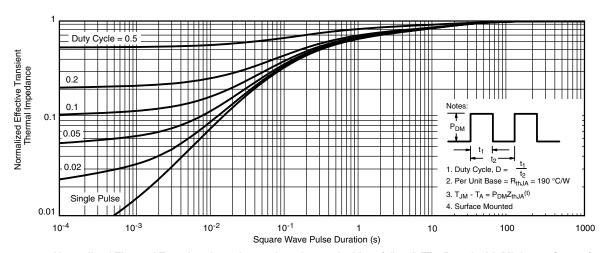
- When mounted on 1" x 1" FR4 with full copper
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

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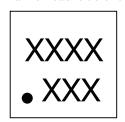


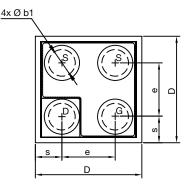
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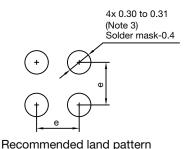
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MICRO FOOT®: 4-Bumps (1 mm x 1 mm, 0.5 mm Pitch, 0.286 mm Bump Height)

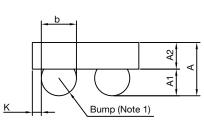
Mark on backside of die











Notes

- 1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
- 2. Backside surface is coated with a Ti/Ni/Ag layer.
- 3. Non-solder mask defined copper landing pad.
- 4. Laser mark on the backside surface of die.
- 5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- 6. is the location of pin 1

DIM.		MILLIMETERS			INCHES			
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.458	0.504	0.550	0.0180	0.0198	0.0217		
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113		
A2	0.244	0.254	0.264	0.0096	0.0100	0.0104		
b	0.297	0.330	0.363	0.0117	0.0130	0.0143		
b1		0.250			0.0098			
е	0.500				0.0197			
S	0.210	0.230	0.250	0.0083	0.0091	0.0096		
D	0.920	0.960	1.000	0.0362	0.0378	0.0394		
K	0.029	0.065	0.102	0.0011	0.0026	0.0040		

Note

• Use millimeters as the primary measurement.

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DWG: 6039

Revision: 27-Apr-15 **1** Document Number: 69370



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