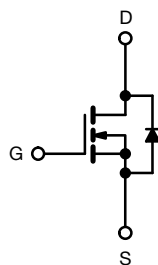


Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Extremely low $R_{DS(on)}$
- Compact plastic package
- Fast switching
- Low drive current
- Ease of paralleling
- Excellent temperature stability
- Parts per million quality
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

The technology has expanded its product base to serve the low voltage, very low $R_{DS(on)}$ MOSFET transistor requirements. Vishay's highly efficient geometry and unique processing have been combined to create the lowest on resistance per device performance. In addition to this feature all have documented reliability and parts per million quality!

The transistor also offer all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and in systems that are operated from low voltage batteries, such as automotive, portable equipment, etc.

PRODUCT SUMMARY

V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.10
Q_g (Max.) (nC)	17	
Q_{gs} (nC)	9.0	
Q_{gd} (nC)	3.0	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFZ20PbF
Lead (Pb)-free and halogen-free	IRFZ20PbF-BE3

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage ^a			V _{DS}	50	V
Gate-source voltage ^a			V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	I _D	15	A
		T _C = 100 °C		10	
Pulsed drain current ^b			I _{DM}	60	
Single pulse avalanche energy ^c			E _{AS}	5	mJ
Linear derating factor (see fig. 16)				0.32	W/°C
Maximum power dissipation (see fig. 16)	T _C = 25 °C		P _D	40	W
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)	For 10 s			300 (0.063" (1.6 mm) from case)	

Notes

a. $T_J = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$

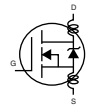
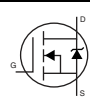
b. Repetitive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 11)

c. Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.07\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 12\text{ A}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Typical socket mount, junction-to-ambient	R_{thJA}	-	80	°C/W
Case-to-sink, mounting surface flat, smooth, and greased	R_{thCS}	1.0	-	
Junction-to-case	R_{thJC}	-	3.12	

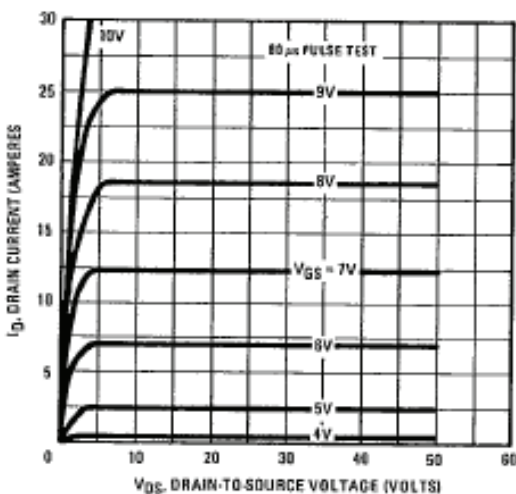
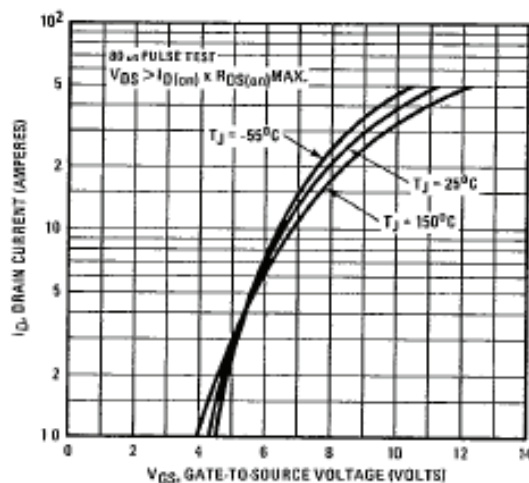
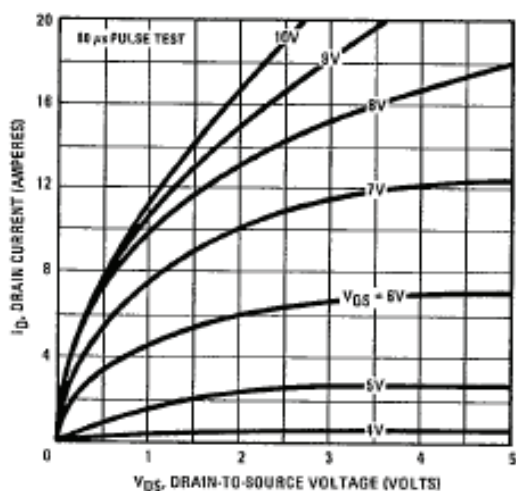
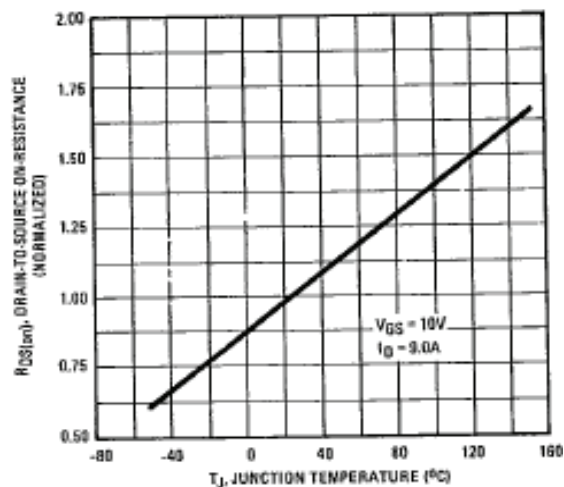
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		50	-	-	V
V _{DS} temperature coefficient	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source threshold voltage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Gate-source leakage	I _{DSS}	V _{DS} > Max. Rating, V _{GS} = 0 V		-	-	250	μA
Zero gate voltage drain current		V _{DS} = Max. Rating x 0.8, V _{GS} = 0 V, T _C = 125 °C		-	-	1000	
		I _{D(on)}	V _{GS} = 10 V	V _{DS} > I _{D(on)} x R _{DS(on)} max.	-	-	15
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.080	0.10	Ω
Forward transconductance ^b	g _{fs}	V _{DS} > I _{D(on)} x R _{DS(on)} max., I _D = 9.0 A		5.0	6.0	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 11		-	560	860	pF
Output capacitance	C _{oss}			-	250	350	
Reverse transfer capacitance	C _{rss}			-	60	100	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 20 A, V _{DS} = 0.8 max. rating, see fig. 18 for test circuit (Gate charge is essentially independent of operating temperature)	-	12	17	nC
Gate-source charge	Q _{gs}			-	9.0	-	
Gate-drain charge	Q _{gd}			-	3.0	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 25 V, I _D = 9.0 A, Z ₀ = 50 Ω, see fig. 5 ^b		-	15	30	ns
Rise time	t _r			-	45	90	
Turn-off delay time	t _{d(off)}			-	20	40	
Fall time	t _f			-	15	30	
Internal drain inductance	L _D	Modified MOSFET symbol showing the internal device inductances 		-	3.5	-	nH
Internal source inductance	L _S			-	4.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction rectifier 		-	-	15	A
Pulsed diode forward current ^a	I _{SM}			-	-	60	
Body diode voltage ^b	V _{SD}	T _C = 25 °C, I _S = 15 A, V _{GS} = 0 V		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 150 °C, I _F = 15 A, dI _F /dt = 100 A/μs		-	100	-	ns
Body diode reverse recovery charge	Q _{rr}			-	0.4	-	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 5)

b. Pulse test: Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 1 - Typical Transfer Characteristics

Fig. 2 - Typical Saturation Characteristics

Fig. 2 - Normalized On-Resistance vs. Temperature

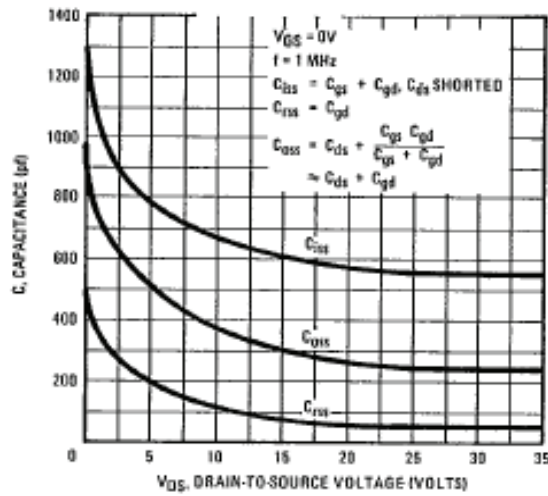


Fig. 3 - Typical Capacitance vs. Drain-to-Source Voltage

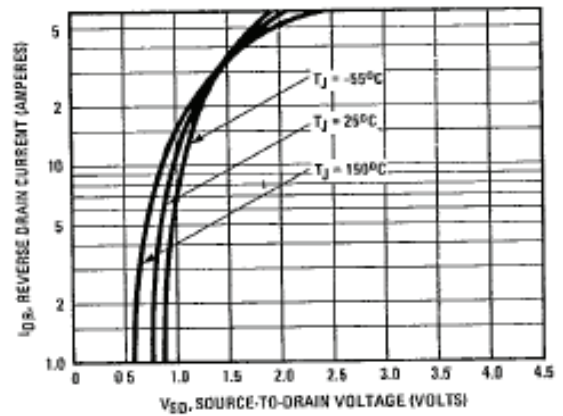


Fig. 5 - Typical Source-Drain Diode Forward Voltage

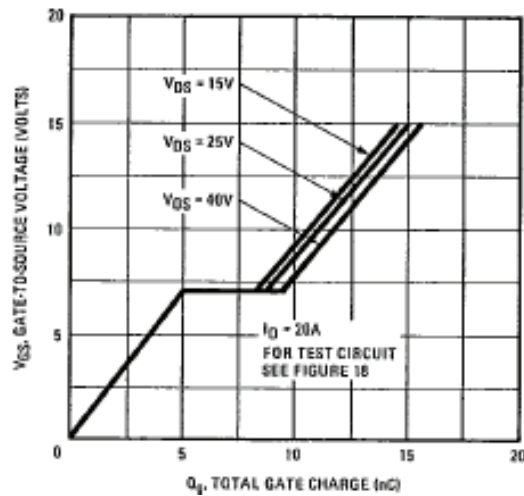


Fig. 4 - Typical Gate Charge vs. Gate-to-Source Voltage

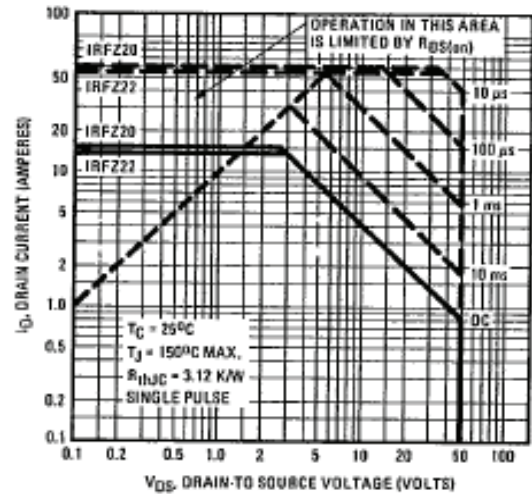
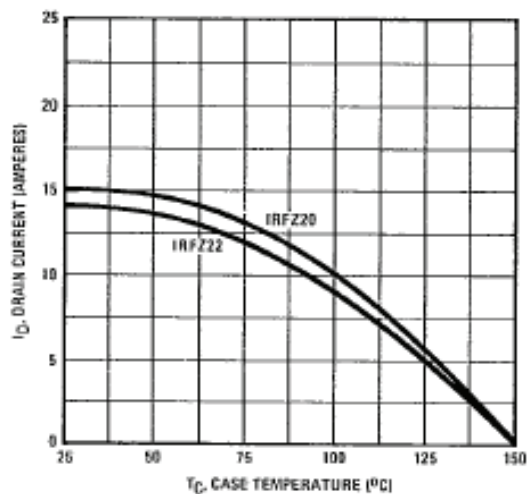
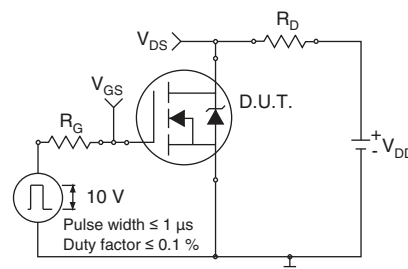
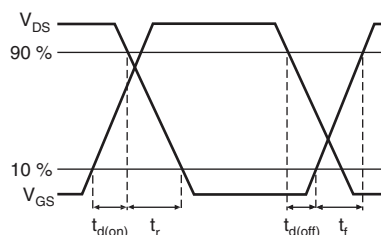
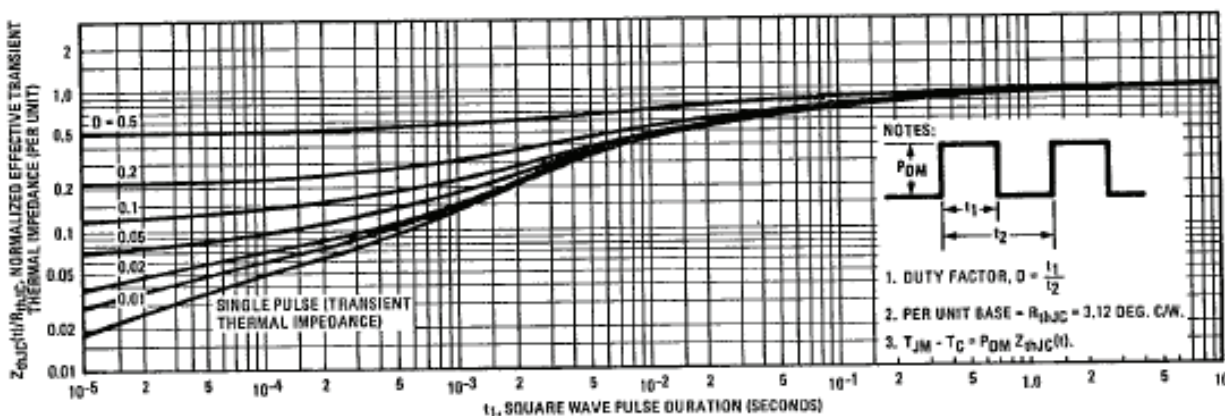
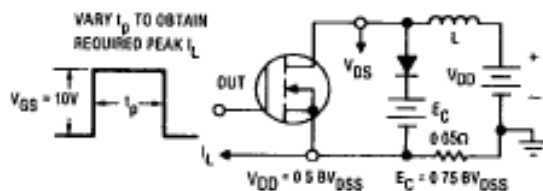
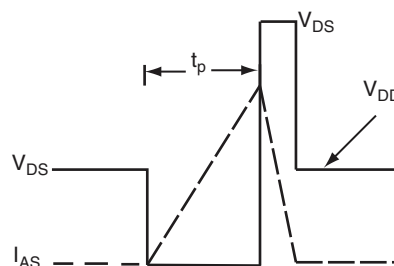


Fig. 6 - Maximum Safe Operating Area


Fig. 7 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

Fig. 12a - Clamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

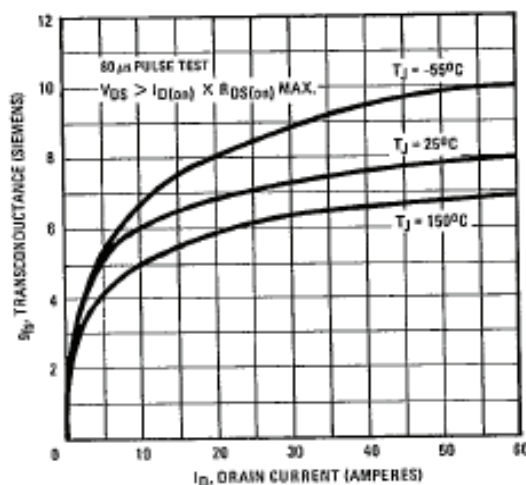


Fig. 13 - Typical Transconductance vs. Drain Current

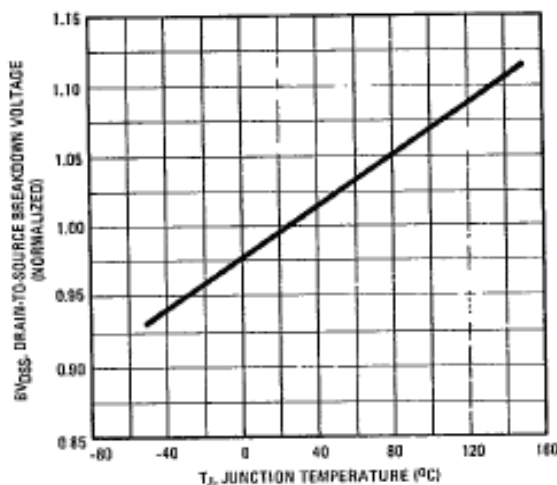


Fig. 14 - Breakdown Voltage vs. Temperature

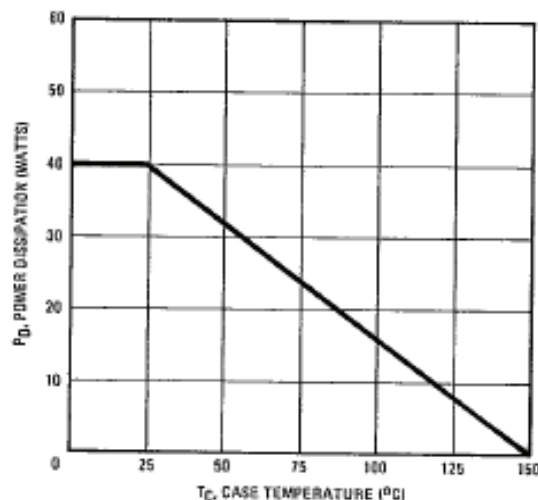


Fig. 16 - Power vs. Temperature Derating Curve

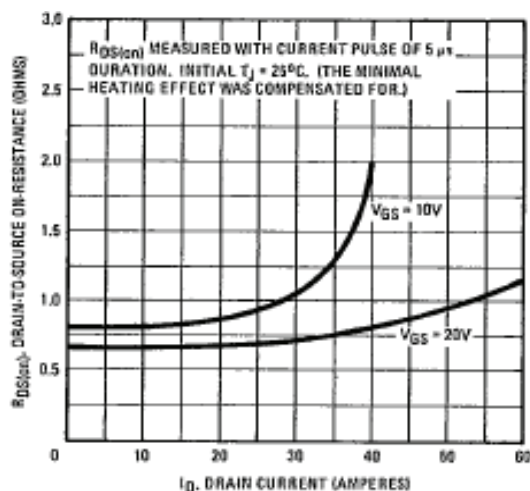


Fig. 15 - Typical On-Resistance vs. Drain Current

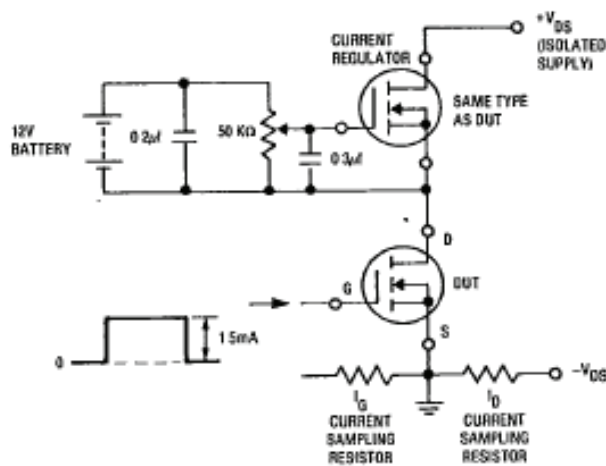
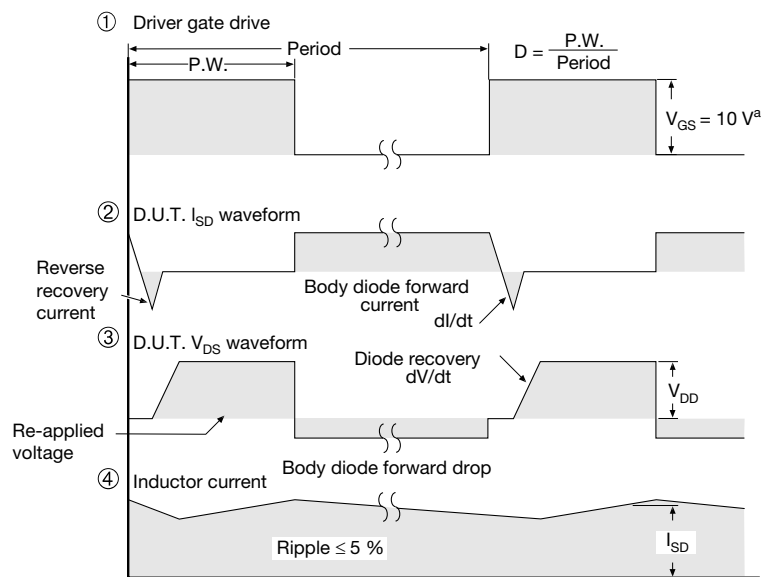
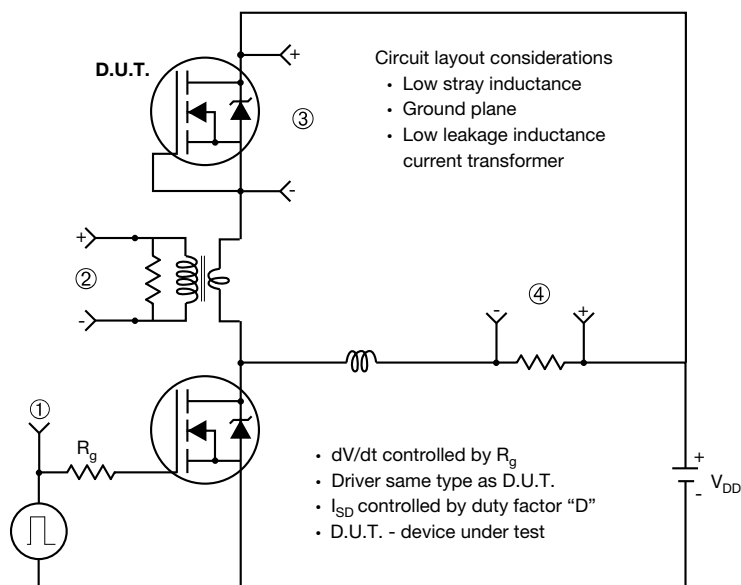


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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