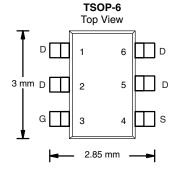




P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I _D (A) ^{d,e}	Q _g (Typ.)			
- 30	0.0252 at V _{GS} = - 10 V	- 8	15 nC			
- 30	0.0360 at $V_{GS} = -4.5$ V	- 8	15110			



Ordering Information:

Si3417DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

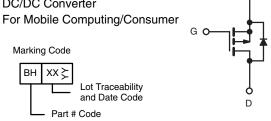
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_q and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Load Switches
- Adaptor Switch
- DC/DC Converter



P-Channel MOSFET

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 30	V	
Gate-Source Voltage	V_{GS}	± 20		
	T _C = 25 °C		- 8 ^e	
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C		- 8 ^e	
Continuous Diam Current (1) = 150 °C)	T _A = 25 °C	l _D	- 7.3 ^{a, b}	
	T _A = 70 °C		- 5.8 ^{a, b}	
Pulsed Drain Current (t = 100 μs)	<u>.</u>	I _{DM}	- 50	Α
Continuous Course Dunin Diada Courset	T _C = 25 °C		- 3.5	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 1.7 ^{a, b}	
Avalanche Current	1 04	I _{AS}	- 20	
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	20	mJ
	T _C = 25 °C		4.2	
Mariana Para Pirata di a	T _C = 70 °C		2.7	
Maximum Power Dissipation	T _A = 25 °C	P _D	2 ^{a, b}	W
	T _A = 70 °C		1.3 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	40	62.5	°C/W		
Maximum Junction-to-Foot	Steady State	R _{thJF}	25	30	0/00		

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under steady state conditions is 110 $^{\circ}\text{C/W}.$
- d. Based on $T_C = 25$ °C.
- e. Package limited.

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 30			V		
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 31		mV/°C		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.5				
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V		
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA		
Zero Gate Voltage Drain Current	lana	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μΑ		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 5			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 30			Α		
Dunin Course On Chata Basistanas	R	$V_{GS} = -10 \text{ V}, I_D = -7.3 \text{ A}$		0.0210	0.0252	0		
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	V _{GS} = - 4.5 V, I _D = - 6.1 A		0.0300	0.0360	Ω		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 7.3 A		23		S		
Dynamic ^b								
Input Capacitance	C _{iss}			1350		pF		
Output Capacitance	C _{oss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		215				
Reverse Transfer Capacitance	C _{rss}			185				
Total Cata Charge	Qg	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -7.3 \text{ A}$		32	50	nC		
Total Gate Charge				15	25			
Gate-Source Charge	Q _{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -7.3 \text{ A}$		4				
Gate-Drain Charge	Q _{gd}			7.5				
Gate Resistance	R _g	f = 1 MHz	1.2	5.8	11.6	Ω		
Turn-On Delay Time	t _{d(on)}			10	15			
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 2.6 \Omega$		8	15			
Turn-Off DelayTime	t _{d(off)}	$I_{D} \cong -5.8 \text{ A}, V_{GEN} = -10 \text{ V}, R_{g} = 1 \Omega$		45	70			
Fall Time	t _f			12	25			
Turn-On Delay Time	t _{d(on)}			42	70	ns		
Rise Time	t _r	$V_{DD} = -15 \text{ V}, R_{L} = 2.6 \Omega$		35	60	- -		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -5.8 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		40	70			
Fall Time	t _f			16	30			
Drain-Source Body Diode Characterist	ics				_			
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 3.5	Α.		
Pulse Diode Forward Current (t = 100 μs)	I _{SM}				- 50	A		
Body Diode Voltage	V _{SD}	I _S = - 5.8 A, V _{GS} = 0 V		- 0.75	- 1.2	V		
Body Diode Reverse Recovery Time	t _{rr}			34	60	ns		
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 5.8 A, dl/dt = 100 A/μs,		22	40	nC		
Reverse Recovery Fall Time	t _a	T _J = 25 °C		11		ns		
Reverse Recovery Rise Time	t _b			23				

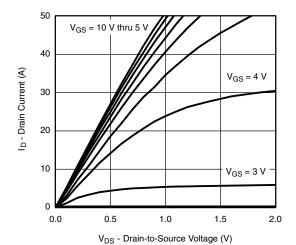
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

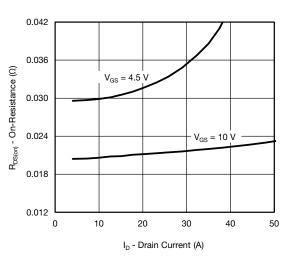
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



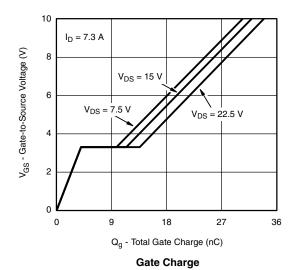
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

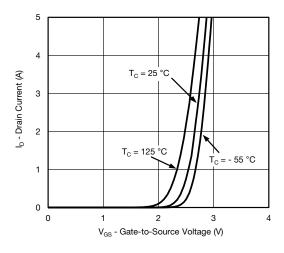


Output Characteristics

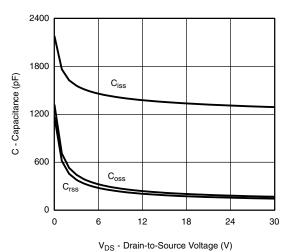


On-Resistance vs. Drain Current

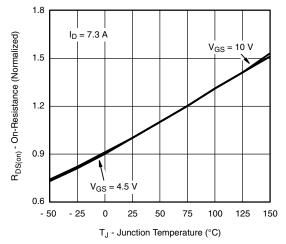




Transfer Characteristics



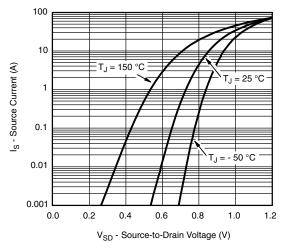
Capacitance



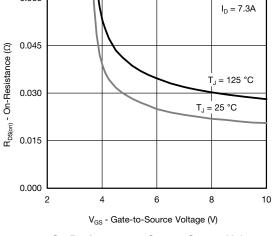
On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

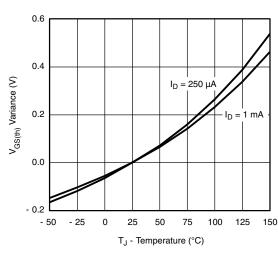




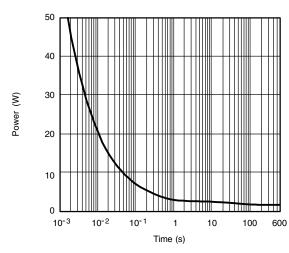


0.060

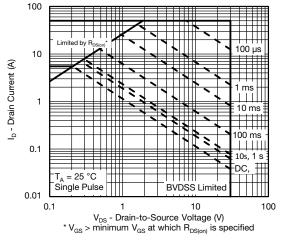
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



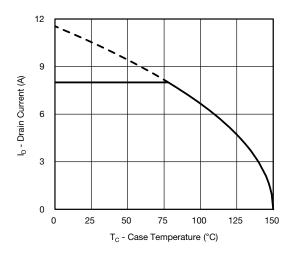
Single Pulse Power, Junction-to-Ambient



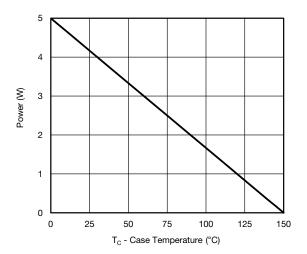
Safe Operating Area

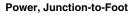


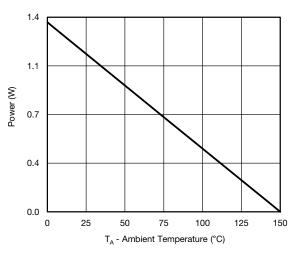
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*







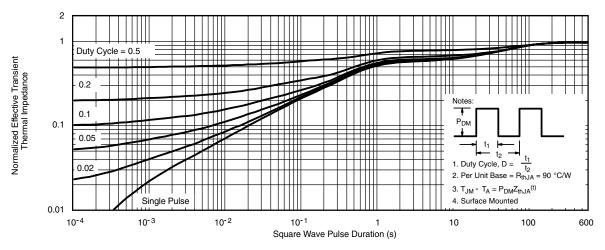
Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

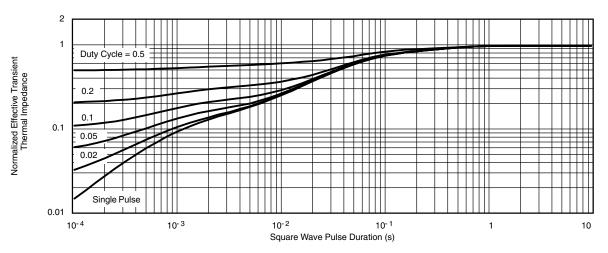
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62890.





TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C





5-LEAD TSOP







	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.008		
D	2.95	3.05	3.10	0.116 0.120		0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC		0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.079		
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

DWG: 5540

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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