

## Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.45
$Q_g$ max. (nC)	41	
$Q_{gs}$ (nC)	6.5	
$Q_{gd}$ (nC)	22	
Configuration	Single	

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic  $dv/dt$  rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHF634S-GE3	-	SiHF634STRR-GE3 <sup>a</sup>
Lead (Pb)-free	-	IRF634STRLPbF <sup>a</sup>	IRF634STRRPbF <sup>a</sup>

### Note

a. See device orientation

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	250	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{DM}$	32	W/ $^\circ\text{C}$
Linear derating factor		0.59	
Linear derating factor (PCB mount) <sup>e</sup>		0.025	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	300	mJ
Avalanche current <sup>a</sup>	$I_{AR}$	8.1	A
Repetitive avalanche energy	$E_{AR}$	7.4	mJ
Maximum power dissipation	$P_D$	$T_C = 25\text{ }^\circ\text{C}$	W
Maximum power dissipation (PCB mount) <sup>e</sup>		$T_A = 25\text{ }^\circ\text{C}$	
Peak diode recovery $dv/dt$ <sup>c</sup>	$dv/dt$	4.8	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	for 10 s	300	

### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b.  $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 7.3\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 8.1\text{ A}$  (see fig. 12)

c.  $I_{SD} \leq 8.1\text{ A}$ ,  $di/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$

d. 1.6 mm from case

e. When mounted on 1" square PCB (FR-4 or G-10 material)

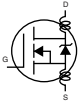

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Maximum junction-to-ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum junction-to-case (drain)	$R_{thJC}$	-	1.7	

**Note**

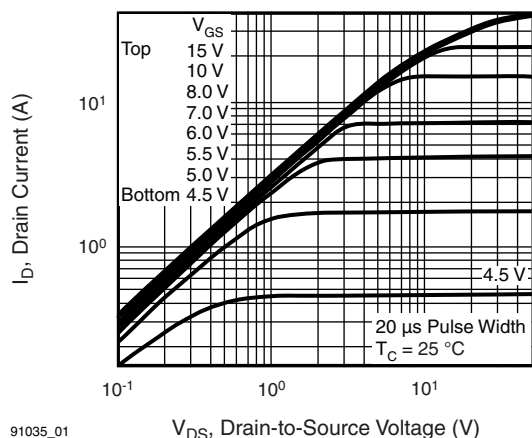
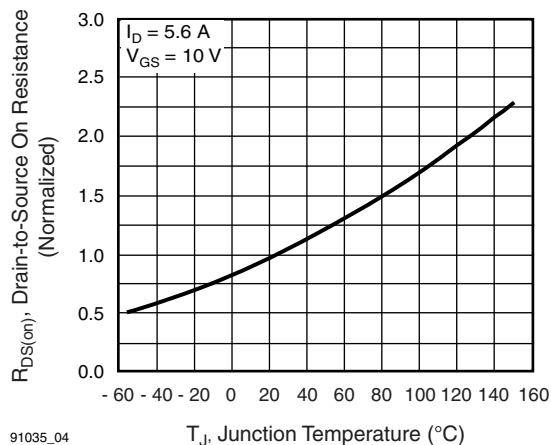
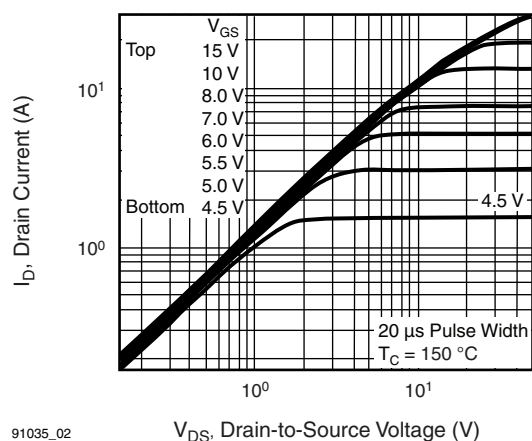
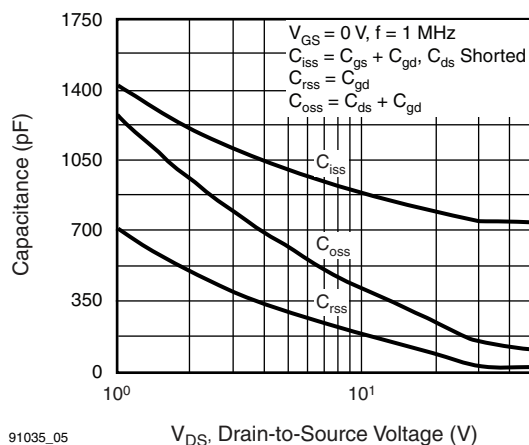
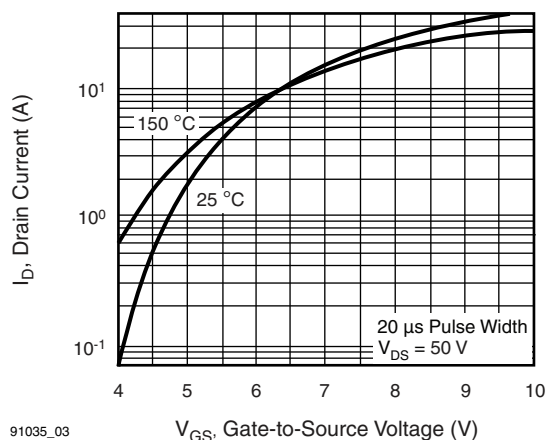
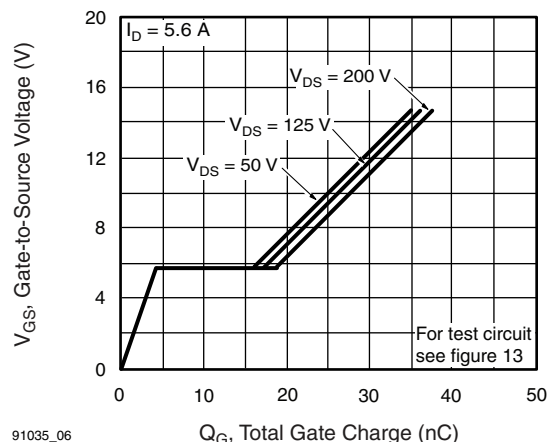
a. When mounted on 1" square PCB (FR-4 or G-10 material)

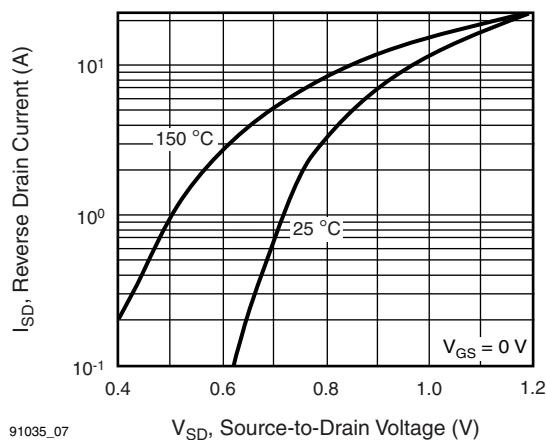
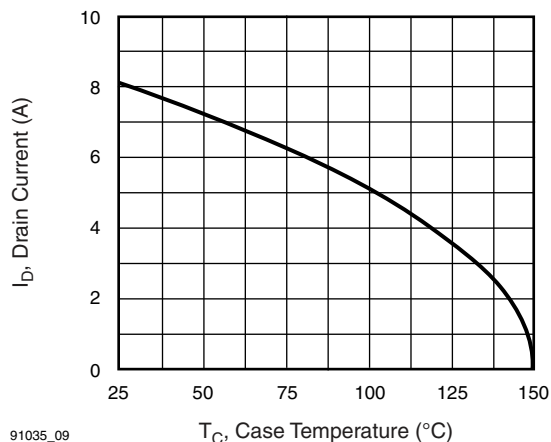
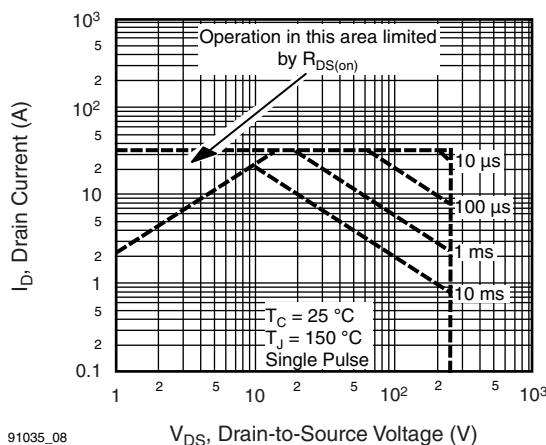
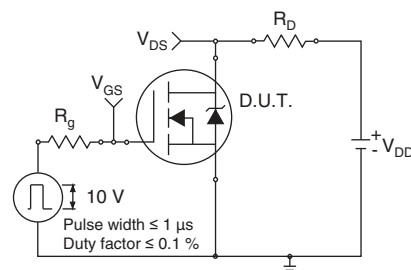
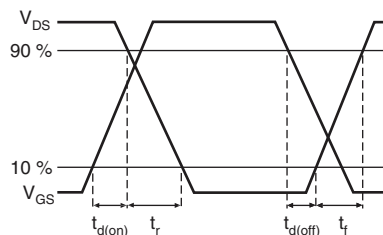
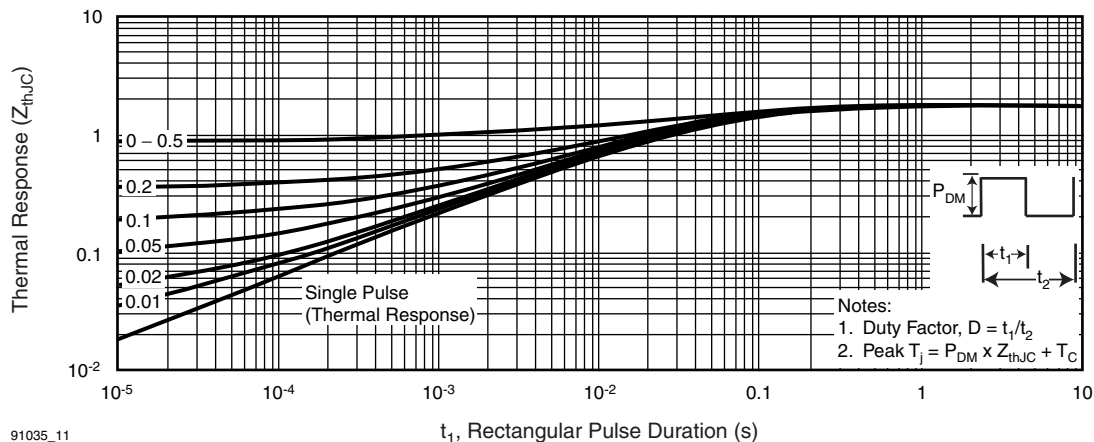
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

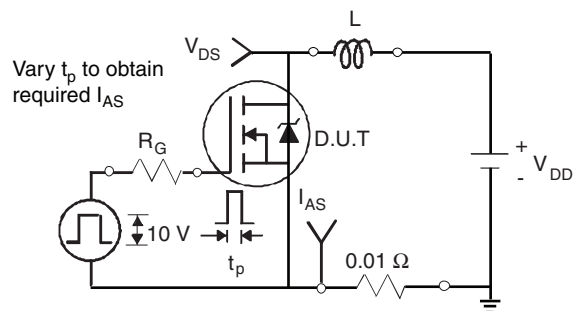
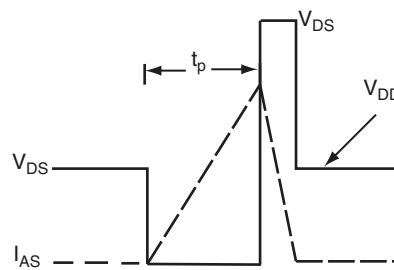
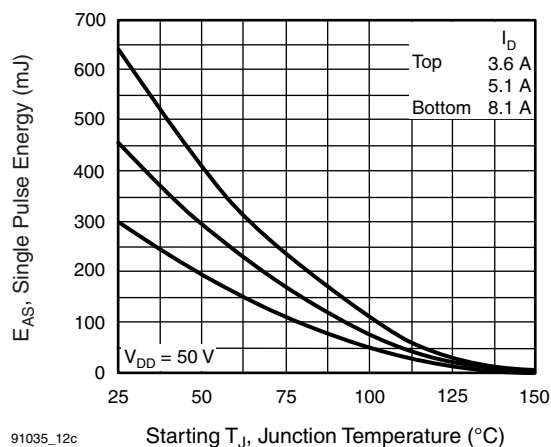
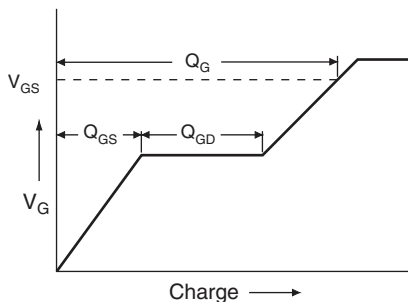
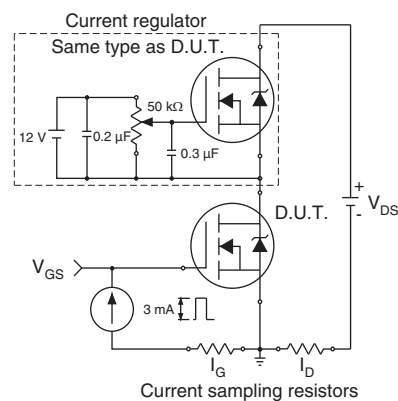
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ , $I_D = 250\text{ }\mu\text{A}$		250	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$		-	0.37	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 250\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 200\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 5.1\text{ A}^b$	-	-	0.45	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 5.1\text{ A}^b$		1.6	-	-	S
Dynamic							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	770	-	pF
Output capacitance	$C_{oss}$			-	190	-	
Reverse transfer capacitance	$C_{rss}$			-	52	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 5.6\text{ A}$ , $V_{DS} = 200\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	41	nC
Gate-source charge	$Q_{gs}$			-	-	6.5	
Gate-drain charge	$Q_{gd}$			-	-	22	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 125\text{ V}$ , $I_D = 5.6\text{ A}$ , $R_g = 12\text{ }\Omega$ , $R_D = 22\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	9.6	-	ns
Rise time	$t_r$			-	21	-	
Turn-off delay time	$t_{d(off)}$			-	42	-	
Fall time	$t_f$			-	19	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		0.6	-	2.9	$\Omega$
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.1	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	32	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 8.1\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = 5.6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}^b$		-	220	440	ns
Body diode reverse recovery charge	$Q_{rr}$			-	1.2	2.4	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

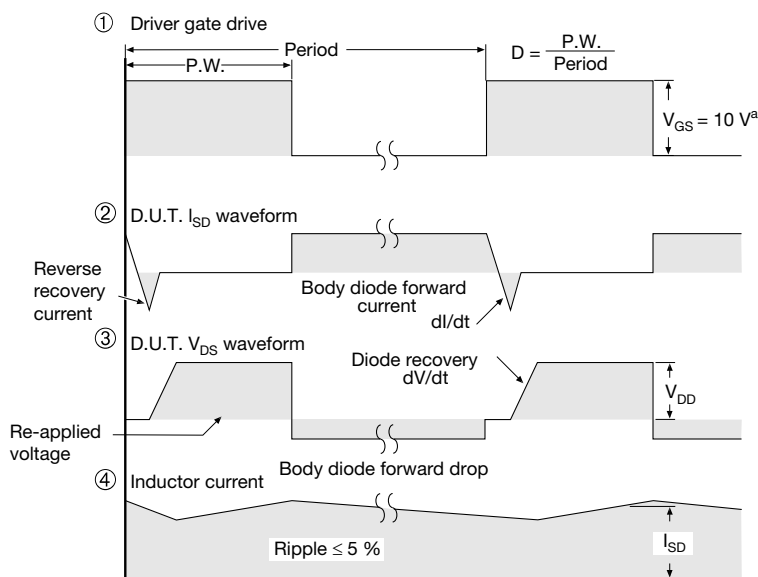
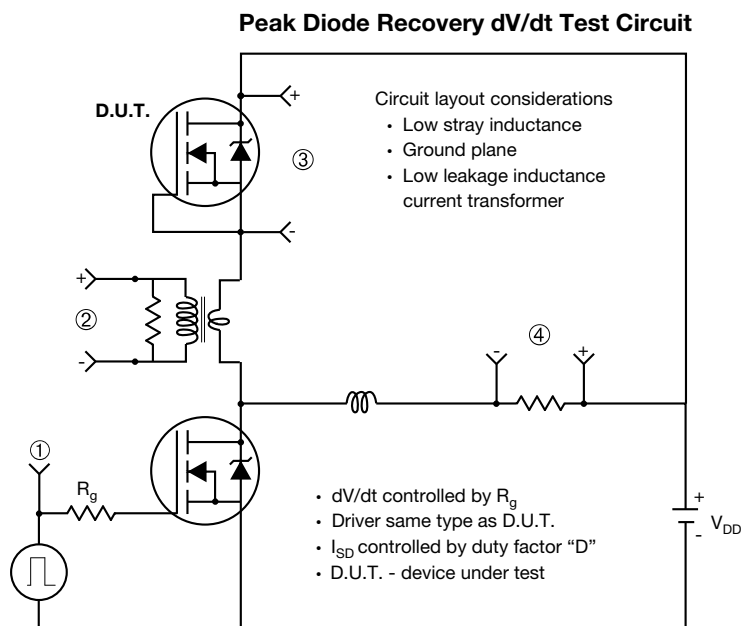
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ °C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ °C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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