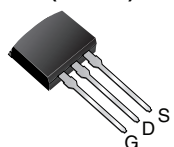
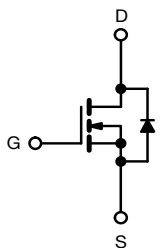
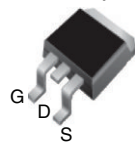


## Power MOSFET

I<sup>2</sup>PAK (TO-262)

D<sup>2</sup>PAK (TO-263)


N-Channel MOSFET

### FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche, and dynamic  $dv/dt$  ruggedness
- Fully characterized capacitance and Avalanche voltage and current
- Effective  $C_{oss}$  specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

### TYPICAL SMPS TOPOLOGIES

- Single transistor flyback

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	2.2
$Q_g$ max. (nC)	23	
$Q_{gs}$ (nC)	5.4	
$Q_{gd}$ (nC)	11	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHFBC30AS-GE3	SiHFBC30ASTRL-GE3 <sup>a</sup>	SiHFBC30ASTRR-GE3 <sup>a</sup>	SiHFBC30AL-GE3
Lead (Pb)-free	IRFBC30ASPbF	IRFBC30ASTRLPbF <sup>a</sup>	-	IRFBC30ALPbF

### Note

a. See device orientation

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	600	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current <sup>a, e</sup>	$I_{DM}$	14	
Linear derating factor		0.69	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	290	mJ
Avalanche current <sup>a</sup>	$I_{AR}$	3.6	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	7.4	mJ
Maximum power dissipation	$P_D$	74	W
Peak diode recovery $dv/dt$ <sup>c, e</sup>	$dv/dt$	7.0	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	for 10 s	300	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 46\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.6\text{ A}$  (see fig. 12)
- $I_{SD} \leq 3.6\text{ A}$ ,  $dI/dt \leq 170\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- Uses IRFBC30A/SiHFBC30A data and test conditions




## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mounted, steady-state) <sup>a</sup>	R <sub>thJA</sub>	-	40	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.7	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

## SPECIFICATIONS (T<sub>J</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA	600	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>	-	0.67	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	25	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.2 A <sup>b</sup>	-	-	2.2	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 2.2 A	2.1	-	-	S
<b>Dynamic</b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5	-	510	-	pF
Output capacitance	C <sub>oss</sub>		-	70	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	3.5	-	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	730	-
			V <sub>DS</sub> = 480 V, f = 1.0 MHz	-	19	
Effective output capacitance	C <sub>oss eff.</sub>	V <sub>DS</sub> = 0 V to 480 V <sup>c</sup>	-	31	-	-
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.6 A, V <sub>DS</sub> = 480 V, see fig. 6 and 13 <sup>b</sup>	-	-	23	nC
Gate-source charge	Q <sub>gs</sub>		-	-	5.4	
Gate-drain charge	Q <sub>gd</sub>		-	-	11	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 3.6 A, R <sub>g</sub> = 12 Ω, R <sub>D</sub> = 82 Ω, see fig. 10 <sup>b, d</sup>	-	9.8	-	ns
Rise time	t <sub>r</sub>		-	13	-	
Turn-off delay time	t <sub>d(off)</sub>		-	19	-	
Fall time	t <sub>f</sub>		-	12	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain	0.8	-	4.6	Ω
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>		-	-	14	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.6 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	1.6	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.6 A, dI/dt = 100 A/μs <sup>b</sup>	-	400	600	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	1.1	1.7	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )				

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>
- Uses IRFBC30A/SiHFBC30A data and test conditions



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

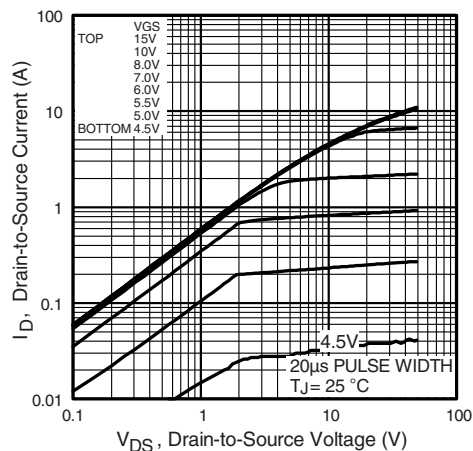


Fig. 1 - Typical Output Characteristics

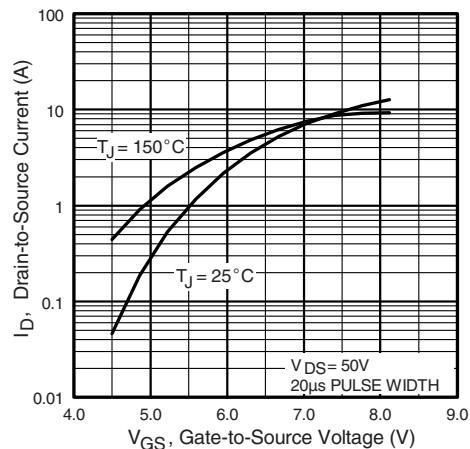


Fig. 3 - Typical Transfer Characteristics

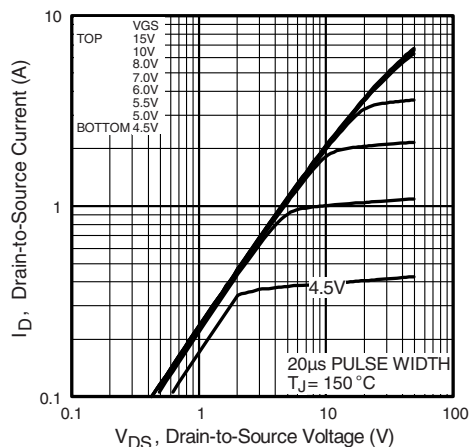


Fig. 2 - Typical Output Characteristics

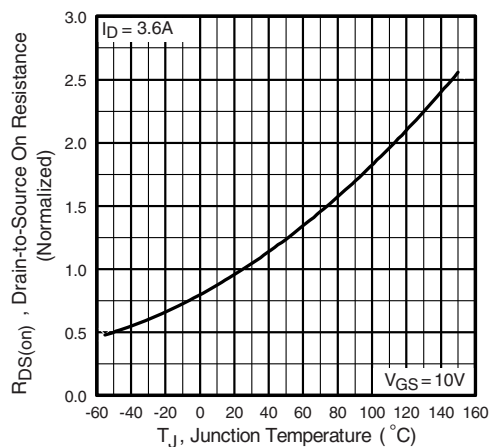


Fig. 4 - Normalized On-Resistance vs. Temperature



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

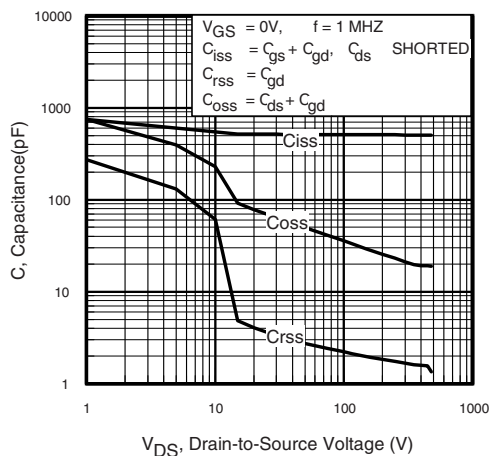


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

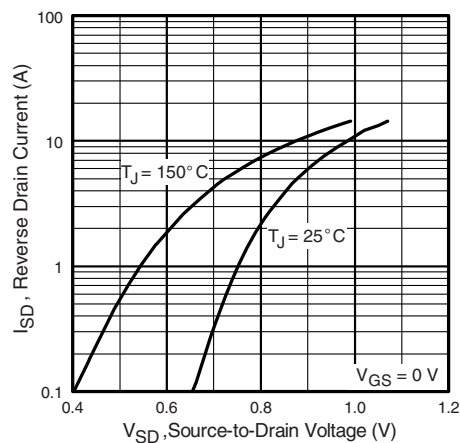


Fig. 7 - Typical Source-Drain Diode Forward Voltage

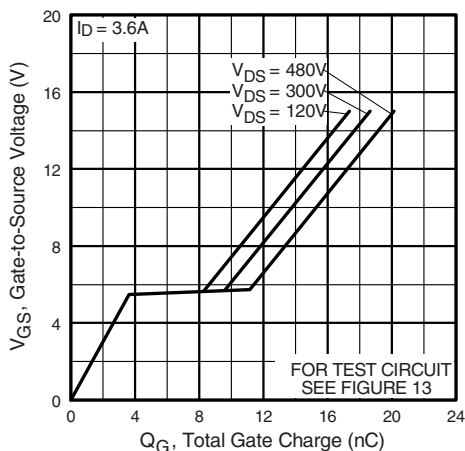


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

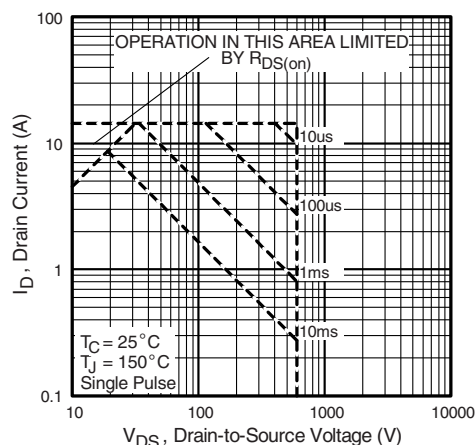


Fig. 8 - Maximum Safe Operating Area

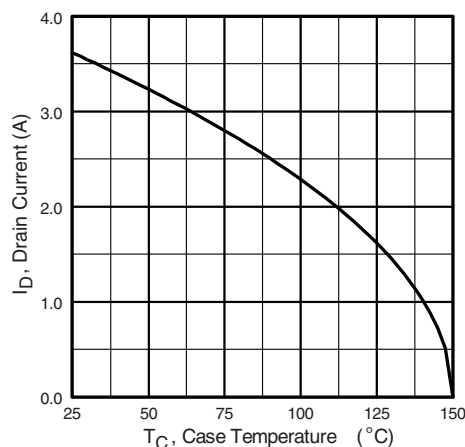


Fig. 9 - Maximum Drain Current vs. Case Temperature

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

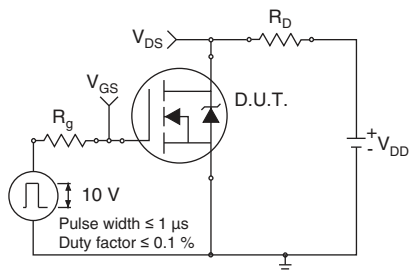


Fig. 10a - Switching Time Test Circuit

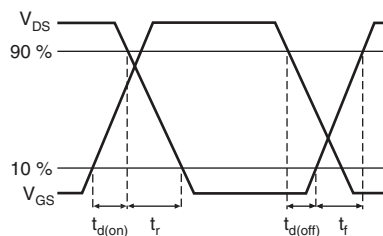


Fig. 10b - Switching Time Waveforms

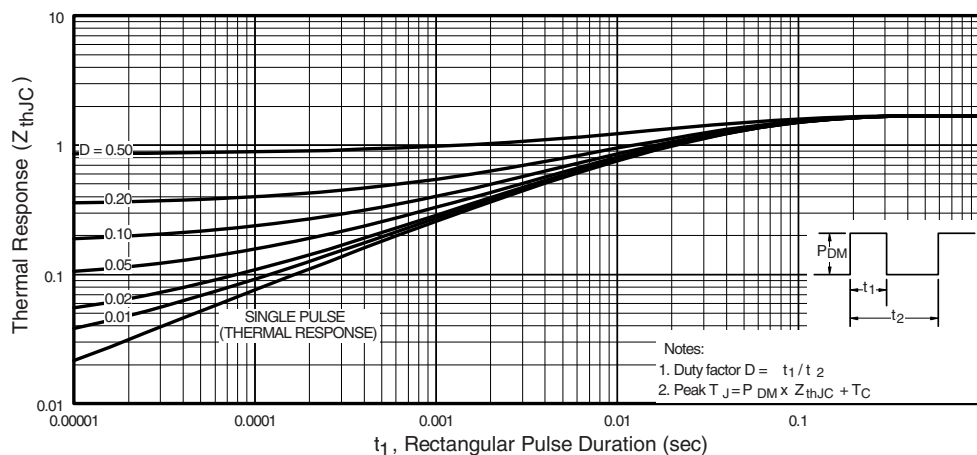


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

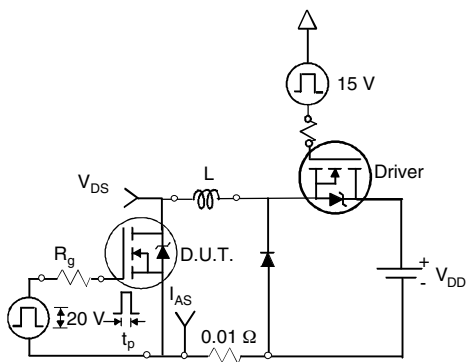


Fig. 12a - Unclamped Inductive Test Circuit

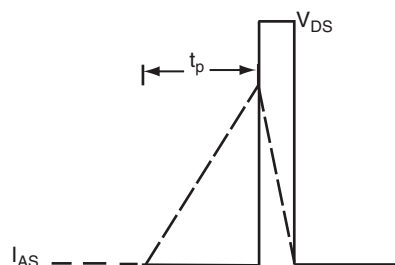


Fig. 12b - Unclamped Inductive Waveforms

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

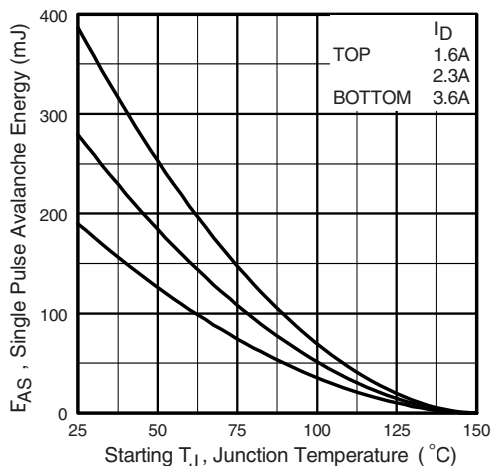


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

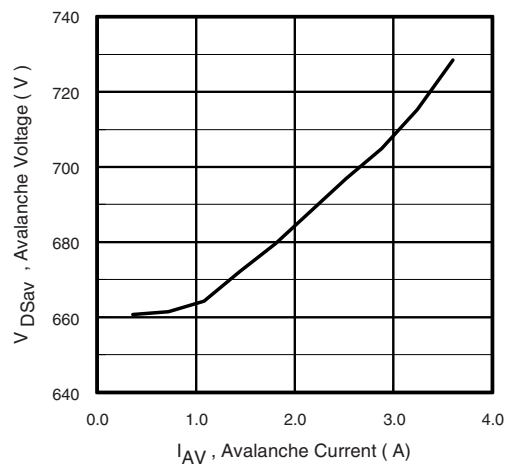


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

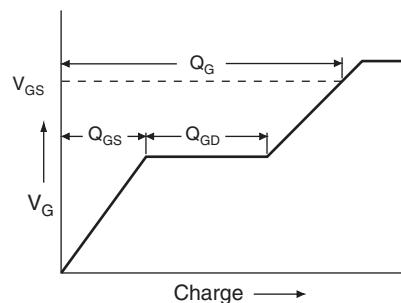


Fig. 13a - Basic Gate Charge Waveform

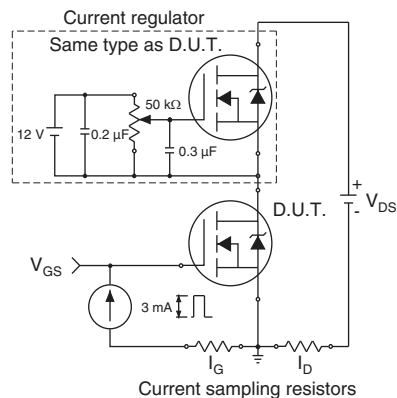
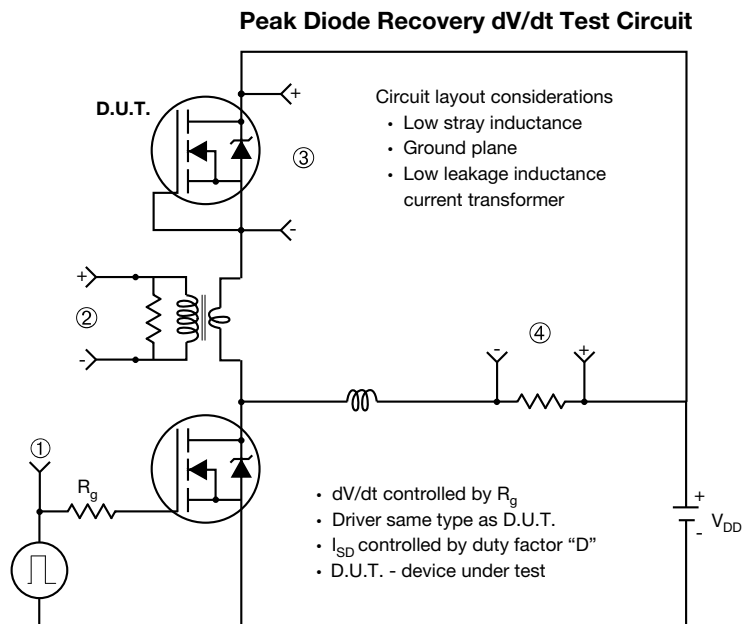


Fig. 13b - Gate Charge Test Circuit



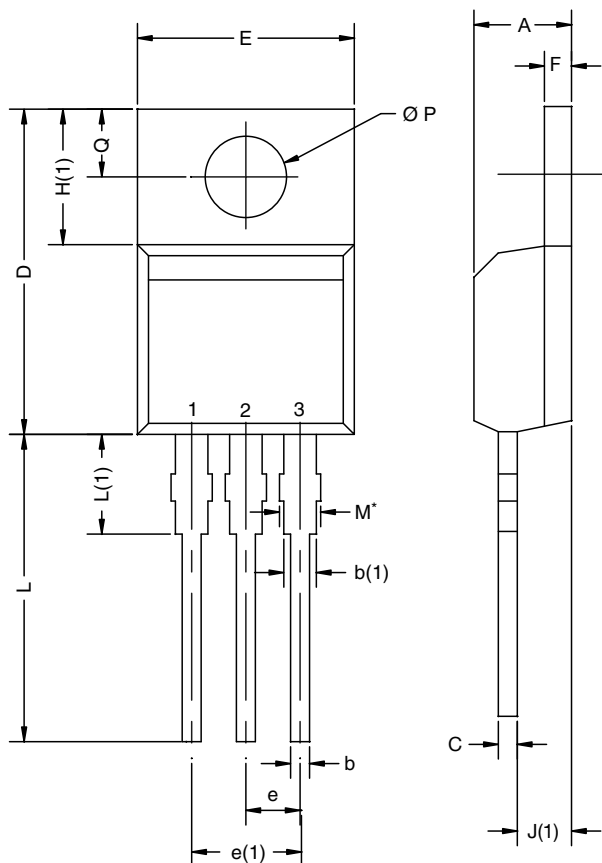
**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**



## TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

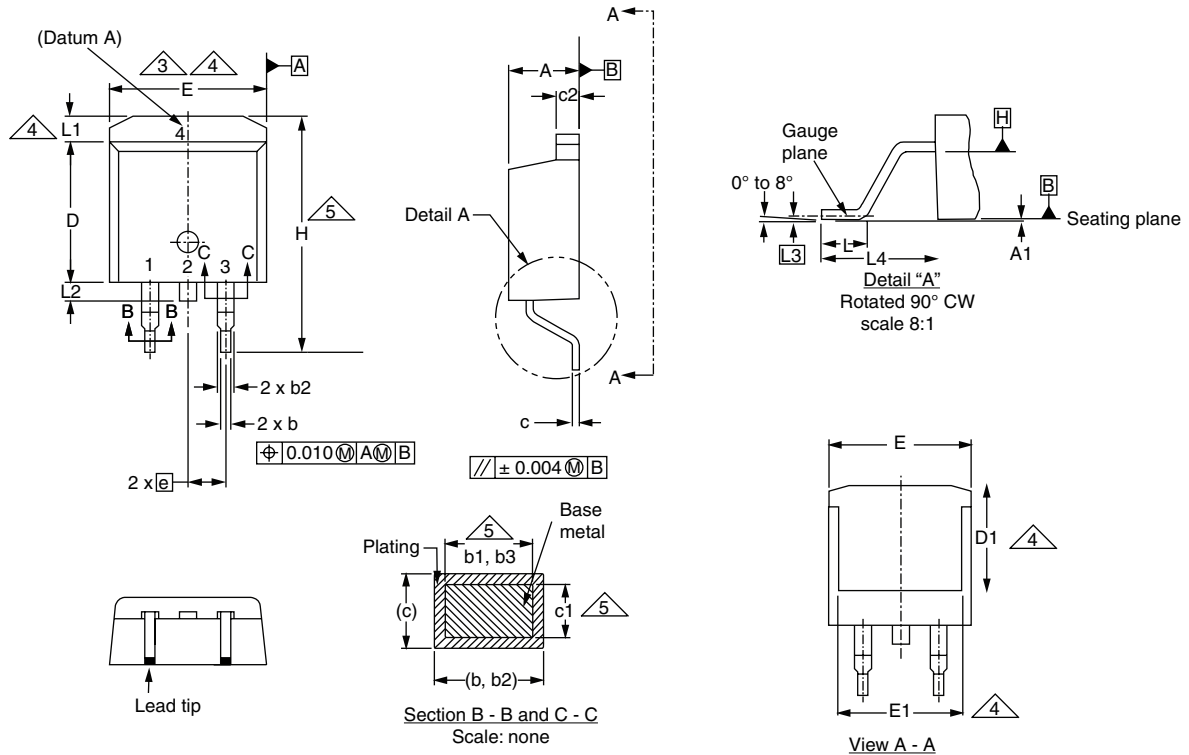
ECN: T14-0413-Rev. P, 16-Jun-14  
DWG: 5471

### Note

\*  $M = 1.32$  mm to  $1.62$  mm (dimension including protrusion)  
Heatsink hole for HVM



### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

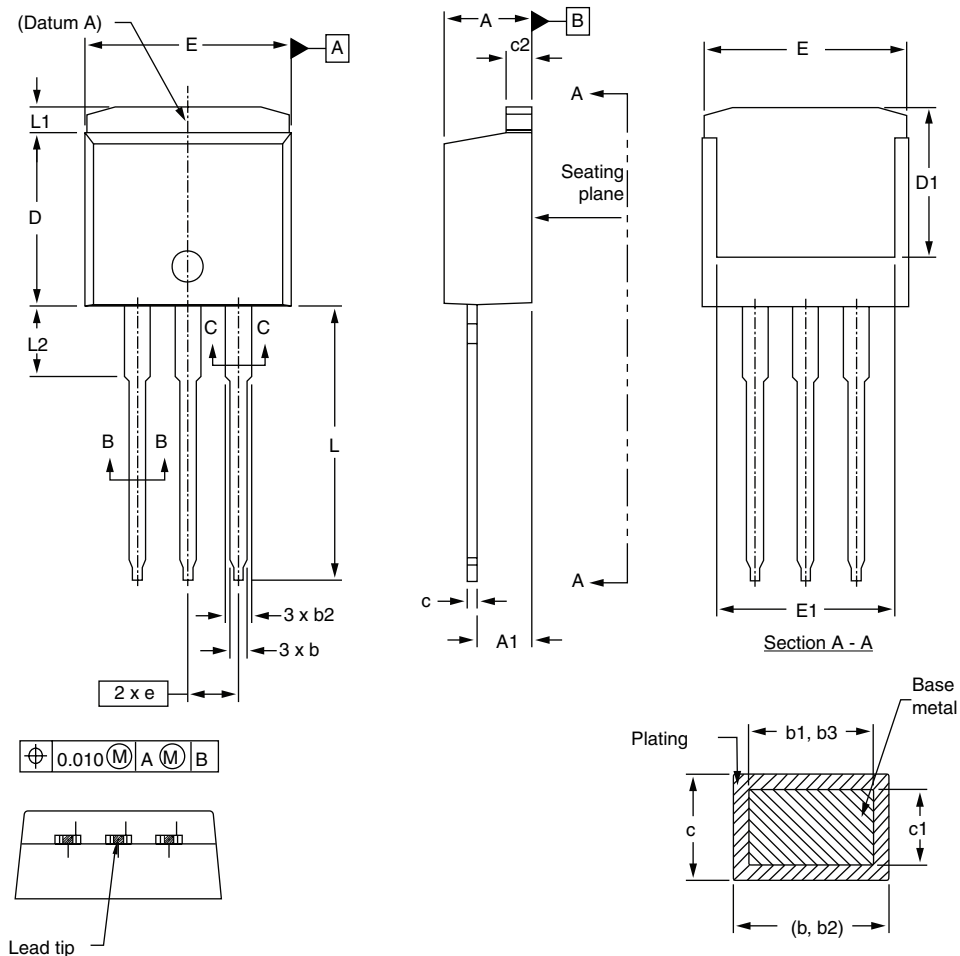
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## I<sup>2</sup>PAK (TO-262) (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

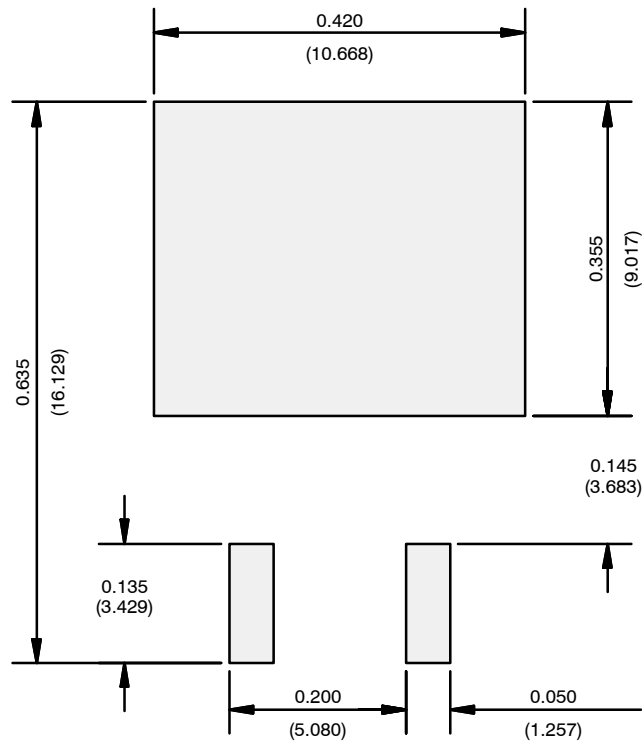
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08  
DWG: 5977

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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