

Vishay Electro-Films

## **Custom Thin Film Dual Resistor Divider Network**



#### Product may not be to scale

The STR, DTR series of dual resistor dividers provides the user with the option to specify the value, tolerance of each individual resistor and ratio tolerance.

The dual resistor dividers are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The dual resistor dividers are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

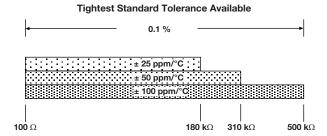
#### **FEATURES**

- Wire bondable
- Individual value and tolerance selection
- Ratio tolerance to 0.05 %
- Chip size: 0.030" x 0.030"
- Case: 0303
- Resistance range: 100  $\Omega$  to 500 k $\Omega$
- Oxidized silicon substrate for good power dissipation
- · Resistor material: Tantalum nitride, self-passivating

### **APPLICATIONS**

Vishay EFI custom-made two resistor chips are designed for hybrid packages requiring close ratio-matching and tracking of two different resistors for gain accuracy and stability. The customized resistance values give the hybrid designer greater flexibility.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	VALUE	UNIT
Total Resistance Range	100 to 500K	Ω
Standard Tolerances	± 0.1	%
TCR	± 25, ± 50, ± 100	ppm/°C



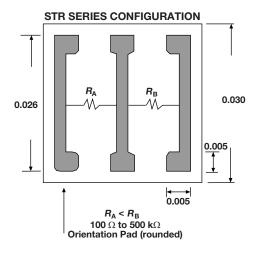
Resistance range refers only to  $R_A$  or  $R_B$ Extended value/TCR range available using nichrome version

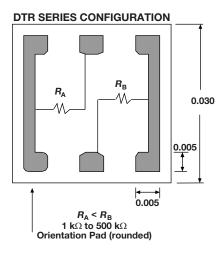
STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
TCR Tracking Between Halves (R <sub>A</sub> /R <sub>B</sub> )	± 10 (R <sub>A</sub> < 1K) ± 5 (R <sub>A</sub> ≥ 1K)	ppm/°C
Resistance Ratio Tolerance R <sub>A</sub> /R <sub>B</sub>	Customer specified to 0.05	%
Noise, MIL-STD-202, Method 308 100 $\Omega$ to 250 k $\Omega$ < 100 $\Omega$ or > 251 k $\Omega$	- 35 typ. - 20 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	$\pm$ 0.5 max. $\Delta R/R$	%
Stability, 1000 h, + 125 °C	± 0.2 max. absolute	%
Derated Power	± 0.02 max. ratio	
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. Δ <i>R</i> / <i>R</i>	%
High Temperature Exposure, + 150 °C, 100 h	± 0.2 max. Δ <i>R/R</i>	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10 <sup>12</sup> min.	Ω
Operating Voltage	100	V
DC Power Rating at 70 °C (derated to zero at + 175 °C)	0.125 each resistor	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.1 max. Δ <i>R</i> / <i>R</i>	%

Revision: 01-Sep-11 Document Number: 61032

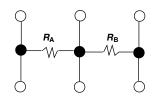
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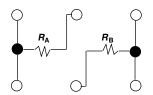
#### **DIMENSIONS** in inches



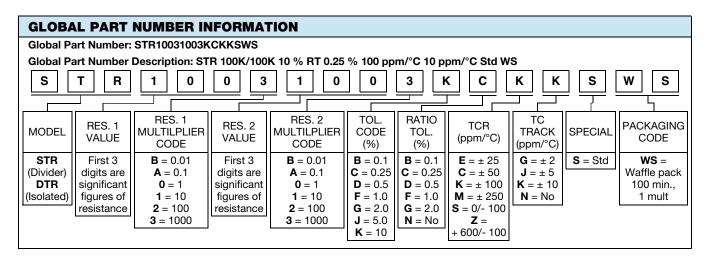


### **SCHEMATIC**





MECHANICAL SPECIFICATIONS		
PARAMETER	VALUE	
Chip Size	0.030" x 0.030" ± 0.003" (0.762 mm x 0.762 mm ± 0.05 mm)	
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)	
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO <sub>2</sub>	
Resistor Material	Tantalum nitride, self-passivating	
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm) min.	
Number of Pads	6	
Pad Material	10 kÅ minimum aluminum (Au optional)	
Backing	None, lapped semiconductor silicon (Au optional)	





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