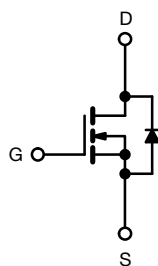
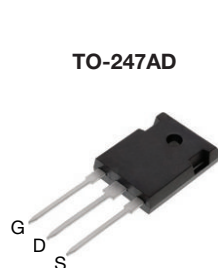


## E Series Power MOSFET



N-Channel MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.125
$Q_g$ max. (nC)	130	
$Q_{gs}$ (nC)	15	
$Q_{gd}$ (nC)	39	
Configuration	Single	

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
  - LED lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers
- Renewable energy
  - Solar (PV inverters)

### ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and Halogen-free	SiHW30N60E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	65	
Linear Derating Factor		2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	690	mJ
Maximum Power Dissipation	$P_D$	250	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$dV/dt$	70	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		18	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

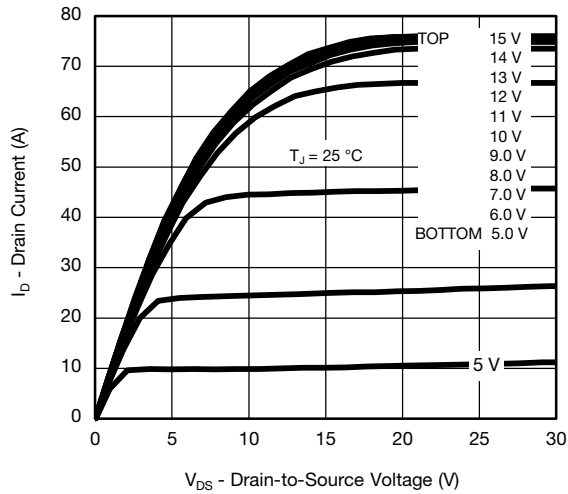
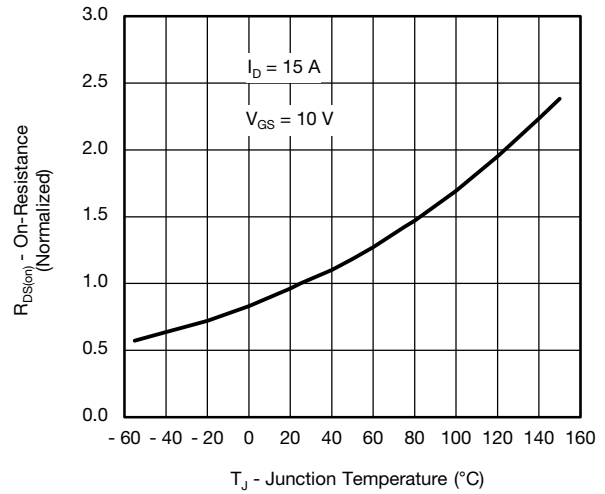
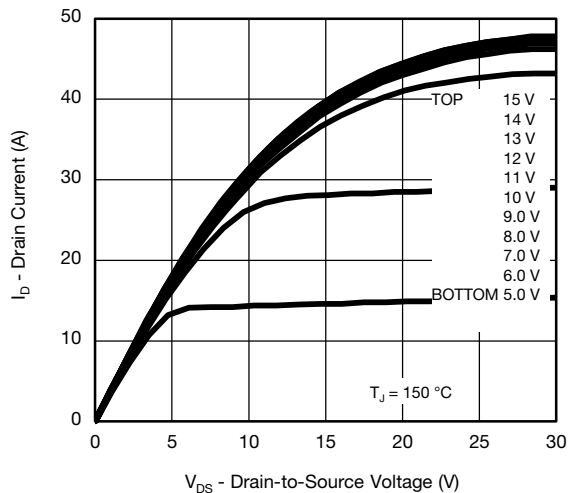
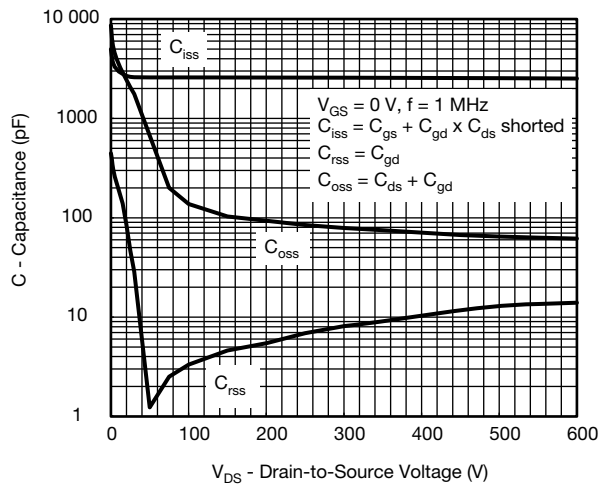
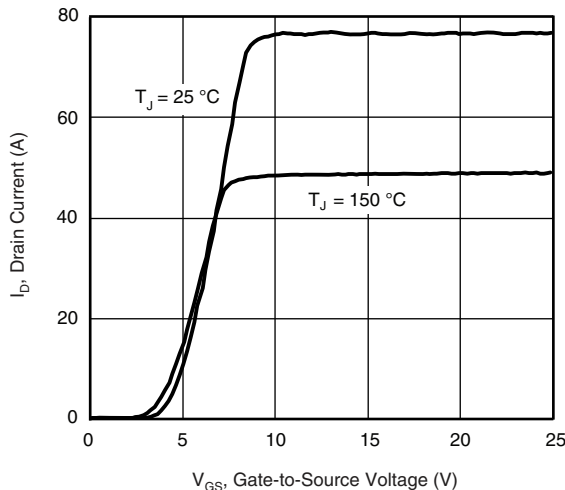
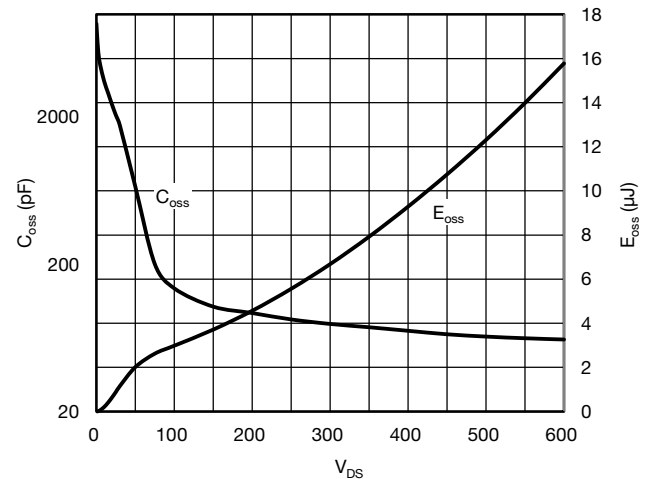
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.5	

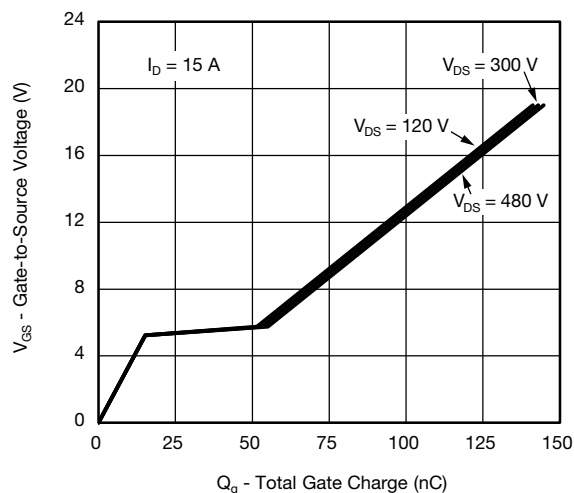
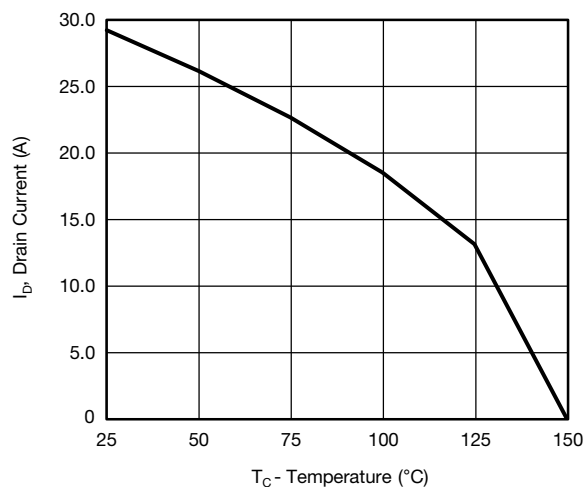
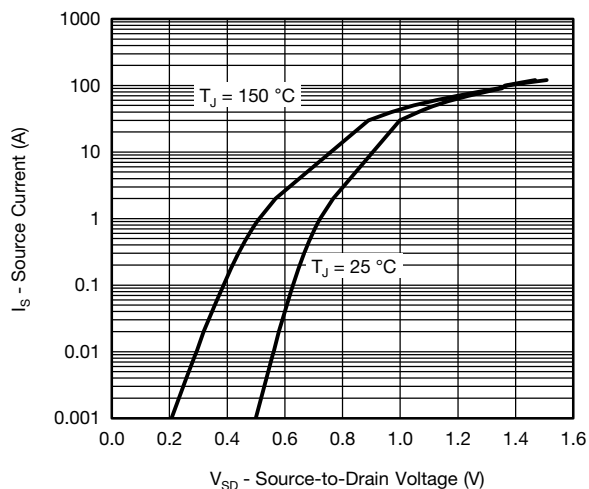
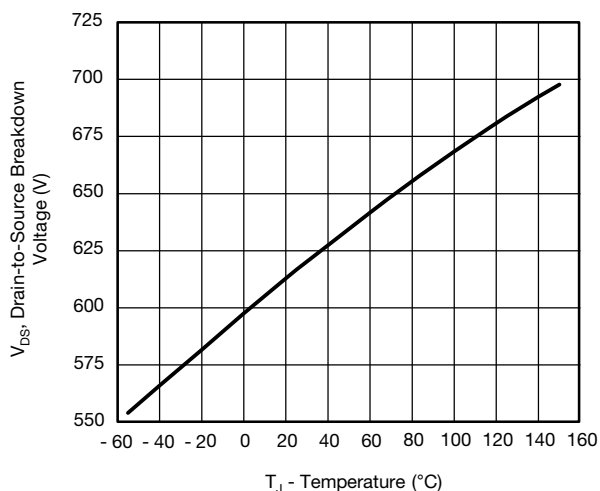
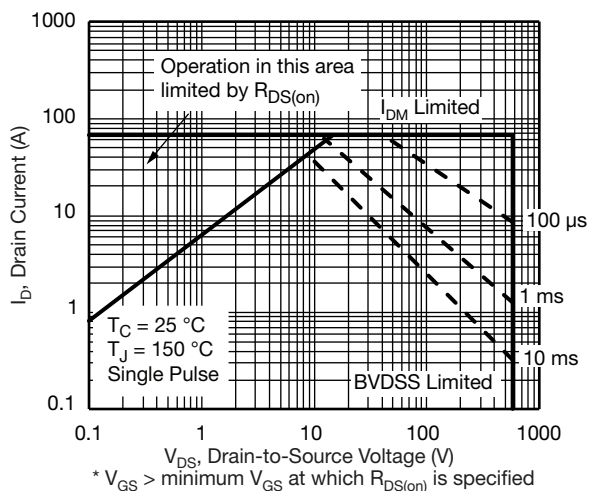
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

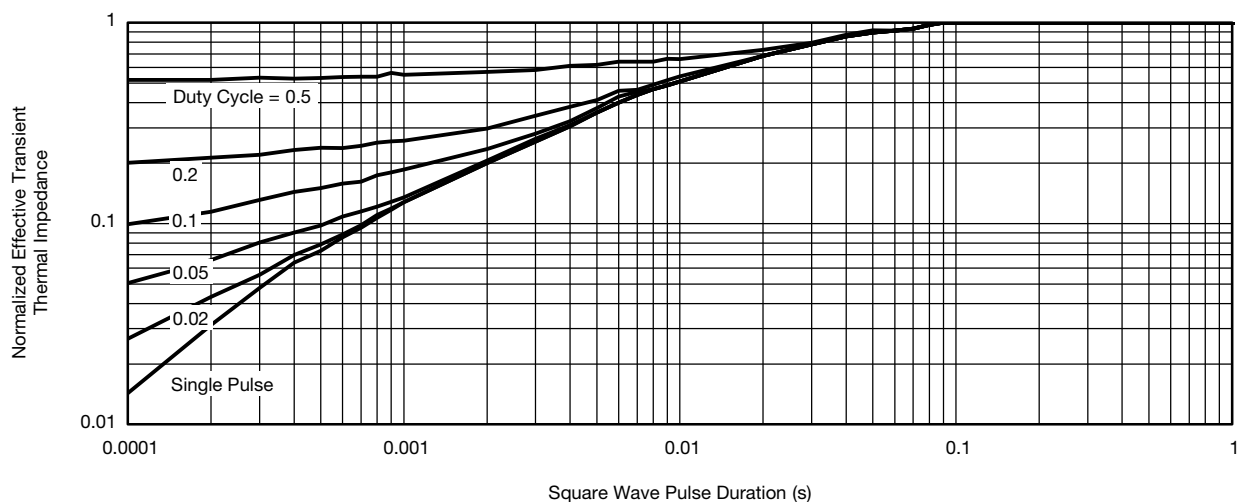
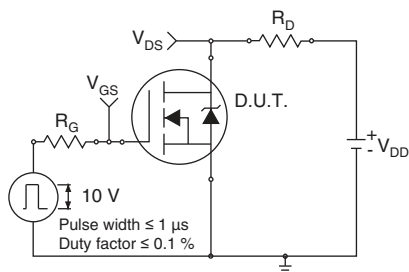
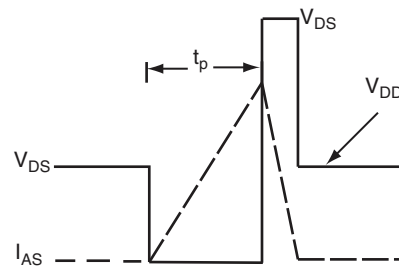
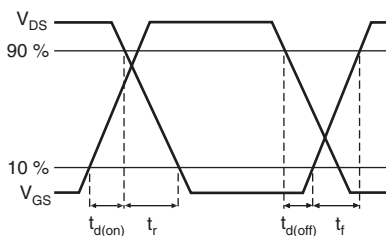
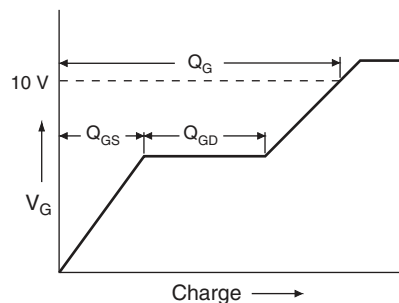
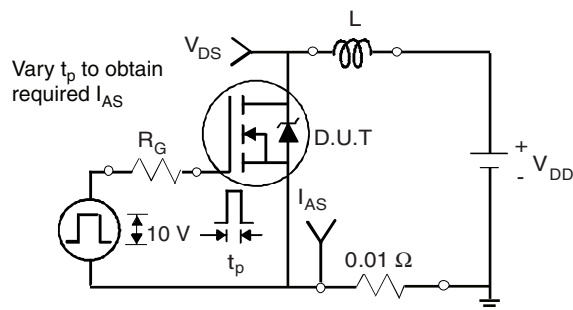
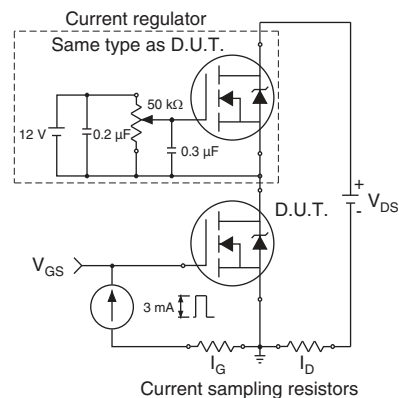
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 250 μA		-	0.64	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	2.8	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	100	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A	-	0.104	0.125	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 8 V, I <sub>D</sub> = 3 A		-	5.4	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1.0 MHz		-	2600	-	pF
Output Capacitance	C <sub>oss</sub>			-	138	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	3	-	
Effective Output Capacitance, Energy Related <sup>b</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	98	-	
Effective Output Capacitance, Time Related <sup>c</sup>	C <sub>o(tr)</sub>			-	346	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, V <sub>DS</sub> = 480 V	-	85	130	nC
Gate-Source Charge	Q <sub>gs</sub>			-	15	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	39	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 380 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 4.7 Ω		-	19	40	ns
Rise Time	t <sub>r</sub>			-	32	65	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	63	95	
Fall Time	t <sub>f</sub>			-	36	75	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.63	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	29	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	65	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 15 A, V <sub>GS</sub> = 0 V		-	-	1.3	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 15 A, dI/dt = 100 A/μs, V <sub>R</sub> = 20 V		-	402	605	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	7	15	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	32	65	A

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$
- c.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**


**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**



**Fig. 19 - For N-Channel**

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