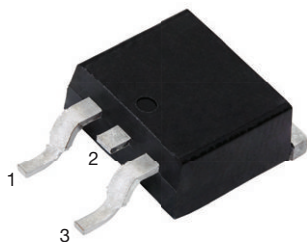
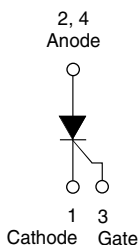


# Thyristor High Voltage Surface Mount Phase Control SCR, 10 A


**D<sup>2</sup>PAK (TO-263AB)**


## FEATURES

- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C
- Designed and qualified according JEDEC®-JESD 47
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Input rectification (soft start)
- Vishay input diodes, switches and output rectifiers which are available in identical package outlines

## DESCRIPTION

The VS-10TTS08S-M3 high voltage series of silicon controlled rectifiers are specifically designed for medium power switching and phase control applications. The glass passivation technology used has reliable operation up to 125 °C junction temperature.

## PRIMARY CHARACTERISTICS

$I_{T(AV)}$	6.5 A
$V_{DRM}/V_{RRM}$	800 V
$V_{TM}$	< 1.15 V
$I_{GT}$	15 mA
$T_J$	-40 to +125 °C
Package	D <sup>2</sup> PAK (TO-263AB)
Circuit configuration	Single SCR

## OUTPUT CURRENT IN TYPICAL APPLICATIONS

APPLICATIONS	SINGLE-PHASE BRIDGE	THREE-PHASE BRIDGE	UNITS
NEMA FR-4 or G-10 glass fabric-based epoxy with 4 oz. (140 µm) copper	2.5	3.5	A
Aluminum IMS, $R_{thCA} = 15$ °C/W	6.3	9.5	
Aluminum IMS with heatsink, $R_{thCA} = 5$ °C/W	14.0	18.5	

### Note

- $T_A = 55$  °C,  $T_J = 125$  °C, footprint 300 mm<sup>2</sup>

## MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$	Sinusoidal waveform	6.5	A
$I_{RMS}$		10	
$V_{RRM}/V_{DRM}$		800	V
$I_{TSM}$		110	A
$V_T$	6.5 A, $T_J = 25$ °C	1.15	V
dV/dt		150	V/µs
dI/dt		100	A/µs
$T_J$	Range	-40 to +125	°C

## VOLTAGE RATINGS

PART NUMBER	$V_{RRM}$ , MAXIMUM PEAK REVERSE VOLTAGE V	$V_{DRM}$ , MAXIMUM PEAK DIRECT VOLTAGE V	$I_{RRM}/I_{DRM}$ AT 125 °C mA
VS-10TTS08S-M3	800	800	1.0

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average on-state current	$I_{T(AV)}$	$T_C = 112\text{ }^{\circ}\text{C}$ , 180° conduction half sine wave	6.5	A
Maximum RMS on-state current	$I_{T(RMS)}$		10	
Maximum peak, one-cycle, non-repetitive surge current	$I_{TSM}$	10 ms sine pulse, rated $V_{RRM}$ applied, $T_J = 125\text{ }^{\circ}\text{C}$	95	
		10 ms sine pulse, no voltage reapplied, $T_J = 125\text{ }^{\circ}\text{C}$	110	
Maximum $I^2t$ for fusing	$I^2t$	10 ms sine pulse, rated $V_{RRM}$ applied, $T_J = 125\text{ }^{\circ}\text{C}$	45	$\text{A}^2\text{s}$
		10 ms sine pulse, no voltage reapplied, $T_J = 125\text{ }^{\circ}\text{C}$	64	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	$t = 0.1\text{ ms to }10\text{ ms}$ , no voltage reapplied, $T_J = 125\text{ }^{\circ}\text{C}$	640	$\text{A}^2\sqrt{\text{s}}$
Maximum on-state voltage drop	$V_{TM}$	6.5 A, $T_J = 25\text{ }^{\circ}\text{C}$	1.15	V
On-state slope resistance	$r_t$	$T_J = 125\text{ }^{\circ}\text{C}$	17.3	$\text{m}\Omega$
Threshold voltage	$V_{T(TO)}$		0.85	V
Maximum reverse and direct leakage current	$I_{RM}/I_{DM}$	$T_J = 25\text{ }^{\circ}\text{C}$	0.05	mA
		$T_J = 125\text{ }^{\circ}\text{C}$	1.0	
Typical holding current	$I_H$	Anode supply = 6 V, resistive load, initial $I_T = 1\text{ A}$ , $T_J = 25\text{ }^{\circ}\text{C}$	30	
Maximum latching current	$I_L$	Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	50	
Maximum rate of rise of off-state voltage	$dV/dt$	$T_J = T_J\text{ max.}$ , linear to 80 %, $V_{DRM} = R_g - k = \text{open}$		$\text{V}/\mu\text{s}$
Maximum rate of rise of turned-on current	$dI/dt$		100	$\text{A}/\mu\text{s}$

**TRIGGERING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	$P_{GM}$		8.0	W
Maximum average gate power	$P_{G(AV)}$		2.0	
Maximum peak positive gate current	$+I_{GM}$		1.5	A
Maximum peak negative gate voltage	$-V_{GM}$		10	V
Maximum required DC gate current to trigger	$I_{GT}$	Anode supply = 6 V, resistive load, $T_J = -65\text{ }^{\circ}\text{C}$	20	mA
		Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	15	
		Anode supply = 6 V, resistive load, $T_J = 125\text{ }^{\circ}\text{C}$	10	
Maximum required DC gate voltage to trigger	$V_{GT}$	Anode supply = 6 V, resistive load, $T_J = -65\text{ }^{\circ}\text{C}$	1.2	V
		Anode supply = 6 V, resistive load, $T_J = 25\text{ }^{\circ}\text{C}$	1	
		Anode supply = 6 V, resistive load, $T_J = 125\text{ }^{\circ}\text{C}$	0.7	
Maximum DC gate voltage not to trigger	$V_{GD}$	$T_J = 125\text{ }^{\circ}\text{C}$ , $V_{DRM} = \text{rated value}$	0.2	mA
Maximum DC gate current not to trigger	$I_{GD}$		0.1	

**SWITCHING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Typical turn-on time	$t_{gt}$	$T_J = 25\text{ }^{\circ}\text{C}$	0.8	$\mu\text{s}$
Typical reverse recovery time	$t_{rr}$	$T_J = 125\text{ }^{\circ}\text{C}$	3	
Typical turn-off time	$t_q$		100	

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-40 to +125	°C
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation	1.5	°C/W
Typical thermal resistance, junction to ambient (PCB mount)	$R_{thJA}^{(1)}$		40	
Approximate weight			2	g
			0.07	oz.
Marking device		Case style D <sup>2</sup> PAK (TO-263AB)	10TTS08S	

**Note**

(1) When mounted on 1" square (650 mm<sup>2</sup>) PCB of FR-4 or G-10 material 4 oz. (140 μm) copper 40 °C/W.  
For recommended footprint and soldering techniques refer to application note #AN-994

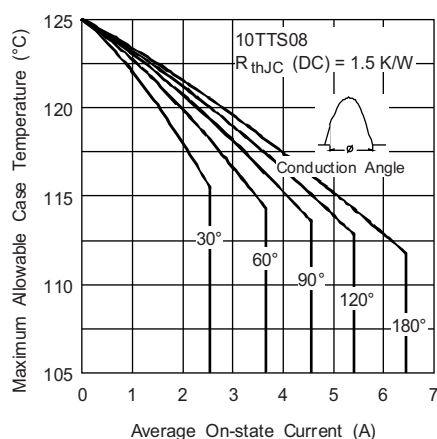


Fig. 1 - Current Rating Characteristics

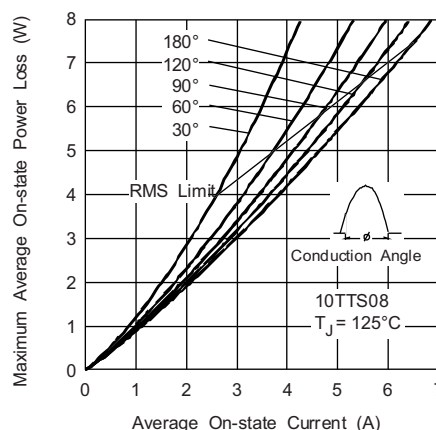


Fig. 3 - On-State Power Loss Characteristics

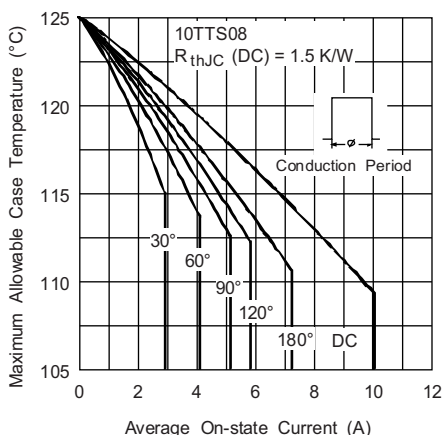


Fig. 2 - Current Rating Characteristics

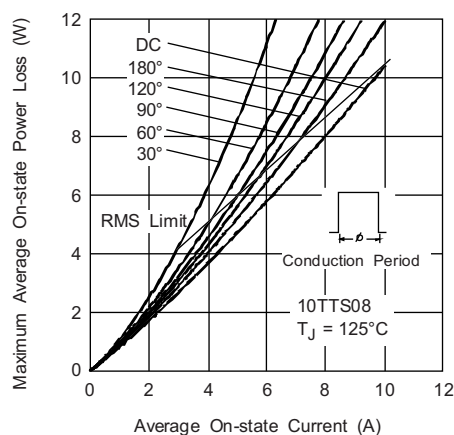


Fig. 4 - On-State Power Loss Characteristics

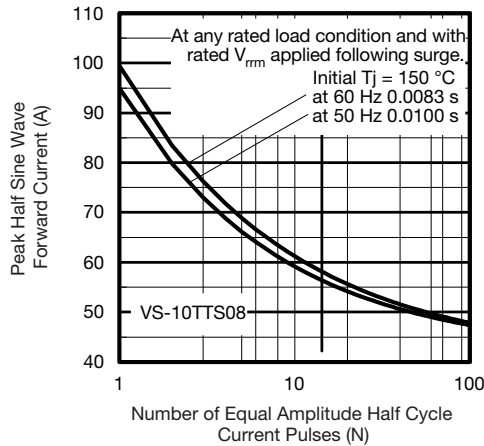


Fig. 5 - Maximum Non-Repetitive Surge Current

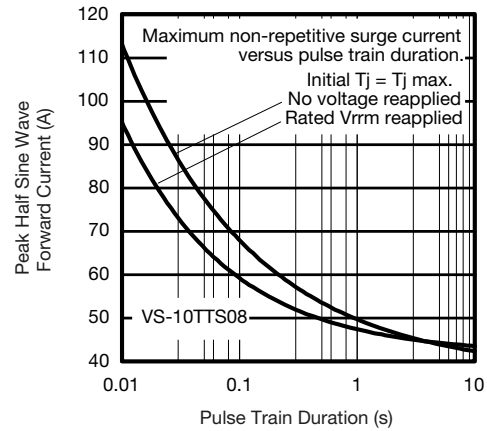


Fig. 6 - Maximum Non-Repetitive Surge Current

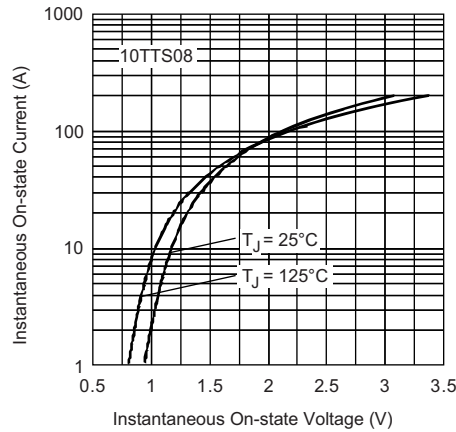
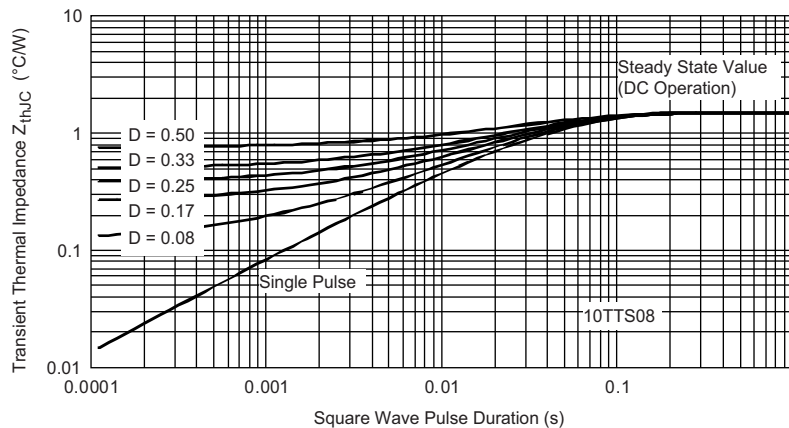


Fig. 7 - On-State Voltage Drop Characteristics


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

## ORDERING INFORMATION TABLE

<b>VS-</b>	<b>10</b>	<b>T</b>	<b>T</b>	<b>S</b>	<b>08</b>	<b>S</b>	<b>TRL</b>	<b>-M3</b>
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**1** - Vishay Semiconductors product

**2** - Current rating, RMS value

**3** - Circuit configuration:  
T = single thyristor

**4** - Package:  
T = D<sup>2</sup>PAK (TO-263AB)

**5** - Type of silicon:  
S = converter grade

**6** - Voltage code x 100 =  $V_{RRM}$

**7** - S = surface mountable

**8** - Tape and reel option:  
• TRL = tape and reel (left oriented)  
• TRR = tape and reel (right oriented)

**9** - -M3 = halogen-free, RoHS-compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (Example)		
PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-10TTS08S-M3	50	Antistatic plastic tubes
VS-10TTS08STRL-M3	800	13" diameter plastic tape and reel
VS-10TTS08STRR-M3	800	13" diameter plastic tape and reel

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?96164">www.vishay.com/doc?96164</a>
Part marking information	<a href="http://www.vishay.com/doc?95444">www.vishay.com/doc?95444</a>
Packaging information	<a href="http://www.vishay.com/doc?96424">www.vishay.com/doc?96424</a>



## D<sup>2</sup>PAK

### DIMENSIONS in millimeters and inches

Conforms to JEDEC® outline D<sup>2</sup>PAK (SMD-220)


SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L2	1.27	1.78	0.050	0.070	
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

#### Notes

- Dimensioning and tolerancing per ASME Y14.5 M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- Thermal pad contour optional within dimension E, L1, D1 and E1
- Dimension b1 and c1 apply to base metal only
- Datum A and B to be determined at datum plane H
- Controlling dimension: inches
- Outline conforms to JEDEC® outline TO-263AB



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