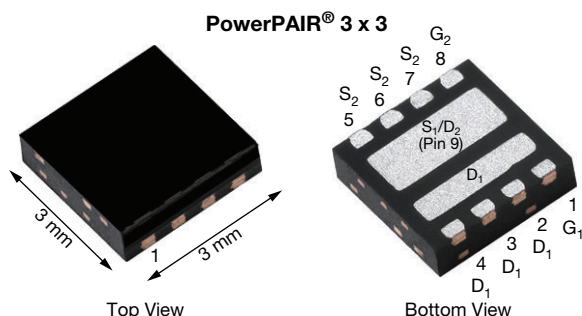


Dual N-Channel 30 V (D-S) MOSFET



FEATURES

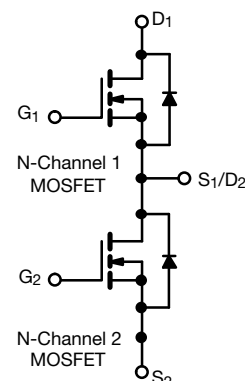
- TrenchFET® Gen IV power MOSFET
- High side and low side MOSFETs form optimized combination for 50 % duty cycle
- Optimized $R_{DS(on)}$ - Q_g and $R_{DS(on)}$ - Q_{gd} FOM elevates efficiency for high frequency switching
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL



PRODUCT SUMMARY

V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00965
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0145
Q_g typ. (nC)	4
I_D (A)	32.9 ^a
Configuration	Dual

ORDERING INFORMATION

Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ342BDT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20 / -16	V
Continuous drain current ($T_J = 150$ °C)	I_D	32.9	A
		26.3	
		15.4 ^{b, c}	
		12.3 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	100	A
Continuous source current (MOSFET diode conduction)	I_S	13.9	A
		3.1 ^{b, c}	
Single pulse avalanche current	I_{AS}	10	A
Single pulse avalanche energy	E_{AS}	5	mJ
Maximum power dissipation	P_D	16.7	W
		10.7	
		3.7 ^{b, c}	
		2.4 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)		260	°C

Notes

- a. $T_C = 25$ °C
b. Surface mounted on 1" x 1" FR4 board
c. $t = 10$ s

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	27	34	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	6	7.5	

Notes

a. Surface mounted on 1" x 1" FR4 board

b. Maximum under steady state conditions is 69 °C/W

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.4	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 V / -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.0071	0.00965	Ω
		V _{GS} = 4.5 V, I _D = 7 A	-	0.011	0.0145	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 10 A	-	30	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	550	-	pF
Output capacitance	C _{oss}		-	230	-	
Reverse transfer capacitance	C _{rss}		-	30	-	
C _{rss} /C _{iss} ratio			-	0.054	0.110	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15 A	-	8.4	12.6	nC
Gate-source charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A	-	4	6	
Gate-drain charge	Q _{gd}		-	2.2	-	
Gate resistance	R _g		-	1.0	-	
Turn-on delay time	t _{d(on)}	f = 1 MHz	0.2	1	2	Ω
Rise time	t _r	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	8	20	ns
Turn-off delay time	t _{d(off)}		-	6	12	
Fall time	t _f		-	18	36	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	5	10	
Rise time	t _r		-	15	25	
Turn-off delay time	t _{d(off)}		-	450	675	
Turn-off delay time	t _{d(off)}		-	10	20	
Fall time	t _f		-	14	28	
Drain-source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25°C	-	-	13.9	A
Pulse diode forward current	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 8 A, V _{GS} = 0 V	-	0.83	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	21	42	ns
Body diode reverse recovery charge	Q _{rr}		-	11	22	nC
Reverse recovery fall time	t _a		-	11	-	ns
Reverse recovery rise time	t _b		-	10	-	

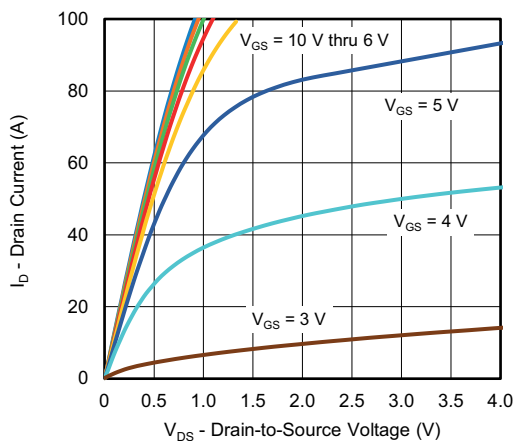
Notesa. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

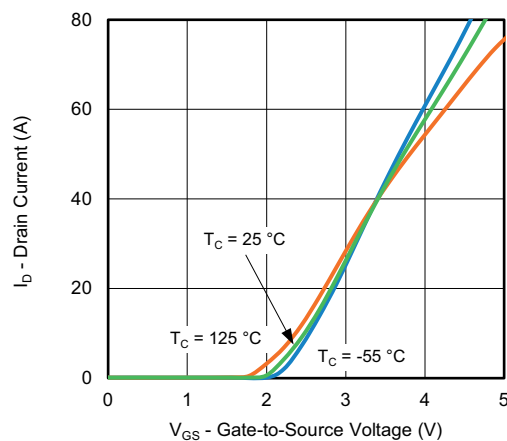
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



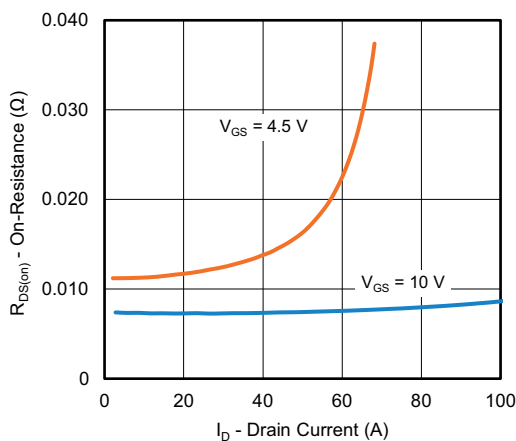
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



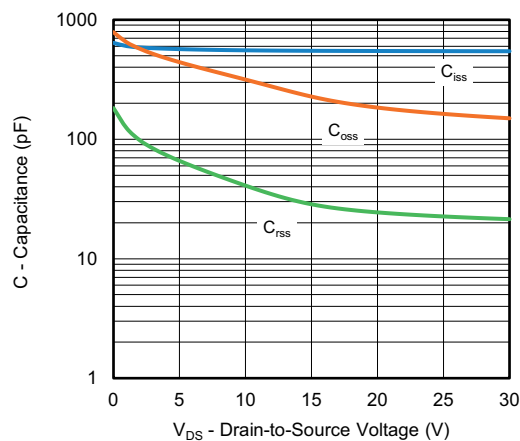
Output Characteristics



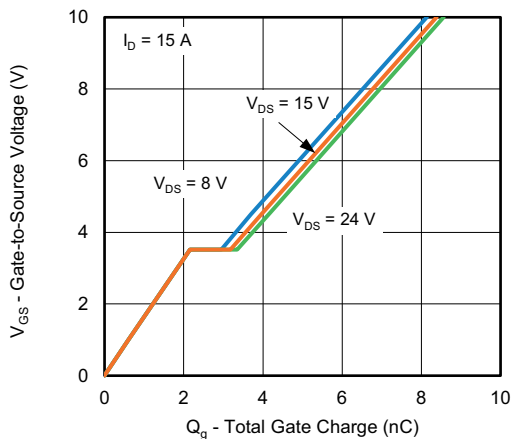
Transfer Characteristics



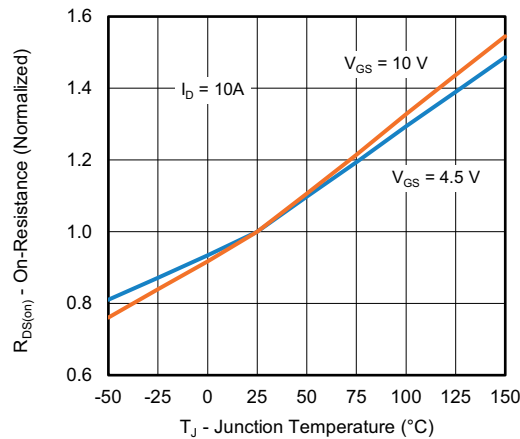
On-Resistance vs. Drain Current and Gate



Capacitance



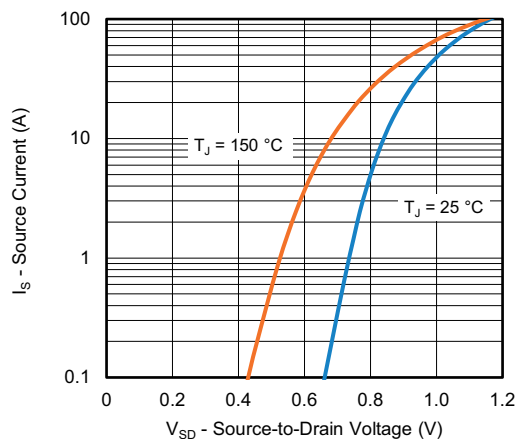
Gate Charge



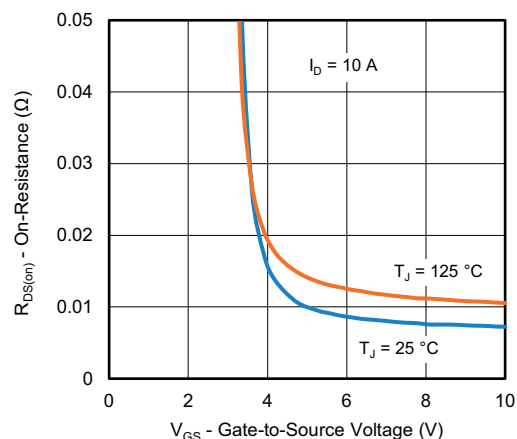
On-Resistance vs. Junction Temperature



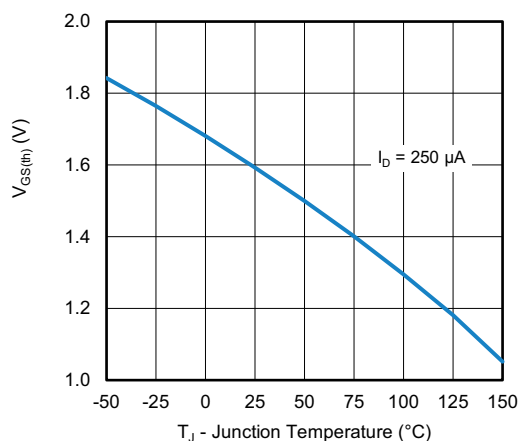
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



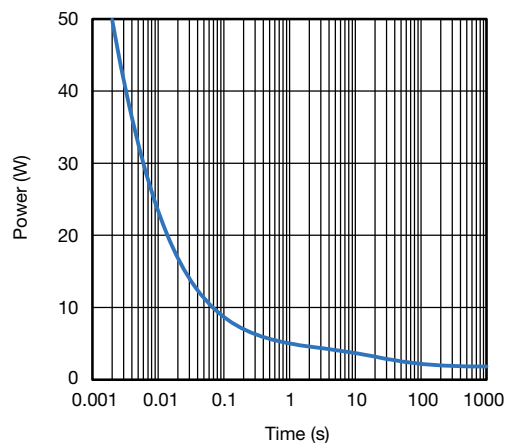
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



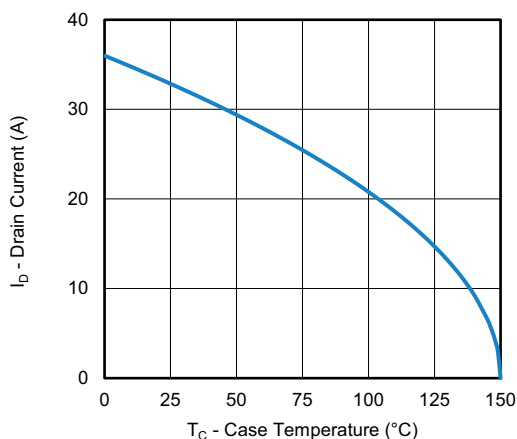
Threshold Voltage



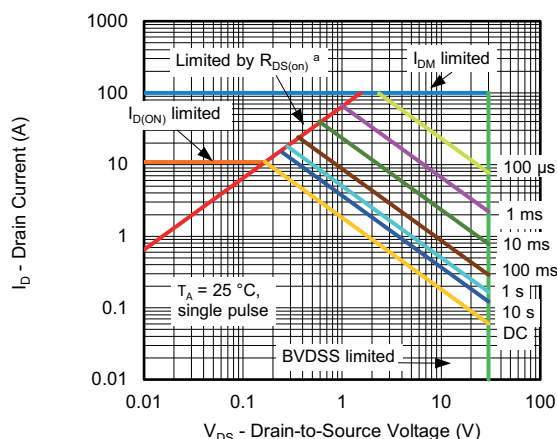
Single Pulse Power



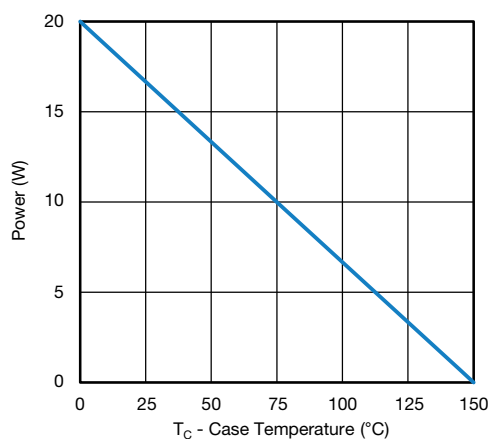
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



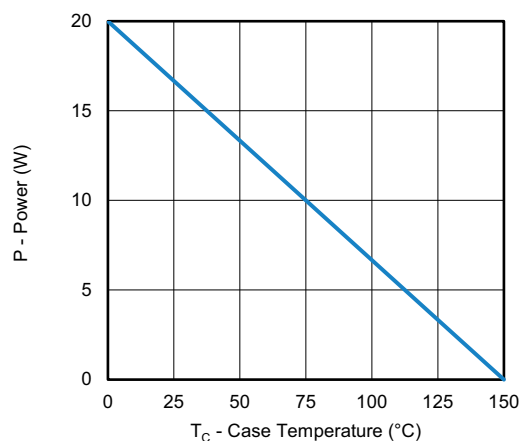
Current Derating ^a



Safe Operating Area, Junction-to-Ambient



Power, Junction-to-Case



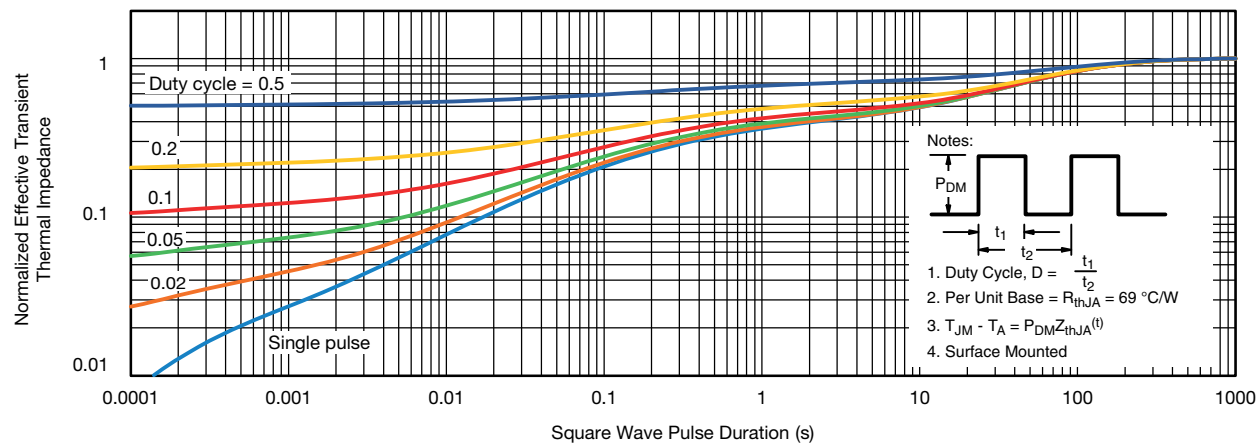
Power, Junction-to-Ambient

Notes

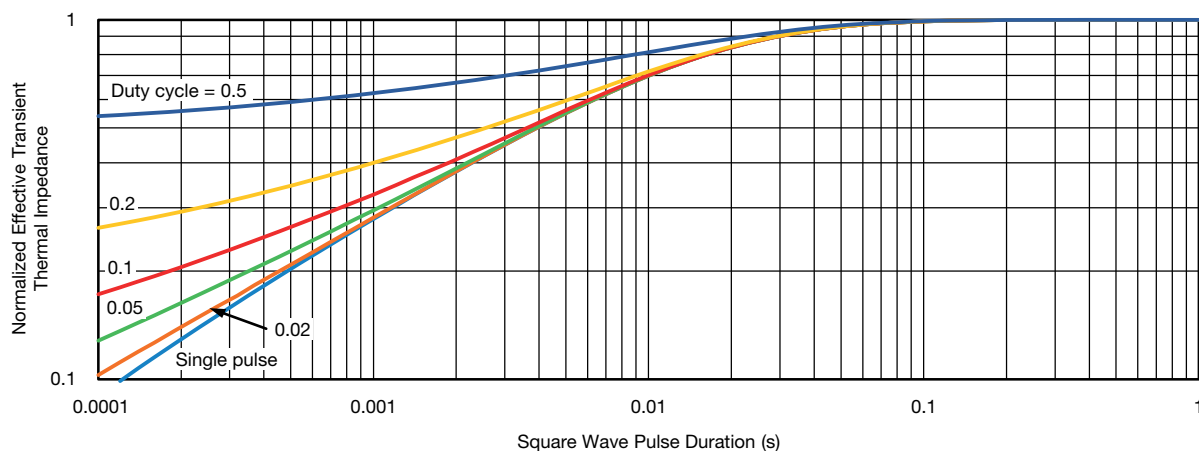
- The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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