

Vishay Siliconix



# N-Channel 25 V (D-S) MOSFET



PRODUCT SUMMARY						
V <sub>DS</sub> (V)	25					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0086					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0095					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	0.0115					
Q <sub>g</sub> typ. (nC)	17.5					
I <sub>D</sub> (A) <sup>a</sup>	18					
Configuration	Single					

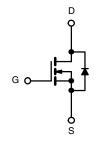
### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



### **APPLICATIONS**

- Synchronous buck
  - Low side



N-Channel MOSFET

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free	Si4116DY-T1-E3
Lead (Pb)-free and halogen-free	Si4116DY-T1-GE3

ABSOLUTE MAXIMUM RATING	10 (. <sub>A</sub> 20 0, c	T T		
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	25	V
Gate-source voltage		$V_{GS}$	± 12	V
	T <sub>C</sub> = 25 °C		18	
Continuous drain augrent (T. 150 °C)	T <sub>C</sub> = 70 °C	1 ,	14.3	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	12.7 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		10.1 <sup>b, c</sup>	^
Pulsed drain current		I <sub>DM</sub>	50	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		4.5	
	T <sub>A</sub> = 25 °C	l <sub>s</sub>	2.2 b, c	
Single pulse avalanche current	1 0.1 ml l	I <sub>AS</sub>	20	
Avalanche energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		5	
	T <sub>C</sub> = 70 °C		3.2	10/
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b, d	t ≤ 10 s	R <sub>thJA</sub>	43	50	°C/W	
Maximum junction-to-foot (drain)	Steady state	$R_{thJF}$	19	25	C/VV	

### Notes

- a. Based on T<sub>C</sub> = 25 °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. Maximum under steady state conditions is 95 °C/W

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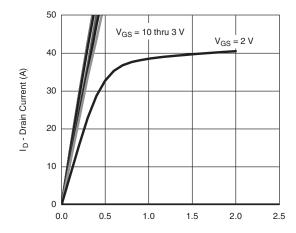
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I - 250 uA	-	30	-	mV/°C	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4	-		
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6	-	1.4	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 100	nA	
Zara gata valtaga drain avurant		V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V			1	_	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.0071	0.0086	Ω	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7 A	-	0.0078	0.0095		
		$V_{GS} = 2.5 \text{ V}, I_D = 5 \text{ A}$	-	0.0090	0.0115		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	-	68	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	1925	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	305	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	135	-		
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	37	56	nC	
Total gate charge	Qg	, <del>, , , , , , , , , , , , , , , , , , </del>	-	17.5	27		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	3.7	-		
Gate-drain charge	Q <sub>gd</sub>		-	3.3	-		
Gate resistance	$R_g$	f = 1 MHz	-	1.6	3	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	13	25		
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_1 = 1.5 \Omega$	-	11	20		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$	-	50	90		
Fall time	t <sub>f</sub>		-	15	30		
Turn-on delay time	t <sub>d(on)</sub>		-	7	14	ns	
Rise time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$	-	10	20	İ	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	31	55		
Fall time	t <sub>f</sub>		-	9	18		
<b>Drain-Source Body Diode Characterist</b>	ics		1				
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	4.5		
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>		-	-	50	Α	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A	-	0.69	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>	-	-	26	45	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	16	30	nC	
Reverse recovery fall time	t <sub>a</sub>	Т <sub>J</sub> = 25 °C	-	13	-		
Reverse recovery rise time	t <sub>b</sub>		_	13	-	ns	

### Notes

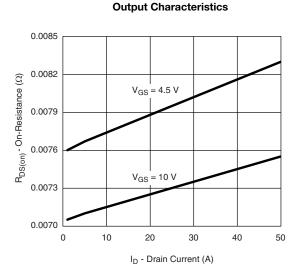
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

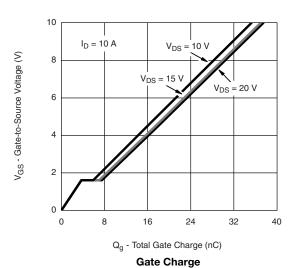


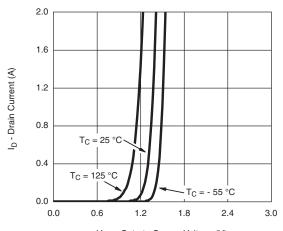


 $V_{\mbox{\footnotesize DS}}$  - Drain-to-Source Voltage (V)



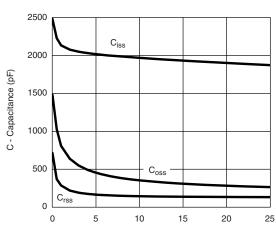
On-Resistance vs. Drain Current and Gate Voltage





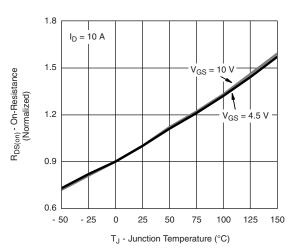
 $V_{GS}$  - Gate-to-Source Voltage (V)

### **Transfer Characteristics**



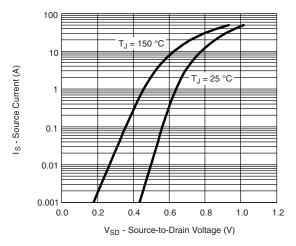
V<sub>DS</sub> - Drain-to-Source Voltage (V)

### Capacitance

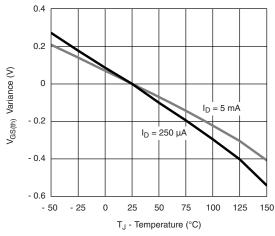


On-Resistance vs. Junction Temperature

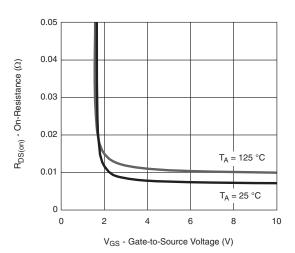




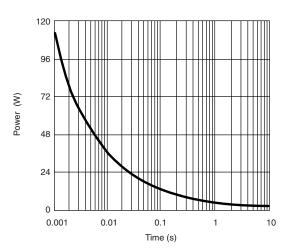
### Source-Drain Diode Forward Voltage



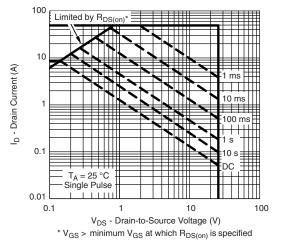
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

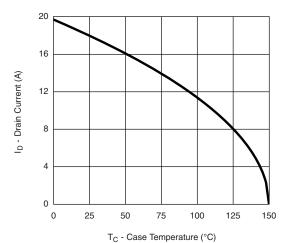


Single Pulse Power, Junction-to-Ambient

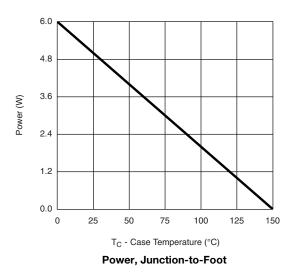


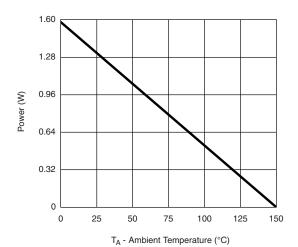
Safe Operating Area, Junction-to-Ambient





Current Derating a



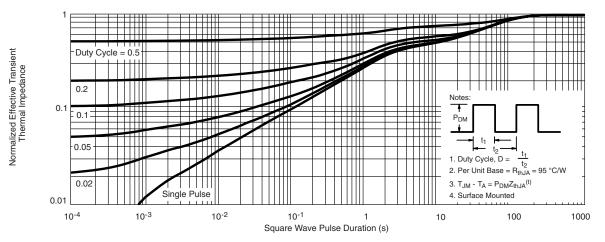


Power, Junction-to-Ambient

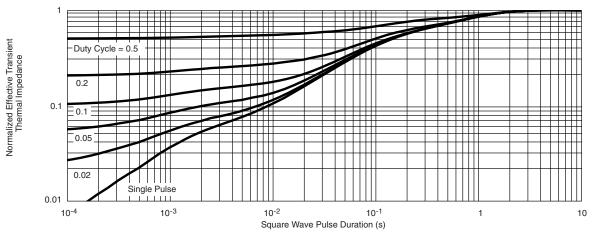
### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

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# LON NOTE



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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