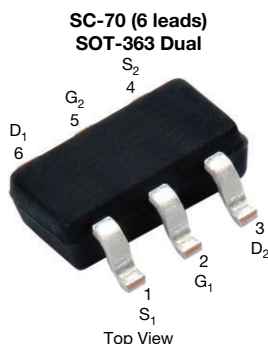


# Dual N-Channel 20 V (D-S) MOSFET



Marking code: PE

PRODUCT SUMMARY	
$V_{DS}$ (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.235
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5$ V	0.306
$Q_g$ typ. (nC)	0.9
$I_D$ (A) <sup>a</sup>	1.1
Configuration	Dual

## FEATURES

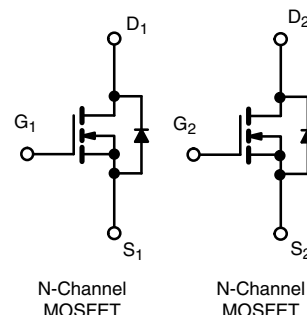
- TrenchFET® power MOSFET
- 100 %  $R_g$  tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- Load switch and DC/DC converter for portable devices
- High speed switching



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



ORDERING INFORMATION	
Package	SC-70
Lead (Pb)-free and halogen-free	Si1902CDL-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	20	V	
Gate-source voltage	$V_{GS}$	$\pm 12$		
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	1.1	A	
	$T_C = 70$ °C	0.9		
	$T_A = 25$ °C	1 <sup>b, c</sup>		
	$T_A = 70$ °C	0.8 <sup>b, c</sup>		
Pulsed drain current ( $t = 300$ $\mu$ s)	$I_{DM}$	2		
Continuous source-drain diode current	$T_C = 25$ °C	0.35		
	$T_A = 25$ °C	0.25 <sup>b, c</sup>		
Maximum power dissipation	$T_C = 25$ °C	0.42	W	
	$T_C = 70$ °C	0.27		
	$T_A = 25$ °C	0.30 <sup>b, c</sup>		
	$T_A = 70$ °C	0.23 <sup>b, c</sup>		
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, d</sup>	$t \leq 5$ s	$R_{thJA}$	290	350	°C/W
Maximum junction-to-foot (drain)	Steady state	$R_{thJF}$	250	300	

## Notes

- Based on  $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 5$  s
- Maximum under steady state conditions is 410 °C/W



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	25	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-2.6	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6	-	1.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C	-	-	10	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	2	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1 A	-	0.195	0.235	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 0.3 A	-	0.255	0.306	
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A	-	3	-	ms
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	62	-	pF
Output capacitance	C <sub>oss</sub>		-	20	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	7	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A	-	2	3	nC
		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1 A	-	0.9	1.4	
Gate-source charge	Q <sub>gs</sub>		-	0.2	-	
Gate-drain charge	Q <sub>gd</sub>		-	0.2	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	2.4	12	24	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 12.5 Ω I <sub>D</sub> ≅ 0.8 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	4	8	ns
Rise time	t <sub>r</sub>		-	13	20	
Turn-off delay time	t <sub>d(off)</sub>		-	11	20	
Fall time	t <sub>f</sub>		-	9	18	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 12.5 Ω I <sub>D</sub> ≅ 0.8 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	6	12	
Rise time	t <sub>r</sub>		-	16	24	
Turn-off delay time	t <sub>d(off)</sub>		-	13	20	
Fall time	t <sub>f</sub>		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	0.35	A
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>		-	-	2	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.8 A	-	0.8	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 0.8 A, di/dt = 100 A/μs	-	2	4	nC
Body diode reverse recovery charge	Q <sub>rr</sub>		-	8	16	ns
Reverse recovery fall time	t <sub>a</sub>		-	5	-	
Reverse recovery rise time	t <sub>b</sub>		-	3	-	

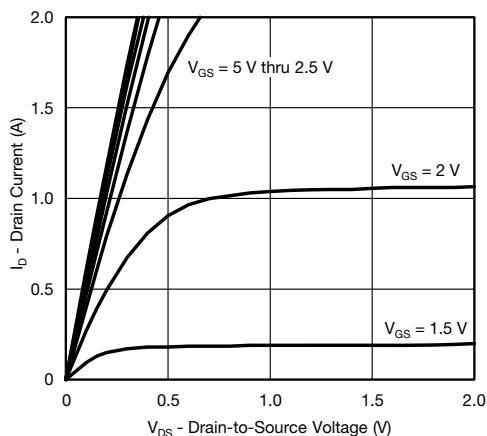
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

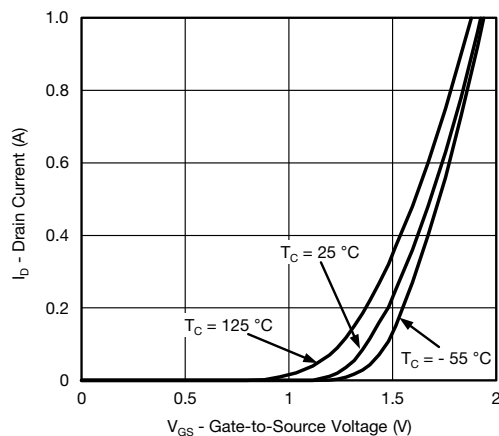
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



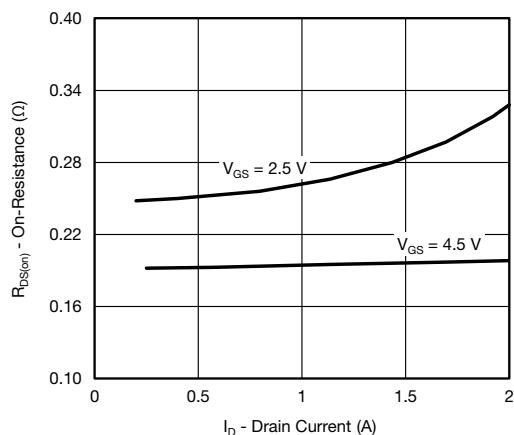
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



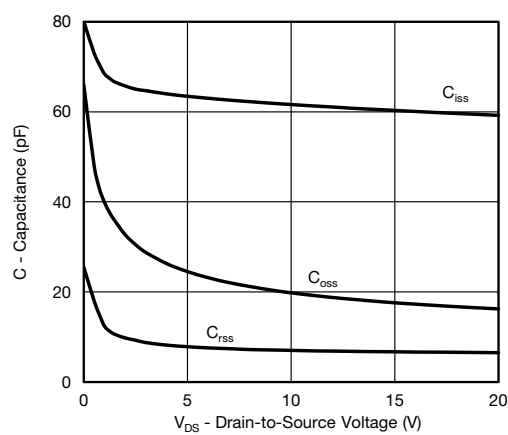
**Output Characteristics**



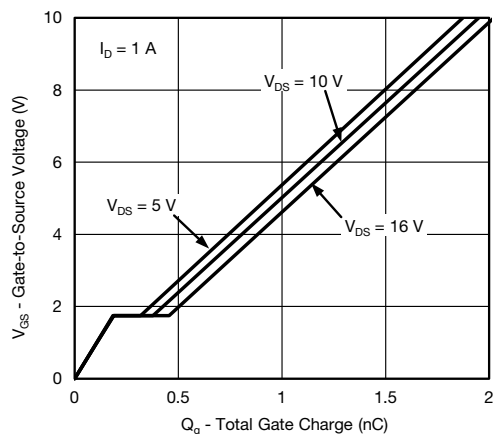
**Transfer Characteristics**



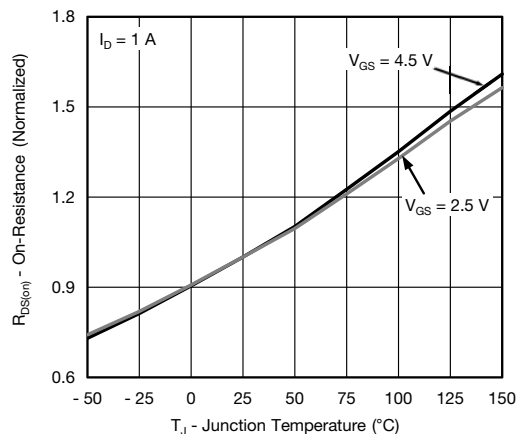
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



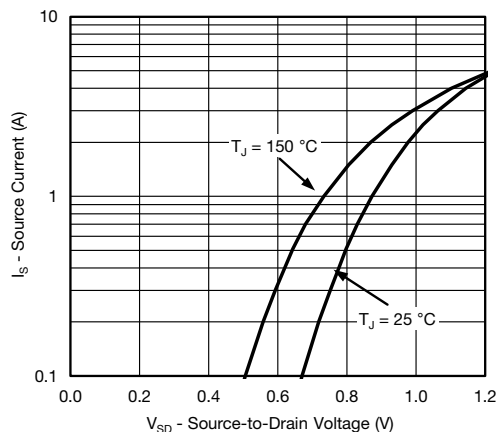
**Gate Charge**



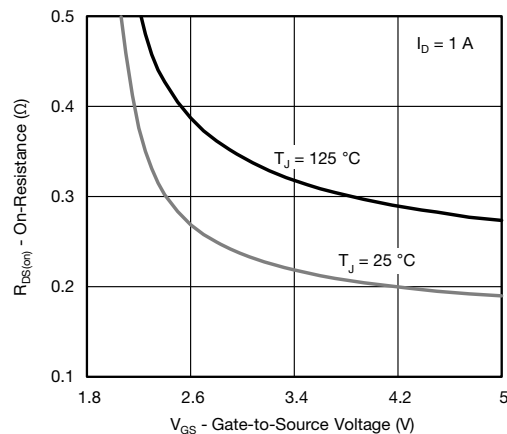
**On-Resistance vs. Junction Temperature**



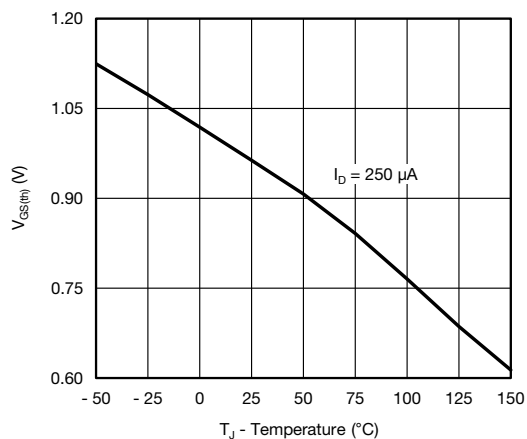
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



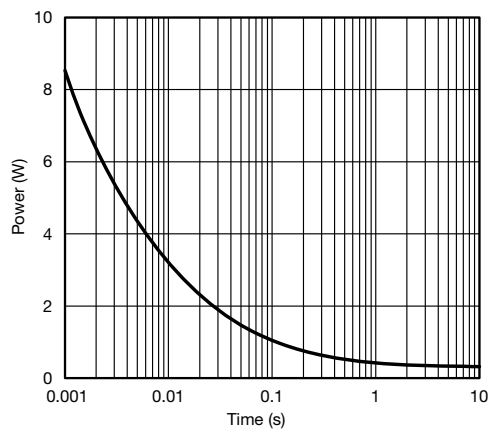
**Source-Drain Diode Forward Voltage**



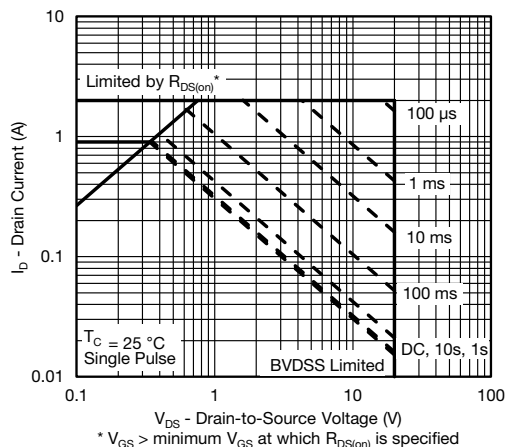
**On-Resistance vs. Gate-to-Source Voltage**



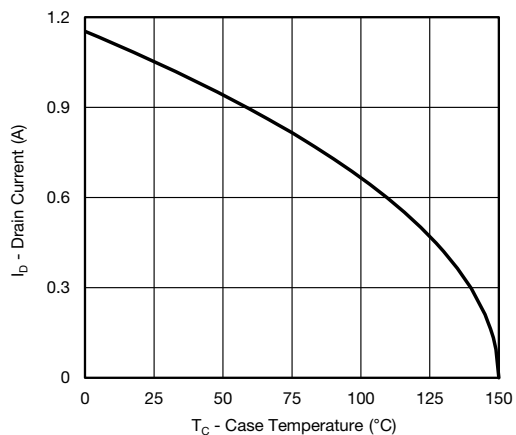
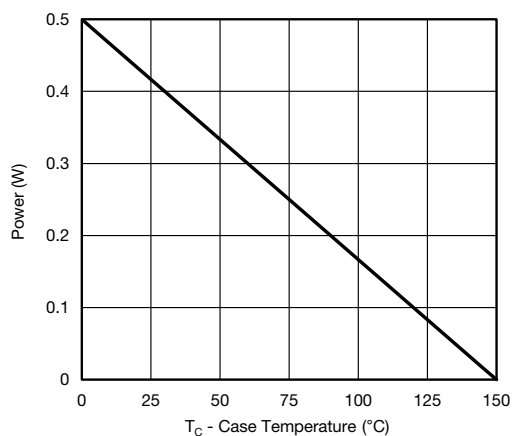
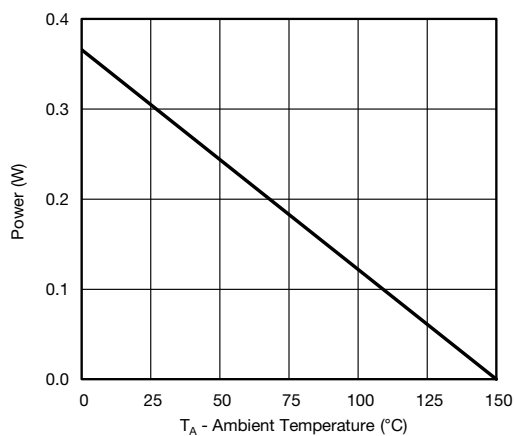
**Threshold Voltage**



**Single Pulse Power (Junction-to-Ambient)**



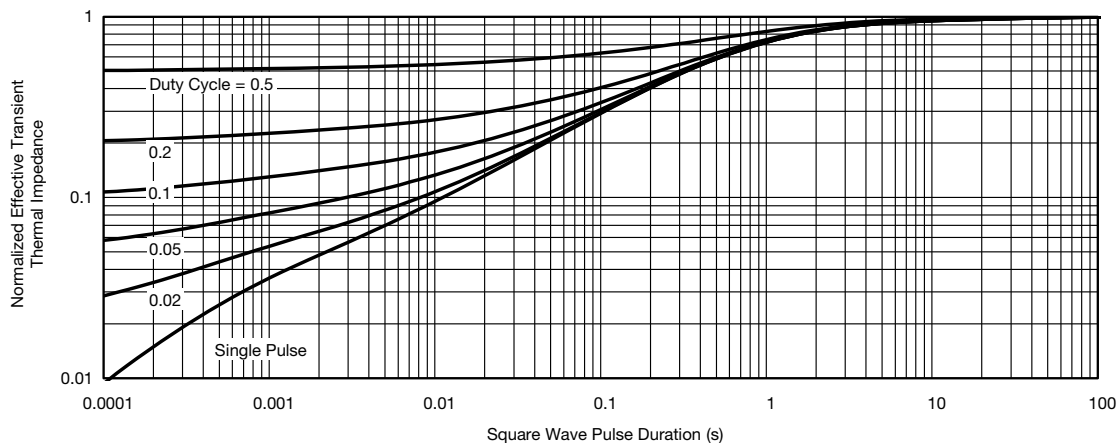
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating <sup>a</sup>**

**Power Derating, Junction-to-Foot**

**Power Derating, Junction-to-Ambient**
**Note**

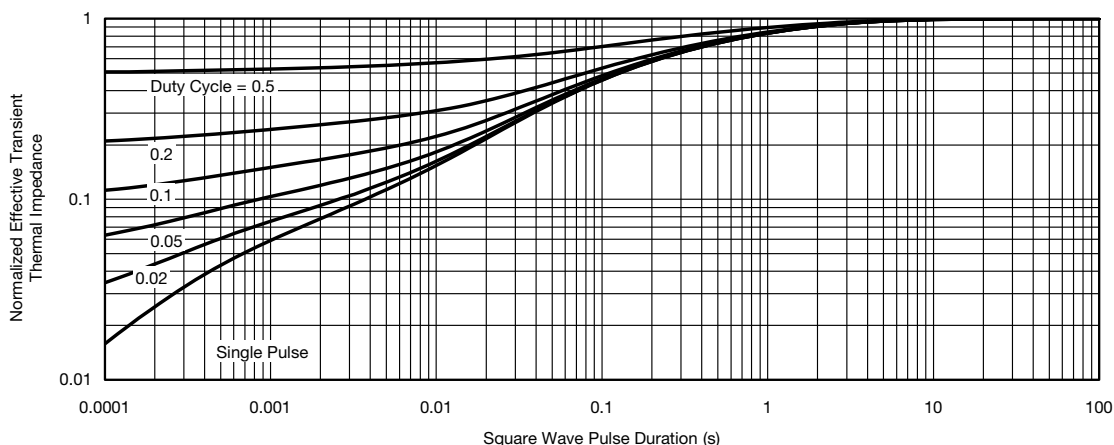
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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