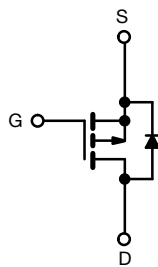


# Power MOSFET

**TO-220AB**


P-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	-200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	1.5
$Q_g$ max. (nC)	22	
$Q_{gs}$ (nC)	12	
$Q_{gd}$ (nC)	10	
Configuration	Single	

## FEATURES

- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



Available  
**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9620PbF
Lead (Pb)-free and halogen-free	IRF9620PbF-BE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	-200	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$V_{GS}$ at -10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	-14	
Linear serating factor		0.32	W/°C
Maximum power dissipation	$P_D$	40	W
Peak diode recovery dV/dt <sup>b</sup>	dV/dt	-5.0	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	
		1.1	N · m

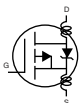

## Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $I_{SD} \leq -3.5$  A,  $dI/dt \leq 95$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	3.1	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

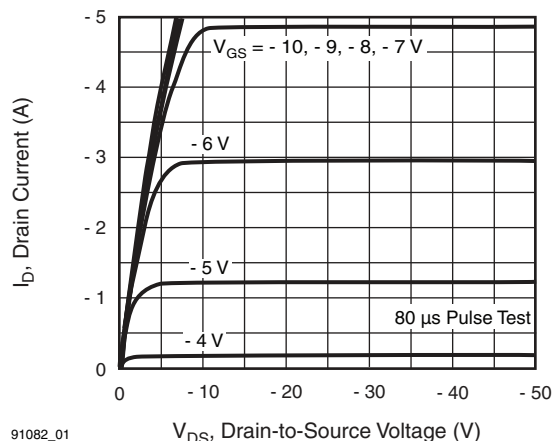
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = -1\text{ mA}$		-	-0.22	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -200\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$		-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.5\text{ A}^b$	-	-	1.5	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}$ , $I_D = -1.5\text{ A}^b$		1.0	-	-	S
Dynamic							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	350	-	pF
Output capacitance	$C_{oss}$			-	100	-	
Reverse transfer capacitance	$C_{rss}$			-	30	-	
Total gate charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -4.0\text{ A}$ , $V_{DS} = -160\text{ V}$ , see fig. 11 and 18 <sup>b</sup>	-	-	22	nC
Gate-source charge	$Q_{gs}$			-	-	12	
Gate-drain charge	$Q_{gd}$			-	-	10	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -100\text{ V}$ , $I_D = -1.5\text{ A}$ , $R_g = 50\text{ }\Omega$ , $R_D = 67\text{ }\Omega$ , see fig. 17 <sup>b</sup>		-	15	-	ns
Rise time	$t_r$			-	25	-	
Turn-off delay time	$t_{d(off)}$			-	20	-	
Fall time	$t_f$			-	15	-	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		0.9	-	5.7	$\Omega$
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-3.5	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	-14	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = -3.5\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	-7.0	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = -3.5\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	300	450	ns
Body diode reverse recovery charge	$Q_{rr}$			-	1.9	2.9	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

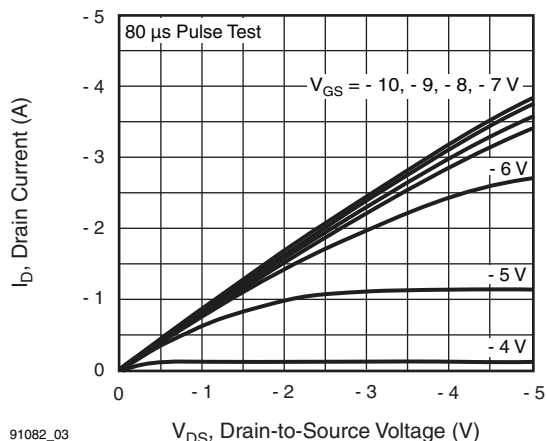


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



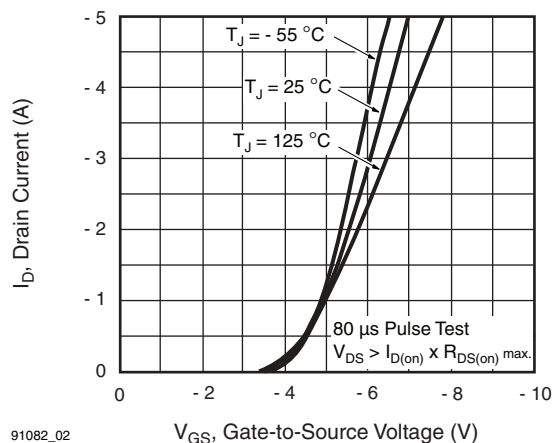
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**Fig. 1 - Typical Output Characteristics**



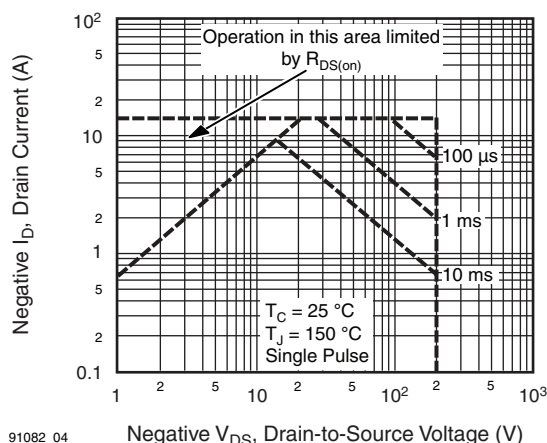
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**Fig. 3 - Typical Saturation Characteristics**



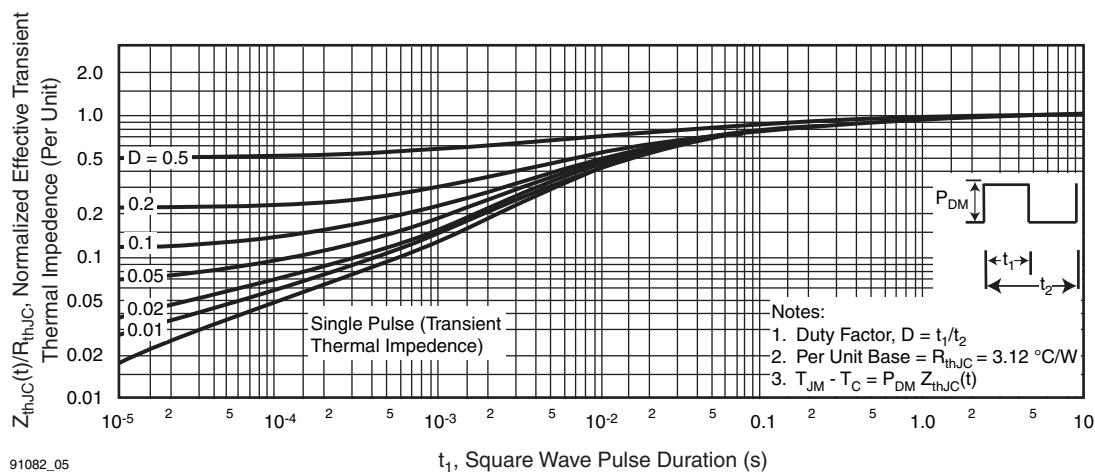
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**Fig. 2 - Typical Transfer Characteristics**



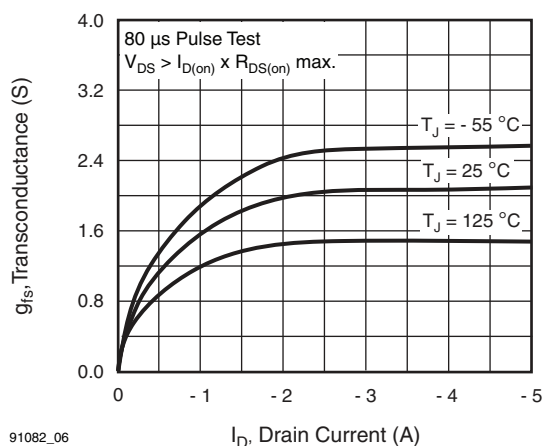
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**Fig. 4 - Maximum Safe Operating Area**

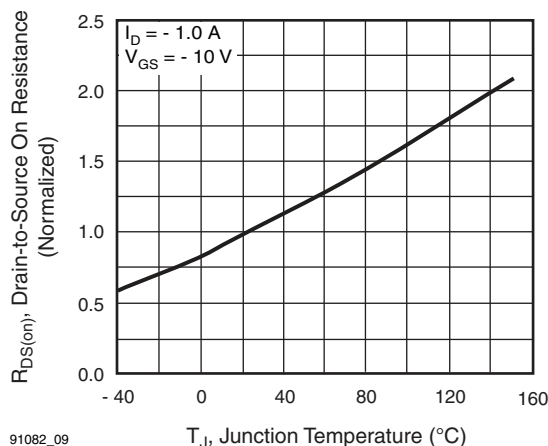


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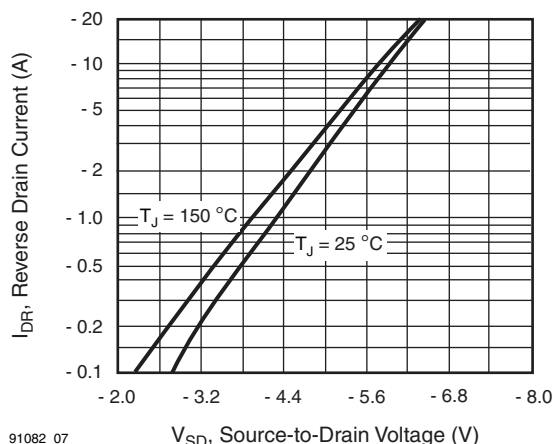
**Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**



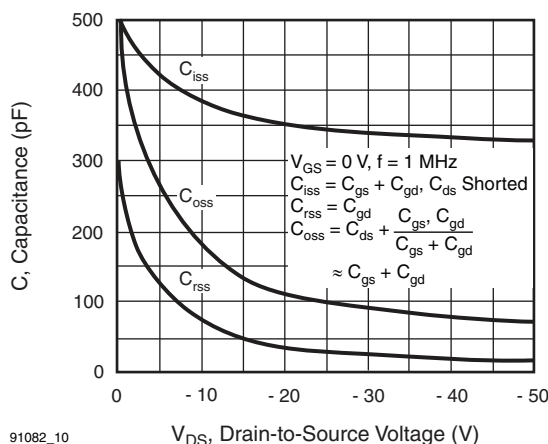
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**Fig. 6 - Typical Transconductance vs. Drain Current**


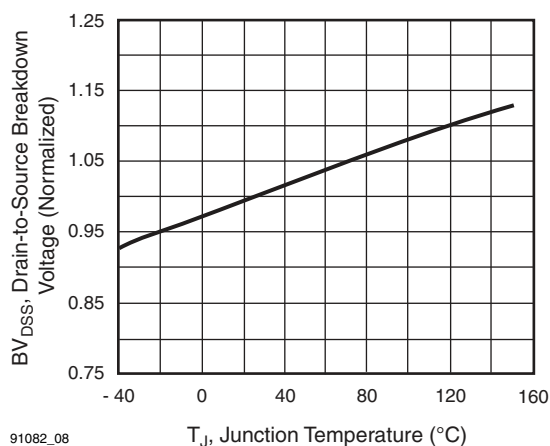
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**Fig. 9 - Normalized On-Resistance vs. Temperature**


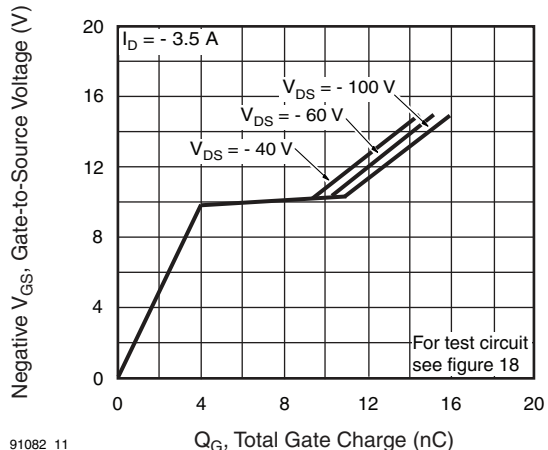
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**


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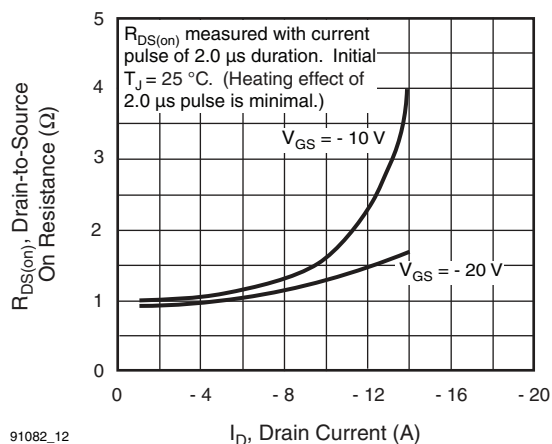
**Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage**


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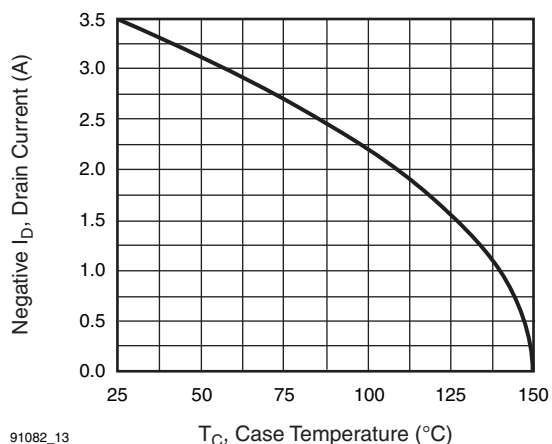
**Fig. 8 - Breakdown Voltage vs. Temperature**


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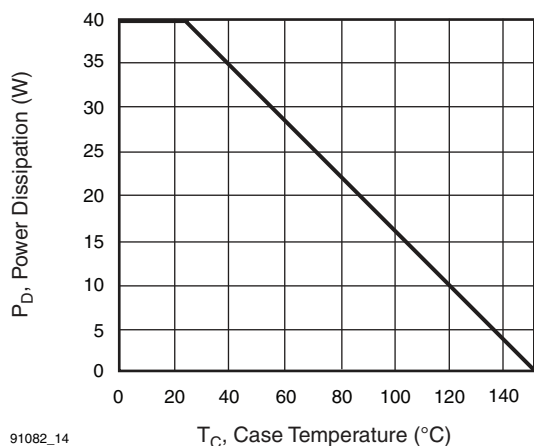
**Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage**



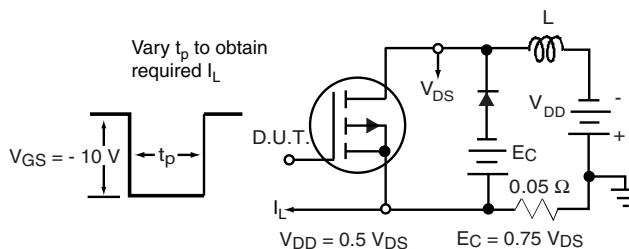
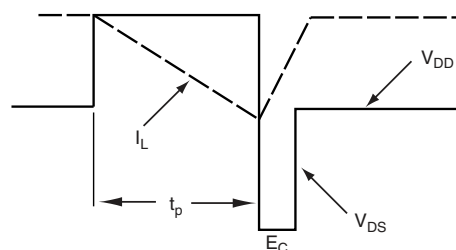
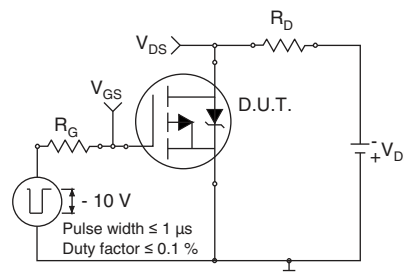
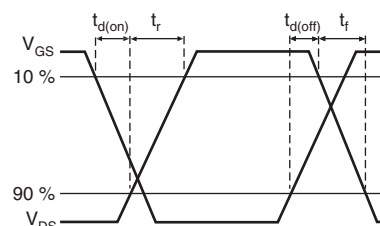
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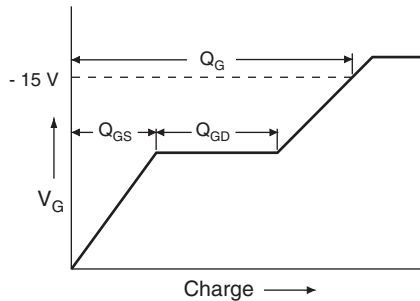
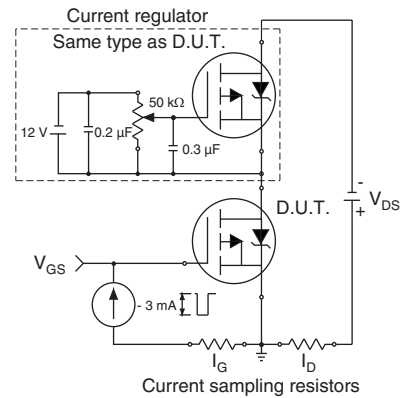
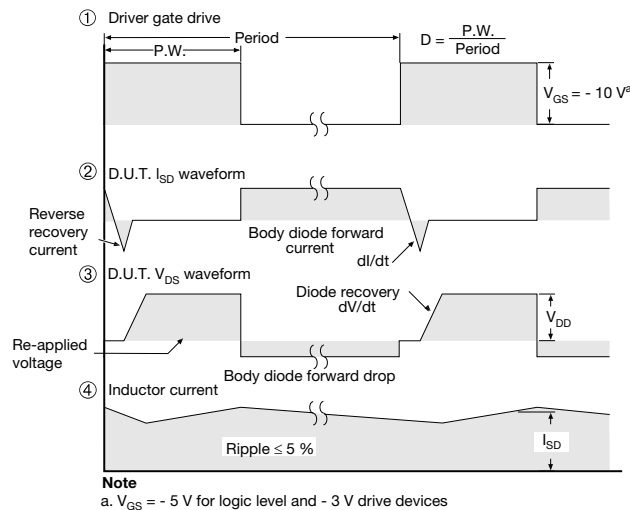
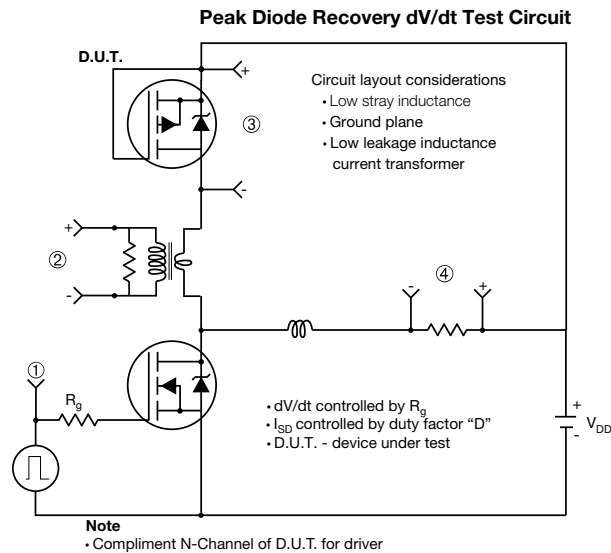
**Fig. 12 - Typical On-Resistance vs. Drain Current**


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**Fig. 13 - Maximum Drain Current vs. Case Temperature**


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**Fig. 14 - Power vs. Temperature Derating Curve**

**Fig. 15 - Clamped Inductive Test Circuit**

**Fig. 16 - Clamped Inductive Waveforms**

**Fig. 17a - Switching Time Test Circuit**

**Fig. 17b - Switching Time Waveforms**


**Fig. 18a - Basic Gate Charge Waveform**

**Fig. 18b - Gate Charge Test Circuit**

**Fig. 19 - For P-Channel**

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