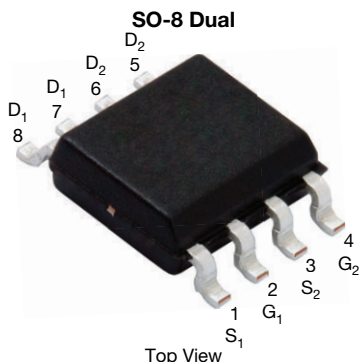


# Automotive N-and P-Channel 30 V (D-S) 175 °C MOSFET

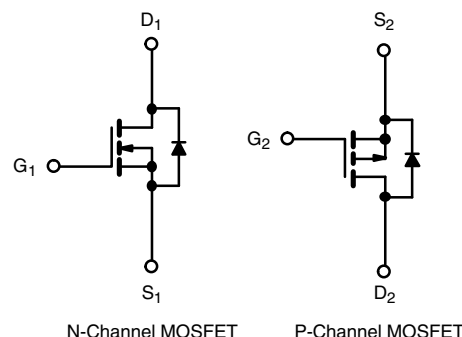


Marking Code: Q4532A

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
$V_{DS}$ (V)	30	-30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = \pm 10$ V	0.031	0.070
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = \pm 4.5$ V	0.042	0.190
$I_D$ (A)	7.3	-5.3
Configuration	N- and p-pair	

## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified <sup>c</sup>
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	SQ4532AEY (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V <sub>DS</sub>	30	-30	V
Gate-source voltage		V <sub>GS</sub>	± 20		
Continuous drain current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	7.3	-5.3	A
	T <sub>C</sub> = 125 °C		4.2	-3	
Continuous source current (diode conduction)		I <sub>S</sub>	4.2	-3	
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	29	-21	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	10	-9	
Single pulse avalanche energy		E <sub>AS</sub>	5	4	
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	3.3	3.3	W
	T <sub>C</sub> = 125 °C		1.1	1.1	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>sta</sub>	-55 to +175		°C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-ambient	$R_{thJA}$	110	105	°C/W
Junction-to-foot (drain)	$R_{thJF}$	45	45	

## Notes

- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- Parametric verification ongoing



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Static								
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		N-Ch	30	-	-	V
		V <sub>GS</sub> = 0, I <sub>D</sub> = -250 μA		P-Ch	-30	-	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		N-Ch	1.5	2	2.5	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		P-Ch	-1.5	-2	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V	N-Ch	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V	P-Ch	-	-	-1	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 125 °C	N-Ch	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	P-Ch	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 30 V, T <sub>J</sub> = 175 °C	N-Ch	-	-	150	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	P-Ch	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 5 V	N-Ch	15	-	-	A
		V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -5 V	P-Ch	-15	-	-	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.9 A	N-Ch	-	0.021	0.031	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A	P-Ch	-	0.056	0.070	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.9 A, T <sub>J</sub> = 125 °C	N-Ch	-	-	0.064	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 125 °C	P-Ch	-	-	0.100	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.9 A, T <sub>J</sub> = 175 °C	N-Ch	-	-	0.082	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 175 °C	P-Ch	-	-	0.117	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 4.1 A	N-Ch	-	0.033	0.042	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2.5 A	P-Ch	-	0.157	0.190	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.9 A		N-Ch	-	22	-	S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.5 A		P-Ch	-	5.5	-	
Dynamic <sup>b</sup>								
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 15 V, f = 1 MHz	N-Ch	-	357	535	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -15 V, f = 1 MHz	P-Ch	-	352	528	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 15 V, f = 1 MHz	N-Ch	-	82	123	pF
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -15 V, f = 1 MHz	P-Ch	-	95	142	
Reverse transfer capacitance	C <sub>rss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 15 V, f = 1 MHz	N-Ch	-	36	53	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -15 V, f = 1 MHz	P-Ch	-	59	88	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.9 A	N-Ch	-	5.9	7.8	
		V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.5 A	P-Ch	-	7.9	10.2	
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.9 A	N-Ch	-	1	-	nC
		V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.5 A	P-Ch	-	1.1	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.9 A	N-Ch	-	1.9	-	
		V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.5 A	P-Ch	-	2.7	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		N-Ch	1.7	3.4	5.1	Ω
				P-Ch	2.8	5.8	8.6	



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	7	10	ns
		V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ -1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	6	9	
Rise time	t <sub>r</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	17	21	
		V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ -1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	17	21	
Turn-off delay time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	10	14	
		V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ -1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	19	24	
Fall time	t <sub>f</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	19	24	
		V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≡ -1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	16	20	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>		N-Ch	-	-	29	A
			P-Ch	-	-	-21	
Forward voltage	V <sub>SD</sub>	I <sub>S</sub> = 2 A	N-Ch	-	0.8	1.2	V
		I <sub>S</sub> = -1.5 A	P-Ch	-	-0.8	-1.2	

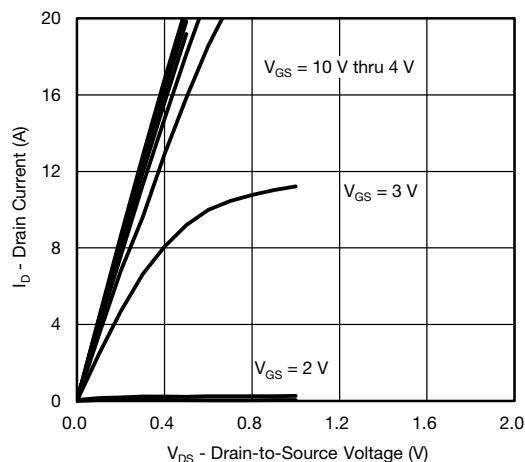
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

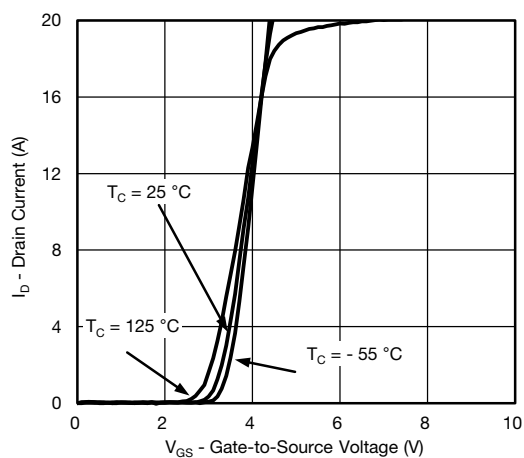
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



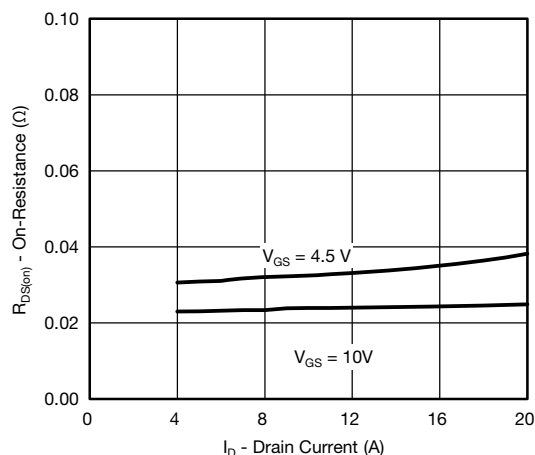
**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



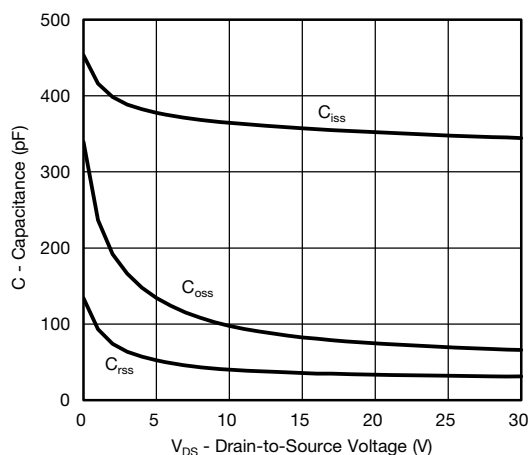
**Output Characteristics**



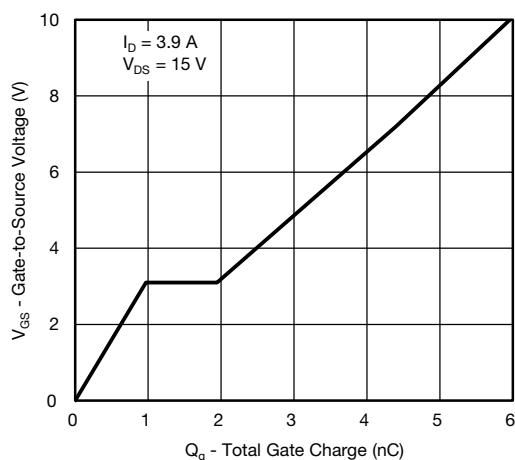
**Transfer Characteristics**



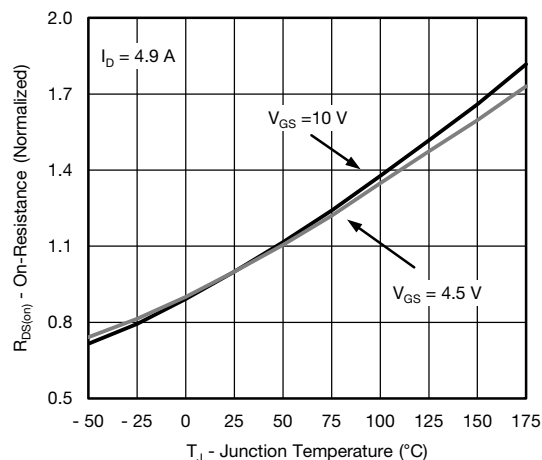
**On-Resistance vs. Drain Current**



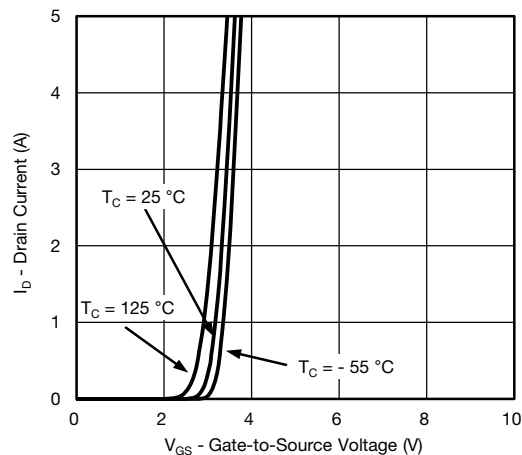
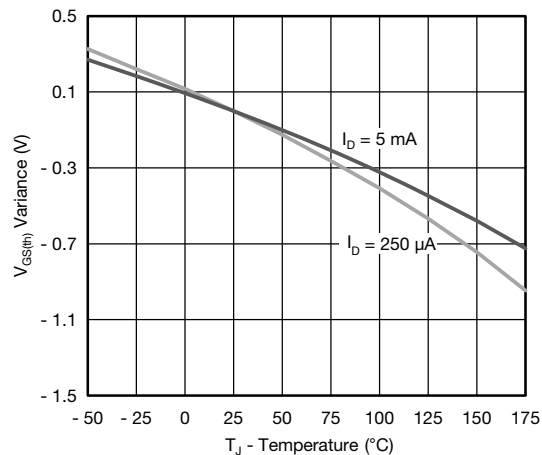
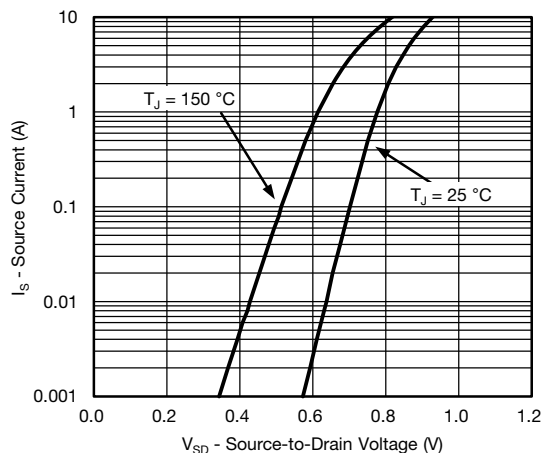
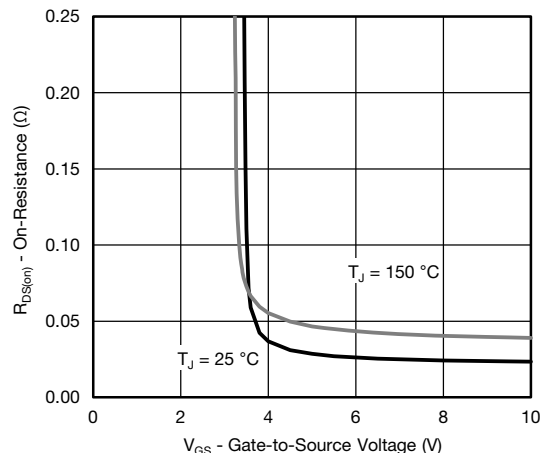
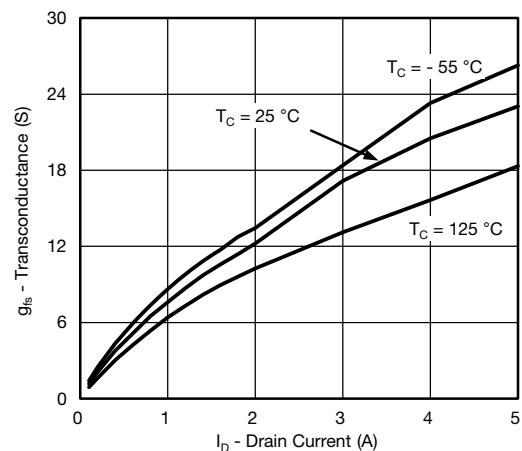
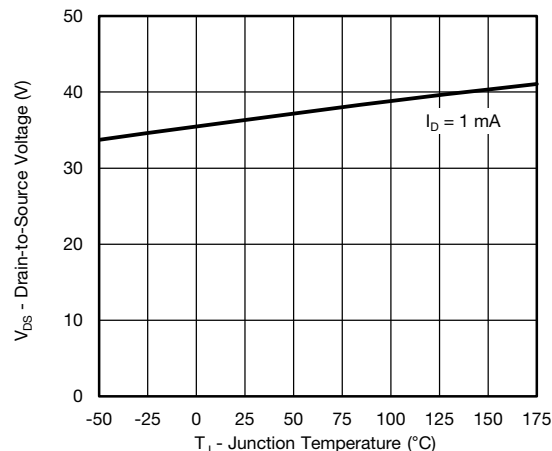
**Capacitance**



**Gate Charge**

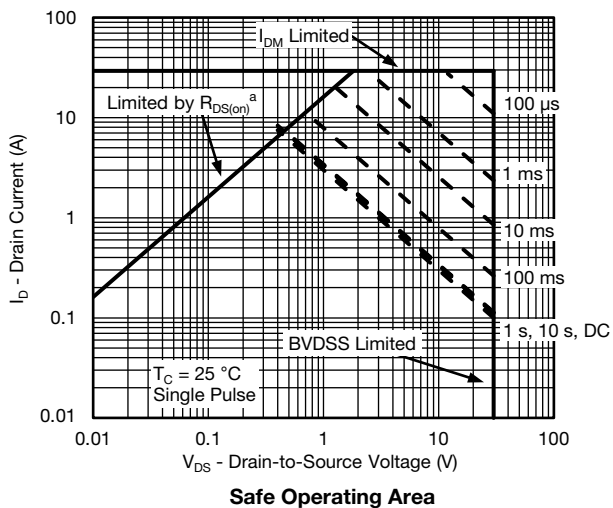


**On-Resistance vs. Junction Temperature**

**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Transfer Characteristics**

**Threshold Voltage**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Transconductance**

**Drain Source Breakdown vs. Junction Temperature**

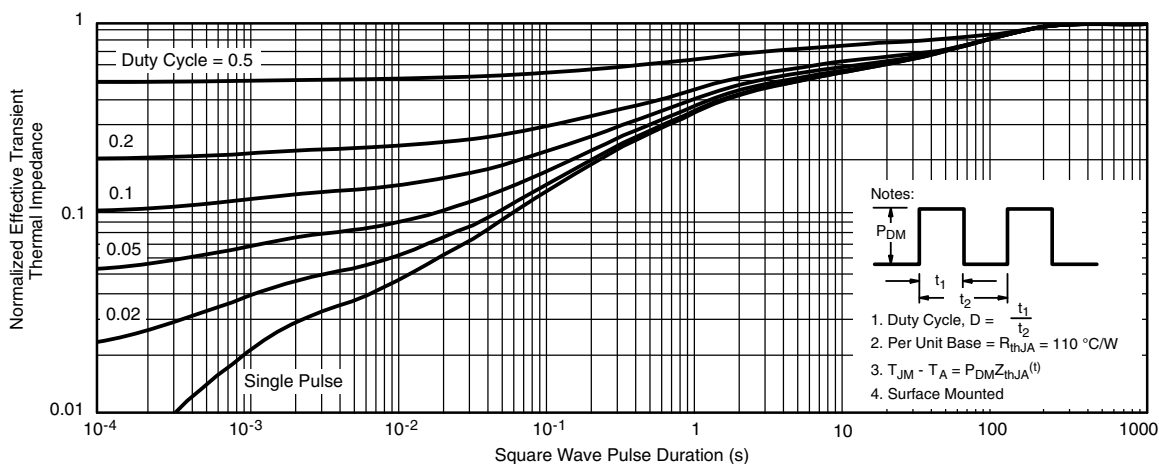
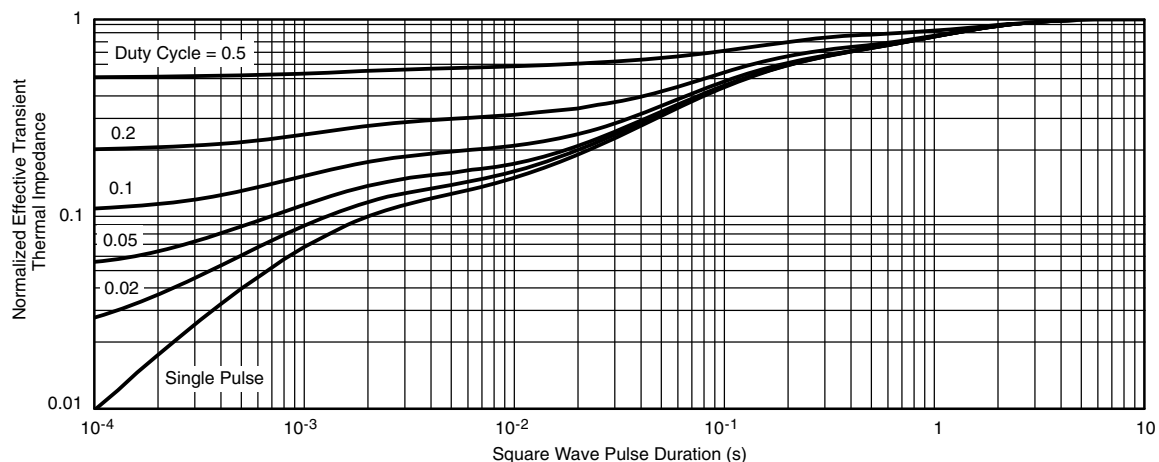


**N-CHANNEL THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

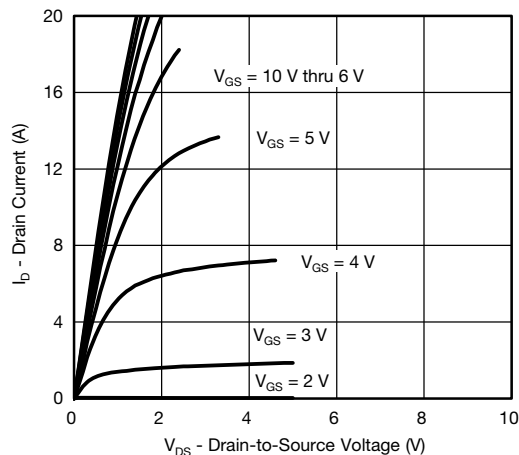
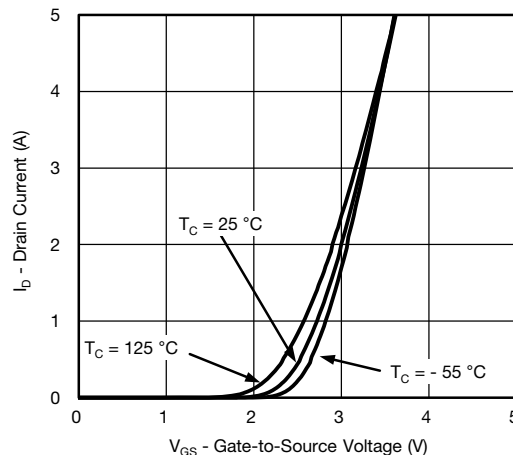
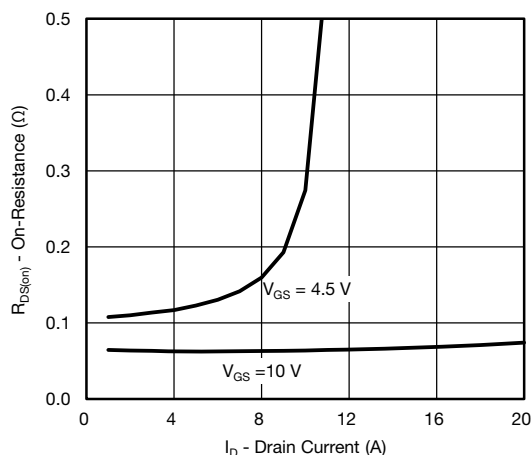
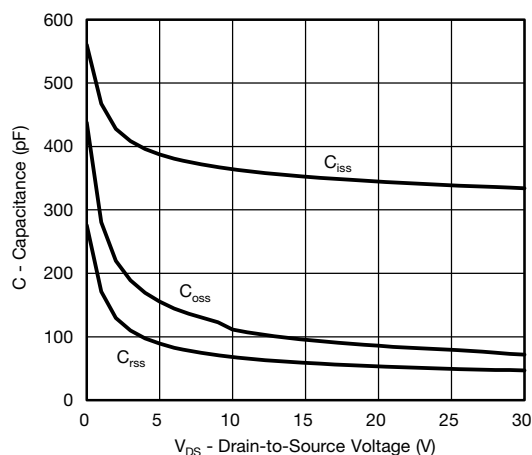
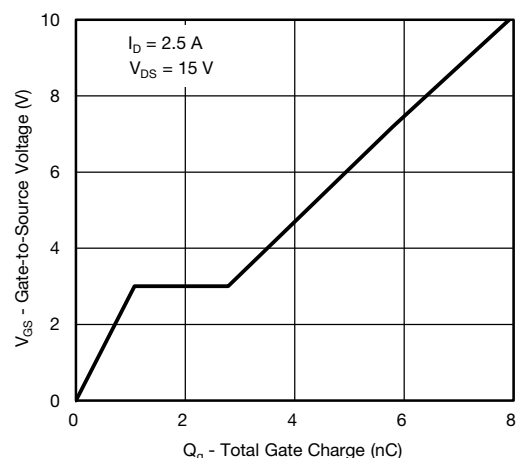
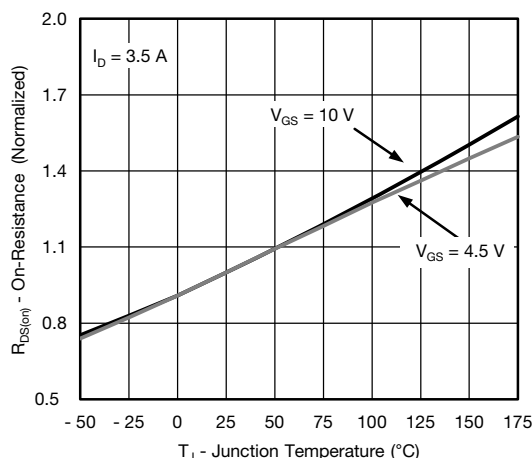


**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**N-CHANNEL THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Foot**
**Note**

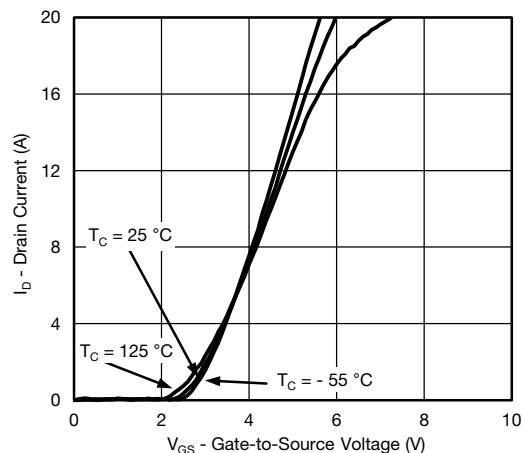
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

**P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

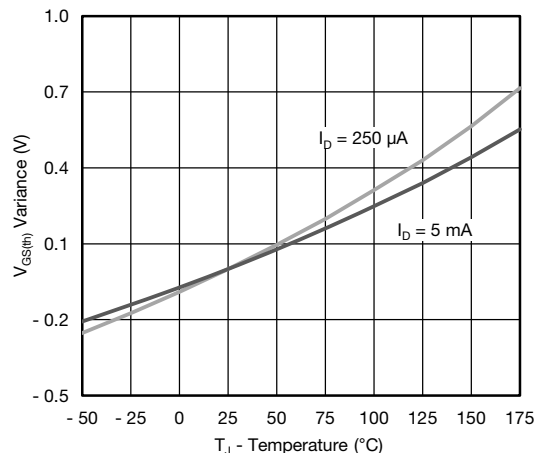




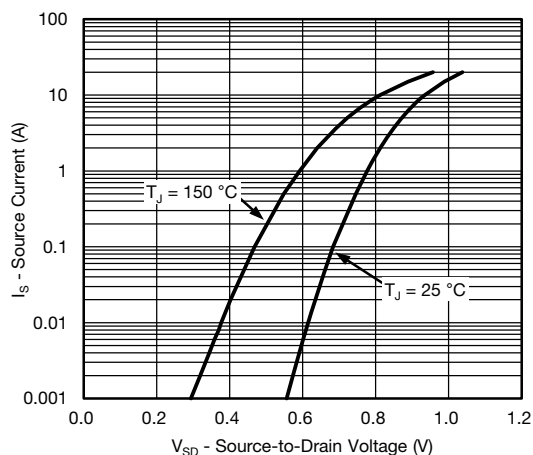
**P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



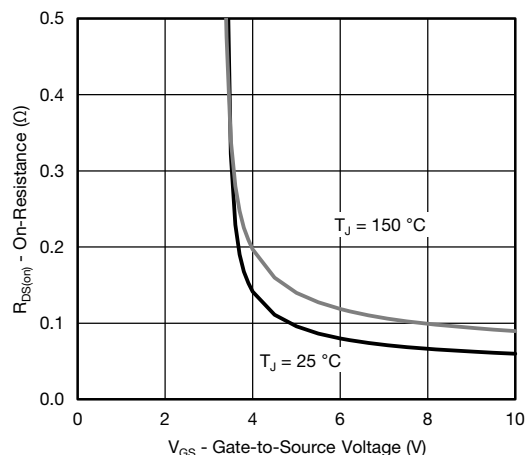
**Transfer Characteristics**



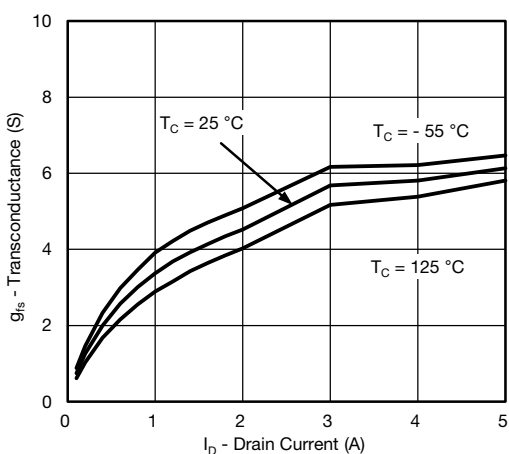
**Threshold Voltage**



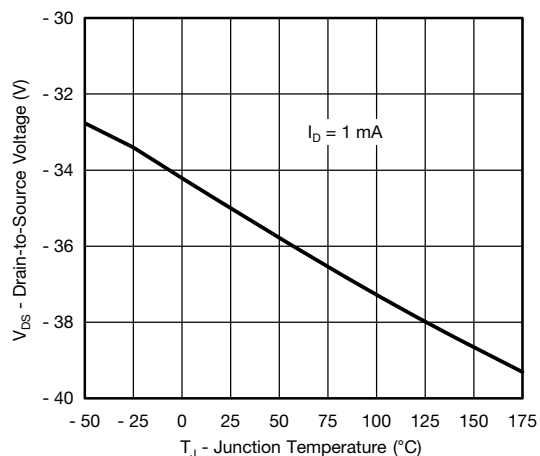
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



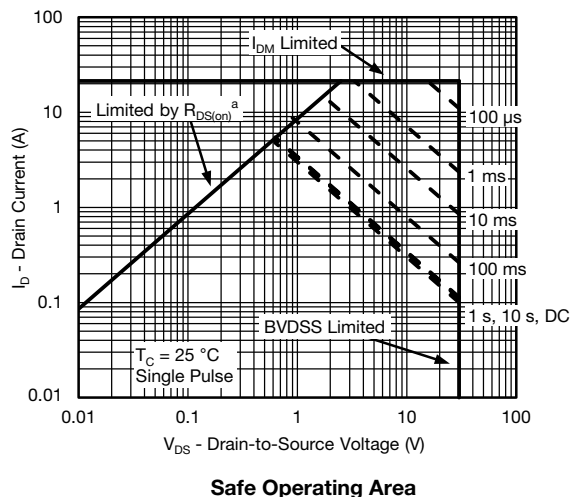
**Transconductance**



**Drain Source Breakdown vs. Junction Temperature**

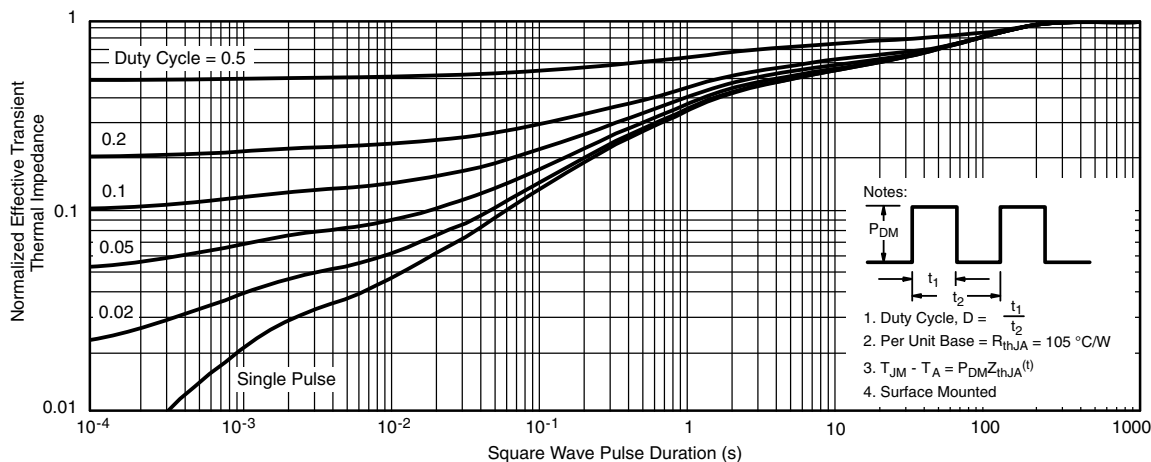
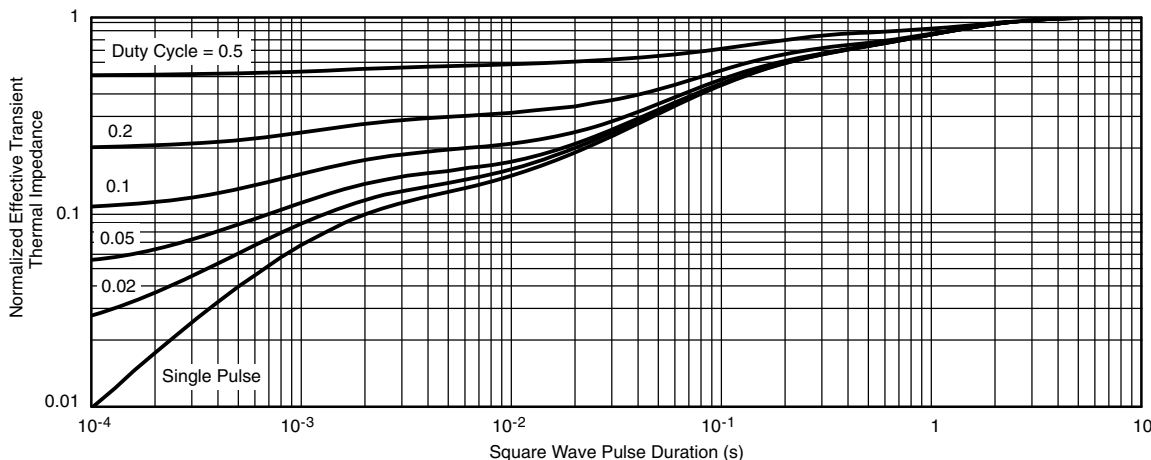


**P-CHANNEL THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

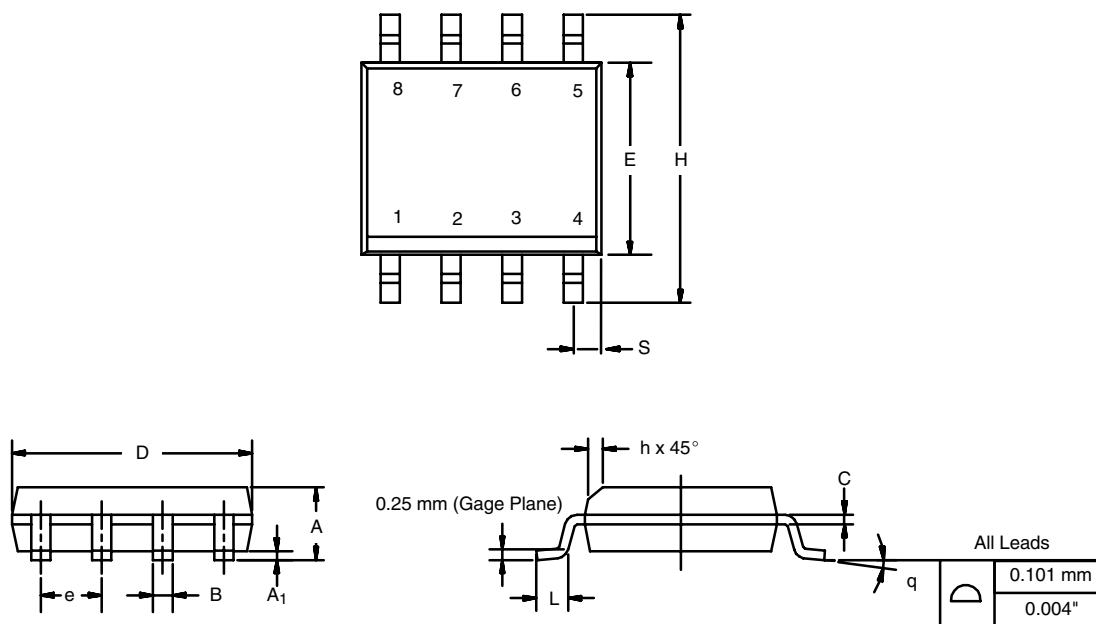
**P-CHANNEL THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot****Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
    - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62981](http://www.vishay.com/ppg?62981).

## SOIC (NARROW): 8-LEAD

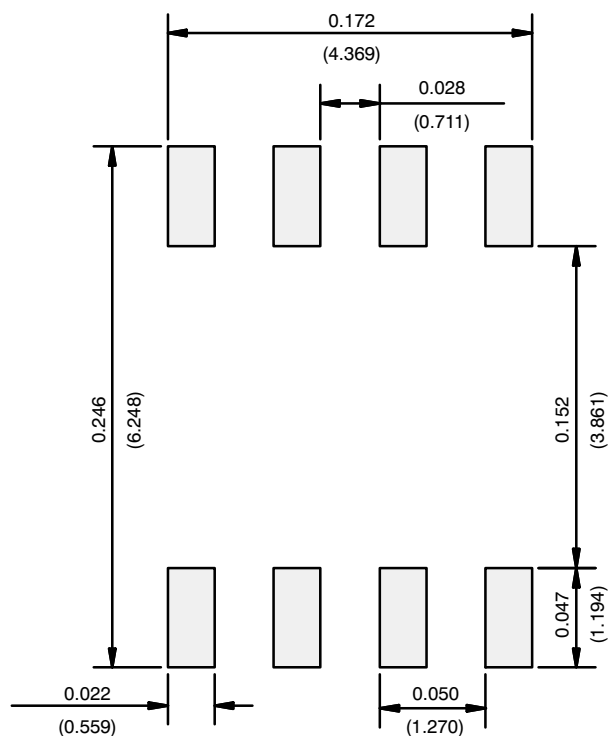
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06  
DWG: 5498

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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