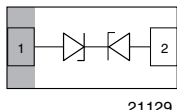
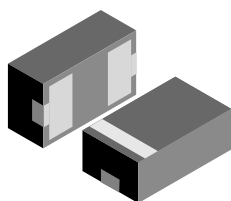


Bidirectional Symmetrical (BiSy) Single Line ESD-Protection Diode in LLP1006-2M



21129



20855

MARKING (example only)



21121

Bar = pin 1 marking

X = date code

Y = type code (see table below)

LINKS TO ADDITIONAL RESOURCES



3D Models

SPICE

Models

FEATURES

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range ± 3.5 V
- Low leakage current < 0.1 μ A
- Low load capacitance $C_D = 12.5$ pF
- ESD immunity acc. IEC 61000-4-2
 ± 18 kV contact discharge
 ± 20 kV air discharge
- Soldering can be checked by standard vision inspection, no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VCUT03B1-DD1	VCUT03B1-DD1-G-08	8000	8000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VCUT03B1-DD1	LLP1006-2M	N	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS VCUT03B1-DD1

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	I_{PPM}	3.5	A
Peak pulse power	Pin 1 to pin 2 Acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	P_{PP}	40	W
ESD immunity	Contact discharge acc. IEC61000-4-2; 10 pulses	V_{ESD}	± 18	kV
	Air discharge acc. IEC61000-4-2; 10 pulses		± 20	
Operating temperature	Junction temperature	T_J	-40 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

CUT THE SPIKES WITH VCUT03B1-DD1

The VCUT03B1-DD1 is a bidirectional and symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT03B1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.

ELECTRICAL CHARACTERISTICS VCUT03B1-DD1

($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	N_{channel}	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	3.5	V
Reverse voltage	At $I_{\text{R}} = 0.1 \mu\text{A}$	V_{R}	3.5	-	-	V
Reverse current	At $V = 3.5 \text{ V}$	I_{R}	-	-	0.1	μA
Reverse breakdown voltage	At $I = 1 \text{ mA}$	V_{BR}	5.8	6.7	7.5	V
Reverse clamping voltage	At $I_{\text{PP}} = 1 \text{ A}$	V_{C}	-	7.8	9	V
	At $I_{\text{PP}} = I_{\text{PPM}} = 3.5 \text{ A}$	V_{C}	-	9.5	11.5	V
Capacitance	At $V = 0 \text{ V}$; $f = 1 \text{ MHz}$	C_{D}	-	12.5	15	pF
	At $V = 2.5 \text{ V}$; $f = 1 \text{ MHz}$	C_{D}	-	11.5	-	pF

TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

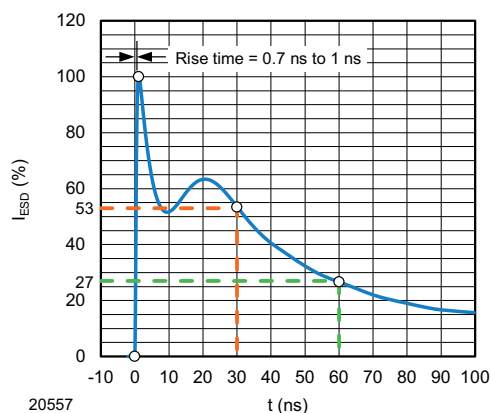


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

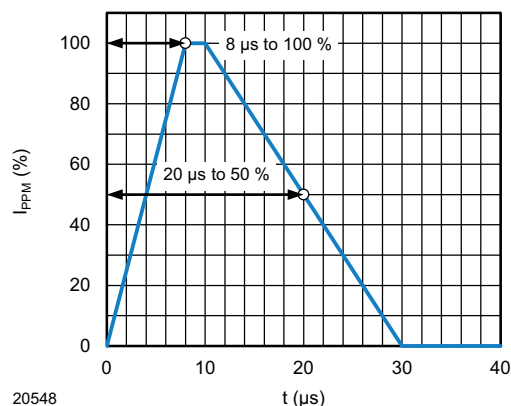


Fig. 2 - 8/20 μ s Peak Pulse Current Wave Form
acc. IEC 61000-4-5

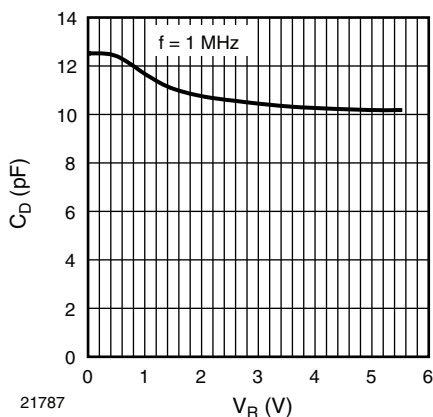
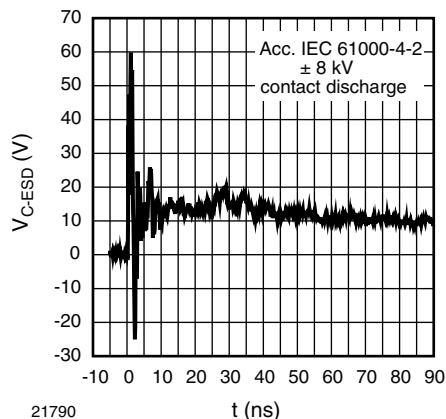
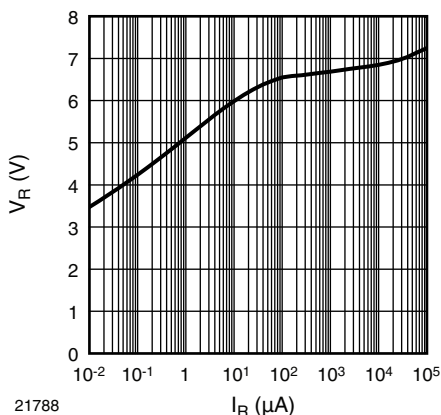
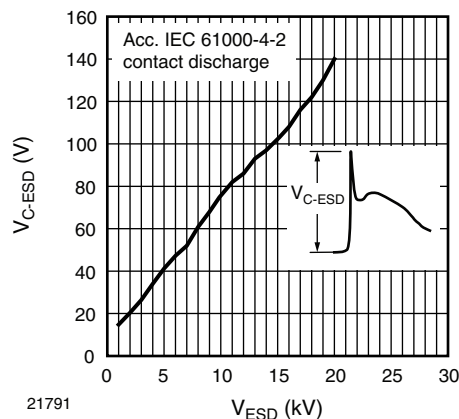
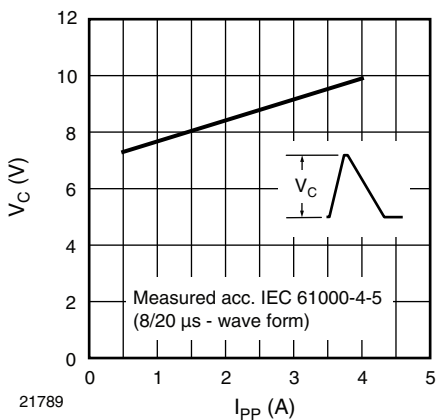
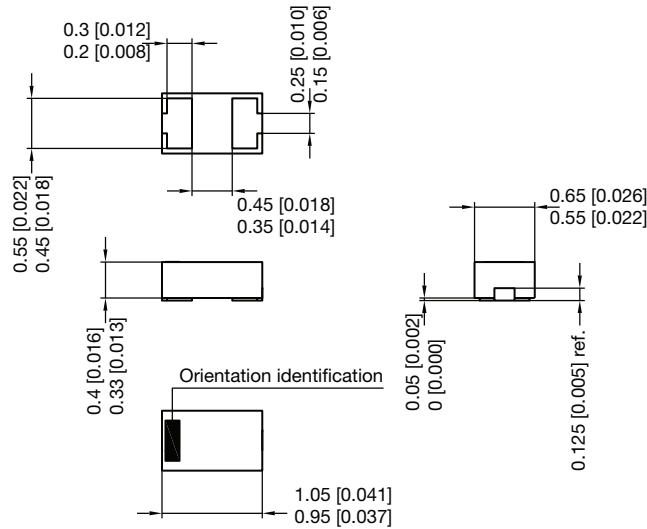
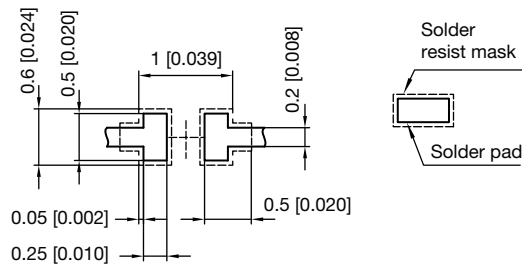

Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

Fig. 6 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F


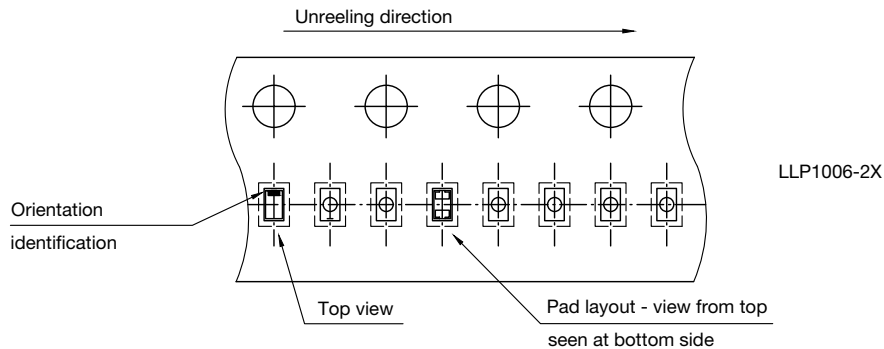
Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

PACKAGE DIMENSIONS in millimeters (inches): **LLP1006-2M**

Foot print recommendation:


Pad Design Patented:
(©US 9.018.537 B2)

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Rev. 7 - Date: 11.May 2016
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02.05.2017
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