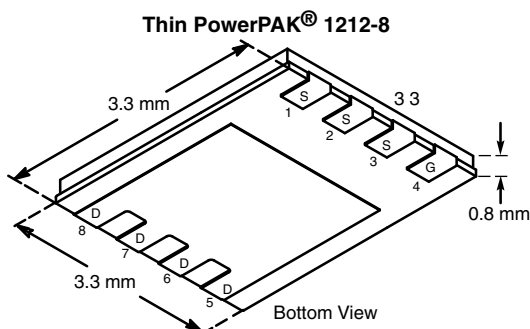


# P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 20	0.0054 at $V_{GS} = - 4.5V$	- 30 <sup>a</sup>	57 nC
	0.0060 at $V_{GS} = - 3.7 V$	- 30 <sup>a</sup>	
	0.0083 at $V_{GS} = - 2.5 V$	- 30 <sup>a</sup>	
	0.0140 at $V_{GS} = - 1.8 V$	- 30 <sup>a</sup>	



Ordering Information:  
SiS435DNT-T1-GE3 (Lead (Pb)-free and Halogen-free)

## FEATURES

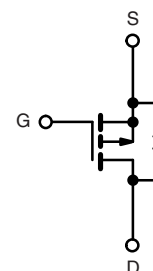
- TrenchFET<sup>®</sup> Gen III P-Channel Power MOSFET
- Thin 0.8 mm max. height
- 100 %  $R_g$  and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS  
COMPLIANT  
HALOGEN  
FREE

## APPLICATIONS

- Smart Phones, Tablet PCs, and Mobile Computing
- Battery Switch
- Load Switch
- Power Management
- Battery Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	- 20	V
Gate-Source Voltage		$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	$I_D$	- 30 <sup>a</sup>	A
	$T_C = 70^\circ\text{C}$		- 30 <sup>a</sup>	
	$T_A = 25^\circ\text{C}$		- 22 <sup>b, c</sup>	
	$T_A = 70^\circ\text{C}$		- 17 <sup>b, c</sup>	
Pulsed Drain Current ( $t = 300 \mu\text{s}$ )		$I_{DM}$	- 80	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	$I_S$	- 30 <sup>a</sup>	
	$T_A = 25^\circ\text{C}$		- 3.1 <sup>b, c</sup>	
Avalanche Current	$L = 0.1 \text{ mH}$	$I_{AS}$	- 20	mJ
Single Pulse Avalanche Energy		$E_{AS}$	20	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	39	W
	$T_C = 70^\circ\text{C}$		25	
	$T_A = 25^\circ\text{C}$		3.7 <sup>b, c</sup>	
	$T_A = 70^\circ\text{C}$		2.4 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$t \leq 10 \text{ s}$	$R_{thJA}$	24	33	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	2.4	3.2	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10 \text{ s}$ .
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The Thin PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 81  $^\circ\text{C/W}$ .

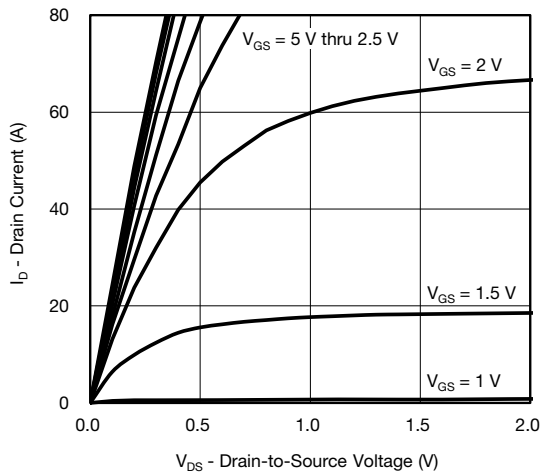
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 20			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 16		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			2.9		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 0.4		- 0.9	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 13 A		0.0044	0.0054	Ω
		V <sub>GS</sub> = - 3.7 V, I <sub>D</sub> = - 10 A		0.0048	0.0060	
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 10 A		0.0065	0.0083	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 5 A		0.0110	0.0140	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 13 A		55		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		5700		pF
Output Capacitance	C <sub>oss</sub>			620		
Reverse Transfer Capacitance	C <sub>rss</sub>			585		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 20 A		98	180	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 20 A		57	86	
Gate-Drain Charge	Q <sub>gd</sub>			7.4		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.8	3.8	7.6	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		40	80	ns
Rise Time	t <sub>r</sub>			30	60	
Turn-Off Delay Time	t <sub>d(off)</sub>			100	200	
Fall Time	t <sub>f</sub>			30	60	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 8 V, R <sub>g</sub> = 1 Ω		15	30	
Rise Time	t <sub>r</sub>			10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			110	220	
Fall Time	t <sub>f</sub>			25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 30	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 80	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 10 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		19	40	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>			9		ns
Reverse Recovery Rise Time	t <sub>b</sub>			10		

## Notes:

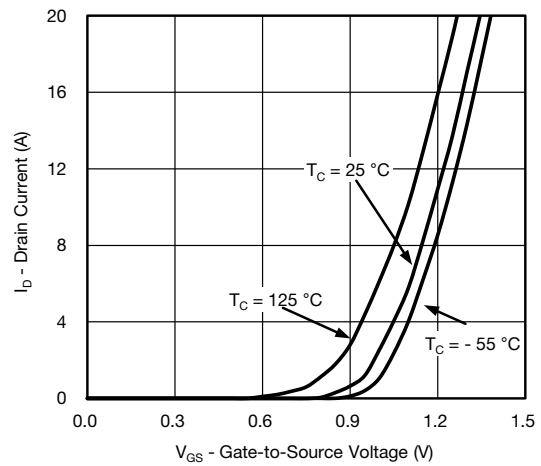
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

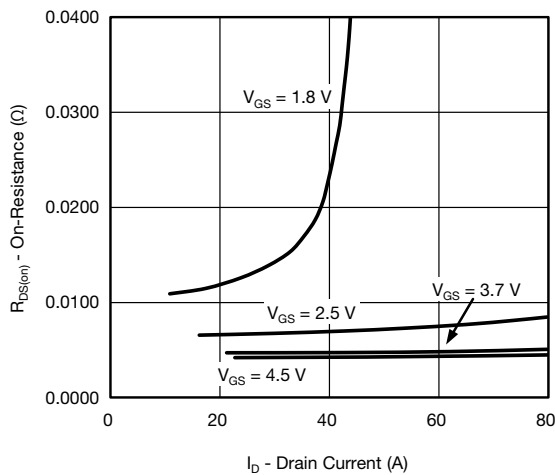
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



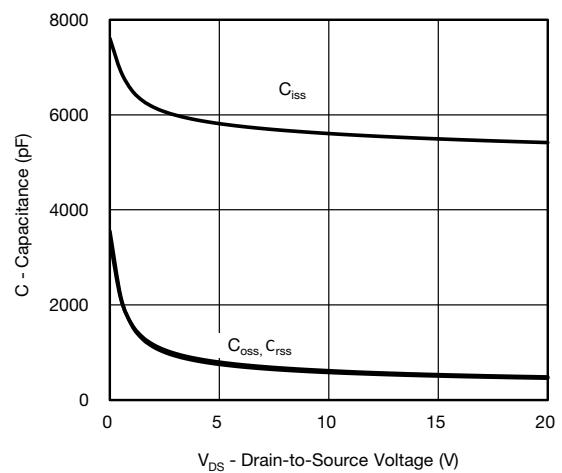
Output Characteristics



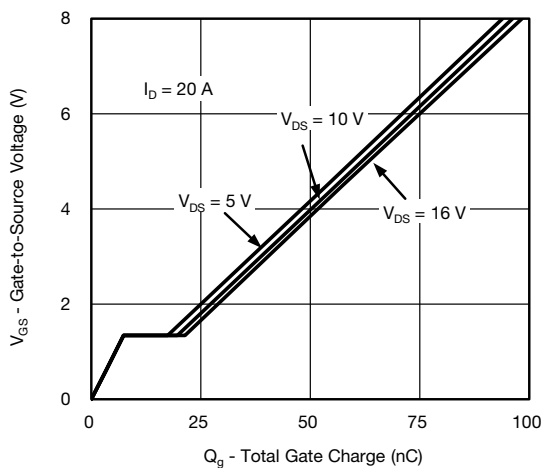
Transfer Characteristics



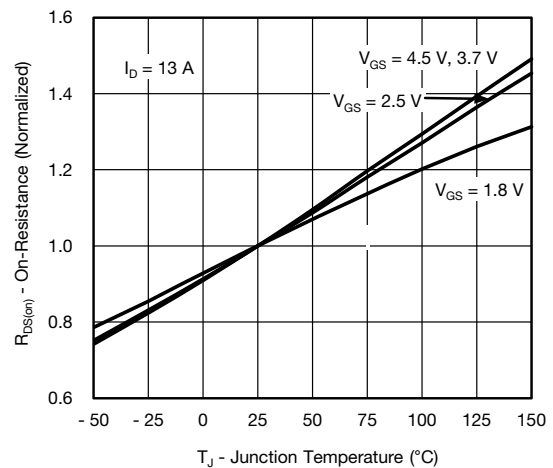
On-Resistance vs. Drain Current and Gate Voltage



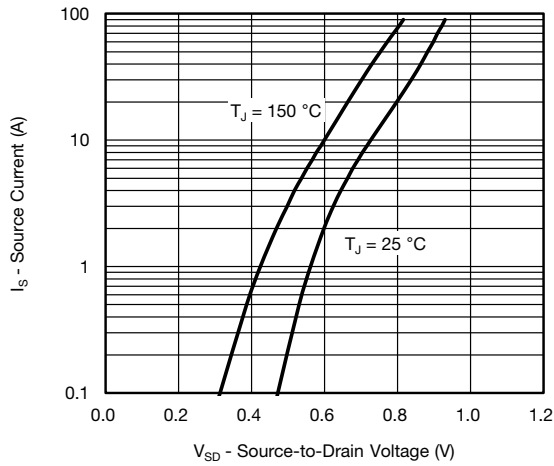
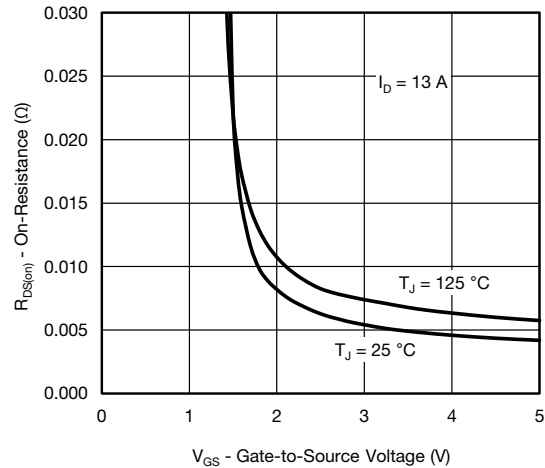
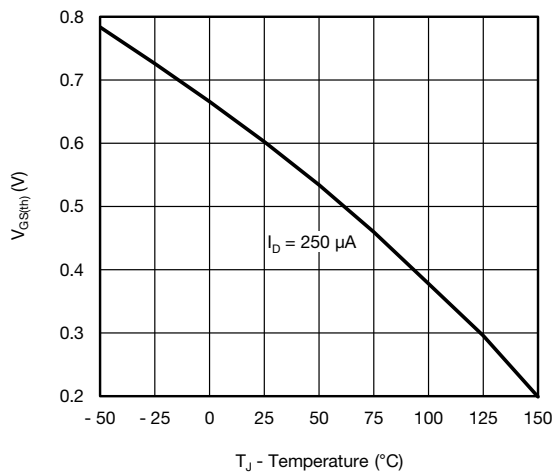
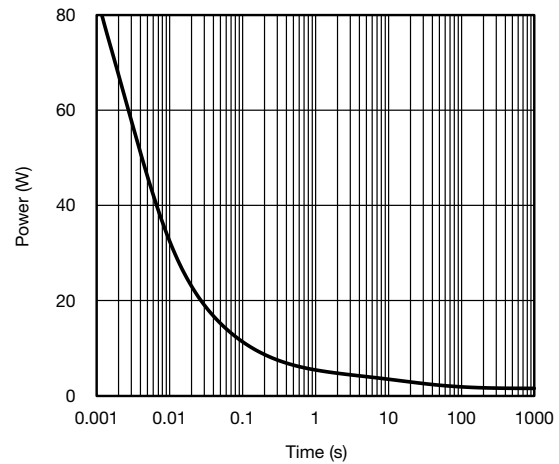
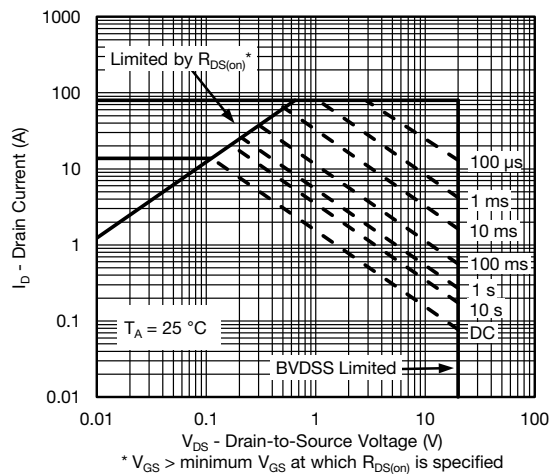
Capacitance



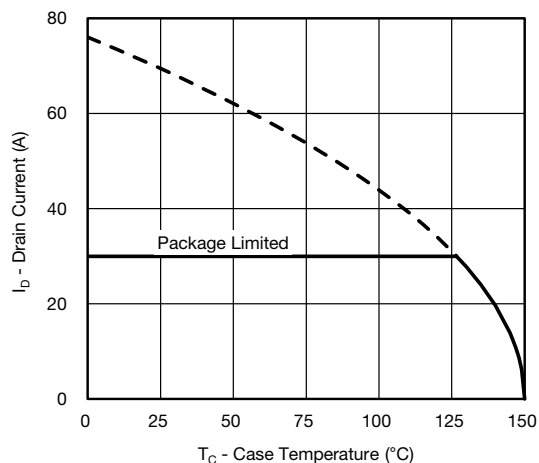
Gate Charge



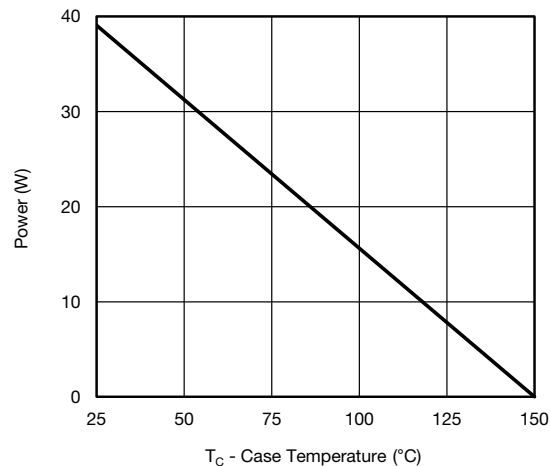
On-Resistance vs. Junction Temperature

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Safe Operating Area, Junction-to-Ambient**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

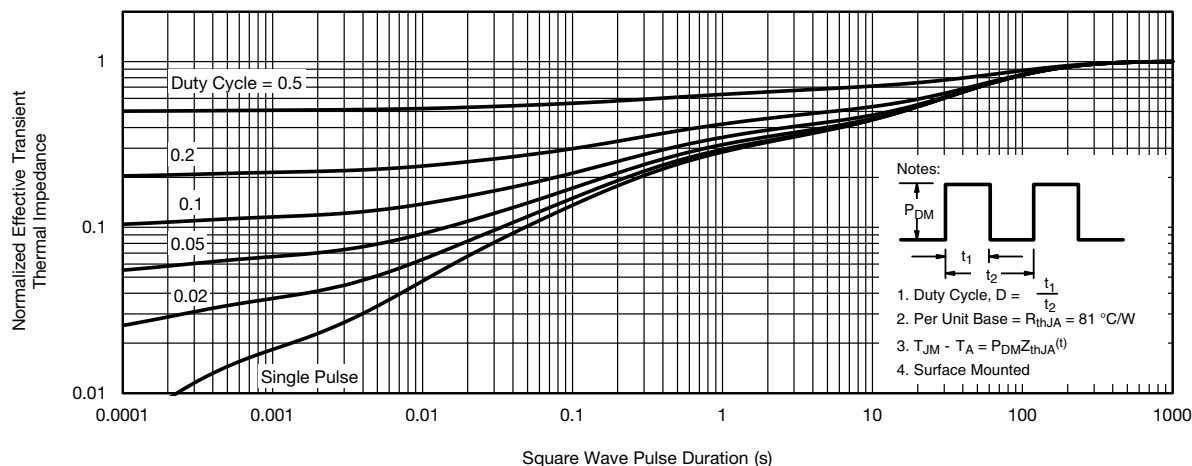
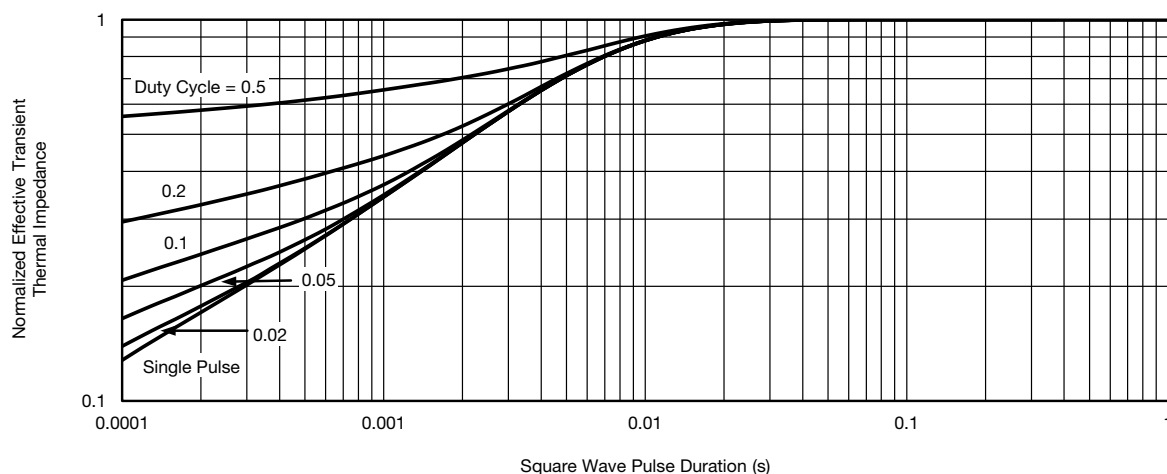


Current Derating\*



Power Derating, Junction-to-Case

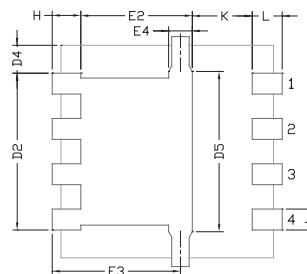
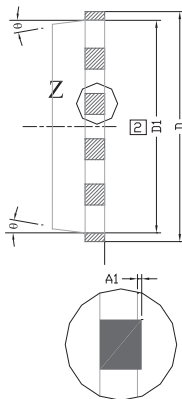
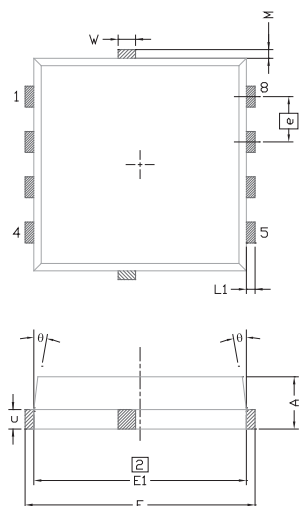
\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

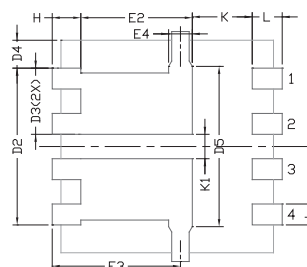
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63264](http://www.vishay.com/ppg?63264).



## PowerPAK® 1212-8T



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

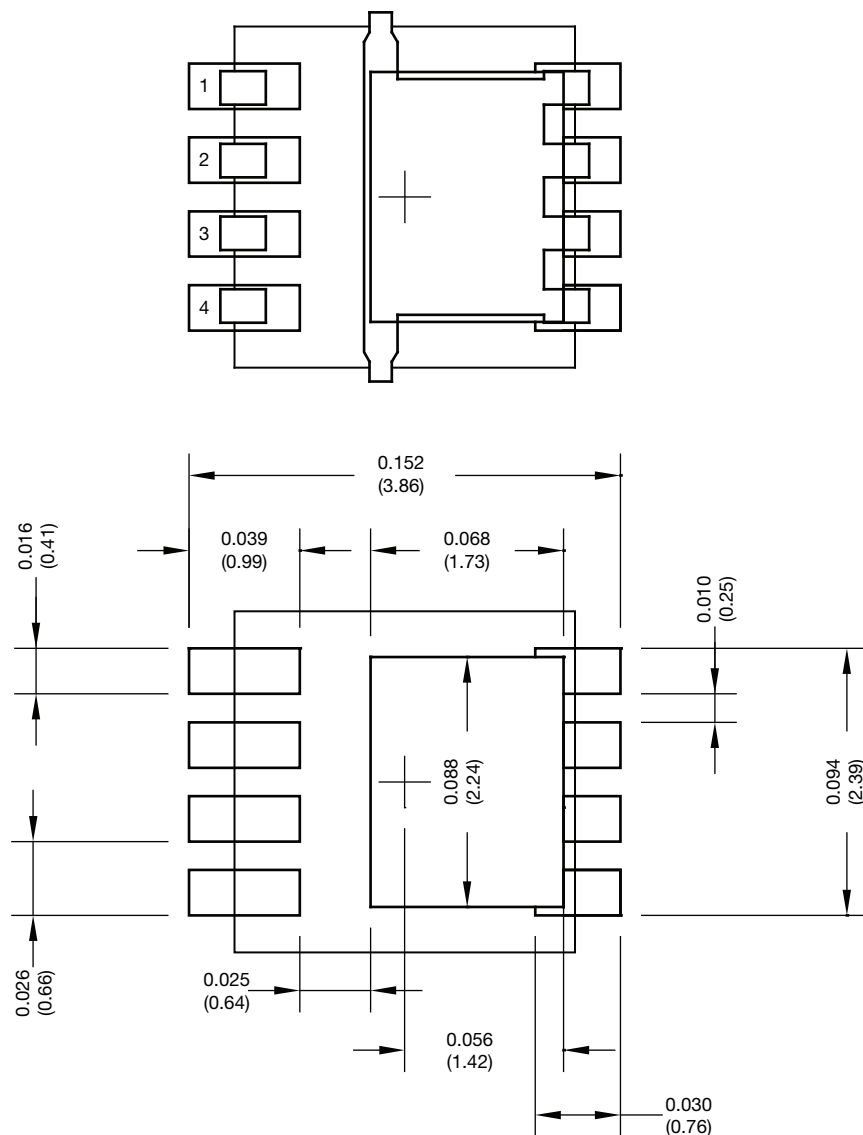
NOTE:		
1	MILLIMETER WILL GOVERN	
2	DIMENSIONS EXCLUSIVE OF MOLD GATE BURRS.	
3	DIMENSIONS EXCLUSIVE OF MOLD FLASH AND CUTTING BURRS.	

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
e	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T13-0056-Rev. A, 18-Feb-13

DWG: 6012

# Recommended Minimum PADs for Thin PowerPAK® 1212-8T







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