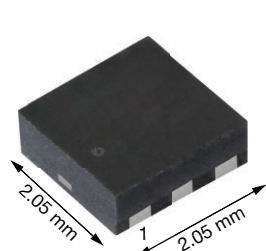
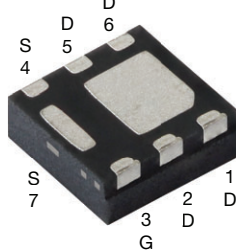


# Automotive N-Channel 80 V (D-S) 175 °C MOSFET

**PowerPAK® SC-70W-6L Single**


Top View



Bottom View

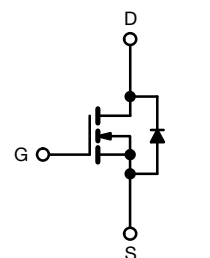
**Marking Code:** Q3XXXX

## PRODUCT SUMMARY

$V_{DS}$ (V)	80
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0940
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.1100
$I_D$ (A)	5.63
Configuration	Single

## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**


N-Channel MOSFET

## ORDERING INFORMATION

Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA602CEJW (for detailed order number please see <a href="http://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	80	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current	$I_D$	$T_C = 25$ °C <sup>a</sup>	5.63
		$T_C = 125$ °C	4.82
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	5.63	A
Pulsed drain current <sup>a</sup>	$I_{DM}$	20	A
Single pulse avalanche current	$I_{AS}$	7.5	A
Single pulse avalanche energy	$E_{AS}$	2.81	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	13.6
		$T_C = 125$ °C	4.5
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	90	°C/W
Junction-to-case (drain)	$R_{thJC}$	11	°C/W

### Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

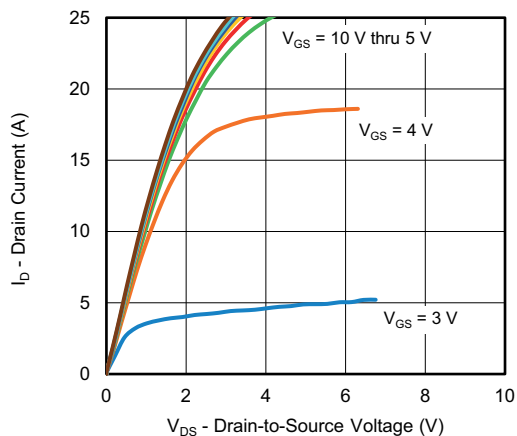
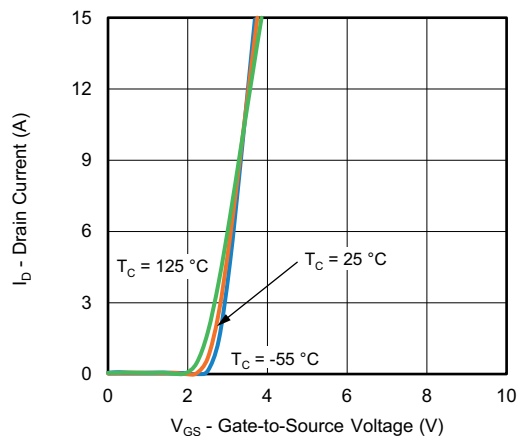
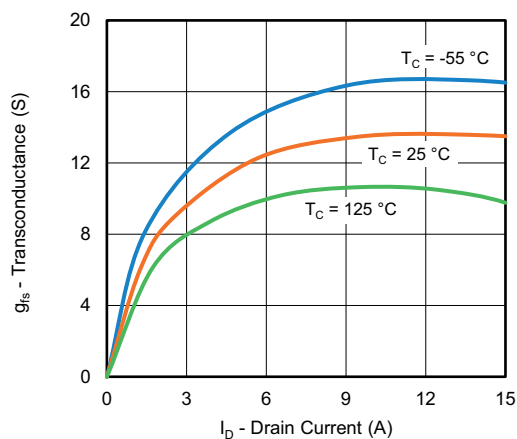
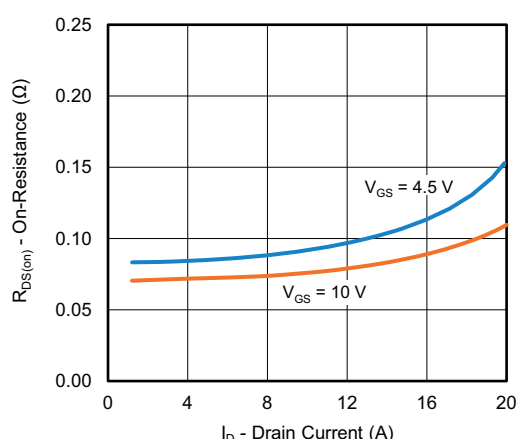
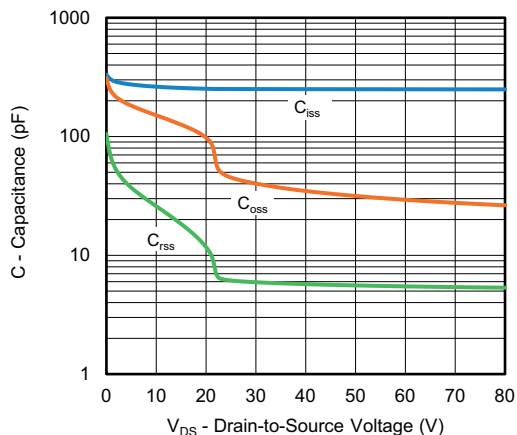
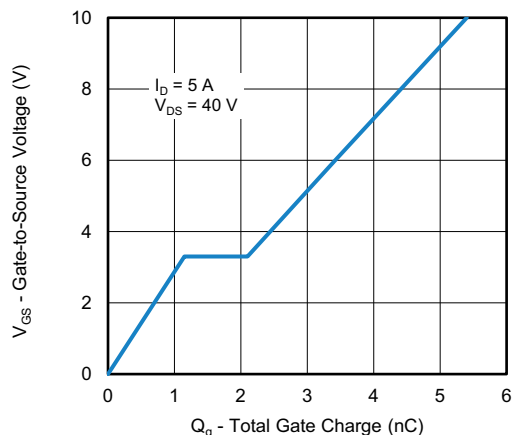


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		80	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 175 °C	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	5	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3 A	-	0.0728	0.0940	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3 A, T <sub>J</sub> = 125 °C	-	-	0.1607	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3 A, T <sub>J</sub> = 175 °C	-	-	0.1954	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 2.5 A	-	0.0855	0.1100	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3 A		-	9.6	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	252	355	pF
Output capacitance	C <sub>oss</sub>			-	46	65	
Reverse transfer capacitance	C <sub>rss</sub>			-	6.2	9.0	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 5 A	-	5.4	8.2	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	1.15	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	0.95	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.63	1.26	1.89	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 40 Ω I <sub>D</sub> ≡ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	5.0	10	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	3.0	6.0	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	13	20	
Fall time <sup>c</sup>	t <sub>f</sub>			-	4.0	8	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	29	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0 V		-	0.86	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 1 A, di/dt = 100 A/μs		-	16	32	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	10.5	21	nC
Reverse recovery fall time	t <sub>a</sub>			-	13	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	3	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.2	-	A

**Notes**

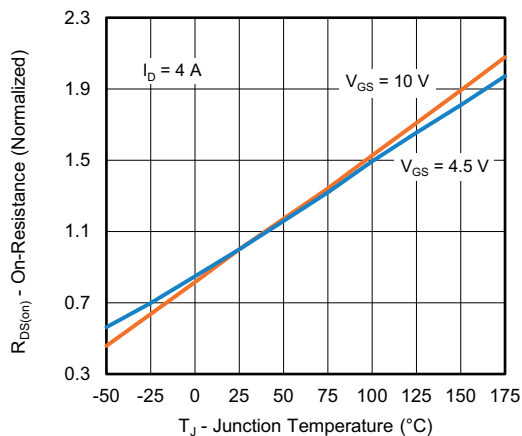
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

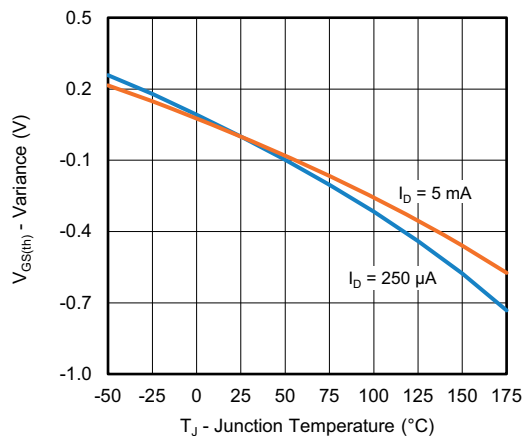
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**



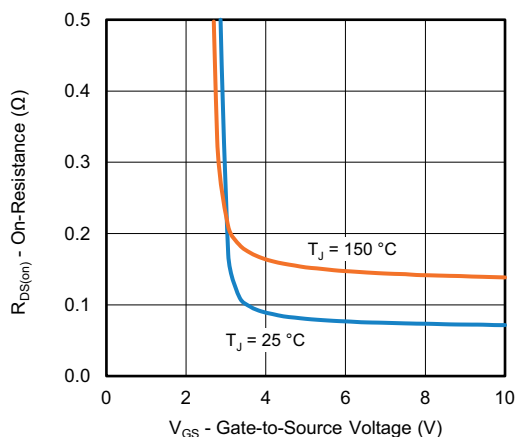
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



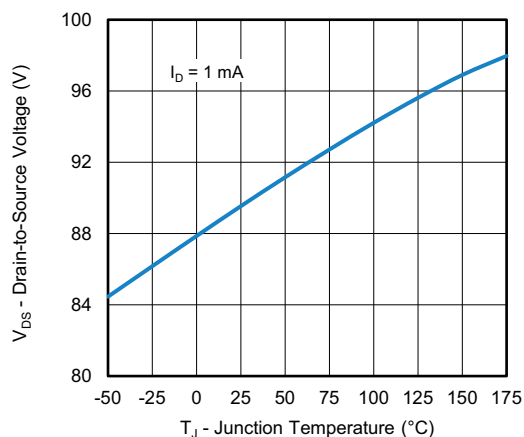
**On-Resistance vs. Junction Temperature**



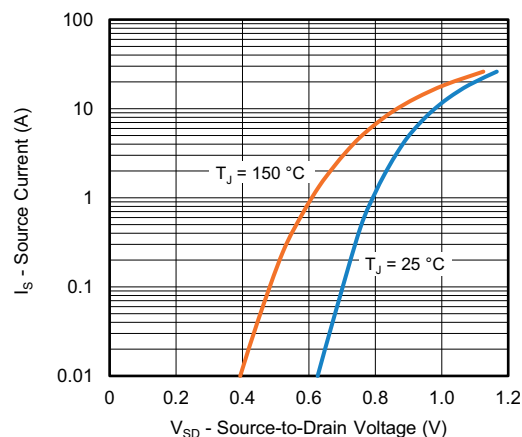
**Threshold Voltage**



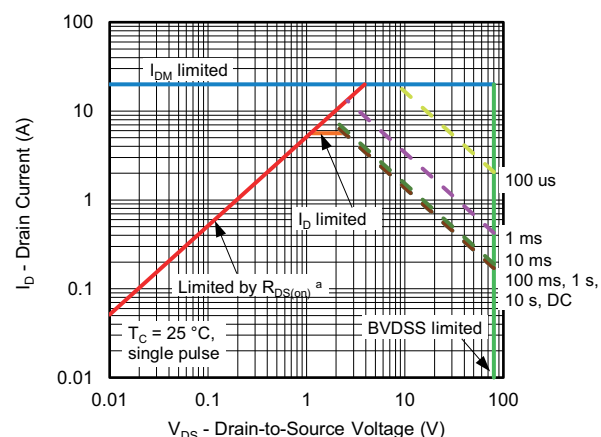
**On-Resistance vs. Gate-to-Source Voltage**



**Drain Source Breakdown vs. Junction Temperature**



**Source Drain Diode Forward Voltage**



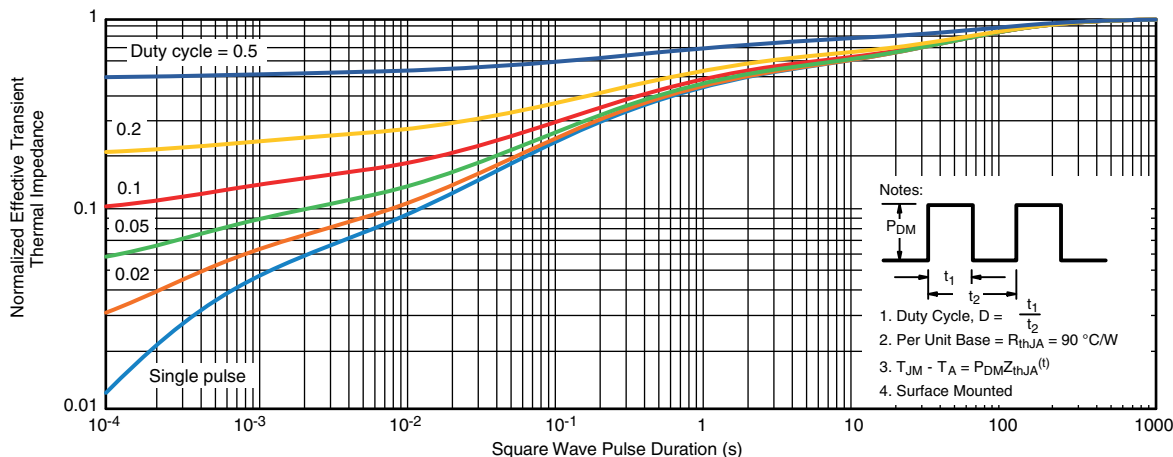
**Safe Operating Area**

**Note**

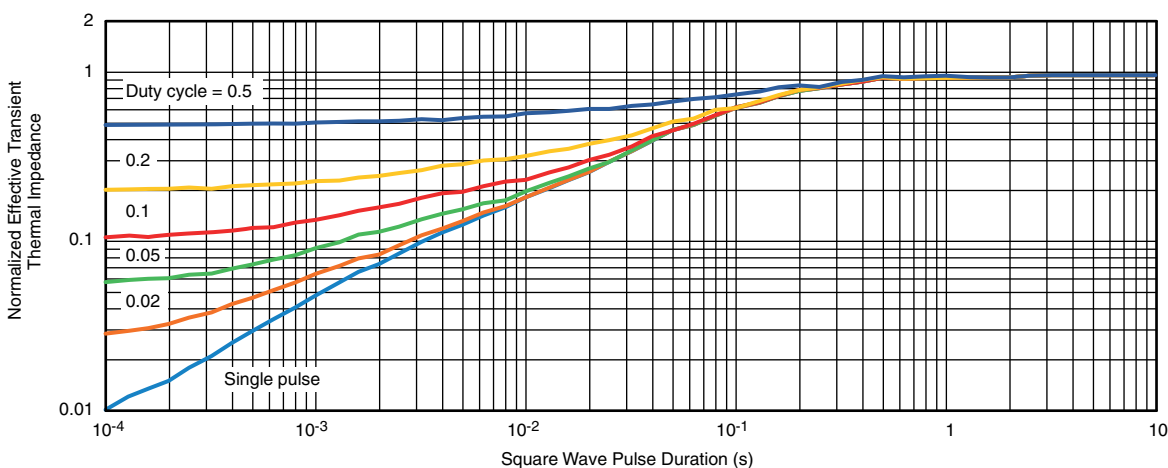
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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## PowerPAK® SC70W-6L SIDEWETTABLE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.10	-	-	0.004	-	-
b	0.25	0.30	0.35	0.010	0.012	0.014
b1	0.15	0.20	0.23	0.006	0.008	0.009
C	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.05	2.15	0.077	0.081	0.085
D1	0.88	0.98	1.08	0.035	0.039	0.043
D2	0.20	0.25	0.30	0.008	0.010	0.012
E	1.95	2.05	2.15	0.077	0.081	0.085
E1	1.06	1.16	1.26	0.042	0.046	0.050
E2	0.82	0.87	0.92	0.032	0.034	0.036
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
K	0.20 typ.			0.008 typ.		
K1	0.47 typ.			0.019 typ.		
K2	0.23 typ.			0.009 typ.		
K3	0.18 typ.			0.007 typ.		
K4	0.35 typ.			0.014 typ.		
K5	0.35 typ.			0.014 typ.		
K6	0.38 typ.			0.015 typ.		
L	0.15	0.25	0.35	0.006	0.010	0.014
L1	-	0.10	-	-	0.004	-

ECN: C19-1644-Rev. A, 10-Jan-2020  
DWG: 6076

### Notes

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating



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