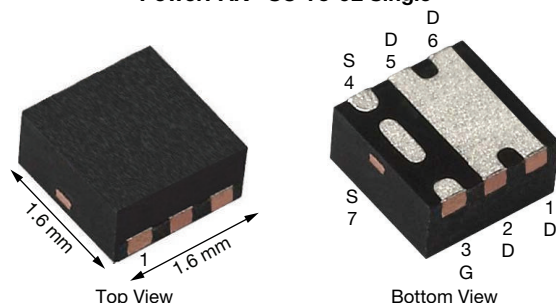


N-Channel 30 V (D-S) MOSFET

PowerPAK® SC-75-6L Single

Marking Code: AK

PRODUCT SUMMARY

V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.057
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.062
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.078
Q_g typ. (nC)	3.5
I_D (A) ^{a, c}	6
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SC-75
Lead (Pb)-free and halogen-free	SiB4316EDK-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 12	
Continuous drain current ($T_J = 150$ °C)	I_D	6^a	A
		6^a	
		$4.5^{b, c}$	
		$3.6^{b, c}$	
Pulsed drain current ($t = 300$ μ s)	I_{DM}	15	A
Continuous source-drain diode current	I_S	6^a	
		$1.63^{b, c}$	
Maximum power dissipation	P_D	10	W
		6.4	
		$1.95^{b, c}$	
		$1.25^{b, c}$	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	R_{thJA}	51	64	°C/W
Maximum junction-to-case (drain)	R_{thJC}	10	12.5	

Notes

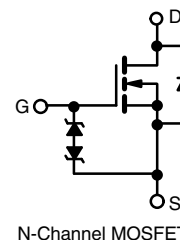
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state condition is 100 °C/W

FEATURES

- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
- Typical ESD protection: 1500 V (HBM)
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Portable devices such as smart phones, tablet PCs and mobile computing
 - Load switch
 - DC/DC converter
 - Power management



N-Channel MOSFET



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	34	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-3.3	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6	-	1.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 0.5	μA
		V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	± 20	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 4 A	-	0.047	0.057	Ω
		V _{GS} = 4.5 V, I _D = 3 A	-	0.051	0.062	
		V _{GS} = 2.5 V, I _D = 1 A	-	0.062	0.078	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 3 A	-	13	-	S
Dynamic ^b						
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 4 A	-	7.5	12	nC
Gate-source charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 4 A	-	3.5	5.5	
Gate-drain charge	Q _{gd}		-	1.8	-	
Gate resistance	R _g	f = 1 MHz	0.6	3.3	6.6	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 4.7 Ω I _D ≅ 3.2 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	20	40	ns
Rise time	t _r		-	60	120	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	45	90	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 4.7 Ω I _D ≅ 3.2 A, V _{GEN} = 10 V, R _g = 1 Ω	-	1.5	5	
Rise time	t _r		-	30	60	
Turn-off delay time	t _{d(off)}		-	15	30	
Fall time	t _f		-	50	100	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	3.9	A
Pulse diode forward current	I _{SM}		-	-	15	
Body diode voltage	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V	-	0.87	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 3.2 A, dI/dt = 100 A/μs, T _J = 25 °C	-	10	20	ns
Body diode reverse recovery charge	Q _{rr}		-	4	10	nC
Reverse recovery fall time	t _a		-	5.3	-	ns
Reverse recovery rise time	t _b		-	4.6	-	

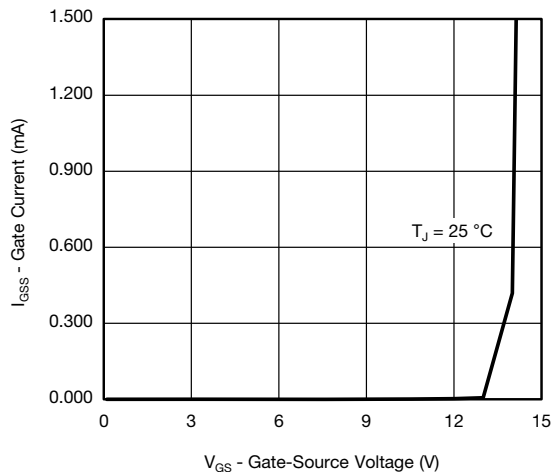
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

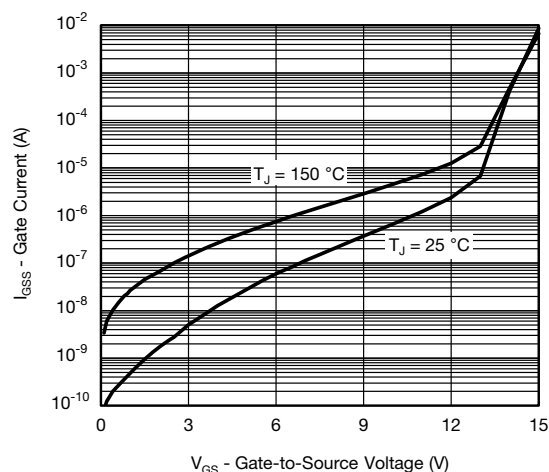
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



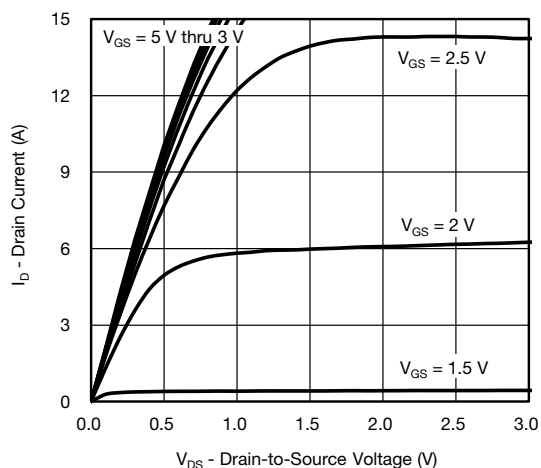
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



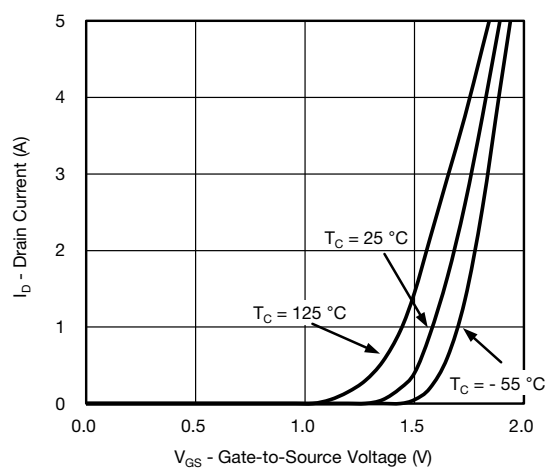
Gate Current vs. Gate-Source Voltage



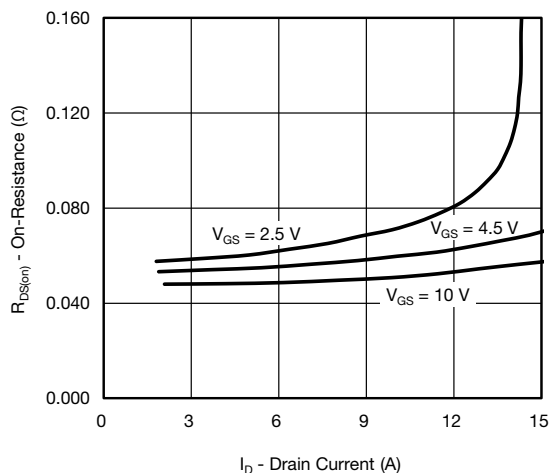
Gate Current vs. Gate-Source Voltage



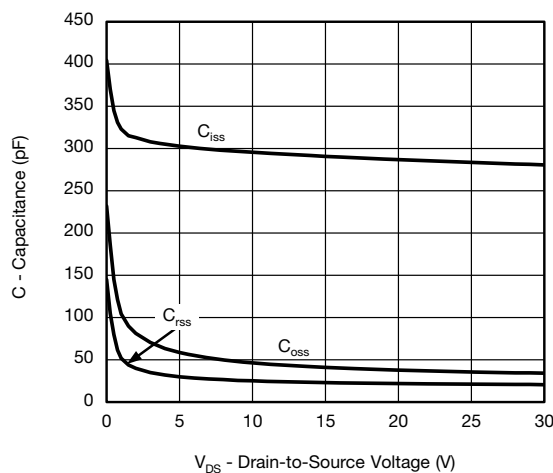
Output Characteristics



Transfer Characteristics



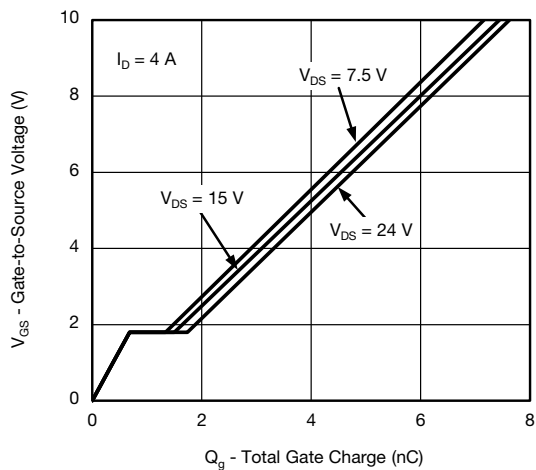
On-Resistance vs. Drain Current and Gate Voltage



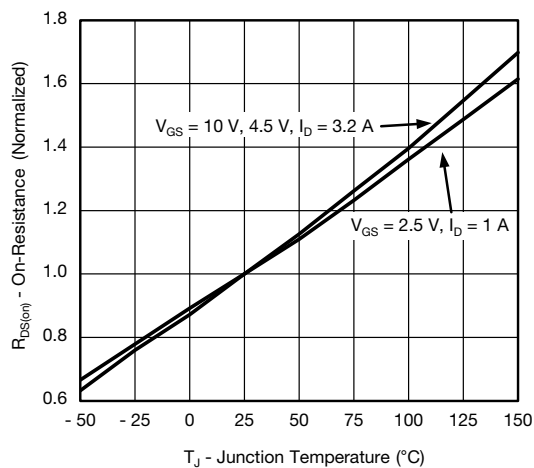
Capacitance



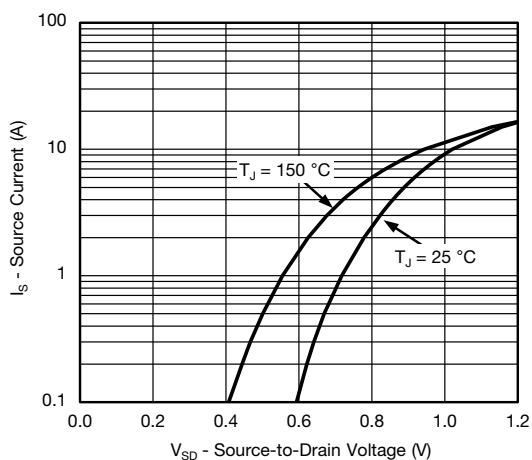
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



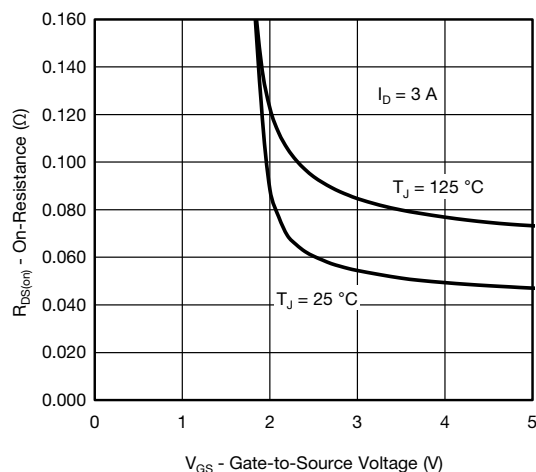
Gate Charge



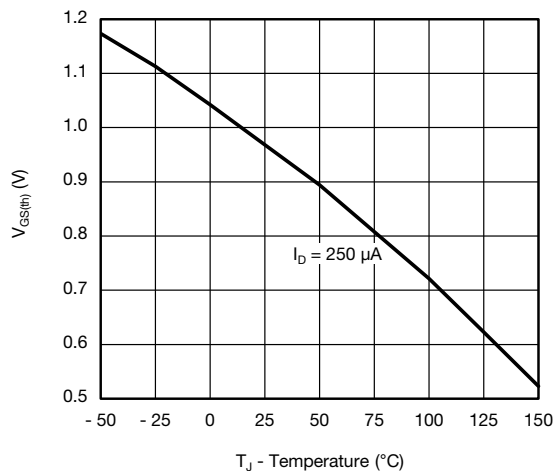
On-Resistance vs. Junction Temperature



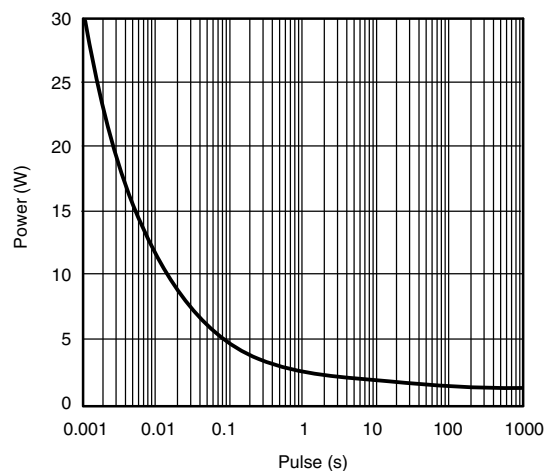
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



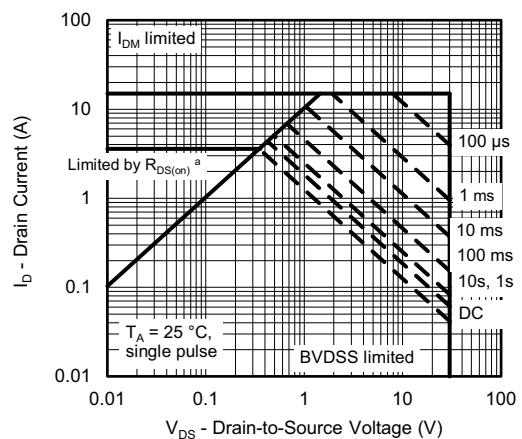
Threshold Voltage



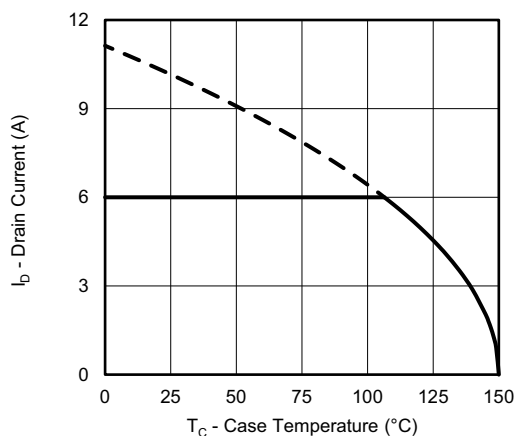
Single Pulse Power (Junction-to-Ambient)



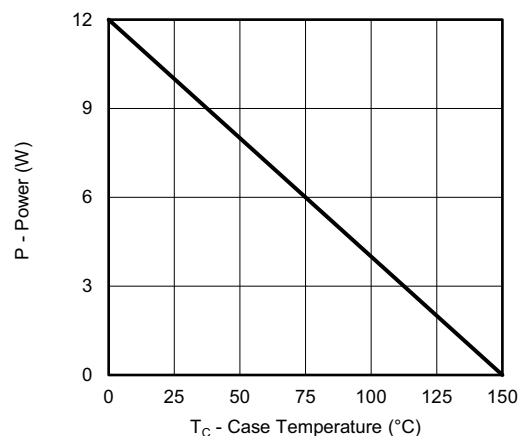
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating ^a



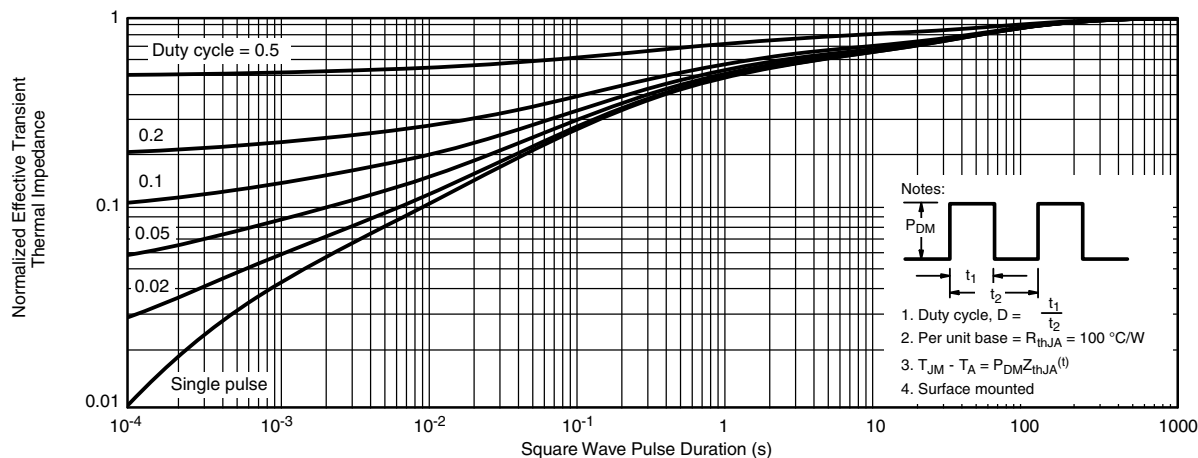
Power Derating

Note

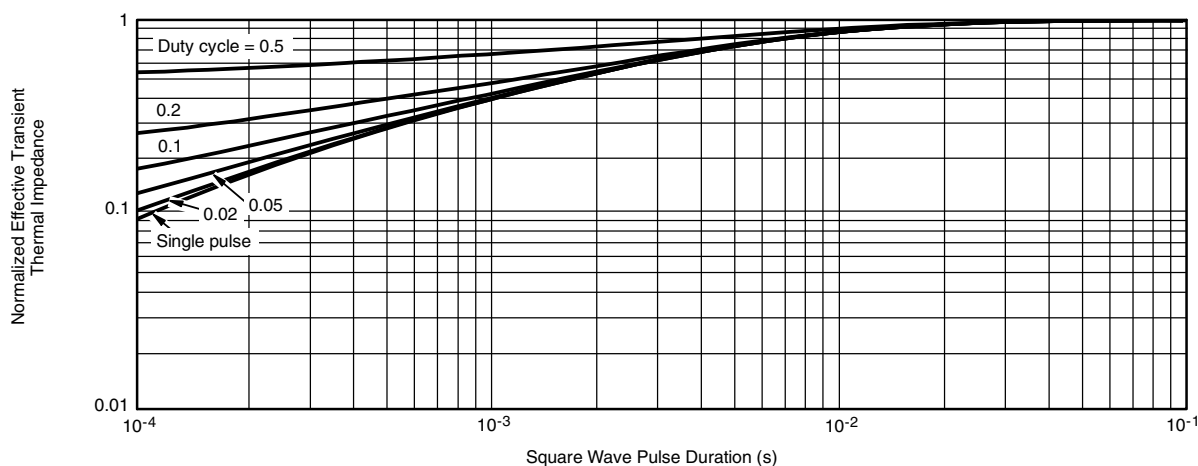
- a. The power dissipation P_D is based on $T_J(\text{max.}) = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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