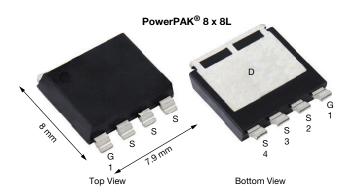


www.vishay.com

Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	80			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0014			
I _D (A)	430			
Configuration	Single			
Package	PowerPAK 8 x 8L			

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Thin 1.6 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



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N-Channel MOSFET	5

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	80	V	
Gate-source voltage		V_{GS}	± 20		
Continuous drain current	T _C = 25 °C	1	430		
	T _C = 125 °C	I _D	250		
Continuous source current (diode conduction)		I _S	450	Α	
Pulsed drain current ^a		I _{DM}	1200		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	65		
Single pulse avalanche energy	L=U.I IIII	E _{AS}	211	mJ	
Maximum power dissipation	T _C = 25 °C	D	600	W	
	T _C = 125 °C	P_{D}	200		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) ^c		-	260	C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount b	R _{thJA}	40	°C/W	
Junction-to-case (drain)		R _{thJC}	0.25	G/VV	

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		80	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	2	3	3.5	1 V	
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
		V _{GS} = 0 V	V _{DS} = 80 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ	
		$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 175 °C	-	-	500		
On-state drain current ^a	I _{D(on)}	$V_{GS} = 10 \text{ V}$	$V_{DS} \ge 5 V$	50	-	-	Α	
		$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$	-	0.0011	0.0014	Ω	
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = 10 \text{ V}$	I _D = 20 A, T _J = 125 °C	-	-	0.0026		
		$V_{GS} = 10 \text{ V}$	I _D = 20 A, T _J = 175 °C	-	-	0.0033		
Forward transconductance b	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		-	82	-	S	
Dynamic ^b								
Input capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	11 435	16 010	pF	
Output capacitance	Coss	$V_{GS} = 0 V$		-	1896	2655		
Reverse transfer capacitance	C _{rss}			-	92	130		
Total gate charge ^c	Q_g		V _{GS} = 10 V	-	181	272	nC	
Gate-source charge ^c	Q_{gs}	$V_{GS} = 10 \text{ V}$		-	51	-		
Gate-drain charge ^c	Q_{gd}			-	36	-		
Gate resistance	R_g	f = 1 MHz		0.7	1.3	2	Ω	
Turn-on delay time ^c	t _{d(on)}	$V_{DD} = 40 \text{ V}, \text{ R}_L = 0.8 \ \Omega,$ $I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \ \Omega$		-	21	28	ns	
Rise time ^c	t _r			-	80	105		
Turn-off delay time ^c	t _{d(off)}			-	65	85		
Fall time ^c	t _f			-	20	28		
Source-Drain Diode Ratings and Character	teristics ^b							
Pulsed current ^a	I _{SM}			-	-	1100	Α	
Forward voltage	V_{SD}	I _F = 40 A, V _{GS} = 0 V		-	0.7	1.2	V	
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs		-	72	144	ns	
Body diode reverse recovery charge	Q _{rr}			-	143	286	nC	
Reverse recovery fall time	t _a			-	41	-		
Reverse recovery rise time	t _b			-	30	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			_	3.5	_	Α	

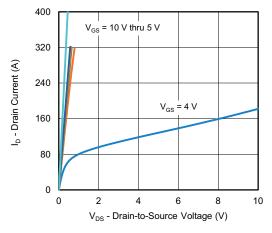
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

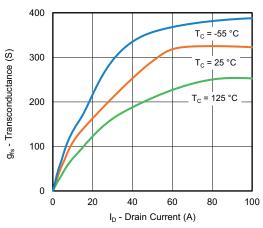
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



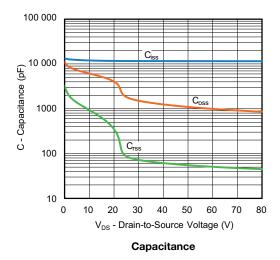
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

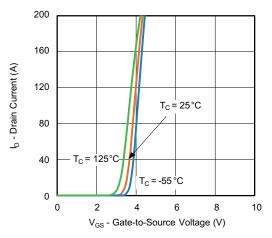


Output Characteristics

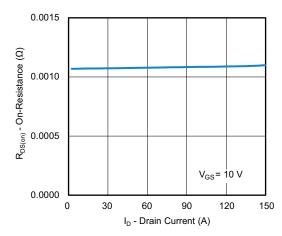


Transconductance

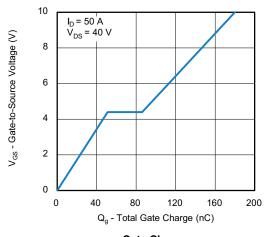




Transfer Characteristics

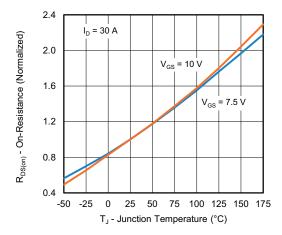


On-Resistance vs. Drain Current

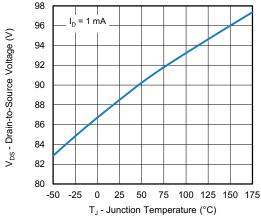




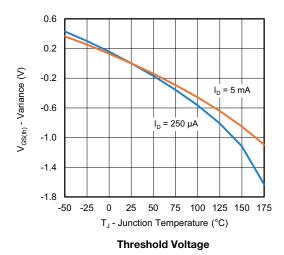
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



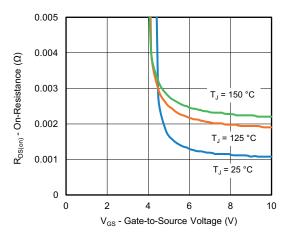
On-Resistance vs. Junction Temperature



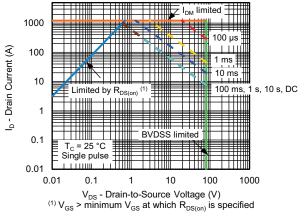
Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Safe Operating Area

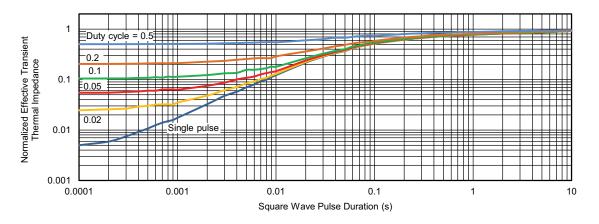
Note

a. $V_{GS} > minimum V_{GS}$ at which $R_{DS(on)}$ is specified

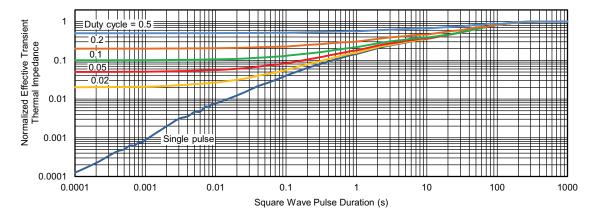
For technical questions, contact: automostechsu



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77102.



PowerPAK® 8 x 8L BWL Case Outline 2



INCHES			
MAX.			
0.067			
0.005			
0.030			
0.043			
0.046			
0.277			
0.012			
0.315			
0.272			
0.022			
0.106			
0.080			
0.319			
0.249			
0.174			
0.202			
0.157			
0.033			
0.030			
0.045			
0.020			
0.017			
0.026			
0.079			
5°			

ECN: S19-0643-Rev. B, 05-Aug-2019

DWG: 6073

Note

Millimeter will govern



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