COMPLIANT

HALOGEN

**FREE** 



# N-Channel 100 V (D-S) MOSFET



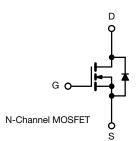
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	100			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0149			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	0.0185			
Q <sub>g</sub> typ. (nC)	8			
I <sub>D</sub> (A) <sup>a</sup>	40.7			
Configuration	Single			

#### **FEATURES**

- TrenchFET® Gen V power MOSFET
- Very low R<sub>DS</sub> x Q<sub>g</sub> figure-of-merit (FOM)
- Tuned for the lowest R<sub>DS</sub> x Q<sub>oss</sub> FOM
- 100 % R<sub>a</sub> and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

# **APPLICATIONS**

- · Synchronous rectification
- · Primary side switch
- DC/DC converters
- Power supplies
- Motor drive control



ORDERING INFORMATION							
Package	PowerPAK 1212-8S						
Lead (Pb)-free and halogen-free	SiSS5112DN-T1-GE3						
ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	LIMIT	UNIT				
Drain-source voltage	$V_{DS}$	100	V				

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	100	V
Gate-source voltage		V <sub>GS</sub>	± 20	V
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		40.7	
	T <sub>C</sub> = 70 °C	1 . 🗆	32.6	
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	11 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C	1	8.8 b, c	^
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	70	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		47.3	
	T <sub>A</sub> = 25 °C	I <sub>S</sub>	3.4 <sup>b, c</sup>	
Single pulse avalanche current	1 0.1 mall	I <sub>AS</sub>	20	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		52	
	T <sub>C</sub> = 70 °C		33.3	10/
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 b, c	W
	T <sub>A</sub> = 70 °C	1	2.4 <sup>b, c</sup>	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering recommendations (peak temperature) d, e			260	-0

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction to ambient <sup>b</sup>	t ≤ 10 s	$R_{thJA}$	24	33	°C/W		
Maximum junction to case (drain)	Steady state	$R_{thJC}$	1.9	2.4	C/VV		

#### **Notes**

- a.  $T_C = 25$  °C
- b. Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 81 °C/W



# Vishay Siliconix

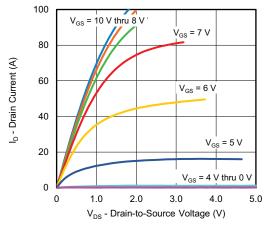
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				1	<u>'</u>		
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_{D} = 1 \text{ mA}$	100	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 10 mA	-	62	-	mV/°C	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-7.0	-		
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	-	4	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zana nata valtana dus' e e e e		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1	μА	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15		
Drain-source on-state resistance a	_	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.0124	0.0149	Ω	
	R <sub>DS(on)</sub>	$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0144	0.0185		
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	-	25	-	S	
Dynamic <sup>b</sup>						ı	
Input capacitance	C <sub>iss</sub>		-	790	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	310	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	7.3	-		
Total gate charge	Q <sub>g</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	10.6	16		
		, 40 , 5	-	8	12		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	4.5	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	0.92	-		
Output charge	Q <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	30	-		
Gate resistance	$R_{g}$	f = 1 MHz	0.4	1.0	1.7	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	9	18		
Rise time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_{L} = 5.0 \Omega$	-	4	8	1	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	11	22		
Fall time	t <sub>f</sub>		-	4	8		
Turn-on delay time	t <sub>d(on)</sub>		-	10	20	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_1 = 5.0 \Omega$	-	4	8		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	9	18		
Fall time	t <sub>f</sub>		-	4	8		
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous source-drain diode current	IS	T <sub>C</sub> = 25 °C	-	-	47.3	^	
Pulse diode forward current (t <sub>p</sub> = 100 μs)	I <sub>SM</sub>	-		-	70	Α	
Body diode voltage	$V_{SD}$	I <sub>S</sub> = 5 A	-	0.78	1.1	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	39	78	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	39	78	nC	
Reverse recovery fall time	ta	T <sub>J</sub> = 25 °C	-	23	-		
Reverse recovery rise time	t <sub>b</sub>		-	16	-	ns	

#### Notes

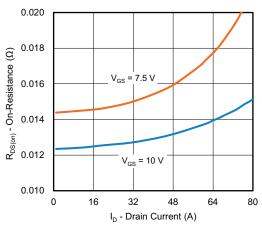
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

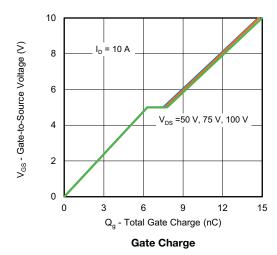


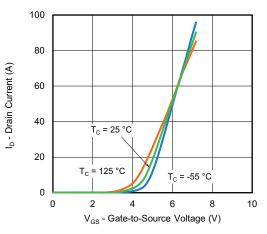


### **Output Characteristics**

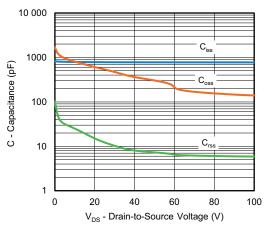


On-Resistance vs. Drain Current

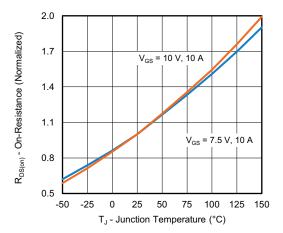




**Transfer Characteristics** 

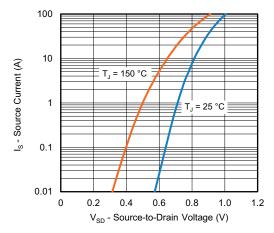


Capacitance

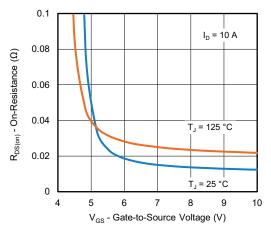


On-Resistance vs. Junction Temperature

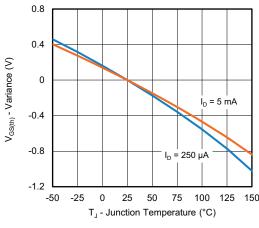




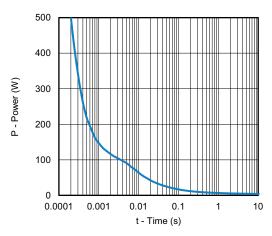
Source-Drain Diode Forward Voltage



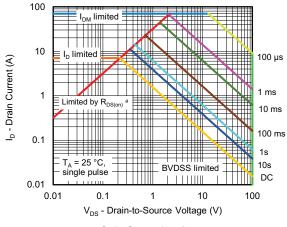
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power, Junction-to-Ambient



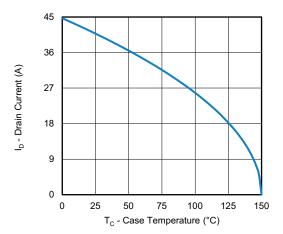
### Safe Operating Area

#### Note

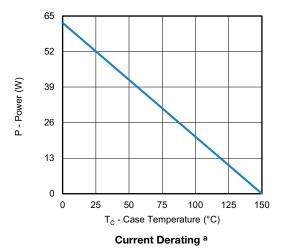
a.  $V_{GS} > minimum V_{GS}$  at which  $R_{DS(on)}$  is specified

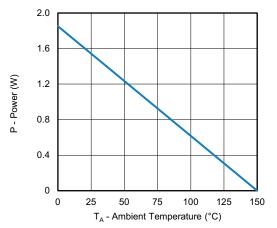
S23-0006-Rev. B, 16-Jan-2023





Power, Junction-to-Case



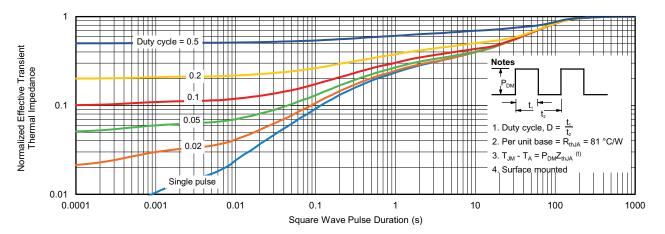


Power, Junction-to-Ambient

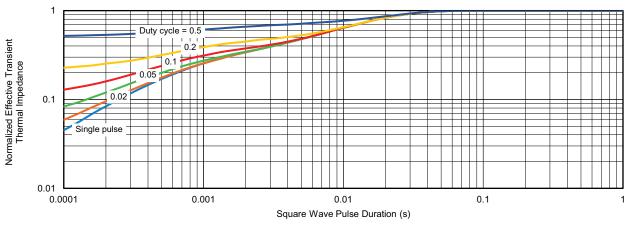
### Note

a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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