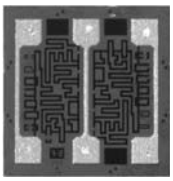
Nichrome Thin Film, Center Tapped Resistor Divider Network



Product may not be to scale

The CTN series is a center tapped nichrome resistor chip providing excellent stability at 250 mW power levels.

The CTN offers the designer flexibility in use as either a single value resistor or as two resistors with a center tap feature. The CTNs six bonding pads allows the user increased layout flexibility.

The CTNs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTNs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- Wire bondable
- Center tap feature
- Chip size: 0.030" x 0.030"
- Case: 0303
- Resistance range total: 10 Ω to 1 MΩ
- Ratio tolerances to: 0.1 %
- Resistor material: Nichrome
- Oxidized silicon substrate for good power dissipation
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

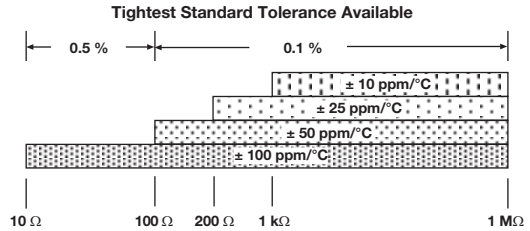
RoHS COMPLIANT

GREEN (5-2008)

APPLICATIONS

The CTN center-tapped resistor chips are used mainly in feedback circuits of amplifiers where ratio matching, high power and tracking between two resistors is critical.
Recommended for Hermetic environment where die is not exposed to moisture.
For low values, the resistance of the six bonding-pad configurations can vary, depending on the method of measurement used.
Vishay EFI measures low-value resistors by the four wire Kelvin technique.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Total Resistance Range	10 to 1M	Ω
Standard Tolerances	± 0.1, ± 0.5	%
TCR	± 10, ± 25, ± 50, ± 100	ppm/°C

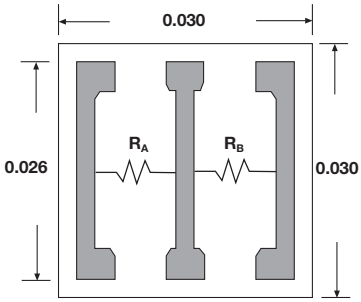


STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
TCR Tracking Between Halves (R_A/R_B) (1)	± 2	ppm/°C
Center Tap Ratio, R_A/R_B: Tolerance	1 ± 1 standard	%
Noise, MIL-STD-202, Method 308, 100 Ω to 250 kΩ	- 35 typ.	dB
Stability, 1000 h, + 125 °C, 125 mW	± 0.1 max. $\Delta R/R$	%
Operating Temperature Range	- 55 to + 125	°C
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at + 70 °C (derated to zero at + 175 °C)	0.25 max.	W

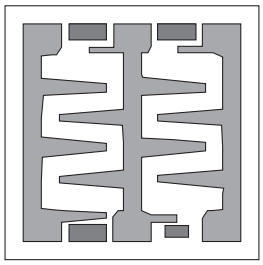
Note

(1) 20 ppm/°C for $R < 20$

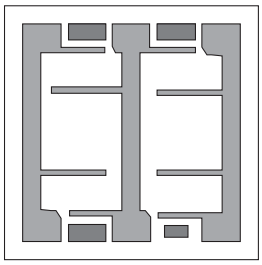
DIMENSIONS in inches



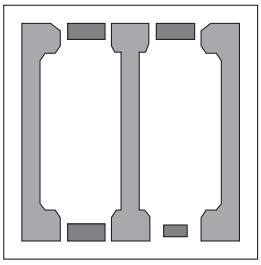
STANDARD CONFIGURATION
Six locations.All pads 0.005 x 0.005 inch



TYPICAL RANGE
10 Ω to 26 Ω

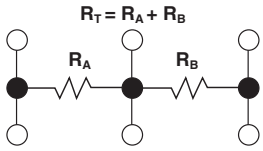


TYPICAL RANGE
27 Ω to 99 Ω



TYPICAL RANGE
100 Ω to 1 MΩ

SCHEMATIC



MECHANICAL SPECIFICATIONS

PARAMETER	VALUE
Chip Size	0.030" x 0.030" ± 0.002" (0.762 mm x 0.762 mm ± 0.050 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Resistor Material	Nichrome
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm) min.
Number of Pads	6
Pad Material	15 kÅ minimum gold (Al optional)
Backing	None, lapped semiconductor silicon (Au optional)

Options: Alphanumeric part marking, up to six characters.

GLOBAL PART NUMBER INFORMATION

Global Part Number: CTN50000KCKKGNHWS

Global Part Number Description: CTN 5K 10 % RT 0.25 % ± 100 ppm/°C ± 10 ppm/°C Au None H WS

C	T	N	5	0	0	0	0	K	C	K	K	G	N	H	W	S

MODEL	RESISTANCE (*R* TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TCR TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
CTN	First 4 digits are significant figures of resistance	**B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **J** = 5.0 **K** = 10.0	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **N** = No	**B** = ± 10 **E** = ± 25 **C** = ± 50 **K** = ± 100	**G** = ± 2 **J** = ± 5 **K** = ± 10 **N** = No	**G** = Au **A** = Al	**G** = Au **N** = None	**H** = Class H **K** = Class K	**WS** = Waffle pack 100 min., 1 mult

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