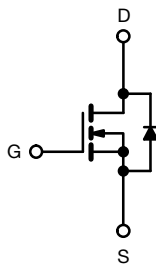
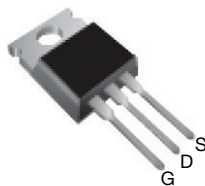


E Series Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
 - Power factor correction (PFC)
 - Two switch forward converter
 - Flyback converter
- Switch mode power supplies (SMPS)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.243
Q_g max. (nC)	66	
Q_{gs} (nC)	8	
Q_{gd} (nC)	14	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP15N50E-BE3 ^a
	SiHP15N50E-GE3

Note

a. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	28	
Linear Derating Factor		1.25	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	136	mJ
Maximum Power Dissipation	P_D	156	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	70	V/ns
Reverse Diode dV/dt ^d		27	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C


Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
 b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3.1$ A
 c. 1.6 mm from case
 d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C

**THERMAL RESISTANCE RATINGS**

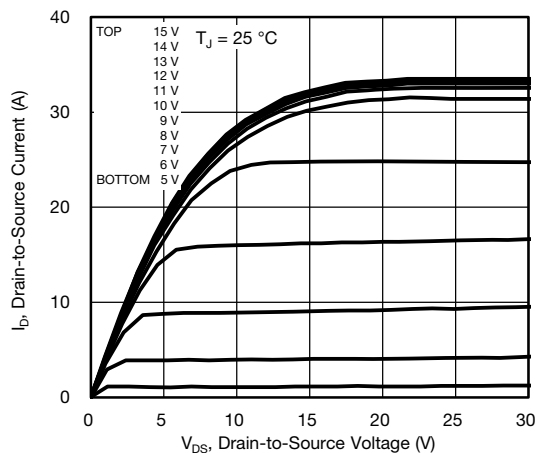
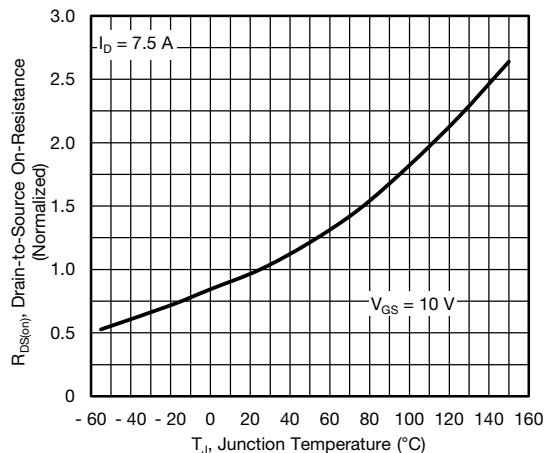
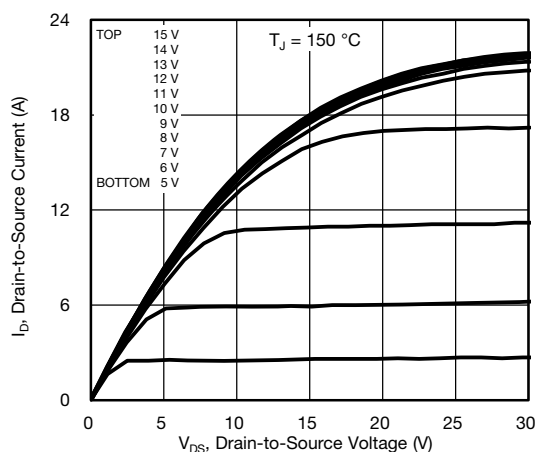
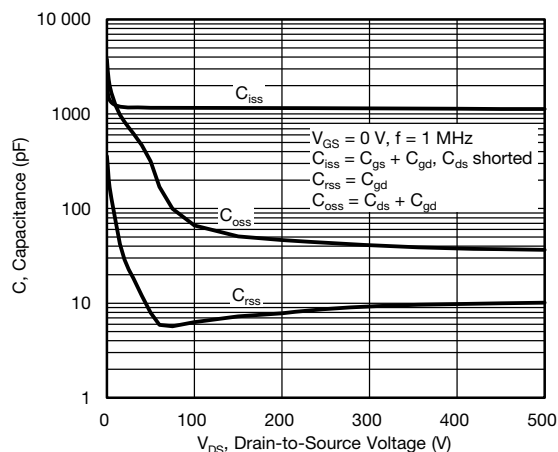
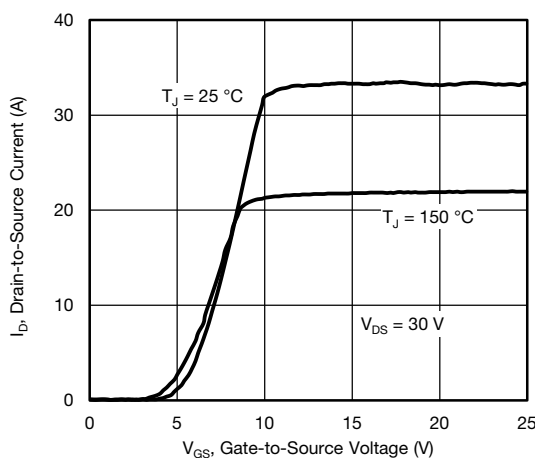
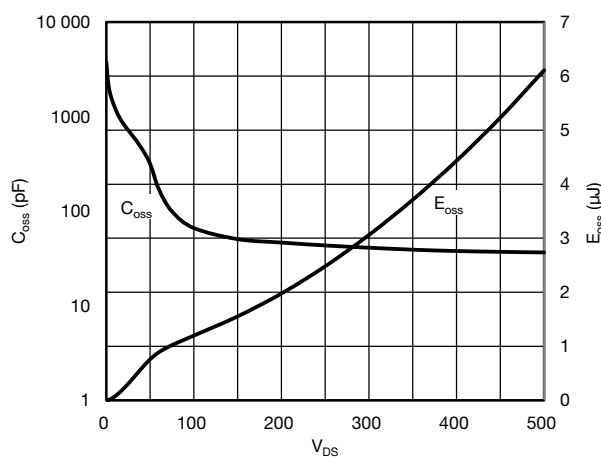
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.8	

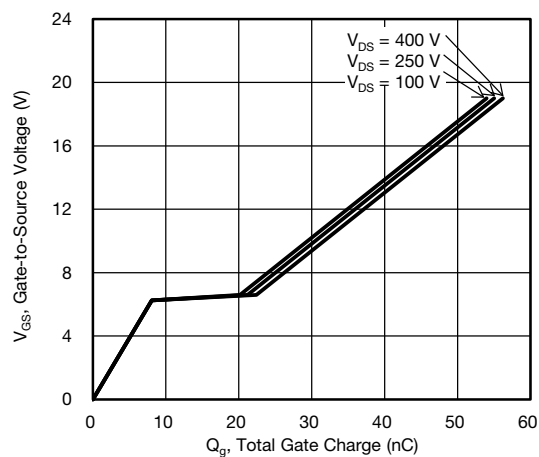
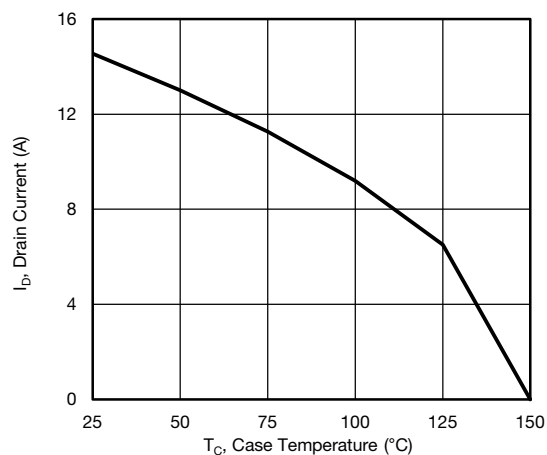
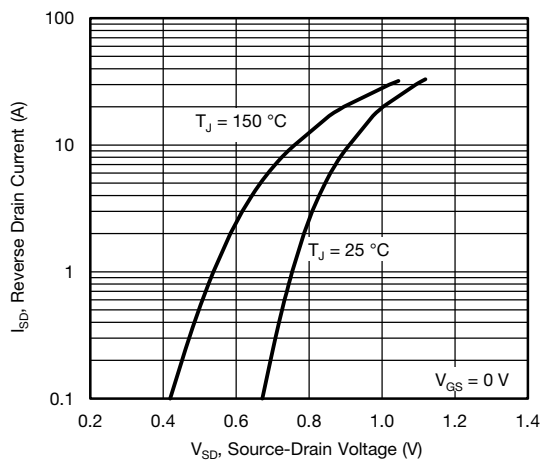
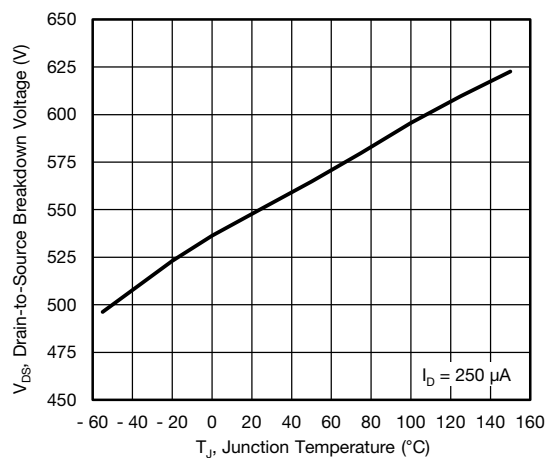
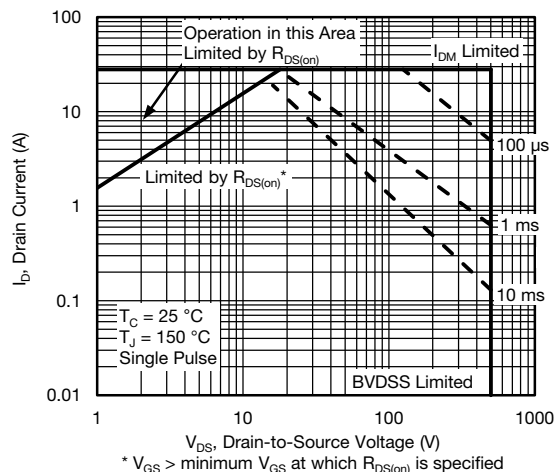
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

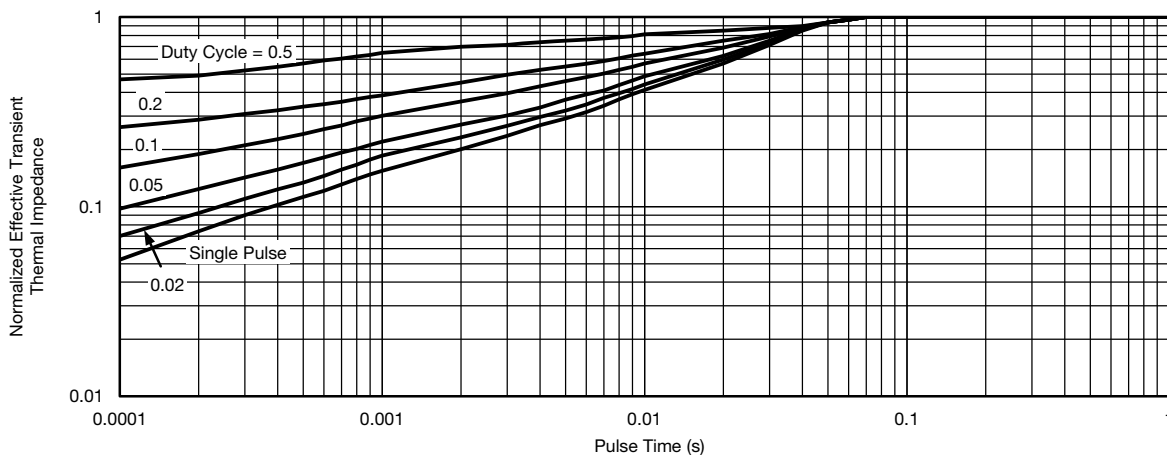
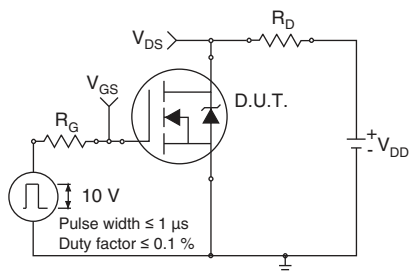
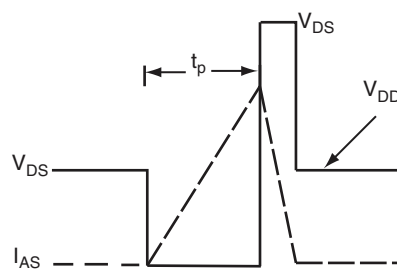
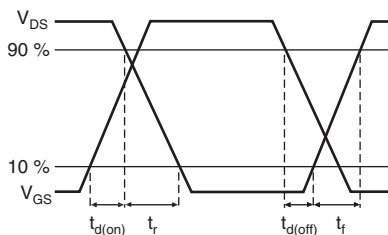
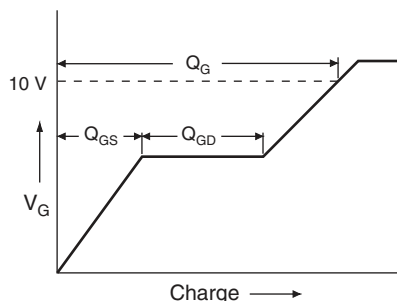
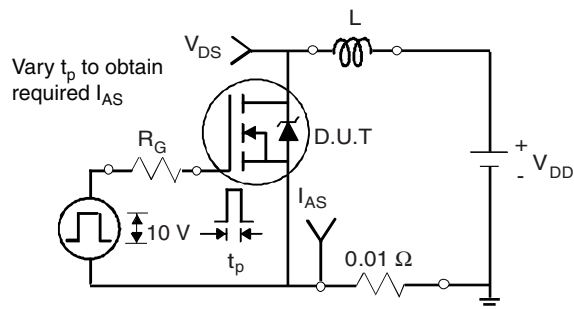
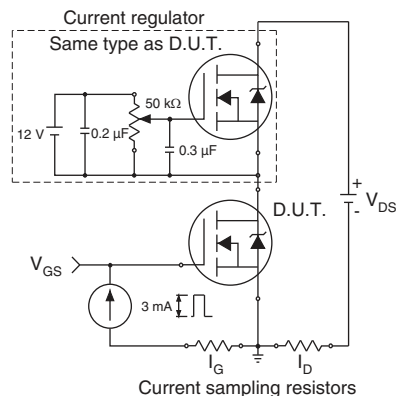
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.62	-	V/ $^{\circ}\text{C}$
Gate-source threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	25	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 7.5\text{ A}$	-	0.243	0.280	Ω
Forward transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 7.5\text{ A}$	-	3.9	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	1162	-	pF
Output capacitance	C_{oss}		-	51	-	
Reverse transfer capacitance	C_{rss}		-	7	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	55	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$		-	164	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 7.5\text{ A}$, $V_{DS} = 400\text{ V}$	-	33	66	nC
Gate-source charge	Q_{gs}		-	8	-	
Gate-drain charge	Q_{gd}		-	14	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	15	30	ns
Rise time	t_r		-	24	48	
Turn-off delay time	$t_{d(off)}$		-	34	68	
Fall time	t_f		-	18	36	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	-	0.85	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14.5	A
Pulsed diode forward current	I_{SM}		-	-	28	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 7.5\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 7.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	265	-	ns
Reverse recovery charge	Q_{rr}		-	3.2	-	μC
Reverse recovery current	I_{RRM}		-	23	-	A

Notes

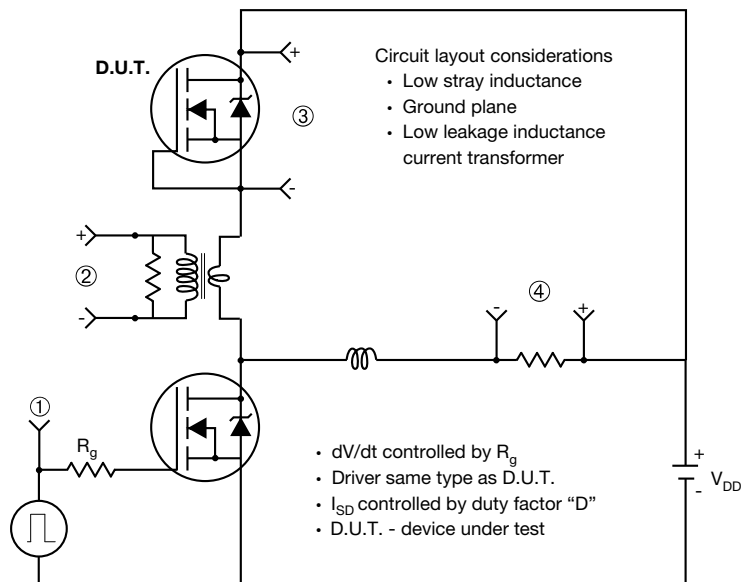
- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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