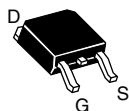
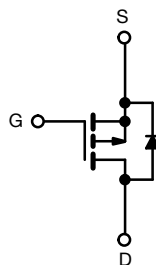
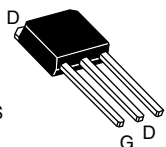


## Power MOSFET

**DPAK**  
(TO-252)

**IPAK**  
(TO-251)


P-Channel MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	-50	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10\text{ V}$	0.28
$Q_g$ max. (nC)	14	
$Q_{gs}$ (nC)	6.5	
$Q_{gd}$ (nC)	6.5	
Configuration	Single	

### FEATURES

- Surface mountable (order as IRFR9020, SiHFR9020)
- Straight lead option (order as IRFU9020, SiHFU9020)
- Repetitive avalanche ratings
- Dynamic  $dV/dt$  rating
- Simple drive requirements
- Ease of paralleling
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery  $dV/dt$ .

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface-mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of power MOSFET's to high volume applications where PC board surface mounting is desirable. The surface-mount option IRFR9020, SiHFR9020 is provided on 16mm tape. The straight lead option IRFU9020, SiHFU9020 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

### ORDERING INFORMATION

PACKAGE	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR9020-GE3	SiHFR9020TR-GE3 <sup>a</sup>	SiHFR9020TRL-GE3 <sup>a</sup>	SiHFU9020-GE3
	IRFR9020TRLPBF-BE3 <sup>ab</sup>	-	-	-
Lead (Pb)-free	IRFR9020PbF	IRFR9020TRPbF <sup>a</sup>	IRFR9020TRLPbF <sup>a</sup>	IRFU9020PbF

#### Notes

- a. See device orientation  
b. "-BE3" denotes alternate manufacturing location

**ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	-50	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{DM}$	-40	
Linear derating factor		0.33	W/ $^{\circ}\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	250	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	-9.9	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	4.2	mJ
Maximum power dissipation	$P_D$	42	W
Peak diode recovery $dV/dt$ <sup>c</sup>	$dV/dt$	5.8	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^{\circ}\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	for 10 s	300	

**Notes**

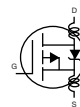
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16)  
b.  $V_{DD} = -25\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 5.1\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ , peak  $I_L = -9.9\text{ A}$   
c.  $I_{SD} \leq -9.9\text{ A}$ ,  $dI/dt \leq -120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 40\text{ V}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$   
d. 0.063" (1.6 mm) from case  
e. When mounted on 1" square PCB (FR-4 or G-10 material)

**THERMAL RESISTANCE RATINGS**


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	-	110	$^{\circ}\text{C}/\text{W}$
Case-to-sink	$R_{thCS}$	-	1.7	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	-	3.0	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	- 50	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -50\text{ }\mu\text{A}$	- 2.0	-	- 4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 500$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = \text{max. rating}$ , $V_{GS} = 0\text{ V}$	-	-	250	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{max. rating}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	-	1000	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$ , $I_D = 5.7\text{ A}$ <sup>b</sup>	-	0.20	0.28	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} \leq -50\text{ V}$ , $I_{DS} = -5.7\text{ A}$	2.3	3.5	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = -25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 9	-	490	-	pF
Output capacitance	$C_{oss}$		-	320	-	
Reverse transfer capacitance	$C_{rss}$		-	70	-	
Total gate charge	$Q_g$	$V_{GS} = -10\text{ V}$ , $I_D = -9.7\text{ A}$ , $V_{DS} = 0.8 \times \text{max. rating}$ , see fig. 18 (Independent operating temperature)	-	9.4	14	nC
Gate-source charge	$Q_{gs}$		-	4.3	6.5	
Gate-drain charge	$Q_{gd}$		-	4.3	6.5	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -25\text{ V}$ , $I_D = -9.7\text{ A}$ , $R_g = 18\text{ }\Omega$ , $R_D = 2.4\text{ }\Omega$ , see fig. 17 (Independent operating temperature)	-	8.2	12	ns
Rise time	$t_r$		-	57	66	
Turn-off delay time	$t_{d(off)}$		-	12	18	
Fall time	$t_f$		-	25	38	
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact.	-	4.5	-	nH
Internal source inductance	$L_S$		-	7.5	-	



**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-source body diode characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-9.9	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$		-	-	-40	
Body diode voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = -9.9\text{ A}$ , $V_{GS} = 0\text{ V}$ <sup>b</sup>	-	-	-6.3	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = -9.7\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ <sup>b</sup>	56	110	280	ns
Body diode reverse recovery charge	$Q_{rr}$		0.17	0.34	0.85	nC
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 16)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$

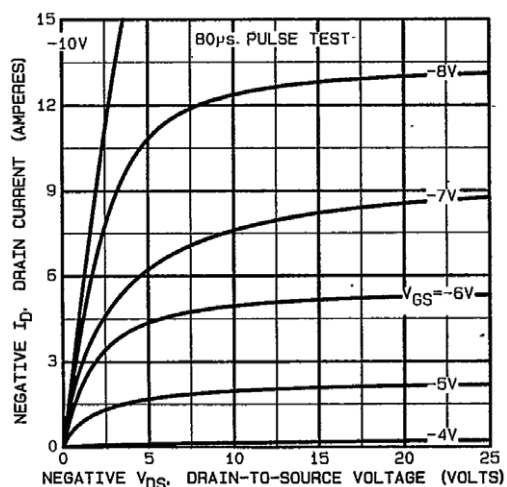
**TYPICAL CHARACTERISTICS** ( $25^\circ\text{C}$ , unless otherwise noted)

Fig. 1 - Typical Output Characteristics

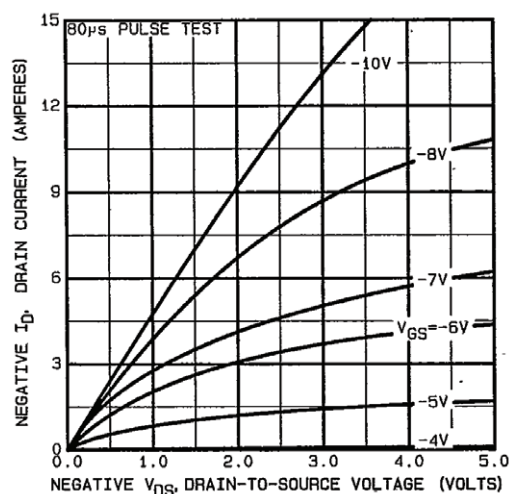


Fig. 3 - Typical Saturation Characteristics

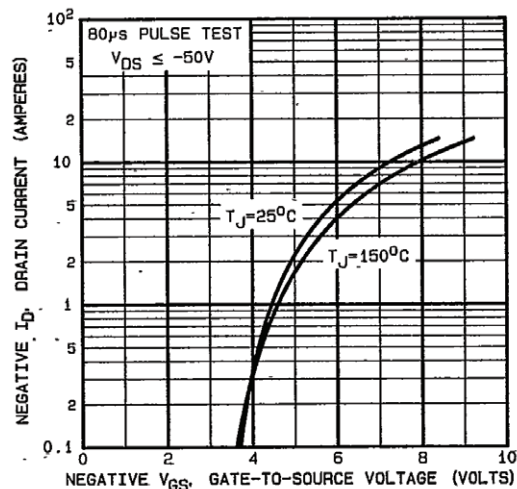


Fig. 2 - Typical Transfer Characteristics

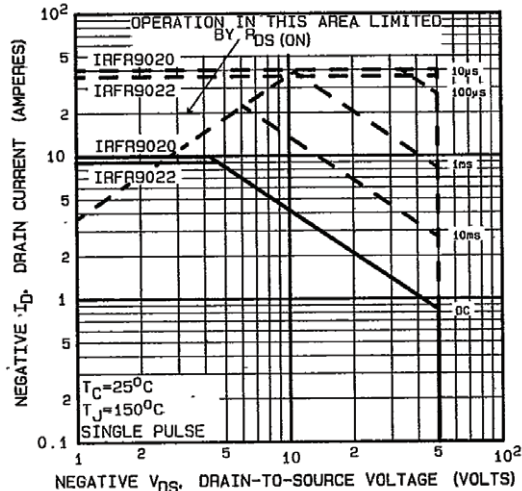


Fig. 4 - Maximum Safe Operating Area

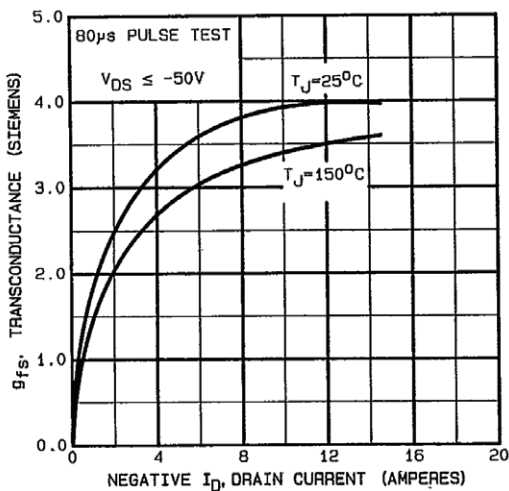


Fig. 5 - Typical Transconductance vs. Drain Current

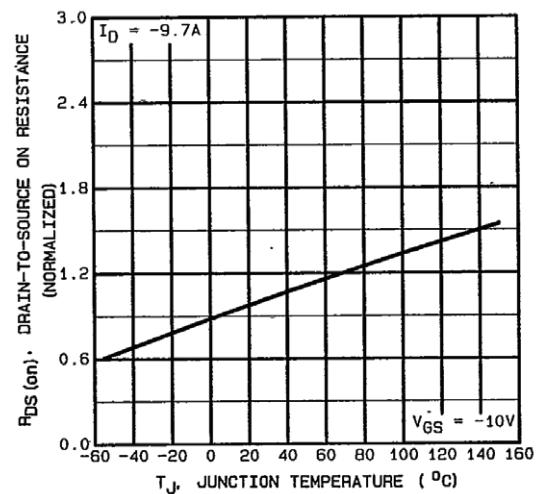


Fig. 8 - Breakdown Voltage vs. Temperature

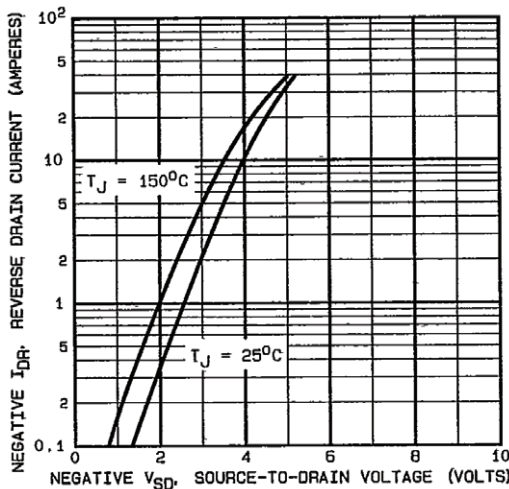


Fig. 6 - Typical Source-Drain Diode Forward Voltage

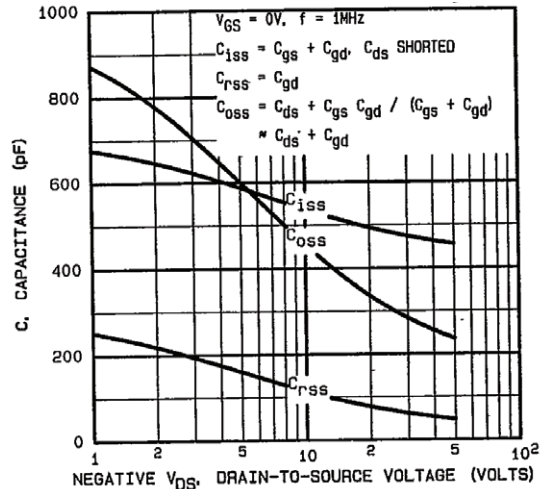


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

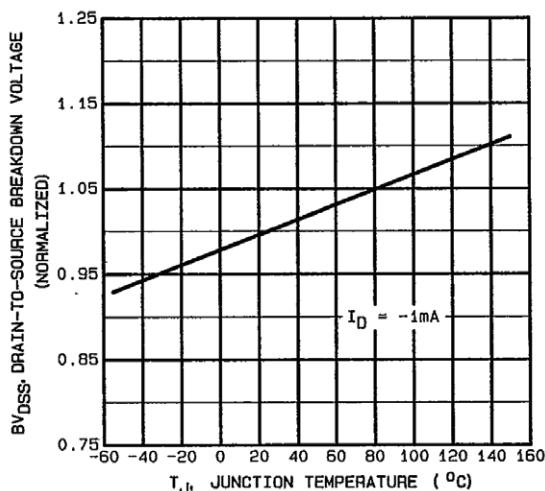


Fig. 7 - Breakdown Voltage vs. Temperature

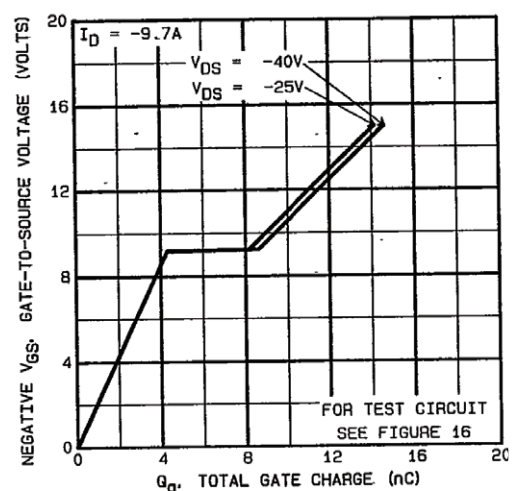


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

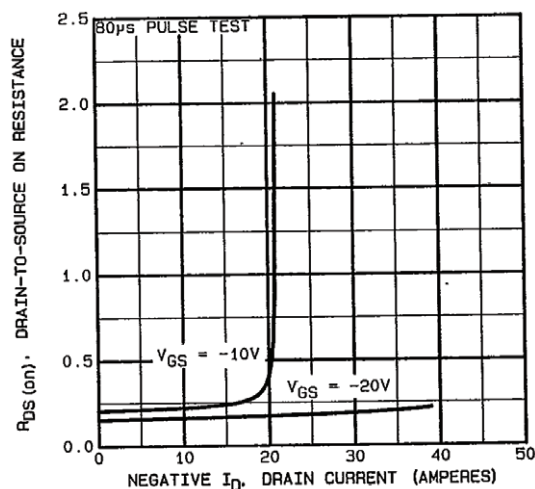


Fig. 11 - Typical On-Resistance vs. Drain Current

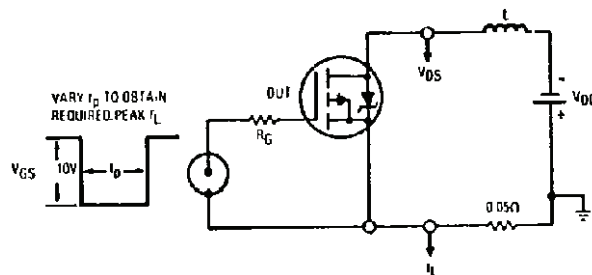


Fig. 14 - Unclamped Inductive Test Circuit

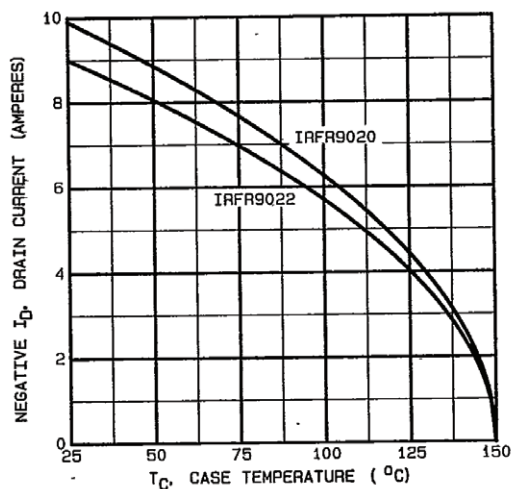


Fig. 12 - Maximum Drain Current vs. Case Temperature

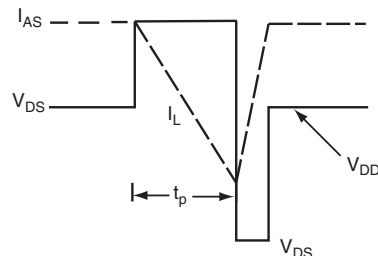


Fig. 15 - Unclamped Inductive Waveforms

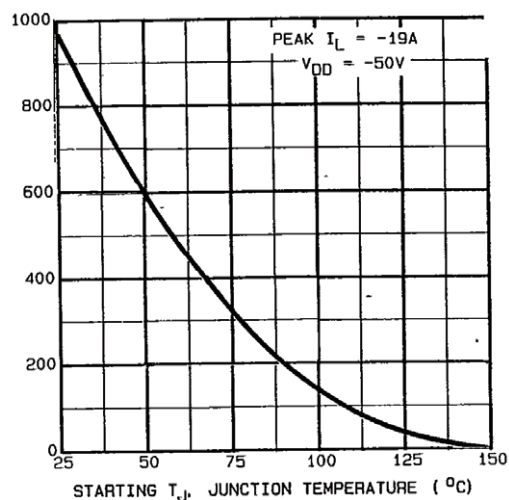


Fig. 13 - Maximum Avalanche vs. Starting Junction Temperature

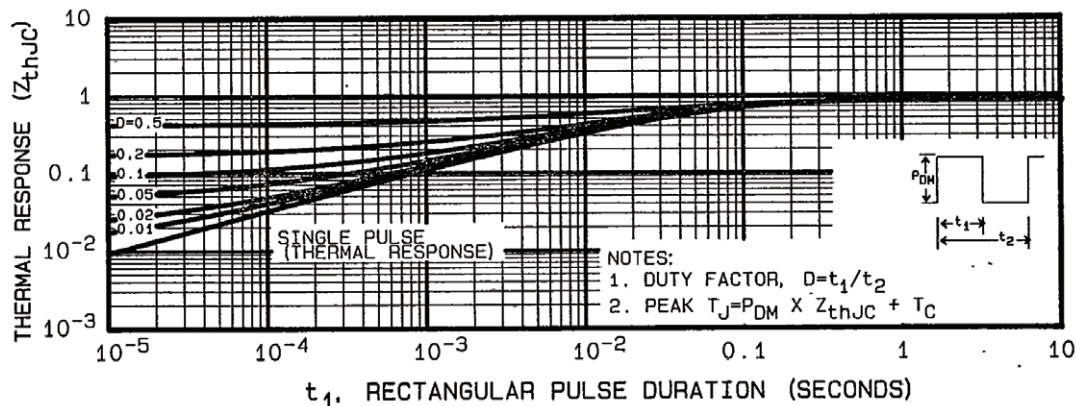


Fig. 16 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

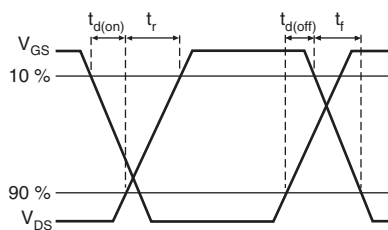


Fig. 17 - Switching Time Waveforms

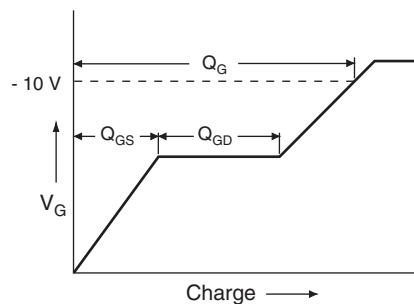


Fig. 19 - Basic Gate Charge Waveform

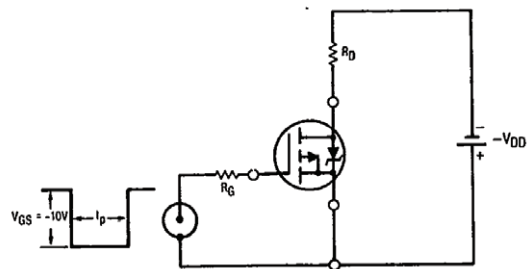


Fig. 18 - Switching Time Test Circuit

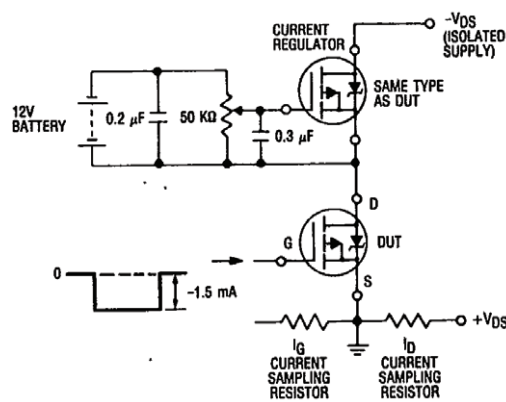
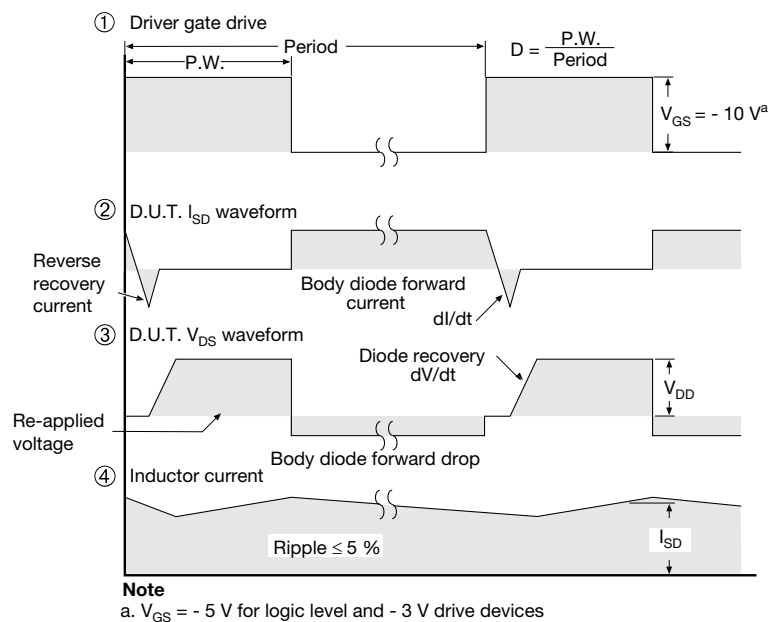
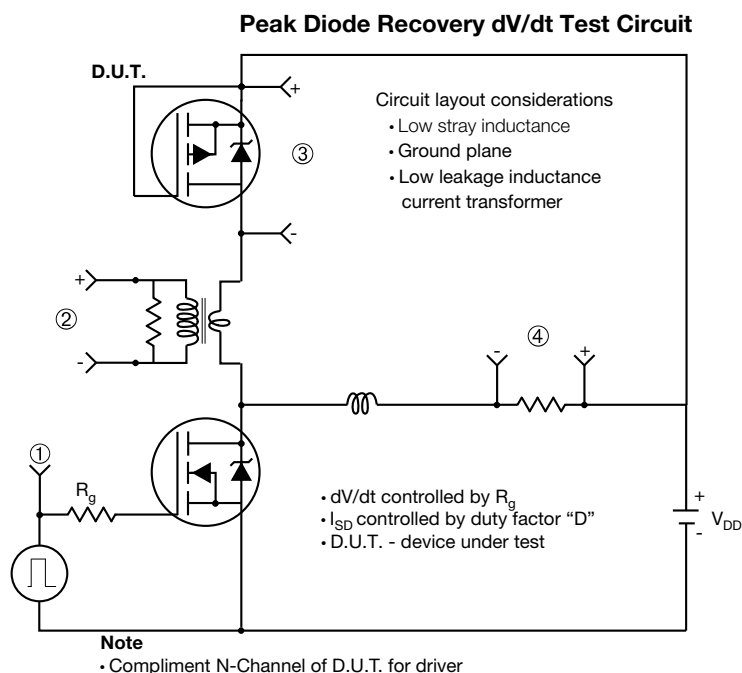


Fig. 20 - Gate Charge Test Circuit



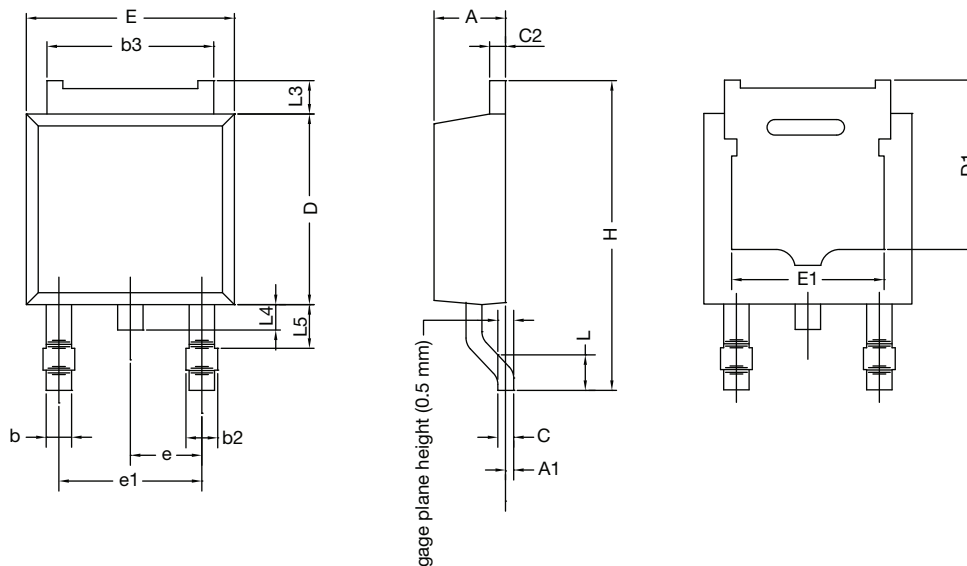


**Fig. 21 - For P-Channel**

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## TO-252AA Case Outline

### VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

#### Note

- Dimension L3 is for reference only





## VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

### Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022  
DWG: 5347

## Case Outline for TO-251AA (High Voltage)

### OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: E21-0682-Rev. C, 27-Dec-2021

DWG: 5968

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



## OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
theta1	0°	7.5°	15°
theta2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021  
DWG: 5968

### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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