

Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5\text{ V}$	0.20
Q_g max. (nC)	8.4	
Q_{gs} (nC)	3.5	
Q_{gd} (nC)	6.0	
Configuration	Single	

FEATURES

- Advanced process technology
- Surface-mount
- 175 °C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient reliable device for use in a wide variety of applications.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHLZ14S-GE3	SiHLZ14STRL-GE3 ^a	SiHLZ14STRR-GE3 ^a
Lead (Pb)-free	IRLZ14SPbF	IRLZ14STRLPbF ^a	IRLZ14STRRPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage ^e	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 10	
Continuous drain current	I_D	$T_C = 25\text{ °C}$	A
		$T_C = 100\text{ °C}$	
Pulsed drain current ^{a, e}	I_{DM}	40	
Linear derating factor		0.29	W/°C
Single pulse avalanche energy ^{b, e}	E_{AS}	68	mJ
Maximum power dissipation	P_D	$T_C = 25\text{ °C}$	W
		$T_A = 25\text{ °C}$	
Peak diode recovery dv/dt ^{c, e}	dv/dt	4.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 790\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 10\text{ A}$ (see fig. 12)
- $I_{SD} \leq 10\text{ A}$, $di/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ °C}$
- 1.6 mm from case
- Uses IRLZ14, SiHLZ14 data and test conditions


**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	40	°C/W
Maximum junction-to- case (drain)	R _{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.07	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0	-	2.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 10 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C	-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 5 V, I _D = 6.0 A ^b	-	-	0.2	Ω
		V _{GS} = 4 V, I _D = 5.0 A ^b	-	-	0.28	
Forward transconductance	g _{fs}	V _{DS} = 25 V, I _D = 6.0 A	3.5	-	-	S
Dynamic						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	400	-	pF
Output capacitance	C _{oss}		-	170	-	
Reverse transfer capacitance	C _{rss}		-	42	-	
Total gate charge	Q _g	V _{GS} = 5 V, I _D = 10 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	8.4	nC
Gate-source charge	Q _{gs}		-	-	3.5	
Gate-drain charge	Q _{gd}		-	-	6.0	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, I _D = 10 A, R _g = 12 Ω, R _D = 2.8 Ω, see fig. 10 ^b	-	9.3	-	ns
Rise time	t _r		-	110	-	
Turn-off delay time	t _{d(off)}		-	17	-	
Fall time	t _f		-	26	-	
Internal source inductance	L _S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	10	A
Pulsed diode forward current ^a	I _{SM}		-	-	40	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V ^b	-	-	1.6	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 10 A, di/dt = 100 A/μs ^b	-	93	130	ns
Body diode reverse recovery charge	Q _{rr}		-	340	650	nC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

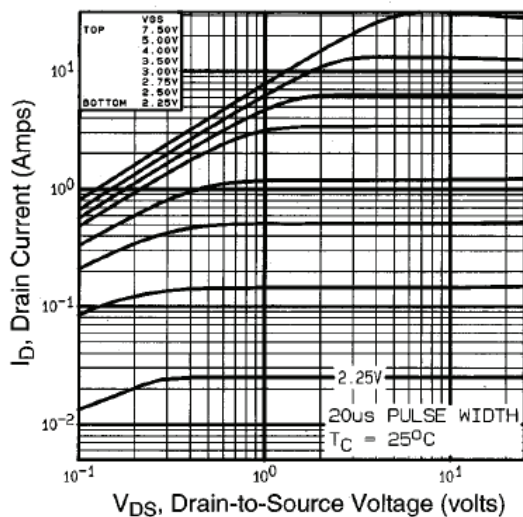


Fig. 1 - Typical Output Characteristics

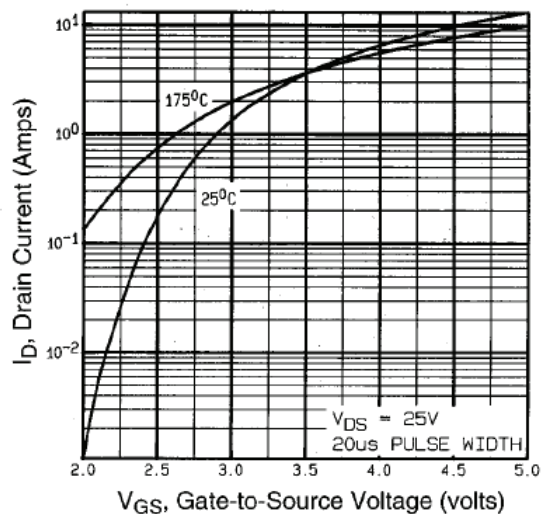


Fig. 3 - Typical Transfer Characteristics

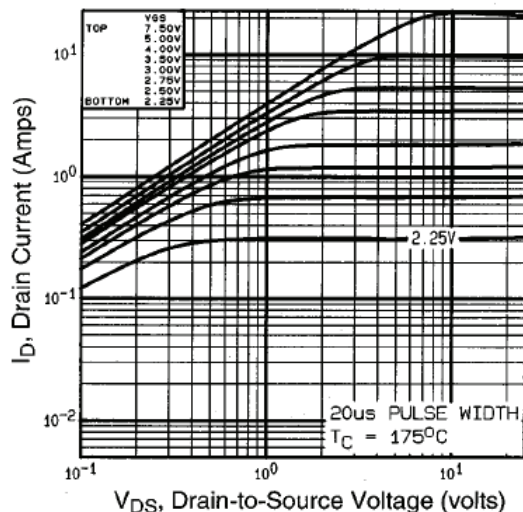


Fig. 2 - Typical Output Characteristics

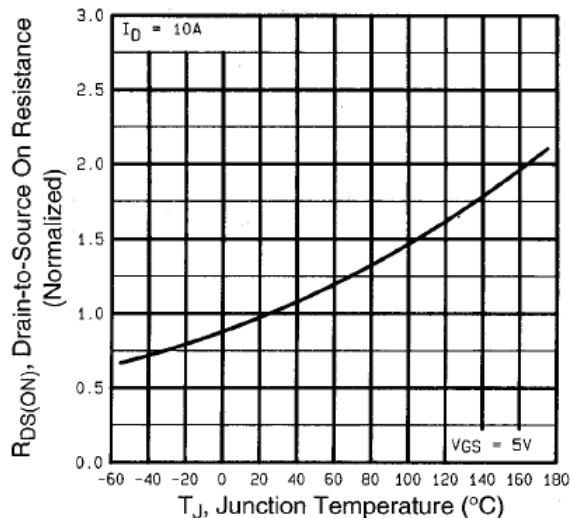
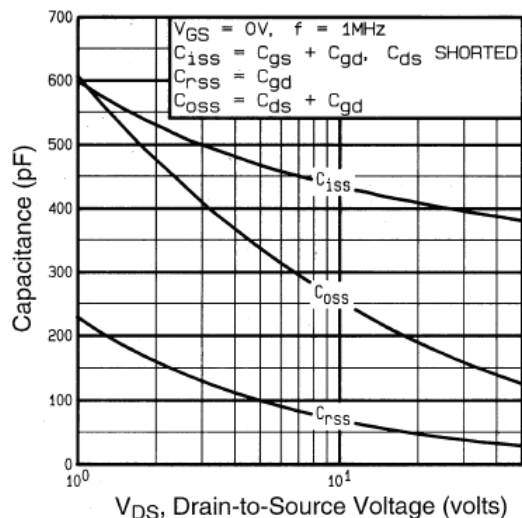
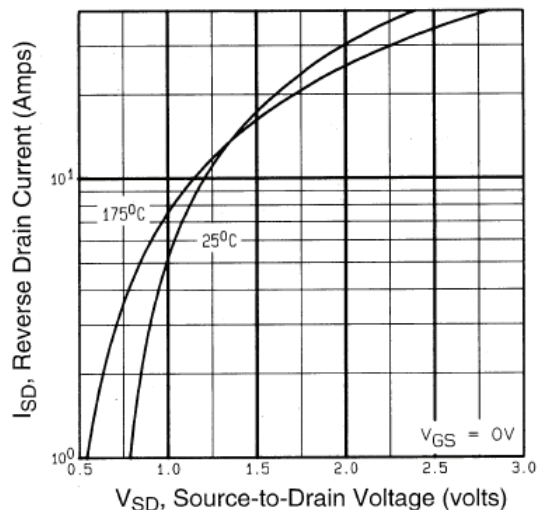
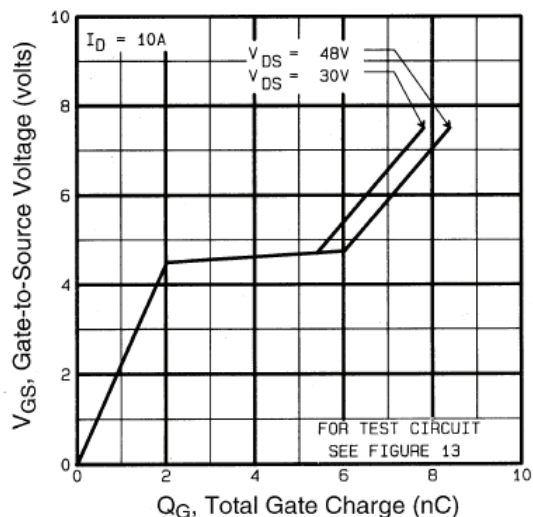
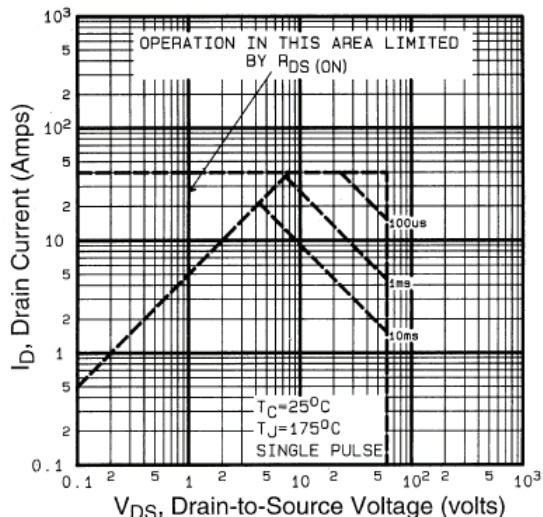
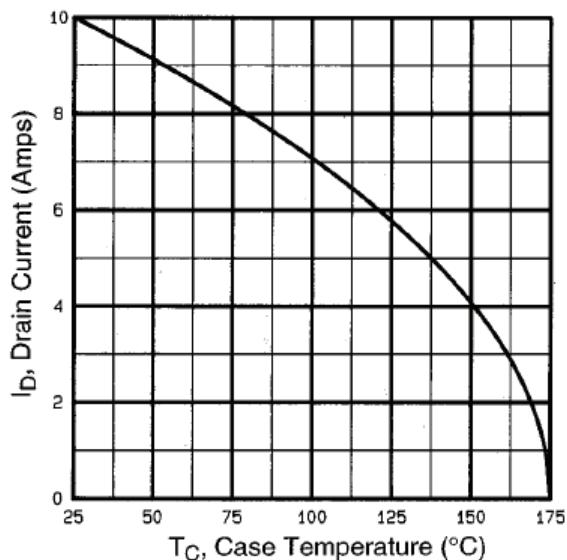
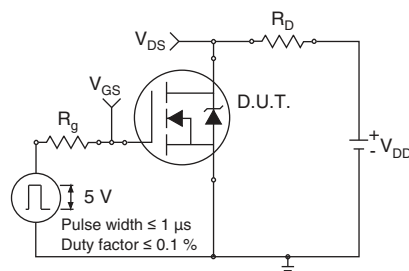
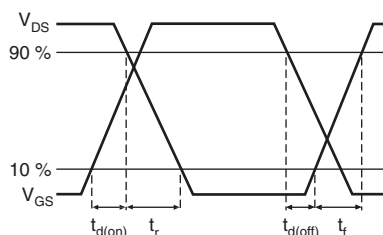
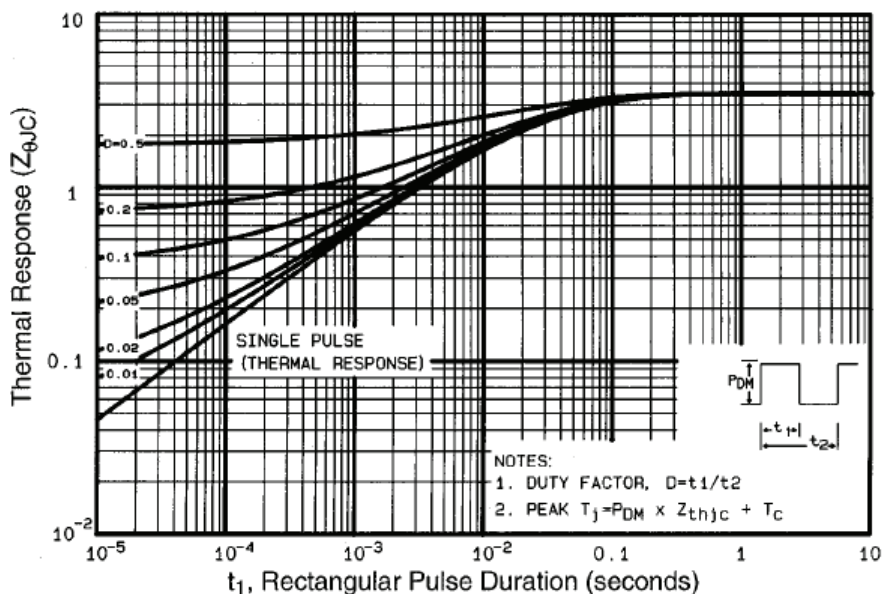
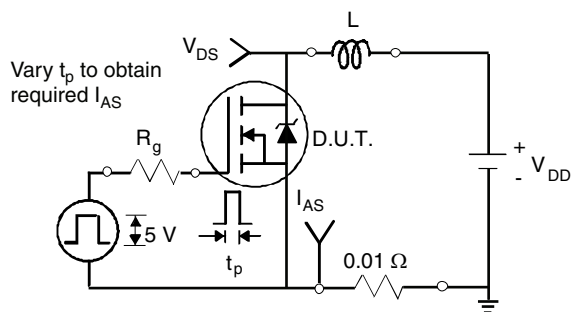
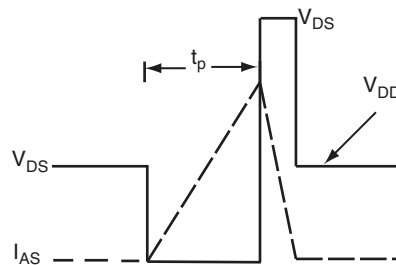
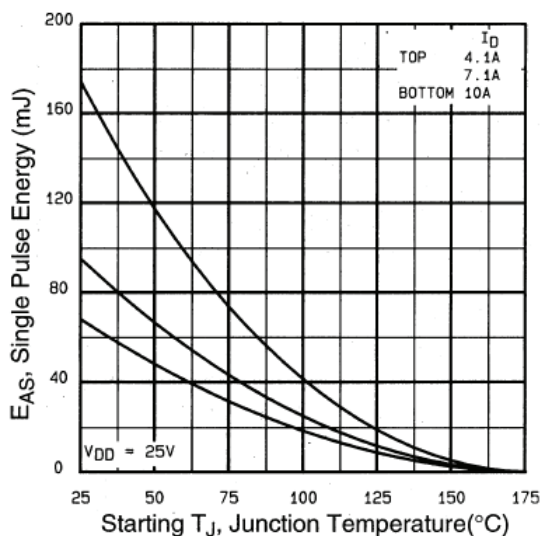
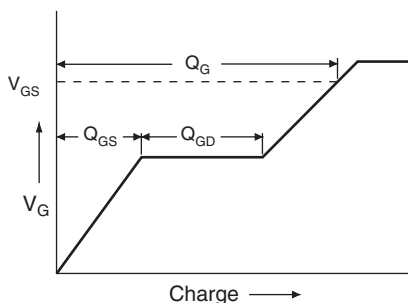
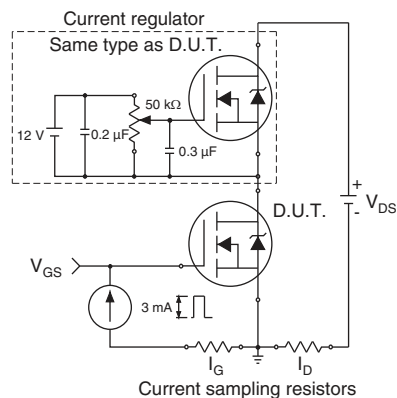
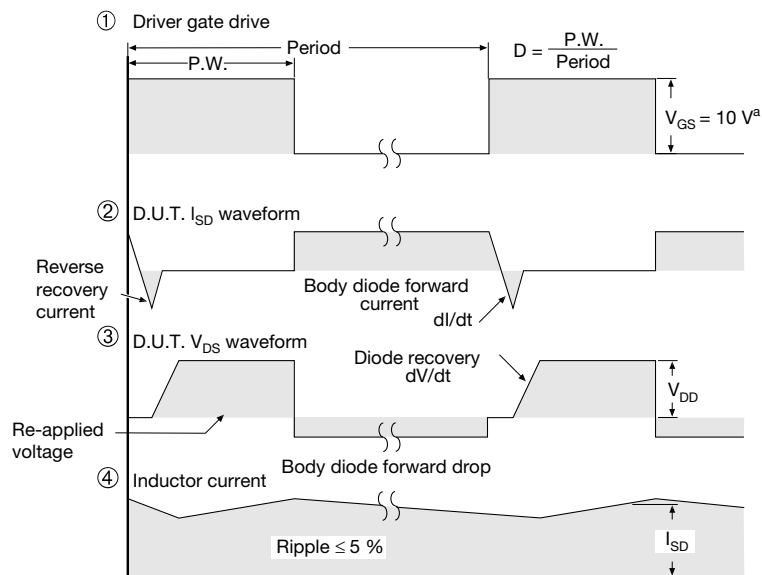
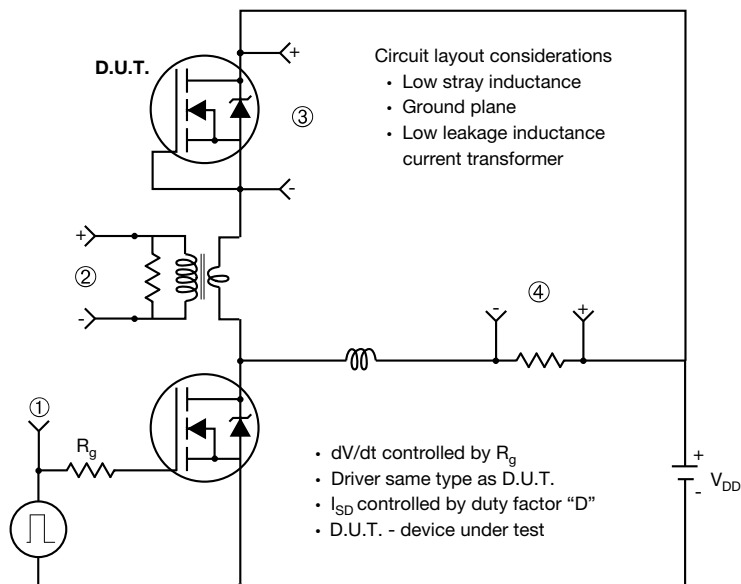


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

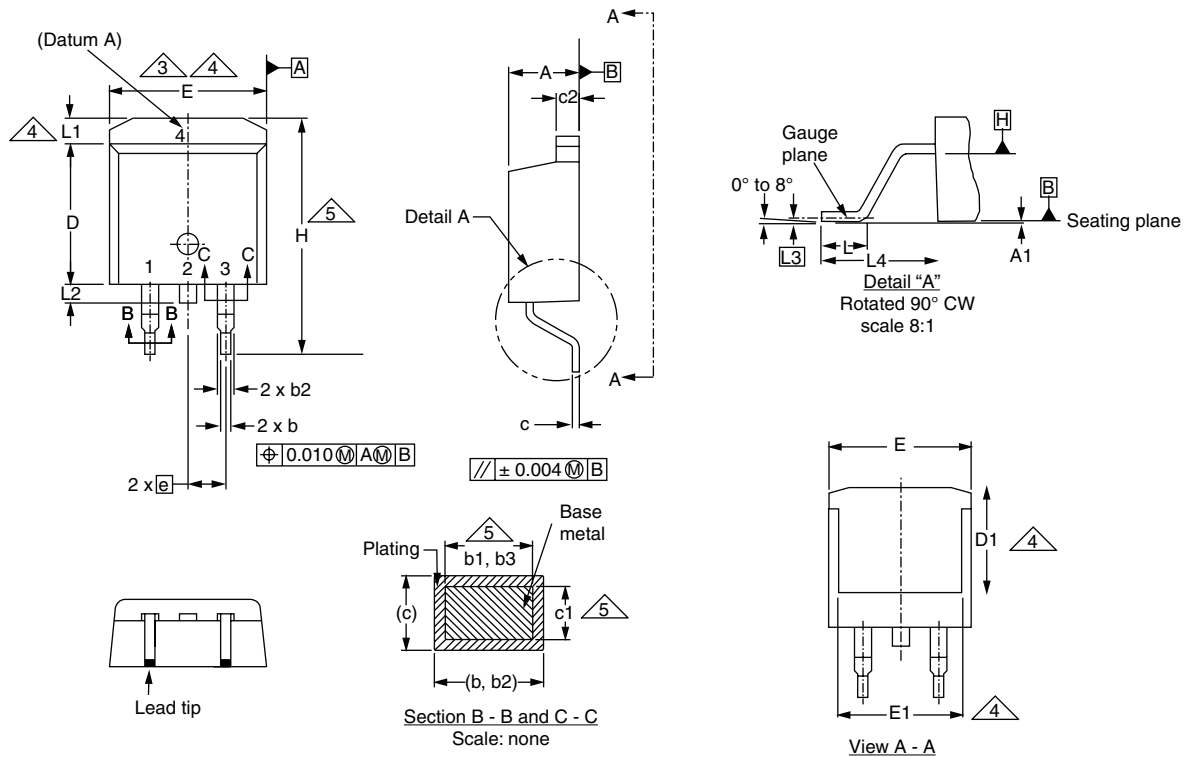
Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

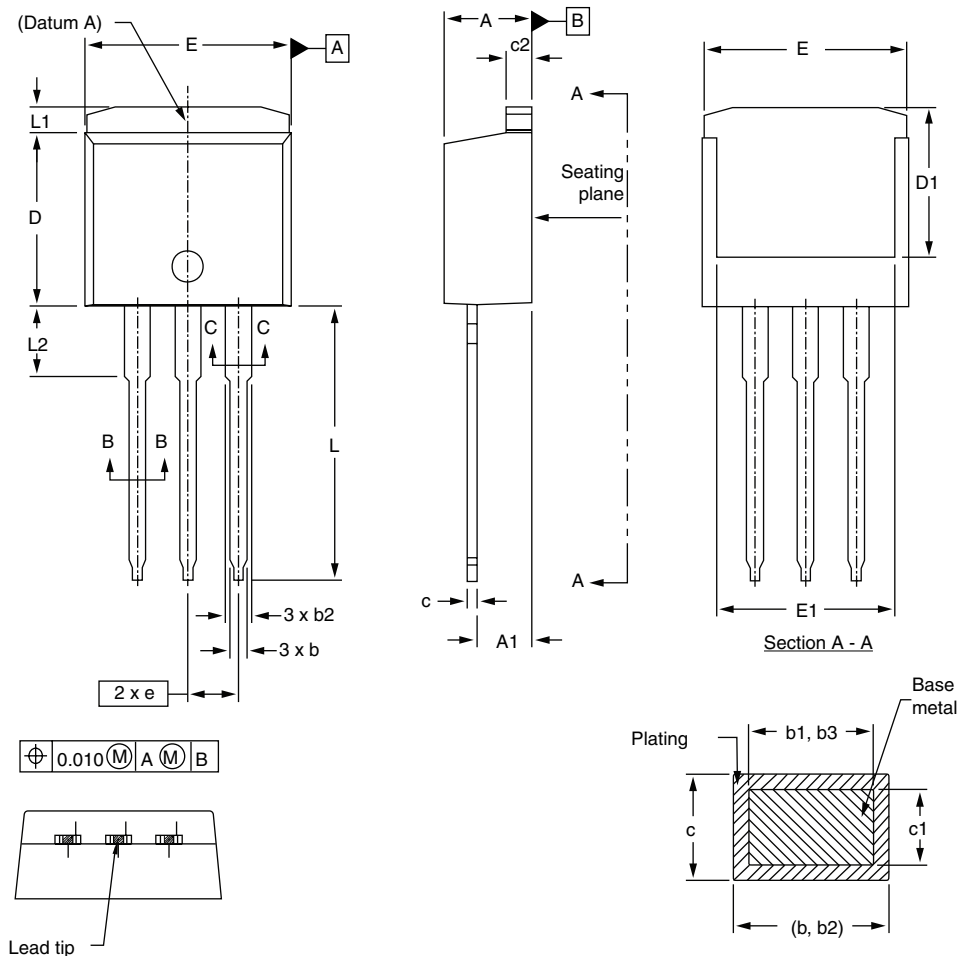
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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