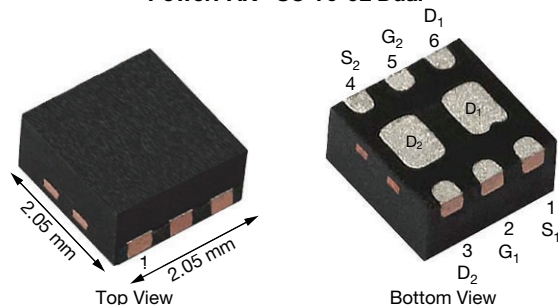


N-Channel 12 V (D-S) and P-Channel 20 V (D-S) MOSFET

PowerPAK® SC-70-6L Dual



Marking code: EK

PRODUCT SUMMARY

	N-CHANNEL	P-CHANNEL
V_{DS} (V)	12	-20
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.028	0.054
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 2.5$ V	0.033	0.070
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 1.8$ V	0.042	0.104
$R_{DS(on)}$ (Ω) at $V_{GS} = -1.5$ V	-	0.165
Q_g typ. (nC)	6.2	9.5
I_D (A) ^a	4.5	-4.5
Configuration	N- and p-pair	

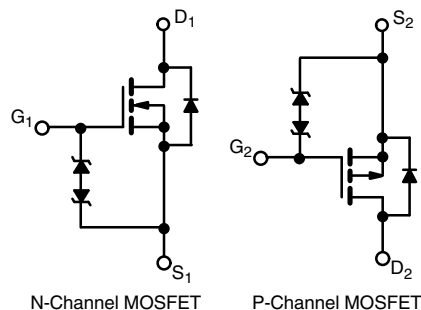
FEATURES

- TrenchFET® power MOSFETs
- Typical ESD protection:
N-channel 2400 V, P-channel 2000 V
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs and mobile computing
 - Load switches
 - Power management
 - DC/DC converters



ORDERING INFORMATION

Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA537EDJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V _{DS}	12	-20	V
Gate-source voltage		V _{GS}	± 8	± 8	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	I _D	4.5 ^a	-4.5 ^a	A
	T _C = 70 °C		4.5 ^a	-4.5 ^a	
	T _A = 25 °C		4.5 ^{a, b, c}	-4.5 ^{a, b, c}	
	T _A = 70 °C		4.5 ^{a, b, c}	-4.5 ^{a, b, c}	
Pulsed drain current (t = 100 μs)		I _{DM}	20	-15	
Source drain current diode current	T _C = 25 °C	I _S	4.5 ^a	-4.5 ^a	
	T _A = 25 °C		1.6 ^{b, c}	-1.6 ^{b, c}	
Maximum power dissipation	T _C = 25 °C	P _D	7.8	7.8	W
	T _C = 70 °C		5	5	
	T _A = 25 °C		1.9 ^{b, c}	1.9 ^{b, c}	
	T _A = 70 °C		1.2 ^{b, c}	1.2 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) ^{d, e}			260		

**THERMAL RESISTANCE RATINGS**

PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, f}	$t \leq 5 \text{ s}$	R_{thJA}	52	65	52	65	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	12.5	16	12.5	16	

Notes

- a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. $t = 5 \text{ s}$
d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 110 °C/W

SPECIFICATIONS ($T_J = 25 \text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	12	-	-	V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-20	-	-	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	-	8	-	mV/°C
		I _D = -250 μA	P-Ch	-	-15	-	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	-	-2.5	-	
		I _D = -250 μA	P-Ch	-	2.5	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.4	-	1	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.4	-	-1	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	N-Ch	-	-	± 0.5	μA
			P-Ch	-	-	± 3	
		V _{DS} = 0 V, V _{GS} = ± 8 V	N-Ch	-	-	± 5	
			P-Ch	-	-	± 30	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V	N-Ch	-	-	1	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch	-	-	-1	
		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	10	
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-10	
On-state drain current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	10	-	-	A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-10	-	-	
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.2 A	N-Ch	-	0.023	0.028	Ω
		V _{GS} = -4.5 V, I _D = -3.8 A	P-Ch	-	0.044	0.054	
		V _{GS} = 2.5 V, I _D = 4.8 A	N-Ch	-	0.027	0.033	
		V _{GS} = -2.5 V, I _D = -3.3 A	P-Ch	-	0.057	0.070	
		V _{GS} = 1.8 V, I _D = 2.5 A	N-Ch	-	0.035	0.042	
		V _{GS} = -1.8 V, I _D = -1 A	P-Ch	-	0.075	0.104	
		V _{GS} = -1.5 V, I _D = -0.5 A	P-Ch	-	0.097	0.165	
Forward transconductance ^b	g _{fs}	V _{DS} = 6 V, I _D = 5.2 A	N-Ch	-	23	-	S
		V _{DS} = -6 V, I _D = -3.6 A	P-Ch	-	11	-	



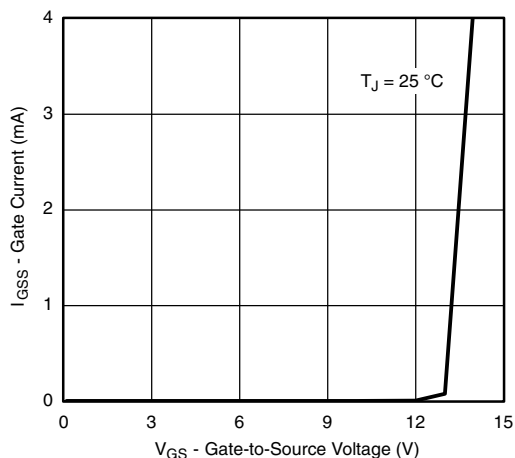
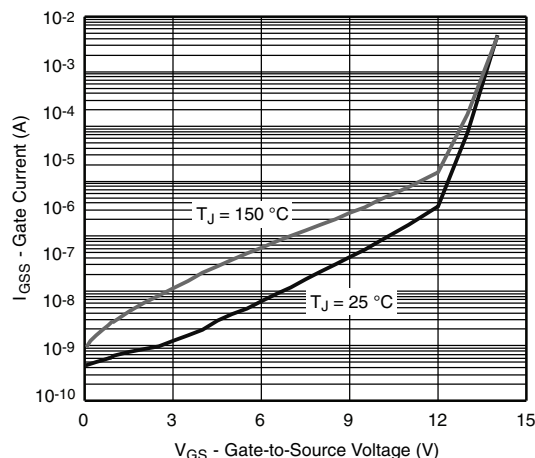
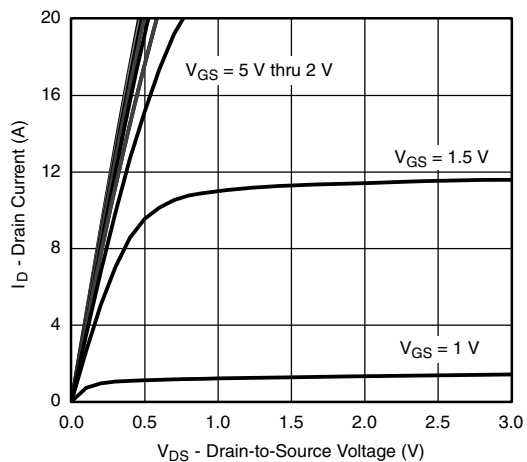
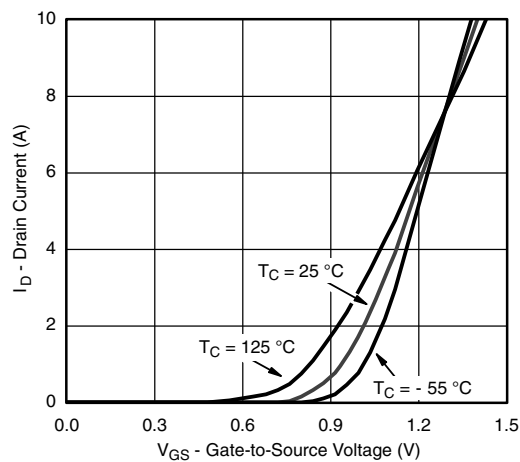
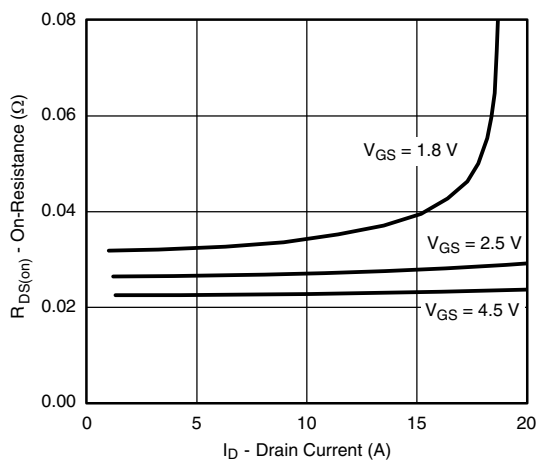
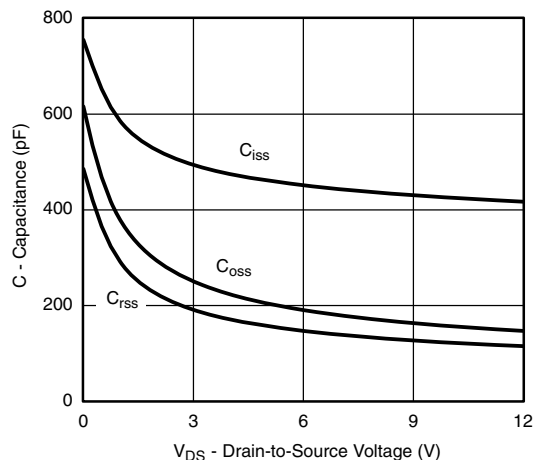
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)										
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT			
Dynamic ^a										
Input capacitance	C _{iss}	N-Channel V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	455	-	pF			
Output capacitance	C _{oss}		P-Ch	-	770	-				
Reverse transfer capacitance	C _{rss}	P-Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	190	-				
			P-Ch	-	90	-				
Total gate charge	Q _g	N-Channel V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 6.8 A	N-Ch	-	150	-	nC			
			P-Ch	-	81	-				
			Gate-source charge	Q _{gs}	V _{DS} = 6 V, V _{GS} = 8 V, I _D = 6.8 A	N-Ch		-	10.5	16
					V _{DS} = -10 V, V _{GS} = -8 V, I _D = -4.9 A	P-Ch		-	16.3	25
Gate-drain charge	Q _{gd}	P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -4.9 A	N-Ch	-	6.2	9.5				
			P-Ch	-	9.5	14.5				
Gate resistance	R _g	f = 1 MHz	N-Ch	-	0.8	-				
			P-Ch	-	1.4	-				
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 1.1 Ω I _D ≅ 5.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch	-	1.6	-	Ω			
Rise time	t _r		P-Ch	-	2.3	-				
Turn-off delay time	t _{d(off)}		P-Channel V _{DD} = -10 V, R _L = 2.6 Ω I _D ≅ -3.9 A, V _{GEN} = -4.5 V, R _g = 1 Ω	N-Ch	-	6.2		9.5		
Fall time	t _f			P-Ch	-	9.5		14.5		
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 1.3 Ω I _D ≅ 5.4 A, V _{GEN} = 8 V, R _g = 1 Ω	N-Ch	-	1.6	-	ns			
			P-Ch	-	2.3	-				
			Rise time	t _r	N-Ch	-		6.2	9.5	
					P-Ch	-		9.5	14.5	
Turn-off delay time	t _{d(off)}	P-Channel V _{DD} = -10 V, R _L = 2.6 Ω I _D ≅ -3.9 A, V _{GEN} = -8 V, R _g = 1 Ω	N-Ch	-	0.8	-				
			P-Ch	-	1.4	-				
Fall time	t _f		N-Ch	-	1.6	-				
			P-Ch	-	2.3	-				
Drain-Source Body Diode Characteristics										
Continuous source-drain diode current	I _S	T _C = 25 °C	N-Ch	-	-	4.5	A			
Pulse diode forward current ^a	I _{SM}		P-Ch	-	-	-4.5				
Body diode voltage	V _{SD}	I _S = 4.8 A, V _{GS} = 0 V	N-Ch	-	-	20	V			
		I _S = -3.9 A, V _{GS} = 0 V	P-Ch	-	-	-15				
Body diode reverse recovery time	t _{rr}	N-Channel I _F = 5.4 A, di/dt = 100 A/μs, T _J = 25 °C	N-Ch	-	0.8	1.2	ns			
Body diode reverse recovery charge	Q _{rr}		P-Ch	-	-0.9	-1.2				
			N-Ch	-	25	50	nC			
Reverse recovery fall time	t _a		P-Channel I _F = -3.9 A, di/dt = -100 A/μs, T _J = 25 °C	N-Ch	-	13		25		
Reverse recovery rise time	t _b		N-Ch	-	10	20	ns			
			P-Ch	-	5.5	12				
			N-Ch	-	13	-				
			P-Ch	-	7.5	-				
			N-Ch	-	12	-				
			P-Ch	-	5.5	-				

Notes

a. Guaranteed by design, not subject to production testing

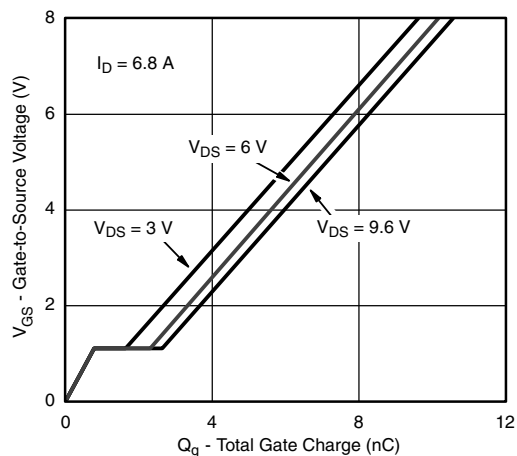
b. Pulse test; pulse width $\leq 300\text{ } \mu\text{s}$, duty cycle $\leq 2\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

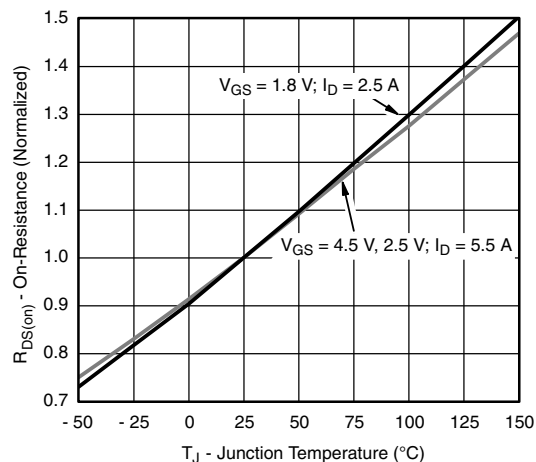
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance



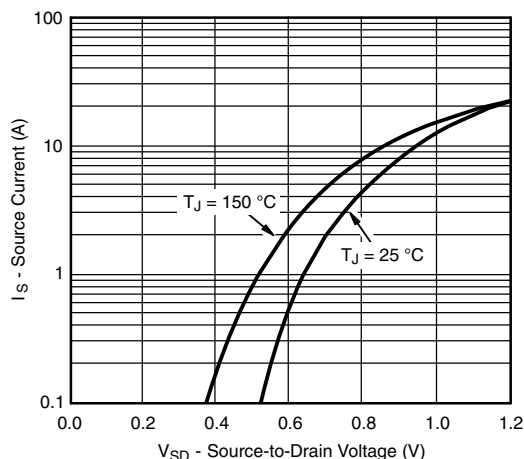
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



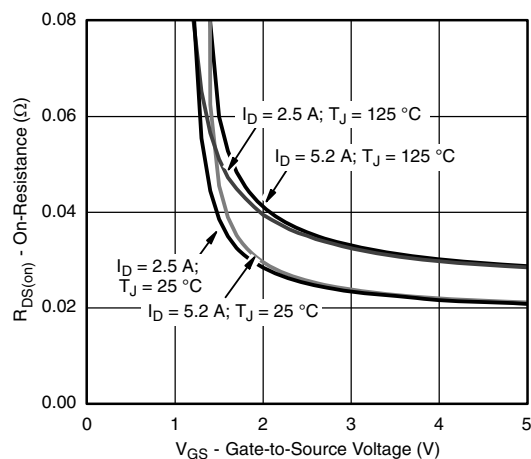
Gate Charge



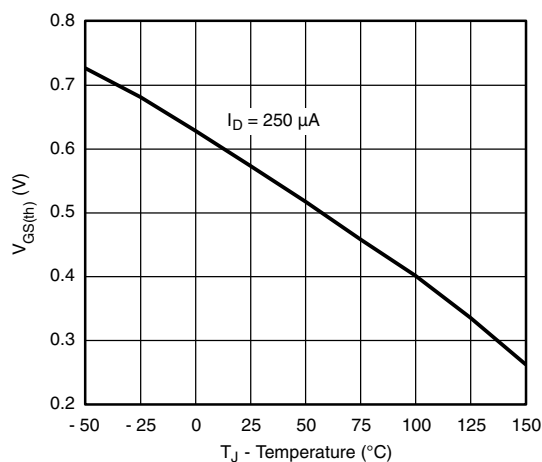
On-Resistance vs. Junction Temperature



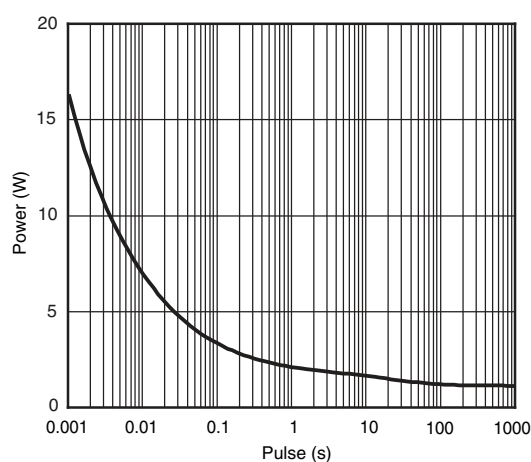
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



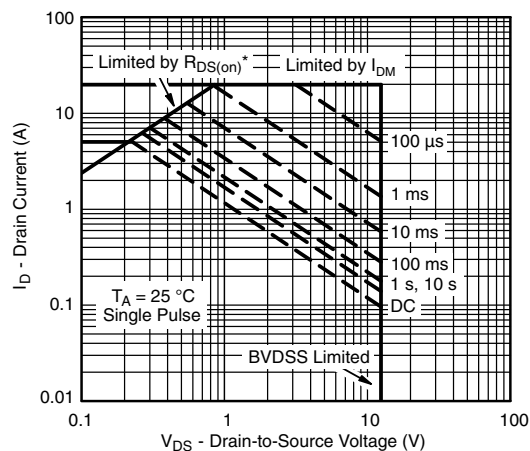
Threshold Voltage



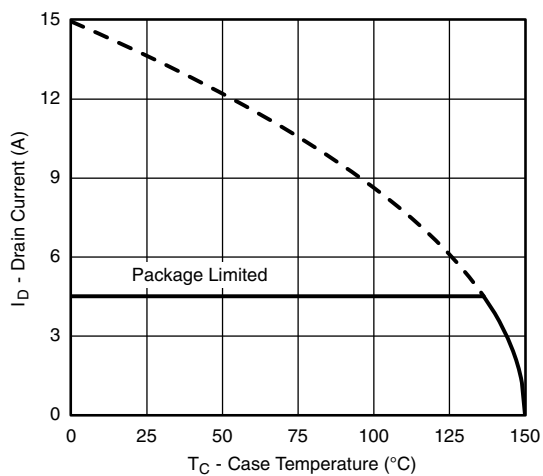
Single Pulse Power (Junction-to-Ambient)



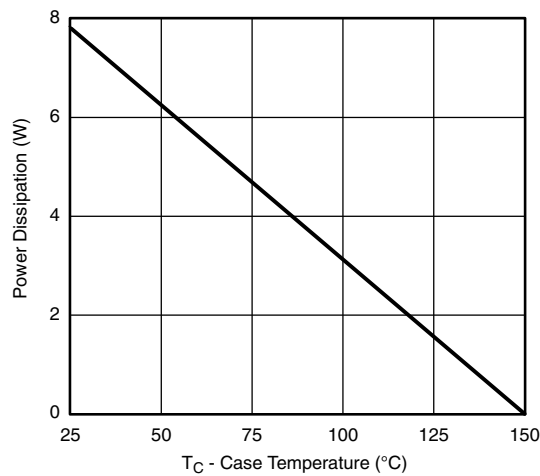
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



Current Derating^a



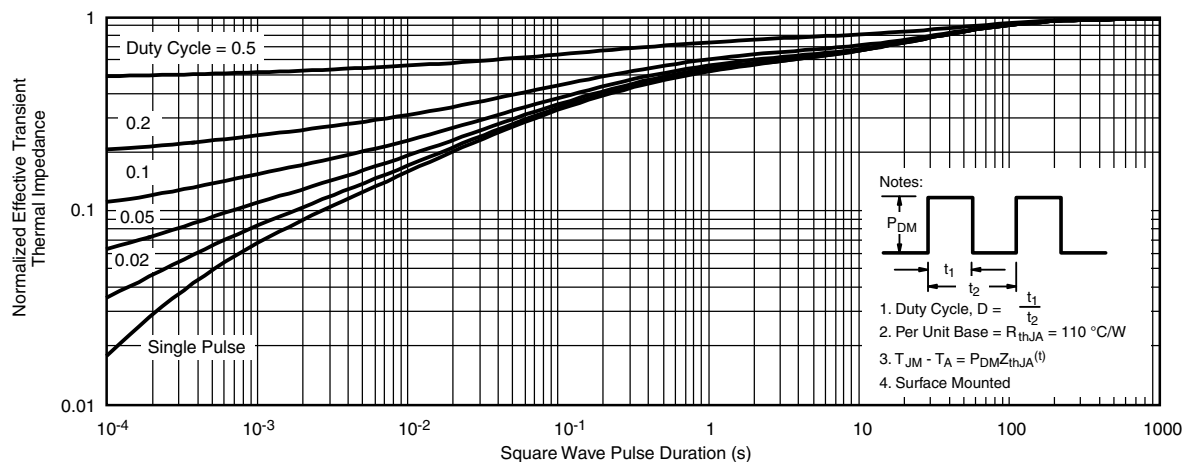
Power Derating

Note

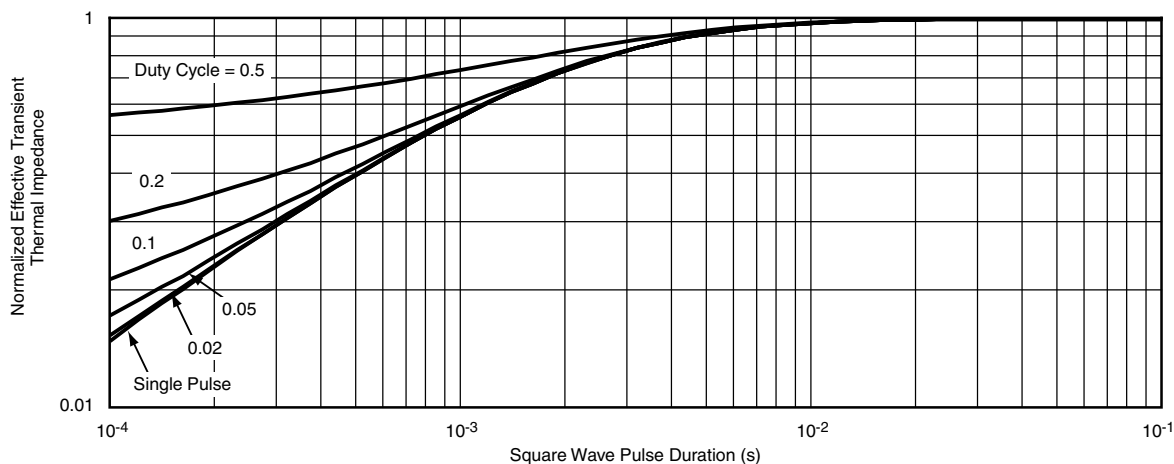
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



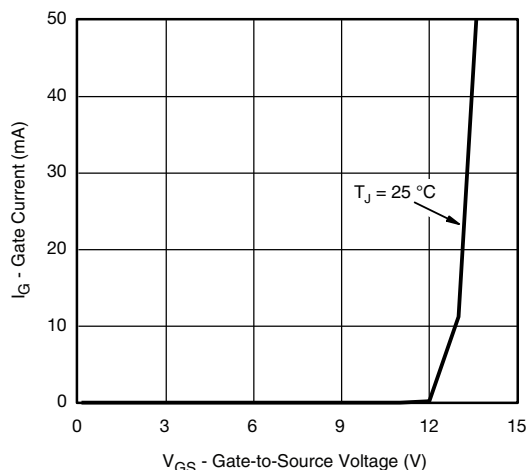
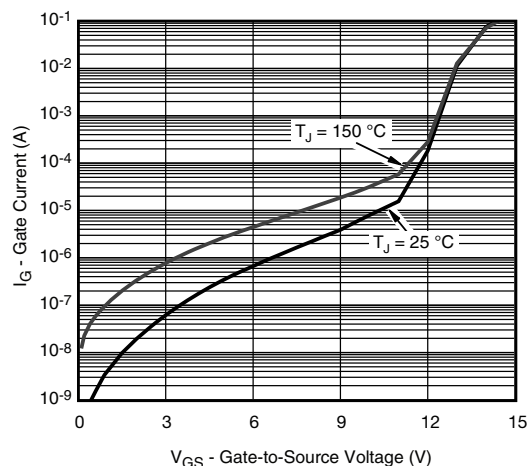
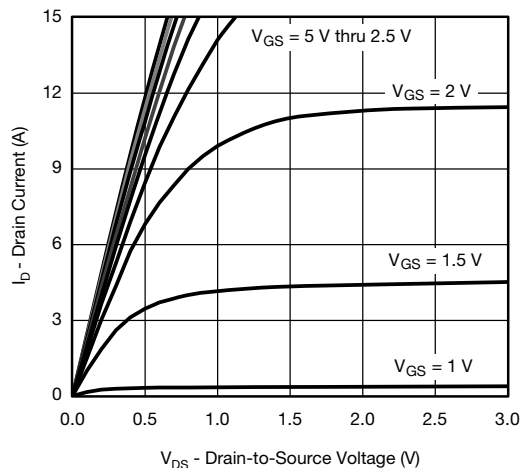
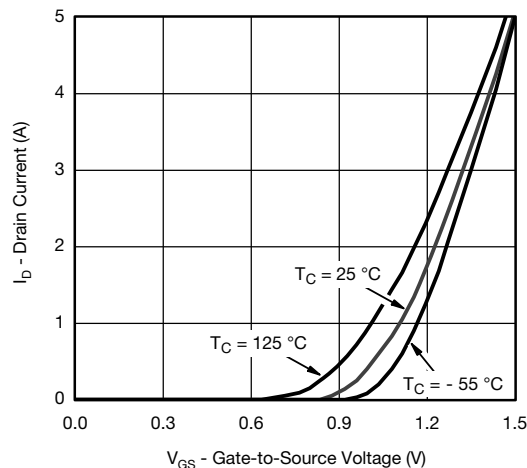
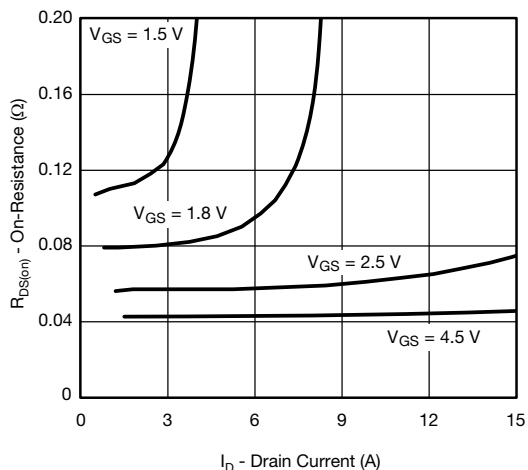
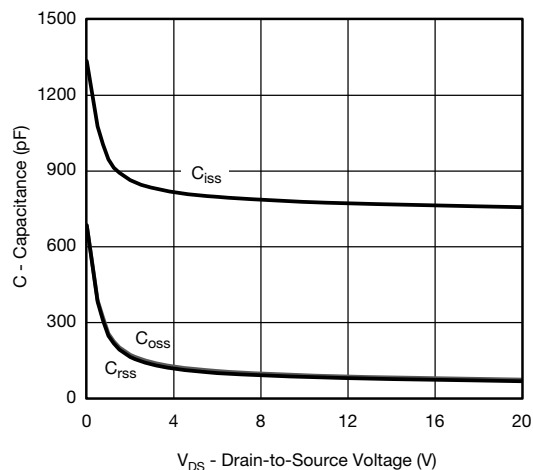
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

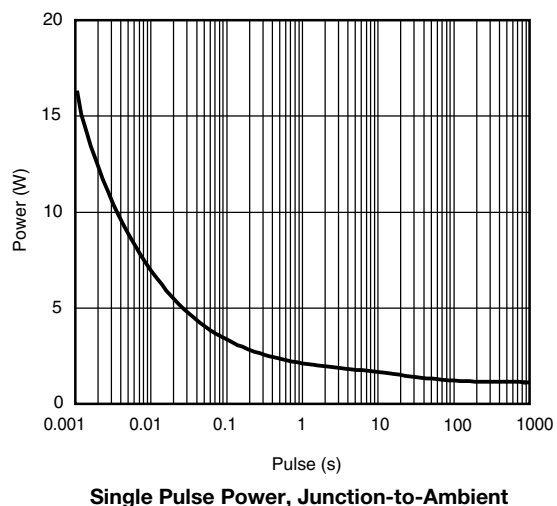
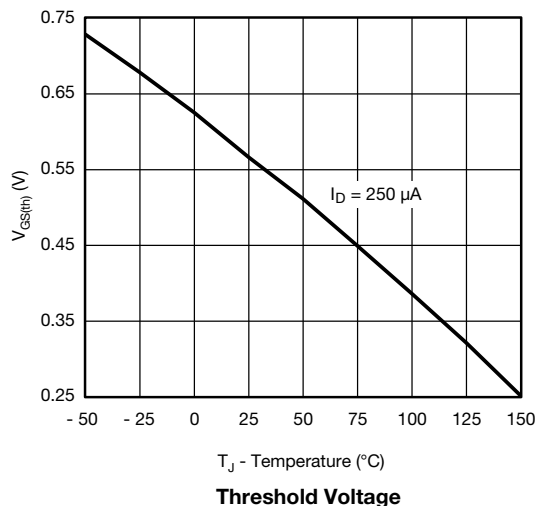
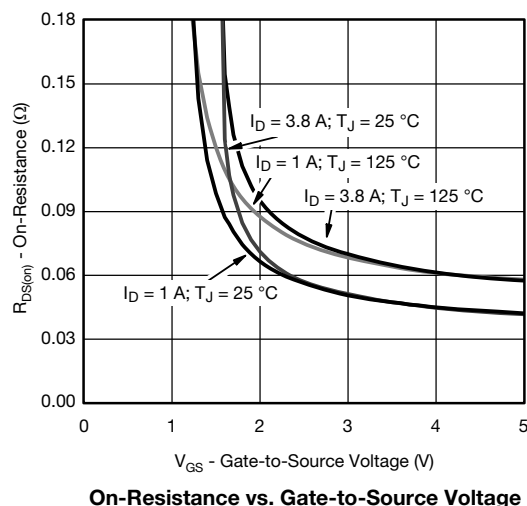
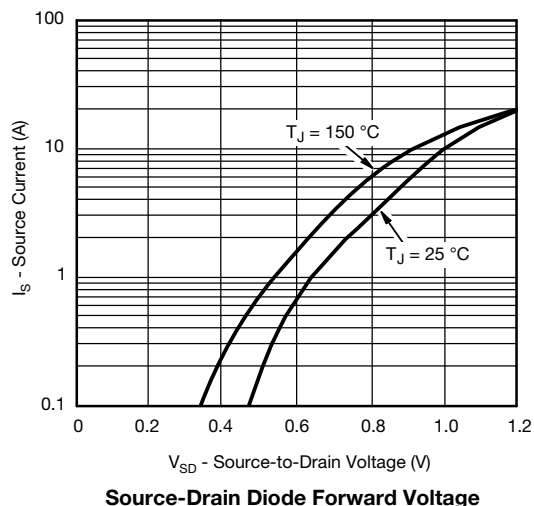
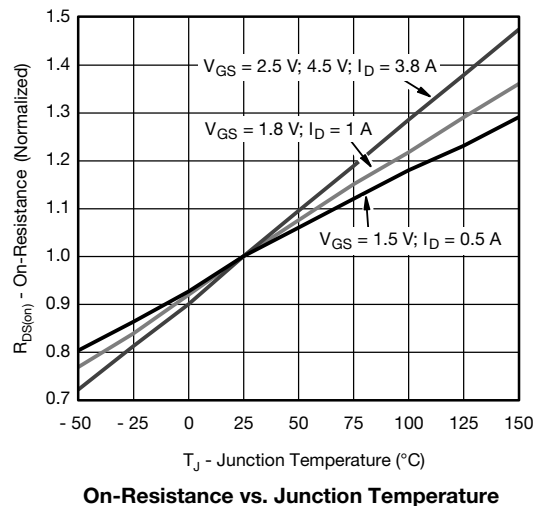
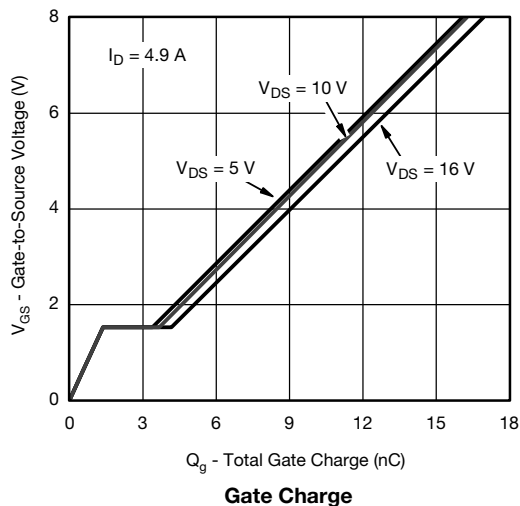


Normalized Thermal Transient Impedance, Junction-to-Case

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-to-Source Voltage

Gate Current vs. Gate-to-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

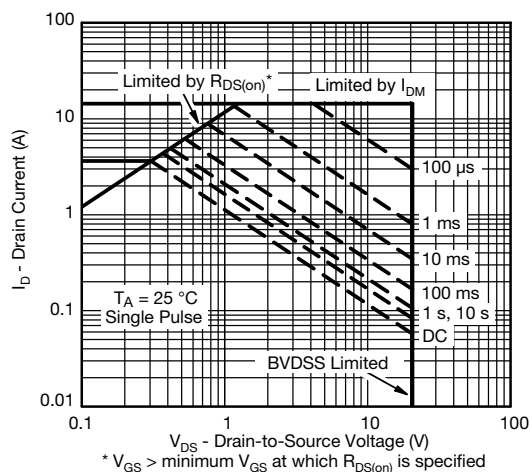


P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

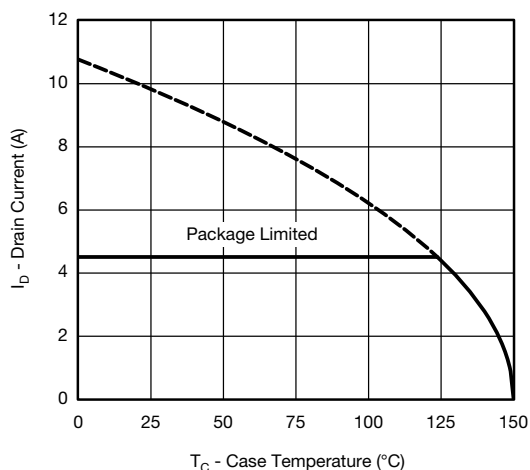




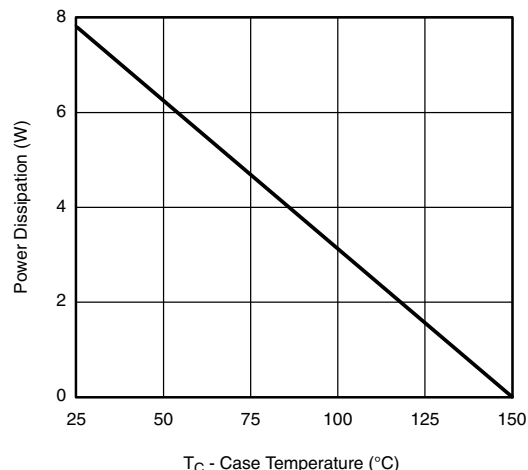
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating ^a



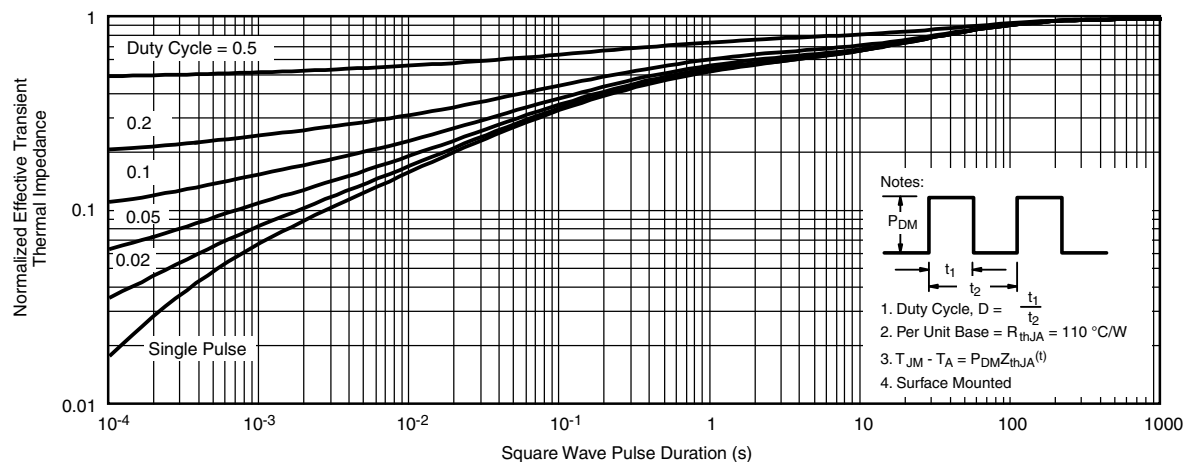
Power Derating

Note

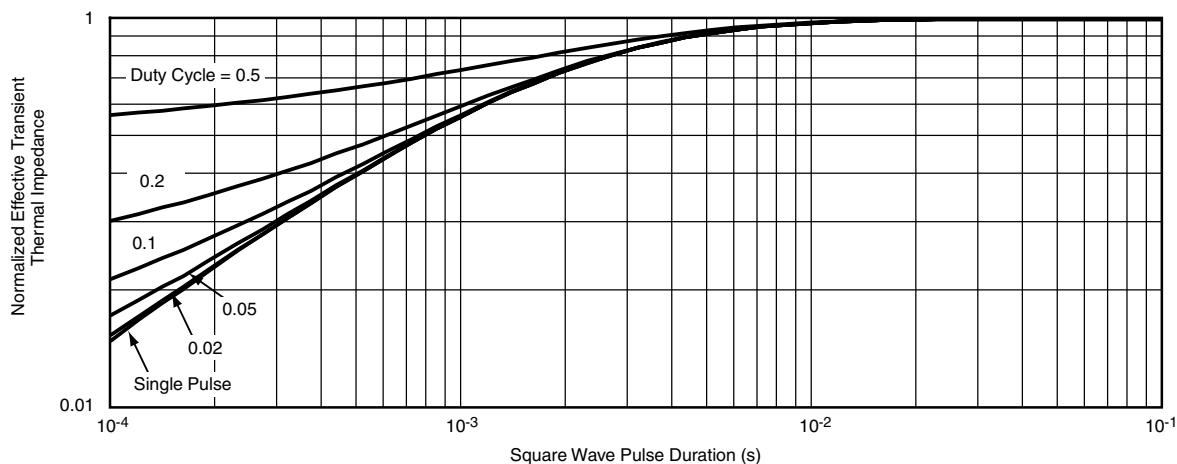
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

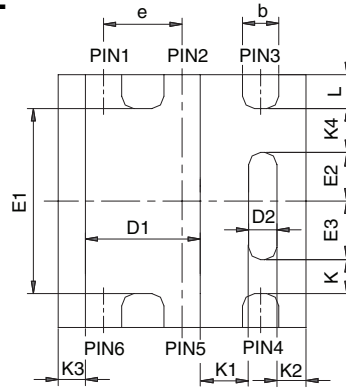


Normalized Thermal Transient Impedance, Junction-to-Case

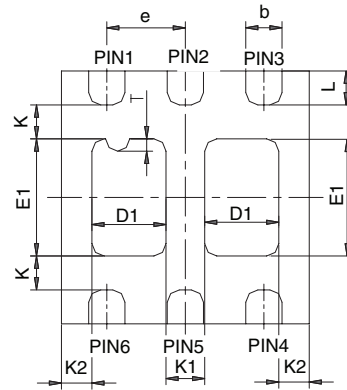
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62934.



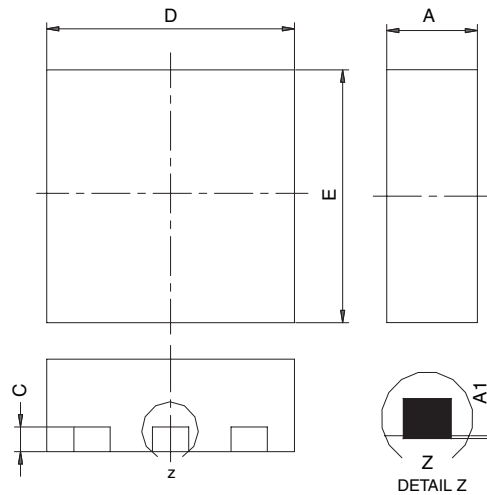
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

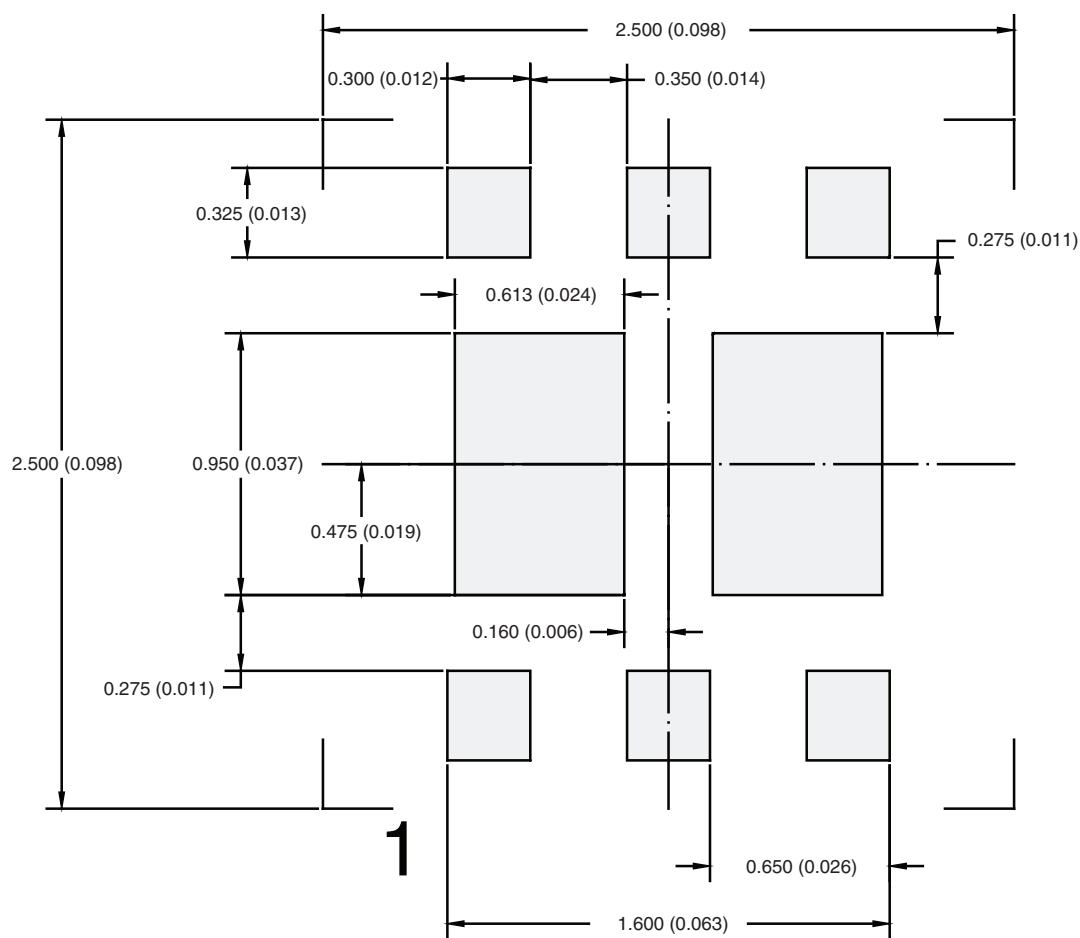


Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07 DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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