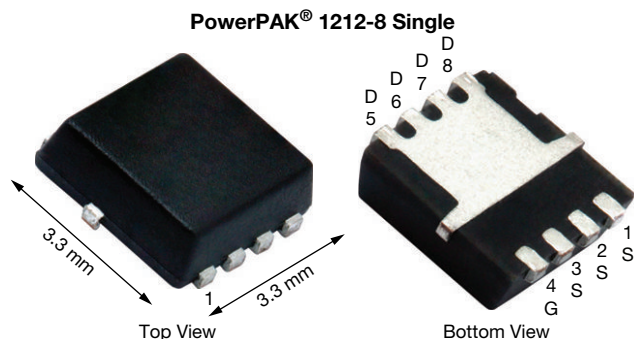


# N-Channel 30 V (D-S) MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



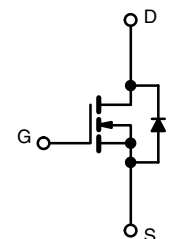
PRODUCT SUMMARY	
$V_{DS}$ (V)	30
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0088
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0120
$Q_g$ typ. (nC)	9.9
$I_D$ (A)	16 <sup>a, g</sup>
Configuration	Single

## FEATURES

- TrenchFET® Gen IV power MOSFET
- Tuned for reducing transient spikes
- 100 %  $R_g$  and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- Synchronous buck converter
- High power density DC/DC
- Motor drive control
- Battery management
- Load switch



N-Channel MOSFET

## ORDERING INFORMATION

Package	PowerPAK 1212-Single
Lead (Pb)-free and halogen-free	SiSA96DN-T1-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GS}$	+20 / -16	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	16 <sup>a</sup>	A
		12 <sup>a</sup>	
		14.8 <sup>b, c</sup>	
		12 <sup>b, c</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	65	
Continuous source-drain diode current	$I_S$	16 <sup>a</sup>	
		3.2 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	15	
Single pulse avalanche energy	$E_{AS}$	11.25	mJ
Maximum power dissipation	$P_D$	26.5	W
		17	
		3.5 <sup>c</sup>	
		2.3 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$R_{thJA}$	28	35	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	3.8	4.7	

### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- $T_C = 25$  °C.

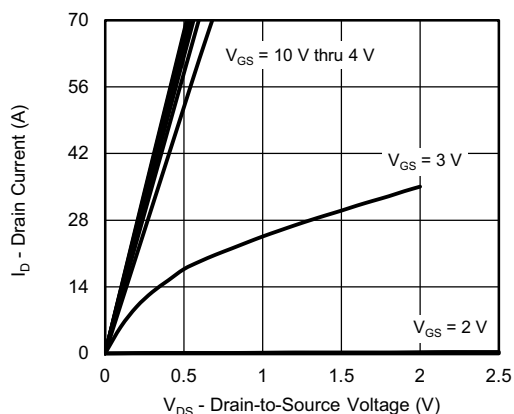
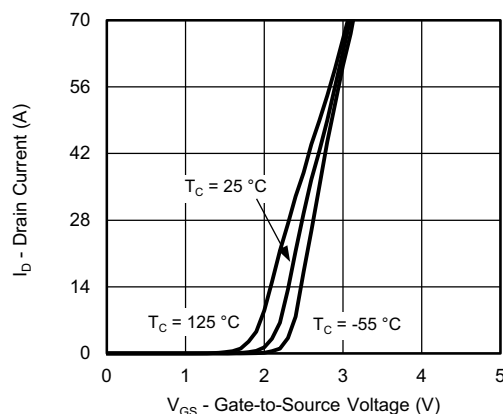
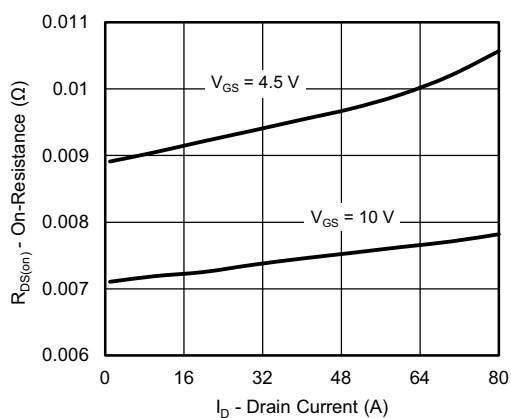
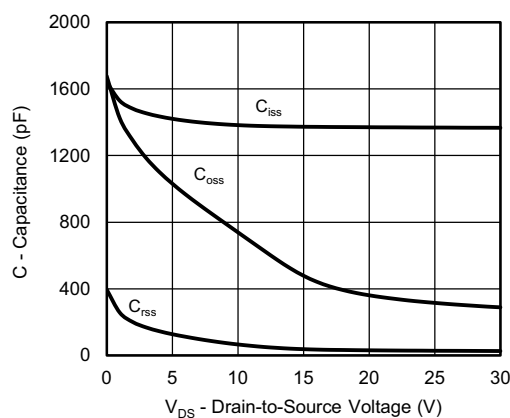
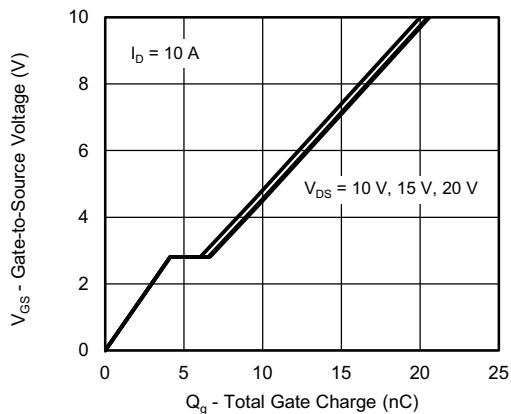
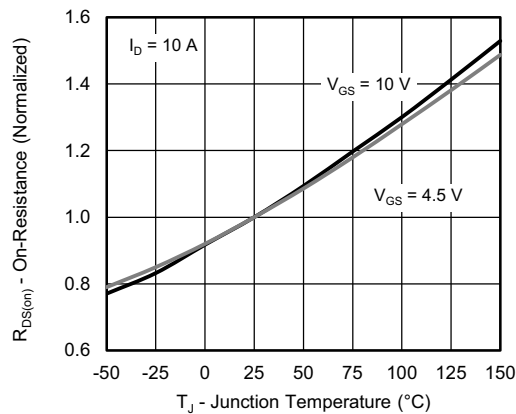


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-	V
Drain-source breakdown voltage (transient) <sup>c</sup>	V <sub>DS(t)</sub>	V <sub>GS</sub> = 0 V, I <sub>D(aval)</sub> = 15 A, t <sub>transient</sub> = 50 ns	36	-	-	
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> =10 mA	-	13	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-4.7	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 μA	1	-	2.2	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20 / -16 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.0073	0.0088	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	0.0092	0.0120	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	-	70	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	1385	-	pF
Output capacitance	C <sub>oss</sub>		-	478	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	37	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	20.5	31	nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A	-	9.9	15	
Gate-source charge	Q <sub>gs</sub>		-	4.2	-	
Gate-drain charge	Q <sub>gd</sub>		-	2.5	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.2	0.73	1.4	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	8	16	ns
Rise time	t <sub>r</sub>		-	25	50	
Turn-off delay time	t <sub>d(off)</sub>		-	13	26	
Fall time	t <sub>f</sub>		-	9	18	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	12	24	
Rise time	t <sub>r</sub>		-	47	94	
Turn-off delay time	t <sub>d(off)</sub>		-	15	30	
Fall time	t <sub>f</sub>		-	25	50	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	16	A
Pulse diode forward current	I <sub>SM</sub>		-	-	50	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.77	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	50	100	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	75	150	nC
Reverse recovery fall time	t <sub>a</sub>		-	43	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	7	-	

**Notes**

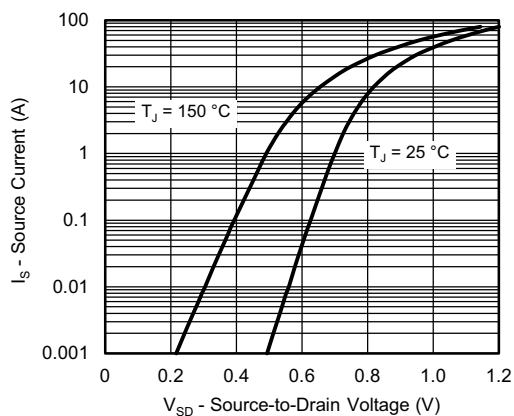
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c.  $T_{CASE} = 25\text{ }^{\circ}\text{C}$ . Expected voltage stress during 100 % UIS test. Production datalog is not available.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

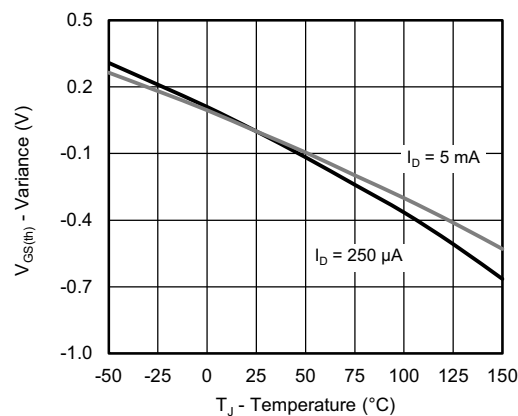
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**



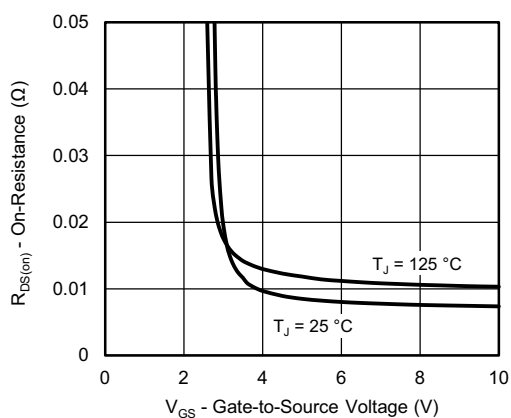
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



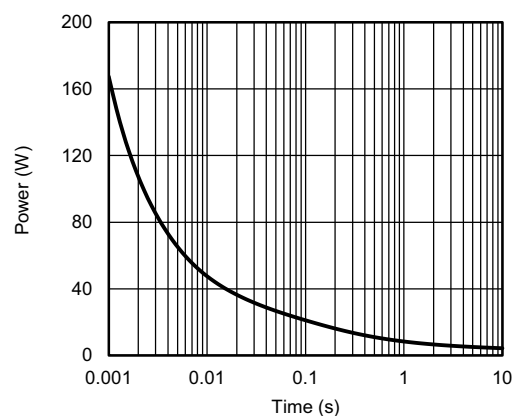
**Source-Drain Diode Forward Voltage**



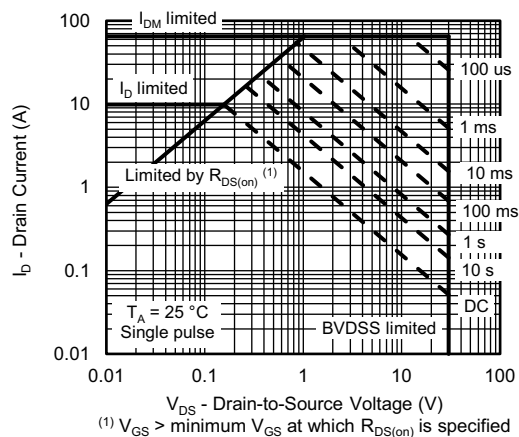
**Threshold Voltage**



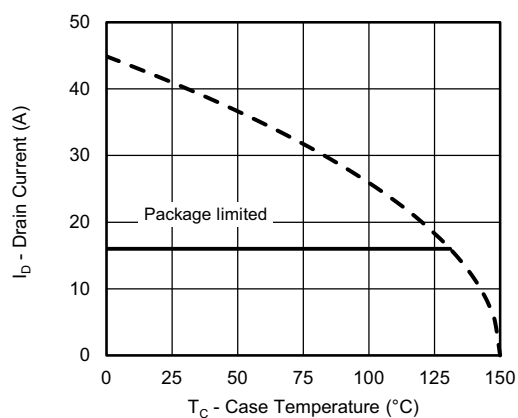
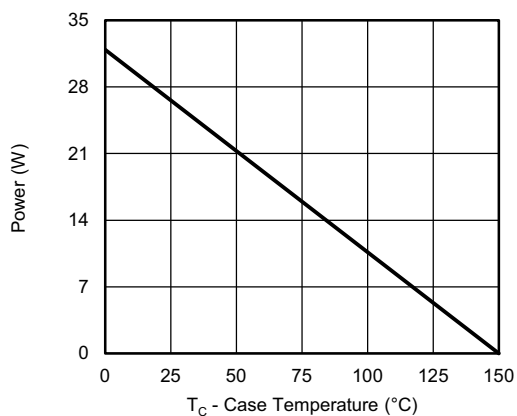
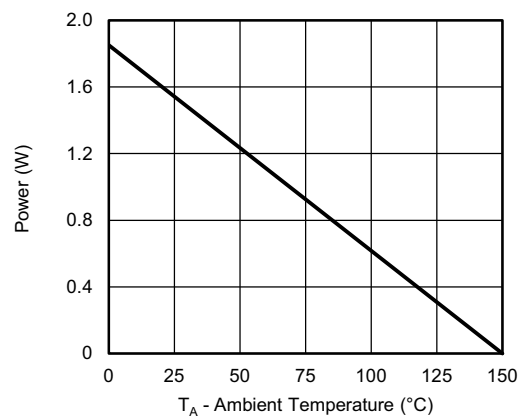
**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



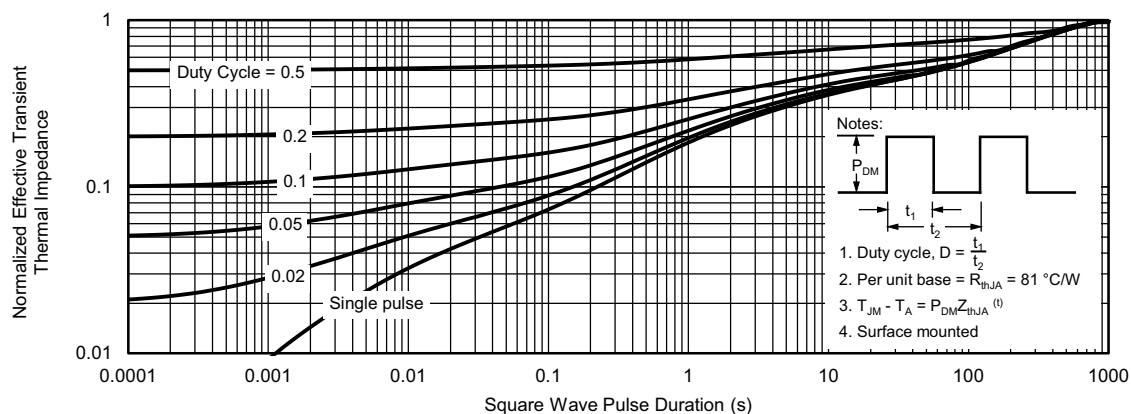
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating <sup>a</sup>**

**Power, Junction-to-Case**

**Power, Junction-to-Ambient**
**Note**

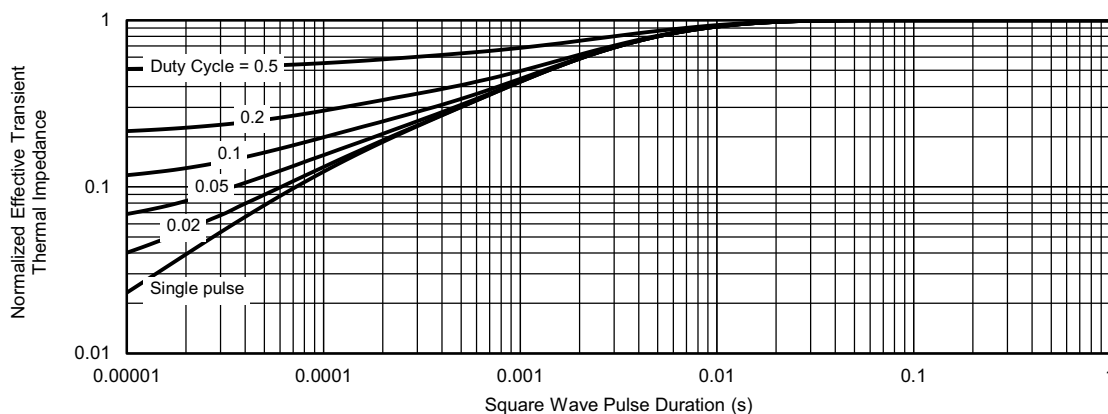
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

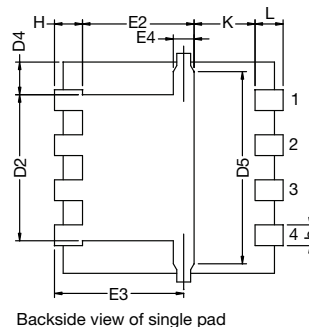


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75285](http://www.vishay.com/ppg?75285).



## PowerPAK® 1212-8, (Single / Dual)



Backside view of single pad



Backside view of dual pad

**Notes**

1. Inch will govern

[2] Dimensions exclusive of mold gate burrs

3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S16-2667-Rev. M, 09-Jan-17						
DWG: 5882						

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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