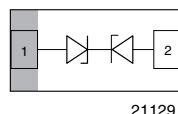




Ultra Low Capacitance Bidirectional Symmetrical (BiSy) Single Line ESD Protection Diode in DFN1006-2B



MARKING (example only)



Bar = cathode marking

X = date code

YY = type code (see table below)

LINKS TO ADDITIONAL RESOURCES



3D Models



Models

FEATURES

- Ultra compact DFN1006-2B package
- Low package height < 0.5 mm
- 1-line ESD protection
- AEC-Q101 qualified available
- Working range ± 3.3 V
- Low leakage current < 0.01 μ A
- Ultra low load capacitance $C_D = 0.36$ pF typ.
- ESD immunity acc. IEC 61000-4-2
 - ± 16 kV contact discharge
 - ± 16 kV air discharge
- e3 - Sn
 - Tin plated exposed side wall of lead frame
 - Soldering can be checked by standard vision inspection
 - AOI = Automated Optical Inspection
 - No X-ray necessary
- Lead material: Cu
- PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ORDERING INFORMATION

PART NUMBER (EXAMPLE)	ENVIRONMENTAL AND QUALITY CODE			PACKAGING CODE	ORDERING CODE (EXAMPLE)
	AEC-Q101 QUALIFIED	RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS	TIN PLATED	10K PER 7" REEL (8 mm TAPE)	
		GREEN		10K = MOQ	
VBUS03N1-DD1	-	G	3	-08	VBUS03N1-DD1-G3-08
VBUS03N1-DD1	H	G	3	-08	VBUS03N1-DD1HG3-08

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	SOLDERING CONDITIONS
VBUS03N1-DD1	DFN1006-2B	3B	0.83 mg	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5, 8/20 μ s/single shot	I_{PPM}	4	A
Peak pulse power	Pin 1 to pin 2 Acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	P_{PP}	90	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 16	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 16	
Operating temperature	Junction temperature	T_J	-55 to +150	°C
Storage temperature		T_{stg}	-55 to +150	°C

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

ESD PROTECTION FOR HIGH-SPEED SIGNAL OR DATA LINES

The VBUS03N1-DD1 is a Bidirectional and Symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS03N1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny DFN1006 package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots. Due to the very low capacitance the VBUS03N1-DD1 can be used for high speed data ports like HDMI, USB 3.0 or Thunderbolt.

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	3.3	V
Reverse voltage	at $I_R = 0.1\ \mu\text{A}$	V_R	3.3	-	-	V
Reverse current	at $V_{RWM} = 3.3\ \text{V}$	I_R	-	-	0.1	μA
Reverse breakdown voltage	at $I_R = 1\ \text{mA}$	V_{BR}	7	8.5	10	V
Reverse clamping voltage	at $I_{PP} = 1\ \text{A}$	V_C	-	11.5	13	V
	at $I_{PP} = I_{PPM} = 4\ \text{A}$	V_C	-	18	21	V
Capacitance	at $V_R = 0\ \text{V}$; $f = 1\ \text{MHz}$	C_D	-	0.36	0.4	pF
	at $V_R = 3.3\ \text{V}$; $f = 1\ \text{MHz}$	C_D	-	0.36	-	pF
Clamping voltage	Transmission Line Pulse (TLP); $t_p = 100\ \text{ns}$ $I_{TLP} = 8\ \text{A}$	V_{C-TLP}	-	22	-	V
	Transmission Line Pulse (TLP); $t_p = 100\ \text{ns}$ $I_{TLP} = 16\ \text{A}$		-	33	-	
Dynamic resistance	Transmission Line Pulse (TLP); $t_p = 100\ \text{ns}$	R_{DYN}	-	1.4	-	Ω

TYPICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)

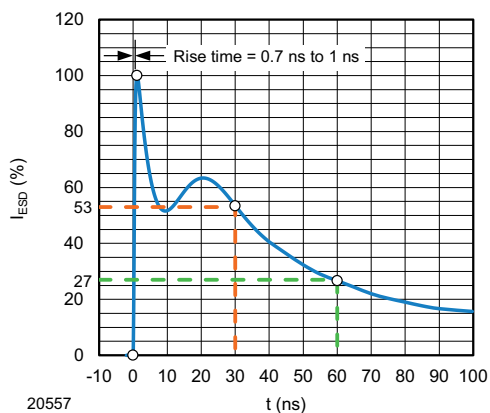


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

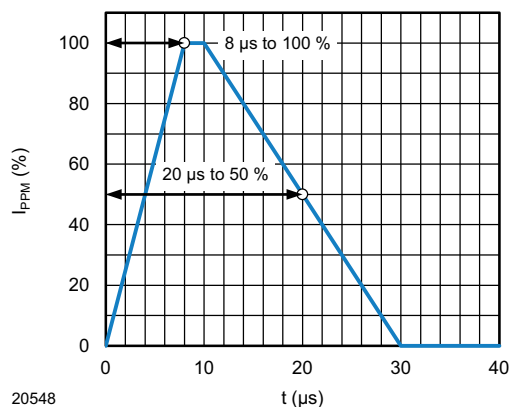


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form
acc. IEC 61000-4-5

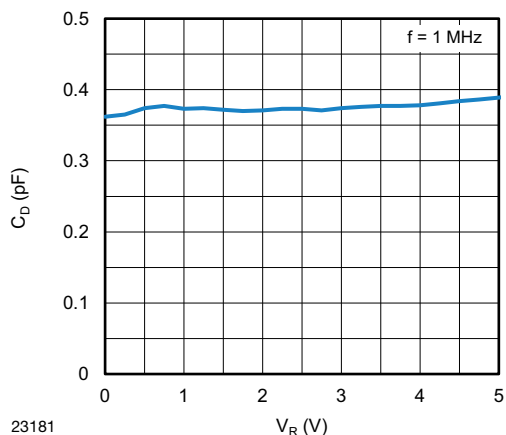


Fig. 3 - Typical Capacitance vs. Reverse Voltage

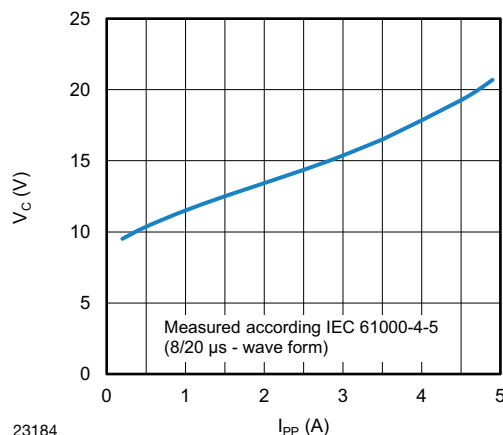


Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current

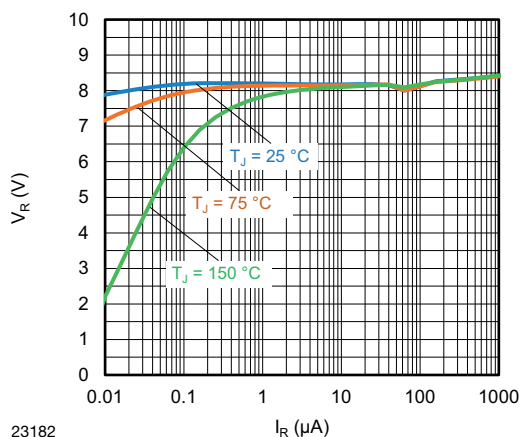


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

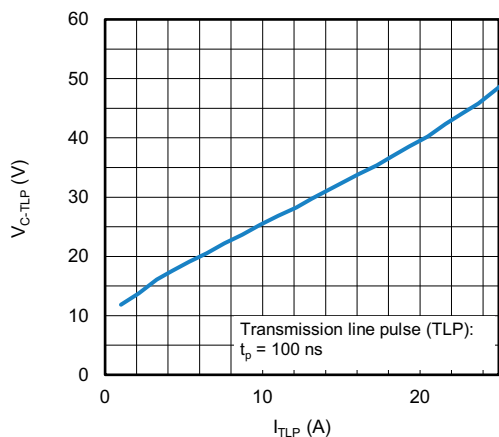
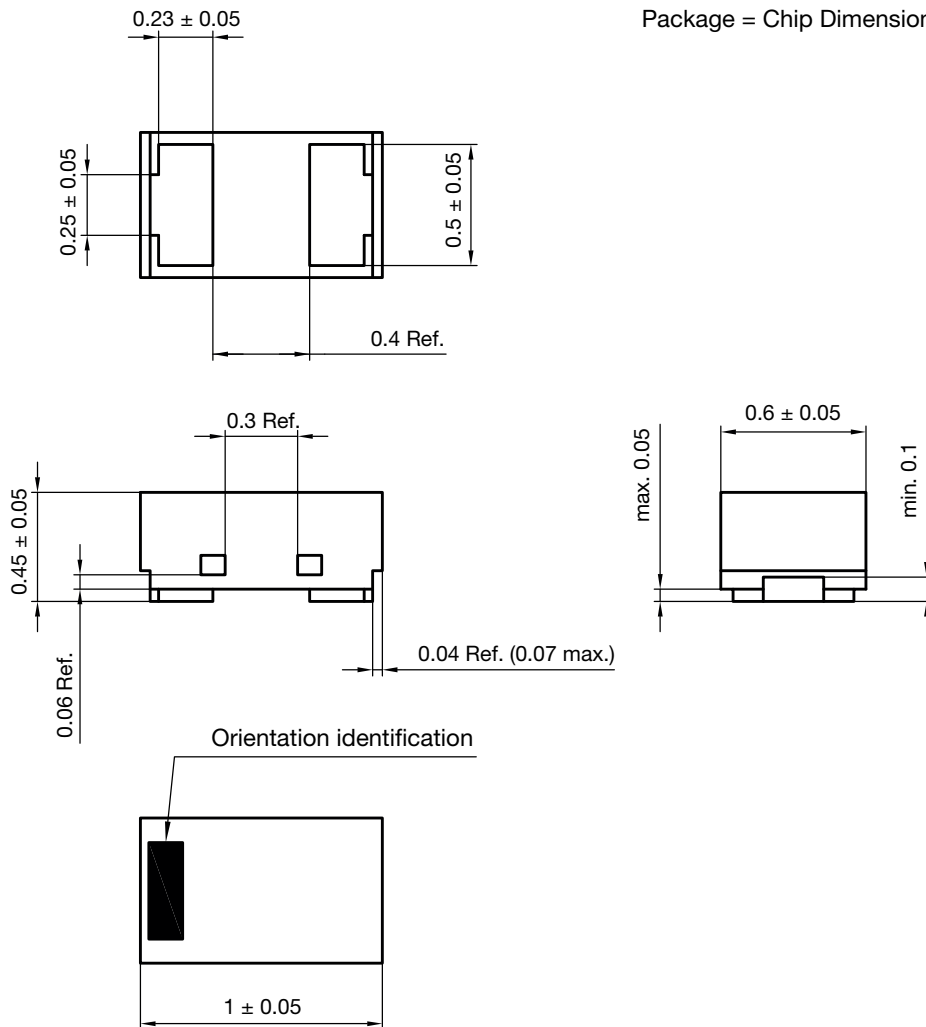
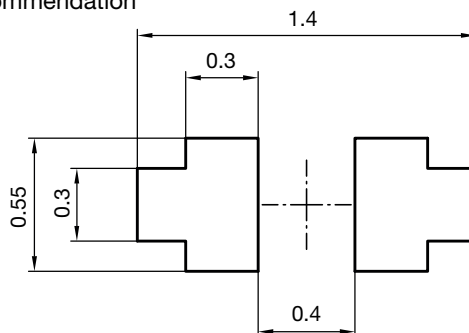


Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current

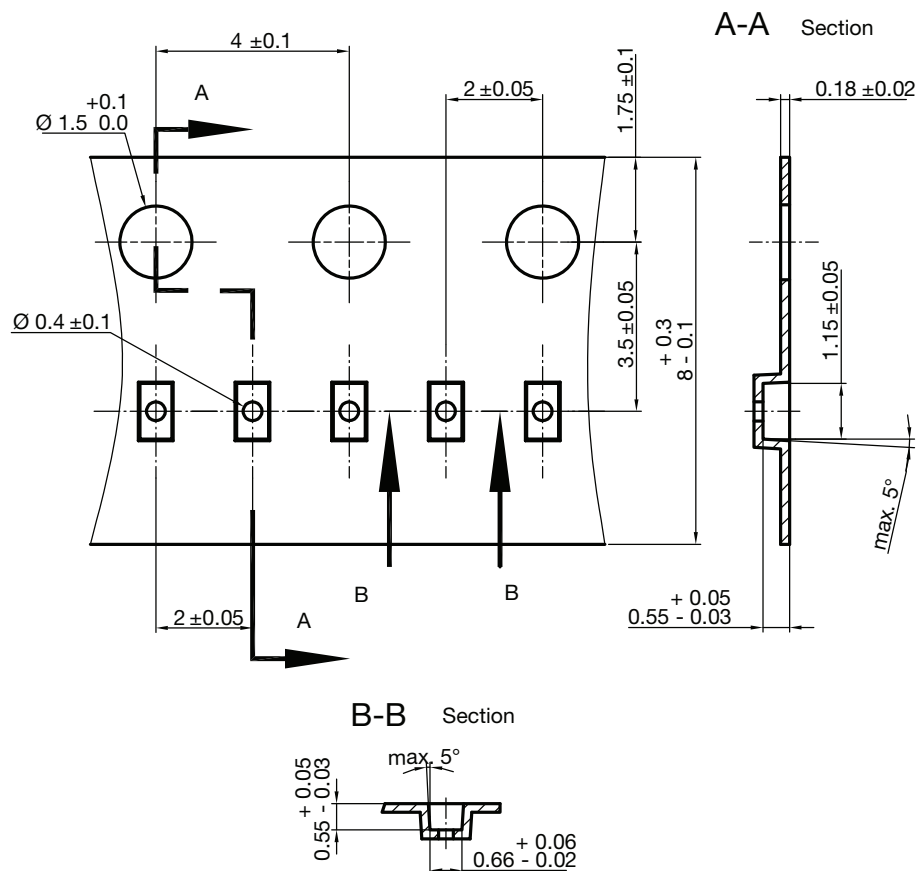
PACKAGE DIMENSIONS in millimeters (inches): **DFN1006-2B**

Package = Chip Dimension in mm


Footprint recommendation


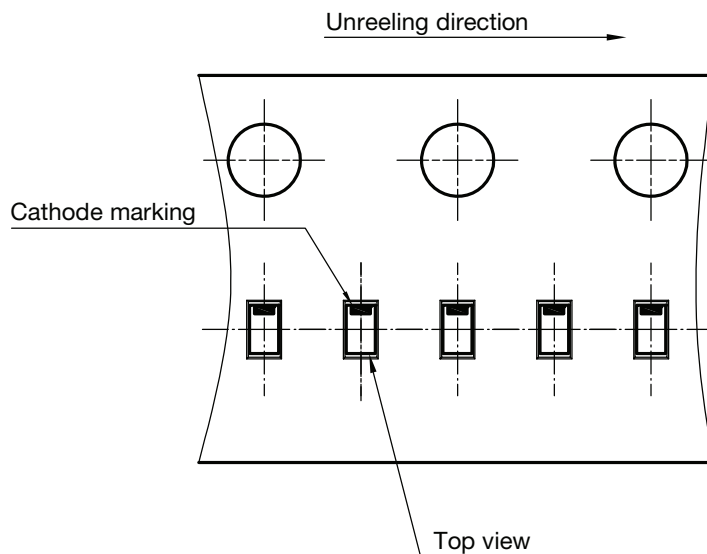
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Created - Date: 11-Jul-2018
Rev.5 - Date: 17-Sep-2021

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CARRIER TAPE DFN1006-2B


S8-V-3906.04-063 (4)
created 28.10.2019

surface resistance: $10^5 - 10^{11} \frac{\text{OHMS}}{\text{SQ}}$
Cumulative tolerances of 10 sprocket holes is $\pm 0.2 \text{ mm}$

ORIENTATION IN CARRIER TAPE DFN1006-2B


S8-V-3906.04-064 (4)
created 28.10.2019



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