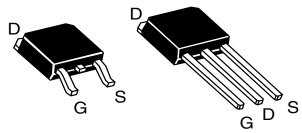
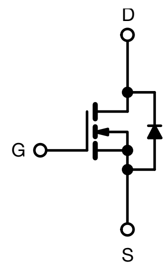
IRFR210, IRFU210, SiHFR210, SiHFU210

Power MOSFET

DPAK (TO-252) IPAK (TO-251)





N-Channel MOSFET

PRODUCT SUMMARY

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.5
Q_g max. (nC)	8.2	
Q_{gs} (nC)	1.8	
Q_{gd} (nC)	4.5	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Surface-mount (IRFR210, SiHFR210)
- Straight lead (IRFU210, SiHFU210)
- Available in tape and reel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

PACKAGE	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR210-GE3	SiHFR210TRL-GE3 [a]	-	SiHFR210TRR-GE3 [a]	SiHFU210-GE3
Lead (Pb)-free	IRFR210PbF	IRFR210TRLPbF [a]	IRFR210TRPbF [a]	IRFR210TRRPbF	IRFU210PbF
Lead (Pb)-free and halogen-free	IRFR210PbF-BE3 [ab]	IRFR210TRLPbF-BE3 [ab]	IRFR210TRPbF-BE3 [ab]	-	-

Notes

a. See device orientation

b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	200	V
Gate-source voltage			V_{GS}	± 20	V
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	2.6	A
		T_C = 100 °C		1.7	
Pulsed drain current [a]			I_{DM}	10	
Linear derating factor				0.20	W/°C
Linear derating factor (PCB mount) [e]				0.020	
Single pulse avalanche Energy [b]			E_{AS}	95	mJ
Avalanche current [a]			I_{AR}	2.7	A
Repetitive avalanche energy [a]			E_{AR}	2.5	mJ
Maximum power dissipation	T_C = 25 °C		P_D	25	W
Maximum power dissipation (PCB mount) [e]	T_A = 25 °C			2.5	
Peak diode recovery dV/dt [c]			dV/dt	5.0	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature)[d]	for 10 s			260	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28 mH, R_g = 25 Ω, I_{AS} = 2.6 A (see fig. 12)

c. $I_{SD} \leq 2.6$ A, dI/dt ≤ 70 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C

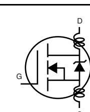
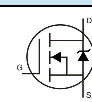
d. 1.6 mm from case

e. When mounted on 1" square PCB (FR-4 or G-10 material)

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	-	110	°C/W
Maximum junction-to-ambient (PCB mount) [a]	R_{thJA}	-	-	50	
Maximum junction-to-case (drain)	R_{thJC}	-	-	5.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.30	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 1.6 A [b]	-	-	1.5	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 1.6 A [b]	0.80	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	140	-	pF
Output capacitance	C_{oss}		-	53	-	
Reverse transfer capacitance	C_{rss}		-	15	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 3.3 A, V_{DS} = 160 V, see fig. 6 and 13 [b]	-	-	8.2	nC
Gate-source charge	Q_{gs}		-	-	1.8	
Gate-drain charge	Q_{gd}		-	-	4.5	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, I_D = 3.3 A, R_g = 24 Ω, R_D = 30 Ω, see fig. 10 [b]	-	8.2	-	ns
Rise time	t_r		-	17	-	
Turn-off delay time	$t_{d(off)}$		-	14	-	
Fall time	t_f		-	8.9	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-source body diode characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	2.6	A
Pulsed diode forward current [a]	I_{SM}		-	-	10	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 2.6 A, V_{GS} = 0 V [b]	-	-	2.0	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 3.3 A, dI/dt = 100 A/μs [b]	-	150	310	ns
Body diode reverse recovery charge	Q_{rr}		-	0.60	1.4	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

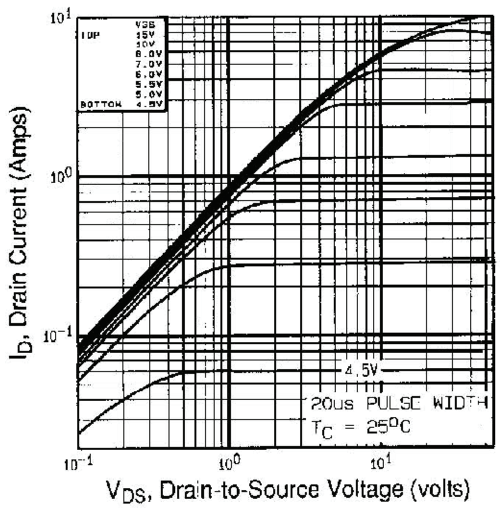


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

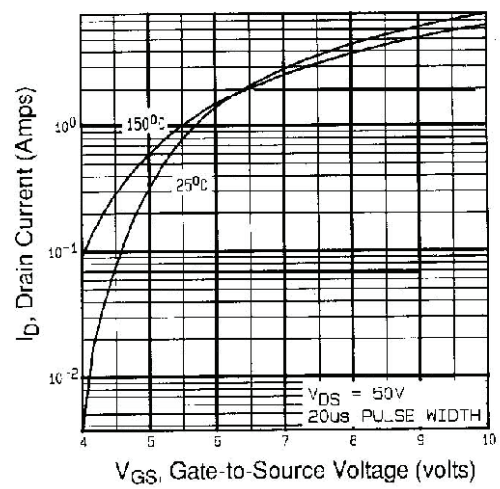


Fig. 2 - Typical Transfer Characteristics

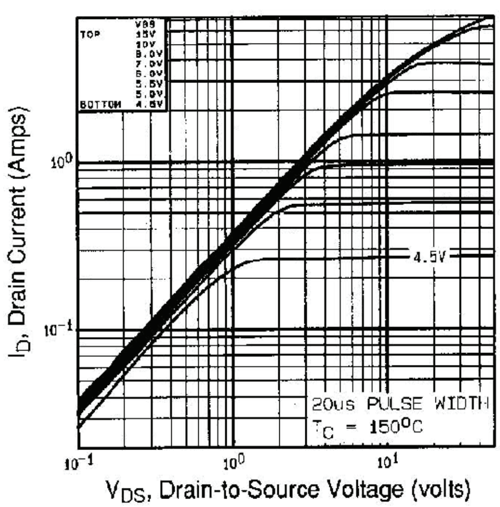


Fig. 1 - Typical Output Characteristics, T_C = 150 °C

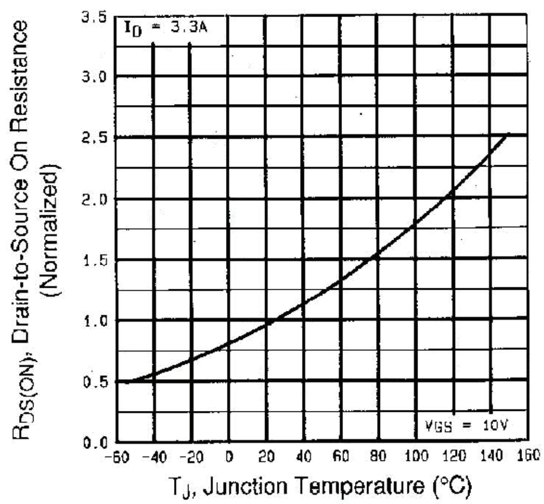


Fig. 3 - Normalized On-Resistance vs. Temperature

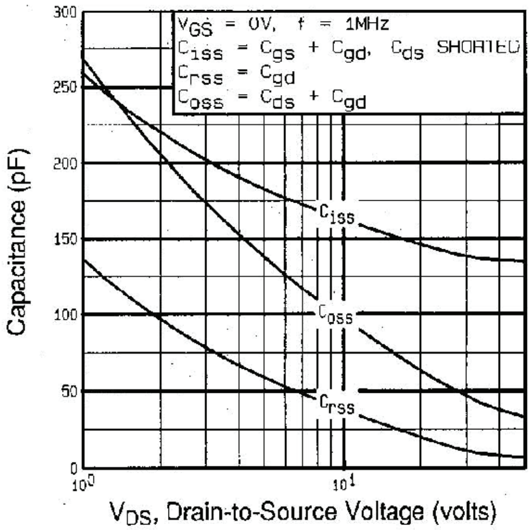


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

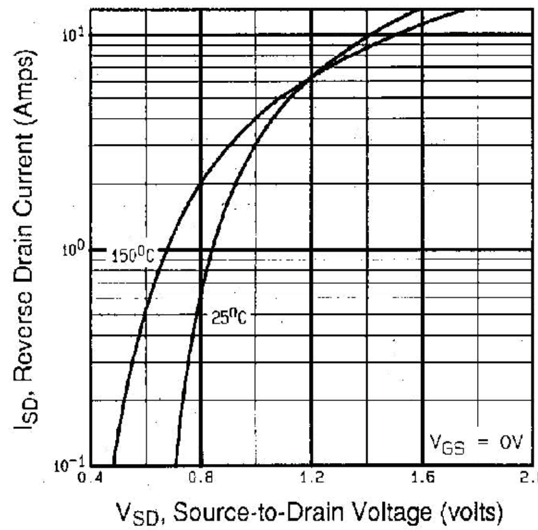


Fig. 6 - Typical Source-Drain Diode Forward Voltage

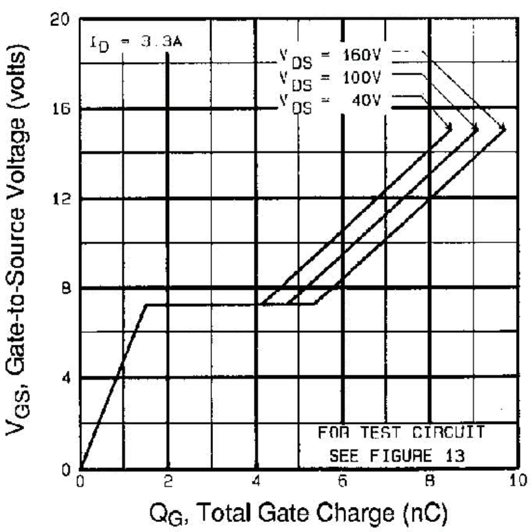


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

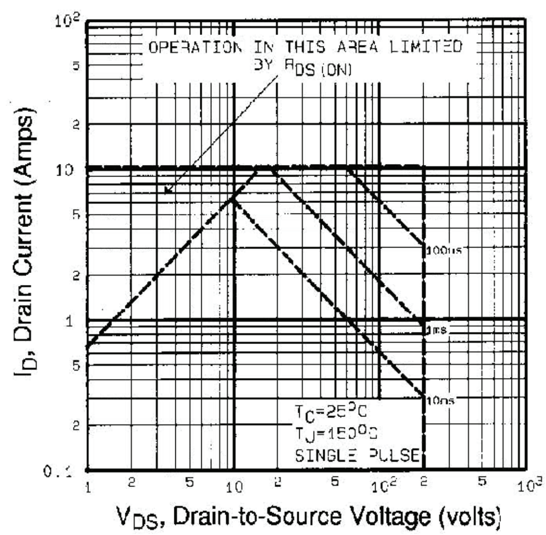


Fig. 7 - Maximum Safe Operating Area

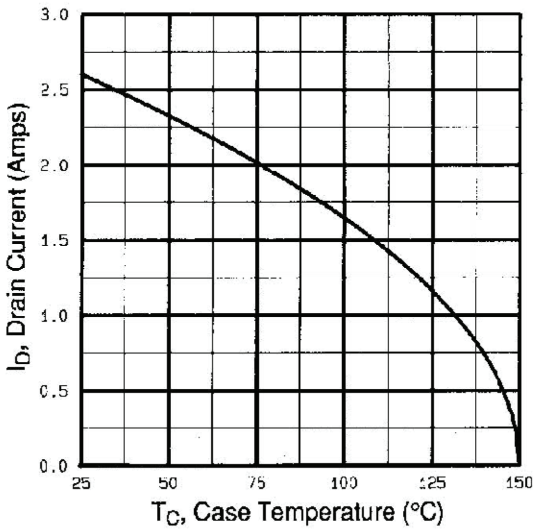


Fig. 8 - Maximum Drain Current vs. Case Temperature

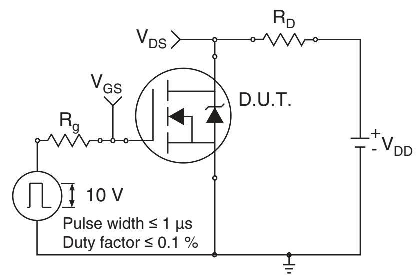


Fig. 10a - Switching Time Test Circuit

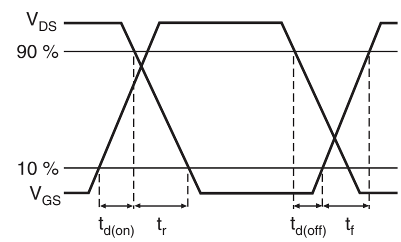


Fig. 10b - Switching Time Waveforms

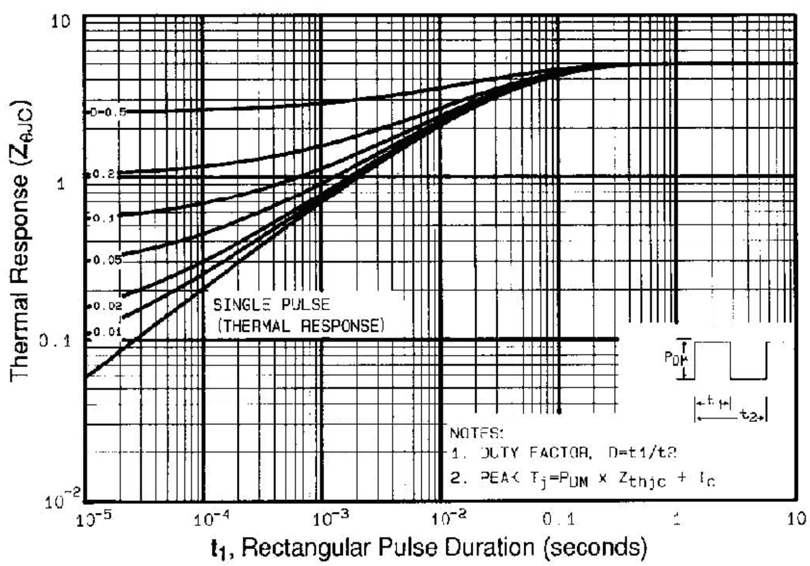


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

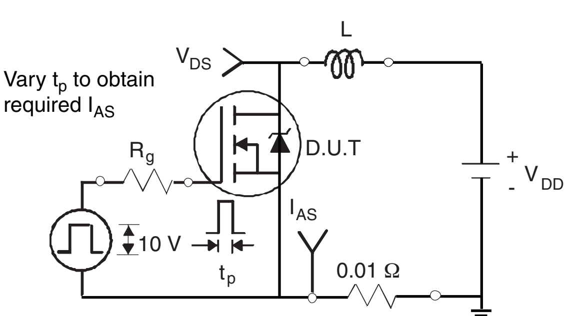


Fig. 12a - Unclamped Inductive Test Circuit

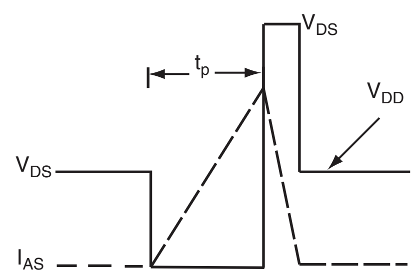


Fig. 12b - Unclamped Inductive Waveforms

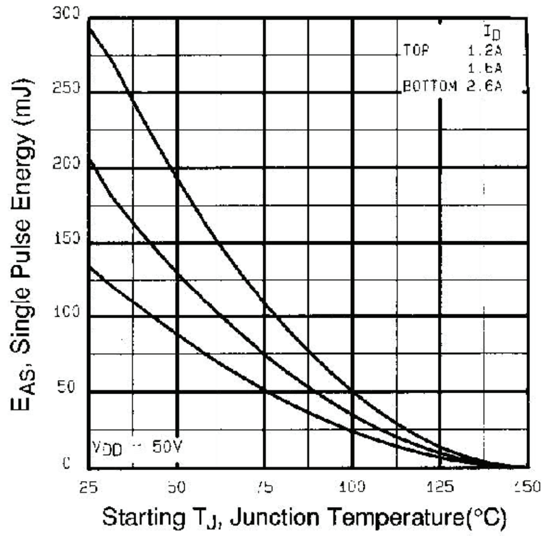


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

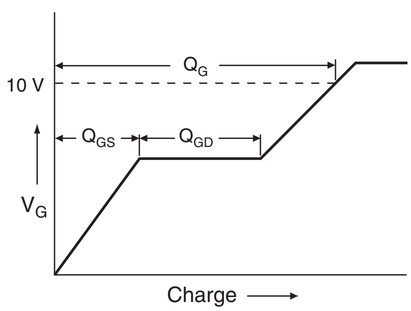


Fig. 13a - Basic Gate Charge Waveform

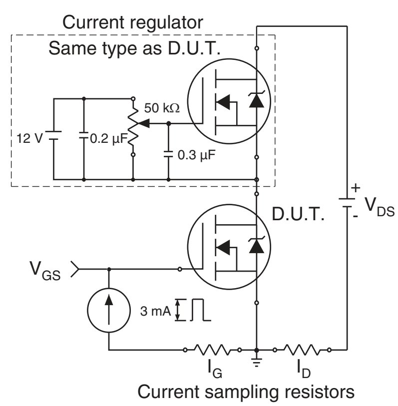
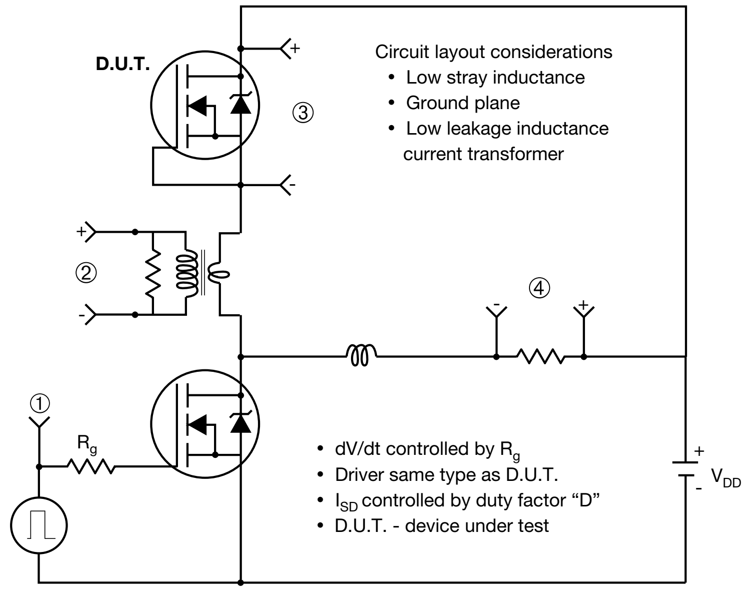
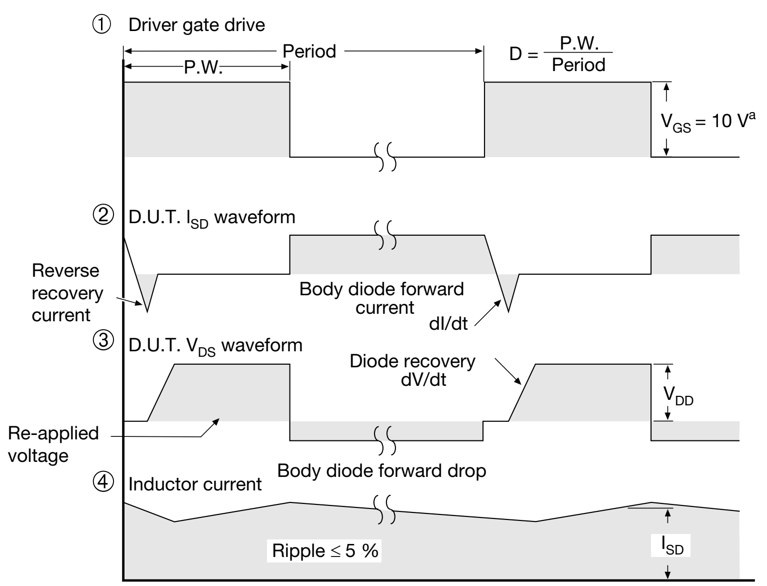


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

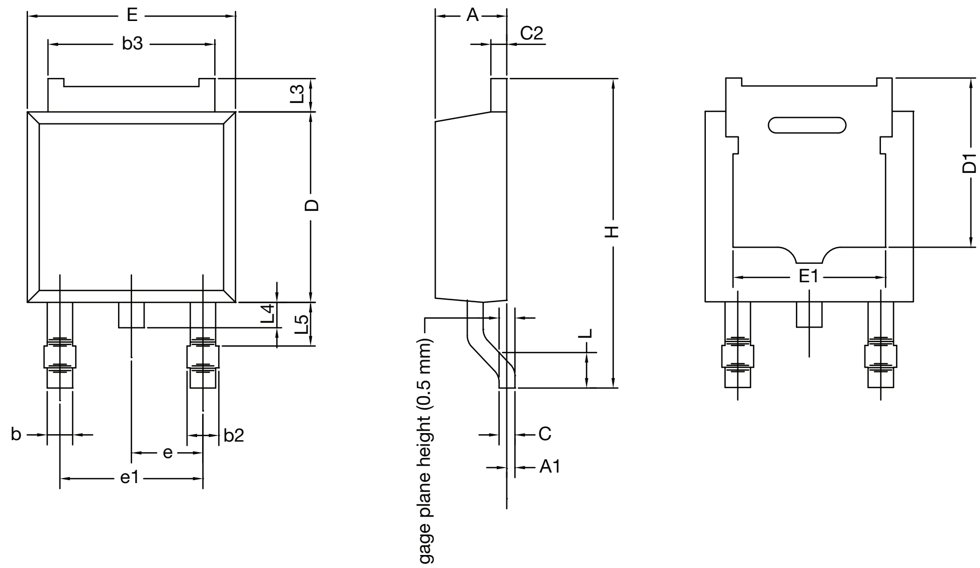
a. V_{GS} = 5 V for logic level devices

Fig. 10 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91268.

TO-252AA Case Outline

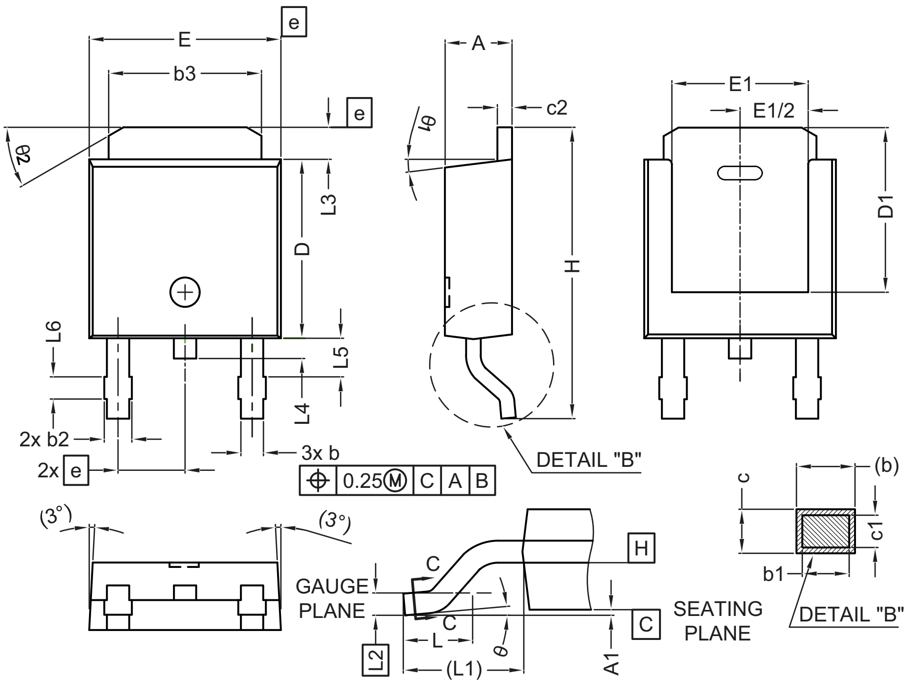
VERSION 1: FACILITY CODE = Y



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note
- Dimension L3 is for reference only

VERSION 2: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

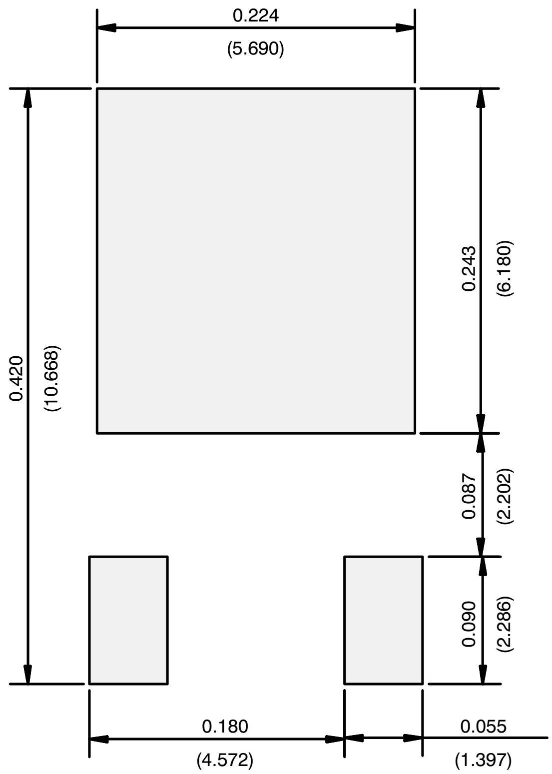
	MILLIMETERS	
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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