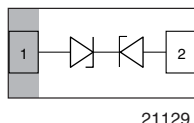
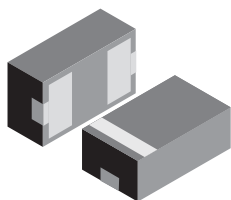


## Bidirectional Symmetrical (BiSy) Low Capacitance, Single-Line ESD Protection Diode in LLP1006-2M



21129



20855

### MARKING (example only)



21121

Bar = pin 1 marking

X = date code

Y = type code (see table below)

### DESIGN SUPPORT TOOLS


[click logo to get started](#)

### FEATURES

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range  $\pm 5.5$  V
- Low leakage current  $I_R < 0.1 \mu A$
- Very low load capacitance  $C_D = 0.3$  pF
- ESD immunity acc. IEC 61000-4-2  
 $\pm 15$  kV contact discharge  
 $\pm 16$  kV air discharge
- Soldering can be checked by standard vision inspection; no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

### ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS05L1-DD1	VBUS05L1-DD1-G-08	8000	8000

### PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS05L1-DD1	LLP1006-2M	R	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

### ABSOLUTE MAXIMUM RATINGS VBUS05L1-DD1

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	$I_{PPM}$	2	A
Peak pulse power	Pin 1 to pin 2, acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	$P_{PP}$	34	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 15$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 16$	kV
Operating temperature	Junction temperature	$T_J$	-40 to +125	°C
Storage temperature		$T_{STG}$	-40 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

**ELECTRICAL CHARACTERISTICS VBUS05L1-DD1**

( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at $I_R = 0.05\text{ }\mu\text{A}$	$V_R$	5.5	-	-	V
Reverse current	at $V_{RWM} = 5.5\text{ V}$	$I_R$	-	-	0.05	$\mu\text{A}$
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	$V_{BR}$	7	8.4	9.5	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$	$V_C$	-	11.5	14	V
	at $I_{PP} = I_{PPM} = 2\text{ A}$	$V_C$	-	14	17	V
Capacitance	at $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$	$C_D$	-	0.33	0.4	pF
	at $V_R = 2.5\text{ V}$ , $f = 1\text{ MHz}$	$C_D$	-	0.34	-	pF

**VBUS05L1-DD1: ESD PROTECTION WITH LOWEST LOAD CAPACITANCE**

The VBUS05L1-DD1 is a bidirectional and symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05L1-DD1 offers a high isolation (low leakage current, lowest capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006-2M package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.

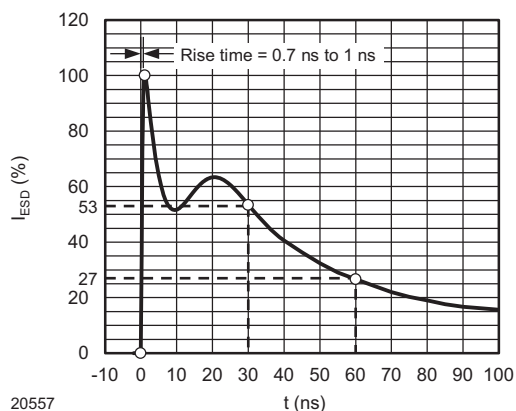
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

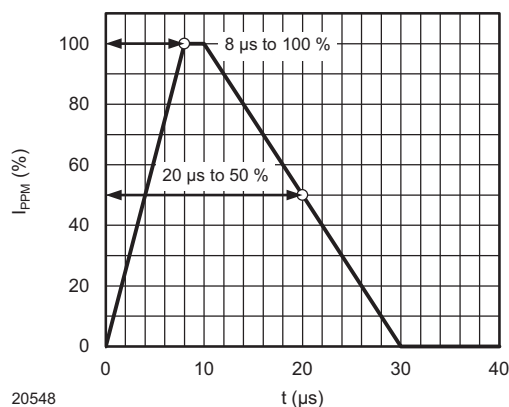


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

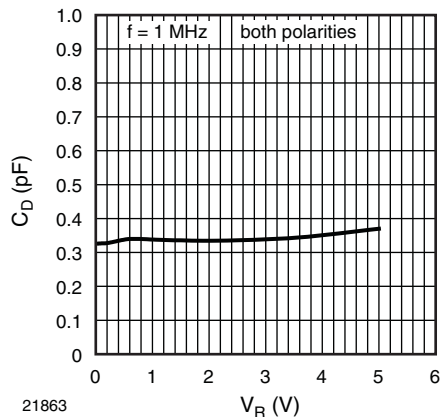
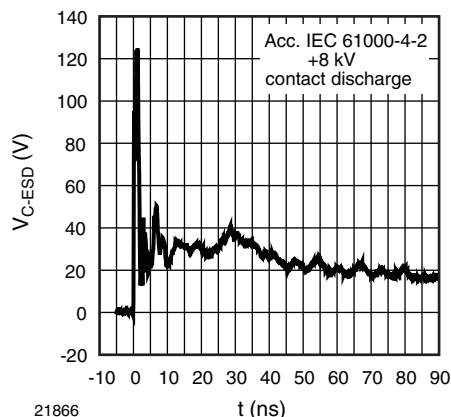

Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$ 


Fig. 6 - Typical Clamping Performance at +8 kV Contact Discharge (acc. IEC 61000-4-2)

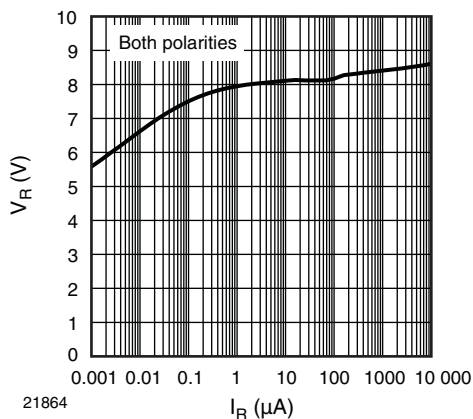
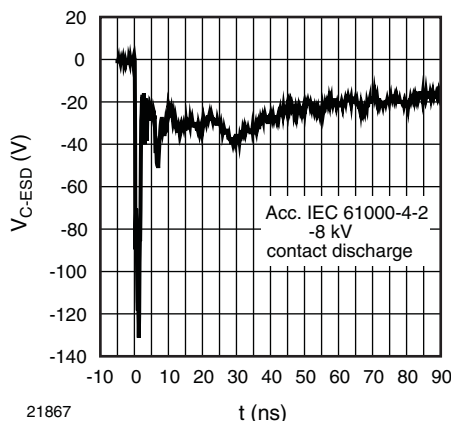

Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$ 


Fig. 7 - Typical Clamping Performance at -8 kV Contact Discharge (acc. IEC 61000-4-2)

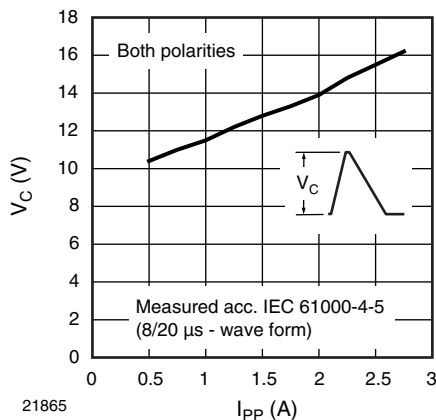
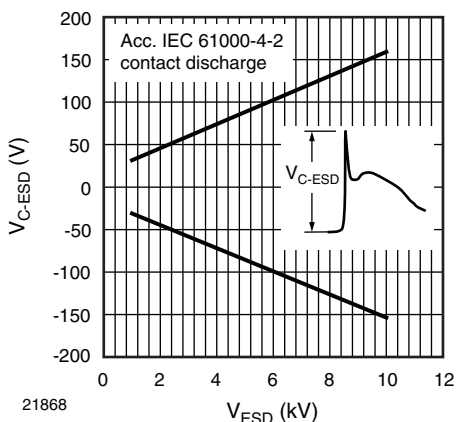
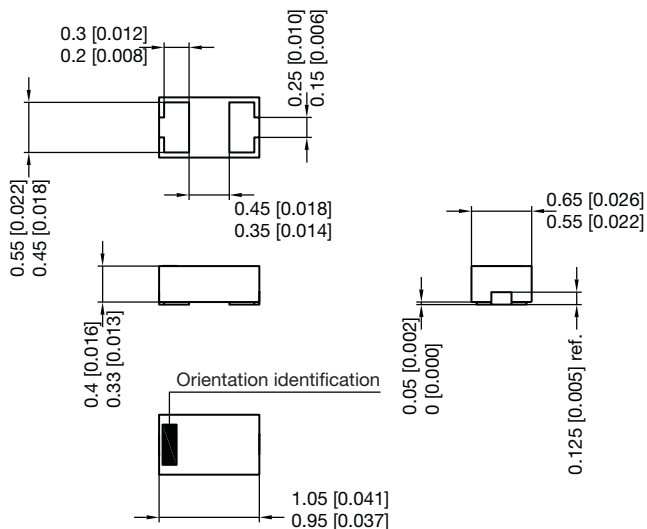
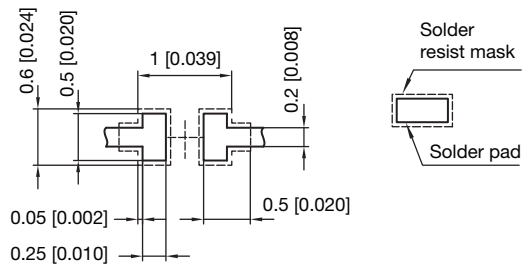
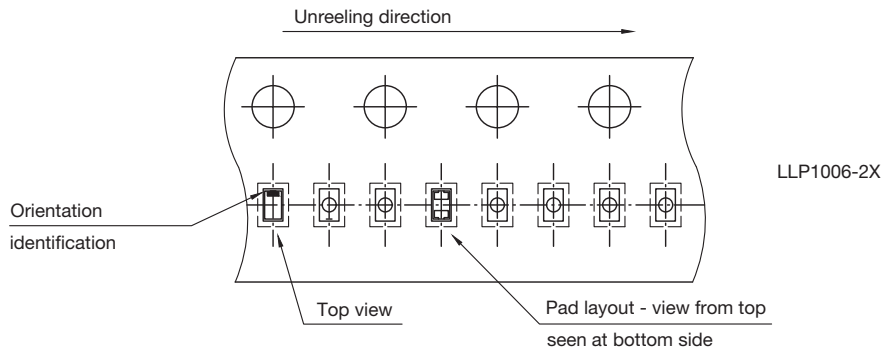

Fig. 5 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$ 


Fig. 8 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

**PACKAGE DIMENSIONS** in millimeters (inches): **LLP1006-2M**

**Foot print recommendation:**


Pad Design Patented:  
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Rev. 7 - Date: 11.May 2016  
20812



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02.05.2017  
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