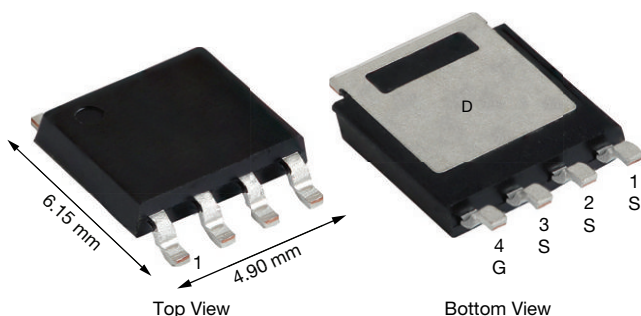
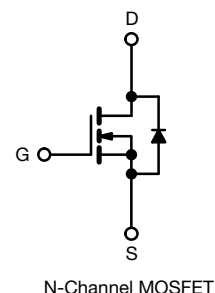


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L


FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0046
I_D (A)	130
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	I_D	$T_C = 25$ °C	130
		$T_C = 125$ °C	75
Continuous source current (diode conduction)	I_S	134	A
Pulsed drain current ^a	I_{DM}	238	
Single pulse avalanche current	I_{AS}	23	
Single pulse avalanche energy	E_{AS}	26.5	mJ
Maximum power dissipation ^a	P_D	$T_C = 25$ °C	148
		$T_C = 125$ °C	49
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	68	°C/W
Junction-to-case (drain)	R_{thJC}	1.0	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 15 A	-	0.0036	0.0046	Ω
		V _{GS} = 10 V	I _D = 15 A, T _J = 125 °C	-	-	0.0074	
		V _{GS} = 10 V	I _D = 15 A, T _J = 175 °C	-	-	0.0088	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 10 A		-	45	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	1510	1960	pF
Output capacitance	C _{oss}			-	510	665	
Reverse transfer capacitance	C _{rss}			-	34	45	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 10 A	-	26	36	nC
Gate-source charge ^c	Q _{gs}			-	7.6	-	
Gate-drain charge ^c	Q _{gd}			-	5.5	-	
Gate resistance	R _g	f = 1 MHz		2.0	3.5	5.6	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		-	11	16.5	ns
Rise time ^c	t _r			-	4.4	6.2	
Turn-off delay time ^c	t _{d(off)}			-	21.5	30	
Fall time ^c	t _f			-	5.7	8	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	238	A
Forward voltage	V _{SD}	I _F = 15 A, V _{GS} = 0 V		-	-	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 40 A, di/dt = 100 A/μs		-	28.4	40	ns
Body diode reverse recovery charge	Q _{rr}			-	15.8	22.2	nC
Reverse recovery fall time	t _a			-	13.8	19.3	ns
Reverse recovery rise time	t _b			-	14.9	20.9	
Body diode peak reverse recovery current	I _{RM(REC)}			-	0.94	1.3	A

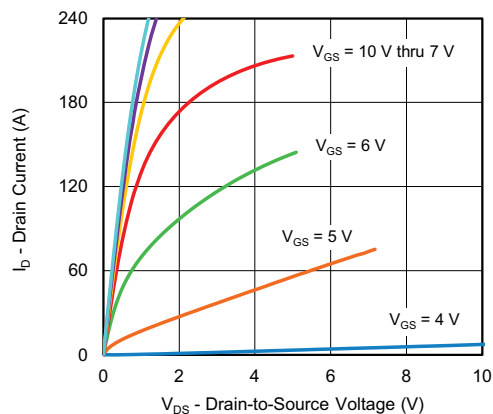
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

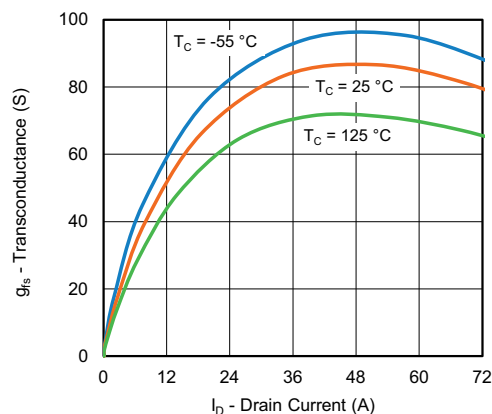
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



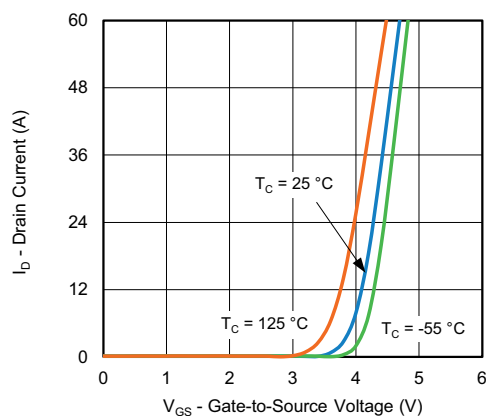
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



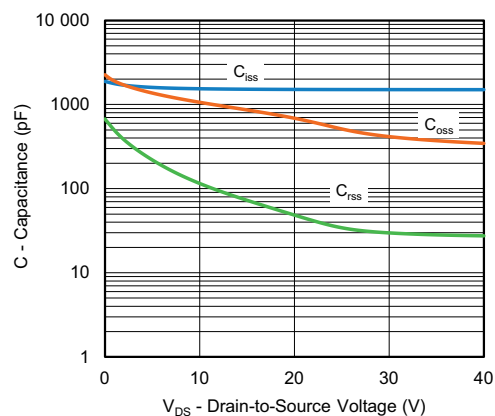
Output Characteristics



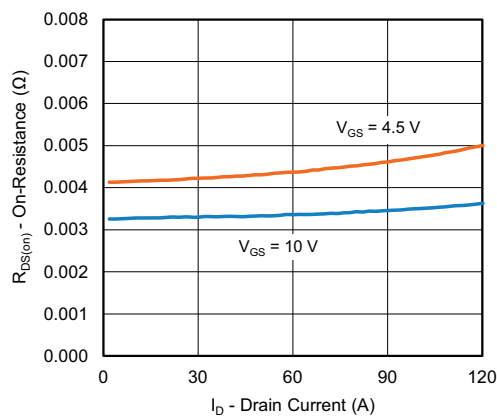
Transconductance



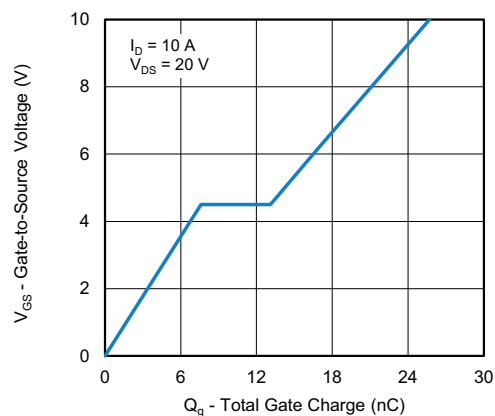
Transfer Characteristics



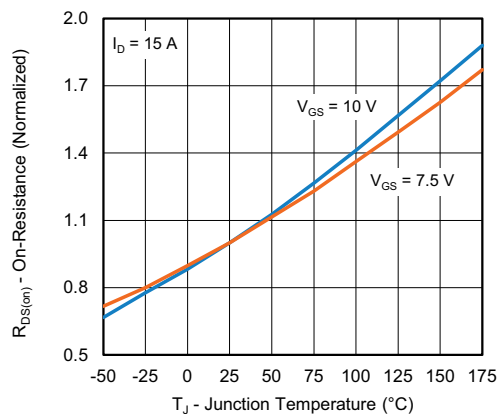
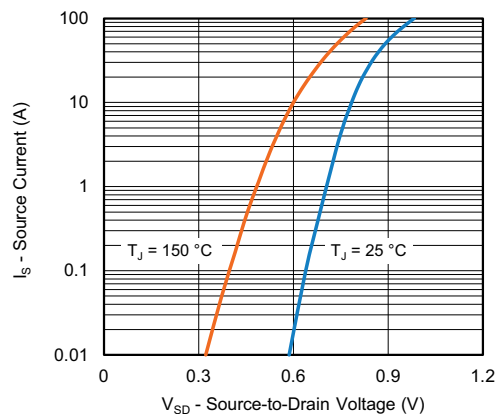
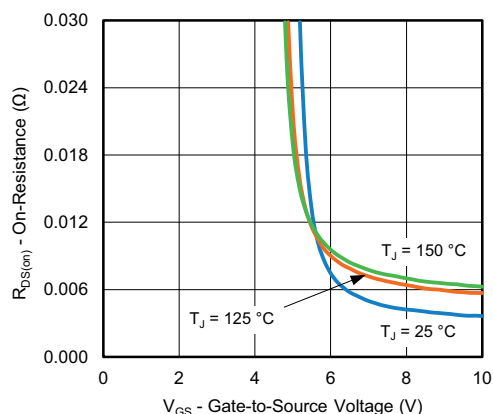
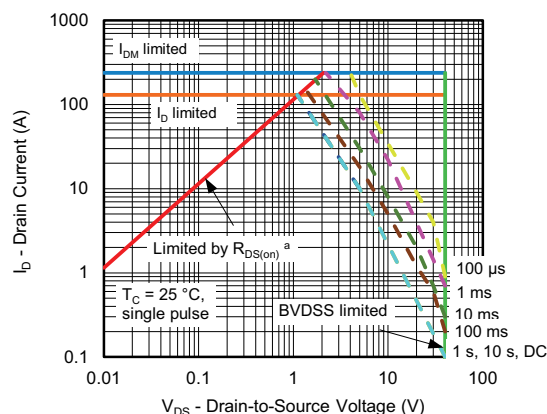
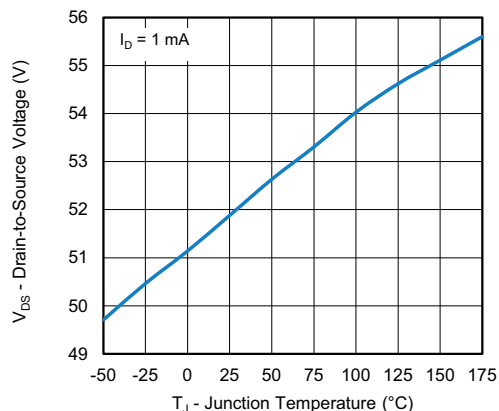
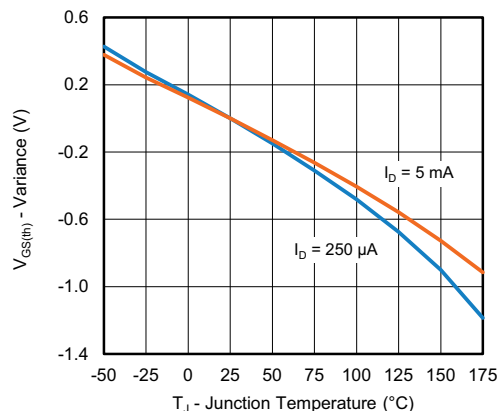
Capacitance



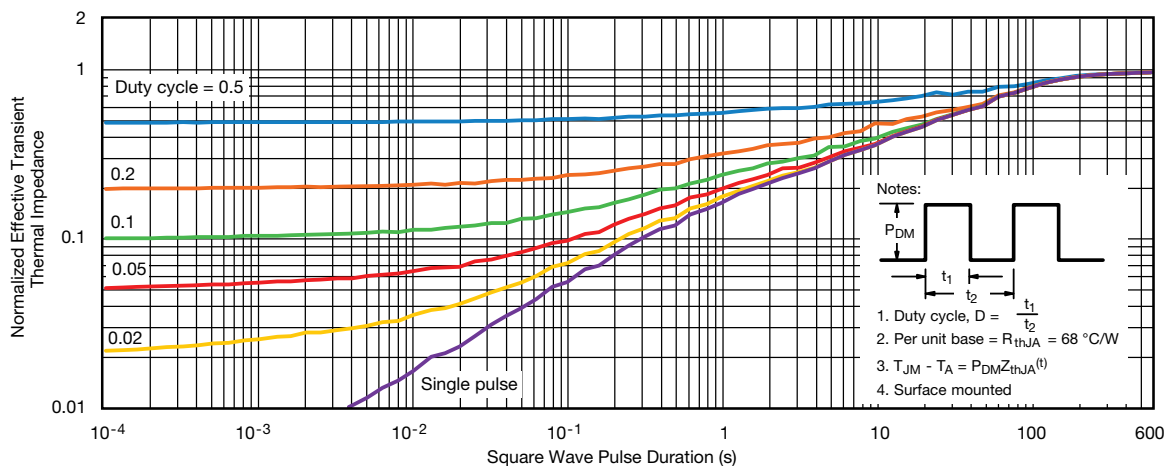
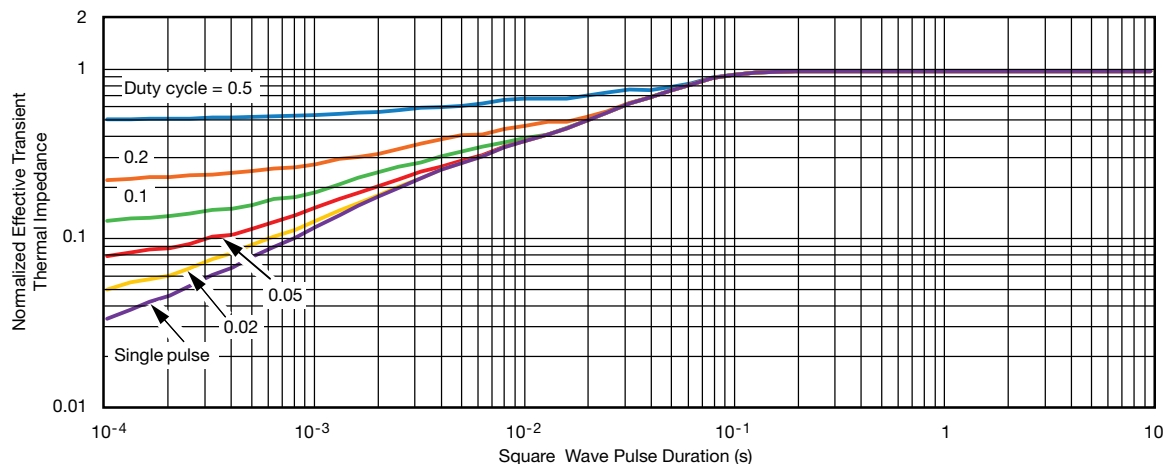
On-Resistance vs. Drain Current



Gate Charge

**TYPICAL CHARACTERISTICS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source Drain Diode Forward Voltage****On-Resistance vs. Gate-to Source Voltage****Safe Operating Area****Drain Source Breakdown vs. Junction Temperature****Threshold Voltage****Note**

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

**TYPICAL CHARACTERISTICS** ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case****Note**

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77430.

PowerPAK® SO-8L (PPKS08LWLA) Case Outline 3



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°

ECN: C23-1016-Rev. D, 18-Sep-2023

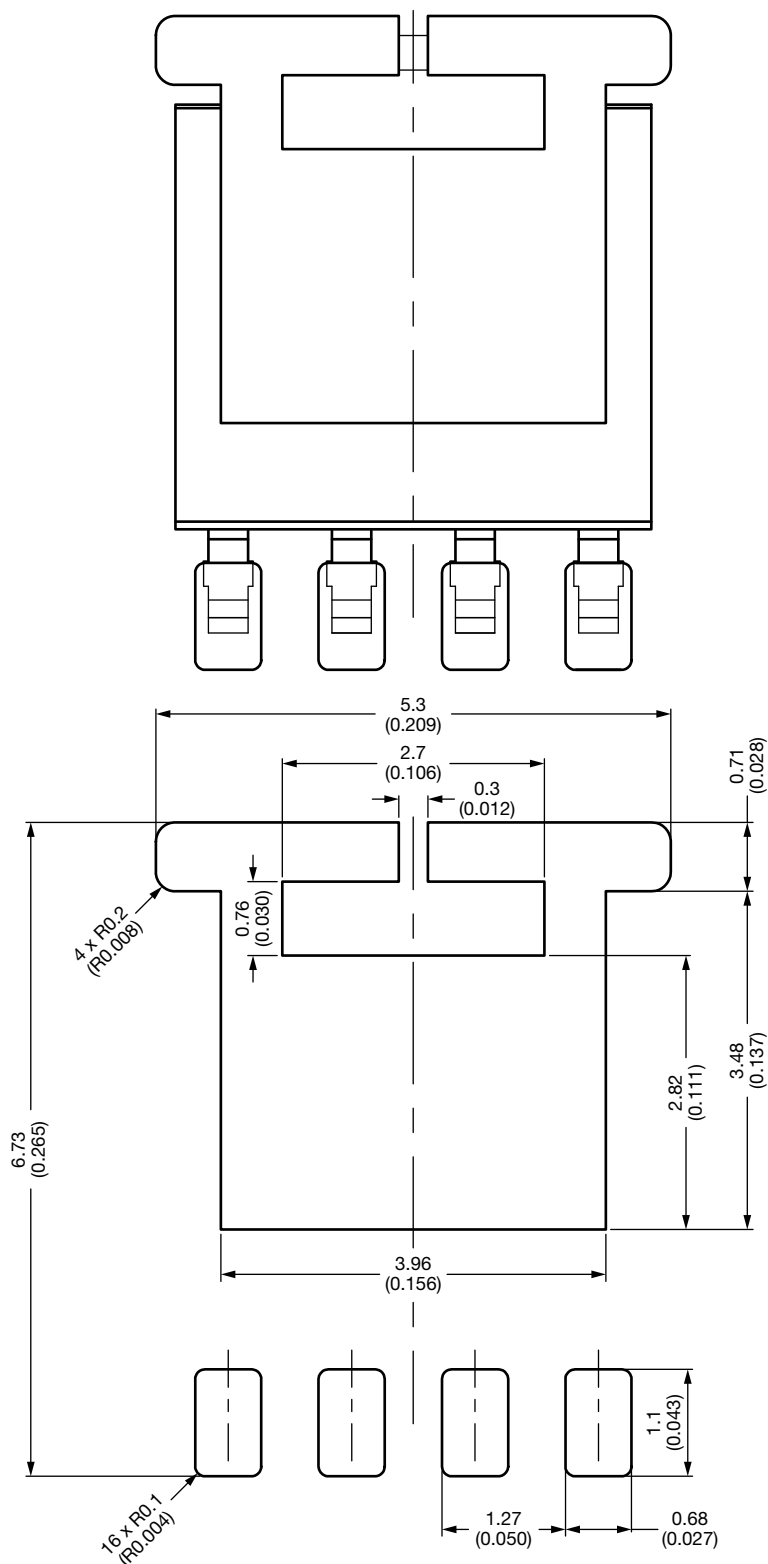
DWG: 6067

Note

- Millimeter will govern



Recommended Land Pattern PowerPAK® SO-8L Single Short Ear



Dimensions in Millimeters (Inches)



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