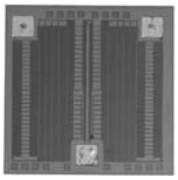
Thin Film MΩ Center-Tap Chip Resistor Divider Network



Product may not be to scale

The CTM resistor chips extends the resistance range to 10M in a center tap configuration while keeping the die size relatively small.

The CTMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTMs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- Wire bondable
- Resistance range total: 200 kΩ to 10 MΩ
- Center tap
- Chip size: 0.040" x 0.040"
- Case: 0404
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant

Pb-free

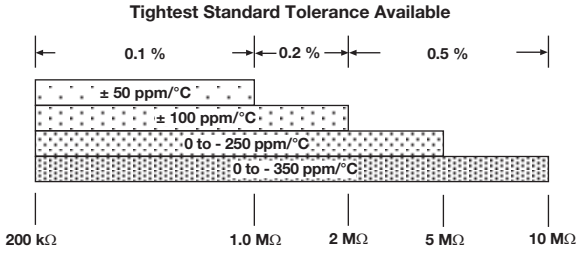
RoHS COMPLIANT

GREEN (5-2008)

APPLICATIONS

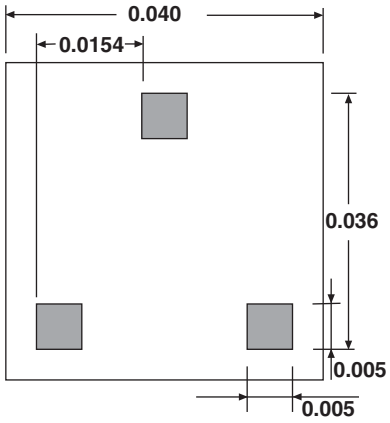
Vishay EFI CTM tapped megohm resistor chips are designed for hybrid packages requiring high value, two resistor combinations.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Total Resistance Range	200K to 10M	Ω
Standard Tolerances	± 0.1, ± 0.2, ± 0.5	%
TCR	± 50, ± 100, 0, - 250, - 350	ppm/°C

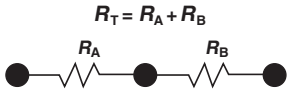


STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
TCR Tracking Between Resistors	± 5	ppm/°C
Ratio/Ratio, R_A/R_B: Tolerance	1 ± 1 standard	%
Noise	- 12 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, + 125 °C, 10 mW	± 0.5 max. absolute ± 0.005 ratio	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. $\Delta R/R$	%
High Temperature Exposure, + 150 °C, 100 h	± 0.5 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at + 70 °C (derated to zero at + 175 °C)	0.02 max.	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 max. $\Delta R/R$	%

DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS

PARAMETER	VALUE
Chip Size	0.040" x 0.040" ± 0.002" (1.02 mm x 1.02 mm ± 0.05 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm) min.
Number of Pads	3
Pad Material	10 kÅ minimum gold (Al optional)
Backing	None, lapped semiconductor silicon (Au optional)

GLOBAL PART NUMBER INFORMATION

Global Part Number: CTM50002KCKKGNHWS

Global Part Number Description: CTM 500K 10 % RT 0.25 % ± 100 ppm/°C ± 10 ppm/°C Au None H WS

C	T	M	5	0	0	0	2	K	C	K	K	G	N	H	W	S

MODEL	RESISTANCE (*R* TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TCR TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
CTM	First 4 digits are significant figures of resistance	**2** = 100 **3** = 1000 **4** = 10 000	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **J** = 5.0 **K** = 10.0	**C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **N** = No	**C** = ± 50 **K** = ± 100 **R** = 0/- 250 **P** = 0/- 350	**J** = ± 5 **K** = ± 10 **N** = No	**G** = Au **A** = Al	**G** = Au **N** = None	**H** = Class H **K** = Class K	**WS** = Waffle pack 100 min., 1 mult

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