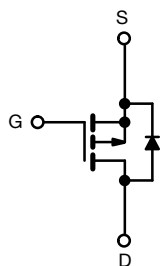
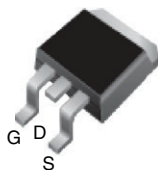


Power MOSFET

D²PAK (TO-263)


P-Channel MOSFET

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- P-channel
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

The power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

PRODUCT SUMMARY

V _{DS} (V)	-200	
R _{DS(on)} (Ω)	V _{GS} = -10 V	1.5
Q _g max. (nC)	22	
Q _{gs} (nC)	12	
Q _{gd} (nC)	10	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9620S-GE3	SiHF9620STRL-GE3 ^a
Lead (Pb)-free	IRF9620SPbF	IRF9620STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-200	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	V _{GS} at -10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	-14	W/°C
Linear Derating Factor		0.32	
Linear Derating Factor (PCB mount) ^e		0.025	A
Inductive Current, Clamp	I _{LM}	-14	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
Maximum Power Dissipation (PCB mount) ^e		T _A = 25 °C	
Peak Diode Recovery dV/dt ^c	dV/dt	-5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
- Not Applicable
- I_{SD} ≤ -3.5 A, dI/dt ≤ 95 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	62	°C/W
Maximum Junction-to-Ambient (PCB mount) ^a	R_{thJA}	-	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.1	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = -1 mA		-	-0.22	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-2.0	-	-4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -200 V, V _{GS} = 0 V		-	-	-100	μA
		V _{DS} = -160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	-500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -1.5 A ^b	-	-	1.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = -50 V, I _D = -1.5 A		1.0	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz, see fig. 10		-	350	-	pF
Output Capacitance	C _{oss}			-	100	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = -10 V	I _D = -4.0 A, V _{DS} = -160 V, see fig. 11 and 18 ^b	-	-	22	nC
Gate-Source Charge	Q _{gs}			-	-	12	
Gate-Drain Charge	Q _{gd}			-	-	10	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -100 V, I _D = -1.5 A, R _G = 50 Ω, R _D = 67 Ω, see fig. 17 ^b		-	15	-	ns
Rise Time	t _r			-	25	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	15	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain		0.9	-	5.7	Ω
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-3.5	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	-14	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = -3.5 A, V _{GS} = 0 V ^b		-	-	-7.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = -3.5 A, dI/dt = 100 A/μs ^b		-	300	450	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.9	2.9	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5)
b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\ \%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

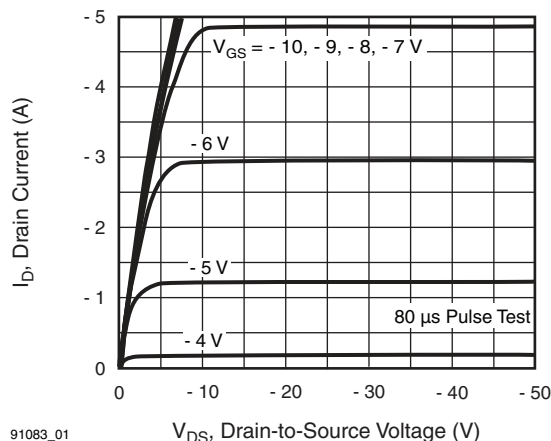


Fig. 1 - Typical Output Characteristics

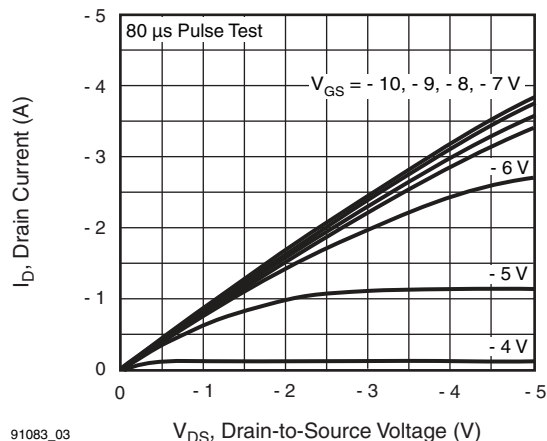


Fig. 3 - Typical Saturation Characteristics

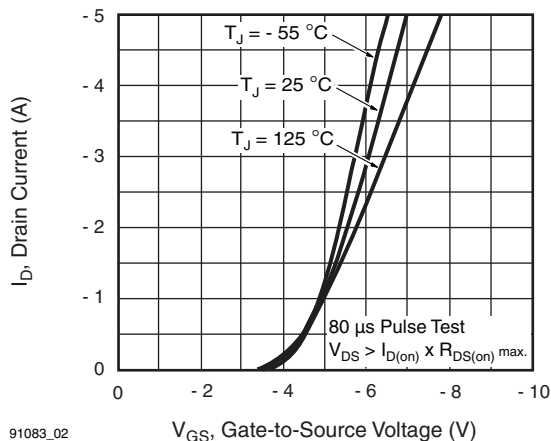


Fig. 2 - Typical Transfer Characteristics

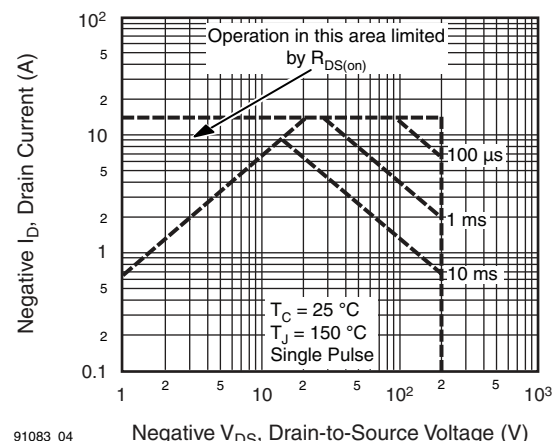


Fig. 4 - Maximum Safe Operating Area

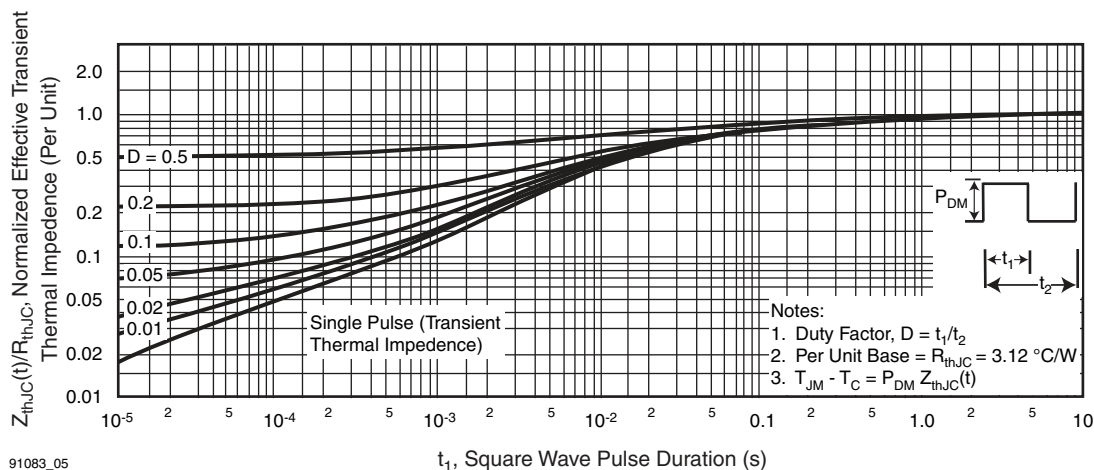
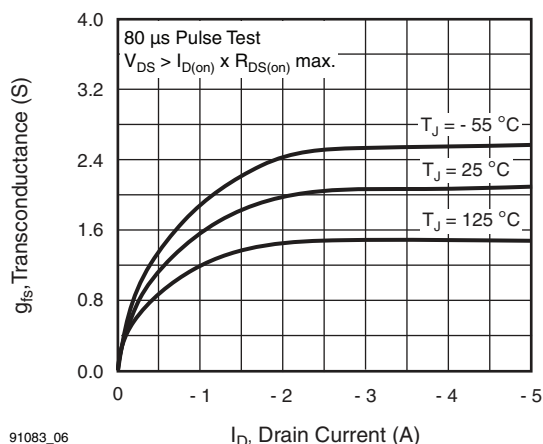
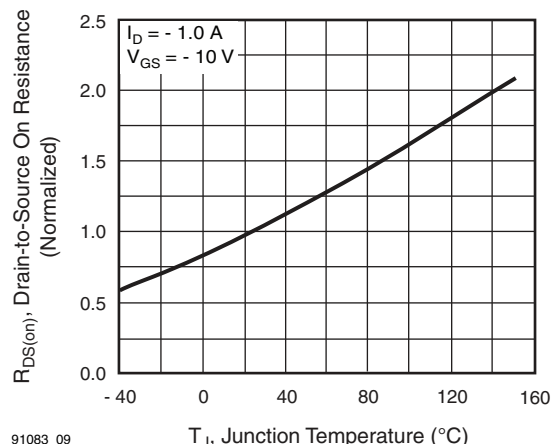
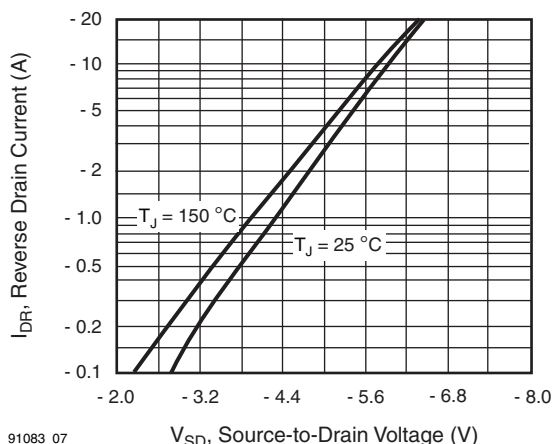
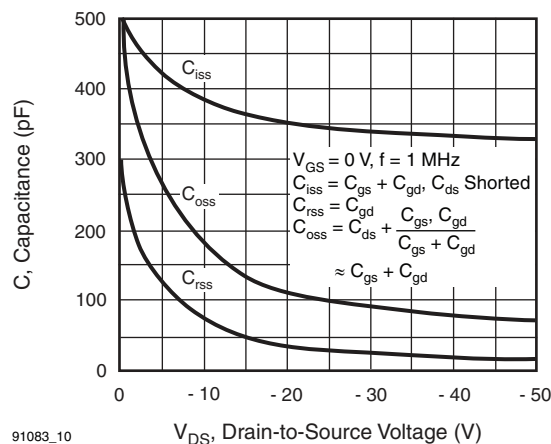
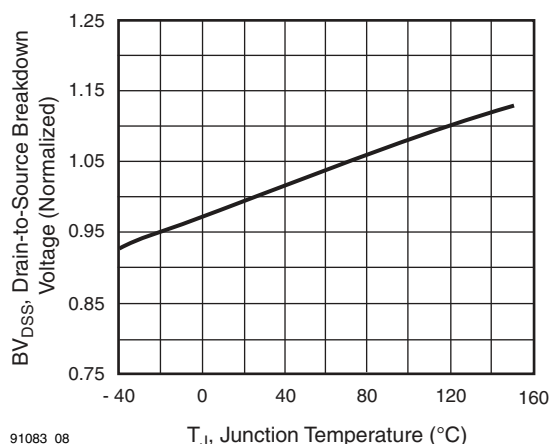
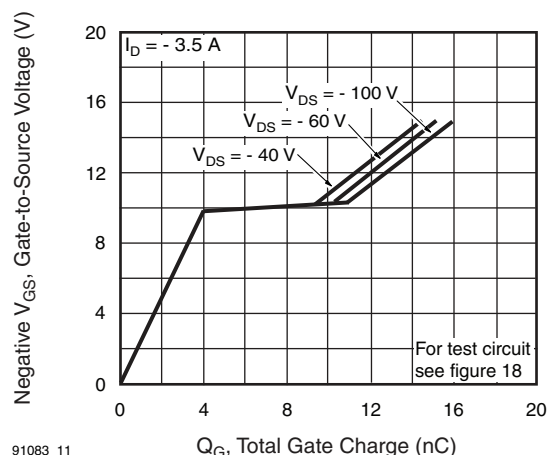
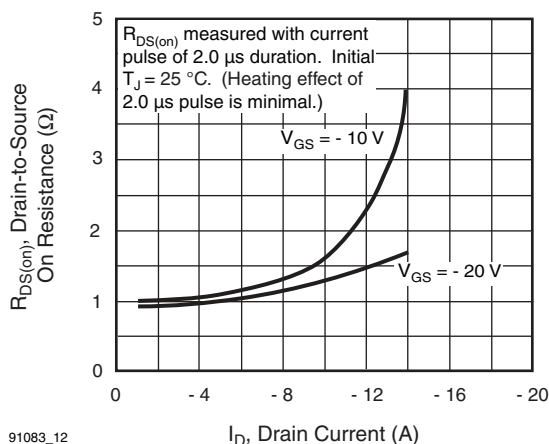
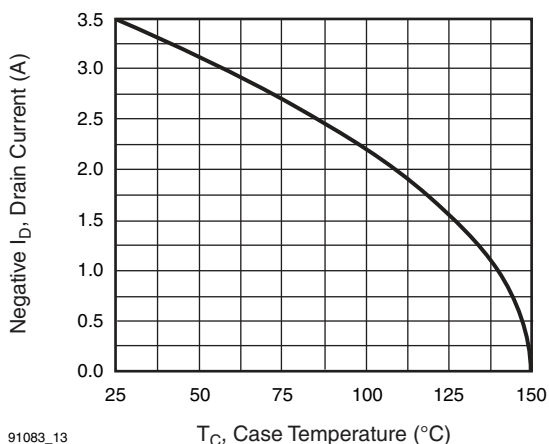


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

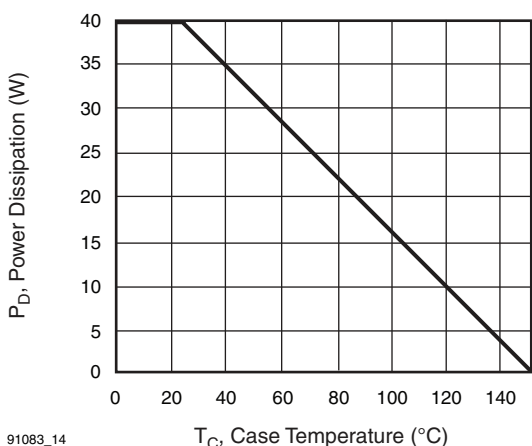

Fig. 6 - Typical Transconductance vs. Drain Current

Fig. 9 - Normalized On-Resistance vs. Temperature

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 8 - Breakdown Voltage vs. Temperature

Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage



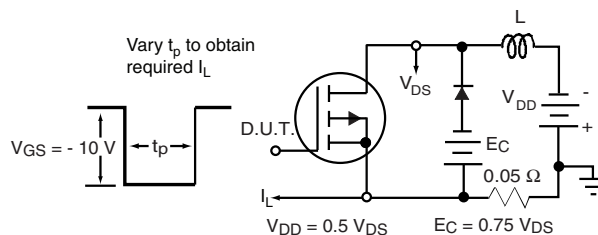
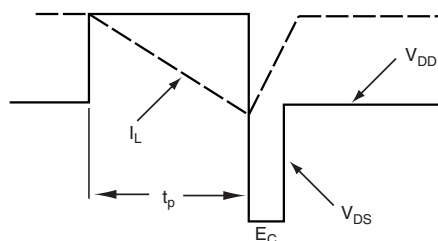
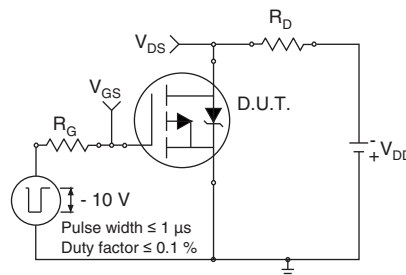
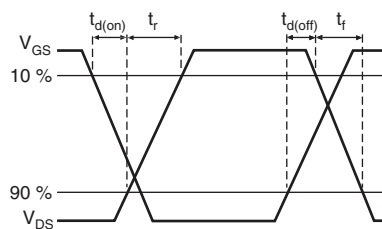
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Fig. 12 - Typical On-Resistance vs. Drain Current


91083_13

Fig. 13 - Maximum Drain Current vs. Case Temperature


91083_14

Fig. 14 - Power vs. Temperature Derating Curve

Fig. 15 - Clamped Inductive Test Circuit

Fig. 16 - Clamped Inductive Waveforms

Fig. 17a - Switching Time Test Circuit

Fig. 17b - Switching Time Waveforms

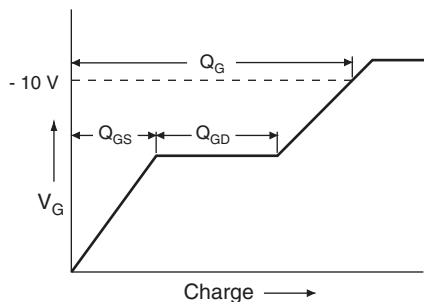


Fig. 18a - Basic Gate Charge Waveform

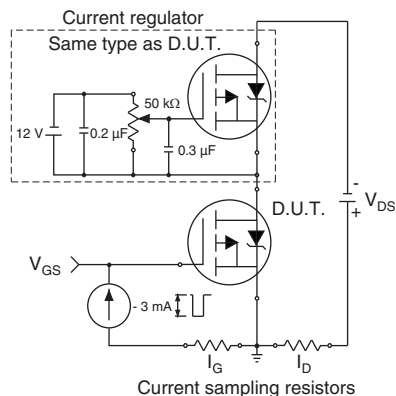
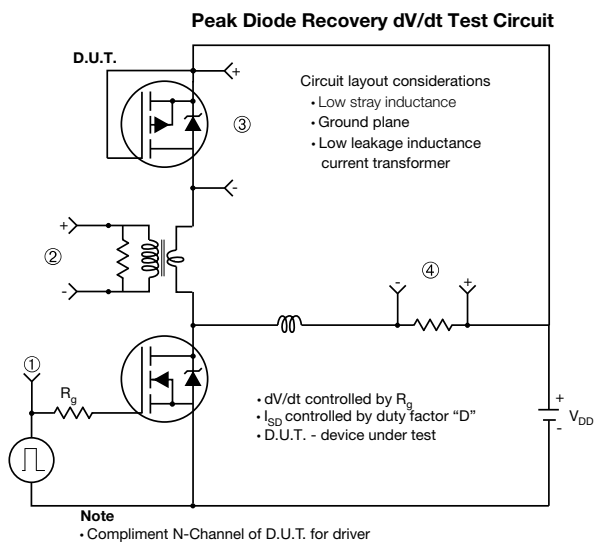
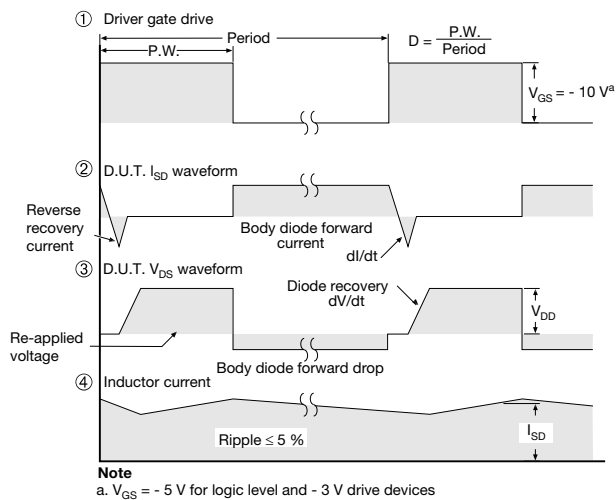


Fig. 18b - Gate Charge Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver

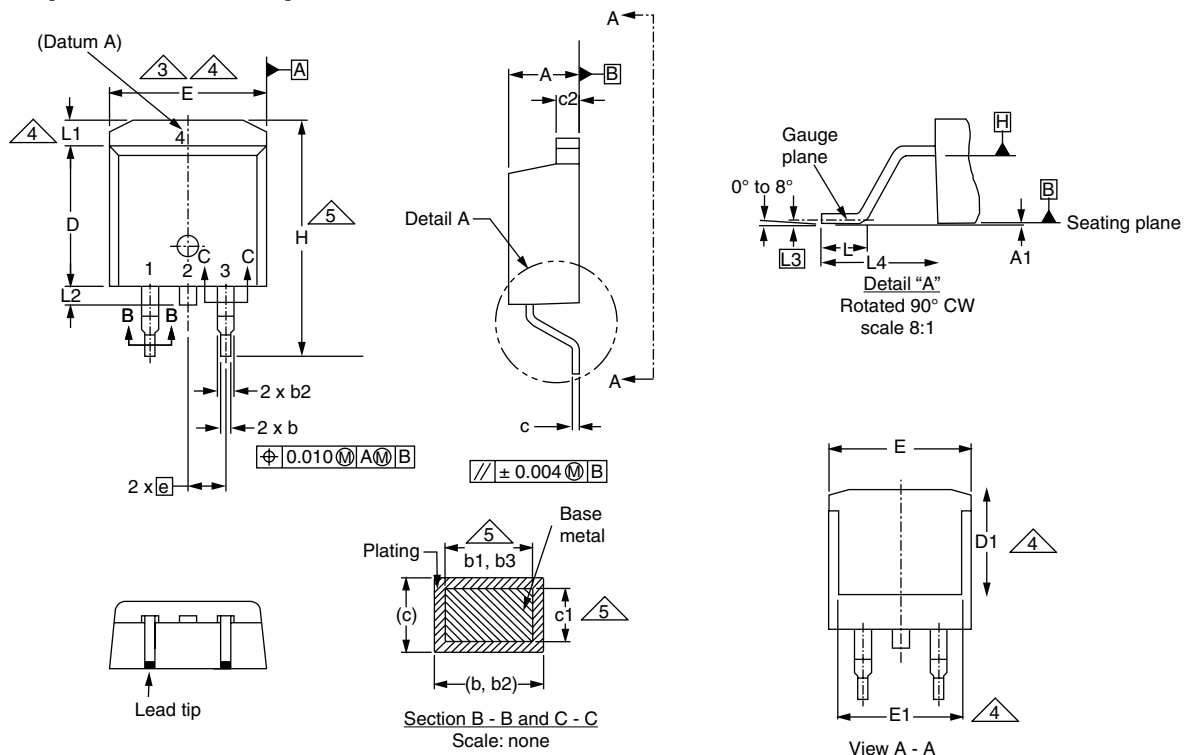


Note
a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 19 - For P-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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