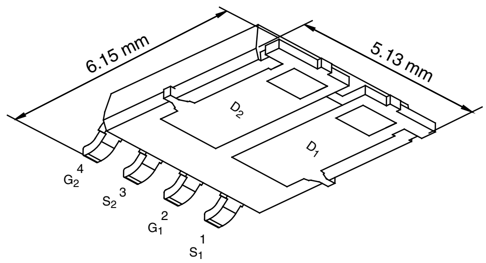
Automotive N- and P-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	**P-CHANNEL**
V_{DS} (V)	40	- 40
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm$ 10 V	0.014	0.028
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm$ 4.5 V	0.015	0.042
I_D (A)	8	- 8
Configuration	N- and P-Pair	

PowerPAK® SO-8L Dual

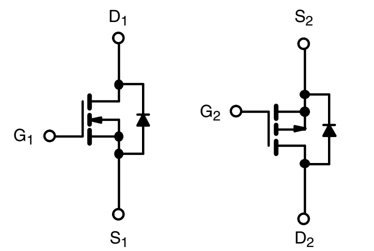


Bottom View

FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified[d]
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE



N-Channel MOSFET P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ500EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		**SYMBOL**	**N-CHANNEL**	**P-CHANNEL**	**UNIT**
Drain-Source Voltage		V_{DS}	40	- 40	V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current[a]	T_C = 25 °C	I_D	8	- 8	A
	T_C = 125 °C		8	- 8	
Continuous Source Current (Diode Conduction)[a]		I_S	8	- 8	
Pulsed Drain Current[b]		I_{DM}	32	- 32	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	30	- 30	
Single Pulse Avalanche Energy		E_{AS}	45	45	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	48	48	W
	T_C = 125 °C		16	16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175		°C
Soldering Recommendations (Peak Temperature)[e, f]			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**N-CHANNEL**	**P-CHANNEL**	**UNIT**
Junction-to-Ambient	PCB Mount[c]	R_{thJA}	85	85	°C/W
Junction-to-Case (Drain)		R_{thJC}	3.1	3.1	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR4 material).
d. Parametric verification ongoing.
e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Static								
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		N-Ch	40	-	-	V
		V_{GS} = 0 V, I_D = - 250 μA		P-Ch	- 40	-	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		N-Ch	1.3	1.8	2.3	
		V_{DS} = V_{GS}, I_D = - 250 μA		P-Ch	- 1.5	- 2	- 2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	N-Ch	-	-	1	μA
		V_{GS} = 0 V	V_{DS} = - 40 V	P-Ch	-	-	- 1	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	N-Ch	-	-	50	
		V_{GS} = 0 V	V_{DS} = - 40 V, T_J = 125 °C	P-Ch	-	-	- 50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	N-Ch	-	-	150	
		V_{GS} = 0 V	V_{DS} = - 40 V, T_J = 175 °C	P-Ch	-	-	- 150	
On-State Drain Current[a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	N-Ch	25	-	-	A
		V_{GS} = - 10 V	V_{DS} ≤ 5 V	P-Ch	- 25	-	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 8 A	N-Ch	-	0.011	0.014	Ω
		V_{GS} = - 10 V	I_D = - 8 A	P-Ch	-	0.022	0.028	
		V_{GS} = 10 V	I_D = 8 A, T_J = 125 °C	N-Ch	-	-	0.017	
		V_{GS} = - 10 V	I_D = - 8 A, T_J = 125 °C	P-Ch	-	-	0.041	
		V_{GS} = 10 V	I_D = 8 A, T_J = 175 °C	N-Ch	-	-	0.025	
		V_{GS} = - 10 V	I_D = - 8 A, T_J = 175 °C	P-Ch	-	-	0.049	
		V_{GS} = 4.5 V	I_D = 6 A	N-Ch	-	0.012	0.015	
		V_{GS} = - 4.5 V	I_D = - 6 A	P-Ch	-	0.033	0.042	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 8 A		N-Ch	-	40	-	S
		V_{DS} = - 15 V, I_D = - 8 A		P-Ch	-	18	-	
Dynamic[b]								
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	N-Ch	-	1799	2248	pF
		V_{GS} = 0 V	V_{DS} = - 20 V, f = 1 MHz	P-Ch	-	1756	2195	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	N-Ch	-	282	352	
		V_{GS} = 0 V	V_{DS} = - 20 V, f = 1 MHz	P-Ch	-	296	370	
Reverse Transfer Capacitance	C_{rss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	N-Ch	-	109	136	
		V_{GS} = 0 V	V_{DS} = - 20 V, f = 1 MHz	P-Ch	-	208	260	
Total Gate Charge[c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 10 A	N-Ch	-	31.5	48	nC
		V_{GS} = - 10 V	V_{DS} = - 20 V, I_D = - 10 A	P-Ch	-	41.5	63	
Gate-Source Charge[c]	Q_{gs}	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 10 A	N-Ch	-	5.7	-	
		V_{GS} = - 10 V	V_{DS} = - 20 V, I_D = - 10 A	P-Ch	-	5.5	-	
Gate-Drain Charge[c]	Q_{gd}	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 10 A	N-Ch	-	4.8	-	
		V_{GS} = - 10 V	V_{DS} = - 20 V, I_D = - 10 A	P-Ch	-	10.5	-	
Gate Resistance	R_g	f = 1 MHz		N-Ch	2	4.11	6.2	Ω
				P-Ch	3.1	6.3	9.5	

Notes

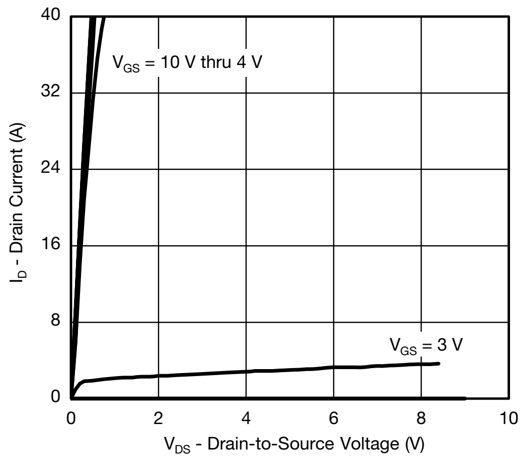
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	7	11	ns
		V_{DD} = - 20 V, R_L = 2 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω	P-Ch	-	11	17	
Rise Time[c]	t_r	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	21	32	
		V_{DD} = - 20 V, R_L = 2 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω	P-Ch	-	9	14	
Turn-Off Delay Time[c]	$t_{d(off)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	33	50	
		V_{DD} = - 20 V, R_L = 2 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω	P-Ch	-	55	83	
Fall Time[c]	t_f	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch	-	19	29	
		V_{DD} = - 20 V, R_L = 2 Ω $I_D \cong$ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω	P-Ch	-	91	137	
Source-Drain Diode Ratings and Characteristics[b]							
Pulsed Current[a]	I_{SM}		N-Ch	-	-	32	A
			P-Ch	-	-	- 32	
Forward Voltage	V_{SD}	I_S = 4 A	N-Ch	-	0.79	1.2	V
		I_S = - 4 A	P-Ch	-	- 0.82	- 1.2	

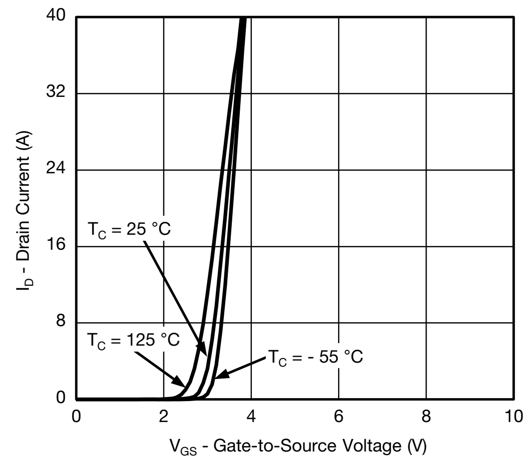
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

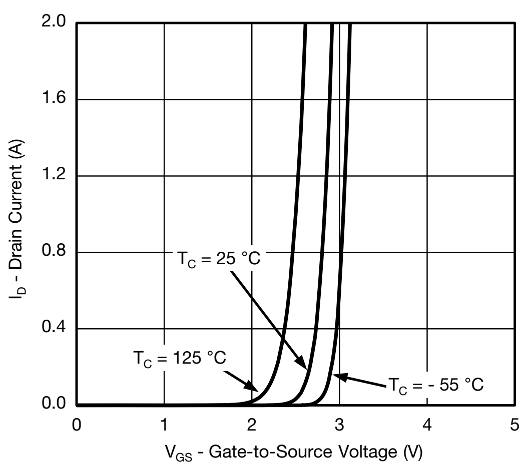
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



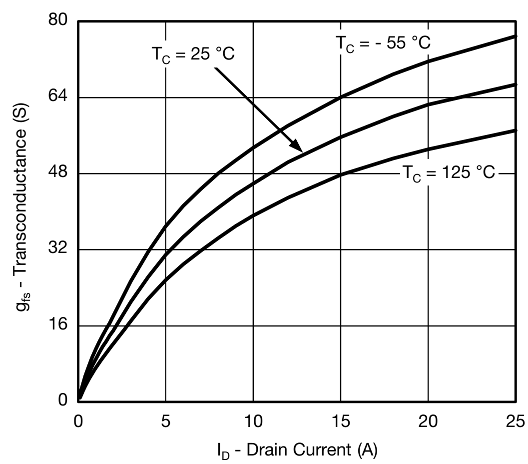
Output Characteristics



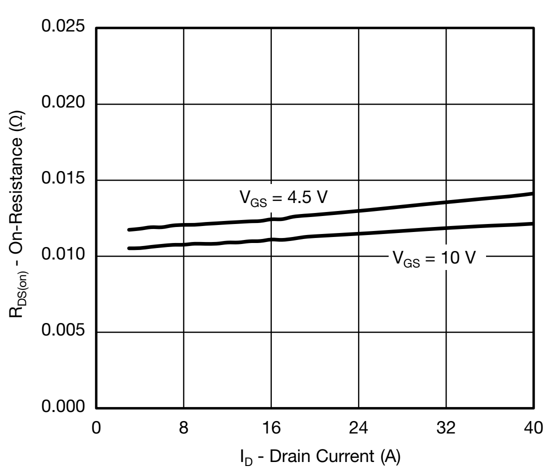
Transfer Characteristics



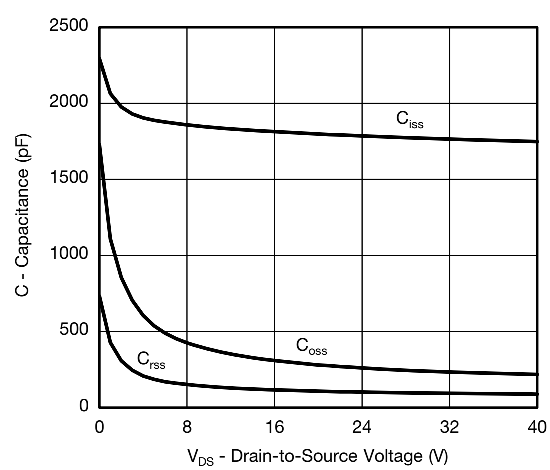
Transfer Characteristics



Transconductance

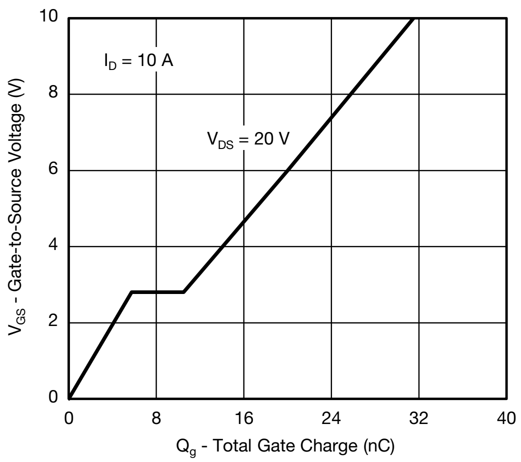


On-Resistance vs. Drain Current

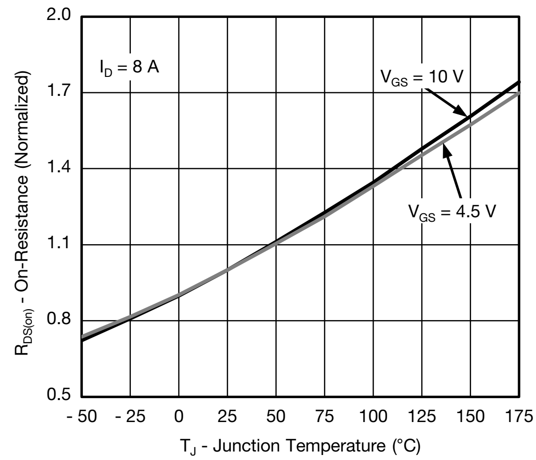


Capacitance

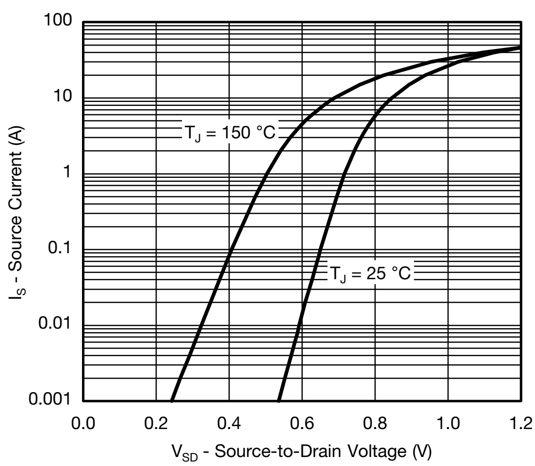
N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



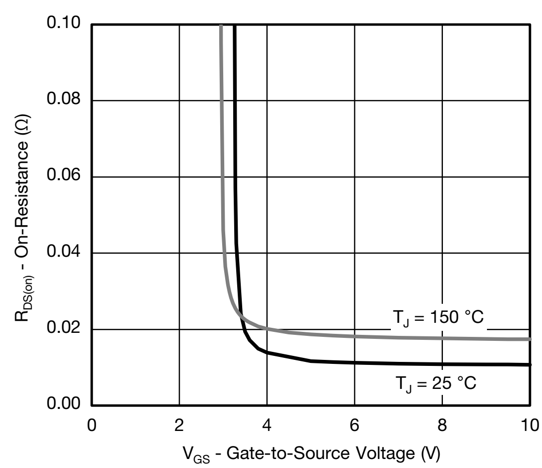
Gate Charge



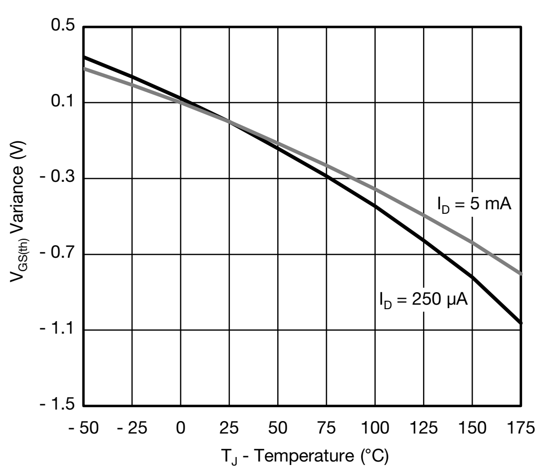
On-Resistance vs. Junction Temperature



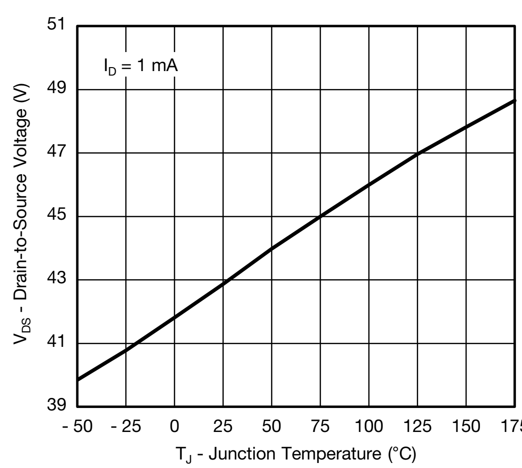
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

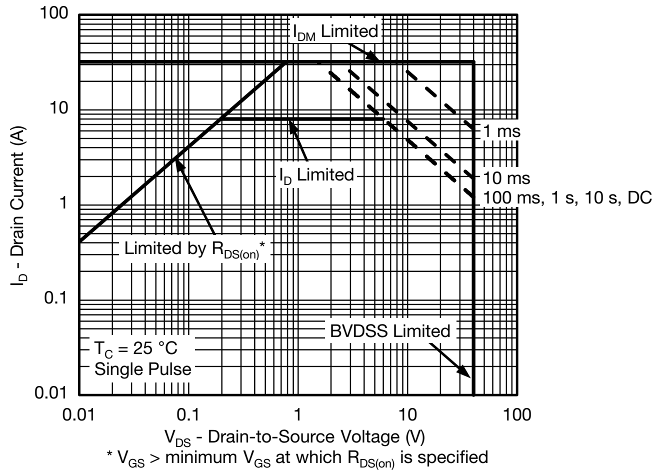


Threshold Voltage

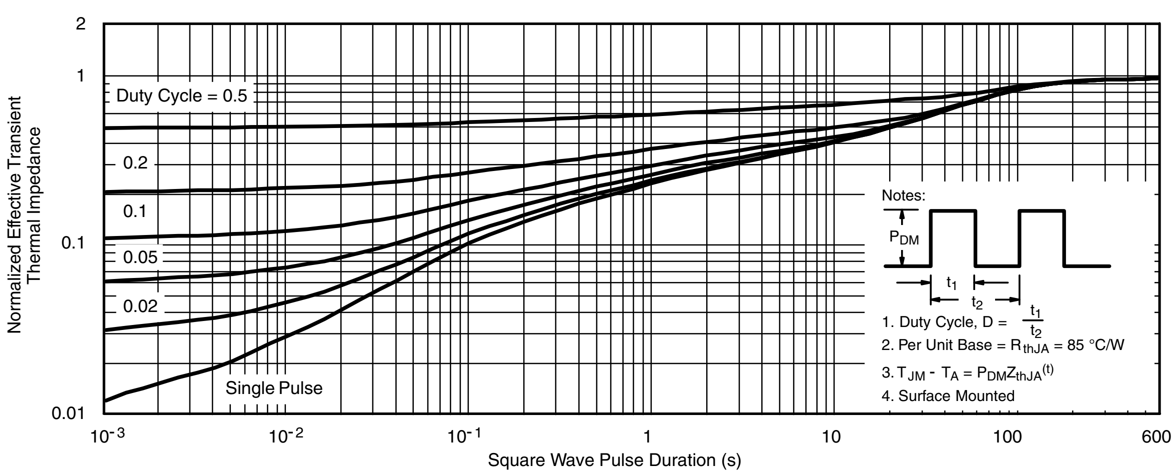


Drain Source Breakdown vs. Junction Temperature

N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

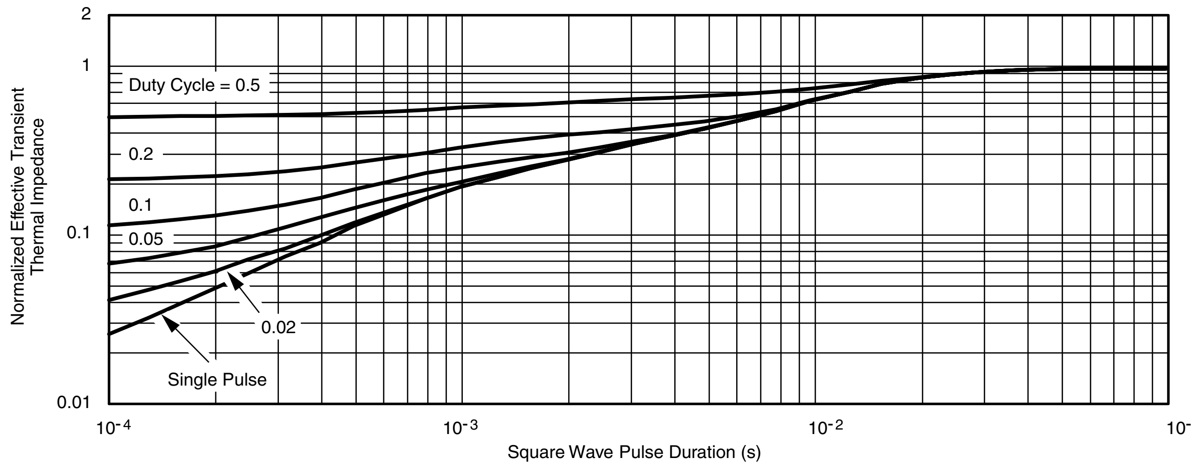


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



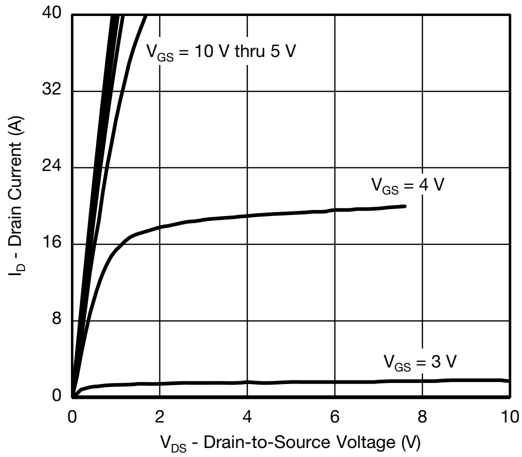
Normalized Thermal Transient Impedance, Junction-to-Case

Note

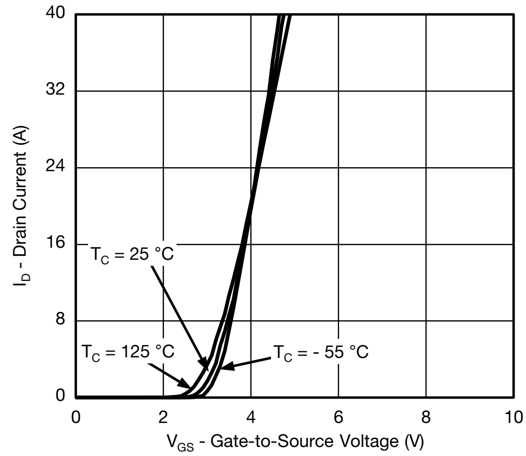
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

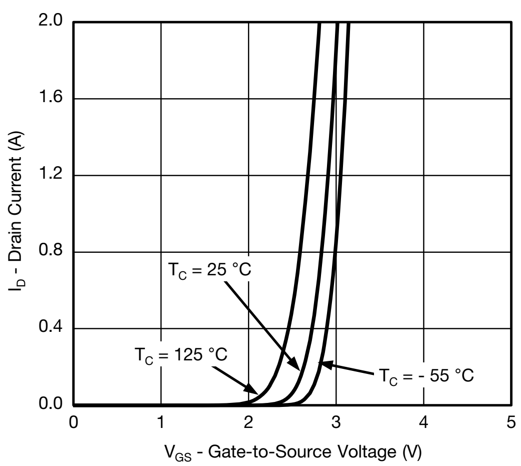
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



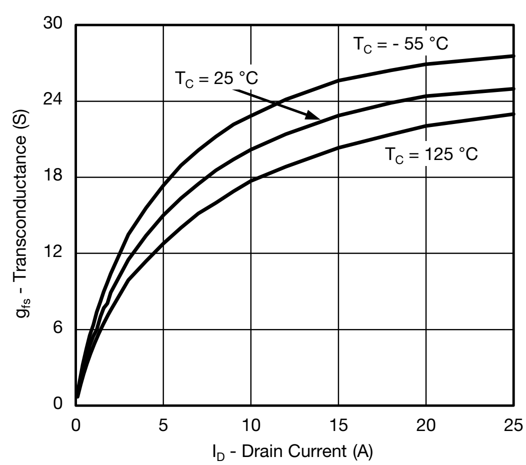
Output Characteristics



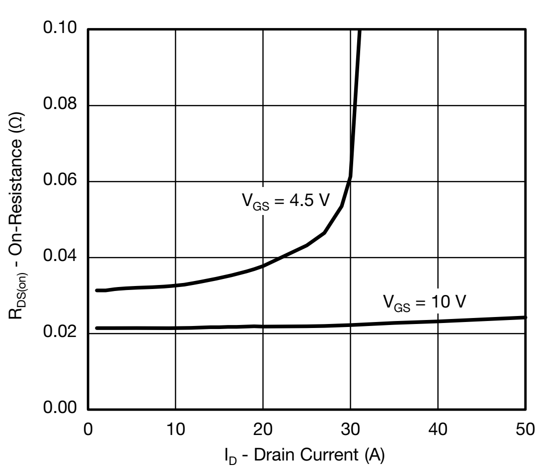
Transfer Characteristics



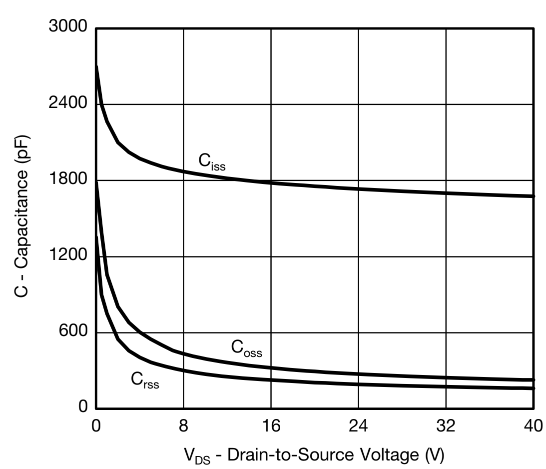
Transfer Characteristics



Transconductance



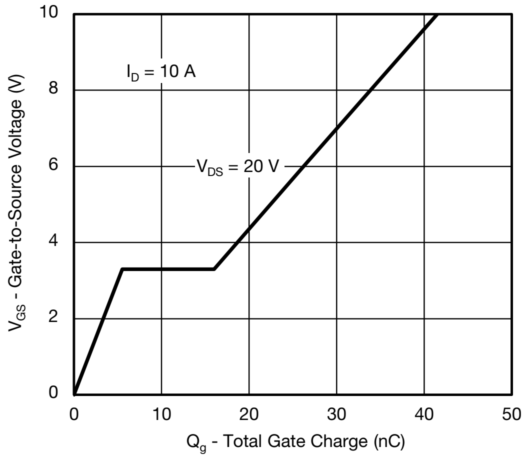
On-Resistance vs. Drain Current



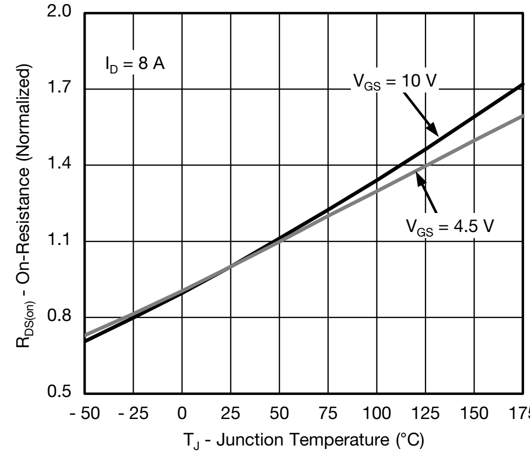
Capacitance

For technical questions, contact: automostechsupport@vishay.com

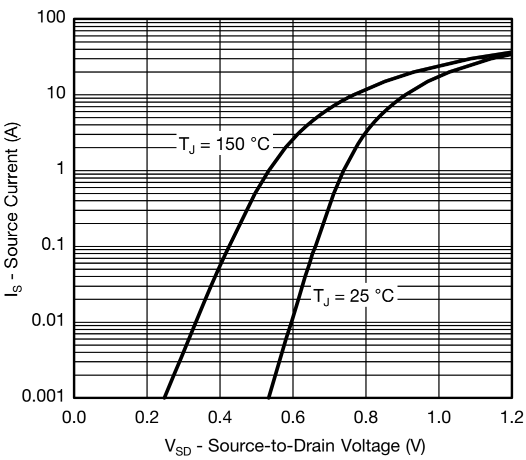
P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



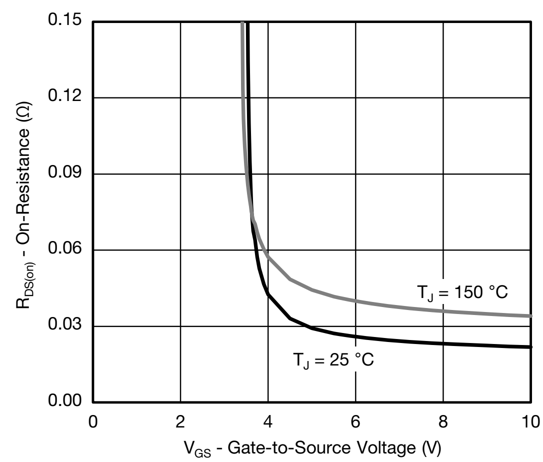
Gate Charge



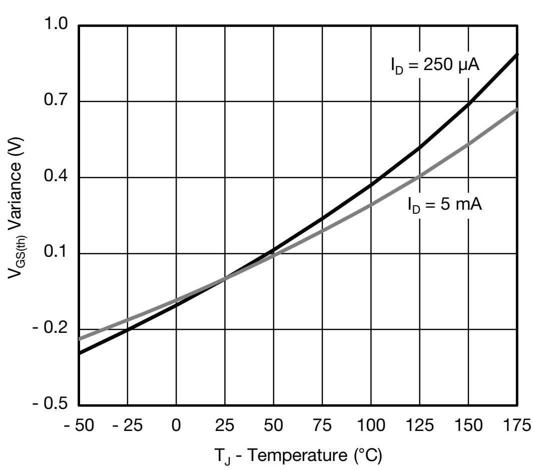
On-Resistance vs. Junction Temperature



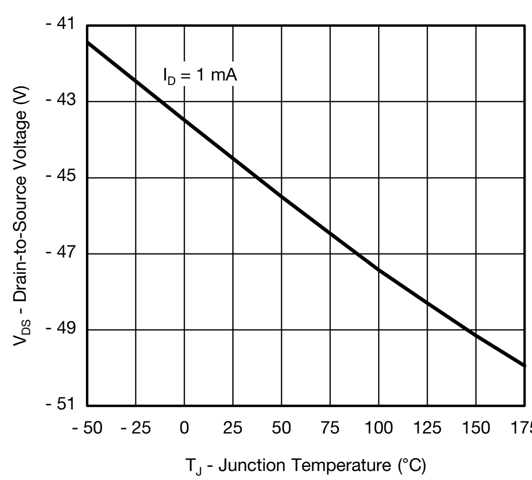
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

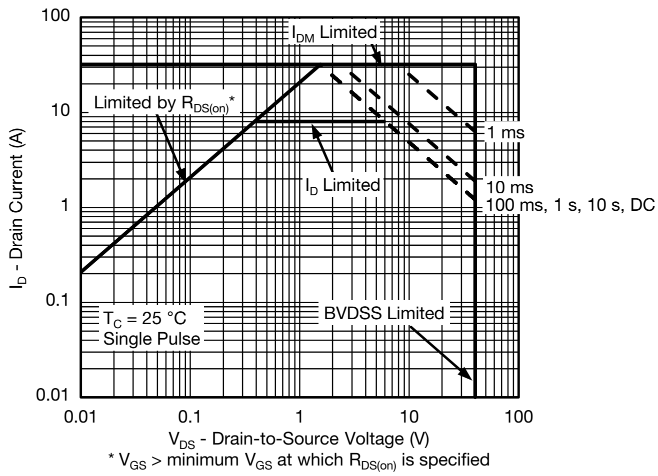


Threshold Voltage

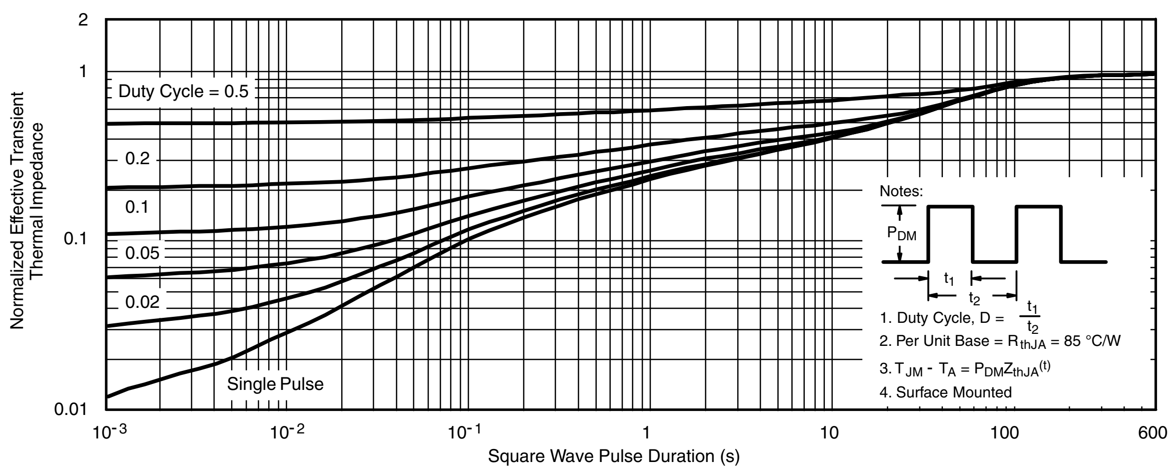


Drain Source Breakdown vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

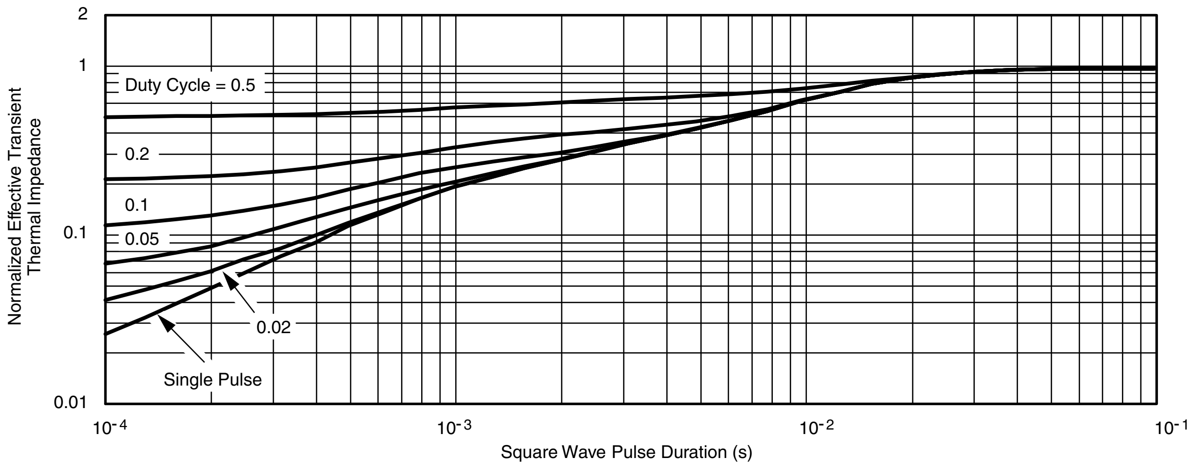


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

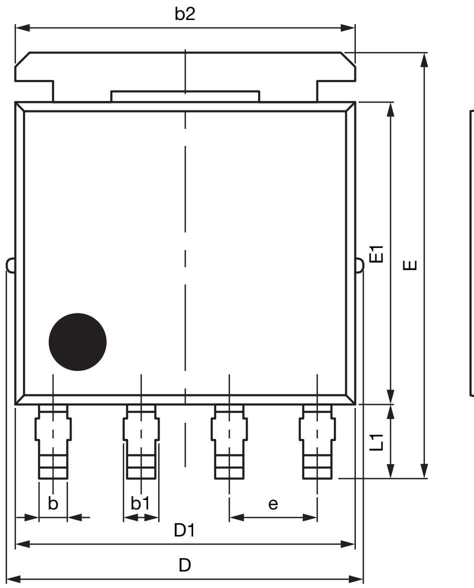
Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

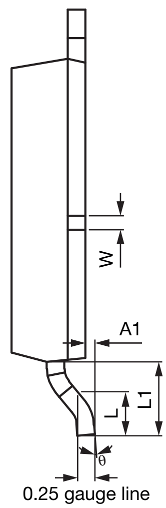
  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

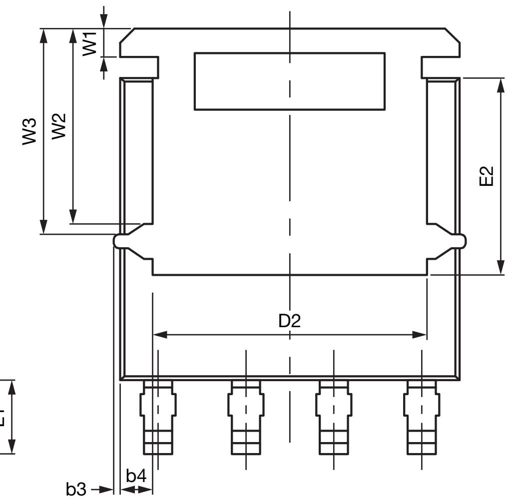
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67517.

PowerPAK® SO-8L Case Outline 2

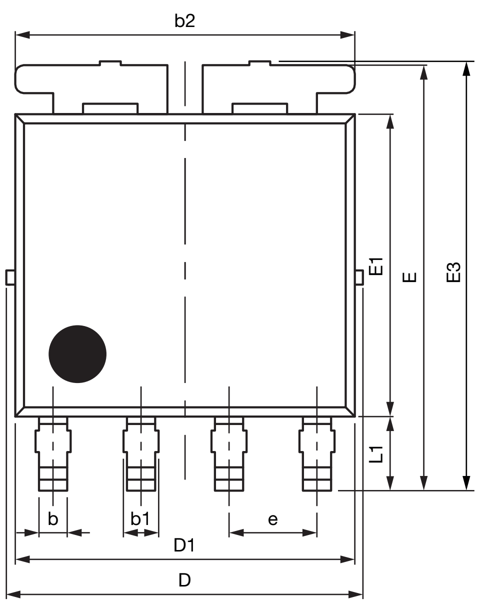


Topside view (single)

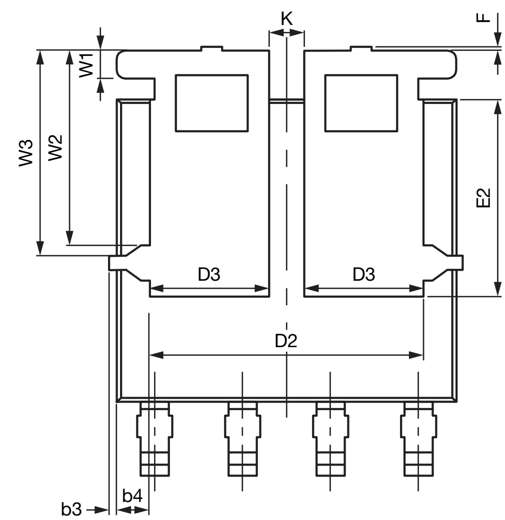




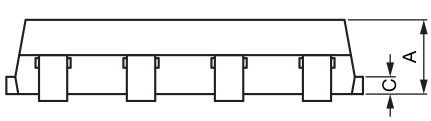
Backside view (single)



Topside view (dual)



Backside view (dual)

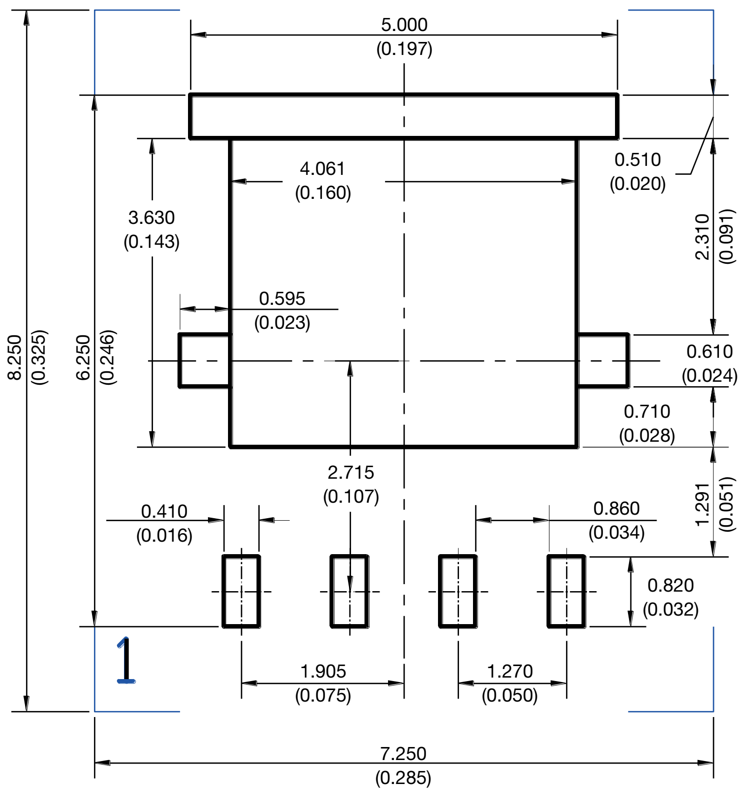


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094			0.004	
b4		0.47			0.019	
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e		1.27 BSC			0.050 BSC	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	6.05	6.22	6.40	0.238	0.245	0.252
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K		0.51			0.020	
W		0.23			0.009	
W1		0.41			0.016	
W2		2.82			0.111	
W3		2.96			0.117	
θ	0°	-	10°	0°	-	10°
ECN: C23-1026-Rev. D, 25-Sep-2023 DWG: 6044						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads
Dimensions in mm (inches)

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