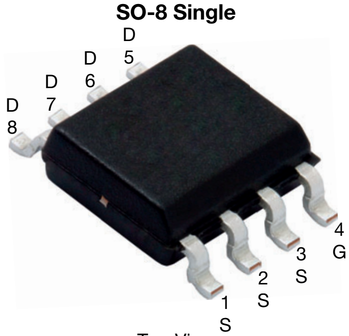
P-Channel 2.5 V (G-S) MOSFET

SO-8 Single



Top View

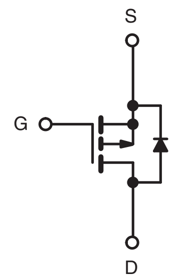
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Adaptor switch
- High current load switch
- Notebook



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0080
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0100
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.0140
Q_g typ. (nC)	54
I_D (A) [d]	-18.6
Configuration	Single

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	Si4463CDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	-18.6	A
	T_C = 70 °C		-15	
	T_A = 25 °C		-13.6 [a, b]	
	T_A = 70 °C		-10.8 [a, b]	
Pulsed drain current		I_{DM}	-60	
Continuous source-drain diode current	T_C = 25 °C	I_S	-4.5	
	T_A = 25 °C		-2.4 [a, b]	
Avalanche current	L = 0.1 mH	I_{AS}	-20	
Single-pulse avalanche energy		E_{AS}	20	mJ
Maximum power dissipation	T_C = 25 °C	P_D	5	W
	T_C = 70 °C		3.2	
	T_A = 25 °C		2.7 [a, b]	
	T_A = 70 °C		1.7 [a, b]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a, c]	t ≤ 10 s	R_{thJA}	38	46	°C/W
Maximum junction-to-foot	Steady state	R_{thJF}	20	25	

Notes
a. Surface mounted on 1" x 1" FR4 board
b. t = 10 s
c. Maximum under steady state conditions is 85 °C/W
d. Based on T_C = 25 °C

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-12	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	3.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.6	-	-1.4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	-	-	-1	µA
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 70 °C	-	-	-10	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \geq$ -10 V, V_{GS} = -10 V	-30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -13 A	-	0.0060	0.0080	Ω
		V_{GS} = 4.5 V, I_D = -12 A	-	0.0073	0.0100	
		V_{GS} = -2.5 V, I_D = -5 A	-	0.0110	0.0140	
Forward transconductance [a]	g_{fs}	V_{DS} = -10 V, I_D = -13 A	-	60	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	-	4250	-	pF
Output capacitance	C_{oss}		-	840	-	
Reverse transfer capacitance	C_{rss}		-	830	-	
Total gate charge	Q_g	V_{DS} = -10 V, V_{GS} = -10 V, I_D = -10 A	-	108	162	nC
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -10 A	-	54	81	
Gate-source charge	Q_{gs}		-	7.8	-	
Gate-drain charge	Q_{gd}		-	18.5	-	
Gate resistance	R_g	f = 1 MHz	0.5	2.3	4.6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 2 Ω $I_D \cong$ -5 A, V_{GEN} = -10 V, R_g = 1 Ω	-	12	24	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	70	120	
Fall time	t_f		-	11	22	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 2 Ω $I_D \cong$ -5 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	34	65	
Rise time	t_r		-	35	65	
Turn-off delay time	$t_{d(off)}$		-	70	120	
Fall time	t_f		-	30	60	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	-4.5	A
Pulse diode forward current	I_{SM}		-	-	-60	
Body diode voltage	V_{SD}	I_S = -3 A, V_{GS} = 0 V	-	-0.7	-1.1	V
Body diode reverse recovery time	t_{rr}	I_F = -2.3 A, di/dt = 100 A/µs, T_J = 25 °C	-	54	100	ns
Body diode reverse recovery charge	Q_{rr}		-	60	120	nC
Reverse recovery fall time	t_a		-	26	-	ns
Reverse recovery rise time	t_b		-	28	-	

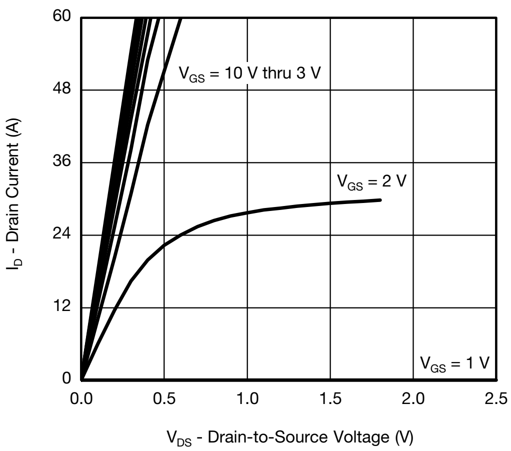
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%

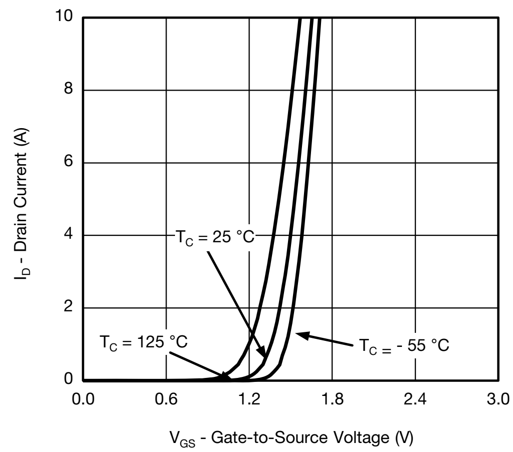
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

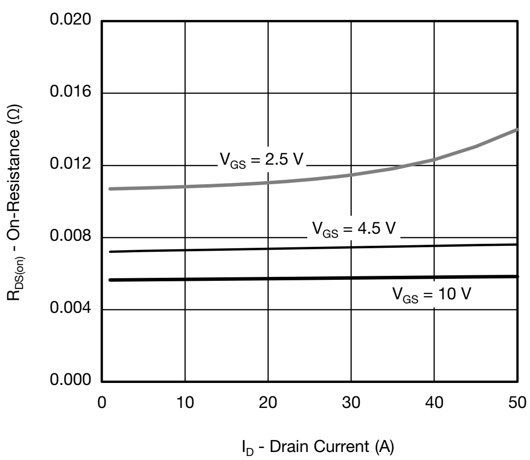
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



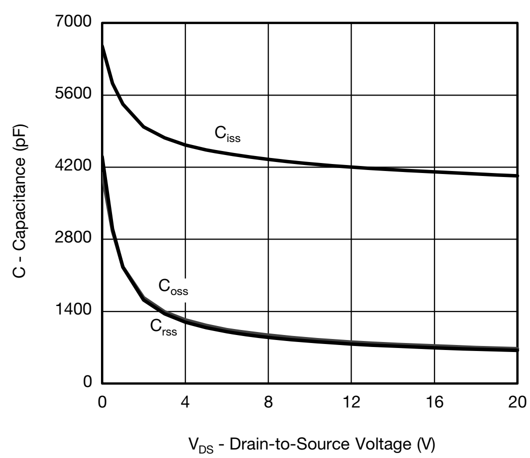
Output Characteristics



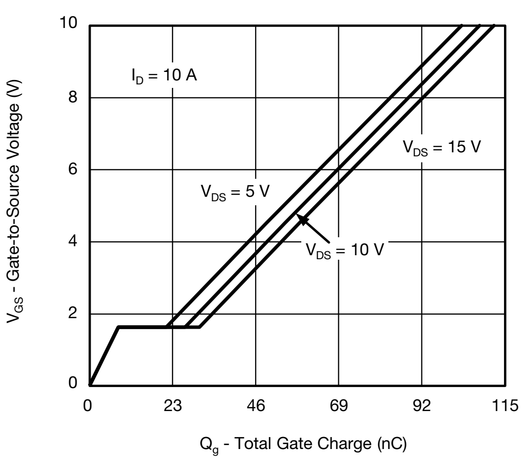
Transfer Characteristics



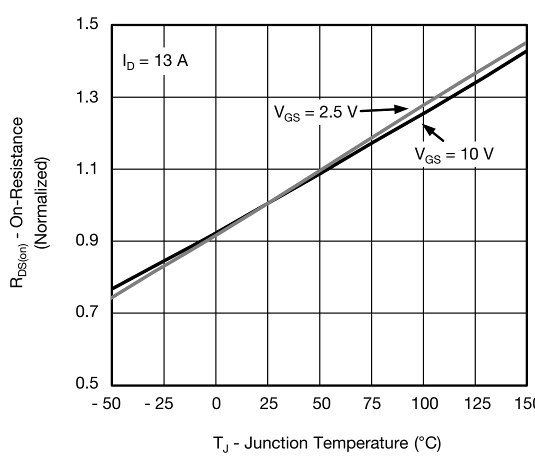
On-Resistance vs. Drain Current



Capacitance

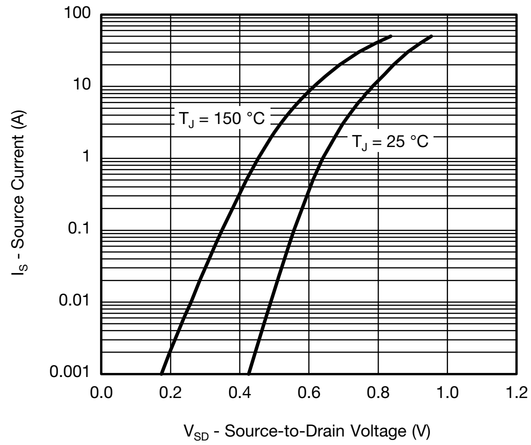


Gate Charge

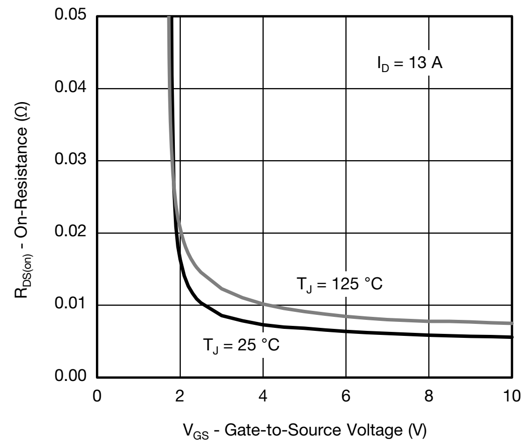


On-Resistance vs. Junction Temperature

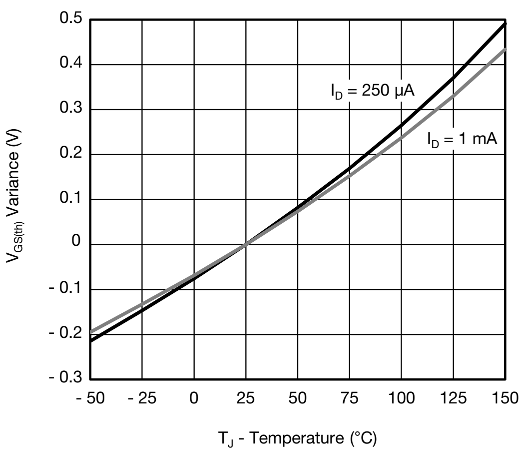
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



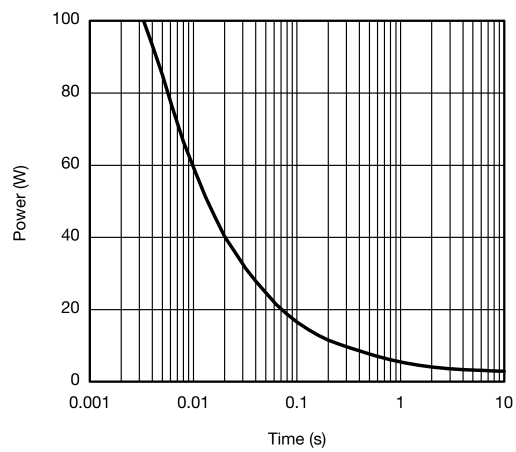
Source-Drain Diode Forward Voltage



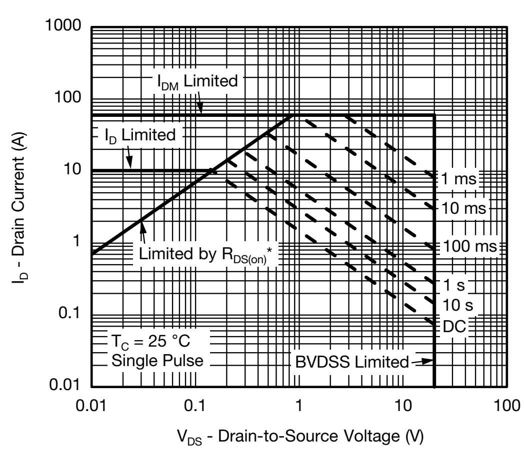
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



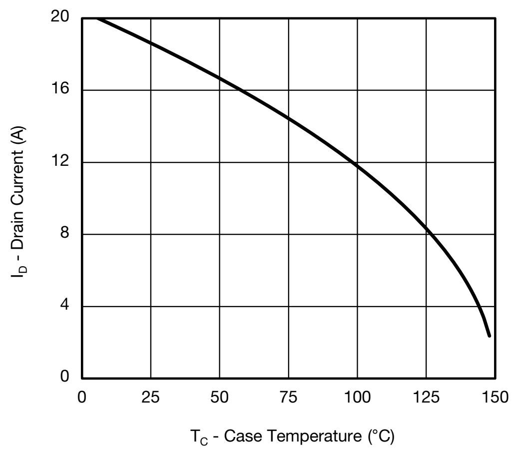
Single Pulse Power, Junction-to-Ambient



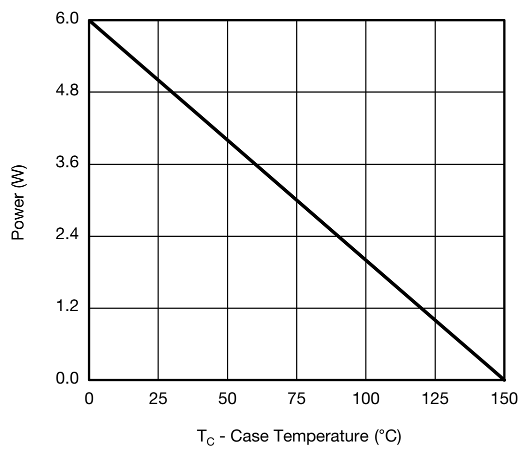
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

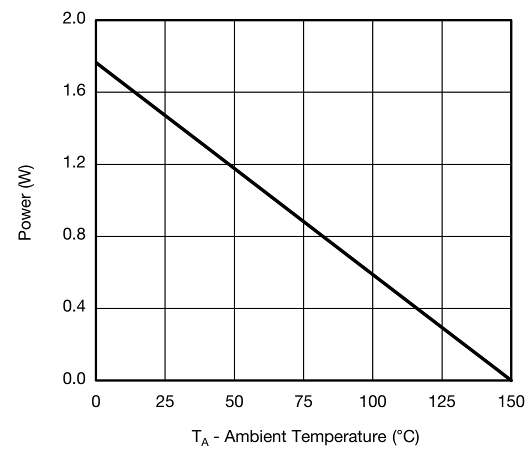
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power Derating, Junction-to-Foot

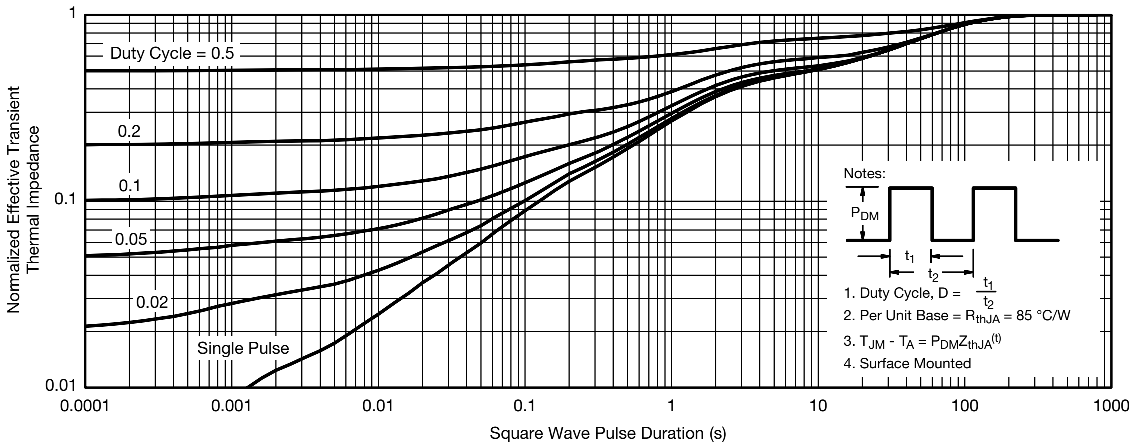


Power Derating, Junction-to-Ambient

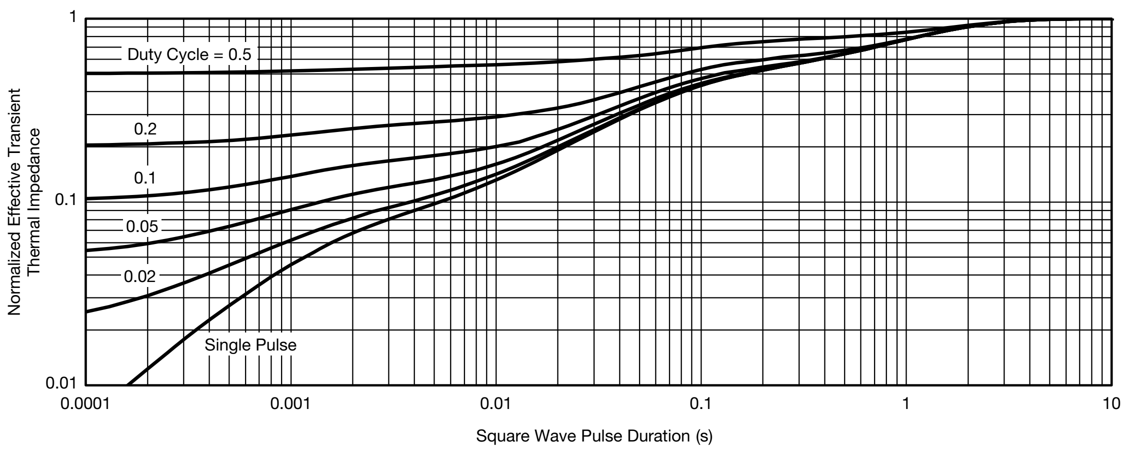
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



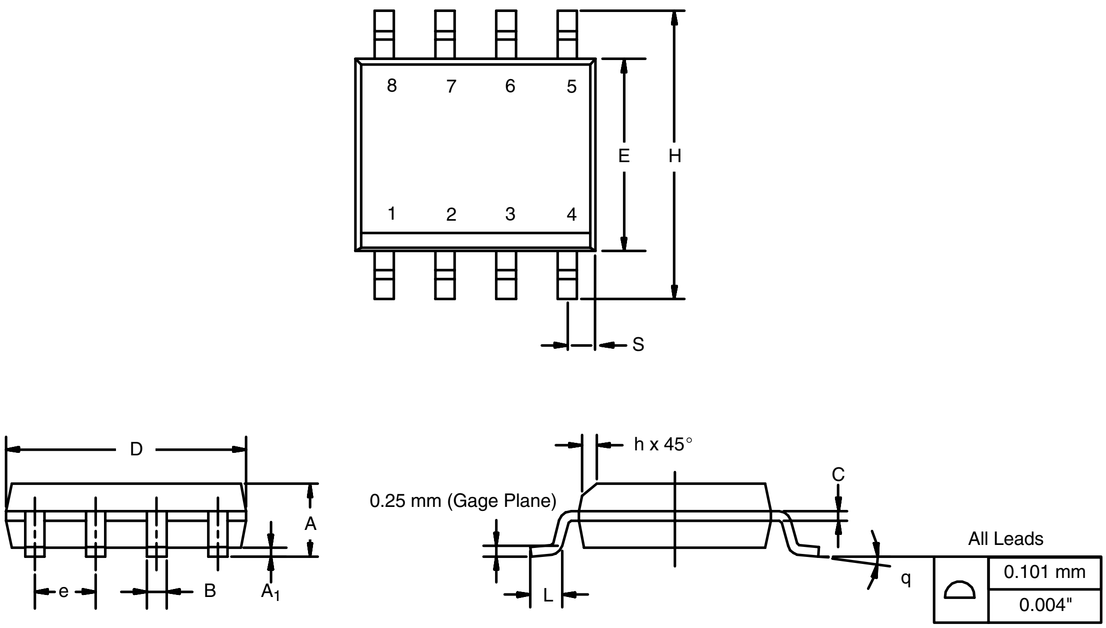
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

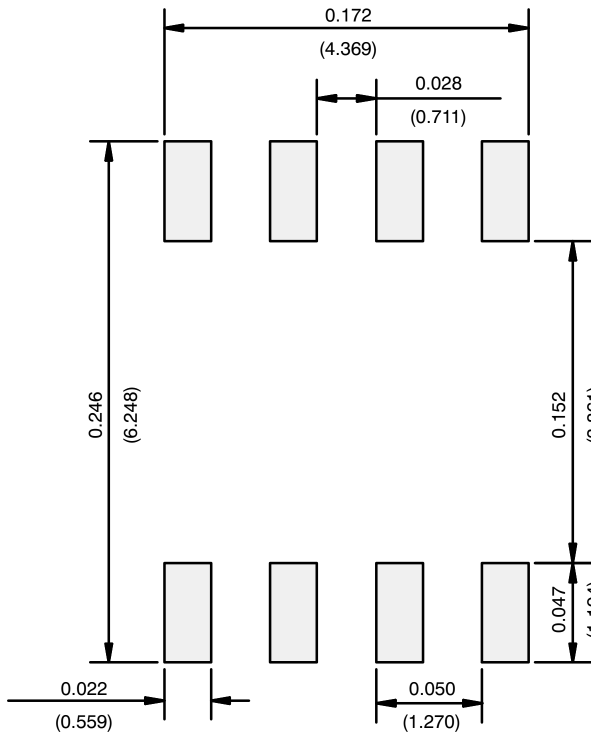
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67335.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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