High Temperature (245 °C) Thick Film Chip Resistor

FEATURES

- High temperature (245 °C)
- Large ohmic value range 0.1 Ω to 100 MΩ
- Operating temperature range (-55 °C to +230 °C)
- SMD wraparound chip resistor
- Storage temperature range (-55 °C to +245 °C)
- Gold terminations for HMP process (< 1 µm thick) for temperature up to 245 °C
- Tin / silver terminations for operating temperature up to 200 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS COMPLIANT

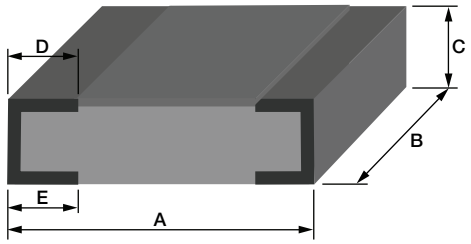
HALOGEN FREE

LINKS TO ADDITIONAL RESOURCES

3D Models

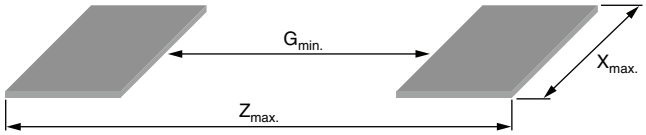
For applications such as down hole applications or aircraft breaking systems, the need for parts able to withstand very severe conditions (temperature as high as 230 °C powered or up to 245 °C un-powered) has leaded Vishay Sfernice to push out the limit of the thick film technology. Designers might read the application note “Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chips Resistors and Arrays (P, PRA etc.) (High Temperature Applications)” (www.vishay.com/doc?53047) in conjunction with this datasheet to help them to properly design their PCBs and get the best performances of the CHPHT. Vishay Sfernice R&D engineers will be willing to support any customer design considerations.

DIMENSIONS in millimeters



CASE SIZE	A	B	C	D	E
	± 0.152	± 0.127	± 0.127	± 0.127	± 0.127
0603	1.60	0.90	0.38	0.31	0.40
0805	1.85	1.25	0.38	0.31	0.50
1206	3.00	1.73	0.38	0.40	0.50
2010	5.03	2.64	0.50	0.50	0.50

SUGGESTED LAND PATTERN (to IPC-7351A)



CASE SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0603	2.15	0.39	1.03
0805	2.70	0.44	1.38
1206	3.85	1.59	1.85
2010	5.88	3.62	2.77

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER P_n W (at 230 °C)	LIMITING ELEMENT VOLTAGE V	MAX. OVERLOAD VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
CHPHT	0603	0.1 to 25M	0.0125	50	100	1, 2, 5	100, 200
CHPHT	0805	0.1 to 25M	0.02	150	300	1, 2, 5	100, 200
CHPHT	1206	0.1 to 50M	0.025	200	400	1, 2, 5	100, 200
CHPHT	2010	0.1 to 100M	0.1	200	400	1, 2, 5	100, 200

CLIMATIC SPECIFICATIONS

Operating temperature range	-55 °C to +230 °C
Storage temperature range	-55 °C to +245 °C

MECHANICAL SPECIFICATIONS

Substrate	Alumina
Technology	Thick film (Ruthenium oxyde)
Protection	0.5 Ω < R < 100 MΩ: double organic coating R ≤ 0.5 Ω: overglaze protection (no organic coating)
Terminations	**N (W/A):** SnAg over nickel barrier for temperature up to 200 °C **G (W/A) type:** gold (< 1 µm) over nickel barrier for temperature up to 245 °C

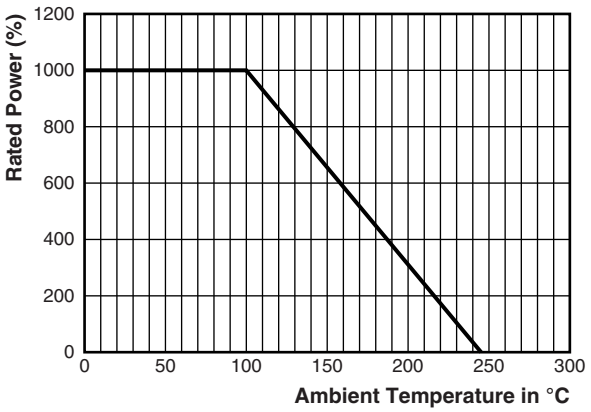
Note

- Refer to Application Note "Guidelines for Vishay Sfernice Resistive and Inductive Components" (document number: 52029) for recommended reflow profile. Profile #3 applies

BEST TOL. AND TCR VERSUS OHMIC VALUE

OHMIC VALUE RANGE (Ω)	TIGHTEST TOLERANCE (%)	BEST TCR (ppm/°C)
5 ≤ R ≤ 10M	1 (F)	100 (K)
1 ≤ R ≤ $R_{max.}$	2 (G)	200 (L)
0.5 ≤ R ≤ $R_{max.}$	5 (J)	200 (L)
0.1 ≤ R ≤ $R_{max.}$	5 (J)	300 (M)

POWER DERATING CURVE



PACKAGING

ESD packaging available: Waffle pack and plastic tape and reel (low conductivity). Paper tapes available on request (ESD only). (For 0603, 0805, and 1206 only.)

SIZE	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
	WAFFLE PACK	TAPE AND REEL		
		MIN.	MAX.	
0603	100	100	5000	8 mm
0805			4000	
1206	140			
2010	60		2000	12 mm

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover. **To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code**

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided. **When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code**

POPULAR OPTIONS

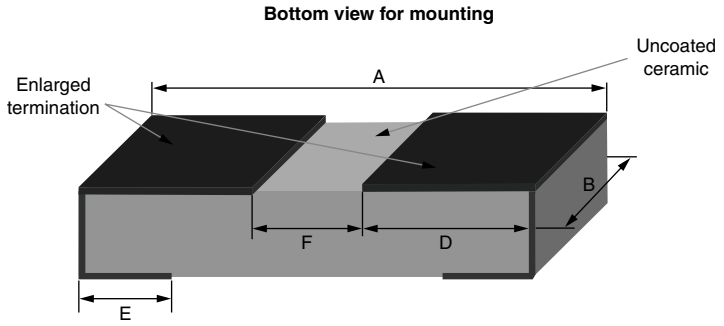
For any option it is recommended to consult Vishay Sfernice for availability first.

Option: Enlarged terminations:

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heat sinks (see application note: “Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film” (www.vishay.com/doc?53048).

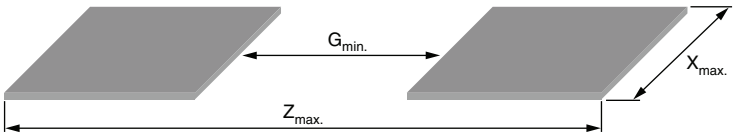
Option to order: 0063 (applies to size 1206/2010).

DIMENSIONS (Option 0063) in millimeters



CASE SIZE	A	B	E	D	F		
	MAX. TOL. +0.152 MIN. TOL. -0.152	MAX. TOL. +0.127 MIN. TOL. -0.127	MAX. TOL. +0.13 MIN. TOL. -0.13	MAX. TOL. +0.13 MIN. TOL. -0.13			
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06 (0.120)	1.60 (0.063)	0.40 (0.016)	1.22 (0.048)	0.63 (0.024)	0.50 (0.020)	0.76 (0.030)
2010	5.08 (0.200)	2.54 (0.100)	0.48 (0.019)	2.23 (0.088)	0.63 (0.024)	0.50 (0.020)	0.76 (0.030)

SUGGESTED LAND PATTERN (Option 0063)



CHIP SIZE	DIMENSIONS (in millimeters)		
	$Z_{max.}$	$G_{min.}$	$X_{max.}$
1206	3.91 (0.154)	0.50 (0.020)	1.73 (0.068)
2010	5.93 (0.233)	0.50 (0.020)	2.67 (0.105)

PERFORMANCE

TESTS	CONDITIONS	REQUIREMENTS	TYPICAL VALUES AND DRIFTS
Termination adhesion	5N for 10 s	± (0.25 % + 0.05 Ω)	< ± 0.1 %
Resistance to solder heat	Immersion 10 s in Sn/Pb 60/40 at +260 °C	± (0.25 % + 0.05 Ω)	< ± 0.1 %
Rapid temperature change	5 cycles -55 °C to +155 °C	± (0.25 % + 0.05 Ω)	< ± 0.1 %
Climatic sequence	Phase A dry heat Phase B damp heat Phase C cold -55 °C Phase D damp heat 5 cycles	± (1 % + 0.05 Ω)	< ± 0.2 %
Humidity (steady state)	56 days	± (1 % + 0.05 Ω)	< ± 0.2 %
Moisture resistance	AEC-Q200 85 °C / 85 % RH / P_n 1000 h	3 % + 0.05 Ω	Max. < 3 % + 0.05 Ω
Short time overload	6.25 P_n for 2 s	± (0.25 % + 0.05 Ω)	< ± 0.1 %
Load life	1000 h at rated power at 230 °C	-	1 % max.
Shelf life	1000 h at 245 °C	-	1 % max.

GLOBAL PART NUMBER INFORMATION

Global Part Numbering: CHPHT0805K1001FGT

C	H	P	H	T	0	8	0	5	K	1	0	0	1	F	G	T	

GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION (1)	PACKAGING	OPTION
CHPHT	**0603** **0805** **1206** **2010**	**K** = 100 ppm **L** = 200 ppm **M** = 300 ppm	The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ	**F** = ± 1 % **G** = ± 2 % **J** = ± 5 %	**N**: SnAg over nickel barrier **G**: gold over nickel barrier	For more information see “Codification of Packaging” table	Leave blank if no option

Note

(1) N terminations for temperature up to 200 °C
G terminations for temperature up to 230 °C

CODIFICATION OF PACKAGING	
WAFFLE PACK	
W	100 min., 1 mult.
WA	100 min., 100 mult. (available only in size 1206)
PLASTIC TAPE (Standard for all sizes)	
T	100 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)
PAPER TAPE (Available for 0603, 0805, and 1206. Please consult Vishay Sfernice for other sizes)	
PT	100 min., 1 mult.
PA	100 min., 100 mult.
PB	250 min., 250 mult.
PC	500 min., 500 mult.
PD	1000 min., 1000 mult.
PE	2500 min., 2500 mult.
PF	Full tape (quantity depending on size of chips)

CODIFICATION OF OPTIONS ON TWO DIGITS			
OPTION	**OPTION 2 DIGITS**	**OPTION**	**OPTION 2 DIGITS**
..	..	0126	1A
0099	99	0127	1B
0100	0A	0128	1C
0101	0B	..	..
0102	0C	0320	8M
0103	0D	0321	8N
0104	0E	0322	8O
0105	0F	0323	8P
..	..	0324	8Q
0124	0Y	0325	8R
0125	0Z	..	..

CODIFICATION OF SIZES			
CODE 18	**CODE 40**	**CODE 18**	**CODE 40**
7	02016	M	22
8	0302	N	33
9	0402	O	44
A	0502	P	55
B	0505	Q	515
C	0603	R	48
D	0805	S	408
E	1005	T	816
F	1010	U	914
G	1020	V	073
H	1206	W	074
I	1505	X	100
J	2010	Y	135
K	2208	Z	182
L	2512		

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