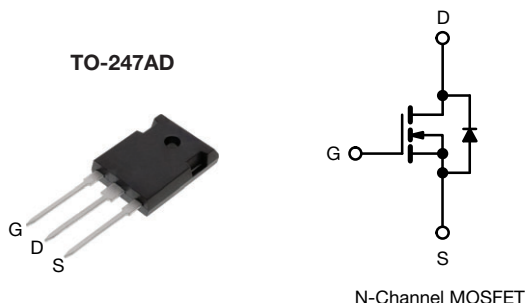


E Series Power MOSFET With Fast Body Diode



FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.063
Q_g typ. (nC)	177	
Q_{gs} (nC)	46	
Q_{gd} (nC)	68	
Configuration	Single	

APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter

ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and halogen-free	SQW44N65EF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	146	
Linear derating factor		3.3	W/°C
Single pulse avalanche energy ^b	E_{AS}	596	mJ
Maximum power dissipation	P_D	500	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	V/ns
Reverse diode dv/dt ^d			
Soldering recommendations (peak temperature) ^c	for 10 s	260	°C


Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 6.5$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 145$ A/ μ s, starting $T_J = 25$ °C

THERMAL RESISTANCE RATINGS

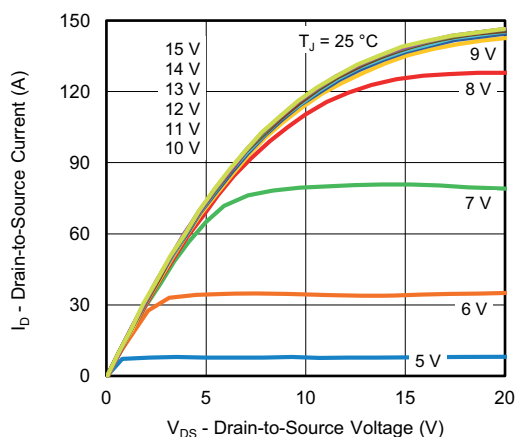
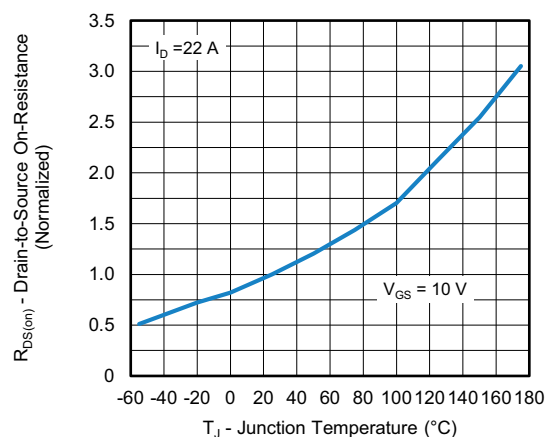
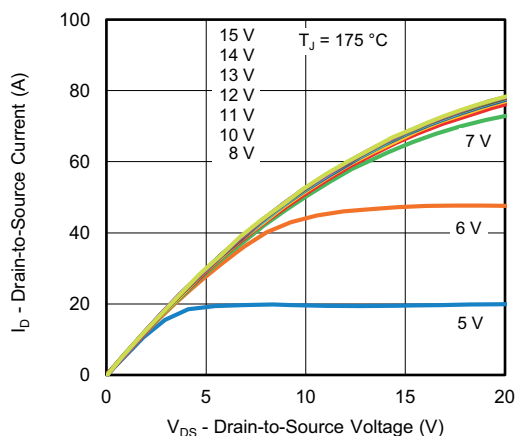
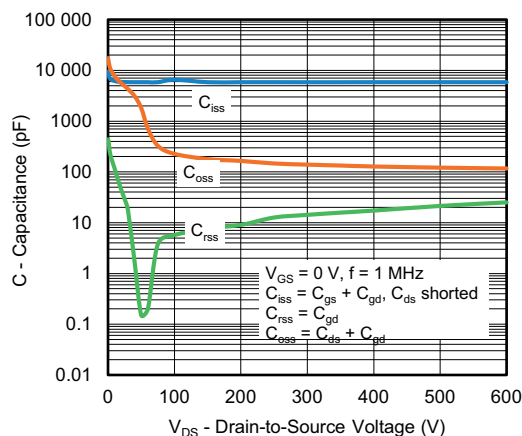
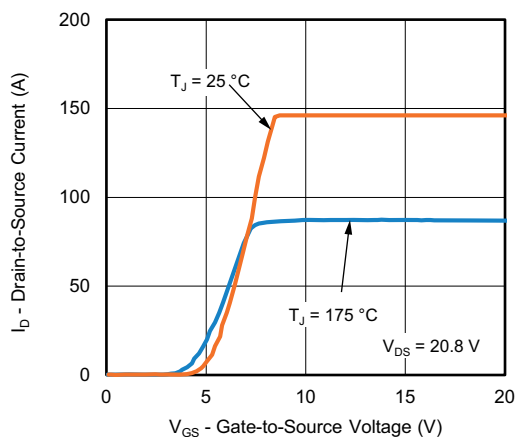
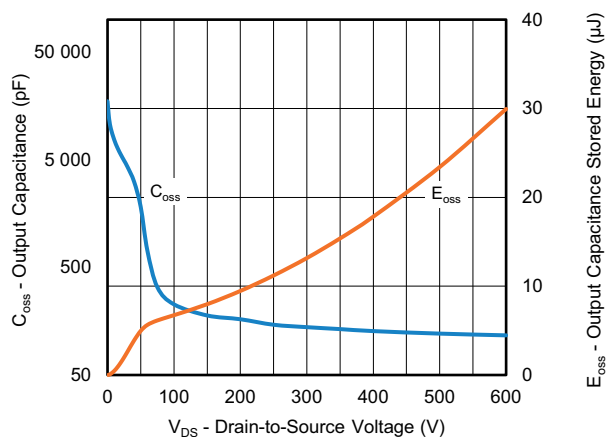
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.3	

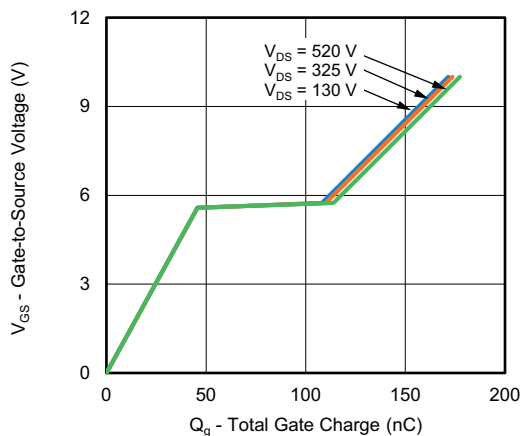
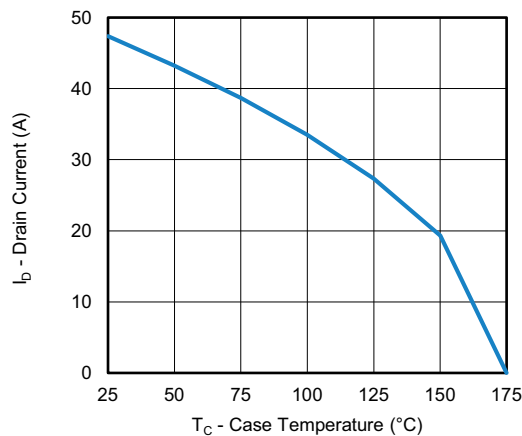
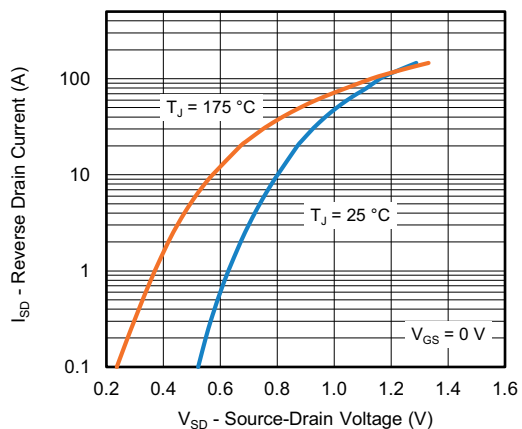
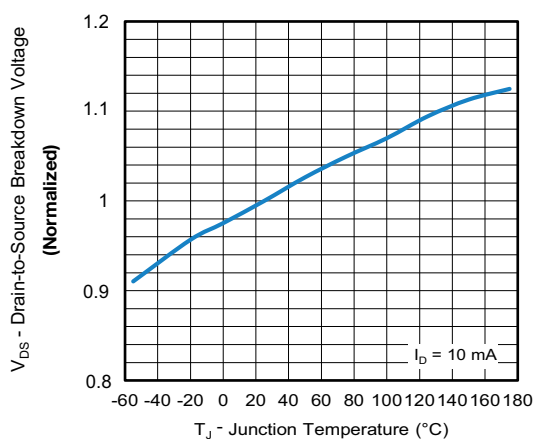
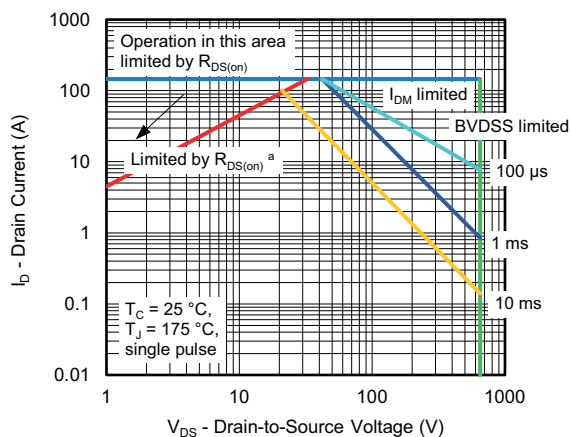


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	650	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 10 mA	-	0.7	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
		V _{GS} = ± 30 V	-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 520 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C	-	-	500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 22 A	-	0.063	0.073	Ω
Forward transconductance ^a	g _{fs}	V _{DS} = 30 V, I _D = 22 A	-	18	-	S
Dynamic						
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	5858	-	pF
Output capacitance	C _{oss}		-	227	-	
Reverse transfer capacitance	C _{rss}		-	6	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 V to 520 V	-	173	-	
Effective output capacitance, time related ^b	C _{o(tr)}		-	710	-	
Total gate charge	Q _g	V _{GS} = 10 V, I _D = 22 A, V _{DS} = 520 V	-	177	266	nC
Gate-source charge	Q _{gs}		-	46	-	
Gate-drain charge	Q _{gd}		-	68	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 520 V, I _D = 22 A R _g = 9.1 Ω, V _{GS} = 10 V	-	47	94	ns
Rise time	t _r		-	71	142	
Turn-off delay time	t _{d(off)}		-	206	412	
Fall time	t _f		-	66	132	
Gate input resistance	R _g	f = 1 MHz, open drain	0.5	1.0	2.0	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	47	A
Pulsed diode forward current	I _{SM}		-	-	146	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 22 A, V _{GS} = 0 V	-	0.9	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S = 22 A, di/dt = 100 A/μs, V _R = 400 V	-	190	380	ns
Reverse recovery charge	Q _{rr}		-	1.7	3.4	μC
Reverse recovery current	I _{RRM}		-	17	-	A

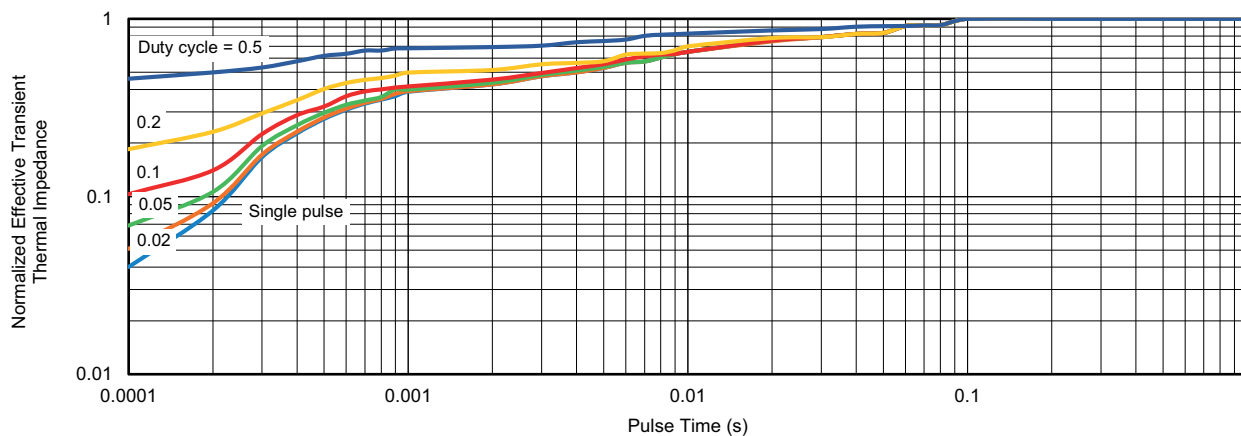
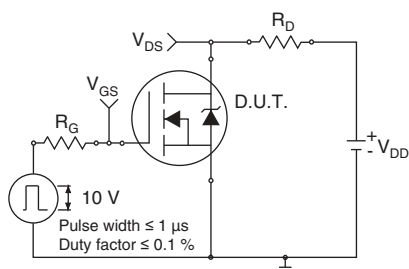
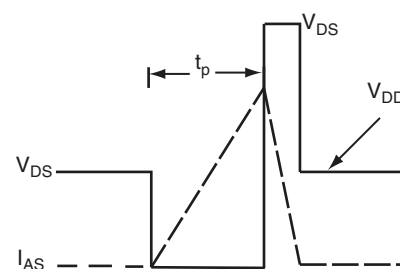
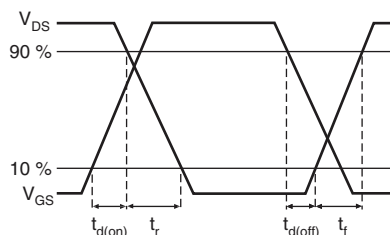
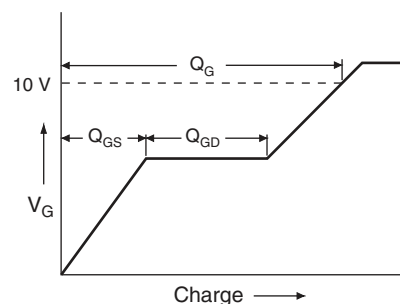
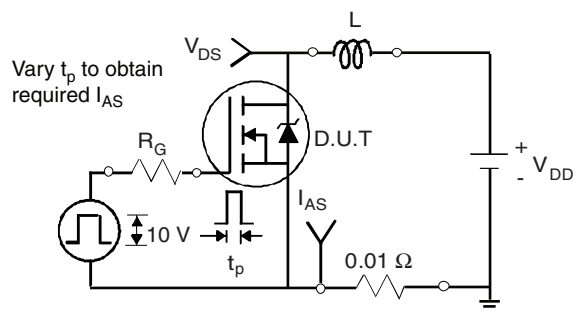
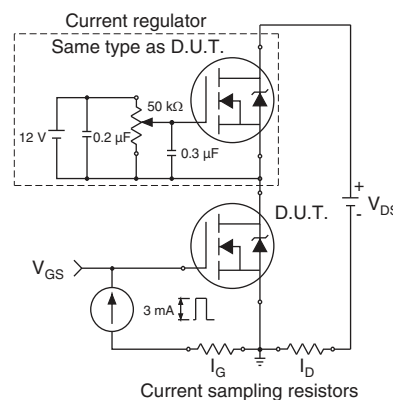
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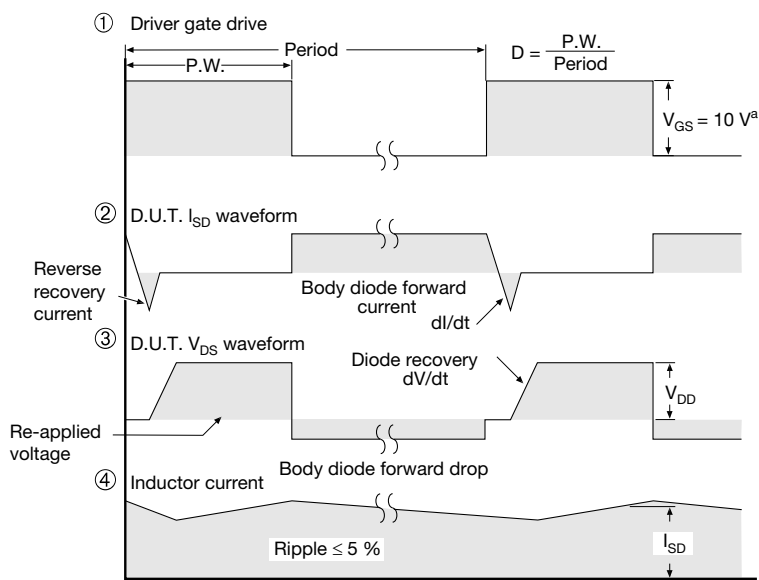
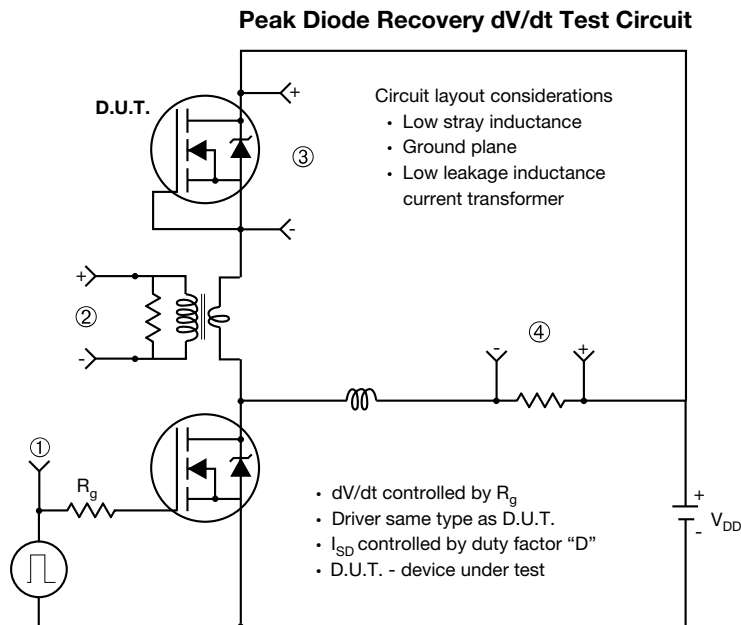
- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
b. C_{oss(tr)} is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

Fig. 9 - Maximum Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

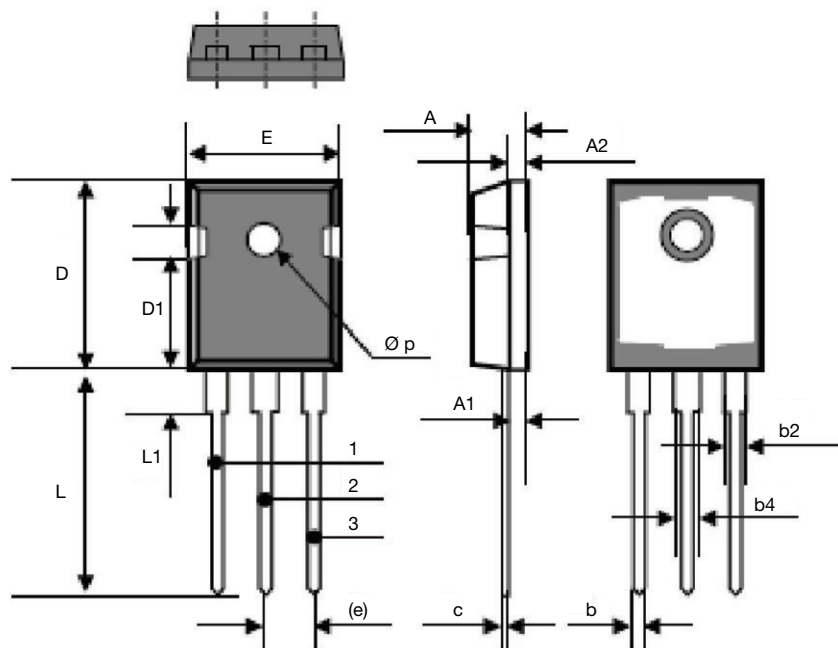

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 19 - For N-Channel

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TO-247AD (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.31	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.41	0.065	0.095
b4	2.59	3.43	0.102	0.135
c	0.61 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	3.68	5.49	0.145	0.216
(e)	5.46 BSC		0.215 BSC	
E	15.49	16.26	0.610	0.640
L	19.81	20.32	0.780	0.800
L1	4.06	4.50	0.160	0.177
$\varnothing p$	3.51	3.66	0.138	0.144
ECN: S17-0178-Rev. B, 06-Feb-17 DWG: 6010				



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