

Thyristor/Diode (Super MAGN-A-PAK Power Modules), 570 A



Super MAGN-A-PAK

PRIMARY CHARACTERISTICS				
I _{T(AV)}	570 A			
Туре	Modules - thyristor/diode			
Package	Super MAGN-A-PAK			

FEATURES

- · High current capability
- High surge capability
- · Industrial standard package
- 3000 V_{RMS} isolating voltage with non-toxic substrate
- · Designed and qualified for industrial level
- UL approved file E78996
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

TYPICAL APPLICATIONS

- Motor starters
- DC motor controls AC motor controls
- Uninterruptible power supplies

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL	CHARACTERISTICS	VALUES	UNITS			
I _{T(AV)} , I _{F(AV)}	T _C = 85 °C	570				
I _{T(RMS)}	T _C = 85 °C	894	Α			
1	50 Hz	18 000	A			
ITSM	60 Hz	18 800				
l ² t	50 Hz	1620	kA ² s			
1-1	60 Hz	1473	KA-S			
I ² √t		16 200	kA ^{2√} s			
V _{DRM} /V _{RRM}		1600	V			
T _{Stg}	Range	-40 to +125	°C			
T _J	Range	-40 to +135	U			

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V _{RRM} /V _{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} MAXIMUM AT T _J = T _J MAXIMUM mA			
VS-VSKH570-16PbF	16	1600	1700	110			



ON-STATE CONDUCTION						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum average on-state current	I _{T(AV)} ,	1000			570	Α
at case temperature	I _{F(AV)}	180° conduction	180° conduction, half sine wave		85	°C
Maximum RMS on-state current	I _{T(RMS)}	180° conduction	n, half sine wave	at T _C = 85 °C	894	Α
		t = 10 ms	No voltage		18.0	
Maximum peak, one-cycle,	I _{TSM.}	t = 8.3 ms	reapplied		18.8	1.0
non-repetitive on-state surge current	I _{FSM}	t = 10 ms	100 % V _{RRM}	<u>-</u>	15.1	- kA -
		t = 8.3 ms	reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	15.8	
Maximum I ² t for fusing		t = 10 ms			1620	- kA ² s
	l ² t	t = 8.3 ms			1473	
		t = 10 ms	100 % V _{RRM}	<u>-</u>	1146	
		t = 8.3 ms	reapplied		1042	
Maximum I ² √t for fusing	I²√t	t = 0.1 ms to 10 ms, no voltage reapplied		16 200	kA²√s	
Low level value or threshold voltage	V _{T(TO)1}	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), $T_J = T_J$ maximum		0.59	V	
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(AV)}), T_{J}$	_J = T _J maximum		0.63	v
Low level value on-state slope resistance	r _{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum		0.41	mΩ	
High level value on-state slope resistance	r _{t2}	r_{t2} $(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		0.38	11122	
SCR Maximum on state valters due:	V_{TM}	I_{pk} = 1500 A, T_J = 25 °C, t_p = 10 ms sine pulse		1.06	.,	
Maximum on-state voltage drop Diode	V_{FM}			ms sine puise	1.36	V
Maximum holding current	I _H	T. 05 00 and a self-to-fee		500	A	
Maximum latching current		T _J = 25 °C, anode supply 12 V resistive load		1000	mA	

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum rate of rise of turned-on current	dl/dt	$T_J = T_J$ maximum, $I_{TM} = 400$ A, V_{DRM} applied	1000	A/µs		
Typical delay time	t _d	Gate current 1 A, $dI_g/dt = 1 A/\mu s$ $V_d = 0.67 \% V_{DRM}$, $T_J = 25 °C$	2.0			
Typical turn-off time	t _q	I_{TM} = 750 A; T_J = T_J maximum, dl/dt = - 60 A/μs, V_R = 50 V, dV/dt = 20 V/μs, gate 0 V 100 Ω	65 to 240	μs		

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to $V_D = 80 \% V_{DRM}$	1000	V/µs
RMS insulation voltage	V _{INS}	t = 1 s	3000	V
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	110	mA



TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P _{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms	10	W
Maximum peak average gate power	P _{G(AV)}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0	- vv
Maximum peak positive gate current	+I _{GM}		3.0	Α
Maximum peak positive gate voltage	+V _{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms	20	V
Maximum peak negative gate voltage	-V _{GM}		5.0	V
Maximum DC gate current required to trigger	I _{GT}	T 05 % V 10 V	200	mA
DC gate voltage required to trigger	V_{GT}	T _J = 25 °C, V _{ak} 12 V	3.0	V
DC gate current not to trigger	I _{GD}	$T_J = T_J maximum$	10	mA
DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction operating temperature range	TJ		-40 to +135	°C	
Maximum storage temperature range	T _{Stg}		-40 to +125		
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation	0.06	0.06 0.02	
Maximum thermal resistance, case to heatsink	R _{thC-hs}		0.02		
Mounting Super MAGN-A-PAK to heatsin	k	A mounting compound is recommended and the torque should be rechecked after a period	6 to 8	Nm	
torque ± 10 % busbar to super MAGN-A-PA	K	of 3 hours to allow for the spread of the compound	12 to 15	INIII	
Approximate weight			1500	g	
Case style		See dimensions (link at the end of datasheet)	Super MAGN-	-A-PAK	

△R _{thJC} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS		
180°	0.009	0.006				
120°	0.011	0.011				
90°	0.014	0.015	$T_J = T_J$ maximum	K/W		
60°	0.021	0.022				
30°	0.037	0.038				

Note

Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC



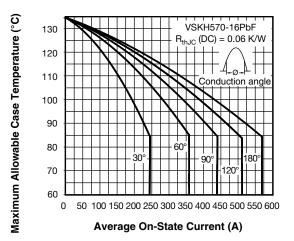


Fig. 1 - Current Ratings Characteristics

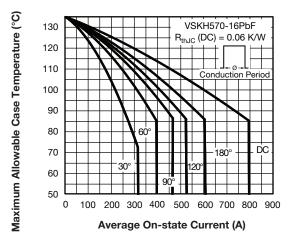


Fig. 2 - Current Ratings Characteristics

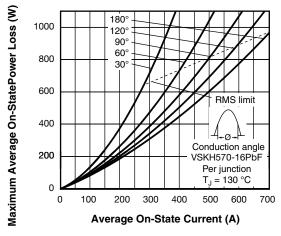


Fig. 3 - On-State Power Loss Characteristics

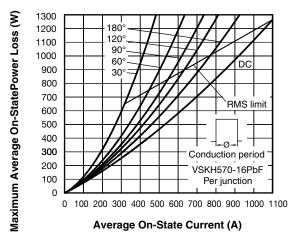


Fig. 4 - On-State Power Loss Characteristics

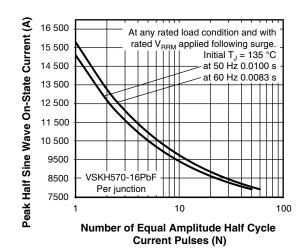


Fig. 5 - Maximum Non-Repetitive Surge Current

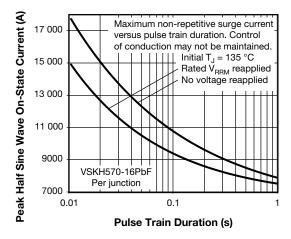
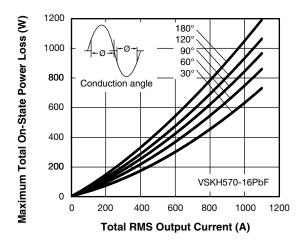


Fig. 6 - Maximum Non-Repetitive Surge Current





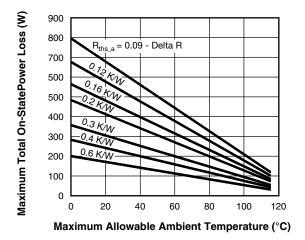


Fig. 7 - On-State Power Loss Characteristics

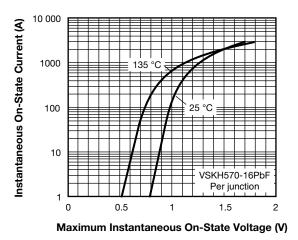


Fig. 8 - On-State Voltage Drop Characteristics

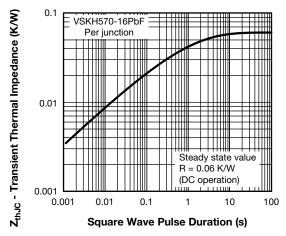
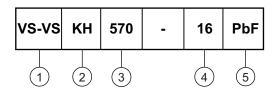


Fig. 9 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

2 - Circuit configuration (see below)

3 - Current rating

Voltage code x 100 = V_{RRM}

5 - Lead (Pb)-free

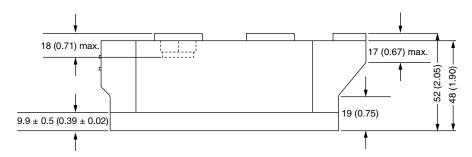
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
SCR/diode doubler circuit	КН	VSKH 1 2 4 (K1) 5 (G1)

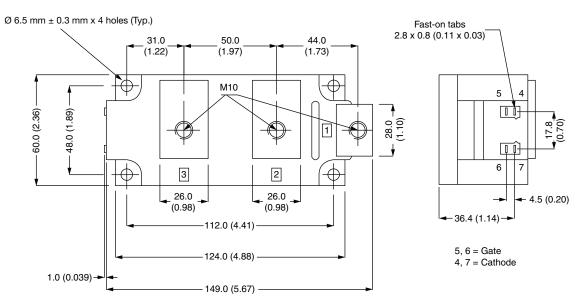
LINKS TO RELAT	TED DOCUMENTS
Dimensions	www.vishay.com/doc?95283



Super MAGN-A-PAK Thyristor/Diode

DIMENSIONS in millimeters (inches)







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