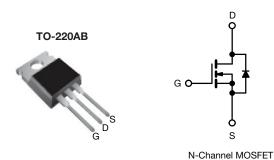


Power MOSFET



PRODUCT SUMMARY			
V _{DS} (V)	200		
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.40	
Q _g max. (nC)	43		
Q _{gs} (nC)	7.0		
Q _{gd} (nC)	23		
Configuration	Single		

FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF630PbF		
Lead (Pb)-free and halogen-free	IRF630PbF-BE3		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	200	V	
Gate-source voltage			V_{GS}	± 20	v	
Continuous drain current	V -+ 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$,	9.0		
	V _{GS} at 10 V	T _C = 100 °C	I _D	5.7	Α	
Pulsed drain current ^a			I _{DM}	36		
Linear derating factor				0.59	W/°C	
Single pulse avalanche energy ^b			E _{AS}	250	mJ	
Repetitive avalanche current a			I _{AR}	9.0	A	
Repetitive avalanche energy ^a			E _{AR}	7.4	mJ	
Maximum power dissipation	T _C =	25 °C	P_{D}	74	W	
Peak diode recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	- °C	
Soldering recommendations (peak temperature) ^d	For 10 s			300	7	
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N·m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 4.6 mH, R_g = 25 Ω , I_{AS} = 9.0 A (see fig. 12)
- c. $I_{SD} \le 9.0$ A, $dI/dt \le 120$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case

S21-0819-Rev. C, 02-Aug-2021



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	1.7		

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		200	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	Reference to 25 °C, I _D = 1 mA		0.24	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}		V _{GS} = ± 20 V		-	± 100	nA
Zoro gata valtaga drain aurrent	1	V _{DS} =	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$		-	25	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 160 V	$V_{\rm S} = 0 \ V_{\rm N} T_{\rm J} = 125 \ ^{\circ}{\rm C}$	-	-	250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5.4 A ^b	-	-	0.40	Ω
Forward transconductance	9 _{fs}	V _{DS}	= 50 V, I _D = 5.4 A	3.8	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	800	-	pF
Output capacitance	C _{oss}		$V_{DS} = 25 \text{ V},$		240	-	
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	76	-	
Total gate charge	Qg		$V_{GS} = 10 \text{ V}$ $I_{D} = 5.9 \text{ A}, V_{DS} = 160 \text{ V},$ see fig. 6 and 13 b	-	-	43	nC
Gate-source charge	Q_{gs}	$V_{GS} = 10 \text{ V}$		-	-	7.0	
Gate-drain charge	Q_{gd}			-	-	23	
Turn-on delay time	t _{d(on)}	V_{DD} = 100 V, I_{D} = 5.9 A, R_{g} = 12 Ω , R_{D} = 16 Ω , see fig. 10 ^b		-	9.4	-	ns ns
Rise time	t _r			-	28	-	
Turn-off delay time	t _{d(off)}			-	39	-	
Fall time	t _f			-	20	-	
Gate input resistance	R_{g}	f = 1 MHz, open drain		0.6	-	3.3	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	الم
Internal source inductance	L _S			-	7.5	-	- nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S		MOSFET symbol showing the		-	9.0	
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	36	- A
Body diode voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 9.0 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	T 05 %			170	340	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 5.9 \text{A}, dI/dt = 100 \text{A}/\mu\text{s}$		-	1.1	2.2	nC
Forward turn-on time	t _{on}	Intrinsic tu	rn-on is dominated by L_S and L_D)			L _D)	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

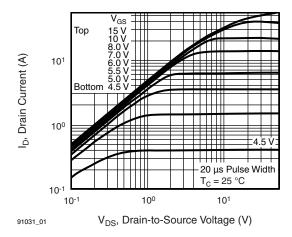


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

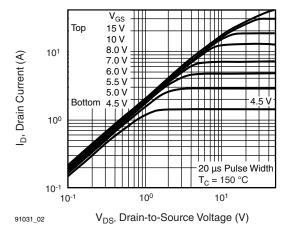


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

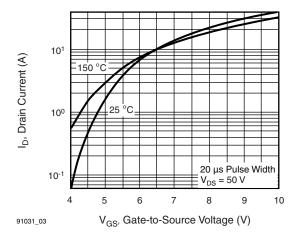


Fig. 3 - Typical Transfer Characteristics

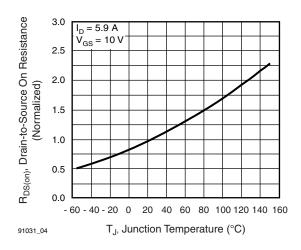


Fig. 4 - Normalized On-Resistance vs. Temperature

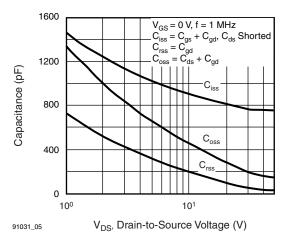


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

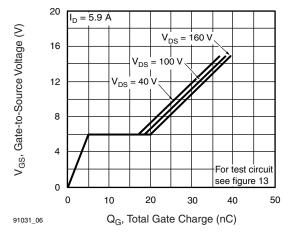


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



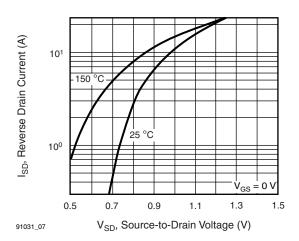


Fig. 7 - Typical Source-Drain Diode Forward Voltage

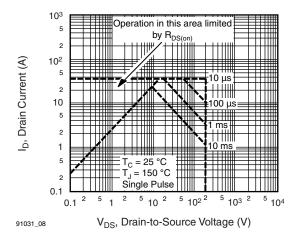


Fig. 8 - Maximum Safe Operating Area

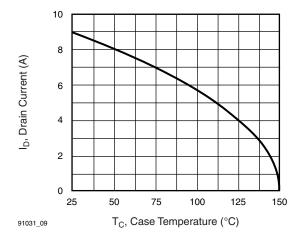


Fig. 9 - Maximum Drain Current vs. Case Temperature

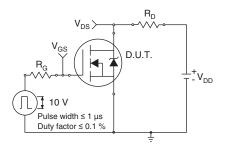


Fig. 10a - Switching Time Test Circuit

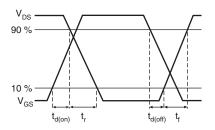


Fig. 10b - Switching Time Waveforms



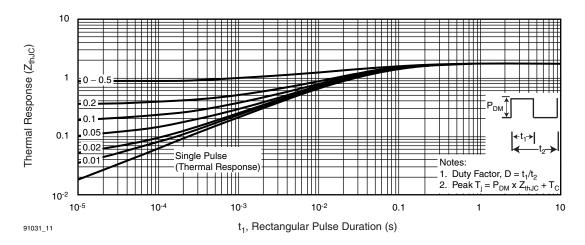


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

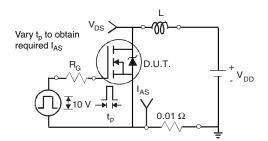


Fig. 12a - Unclamped Inductive Test Circuit

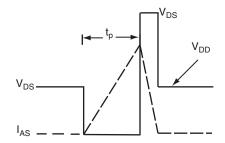


Fig. 12b - Unclamped Inductive Waveforms

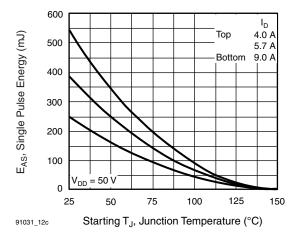
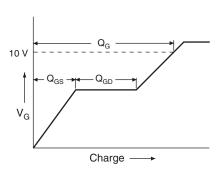


Fig. 12c - Maximum Avalanche Energy vs. Drain Current







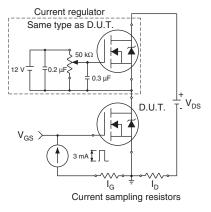
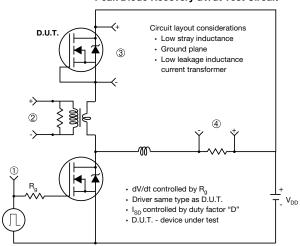


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



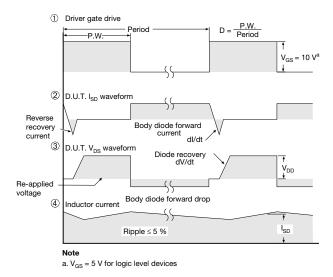


Fig. 14 - For N-Channel

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