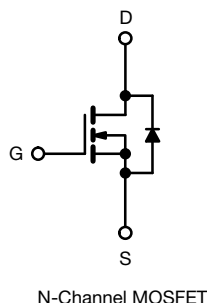
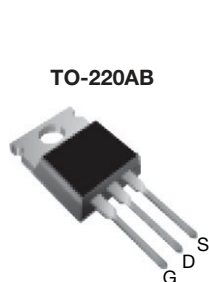


# Power MOSFET



## FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective  $C_{oss}$  specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

## TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half bridge
- Full bridge

## PRODUCT SUMMARY

$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 3.0
$Q_g$ (Max.) (nC)	17
$Q_{gs}$ (nC)	4.3
$Q_{gd}$ (nC)	8.5
Configuration	Single

## ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF820APbF
Lead (Pb)-free and halogen-free	IRF820APbF-BE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current	$I_D$	2.5 1.6	A
Pulsed drain current <sup>a</sup>	$I_{DM}$	10	
Linear derating factor		0.40	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	140	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	2.5	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	5.0	mJ
Maximum power dissipation	$P_D$	50	W
Peak diode recovery $dV/dt$ <sup>c</sup>	$dV/dt$	3.4	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>	
Mounting torque	6-32 or M3 screw	10 1.1	lbf · in N · m


## Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 45\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.5\text{ A}$  (see fig. 12)
- $I_{SD} \leq 2.5\text{ A}$ ,  $dI/dt \leq 270\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

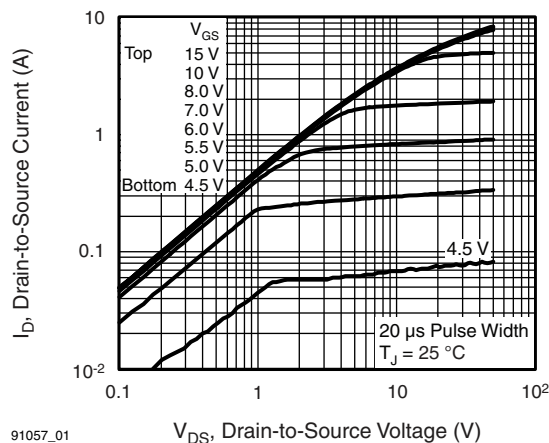
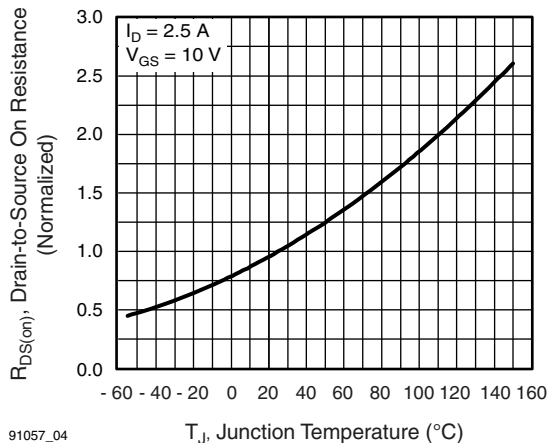
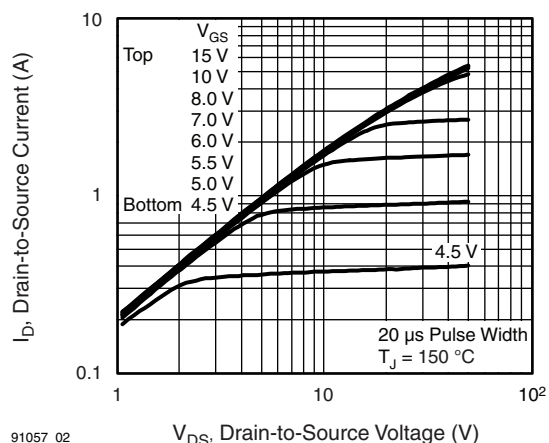
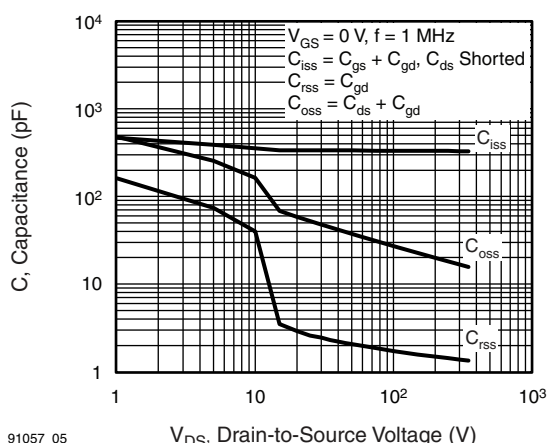
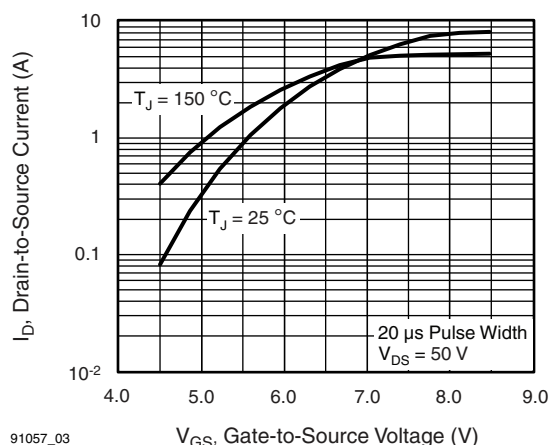
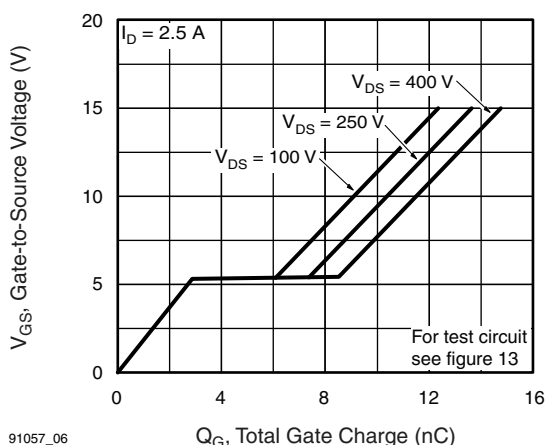
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Case-to-sink, flat, greased surface	$R_{thCS}$	0.50	-	
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.5	

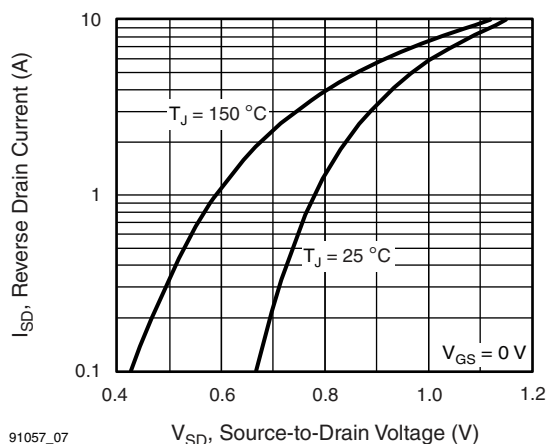
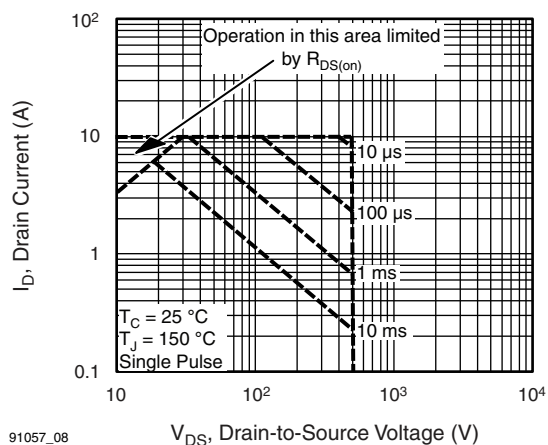
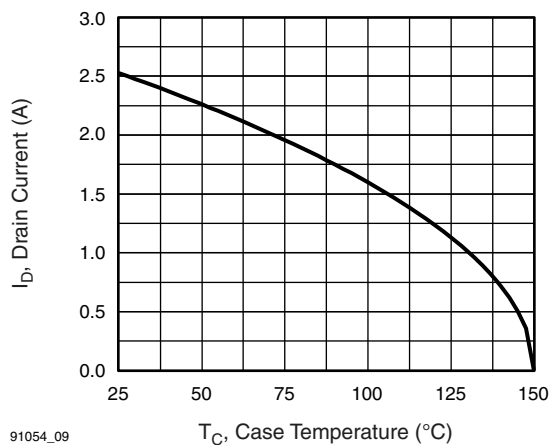
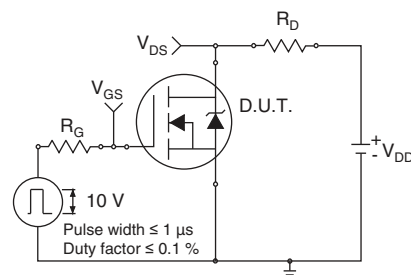
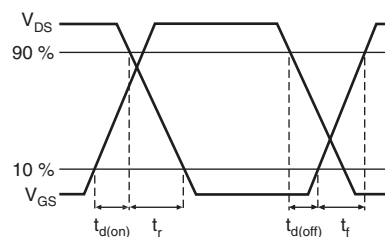
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

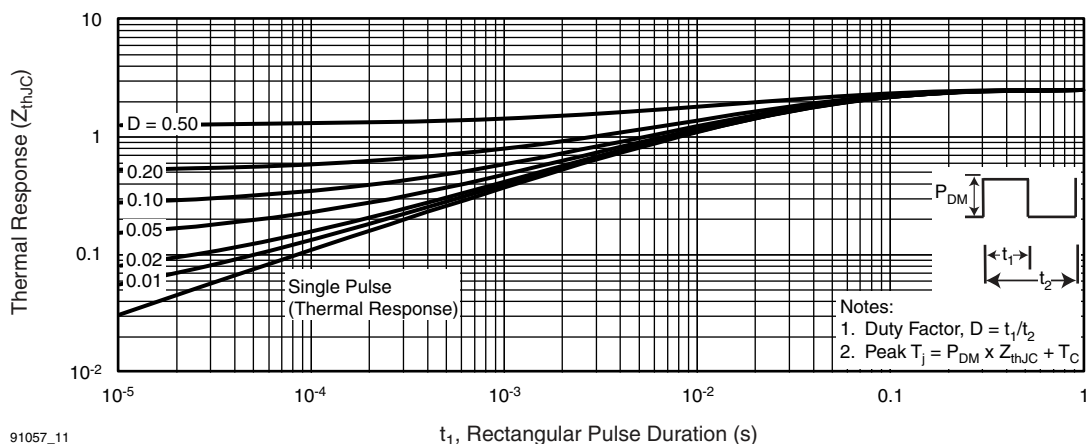
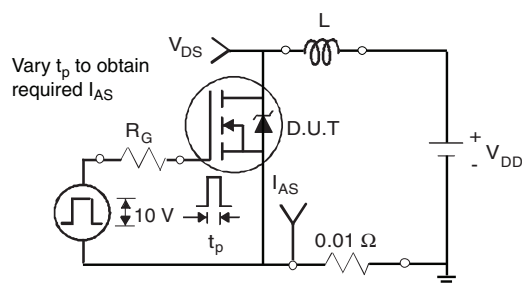
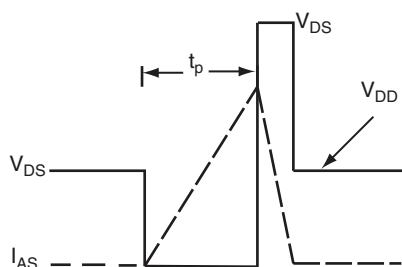
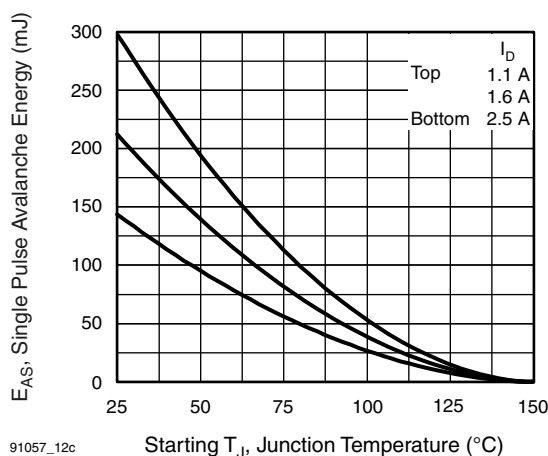
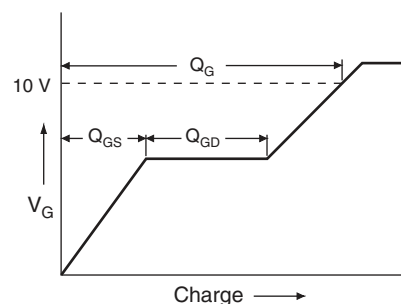
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.60	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.5 A <sup>b</sup>	-	-	3.0	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.5 A <sup>b</sup>		1.4	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	340	-	pF
Output capacitance	C <sub>oss</sub>			-	53	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	2.7	-	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 1.0 V, f = 1.0 MHz			490		
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 400 V, f = 1.0 MHz			15		
Effective output capacitance	C <sub>oss eff.</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 0 V to 400 V <sup>c</sup>			28		
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.5 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	17	nC
Gate-source charge	Q <sub>gs</sub>			-	-	4.3	
Gate-drain charge	Q <sub>gd</sub>			-	-	8.5	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 2.5 A, R <sub>g</sub> = 21 Ω, R <sub>D</sub> = 97 Ω, see fig. 10 <sup>b</sup>		-	8.1	-	ns
Rise time	t <sub>r</sub>			-	12	-	
Turn-Off delay time	t <sub>d(off)</sub>			-	16	-	
Fall time	t <sub>f</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.5	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	10	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 2.5 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 2.5 A, dI/dt = 100 A/μs <sup>b</sup>		-	330	500	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	760	1140	nC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

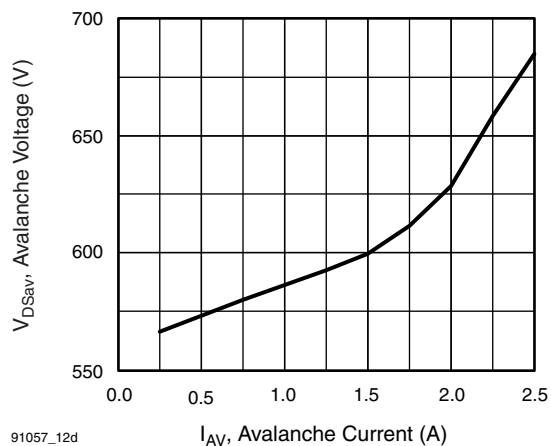
**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

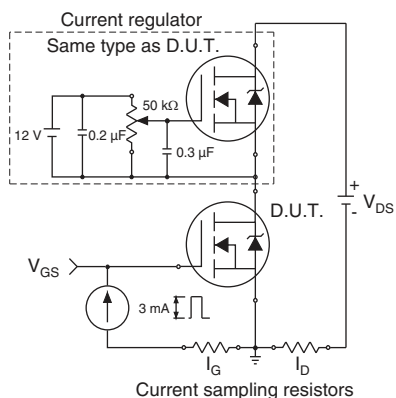
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10 - Switching Time Test Circuit**

**Fig. 11 - Switching Time Waveforms**

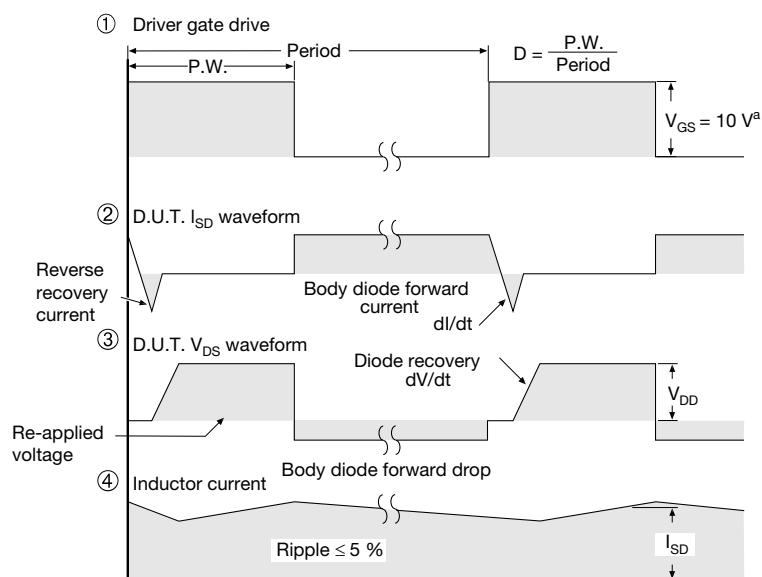
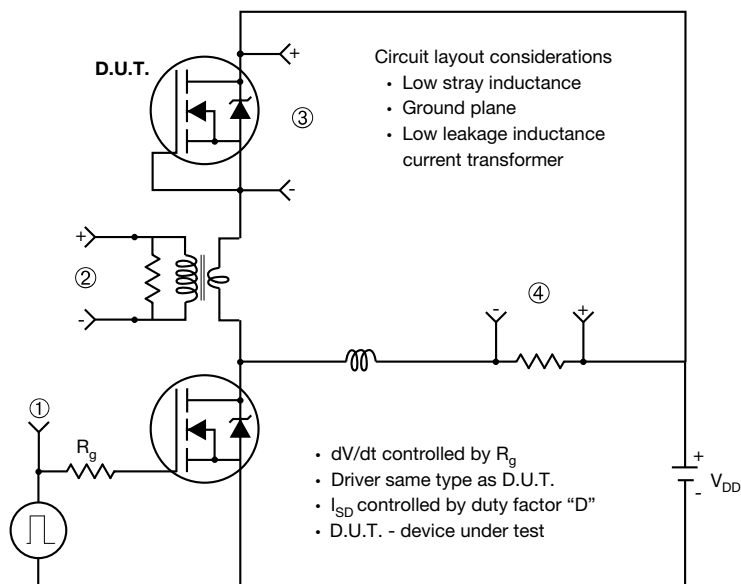

**Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 13 - Unclamped Inductive Test Circuit**

**Fig. 14 - Unclamped Inductive Waveforms**

**Fig. 15 - Maximum Avalanche Energy vs. Drain Current**

**Fig. 16 - Basic Gate Charge Waveform**



**Fig. 17 - Typical Drain-to-Source Voltage vs. Avalanche Current**



**Fig. 18 - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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