



# Automotive P-Channel 30 V (D-S) 175 °C MOSFET

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Top View

Marking Code: 90

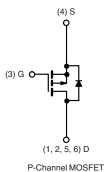
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	- 30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.043			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.070			
I <sub>D</sub> (A)	- 7.5			
Configuration	Single			

#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



FREE



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and halogen-free	SQ3481CEV (for detailed order number please see <a href="https://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	$V_{DS}$	-30			
Gate-source voltage	$V_{GS}$	± 20	V		
Continuous drain current	T <sub>C</sub> = 25 °C		-7.5		
	T <sub>C</sub> = 125 °C	l <sub>D</sub>	-4.3		
Continuous source current	I <sub>S</sub>	-5.2	Α		
Pulsed drain current <sup>a</sup>	I <sub>DM</sub>	-30			
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	-15		
Single pulse avalanche energy	L = 0.1 IIII	E <sub>AS</sub>	11	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C	D	4	W	
	T <sub>C</sub> = 125 °C	$P_{D}$	1.3	V V	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	LIMIT	UNIT			
Junction-to-ambient	PCB mount	$R_{thJA}$	110	°C/W		
Junction-to-foot (drain)		$R_{thJF}$	36	C/VV		

#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. When mounted on 1" square PCB (FR-4 material)



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static							ı	
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-0	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-2.0	-2.5	V	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V	-	-	-1		
Zero gate voltage drain current	$I_{DSS}$	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	-	-	-50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-150		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	$V_{DS} \le -5 \text{ V}$	-10	-	-	Α	
Drain course on state registence 3		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -5.3 A	-	0.035	0.043	Ω	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -2 A	-	0.055	0.070		
Forward transconductance b	9fs	V <sub>DS</sub> =	-15 V, I <sub>D</sub> = -5.3 A	-	13	-	S	
		Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>			-	704	870		
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = -15 V, f = 1 MHz	-	149	200	pF	
Reverse transfer capacitance	C <sub>rss</sub>			-	109	150		
Total gate charge <sup>c</sup>	Qg			-	15.5	23.5		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	$V_{DS} = -15 \text{ V}, I_{D} = -5.3 \text{ A}$	-	3.0		nC	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	3.9			
Gate resistance	$R_g$	f = 1 MHz		3.2	6.6	18.5	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	9	14		
Rise time <sup>c</sup>	t <sub>r</sub>		$V_{DD} = -15 \text{ V}, R_{I} = 15 \Omega$		15	23	- ns	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$		-	28	42		
Fall time <sup>c</sup>	t <sub>f</sub>			-	12	18		
Source-Drain Diode Ratings and Characte	eristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			1	-	-30	Α	
Forward voltage	$V_{SD}$	I <sub>F</sub> = -1.7 A, V <sub>GS</sub> = 0 V		-	-0.8	-1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>				15	30	ns	
Body diode reverse recovery charge	$Q_{rr}$			1	8	16	nC	
Reverse recovery fall time	ta			-	9	-	ne	
Reverse recovery rise time	t <sub>b</sub>			-	6	-	ns	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.11	-	Α	

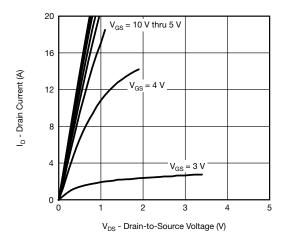
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

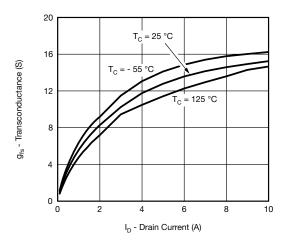
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



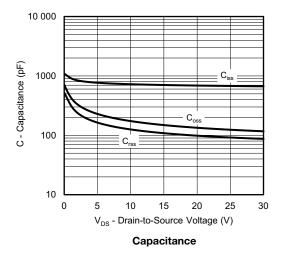
# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

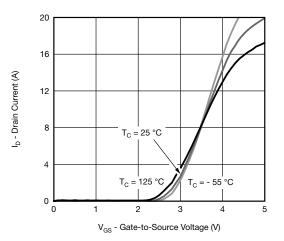


#### **Output Characteristics**

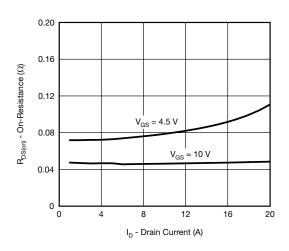


## Transconductance

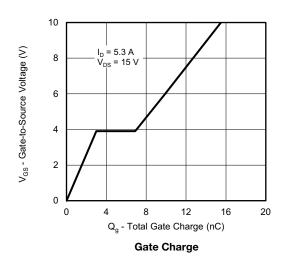




#### **Transfer Characteristics**

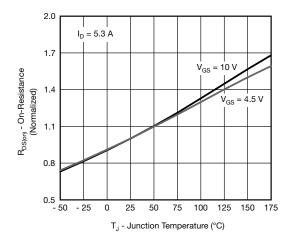


### On-Resistance vs. Drain Current

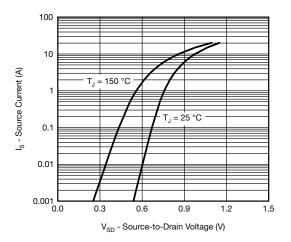




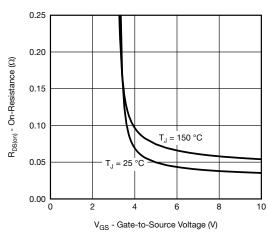
# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



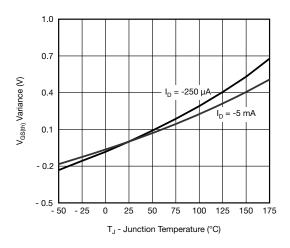
On-Resistance vs. Junction Temperature



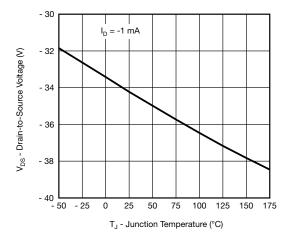
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



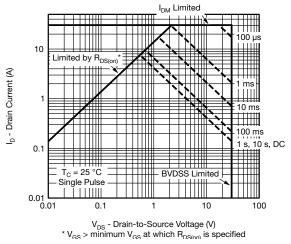
Threshold Voltage



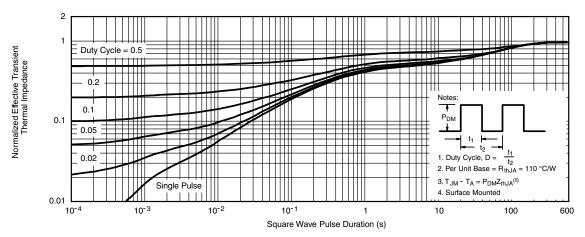
**Drain Source Breakdown vs. Junction Temperature** 



# **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



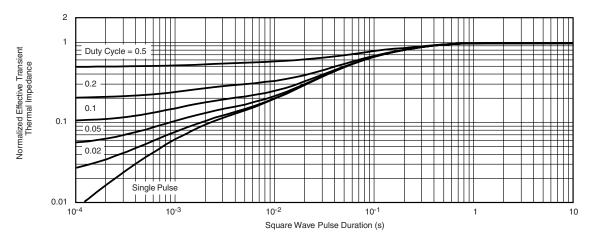
#### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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# **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?62288">www.vishay.com/ppg?62288</a>.





TSOP: 5/6-LEAD

**JEDEC Part Number: MO-193C** 





**5-LEAD TSOP** 







	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A <sub>1</sub>	0.01	-	0.10	0.0004	-	0.004	
A <sub>2</sub>	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC		0.0374 BSC			
e <sub>1</sub>	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L <sub>1</sub>		0.60 Ref		0.024 Ref			
L <sub>2</sub>		0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

DWG: 5540

Document Number: 71200 18-Dec-06



# Recommended Land Pattern For TSOP-5L / TSOP-6L



# Note

• All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022 DWG: 3010



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