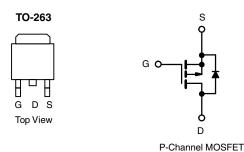


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Vishay Siliconix

# Automotive P-Channel 80 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	- 80				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.025				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.031				
I <sub>D</sub> (A)	- 50				
Configuration	Single				



#### **FEATURES**

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R<sub>q</sub> and UIS Tested
- AEC-Q101 Qualified<sup>d</sup>
- Material categorization:
  For definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>



HALOGEN

FREE

ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and Halogen-free	SQM50P08-25L-GE3

ABSOLUTE MAXIMUM RATING	GS (T <sub>C</sub> = 25 °C, unles	ss otherwise noted	d)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	- 80	V	
Gate-Source Voltage	$V_{GS}$	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>		- 50	
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	- 30	
Continuous Source Current (Diode Conduc	I <sub>S</sub>	- 50	Α	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	- 120		
Single Pulse Avalanche Current	0.1 ml	I <sub>AS</sub>	- 47	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	110	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	5	150	10/
	T <sub>C</sub> = 125 °C	$P_{D}$	50	W
Operating Junction and Storage Temperatu	ure Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W		
Junction-to-Case (Drain)		$R_{thJC}$	1	C/VV		

### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



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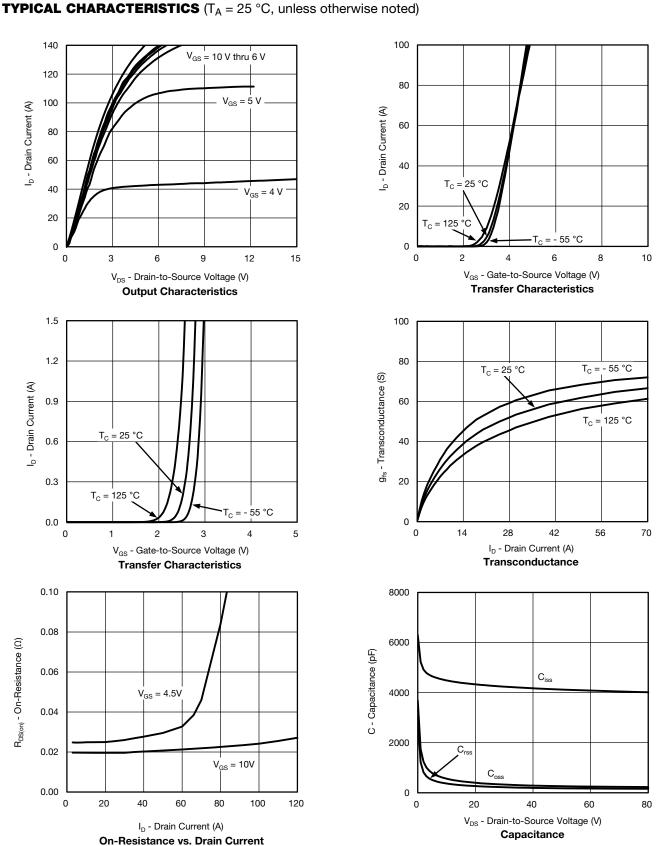
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static		-						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		- 80	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1.5	- 2.0	- 2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V	-	-	- 1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V, T <sub>J</sub> = 125 °C	-	-	- 50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 80 V, T <sub>J</sub> = 175 °C	-	-	- 250	1	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V	$V_{DS} \le -5 V$	- 50	-	-	Α	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A	-	0.020	0.025	Ω	
Dunin Course On Otata Basistanas		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A, T <sub>J</sub> = 125 °C	-	-	0.044		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 12.5 A, T <sub>J</sub> = 175 °C	-	-	0.055		
		V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 10.5 A	-	0.025	0.031		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 12.5 A		-	36	=-	S	
Dynamic <sup>b</sup>		<u> </u>					•	
Input Capacitance	C <sub>iss</sub>				4280	5350		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = - 25 V, f = 1 MHz	-	356	445	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	240	300		
Total Gate Charge <sup>c</sup>	Qg			-	91	137	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = - 10 V	$V_{DS} = -40 \text{ V}, I_{D} = -12.5 \text{ A}$	-	8.2	=-		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>				24	-	1	
Gate Resistance	R <sub>g</sub>		f = 1 MHz		2.99	4.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	11	17		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = -40 \text{ V}, \text{ R}_{L} = 3.2 \Omega$ $I_{D} \cong -12.5 \text{ A}, \text{ V}_{GEN} = -10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	11	17	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	71	107		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	16	24		
Source-Drain Diode Ratings and Char	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 120	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> =	I <sub>F</sub> = - 20 A, V <sub>GS</sub> = 0 V			- 1.5	V	

#### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



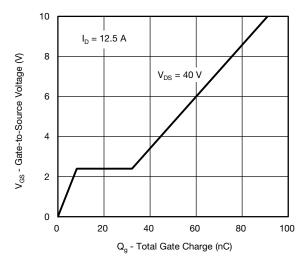


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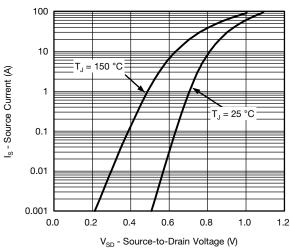


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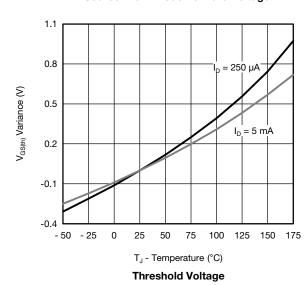
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)

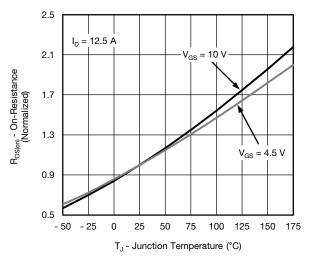


### **Gate Charge**

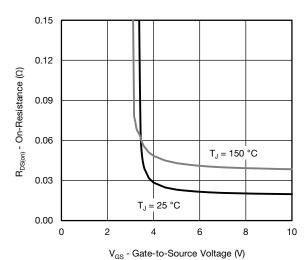


**Source Drain Diode Forward Voltage** 

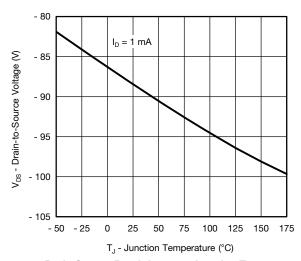




On-Resistance vs. Junction Temperature



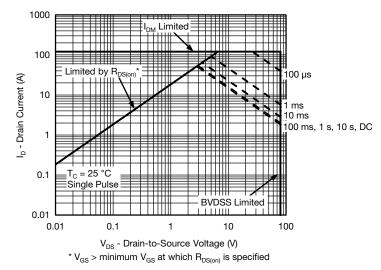
On-Resistance vs. Gate-to-Source Voltage



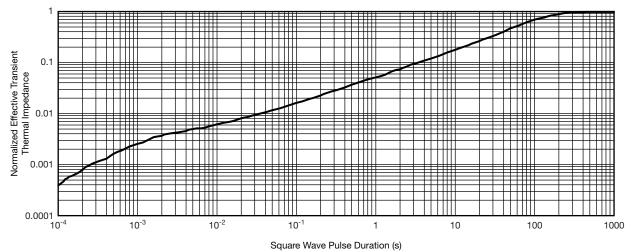
Drain Source Breakdown vs. Junction Temperature



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



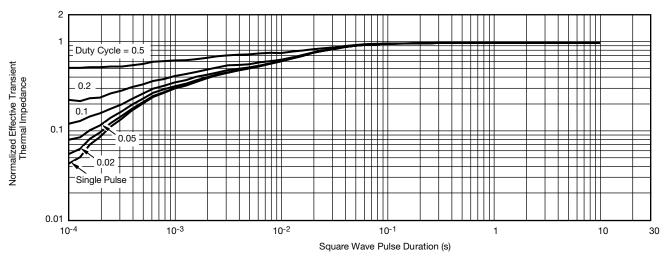
#### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD









DETAIL A (ROTATED 90°)



⋝:	,	 	b— b1–		ļ	ļ
2:	П				5	ပ
	SE	СТ	ION	ΙΔ.	- 1 - Δ	Ŧ

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6 This feature is for thick lead.

		INCHES		MILLIMETERS		
	DIM.	MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	BSC	2.54 BSC		
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
M		- 0.002		-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





## RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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