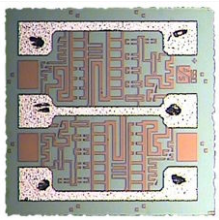
Thin Film Center-Tapped Resistors Divider Network for High Temperature Applications



Product may not be to scale

The TCTR series of center-tapped resistor dividers offer a small size, wide ohmic value range and excellent power capacity, maintaining these qualities to temperatures up to 250 °C. The TCTR Tantalum Nitride resistor material offers excellent resistance to high moisture environments. The TCTR's six bonding pad configuration allows for maximum layout flexibility.

The TCTRs are manufactured using Vishay Electro-Films (EFI) sophisticated thin-film equipment and manufacturing technology. The TCTR's are 100 % electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Qualified to operate at elevated temperatures up to 250 °C
- DC power rating up to 250 mW
- Small size: 0.03" square
- Case: 0303
- Self passivating tantalum nitride film
- Oxidized silicon substrate
- Wide value range: 100 Ω to 100 kΩ
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

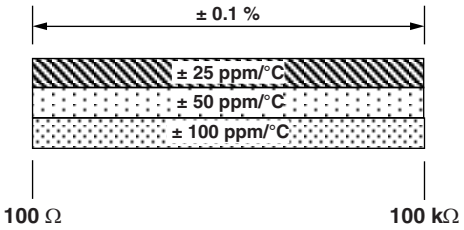
HALOGEN FREE GREEN (5-2008)

APPLICATIONS

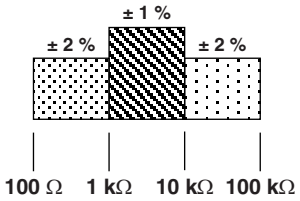
Vishay EFI TCTR top-contact 0.03" square resistor divider chips are designed to operate at elevated temperatures and power loads in many types of hybrid (chip and wire) assemblies. They are ideally suited for extreme environment applications such as "down hole" drilling.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	**VALUE**	**UNIT**
Resistance Range	100 to 100K	Ω
Tolerances	± 0.1	%
TCR	Down to ± 25	ppm/°C

Tightest Standard Tolerance Available

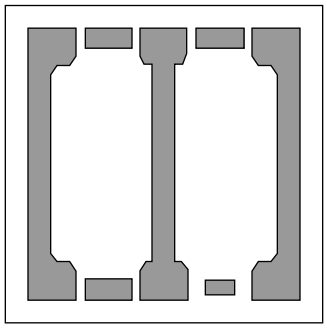


Load Life Stability, 1000 h, +125 °C, 175 mW



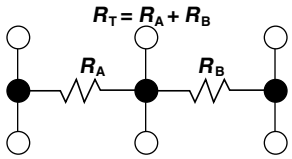
STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	**VALUE**	**UNIT**
Noise, MIL-STD-202, Method 308	-20	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, +125 °C, 175 mW	Down to ± 1	%
Operating Temperature Range	-55 to +250	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. $\Delta R/R$	%
High Temperature Exposure, +250 °C, 1000 h	Down to ± 1	%
Dielectric Voltage Breakdown	200	V
Operating Voltage	100 max.	V
DC Power Rating at +125 °C (Derated to Zero at +250 °C)	250 at 70 °C	mW
5 x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.25 max. $\Delta R/R$	%
TCR Tracking Between Halves (RA/RB)	± 2	ppm/°C
Center Tap Ratio (RA/RB) Tolerance	1 ± 1 standard	%

DIMENSIONS



TYPICAL RANGE
100 Ω to 1 MΩ

SCHEMATIC



MECHANICAL SPECIFICATIONS in inches (millimeters)	
PARAMETER	
Chip Size	0.030 x 0.030 ± 0.002 (0.762 x 0.762 ± 0.05)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO_2
Film Material	Tantalum nitride, self-passivating
Passivation	None
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127)
Number of Pads	6
Pad Material	100 µ" Au
Backing	None, lapped silicon (Au optional)

GLOBAL PART NUMBER INFORMATION

Global Part Number: TCTR50000FKGNHWS

Global Part Number Description: TCTR 5K 1 % 100 ppm/°C Au None H WS

T	C	T	R	5	0	0	0	0	F	K	G	N	H	W	S

MODEL	RESISTANCE	RESISTANCE MULTILPLIER CODE	TOL. CODE (%)	TCR (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE
TCTR	First 4 digits are significant figures of resistance	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10 **2** = 100 **3** = 1000	**B** = 0.1 **C** = 0.25 **D** = 0.5 **F** = 1.0 **G** = 2.0 **H** = 2.5 **J** = 5.0 **K** = 10.0	**E** = ± 25 **C** = ± 50 **K** = ± 100 **M** = ± 250	**G** = Au	**G** = Au **N** = None	**H** = Class H **K** = Class K	**WS** = Waffle pack 100 min., 1 mult

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