

## E Series Power MOSFET with Fast Body Diode



### FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM)  $R_{DS(on)} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.157
$Q_g$ max. (nC)	102	
$Q_{gs}$ (nC)	15	
$Q_{gd}$ (nC)	28	
Configuration	Single	

### ORDERING INFORMATION

Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH21N65EF-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	53	
Linear derating factor		1.47	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	353	mJ
Maximum power dissipation	$P_D$	156	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dV/dt$	$T_J = 125$ °C	V/ns
Reverse diode $dv/dt$ <sup>c</sup>			


#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature  
 b.  $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 5$  A  
 c.  $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

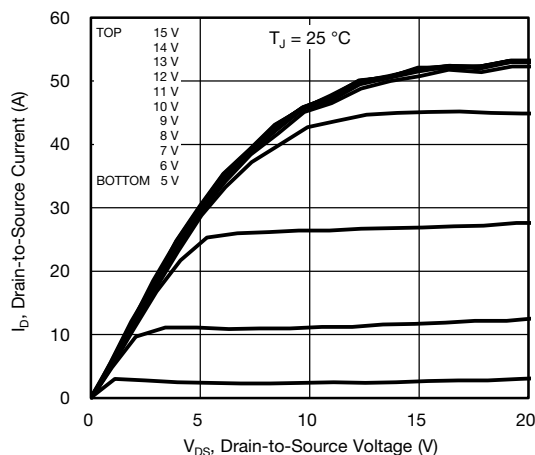
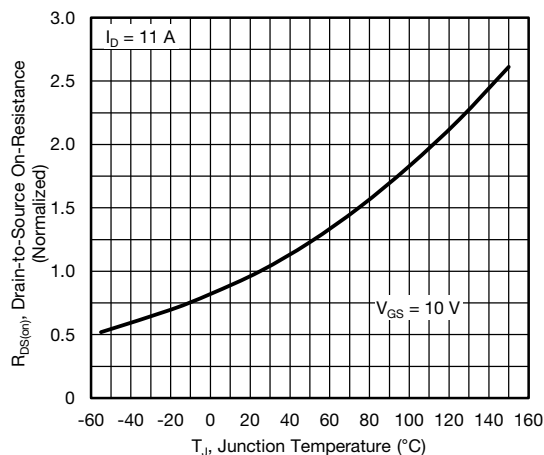
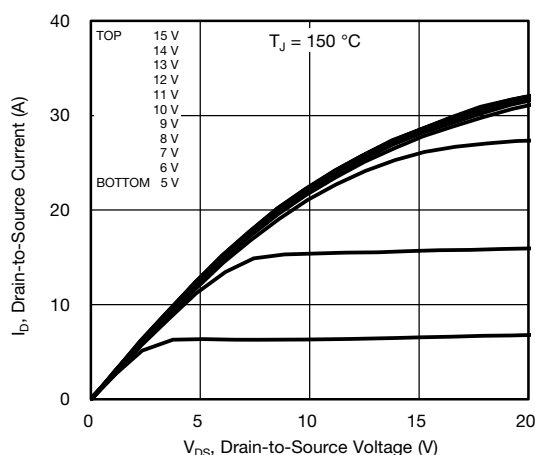
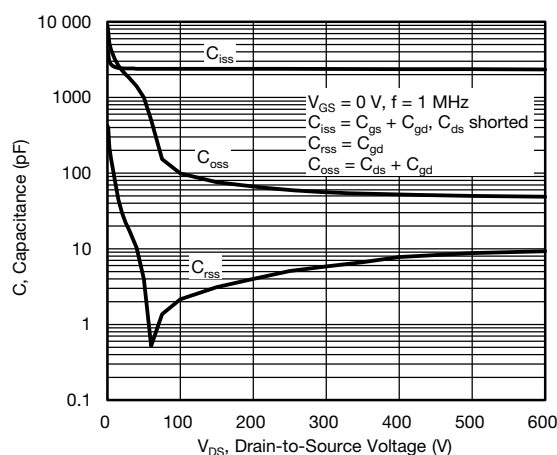
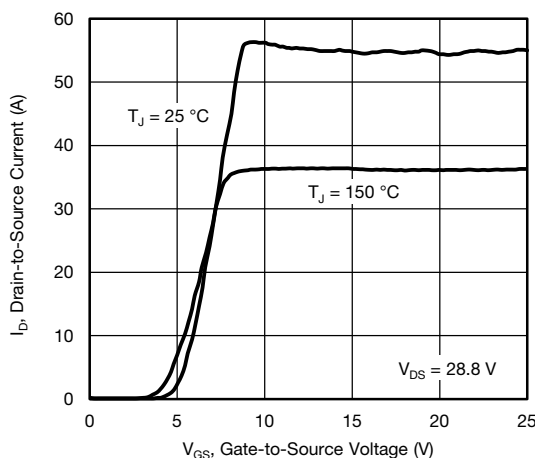
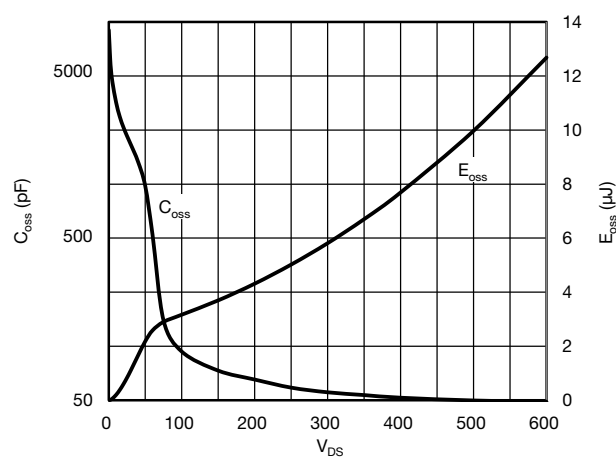
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	39	51	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.51	0.68	

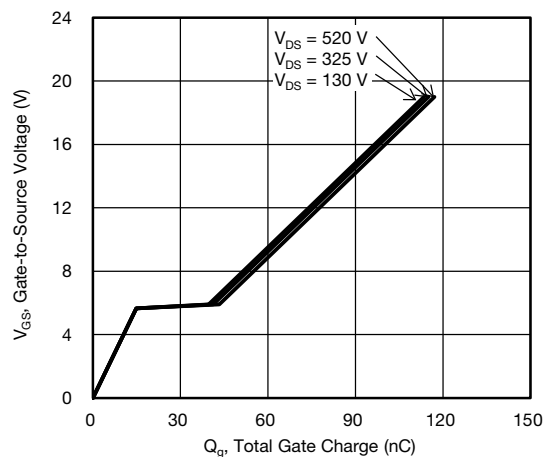
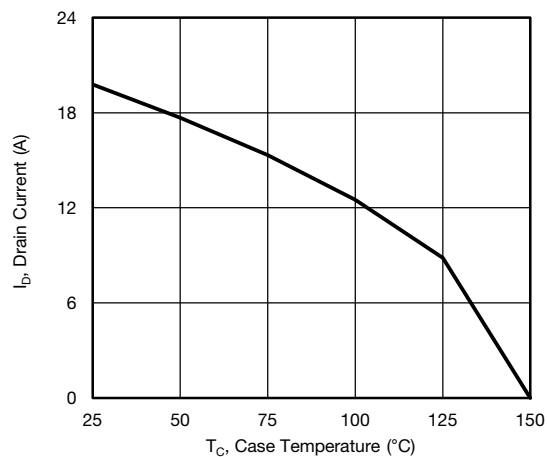
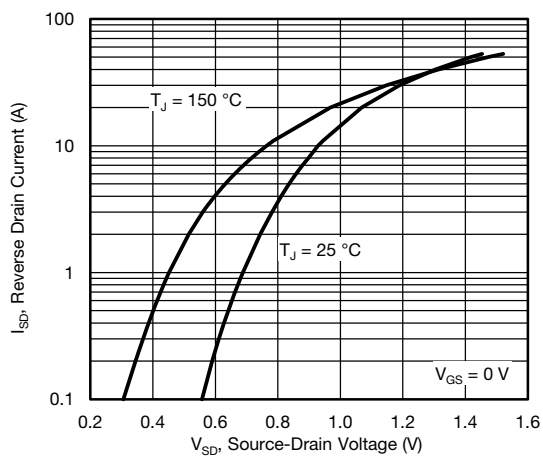
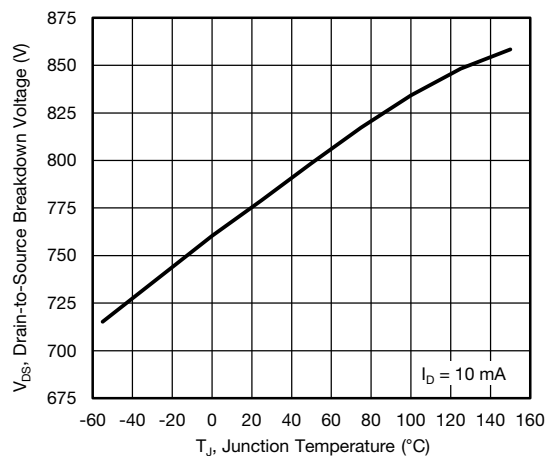
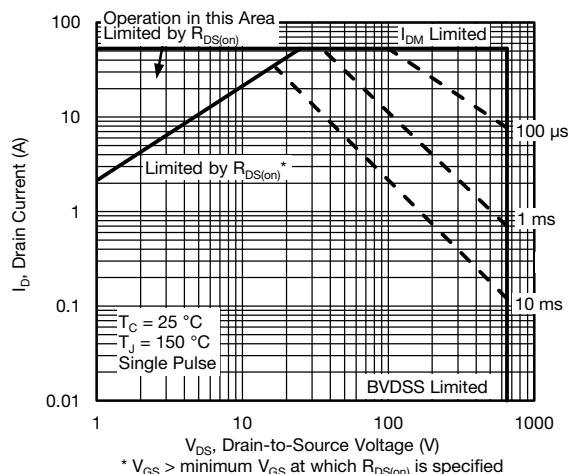
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

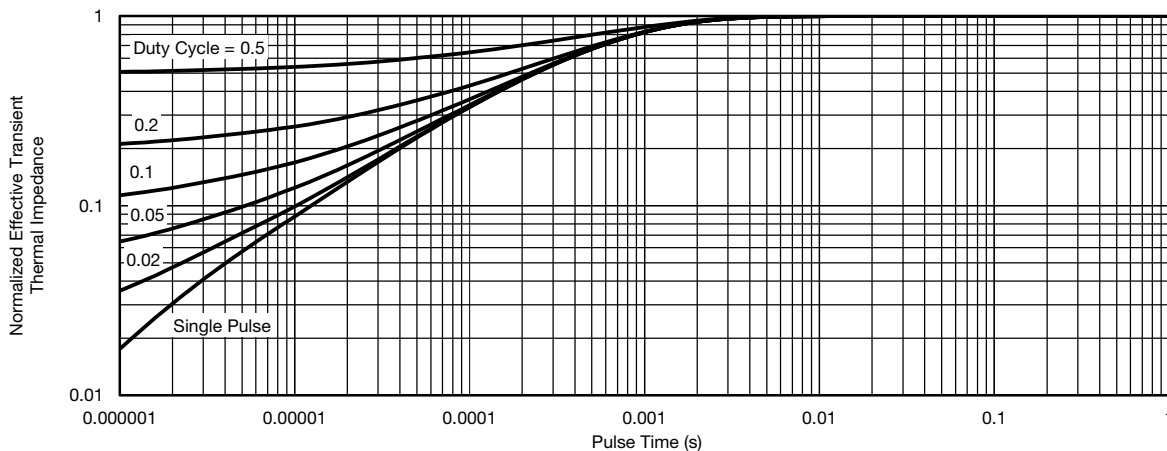
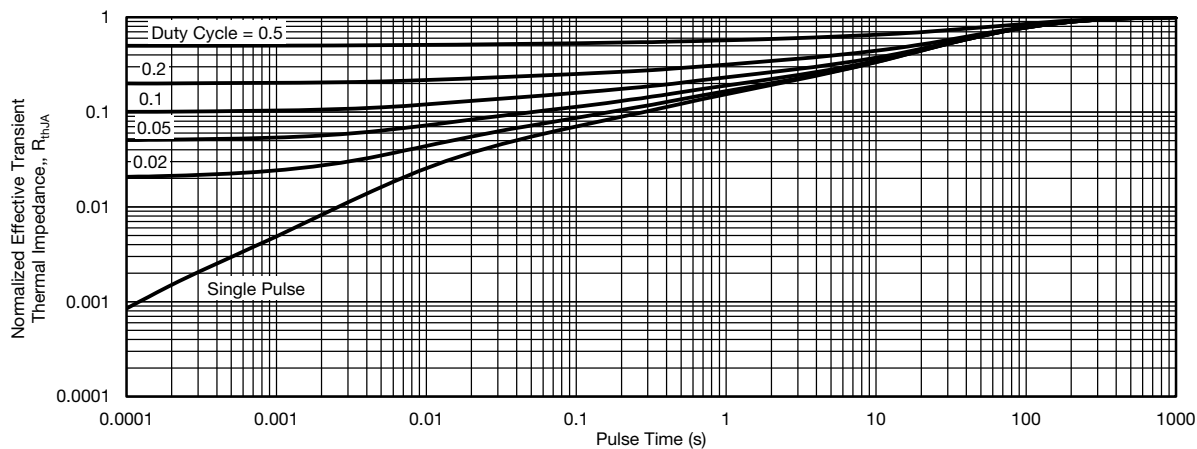
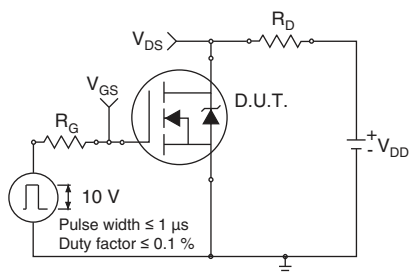
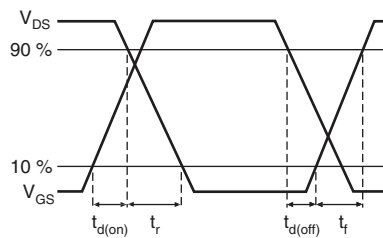
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 10\text{ mA}$		-	0.70	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 520\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}$	-	0.157	0.180	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}$ , $I_D = 11\text{ A}$		-	7.8	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$		-	2396	-	pF
Output Capacitance	$C_{oss}$			-	99	-	
Reverse Transfer Capacitance	$C_{rss}$			-	2	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}$ , $V_{GS} = 0\text{ V}$		-	74	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	316	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}$ , $V_{DS} = 520\text{ V}$	-	68	102	nC
Gate-Source Charge	$Q_{gs}$			-	15	-	
Gate-Drain Charge	$Q_{gd}$			-	28	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$ , $I_D = 11\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_g = 9.1\text{ }\Omega$		-	24	48	ns
Rise Time	$t_r$			-	43	86	
Turn-Off Delay Time	$t_{d(off)}$			-	72	108	
Fall Time	$t_f$			-	46	92	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		0.27	0.55	1.10	$\Omega$
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	19.8	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	53	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 11\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.95	1.3	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = I_S = 11\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 25\text{ V}$		-	145	290	ns
Reverse Recovery Charge	$Q_{rr}$			-	0.9	1.8	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	11.6	-	A

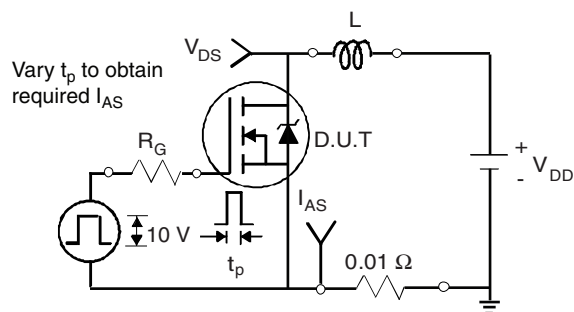
**Notes**

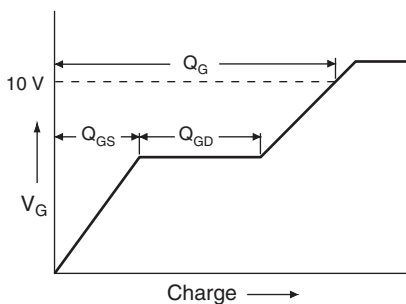
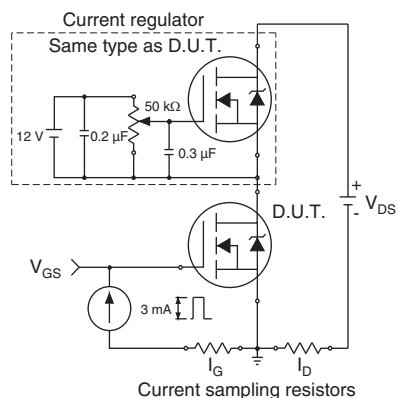
- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

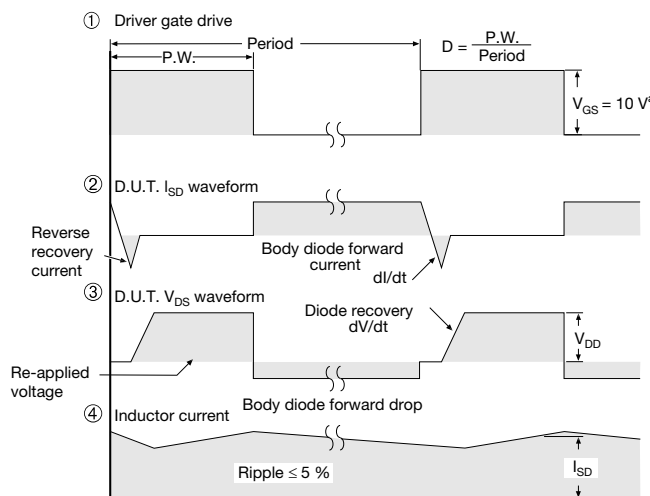
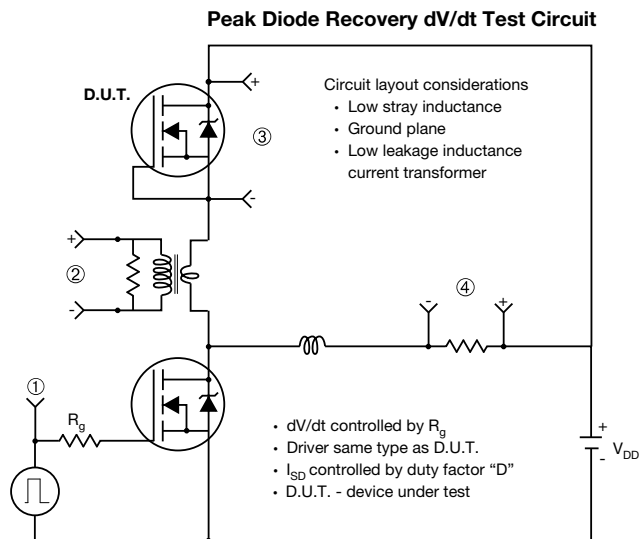
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{ds}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**


**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

**Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Fig. 14 - Switching Time Test Circuit**

**Fig. 15 - Switching Time Waveforms**


**Fig. 16 - Unclamped Inductive Test Circuit**

**Fig. 17 - Unclamped Inductive Waveforms**

**Fig. 18 - Basic Gate Charge Waveform**

**Fig. 19 - Gate Charge Test Circuit**



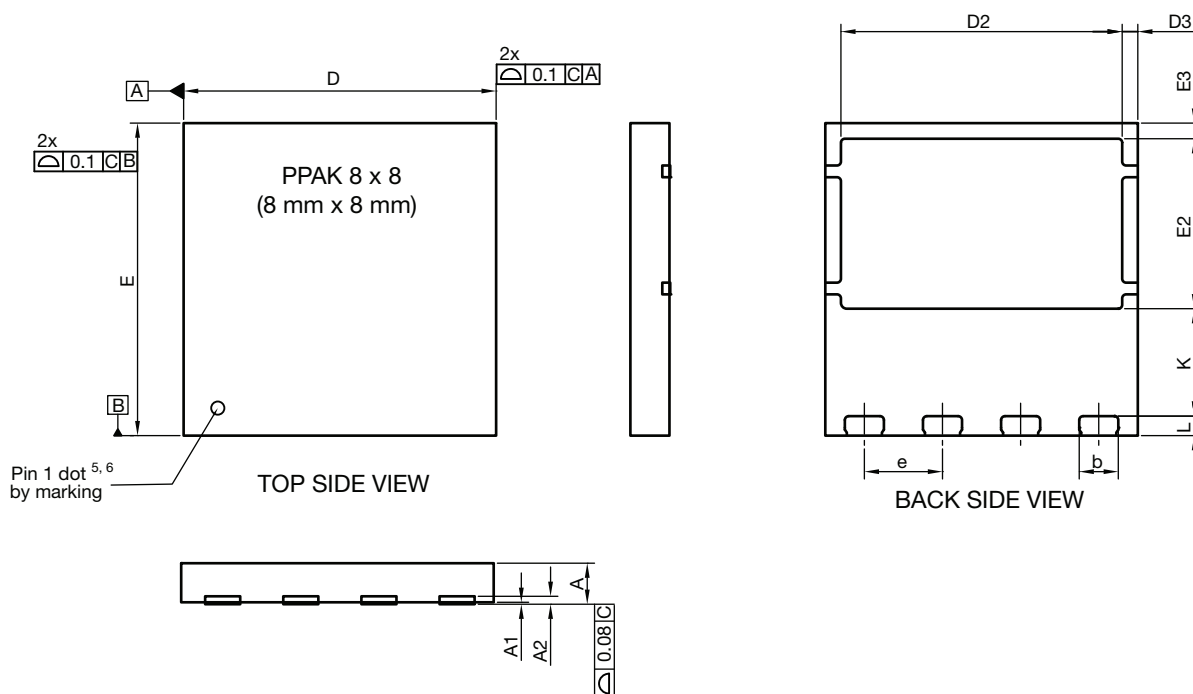
**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 20 - For N-Channel**

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## PowerPAK® 8 x 8 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>(3)</sup>	8			8		

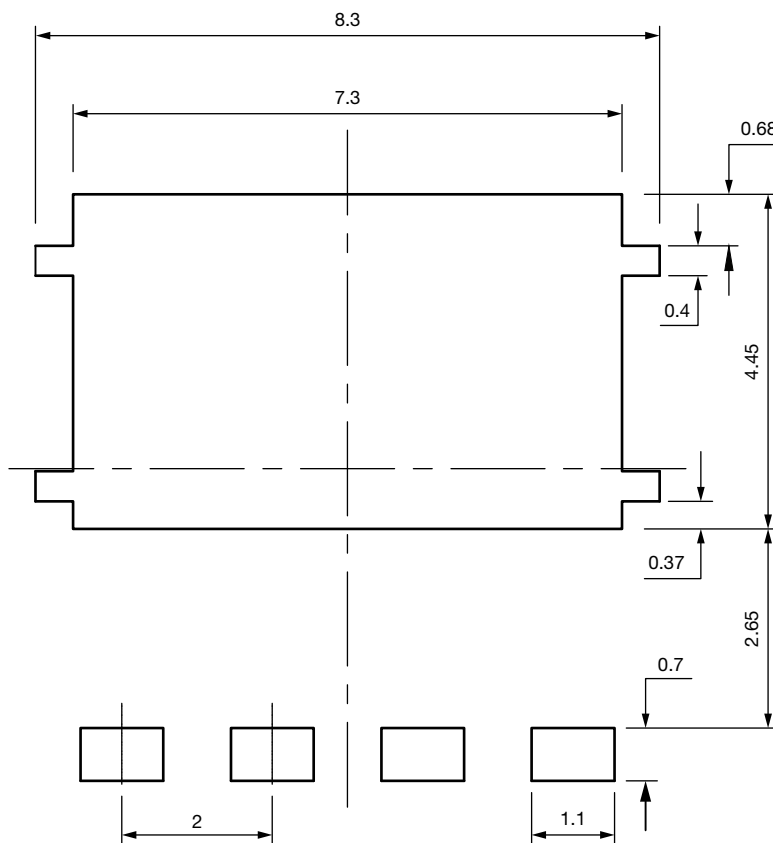
### Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020  
DWG: 6041



## Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm



Dimensions in millimeters



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