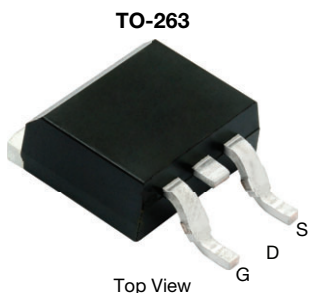


## P-Channel 80 V (D-S) MOSFET



### FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low  $R_{DS(on)}$  minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

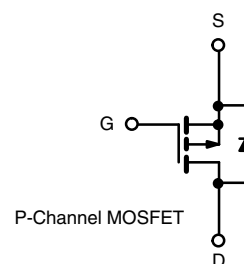


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
$V_{DS}$ (V)	-80
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -10$ V	0.0061
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0086
$Q_g$ typ. (nC)	145
$I_D$ (A)	-150
Configuration	Single

### APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



ORDERING INFORMATION	
Package	TO-263
Lead (Pb)-free and halogen-free	SUM60061EL-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	-80	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current <sup>d</sup> (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-150 <sup>d</sup>	A
	T <sub>C</sub> = 70 °C		-150 <sup>d</sup>	
Pulsed drain current (100 μs)		I <sub>DM</sub>	-250	
Avalanche current	L = 0.1 mH	I <sub>AS</sub>	-75	
Single pulse avalanche energy <sup>a</sup>		E <sub>AS</sub>	281	mJ
Power dissipation	T <sub>C</sub> = 25 °C <sup>c</sup>	P <sub>D</sub>	375	W
	T <sub>C</sub> = 125 °C <sup>b</sup>		125	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	$R_{thJA}$	40	°C/W
Junction-to-case		$R_{thJC}$	0.4	

### Notes

- Duty cycle  $\leq 1$  %
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Limited by package



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -10 mA	-80	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-	-2.5	
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -80 V, V <sub>GS</sub> = 0 V	-	-	-10	μA
		V <sub>DS</sub> = -64 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>DS</sub> = -64 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	-30	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -20 A	-	0.0051	0.0061	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -15 A	-	0.0069	0.0086	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -15 A	-	80	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -40 V, f = 1 MHz	-	9600	-	pF
Output capacitance	C <sub>oss</sub>		-	3300	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	110	-	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -110 A	-	145	218	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	34	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	16	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.46	2.3	4.6	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -40 V, R <sub>L</sub> = 0.71 Ω I <sub>D</sub> ≅ -20 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	-	25	35	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	20	30	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	90	140	
Fall time <sup>c</sup>	t <sub>f</sub>		-	20	30	
Drain-Source Body Diode Characteristics (T <sub>C</sub> = 25 °C <sup>b</sup> )						
Continuous current	I <sub>S</sub>		-	-	-150	A
Pulsed current	I <sub>SM</sub>		-	-	-250	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0 V	-	-0.8	-1.5	V
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -20 A, dI/dt = 100 A/μs	-	90	135	ns
Peak reverse recovery charge	I <sub>RM(REC)</sub>		-	-2.8	-4.2	A
Reverse recovery charge	Q <sub>rr</sub>		-	145	218	nC

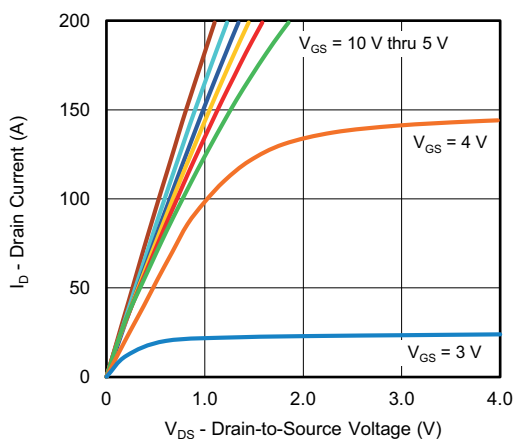
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

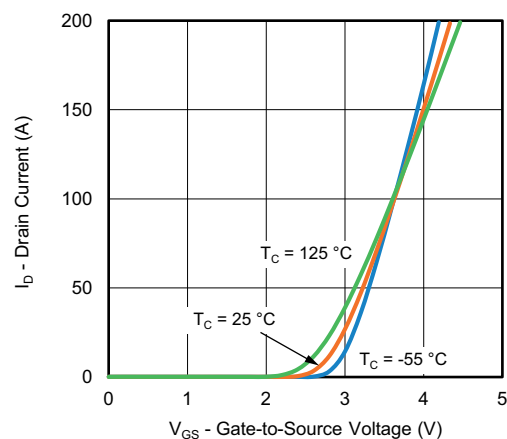
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



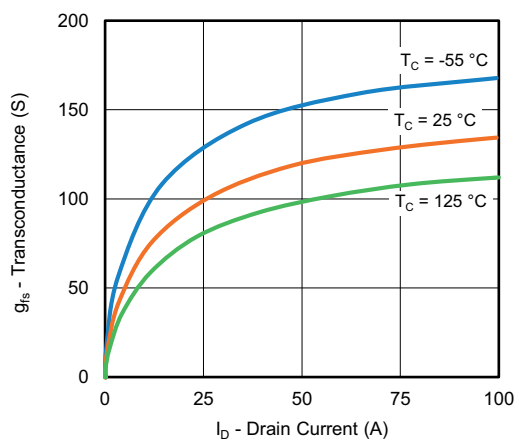
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



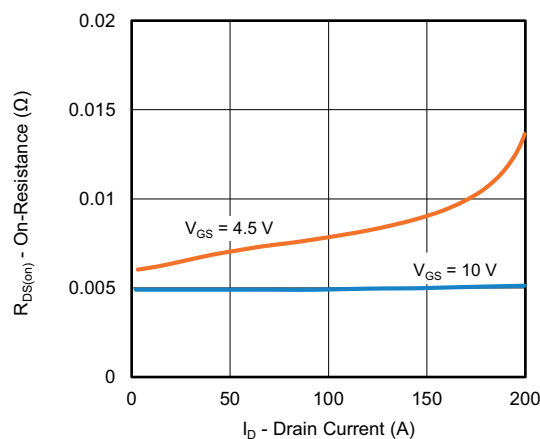
**Output Characteristics**



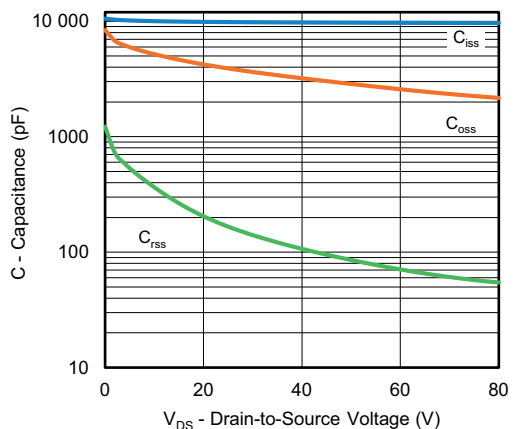
**Transfer Characteristics**



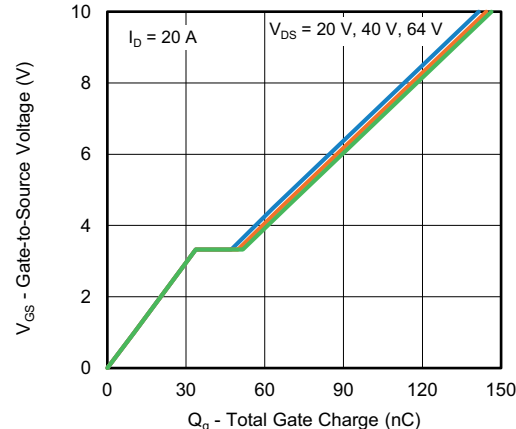
**Transconductance**



**On-Resistance vs. Drain Current**



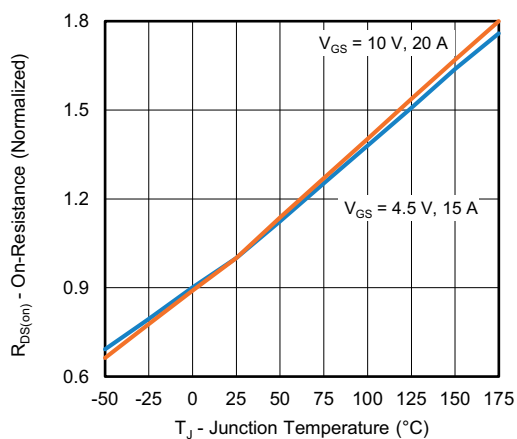
**Capacitance**



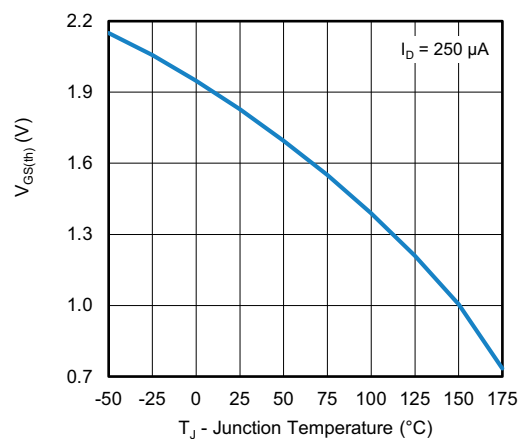
**Gate Charge**



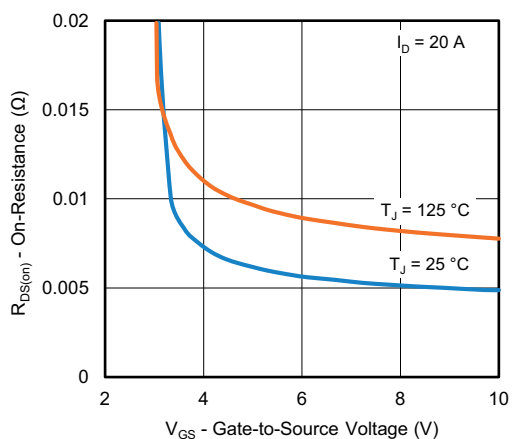
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



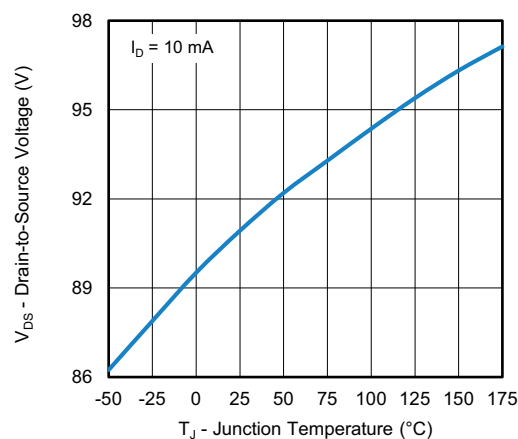
**On-Resistance vs. Junction Temperature**



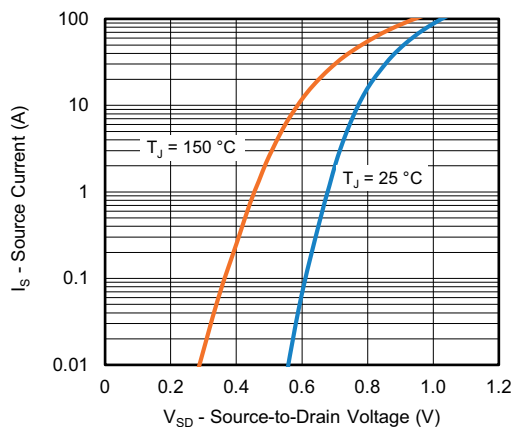
**Threshold Voltage**



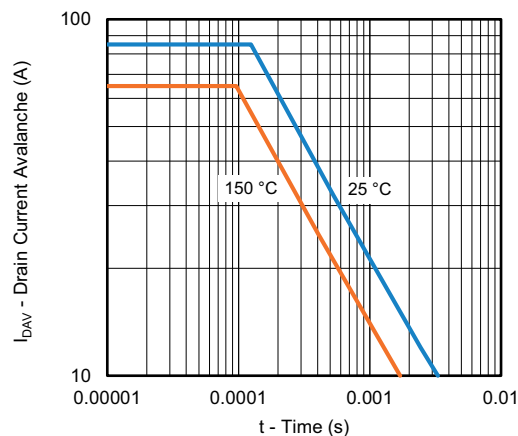
**On-Resistance vs. Gate-to-Source Voltage**



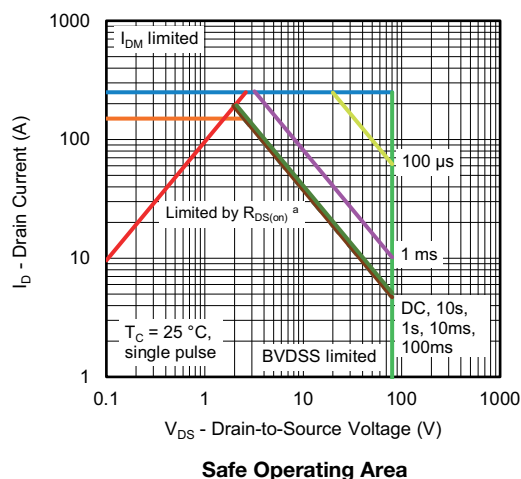
**Drain Source Breakdown vs. Junction Temperature**



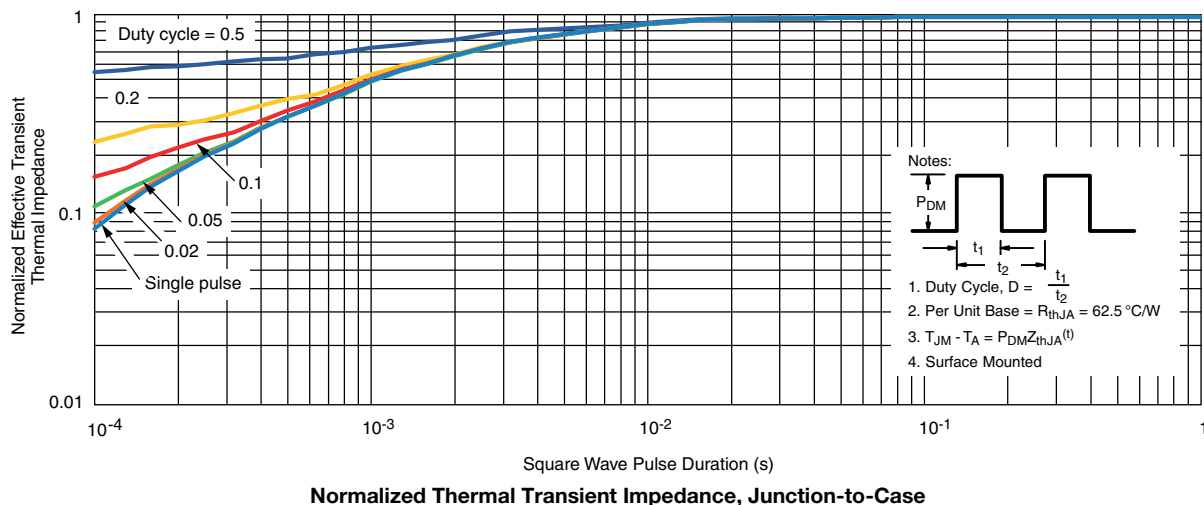
**Source Drain Diode Forward Voltage**



**Avalanche Current vs. Time**

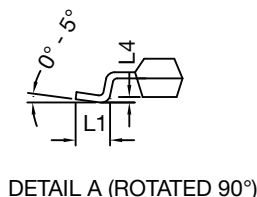
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

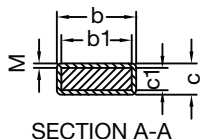


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## TO-263 (D<sup>2</sup>PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

### Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

ECN: T13-0707-Rev. K, 30-Sep-13  
DWG: 5843

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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