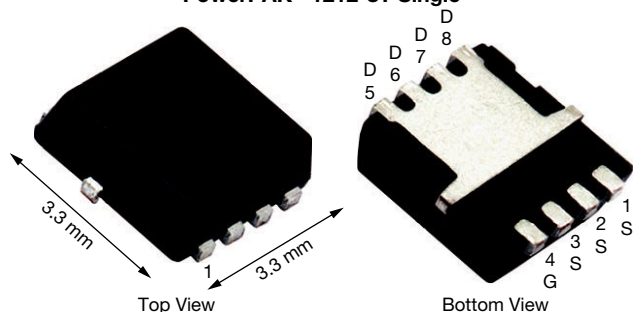


P-Channel 30 V (D-S) MOSFET

PowerPAK® 1212-8T Single


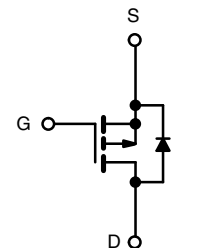
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Thin 0.8 mm profile
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook PC
 - Load switch
 - Battery switch
 - Adaptor switch



P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.021
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.034
Q_g typ. (nC)	15
I_D (A) ^{d, e}	-20
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 1212-8T
Lead (Pb)-free and halogen-free	SiS429DNT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	-20 ^e
		$T_C = 70^\circ\text{C}$	-20 ^e
		$T_A = 25^\circ\text{C}$	-10.5 ^{a, b}
		$T_A = 70^\circ\text{C}$	-8.3 ^{a, b}
Pulsed drain current ($t = 100 \mu\text{s}$)	I_{DM}	-50	A
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-20 ^e
		$T_A = 25^\circ\text{C}$	-2.9 ^{a, b}
Avalanche current	I_{AS}	-20	A
Single-pulse avalanche energy	E_{AS}	20	mJ
Maximum power dissipation	P_D	$T_C = 25^\circ\text{C}$	27.8
		$T_C = 70^\circ\text{C}$	17.8
		$T_A = 25^\circ\text{C}$	3.5 ^{a, b}
		$T_A = 70^\circ\text{C}$	2.2 ^{a, b}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^{f, g}		260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, c}	R_{thJA}	29	36	$^\circ\text{C}/\text{W}$
Maximum junction-to-case	R_{thJC}	3.6	4.5	$^\circ\text{C}/\text{W}$

Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is $81^\circ\text{C}/\text{W}$
- Based on $T_C = 25^\circ\text{C}$
- Package limited
- See solder profile (www.vishay.com/doc?73257). The Thin PowerPAK 1212-8T is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-31	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	4.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-3	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-5	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ -10 V, V _{GS} = -10 V	-30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -10.5 A	-	0.0175	0.0210	Ω
		V _{GS} = -4.5 V, I _D = -8.3 A	-	0.0283	0.0340	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -10.5 A	-	23	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	1350	-	pF
Output capacitance	C _{oss}		-	215	-	
Reverse transfer capacitance	C _{rss}		-	185	-	
Total gate charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -10.5 A	-	32	50	nC
Gate-source charge	Q _{gs}	V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -10.5 A	-	15	25	
Gate-drain charge	Q _{gd}		-	4	-	
Gate resistance	R _g		-	7.5	-	
Gate resistance	R _g	f = 1 MHz	1.2	5.8	11.6	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.8 Ω I _D ≅ -8.4 A, V _{GEN} = -10 V, R _g = 1 Ω	-	10	15	ns
Rise time	t _r		-	8	15	
Turn-off delay time	t _{d(off)}		-	45	70	
Fall time	t _f		-	12	25	
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.8 Ω I _D ≅ -8.4 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	42	70	
Rise time	t _r		-	35	60	
Turn-off delay time	t _{d(off)}		-	40	70	
Fall time	t _f		-	16	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-20	A
Pulse diode forward current (t = 100 μs)	I _{SM}		-	-	-50	
Body diode voltage	V _{SD}	I _S = -8.4 A, V _{GS} = 0 V	-	-0.85	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -8.4 A, di/dt = 100 A/μs, T _J = 25 °C	-	34	60	ns
Body diode reverse recovery charge	Q _{rr}		-	22	40	nC
Reverse recovery fall time	t _a		-	11	-	ns
Reverse recovery rise time	t _b		-	23	-	

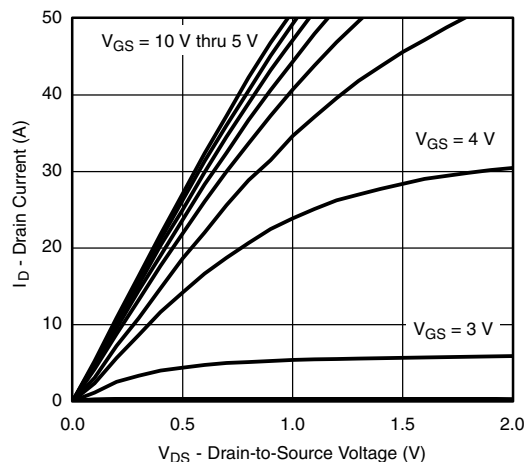
Notes

- a. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

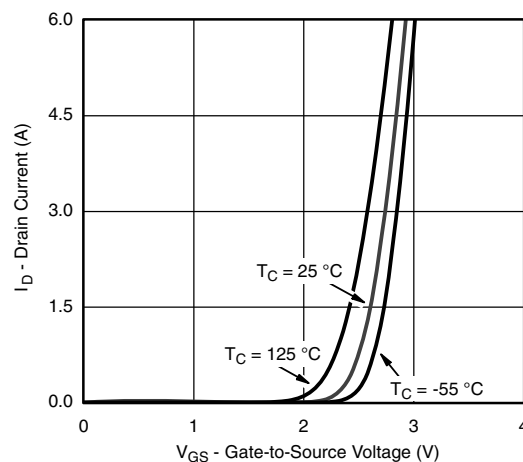
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



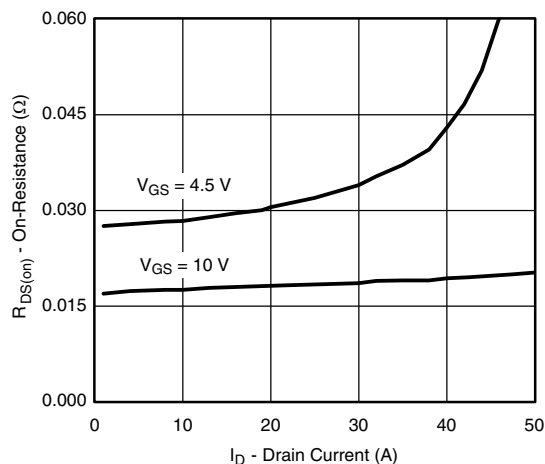
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



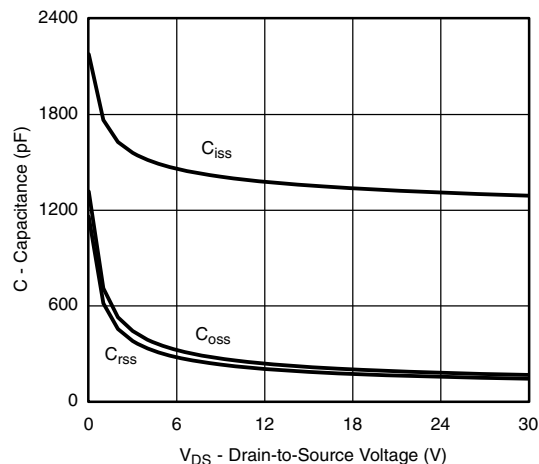
Output Characteristics



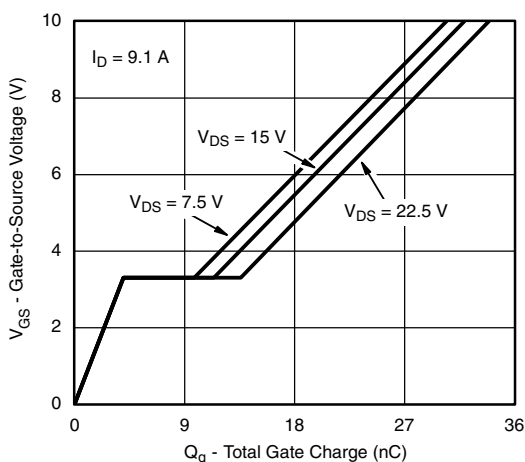
Transfer Characteristics



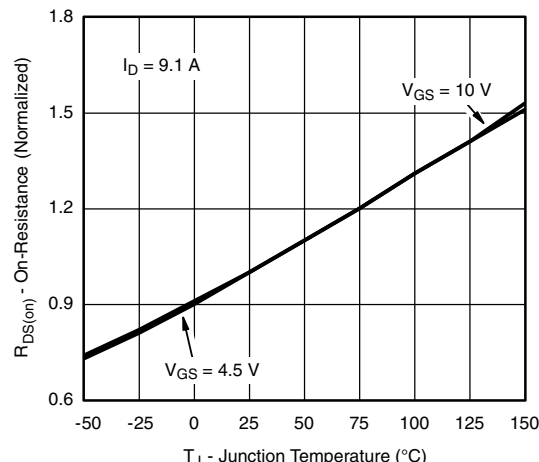
On-Resistance vs. Drain Current



Capacitance



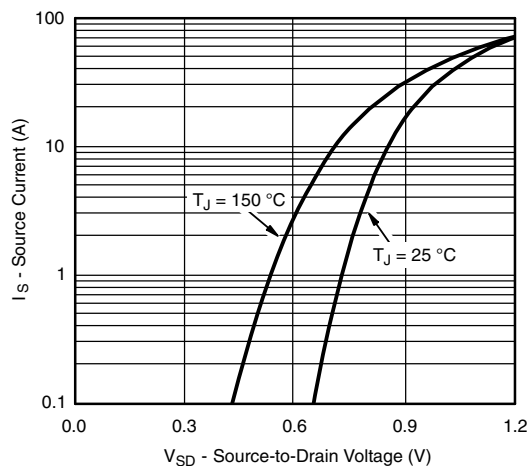
Gate Charge



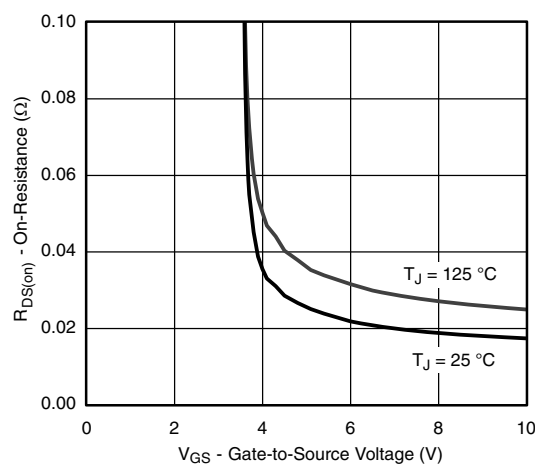
On-Resistance vs. Junction Temperature



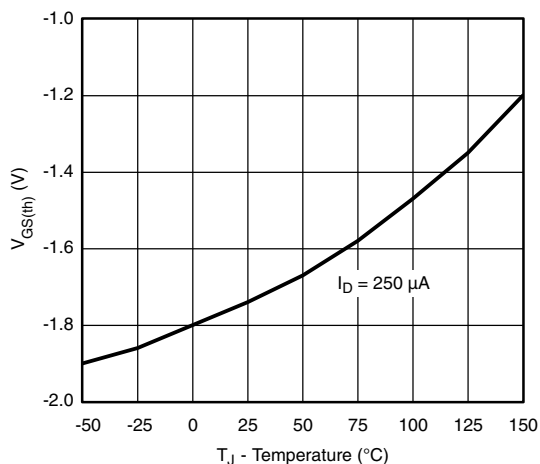
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



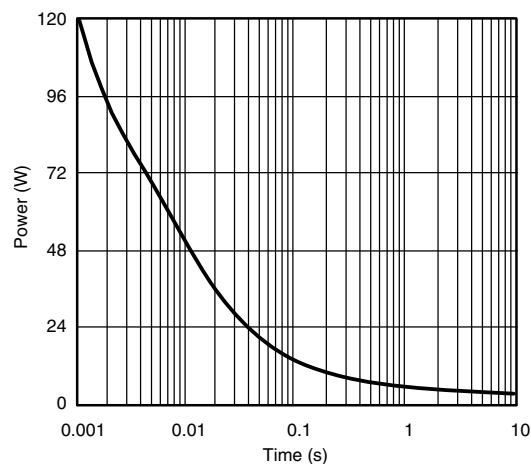
Source-Drain Diode Forward Voltage



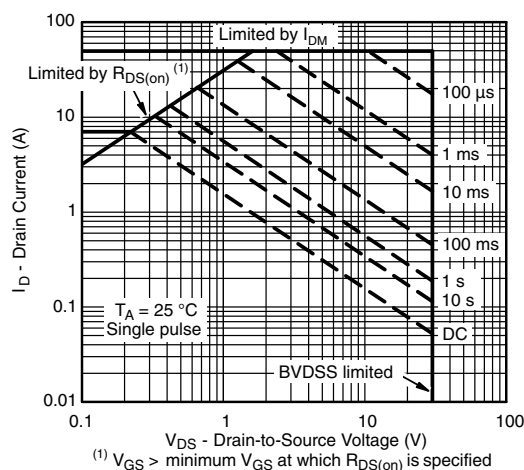
On-Resistance vs. Gate-to-Source Voltage



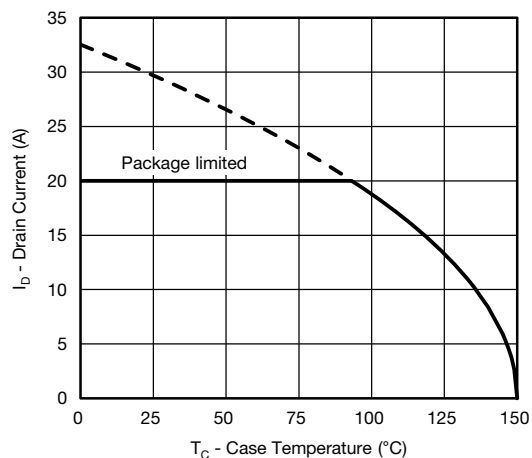
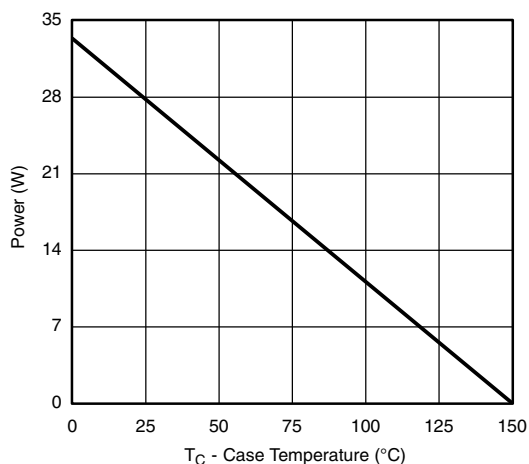
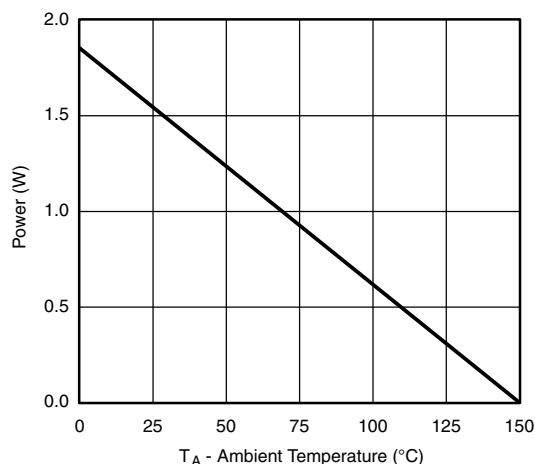
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



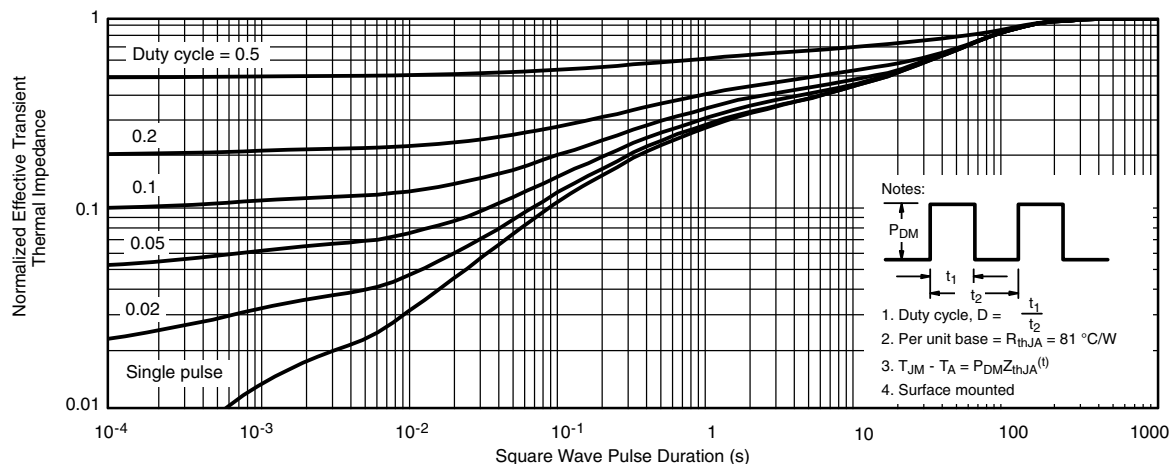
Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power Derating, Junction-to-Ambient
Note

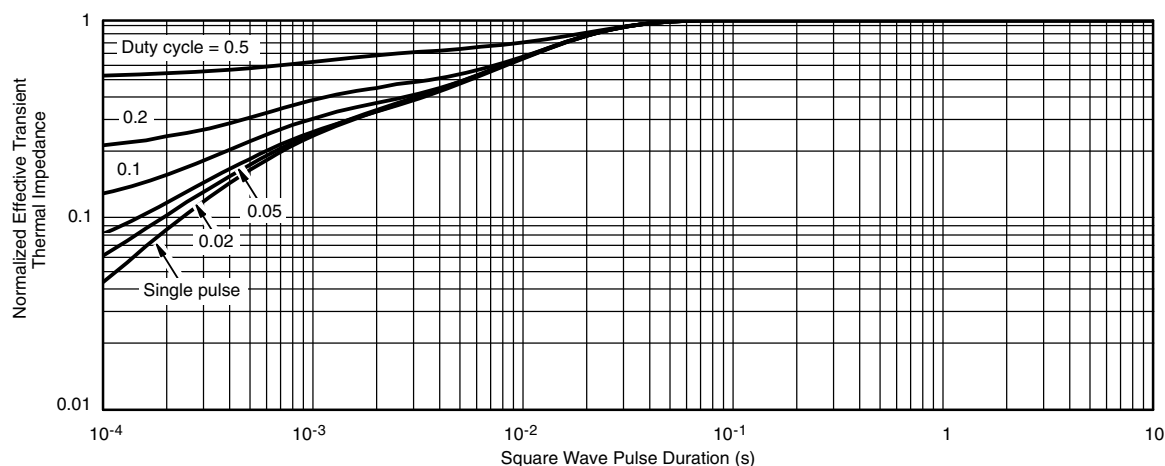
- c. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

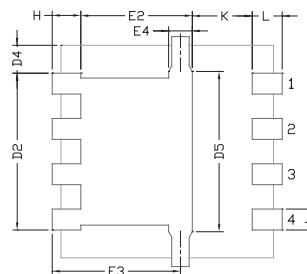
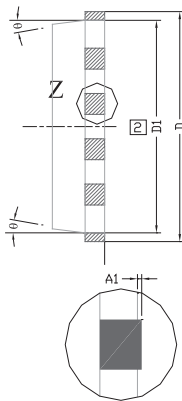
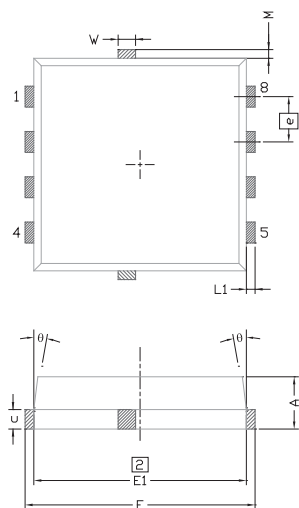


Normalized Thermal Transient Impedance, Junction-to-Case

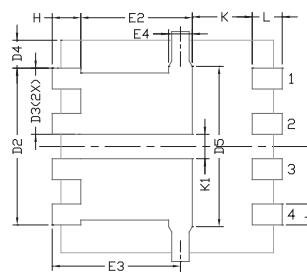
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PowerPAK® 1212-8T



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

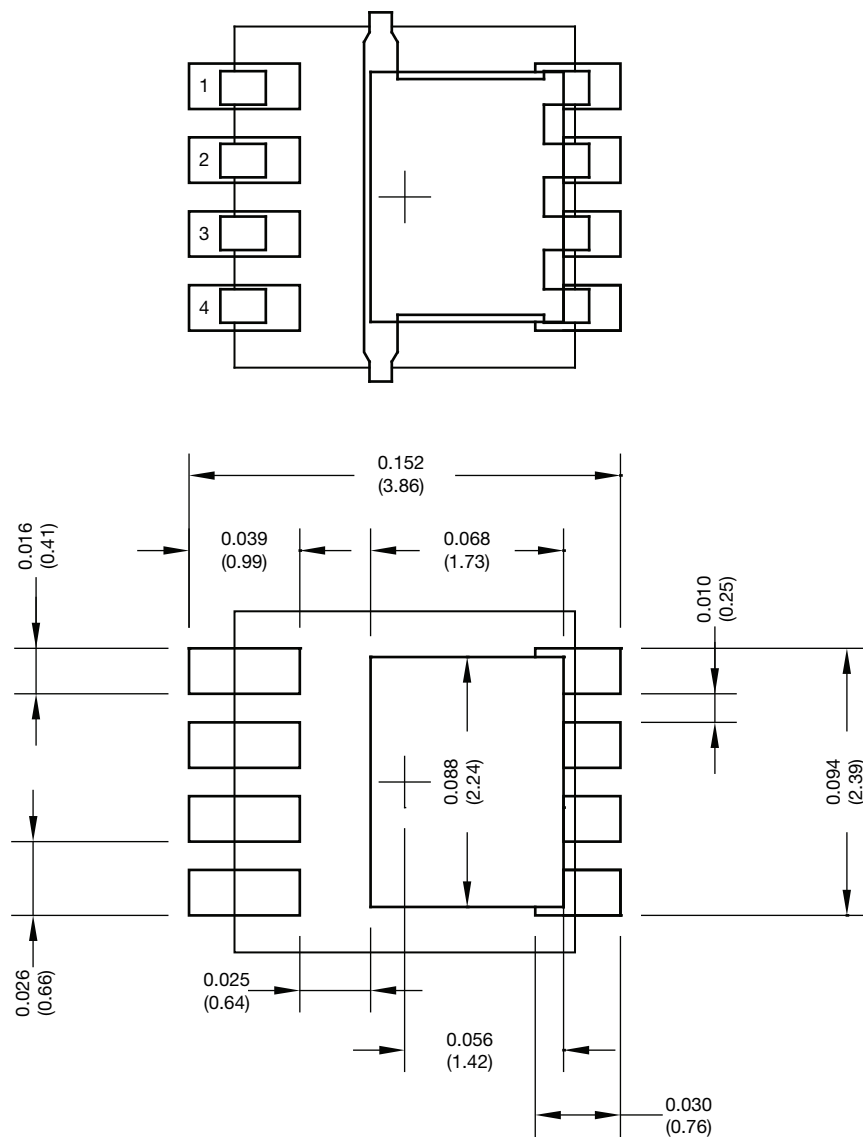
NOTE:	
1	MILLIMETER WILL GOVERN
2	DIMENSIONS EXCLUSIVE OF MOLD GATE BURRS.
3	DIMENSIONS EXCLUSIVE OF MOLD FLASH AND CUTTING BURRS.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
e	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T13-0056-Rev. A, 18-Feb-13

DWG: 6012

Recommended Minimum PADs for Thin PowerPAK® 1212-8T





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