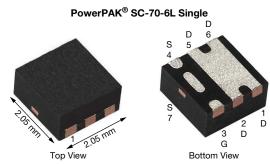


# N-Channel 25 V (D-S) MOSFET

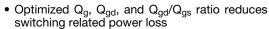


Marking code: A5

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	25								
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.0056								
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.0075								
Q <sub>g</sub> typ. (nC)	7.4								
I <sub>D</sub> (A)	40 <sup>a, g</sup>								
Configuration	Single								

#### **FEATURES**

TrenchFET® Gen IV power MOSFET





Provides exceptional versatility for power management design

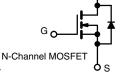
HALOGEN FREE

- Very low R<sub>DS(on)</sub> and excellent R<sub>DS</sub> Q<sub>g</sub> Figure-of-Merit (FOM) in an ultra-compact package footprint
- Optimized for high frequency switching
- Optimized for high-frequency switching
- 100 % R<sub>a</sub> and UIS tested
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### **APPLICATIONS**

- Synchronous rectification
- High power density DC/DC
- · Synchronous buck converter





· Battery charging and management

ORDERING INFORMATION	
Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiAA00DJ-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V <sub>DS</sub>	25	V		
Gate-source voltage		V <sub>GS</sub>	+16 / -12			
	T <sub>C</sub> = 25 °C		40 a			
Continuous dusin summent (T. 150 °C)	T <sub>C</sub> = 70 °C	1 . —	40 <sup>a</sup>			
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	20.1 <sup>b, c</sup>			
	T <sub>A</sub> = 70 °C		16.1 <sup>b, c</sup>	Α		
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	80			
Continuous source dusin diada surrent	T <sub>C</sub> = 25 °C		16			
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.9 <sup>b, c</sup>			
	T <sub>C</sub> = 25 °C		19.2			
Maximum navvay discination	T <sub>C</sub> = 70 °C		12.3	W		
Maximum power dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5 b, c	VV		
	T <sub>A</sub> = 70 °C		2.2 b, c			
Operating junction and storage temperature	range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C		
Soldering recommendations (peak tempera	ture) <sup>c</sup>		260			

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient <sup>b</sup>	t ≤ 10 s	R <sub>thJA</sub>	28	36	°C/W				
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	5.3	6.5	C/VV				

#### Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 80 °C/W
- g.  $T_C = 25$  °C



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# Vishay Siliconix

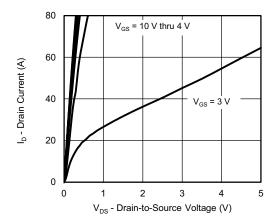
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•		•	
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA	-	16.9	-	1400
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4.2	_	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	-	2.5	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = +16 / -12 \text{ V}$	-	-	100	nA
7	I <sub>DSS</sub>	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ
Zero gate voltage drain current		V <sub>DS</sub> =25 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α
Delta de la contra del contra de la contra del la contra de la contra de la contra de la contra del la contra de la contra de la contra del la contra de la contra de la contra de la contra del la contra del la contra de la contra de la contra del la c	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	0.0046	0.0056	
Drain-source on-state resistance <sup>a</sup>		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0060	0.0075	Ω
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	-	66	-	S
Dynamic <sup>b</sup>			•	1	•	•
Input capacitance	C <sub>iss</sub>		-	1090	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 12.5 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	475	-	рF
Reverse transfer capacitance	C <sub>rss</sub>		-	50	-	
Table and a decide and	0	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	15.7	24	
Total gate charge	Qg		-	7.4	11.1	
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 12.5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	3	-	nC
Gate-drain charge	$Q_{gd}$		-	1.6	-	
Gate resistance	$R_g$	f = 1 MHz	0.25	1.25	2.5	Ω
Turn-on delay time	t <sub>d(on)</sub>		-	10	20	
Rise time	t <sub>r</sub>	$V_{DD} = 12.5 \text{ V}, R_L = 0.8 \Omega, I_D \cong 16 \text{ A},$	-	30	46	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	16	36	
Fall time	t <sub>f</sub>		-	10	20	
Turn-on delay time	t <sub>d(on)</sub>		-	15	30	ns
Rise time	t <sub>r</sub>	$V_{DD}$ = 12.5 V, $R_L$ = 0.8 $\Omega$ , $I_D \cong$ 16 A,	-	65	100	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$	-	15	30	
Fall time	, ,					
Drain-Source Body Diode Characteristi	cs					•
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	16	_
Pulse diode forward current	I <sub>SM</sub>		-	-	80	A
Body diode voltage	$V_{SD}$	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.75	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>		-	23.2	35	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	L E A di/d+ 100 A / T 05 00	-	13	26	nC
Reverse recovery fall time	ta	$I_F = 5 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	11.5	-	
Reverse recovery rise time	t <sub>b</sub>		-	11.7	-	ns

#### Notes

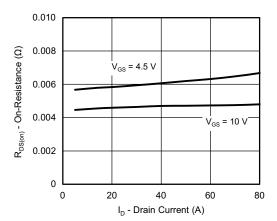
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

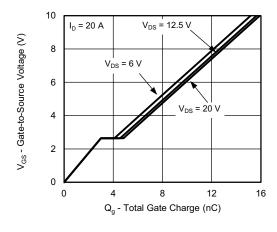




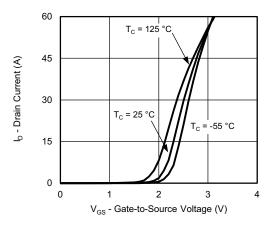
#### **Output Characteristics**



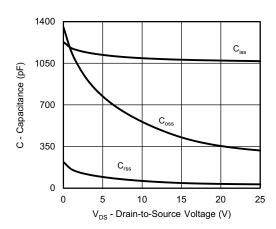
On-Resistance vs. Drain Current and Gate Voltage



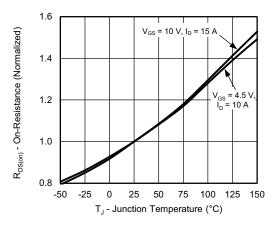
**Gate Charge** 



**Transfer Characteristics** 

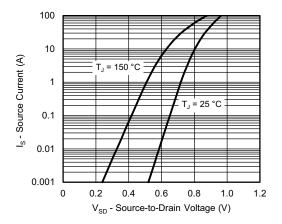


Capacitance

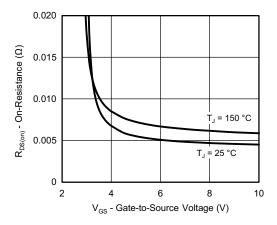


On-Resistance vs. Junction Temperature

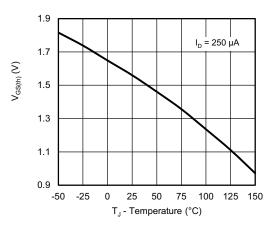




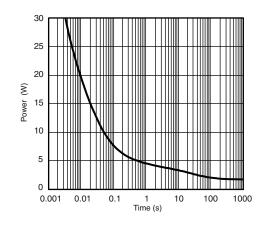
Source-Drain Diode Forward Voltage



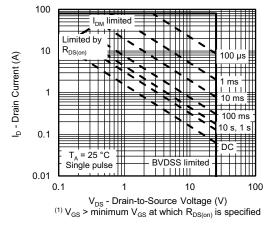
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

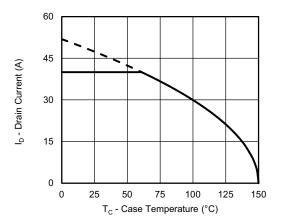


Single Pulse Power, Junction-to-Ambient

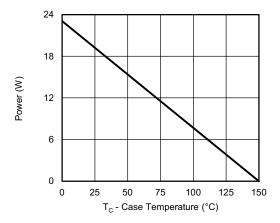


Safe Operating Area, Junction-to-Ambient

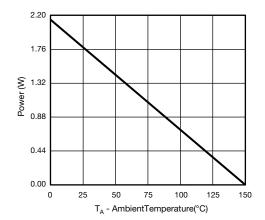




#### Current Derating a





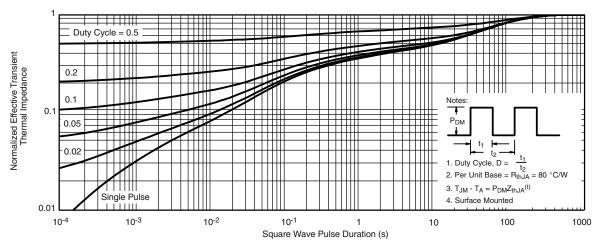


Power, Junction-to-Ambient

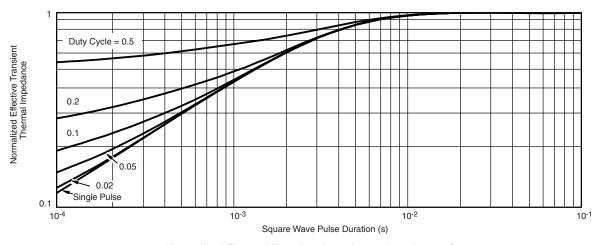
#### Note

a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Vishay Siliconix

# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

			SINGL	LE PAD			DUAL PAD						
DIM	M	ILLIMETER	RS		INCHES		M	ILLIMETER	RS		INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	,	0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP		0.275 TYP			0.011 TYP			
K1		0.400 TYP	1		0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP	1		0.009 TYP			0.252 TYP			0.010 TYP		
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP	1	0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
ECNI- C C	7404 D	. 0 00 1	. 07										

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

Document Number: 73001 06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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Vishay

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