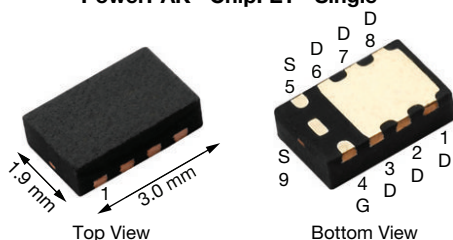


## P-Channel 20 V (D-S) MOSFET

### PRODUCT SUMMARY

| V <sub>DS</sub> (V) | R <sub>DS(on)</sub> (Ω)           | I <sub>D</sub> (A) <sup>a</sup> | Q <sub>g</sub> (TYP.) |
|---------------------|-----------------------------------|---------------------------------|-----------------------|
| -20                 | 0.052 at V <sub>GS</sub> = -4.5 V | -8 <sup>e</sup>                 | 8                     |
|                     | 0.082 at V <sub>GS</sub> = -2.5 V | -7.5                            |                       |

**PowerPAK® ChipFET® Single**


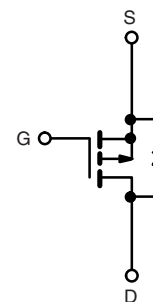
### FEATURES

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load switch
- HDD DC/DC



P-Channel MOSFET

### Ordering Information:

Si5459DU-T1-GE3 (Lead (Pb)-free and halogen-free)

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

| PARAMETER  | SYMBOL                            | LIMIT                  | UNIT                 |
|--|-----------------------------------|------------------------|----------------------|
| Drain-Source Voltage   | V <sub>DS</sub>                   | -20                    | V                    |
| Gate-Source Voltage  | V <sub>GS</sub>                   | ± 12                   |                      |
| Continuous Drain Current (T <sub>J</sub> = 150 °C)           | I <sub>D</sub>                    | T <sub>C</sub> = 25 °C | A                    |
|  |                                   | T <sub>C</sub> = 70 °C |                      |
|  |                                   | T <sub>A</sub> = 25 °C |                      |
|  |                                   | T <sub>A</sub> = 70 °C |                      |
| Pulsed Drain Current (10 μs pulse width)                     | I <sub>DM</sub>                   | -20                    | A                    |
| Source-Drain Current Diode Current                           | I <sub>S</sub>                    | T <sub>C</sub> = 25 °C |                      |
|  |                                   | T <sub>A</sub> = 25 °C | -2.9 <sup>b, c</sup> |
| Maximum Power Dissipation                                    | P <sub>D</sub>                    | T <sub>C</sub> = 25 °C | W                    |
|  |                                   | T <sub>C</sub> = 70 °C |                      |
|  |                                   | T <sub>A</sub> = 25 °C |                      |
|  |                                   | T <sub>A</sub> = 70 °C |                      |
| Operating Junction and Storage Temperature Range             | T <sub>J</sub> , T <sub>stg</sub> | -50 to 150             | °C                   |
| Soldering Recommendations (Peak temperature) <sup>d, e</sup> |                                   | 260                    |                      |

### THERMAL RESISTANCE RATINGS

| PARAMETER                                   | SYMBOL            | LIMIT   |         | UNIT |
|---|-------------------|---------|---------|------|
|   |                   | TYPICAL | MAXIMUM |      |
| Maximum Junction-to-Ambient <sup>b, d</sup> | R <sub>thJA</sub> | 30      | 36      | °C/W |
| Maximum Junction-to-Case (Drain)            | R <sub>thJC</sub> | 9.5     | 11.5    |      |

### Notes

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 72 °C/W.
- Package limited.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.



| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                                      |   |      |                   |       |       |
|---|--------------------------------------|---|------|-------------------|-------|-------|
| PARAMETER   | SYMBOL                               | TEST CONDITIONS   | MIN. | TYP. <sup>a</sup> | MAX.  | UNIT  |
| Static  |                                      |   |      |                   |       |       |
| Drain-Source Breakdown Voltage                                  | V <sub>DS</sub>                      | V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA   | -20  | -                 | -     | V     |
| V <sub>DS</sub> Temperature Coefficient                         | ΔV <sub>DS</sub> /T <sub>J</sub>     | I <sub>D</sub> = -250 μA  | -    | -19               | -     | mV/°C |
| V <sub>GS(th)</sub> Temperature Coefficient                     | ΔV <sub>GS(th)</sub> /T <sub>J</sub> |   | -    | 3.1               | -     |       |
| Gate Threshold Voltage  | V <sub>GS(th)</sub>                  | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA  | -0.6 | -                 | -1.4  | V     |
| Gate-Body Leakage   | I <sub>GSS</sub>                     | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V   | -    | -                 | -100  | nA    |
| Zero Gate Voltage Drain Current                                 | I <sub>DSS</sub>                     | V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V  | -    | -                 | -1    | μA    |
|   |                                      | V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C  | -    | -                 | -10   |       |
| On-State Drain Current <sup>b</sup>                             | I <sub>D(on)</sub>                   | V <sub>DS</sub> = ≤ -5 V, V <sub>GS</sub> = -10 V   | -20  | -                 | -     | A     |
| Drain-Source On-State Resistance <sup>b</sup>                   | R <sub>DS(on)</sub>                  | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.7 A   | -    | 0.043             | 0.052 | Ω     |
|   |                                      | V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1 A   | -    | 0.068             | 0.082 |       |
| Forward Transconductance <sup>b</sup>                           | g <sub>fs</sub>                      | V <sub>DS</sub> = -10 V, I <sub>D</sub> = -6.7 A  | -    | 11                | -     | S     |
| Dynamic <sup>a</sup>  |                                      |   |      |                   |       |       |
| Input Capacitance   | C <sub>iss</sub>                     | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz   | -    | 665               | -     | pF    |
| Output Capacitance  | C <sub>oss</sub>                     |   | -    | 140               | -     |       |
| Reverse Transfer Capacitance                                    | C <sub>rss</sub>                     |   | -    | 115               | -     |       |
| Total Gate Charge   | Q <sub>g</sub>                       | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.7 A   | -    | 17                | 26    | nC    |
|   |                                      | V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.7 A  | -    | 8                 | 12    |       |
| Gate-Source Charge  | Q <sub>gs</sub>                      |   | -    | 2                 | -     |       |
| Gate-Drain Charge   | Q <sub>gd</sub>                      |   | -    | 3                 | -     |       |
| Gate Resistance   | R <sub>g</sub>                       | f = 1 MHz   | 1.2  | 6                 | 12    | Ω     |
| Turn-On Delay Time  | t <sub>d(on)</sub>                   | V <sub>DD</sub> = -10 V, R <sub>L</sub> = 1.9 Ω<br>I <sub>D</sub> ≅ -5.3 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω  | -    | 6                 | 12    | ns    |
| Rise Time   | t <sub>r</sub>                       |   | -    | 15                | 23    |       |
| Turn-Off Delay Time   | t <sub>d(off)</sub>                  |   | -    | 26                | 39    |       |
| Fall Time   | t <sub>f</sub>                       |   | -    | 9                 | 18    |       |
| Turn-On Delay Time  | t <sub>d(on)</sub>                   | V <sub>DD</sub> = -10 V, R <sub>L</sub> = 1.9 Ω<br>I <sub>D</sub> ≅ -5.3 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω | -    | 21                | 32    |       |
| Rise Time   | t <sub>r</sub>                       |   | -    | 50                | 75    |       |
| Turn-Off Delay Time   | t <sub>d(off)</sub>                  |   | -    | 29                | 44    |       |
| Fall Time   | t <sub>f</sub>                       |   | -    | 13                | 20    |       |
| Drain-Source Body Diode Characteristics                         |                                      |   |      |                   |       |       |
| Continuous Source-Drain Diode Current                           | I <sub>S</sub>                       | T <sub>C</sub> = 25 °C  | -    | -                 | -8    | A     |
| Pulse Diode Forward Current <sup>a</sup>                        | I <sub>SM</sub>                      |   | -    | -                 | -20   |       |
| Body Diode Voltage  | V <sub>SD</sub>                      | I <sub>S</sub> = -5.3 A   | -    | -0.77             | -1.2  | V     |
| Body Diode Reverse Recovery Time                                | t <sub>rr</sub>                      | I <sub>F</sub> = -5.3 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C   | -    | 30                | 45    | ns    |
| Body Diode Reverse Recovery Charge                              | Q <sub>rr</sub>                      |   | -    | 17                | 26    | nC    |
| Reverse Recovery Fall Time                                      | t <sub>a</sub>                       |   | -    | 16                | -     | ns    |
| Reverse Recovery Rise Time                                      | t <sub>b</sub>                       |   | -    | 14                | -     |       |

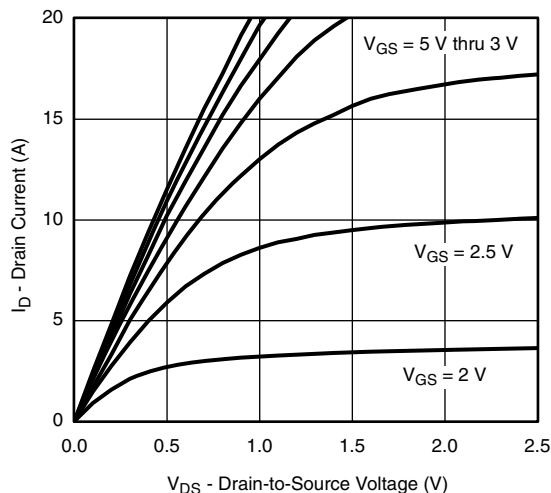
**Notes**

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

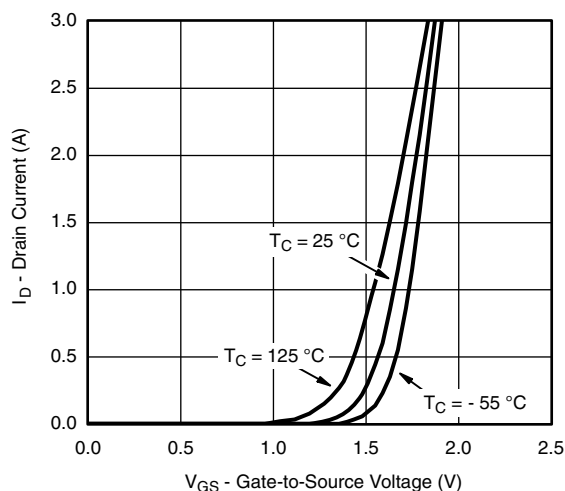
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



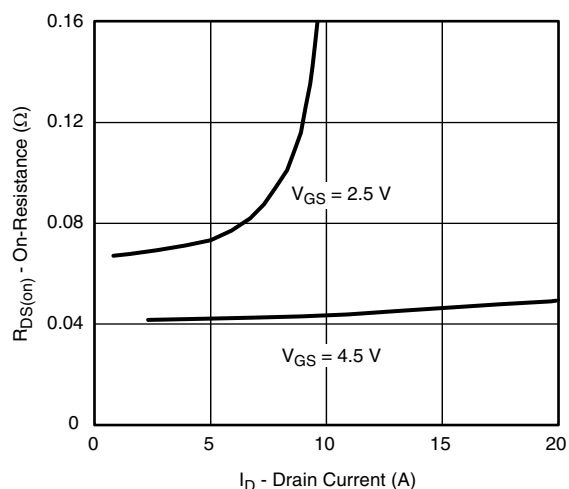
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



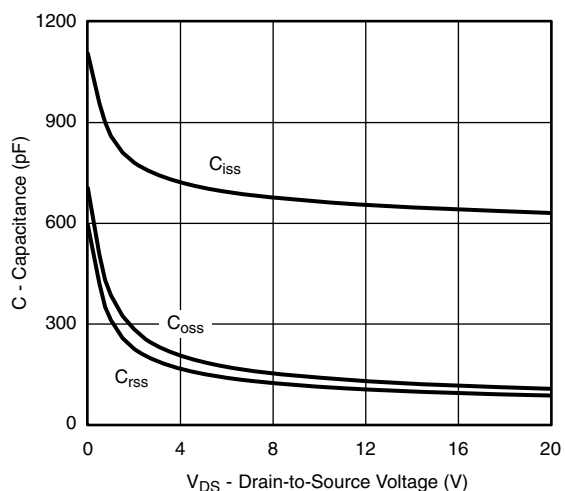
**Output Characteristics**



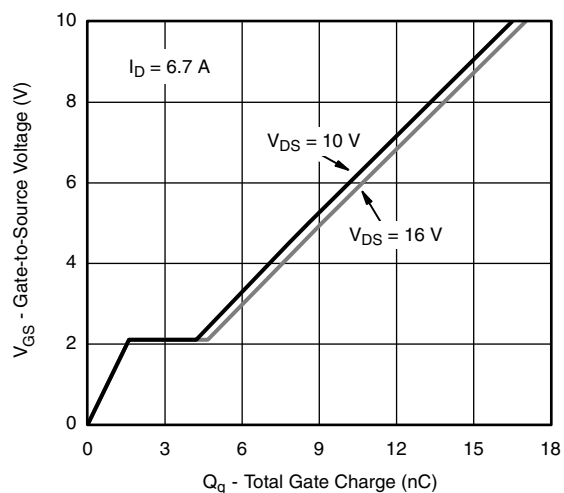
**Transfer Characteristics**



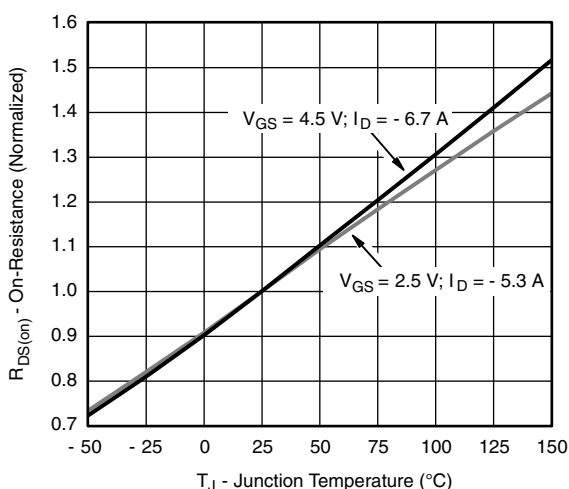
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



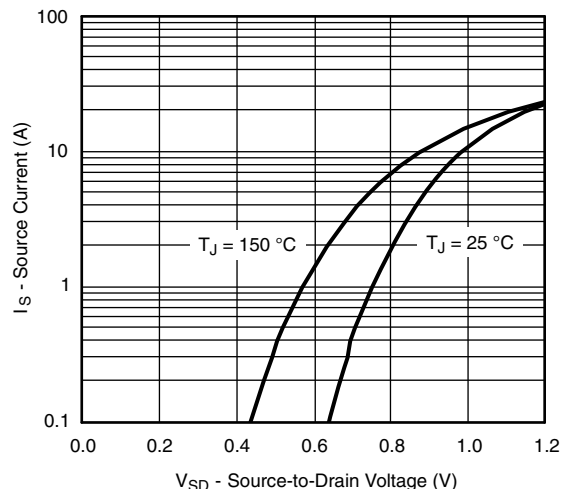
**Gate Charge**



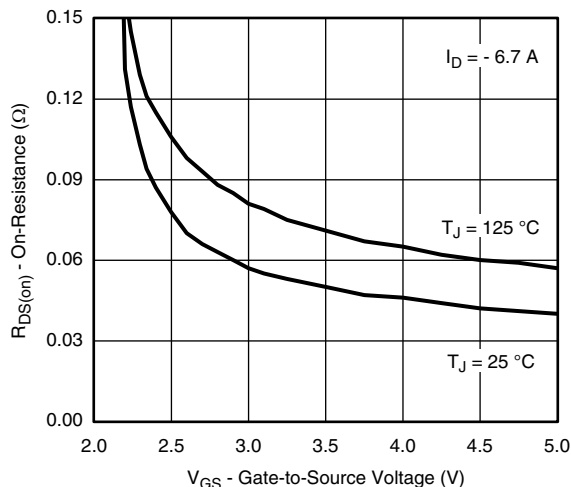
**On-Resistance vs. Junction Temperature**



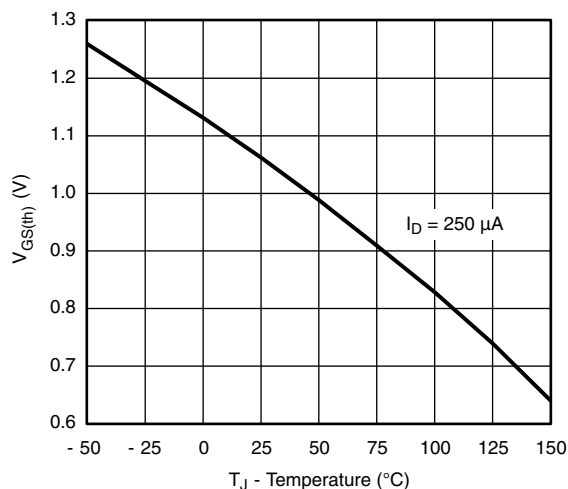
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



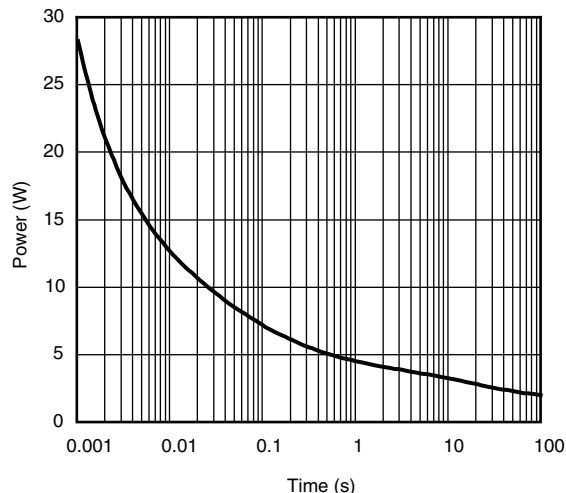
**Source-Drain Diode Forward Voltage**



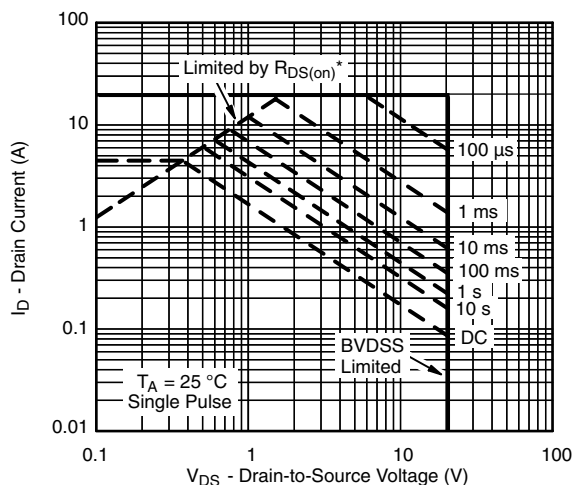
**On-Resistance vs. Gate-to-Source Voltage**



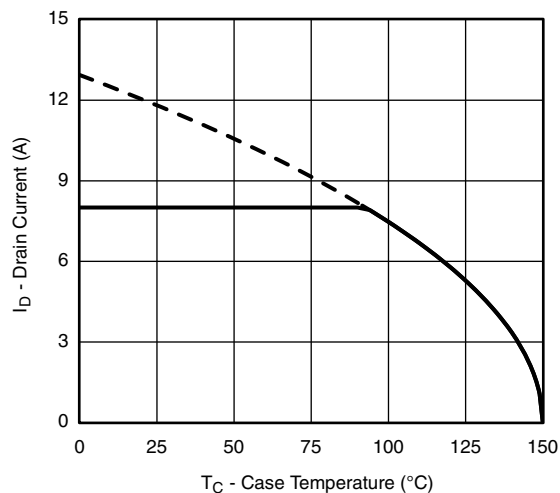
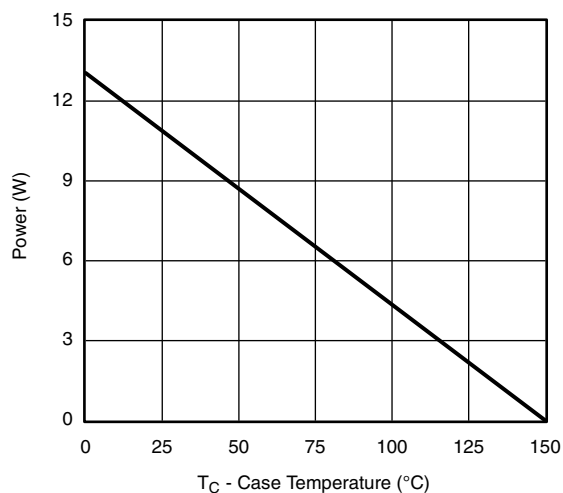
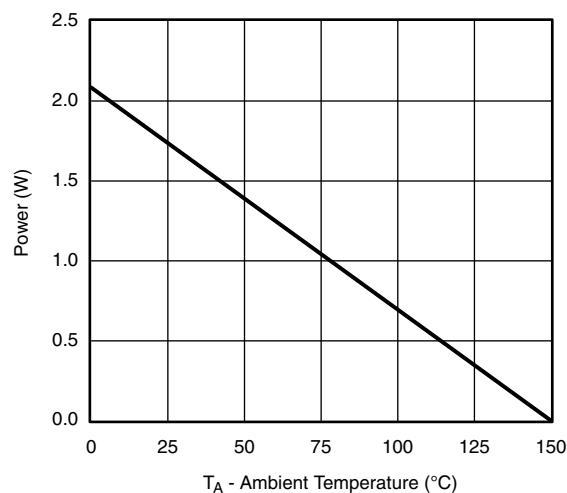
**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



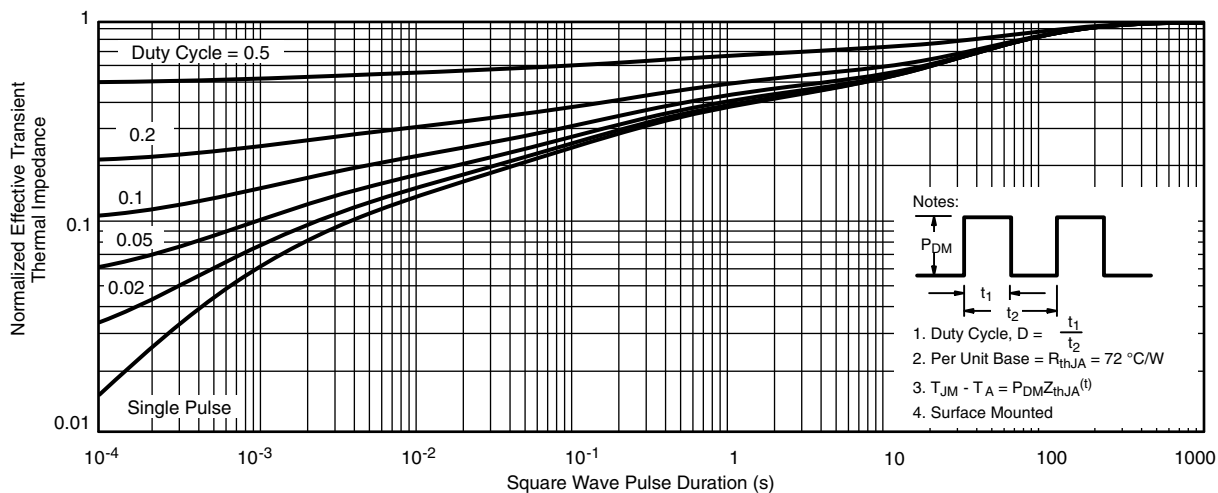
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating <sup>a</sup>**

**Power Derating, Junction-to-Case**

**Power Derating, Junction-to-Ambient**
**Note**

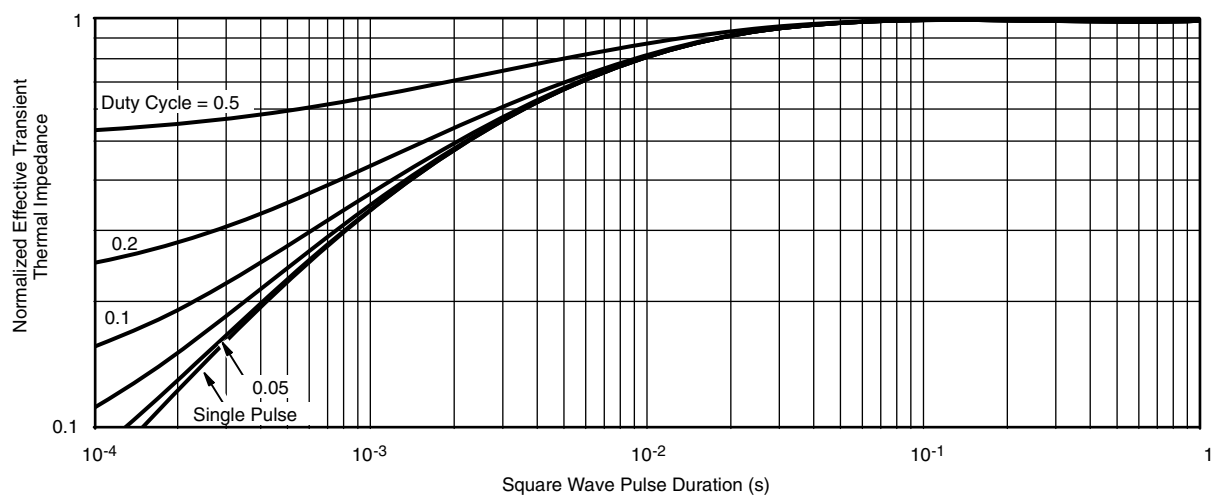
- a. The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



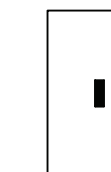
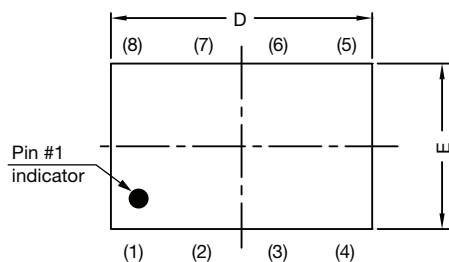
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65017](http://www.vishay.com/ppg?65017).

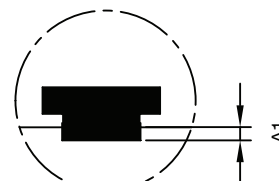
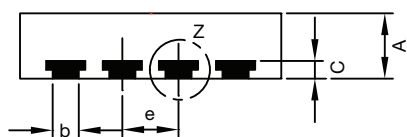
## PowerPAK® ChipFET® Case Outline



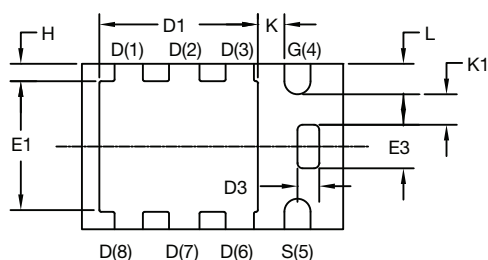
Side view of single



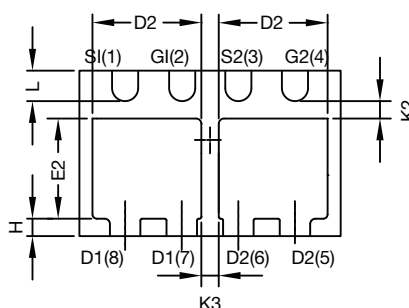
Side view of dual



Detail Z



Backside view of single pad



Backside view of dual pad

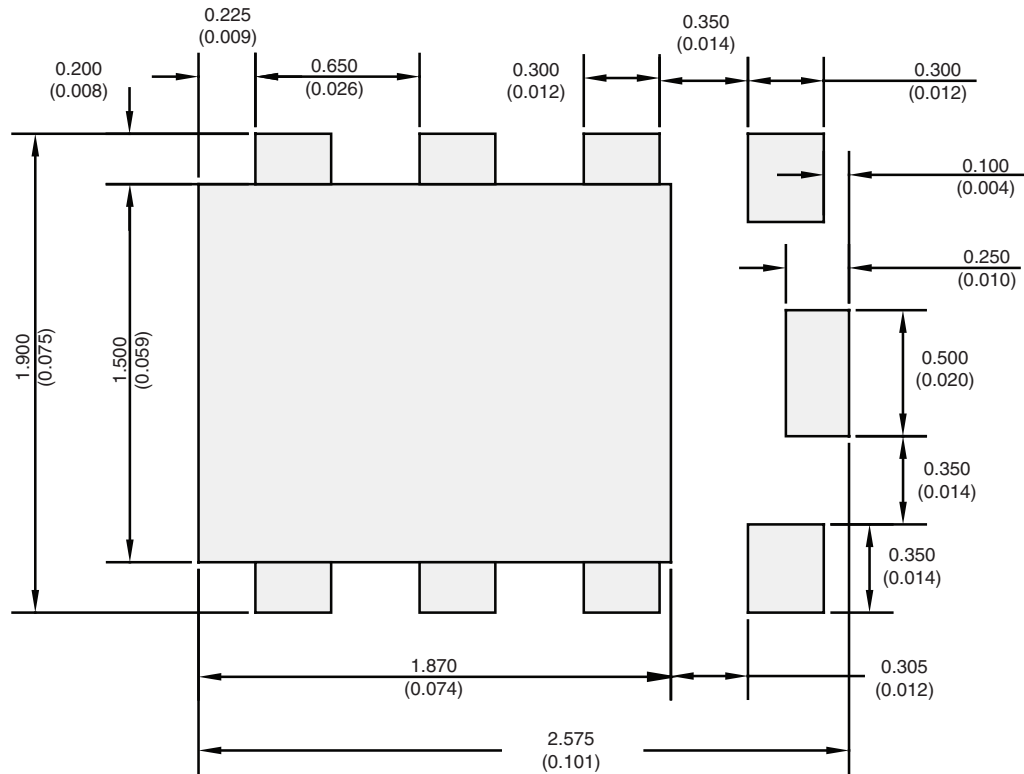
| DIM. | MILLIMETERS |      |      | INCHES    |       |       |
|------|-------------|------|------|-----------|-------|-------|
|      | MIN.        | NOM. | MAX. | MIN.      | NOM.  | MAX.  |
| A    | 0.70        | 0.75 | 0.85 | 0.028     | 0.030 | 0.033 |
| A1   | 0           | -    | 0.05 | 0         | -     | 0.002 |
| b    | 0.25        | 0.30 | 0.35 | 0.010     | 0.012 | 0.014 |
| C    | 0.15        | 0.20 | 0.25 | 0.006     | 0.008 | 0.010 |
| D    | 2.92        | 3.00 | 3.08 | 0.115     | 0.118 | 0.121 |
| D1   | 1.75        | 1.87 | 2.00 | 0.069     | 0.074 | 0.079 |
| D2   | 1.07        | 1.20 | 1.32 | 0.042     | 0.047 | 0.052 |
| D3   | 0.20        | 0.25 | 0.30 | 0.008     | 0.010 | 0.012 |
| E    | 1.82        | 1.90 | 1.98 | 0.072     | 0.075 | 0.078 |
| E1   | 1.38        | 1.50 | 1.63 | 0.054     | 0.059 | 0.064 |
| E2   | 0.92        | 1.05 | 1.17 | 0.036     | 0.041 | 0.046 |
| E3   | 0.45        | 0.50 | 0.55 | 0.018     | 0.020 | 0.022 |
| e    | 0.65 BSC    |      |      | 0.026 BSC |       |       |
| H    | 0.15        | 0.20 | 0.25 | 0.006     | 0.008 | 0.010 |
| K    | 0.25        | -    | -    | 0.010     | -     | -     |
| K1   | 0.30        | -    | -    | 0.012     | -     | -     |
| K2   | 0.20        | -    | -    | 0.008     | -     | -     |
| K3   | 0.20        | -    | -    | 0.008     | -     | -     |
| L    | 0.30        | 0.35 | 0.40 | 0.012     | 0.014 | 0.016 |

C14-0630-Rev. E, 21-Jul-14  
DWG: 5940

### Note

- Millimeters will govern

## RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads  
Dimensions in mm/(Inches)

[Return to Index](#)





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