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Vishay Siliconix

Automotive N-Channel 150 V (D-S) 175 °C MOSFET



Marking code: Q052

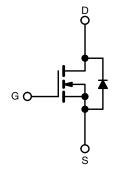
PRODUCT SUMMARY				
V _{DS} (V)	150			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0685			
I _D (A)	18			
Configuration	Single			

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8W
Lead (Pb)-free and halogen-free	SQSA70CENW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless	s otherwise noted	i)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	150		
Gate-source voltage		V_{GS}	± 20	V	
Continuous drain current a	T _C = 25 °C ^a	I-	18		
Continuous drain current "	T _C = 125 °C	I _D	11.2		
Continuous source current (diode conduction) a	I _S	18	Α		
Pulsed drain current ^b		I _{DM}	40		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	18		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	16.2	mJ	
Maximum power dissipation	T _C = 25 °C	P _D	62.5	W	
Maximum power dissipation	T _C = 125 °C		20		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	R_{thJA}	81	°C/W
Junction-to-case (drain)		R _{thJC}	2.4	C/VV

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V_{GS}	= 0, I _D = 250 μA	150	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		3.0	3.5	V
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	1	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 150 V	1	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 150 V, T _J = 125 °C	1	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 150 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	10	-	-	Α
		V _{GS} = 10 V	I _D = 7 A	-	0.0554	0.0685	
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 10 V	I _D = 7 A, T _J = 125 °C	-	-	0.1296	Ω
		V _{GS} = 10 V	I _D = 7 A, T _J = 175 °C	=	-	0.1602	
Forward transconductance b	9 _{fs}	V _{DS} = 15 V, I _D = 7 A		-	11	-	S
Dynamic ^b		•					
Input capacitance	C _{iss}			-	384	540	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	270	380	pF
Reverse transfer capacitance	C _{rss}			-	15	22	
Total gate charge ^c	Qg			1	8	12	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 75 \text{ V}, I_{D} = 2 \text{ A}$	-	2.1	-	nC
Gate-drain charge ^c	Q _{gd}			-	2.1	-	
Gate resistance	R _g	f = 1 MHz		0.80	1.61	2.41	Ω
Turn-on delay time ^c	t _{d(on)}			-	10	20	
Rise time ^c	t _r	V _{DD} =	75 V, R_L = 37.5 Ω	-	4	10	ns
Turn-off delay time ^c	t _{d(off)}	$I_D \cong 2 A, V$	$V_{\text{GEN}} = 10 \text{ V}, R_{\text{g}} = 1 \Omega$	-	16	30	
Fall time ^c	t _f	1		-	10	20	
Source-Drain Diode Ratings and Charact	eristic ^b						
Pulsed current ^a	I _{SM}			-		40	Α
Forward voltage	V _{SD}	I _F = 7 A, V _{GS} = 0 V		-	0.85	1.1	V
Body diode reverse recovery time	t _{rr}			1	43	90	ns
Body diode reverse recovery charge	Q _{rr}	- I _F = 2 A, di/dt = 100 A/μs		1	87	175	nC
Reverse recovery fall time	ta			-	38	-	ns
Reverse recovery rise time	t _b			-	5	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-3.9	-	Α

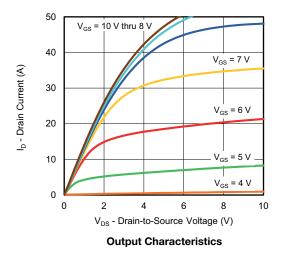
Notes

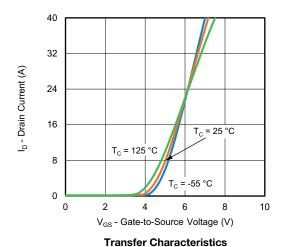
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

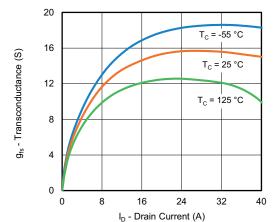
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

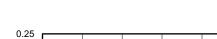


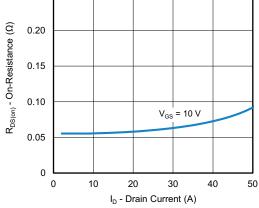
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



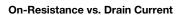


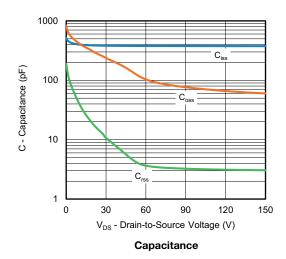


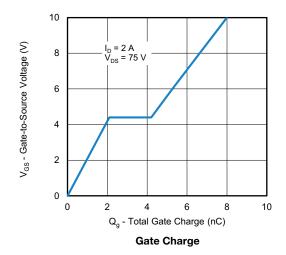






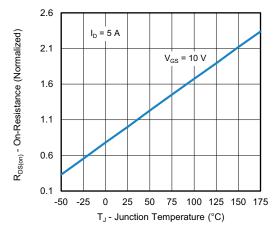




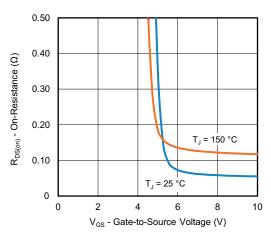




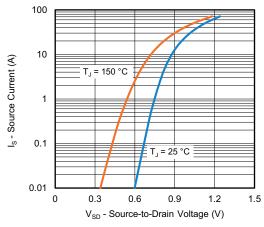
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



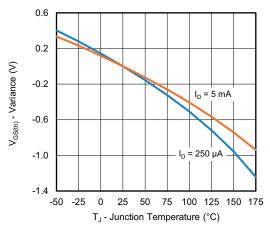
On-Resistance vs. Junction Temperature



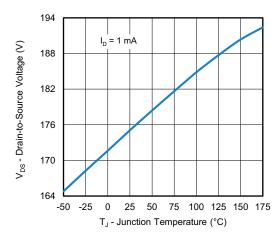
On-Resistance vs. Gate-to-Source Voltage



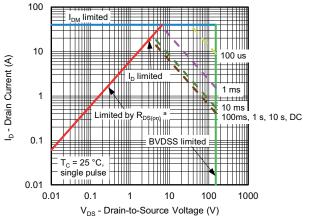
Source Drain Diode Forward Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



Safe Operating Area

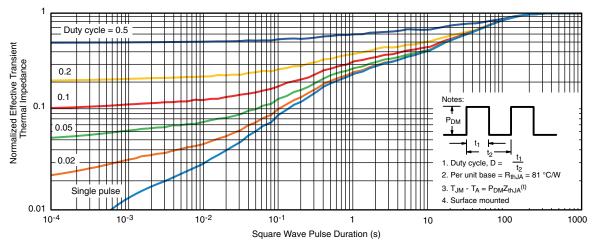
Note

a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

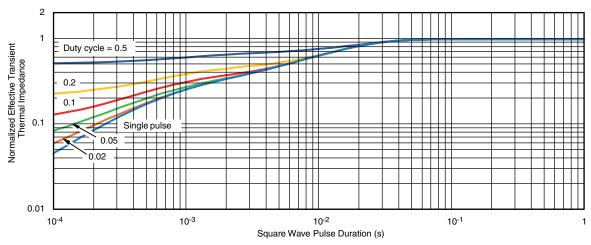
For technical questions, contact: automostech



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

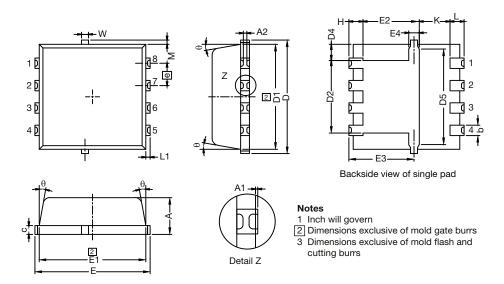
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 - are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63002.



PowerPAK® 1212-8W Case Outline



DIM.		MILLIMETERS		INCHES			
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1	0	-	0.05	0	-	0.002	
A2	0	-	0.13	0	-	0.005	
b	0.23	0.30	0.41	0.009	0.012	0.016	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
D4		0.47 typ.			0.0185 typ.		
D5		2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134	
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	1.75	1.85	1.98	0.069	0.073	0.078	
E4		0.34 typ.		0.013 typ.			
е		0.65 BSC.		0.026 BSC			
K		0.86 typ.		0.034 typ.			
Н	0.30	0.41	0.51	0.012	0.016	0.020	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.				0.005 typ.		

DWC: 6020

DWG: 6032



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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