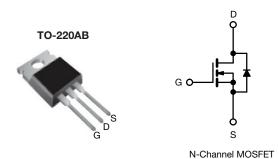


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	500			
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.85		
Q _g max. (nC)	39			
Q _{gs} (nC)	10			
Q _{gd} (nC)	19			
Configuration	Single			

FEATURES

- · Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V V_{GS} rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely high frequency operation
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

This new series of low charge power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free	IRF840LCPbF			
Lead (Pb)-free and halogen-free	IRF840LCPbF-BE3			

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	500	- V	
Gate-source voltage			V_{GS}	± 30		
Continuous drain current	V at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$,	8.0	А	
	V _{GS} at 10 V	T _C = 100 °C	I _D	5.1		
Pulsed drain current ^a			I _{DM}	28		
Linear derating factor				1.0	W/°C	
Single pulse avalanche energy b			E _{AS}	510	mJ	
Repetitive avalanche current a			I _{AR}	8.0	А	
Repetitive avalanche energy ^a			E _{AR}	13	mJ	
Maximum power dissipation	T _C = 25 °C		P_{D}	125	W	
Peak diode recovery dV/dt c			dV/dt	3.5	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^d	For	10 s	-	300		
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. $V_{DD}=50$ V, starting $T_J=25$ °C, L=14 mH, $R_g=25$ Ω , $I_{AS}=8.0$ A (see fig. 12) c. $I_{SD}\leq 8.0$ A, $I_{AS}=8.0$ A, $I_{AS}=8.0$ A (see fig. 12)
- d. 1.6 mm from case



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	1.0		

SPECIFICATIONS (T _J = 25 °C, u	SYMBOL	TEC	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	STWIBOL	TES	TEST CONDITIONS		IIF.	WAA.	ONIT
Drain-source breakdown voltage	V _{DS}	Vac	= 0 V, I _D = 250 μA	500	_	_	V
	$\Delta V_{DS}/T_{.1}$	<u> </u>	e to 25 °C, I _D = 1 mA	300	0.63	_	V/°C
V _{DS} temperature coefficient	50 0			2.0	-		V/ C
Gate-source threshold voltage	V _{GS(th)}		= V _{GS} , I _D = 250 μA	2.0	-	4.0	<u> </u>
Gate-source leakage	I _{GSS}		V _{GS} = ± 20 V			± 100	nA
Zero gate voltage drain current	I _{DSS}		= 500 V, V _{GS} = 0 V	-	-	25	μA
Drain course on state registance			$I_{D} = 4.8 \text{ A}^{\text{b}}$	-	-	250 0.85	0
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V				0.65	Ω
Forward transconductance	9fs	V _{DS} =	= 50 V, I _D = 4.8 A ^b	4.0	-	-	S
Dynamic		<u> </u>		T	1	I	T
Drain-source breakdown voltage	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0 MHz, see fig. 5		-	1100	-	pF
V _{DS} temperature coefficient	C _{oss}			-	170	-	
Gate-source threshold voltage	C _{rss}			-	18	-	
Gate-source leakage	Q_{g}			-	-	39	
Zero gate voltage drain current	Q_{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 8.0 \text{ A}, V_{DS} = 400 \text{ V}$ see fig. 6 and 13 b	-	-	10	nC	
Zero gate voltage drain current	Q_{gd}		see lig. o and to	-	-	19	
Drain-source on-state resistance	t _{d(on)}	$V_{DD} = 250 \text{ V, } I_D = 8.0 \text{ A,}$ $R_g = 9.1 \Omega, R_D = 30 \Omega$ see fig. $10^{\text{ b}}$		-	12	-	ns
Forward transconductance	t _r			-	25	-	
Drain-source breakdown voltage	t _{d(off)}			-	27	-	
V _{DS} temperature coefficient	t _f			-	19	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.7	-	3.7	Ω
Internal drain inductance	L _D	6 mm (0.25	Between lead, 6 mm (0.25") from		4.5	-	ml I
Internal source inductance	L _S	package and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.0	^
Pulsed diode forward current ^a	I _{SM}			-	-	28	A
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 8.0 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	$T_{J} = 25 ^{\circ}\text{C}, I_{F} = 8.0 \text{A},$		-	490	740	ns
Body diode reverse recovery charge	Q _{rr}	$dI/dt = 100 \text{ A/} \mu\text{s}^{\text{b}}$		-	3.0	4.5	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _I				<u> </u>	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

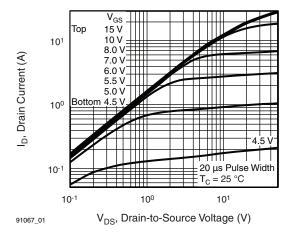


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

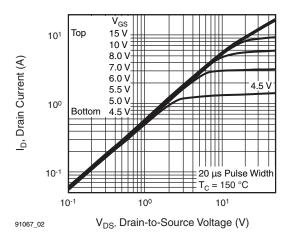


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

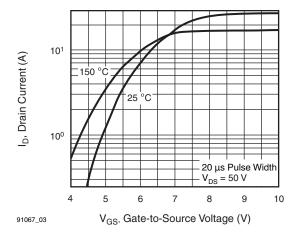


Fig. 3 - Typical Transfer Characteristics

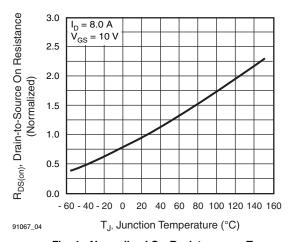


Fig. 4 - Normalized On-Resistance vs. Temperature

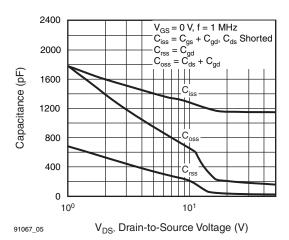


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

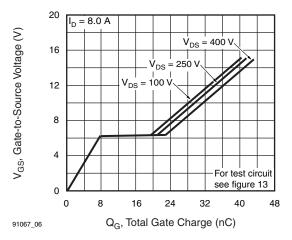


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



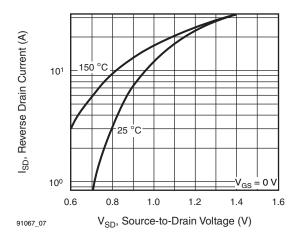


Fig. 7 - Typical Source-Drain Diode Forward Voltage

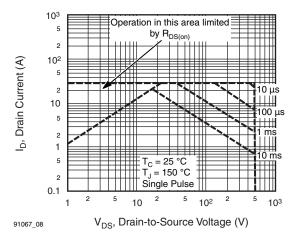


Fig. 8 - Maximum Safe Operating Area

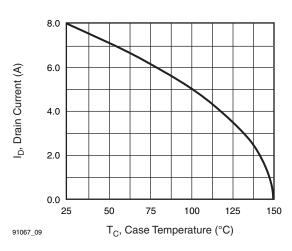


Fig. 9 - Maximum Drain Current vs. Case Temperature

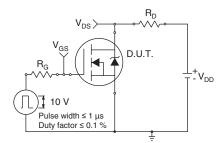


Fig. 10a - Switching Time Test Circuit

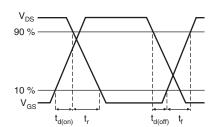


Fig. 10b - Switching Time Waveforms

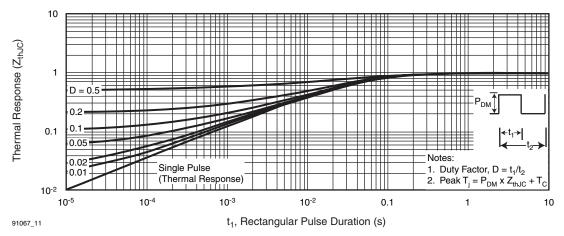


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



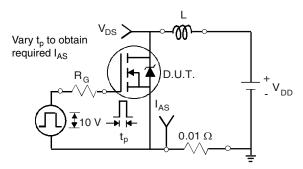


Fig. 12a - Unclamped Inductive Test Circuit

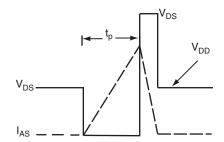


Fig. 12b - Unclamped Inductive Waveforms

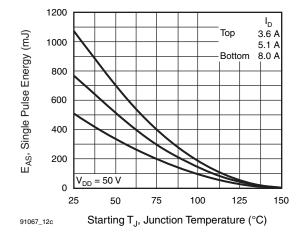


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

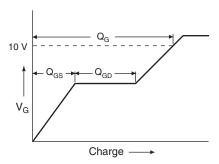


Fig. 13a - Basic Gate Charge Waveform

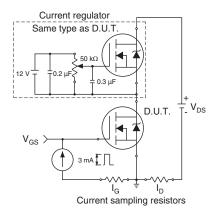
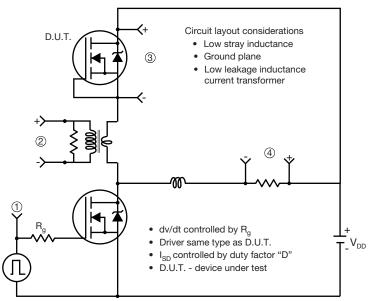


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



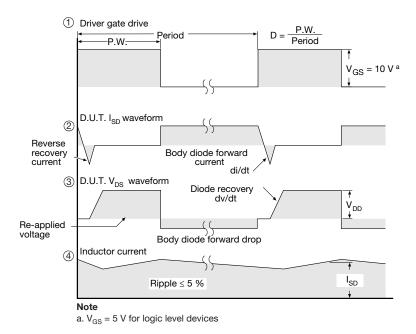


Fig. 14 - For N-Channel

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