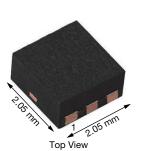


www.vishay.com

Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PowerPAK® SC-70-6L Single





Marking code: BL

PRODUCT SUMMARY									
V _{DS} (V)	-20								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.018								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5 \text{ V}$	0.026								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8 \text{ V}$	0.065								
Q _g typ. (nC)	20								
I _D (A) ^a	12								
Configuration	Single								

FEATURES

- TrenchFET® power MOSFET
- New thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
- 100 % R_g tested
- Built in ESD protection with Zener diode
- Typical ESD performance: 1800 V
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

P-Channel MOSFET

APPLICATIONS

- · Portable devices
 - Load switch
 - Battery switch
 - Charger switch



RoHS COMPLIANT HALOGEN

Configuration	Single		o D
ORDERING INFORMATION	ON		
Package		PowerPAK SC-70	
Lead (Pb)-free and halogen-free		SiA433EDJ-T1-GE3	

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unless	otherwise note	d)			
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V_{DS}	-20	V		
Gate-source voltage		V _{GS}	V _{GS} ± 12			
	T _C = 25 °C		-12 ^a			
Continuous drain surrent (T. 150 °C)	T _C = 70 °C		-12 ^a			
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	-11.3 ^{b, c}			
	T _A = 70 °C		-9.1 ^{b, c}	Α		
Pulsed drain current		I _{DM}	-50			
Continuous source-drain diode current	T _C = 25 °C		-12 ^a			
Continuous source-drain diode current	T _A = 25 °C	I _S	-2.9 ^{b, c}			
	T _C = 25 °C		19			
Maximum power dissipation	T _C = 70 °C		12	_ w		
	T _A = 25 °C	P _D	3.5 b, c	vv		
	T _A = 70 °C		2.2 b, c			
Operating junction and storage temperature ra	nge	T _J , T _{stg}	-55 to +150	°C		
Soldering recommendations (peak temperature	e) ^{d, e}		260			

THERMAL RESISTANCE RATINGS									
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT					
Maximum junction-to-ambient b, f	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.3	6.5	C/VV				

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 80 °C/W



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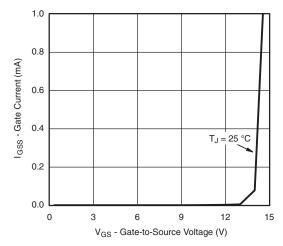
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -250 μA	-	-12	-	mV/°C
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	3	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-0.5	-	-1.2	V
Cata aguraa laakaga	1	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	± 20		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	-	-	± 0.5	μA
Zero gate voltage drain current	1	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μΑ
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-state drain current a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20	-	-	Α
		$V_{GS} = -4.5 \text{ V}, I_D = -7.6 \text{ A}$	-	0.015	0.018	Ω
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -6.3 \text{ A}$	-	0.021	0.026	
		V _{GS} = -1.8 V, I _D = -2.5 A				
Forward transconductance a	9 _{fs}	$V_{DS} = -10 \text{ V}, I_D = -7.6 \text{ A}$	-	35	-	S
Dynamic ^b						
Total gate charge		V _{DS} = -10 V, V _{GS} = -8 V, I _D = -11 A	-	50	75	nC
Gate-source charge	Q _g		-	20	30	
Gate-source charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -11 \text{ A}$	-	3.3	1	
Gate-drain charge	Q_{gd}		-	8.4	ı	
Gate resistance	R_g	f = 1 MHz	200	1000	2000	Ω
Turn-on delay time	t _{d(on)}		-	0.71	1.1	
Rise time	t _r	V_{DD} = -10 V, R_L = 1 Ω	-	1.7	2.6	
Turn-off delay time	t _{d(off)}	$I_D \cong$ -9 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	6	9	
Fall time	t _f		-	3.2	5	μs
Turn-on delay time	t _{d(on)}		-	0.3	0.45	μδ
Rise time	t _r	V_{DD} = -10 V , R_L = 1 Ω	-	0.6	0.9	
Turn-off delay time	t _{d(off)}	$I_D\cong$ -9 A, V_{GEN} = -10 V, R_g = 1 Ω	-	10	15	
Fall time	t _f		-	3.5	5.5	
Drain-Source Body Diode Characterist	ics					
Continuous source-drain diode current	I _S	$T_C = 25 ^{\circ}C$	-	-	-12	A
Pulse diode forward current	I _{SM}		-	-	-50	
Body diode voltage	V_{SD}	$I_S = -9 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.85	-1.2	V
Body diode reverse recovery rime	t _{rr}			30	60	ns
Body diode reverse recovery charge	Q _{rr}	$I_F = 9 A$, di/dt =100 A/ μ s,	-	20	40	nC
Reverse recovery fall time	ta	T _J =25 °C	-	13	-	ns
Reverse recovery rise time	t _b		-	17	-	

Notes

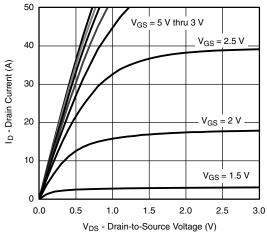
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

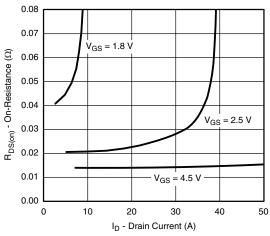




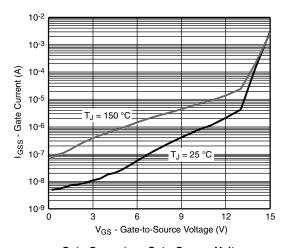
Gate Current vs. Gate-Source Voltage



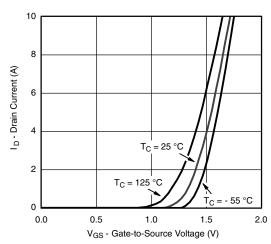
Output Characteristics



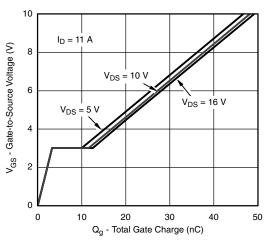
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage

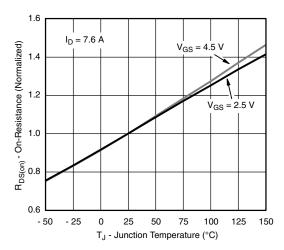


Transfer Characteristics

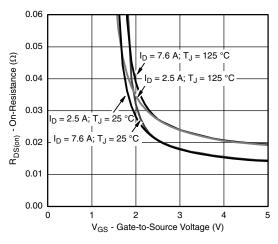


Gate Charge

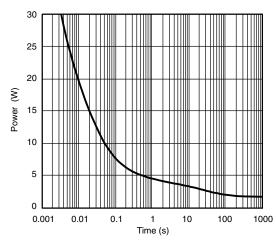




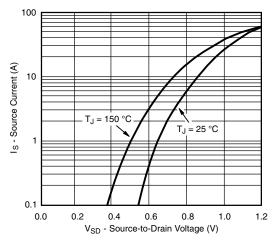
On-Resistance vs. Junction Temperature



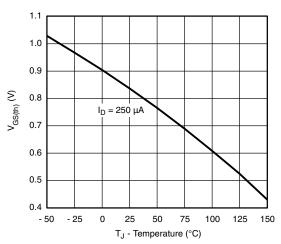
On-Resistance vs. Gate-to-Source Voltage



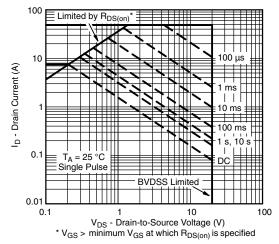
Single Pulse Power, Junction-to-Ambient



Source-Drain Diode Forward Voltage

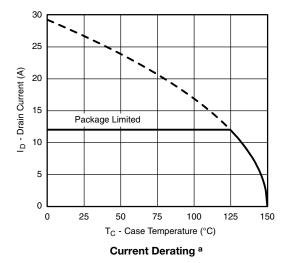


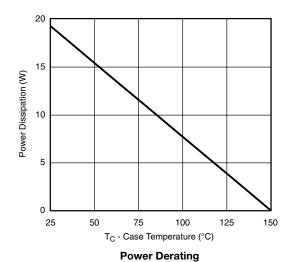
Threshold Voltage



Safe Operating Area, Junction-to-Ambient



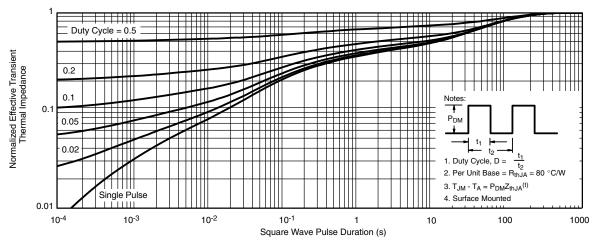




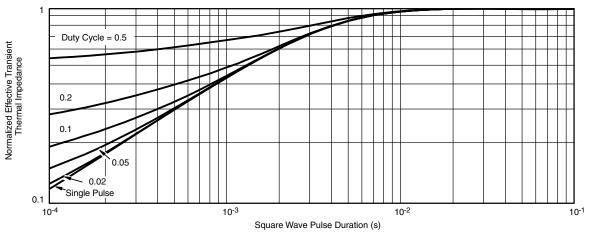
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65472.





Vishay Siliconix

PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

			SINGL	E PAD	DUAL PAD								
DIM	M	ILLIMETER	RS		INCHES		M	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	,	0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP		0.275 TYP			0.011 TYP			
K1		0.400 TYP	1		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP	1		0.009 TYP			0.252 TYP			0.010 TYP		
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP	1		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
ECNI- C C	7404 D	. 0 00 1	. 07										

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

Document Number: 73001 06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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