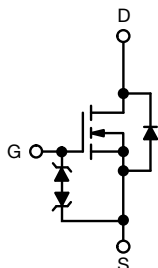
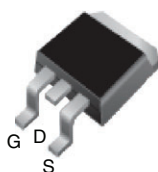


## E Series Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low effective capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Integrated Zener diode ESD protection
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	850	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	1.17
$Q_g$ max. (nC)	16.5	
$Q_{gs}$ (nC)	3	
$Q_{gd}$ (nC)	6	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB5N80AE-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V <sub>DS</sub>	800	V
Gate-source voltage			V <sub>GS</sub>	± 30	
Continuous drain current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	4.4	A
		T <sub>C</sub> = 100 °C		2.8	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	7	
Linear derating factor				0.5	W/°C
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	17	mJ
Maximum power dissipation			P <sub>D</sub>	62.5	W
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-source voltage slope		T <sub>J</sub> = 125 °C	dv/dt	70	V/ns
Reverse diode dv/dt <sup>d</sup>				0.3	
Soldering recommendations (peak temperature) <sup>c</sup>		For 10 s		260	°C


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 1.1$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ , di/dt = 100 A/ $\mu$ s, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

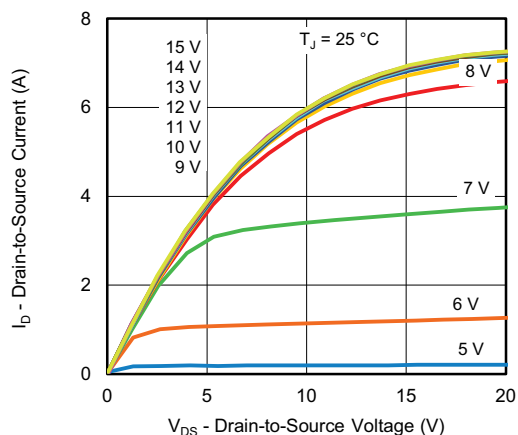
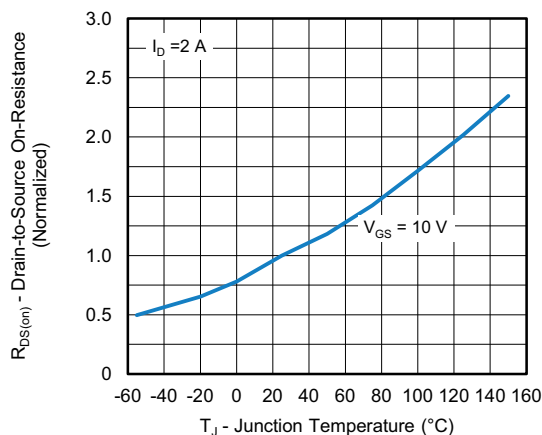
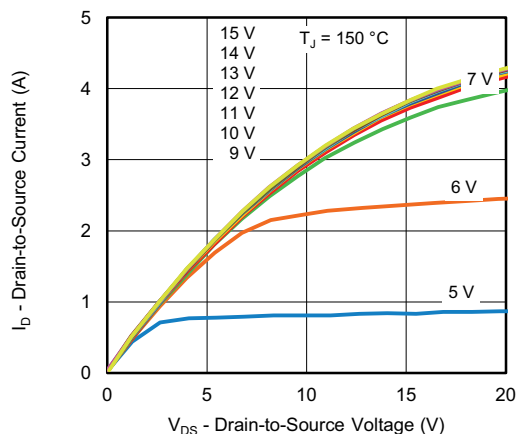
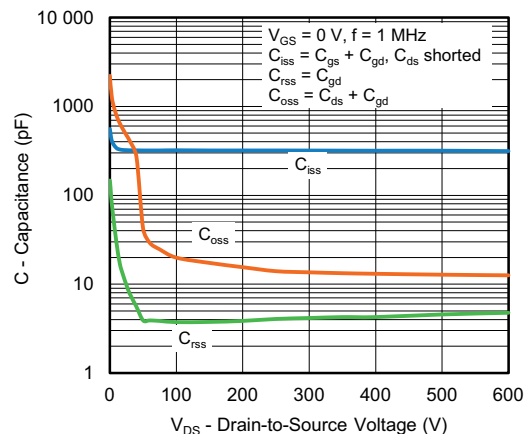
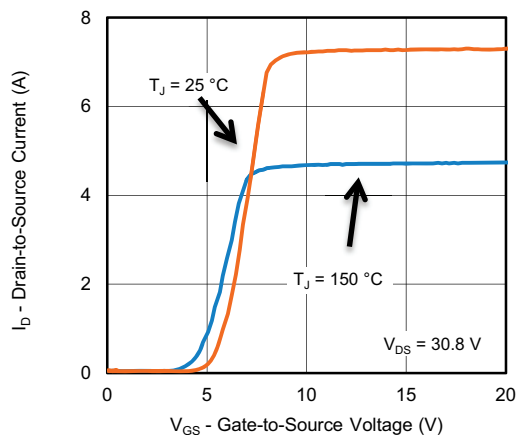
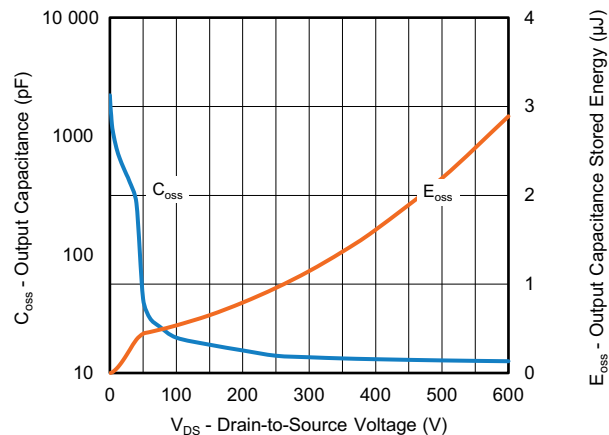
PARAMETER	SYMBOL	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	62	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	2	

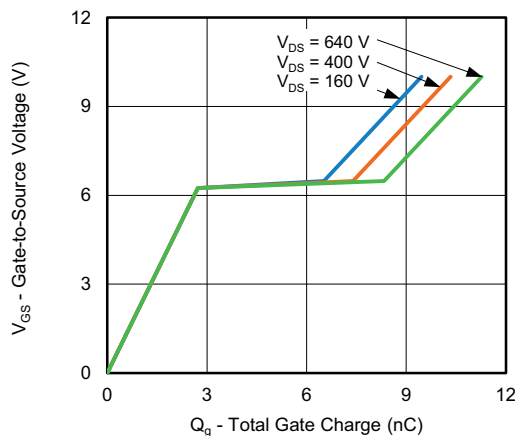
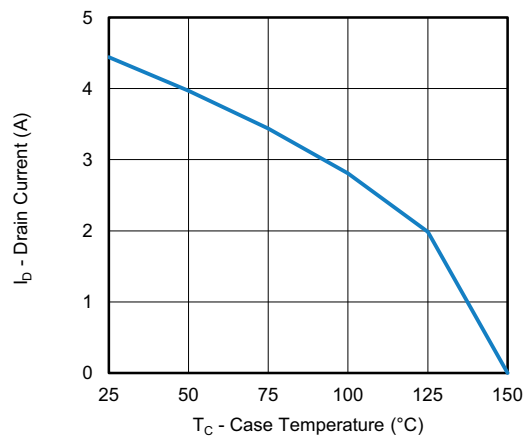
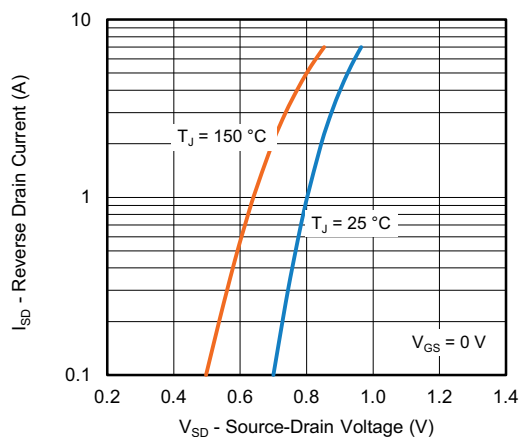
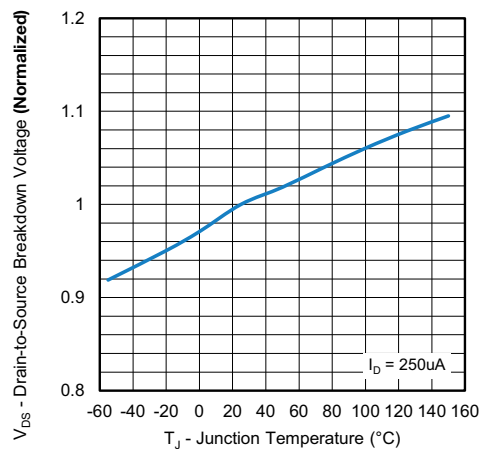
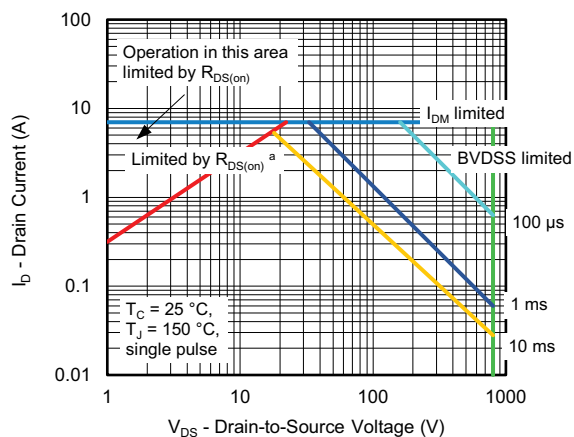
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	800	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$	-	0.8	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 50$	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 640\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 1.5\text{ A}$	-	1.17	1.35	$\Omega$
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 30\text{ V}$ , $I_D = 2\text{ A}$	-	1.2	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	321	-	pF
Output capacitance	$C_{oss}$		-	20	-	
Reverse transfer capacitance	$C_{rss}$		-	4	-	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	14	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$		-	71	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$ , $V_{DS} = 640\text{ V}$	-	11	16.5	nC
Gate-source charge	$Q_{gs}$		-	3	-	
Gate-drain charge	$Q_{gd}$		-	6	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 640\text{ V}$ , $I_D = 2\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_g = 9.1\text{ }\Omega$	-	12	24	ns
Rise time	$t_r$		-	8	16	
Turn-off delay time	$t_{d(off)}$		-	10	20	
Fall time	$t_f$		-	28	56	
Gate input resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	1.6	3.2	6.4	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	4.4	A
Pulsed diode forward current	$I_{SM}$		-	-	7	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 2\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = I_S = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 25\text{ V}$	-	267	534	ns
Reverse recovery charge	$Q_{rr}$		-	1.2	2.4	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$		-	7.5	-	A

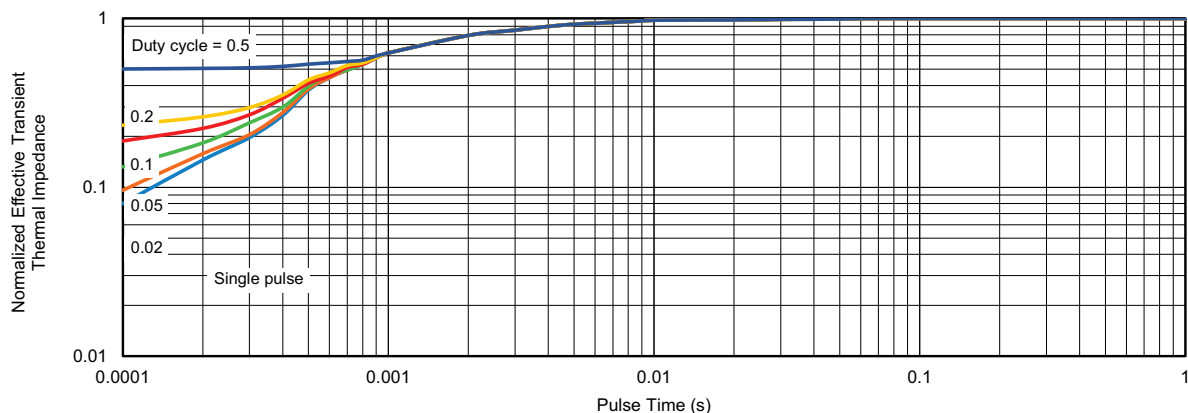
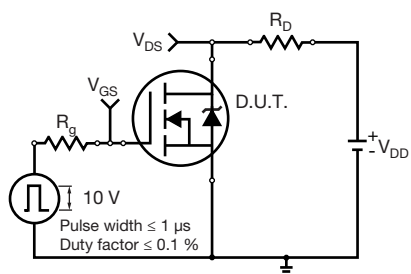
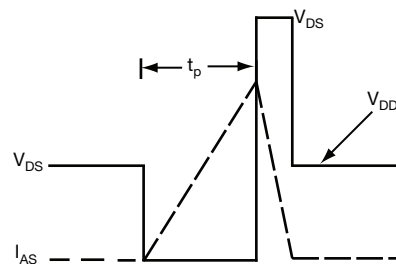
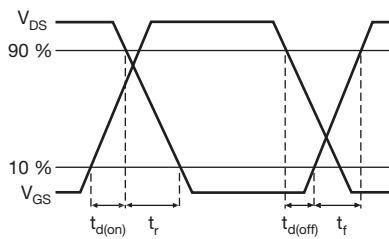
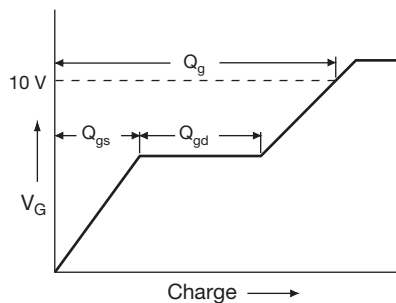
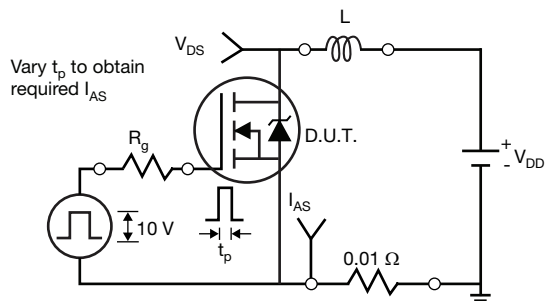
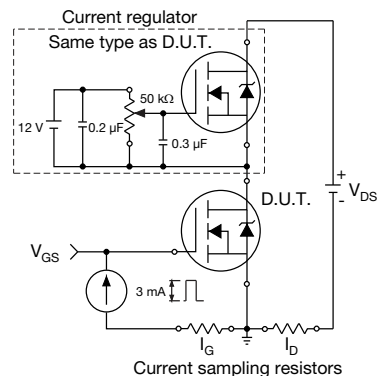
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 480 V  $V_{DSS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 480 V  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Normalized Breakdown Voltage vs. Temperature**

**Fig. 9 - Maximum Safe Operating Area**
**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified


**Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**



**Fig. 19 - For N-Channel**

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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