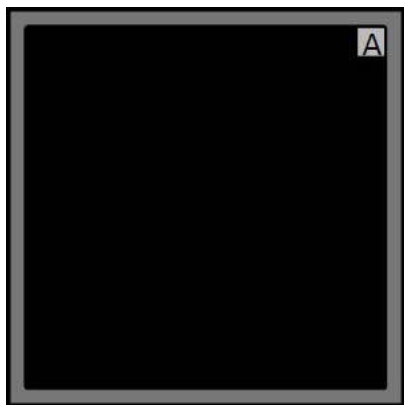


Silicon PIN Photodiode



DESCRIPTION

T1113P is a high speed and high sensitive PIN photodiode chip with 7.5 mm² sensitive area detecting visible and near infrared radiation. Anode is the bond pad on top.

FEATURES

- Package type: chip
- Package form: single chip
- Dimensions (L x W x H in mm): 2.97 x 2.97 x 0.28
- Radiant sensitive area (in mm²): 7.5
- Peak sensitivity wavelength: 960 nm
- High photo sensitivity
- Suitable for visible light and near infrared radiation
- Fast response times
- Angle of half sensitivity: $\phi = \pm 60^\circ$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- High speed photo detector

GENERAL INFORMATION

The datasheet is based on Vishay optoelectronics sample testing under certain predetermined and assumed conditions, and is provided for illustration purpose only. Customers are encouraged to perform testing in actual proposed packaged and used conditions. Vishay optoelectronics die products are tested using Vishay optoelectronics based quality assurance procedures and are manufactured using Vishay optoelectronics established processes. Estimates such as those described and set forth in this datasheet for semiconductor die will vary depending on a number of packaging, handling, use, and other factors. Therefore sold die may not perform on an equivalent basis to standard package products.

PRODUCT SUMMARY

COMPONENT	I_{ra} (μA)	ϕ (deg)	$\lambda_{0.5}$ (nm)
T1113P	55	± 60	660 to 1050

Note

- Test conditions see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
T1113P-SD-F	Wafer sawn on foil with disco frame	MOQ: 8000 pcs	Chip

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ C$, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	60	V
Junction temperature		T_j	100	$^\circ C$
Operating temperature range		T_{amb}	-40 to +100	$^\circ C$
Storage temperature range		T_{stg1}	-40 to +100	$^\circ C$
Storage temperature range on foil		T_{stg2}	-40 to +50	$^\circ C$

BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Breakdown voltage	$I_R = 40\text{ }\mu\text{A}$, $E = 0$	$V_{(BR)}$	60			V
Reverse dark current	$V_R = 10\text{ V}$, $E = 0$	I_{ro}		2	5	nA
Diode capacitance	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$, $E = 0$	C_D		70		pF
	$V_R = 3\text{ V}$, $f = 1\text{ MHz}$, $E = 0$	C_D		25		pF
Reverse light current	$E_e = 1\text{ mW/cm}^2$, $\lambda = 890\text{ nm}$, $V_R = 5\text{ V}$	I_{ra}		51		μA
	$E_e = 1\text{ mW/cm}^2$, $\lambda = 950\text{ nm}$, $V_R = 5\text{ V}$	I_{ra}		55		μA
Angle of half sensitivity		ϕ		± 60		deg
Wavelength of peak sensitivity		λ_p		960		nm
Range of spectral bandwidth		$\lambda_{0.5}$		660 to 1050		nm
Rise time	$V_R = 10\text{ V}$, $R_L = 1\text{ k}\Omega$, $\lambda = 830\text{ nm}$	t_r		100		ns
Fall time		t_f		100		ns

Note

- The measurements are based on samples of die which are mounted on a TO18-header without epoxy coating

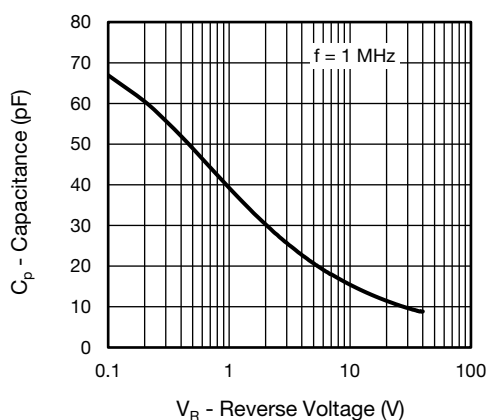
BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - Diode Capacitance vs. Reverse Voltage

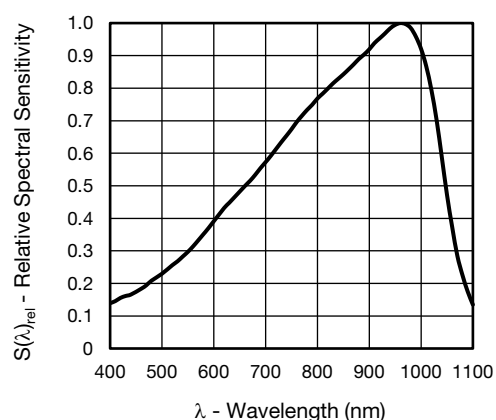
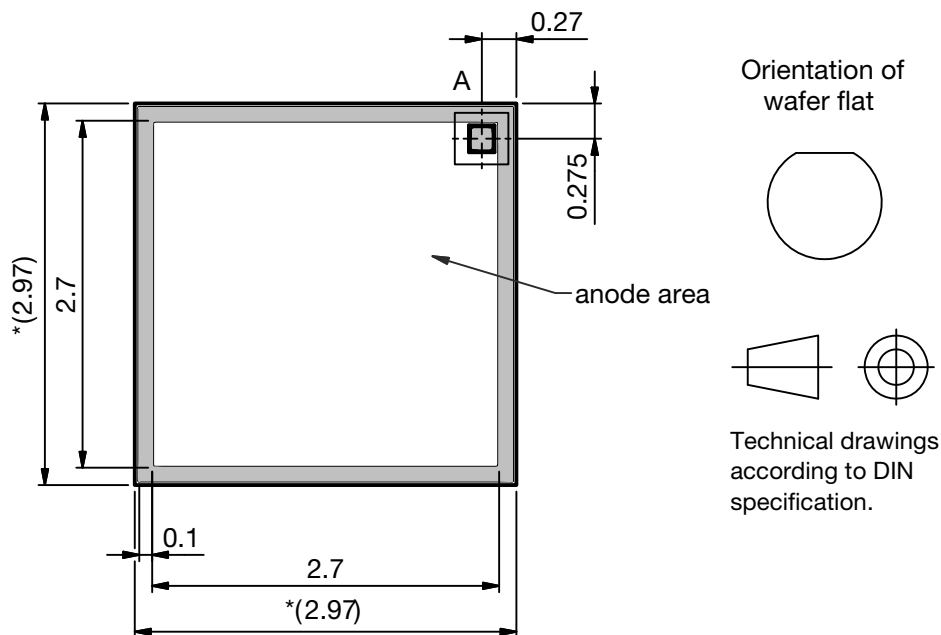
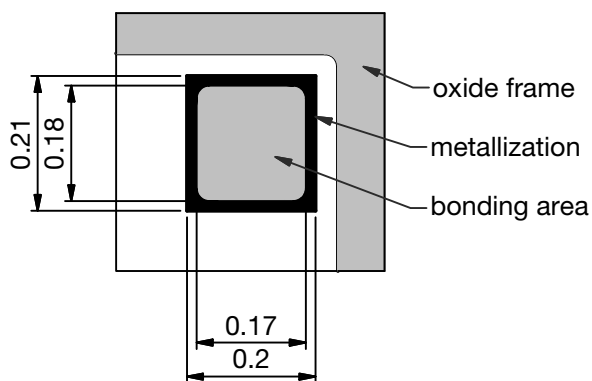


Fig. 2 - Relative Spectral Sensitivity vs. Wavelength without Epoxy Coating

DIMENSIONS in millimeters


*only for information:
dimension of sawn die under consideration of 30 µm saw kerf

A (100 : 1)



Opt. sensitive area: 7.5 mm²

Bonding area: 170 µm x 180 µm
Bonding restricted to this area
in order to avoid damage
of adjacent structures

Thickness: 280 µm ± 15 µm

Drawing-No.: 9.000-5126.01-4
Issue: 1; 25.09.2013

MECHANICAL DIMENSIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Length of chip edge (x-direction)	L _x		2.97		mm
Length of chip edge (y-direction)	L _y		2.97		mm
Sensitive area	A _S		7.5		mm ²
Wafer diameter	D		150		mm
Die height	H	0.265	0.28	0.295	mm
Bond pad anode			0.17 x 0.18		mm ²

**ADDITIONAL INFORMATION**

Frontside metallization, anode	Al
Backside metallization, cathode	NiV-Ag
Dicing	Sawing
Die bonding technology	Epoxy bonding

Note

- All chips are checked in accordance with the Vishay Semiconductor, specification of visual inspection FVOV6870. The visual inspection shall be made in accordance with the "specification of visual inspection as referenced". The visual inspection of chip backside is performed with stereo microscope with incident light and 40x to 80x magnification. The quality inspection (final visual inspection) is performed by production. An additional visual inspection step as special release procedure by QM is not installed.

HANDLING AND STORAGE CONDITIONS

- The hermetically sealed shipment lots shall be opened in temperature and moisture controlled cleanroom environment only. It is mandatory to follow the rules for disposition of material that can be hazardous for humans and environment.
- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Singulated die are not to be handled with tweezers. A vacuum wand with non metallic ESD protected tip should be used.

PACKING

Chips are fixed on adhesive foil. Upon request the foils can be mounted on plastic frame or disco frame. For shipment, the wafers are arranged to stacks and hermetically sealed in plastic bags to ensure protection against environmental influence (humidity and contamination).

Use for recycling reliable operators only. We can help getting in touch with your nearest sales office. By agreement we will take back packing material, if it is sorted. You will have to bear the costs of transport. We will invoice you for any costs incurred for packing material that is returned unsorted or which we are not obliged to accept.



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