Phase Control Thyristors (Stud Version), 300 A

TO-118 (TO- 209AE)

FEATURES

- Center amplifying gate
- International standard case TO-118 (TO-209AE)
- Hermetic metal case with ceramic insulator
- Threaded studs UNF 3/4"-16UNF-2A or ISO M24 x 1.5
- Compression bonded encapsulation for heavy duty operations such as severe thermal cycling
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	300 A
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V, 1600 V, 1800 V, 2000 V
V_{TM}	1.28 V
I_{GT}	200 mA
T_J	-40 °C to +125 °C
Package	TO-118 (TO-209AE)
Circuit configuration	Single SCR

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		300	A
	T_C	75	°C
$I_{T(RMS)}$		470	A
I_{TSM}	50 Hz	8000	
	60 Hz	8380	
I^2t	50 Hz	320	kA^2s
	60 Hz	292	
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	Typical	100	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST300S	04	400	500	50
	08	800	900	
	12	1200	1300	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNITS**
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			300	A
					75	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 64 °C case temperature			470	A
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	8000	
		t = 8.3 ms			8380	
		t = 10 ms	100 % V_{RRM} reapplied		6730	
		t = 8.3 ms			7040	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		320	kA^2s
		t = 8.3 ms			292	
		t = 10 ms	100 % V_{RRM} reapplied		226	
		t = 8.3 ms			207	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			3200	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.97	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.98	
Low level value of on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.74	mΩ
High level value of on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.73	
Maximum on-state voltage	V_{TM}	I_{pk} = 940 A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			1.66	V
Maximum holding current	I_H	T_J = 25 °C, anode supply 12 V resistive load			600	mA
Typical latching current	I_L				1000	

SWITCHING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ µs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/µs
Typical delay time	t_d	Gate current 1 A, dI_g/dt = 1 A/µs V_d = 0.67 % V_{DRM}, T_J = 25 °C	1.0	µs
Typical turn-off time	t_q	I_{TM} = 550 A, $T_J = T_J$ maximum, dI/dt = 40 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 Ω, t_p = 500 µs	100	

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

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TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10.0		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		2.0		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3.0		A
Maximum peak positive gate voltage	$+ V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	$- V_{GM}$			5.0		V
DC gate current required to trigger	I_{GT}	T_J = -40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		T_J = 25 °C		100	200	mA
		T_J = 125 °C		50	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40 °C		2.5	-	V
		T_J = 25 °C		1.8	3	V
		T_J = 125 °C		1.1	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{Stg}		-40 to 150	°C
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.10	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.03	K/W
Mounting torque, ± 10 %		Non-lubricated threads	48.5 (425)	N · m (lbf · in)
Approximate weight			535	g
Case style		See dimensions - link at the end of datasheet	TO-118 (TO-209AE)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.011	0.008	$T_J = T_J$ maximum	K/W
120°	0.013	0.014		
90°	0.017	0.018		
60°	0.025	0.026		
30°	0.041	0.042		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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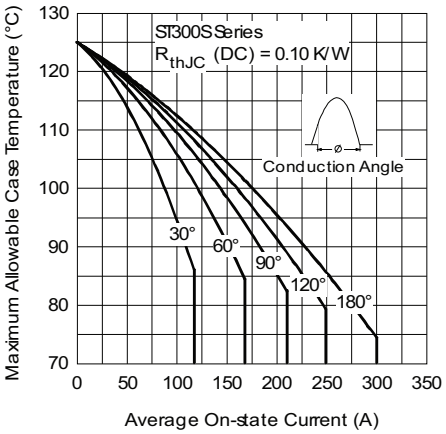

Fig. 1 - Current Ratings Characteristics

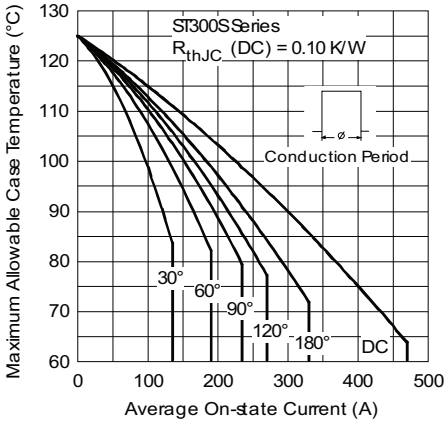

Fig. 2 - Current Ratings Characteristics

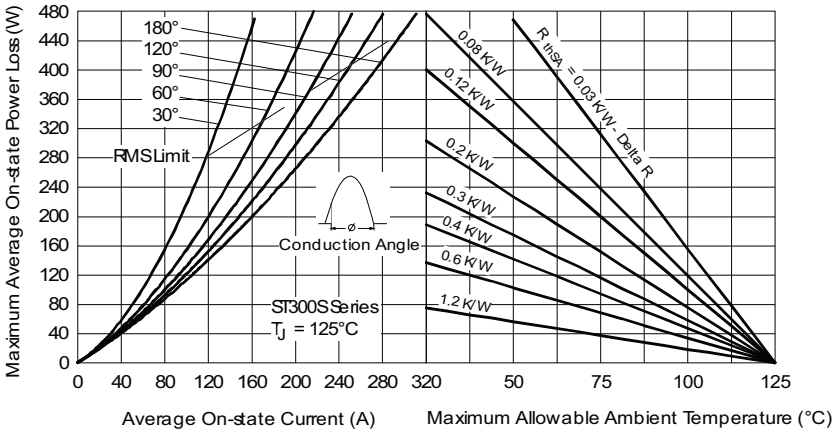

Fig. 3 - On-State Power Loss Characteristics

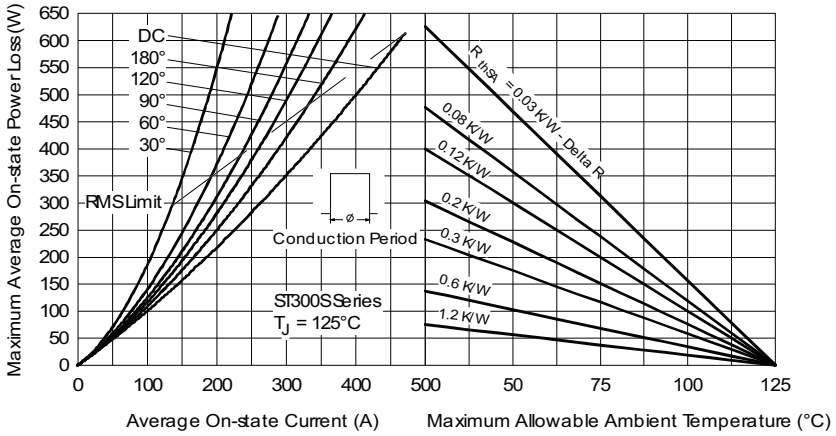

Fig. 4 - On-State Power Loss Characteristics

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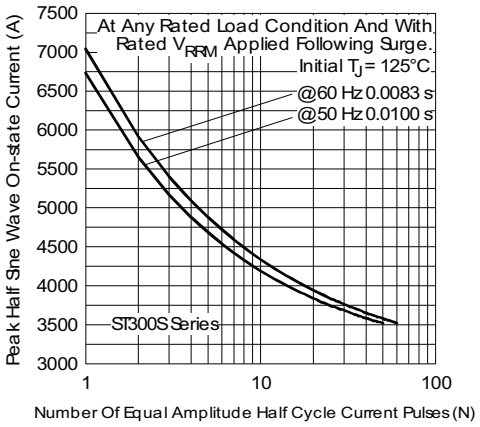

Fig. 5 - Maximum Non-Repetitive Surge Current

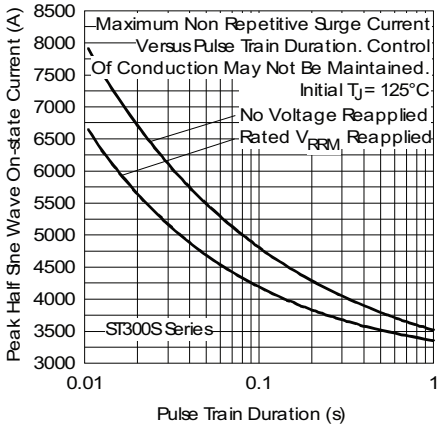

Fig. 6 - Maximum Non-Repetitive Surge Current

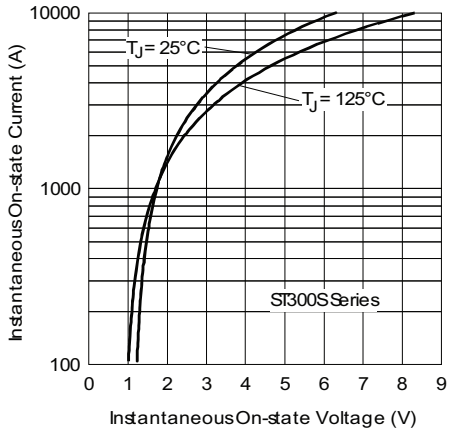

Fig. 7 - On-State Voltage Drop Characteristics

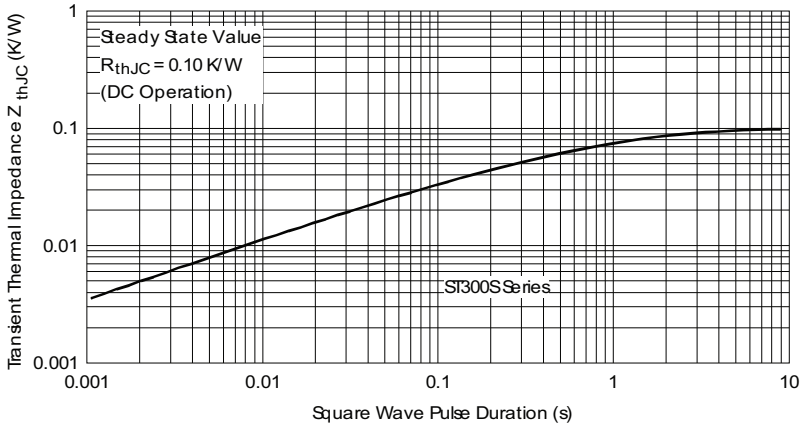

Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

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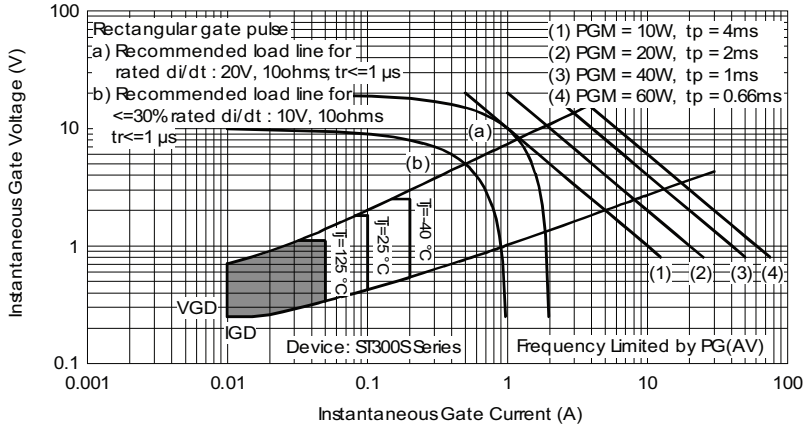

Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

VS-	ST	30	0	S	20	P	0	-	PbF
1	2	3	4	5	6	7	8	9	10

1 - Vishay Semiconductors product

2 - Thyristor

3 - Essential part number

4 - 0 = Converter grade

5 - S = Compression bonding stud

6 - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)

7 - P = stud base 3/4" 16UNF-2A threads
M = stud base metric threads (M24 x 1.5)

8 - 0 = Eyelet terminals (gate and auxiliary cathode leads)
1 = Fast-on terminals (gate and auxiliary cathode leads)
3 = Threaded top terminal 3/8" 24UNF-2A

9 - Critical dV/dt:
- None = 500 V/µs (standard value)
- L = 1000 V/µs (special selection)

10 - None = Standard production
- PbF = Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95084

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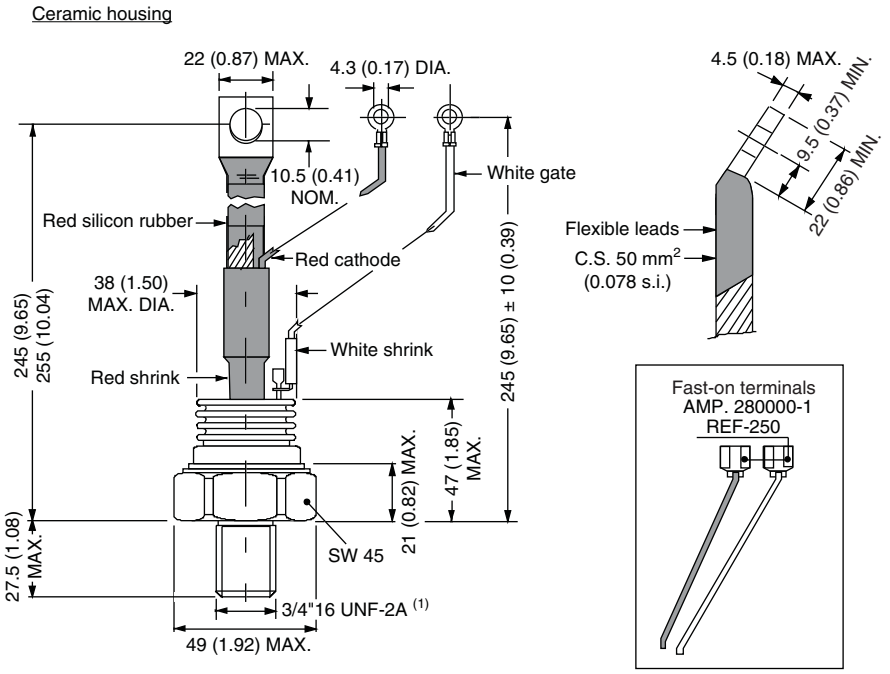
TO-209AE (TO-118)

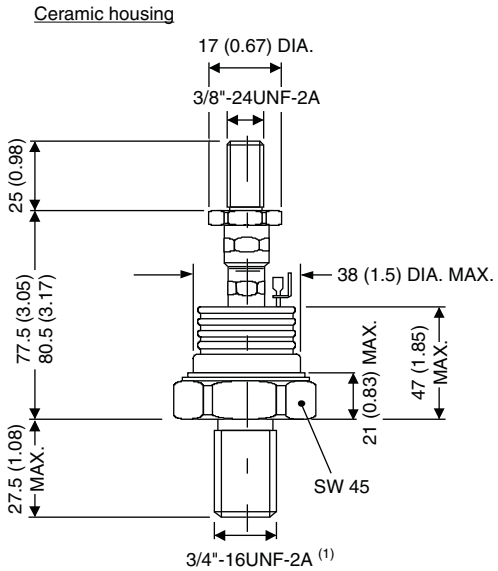
DIMENSIONS - TO-209AE (TO-118) in millimeters (inches)



Note

(1) For metric device: M24 x 1.5 - length screw 21 (0.83) maximum

DIMENSIONS - TO-209AE (TO-118) WITH TOP THREAD TERMINAL 3/8" in millimeters (inches)



Note

(1) For metric device: M24 x 1.5 - length screw 21 (0.83) maximum

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