Vishay Siliconix

N-Channel 20 V (D-S) MOSFET



PRODUCT SUMMARY	
V _{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0013
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0014
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5 \text{ V}$	0.00265
Q _g typ. (nC)	24.6
I _D (A)	165 ^g
Configuration	Single

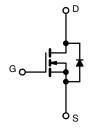
FEATURES

- TrenchFET® Gen V power MOSFET
- 2.5 V rated R_{DS(on)}
- 100 % R_q and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- · Battery management
- · Load switching



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR5208DP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	20	V	
Gate-source voltage		V _{GS}	+8 / -7	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		165		
	T _C = 70 °C		132		
	T _A = 25 °C	I _D	48 b, c		
	T _A = 70 °C		38.4 ^{b, c}	_	
Pulsed drain current (t = 100 µs)		I _{DM}	150	A	
Continuous source-drain diode current	T _C = 25 °C		51.6		
	T _A = 25 °C	I _S	4.3 ^{b, c}		
Single pulse avalanche current	. 0.1!!	I _{AS}	35		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	61.25	mJ	
Maximum power dissipation	T _C = 25 °C		56.8		
	T _C = 70 °C		36.3		
	T _A = 25 °C	P _D	4.8 b, c	W	
	T _A = 70 °C		3.0 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	.0	
Soldering recommendations (peak temperature) c			260	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	21	26	°C/W	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.8	2.2	C/VV	

Notes

- a. Package limited
- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- g. T_C = 25 °C

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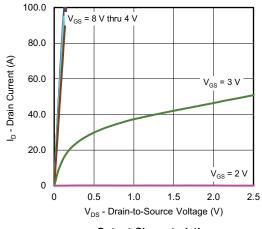
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	20	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.2	-	mV/°0	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.4	-	1.3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +8 / -7 \text{ V}$	-	-	100	nA	
Zero gate voltage drain current		V _{DS} = 16 V, V _{GS} = 0 V	-	-	1	<u> </u>	
	I _{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$	-	-	50	μA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 8 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
Drain-source on-state resistance ^a	, ,	$V_{GS} = 8 \text{ V}, I_D = 10 \text{ A}$	-	0.00108	0.0013	<u> </u>	
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.00114	0.0014	Ω	
		V _{GS} = 2.5 V, I _D = 10 A	-	0.00195	0.00265		
Forward transconductance ^a	9fs	V _{DS} = 15 V, I _D = 10 A	-	70	-	S	
Dynamic ^b		-	1	L	L		
Input capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	4100	-	pF	
Output capacitance	Coss		-	1600	-		
Reverse transfer capacitance	C _{rss}		- 52 -	-	1 "		
		$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	-	45	68	nC	
Total gate charge	Qg		-	24.6	37		
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	8.8	-		
Gate-drain charge	Q _{gd}		-	2.0	-		
Gate resistance	Rg	f = 1 MHz	0.4	0.96	1.6	Ω	
Turn-on delay time	t _{d(on)}		-	12	24		
Rise time	t _r	V_{DD} = 10 V, R_L = 1 Ω , $I_D \cong$ 10 A,	-	5	10		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$	-	36	72		
Fall time	t _f		-	5	10		
Turn-on delay time	t _{d(on)}		-	23	46	ns	
Rise time	t _r	$V_{DD} = 10 \text{ V}, R_{I} = 1 \Omega, I_{D} \cong 10 \text{ A},$	-	39	78		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	39	78		
Fall time	t _f		-	6	10		
Drain-Source Body Diode Characteristi	cs		1	L	L		
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	51.6		
Pulse diode forward current	I _{SM}	-	-	-	150	A	
Body diode voltage	V _{SD}	$I_{S} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.66	1.1	V	
Body diode reverse recovery time	t _{rr}		-	39	78	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	34	68	nC	
Reverse recovery fall time	ta	$T_{\rm J} = 25 ^{\circ}{\rm C}$	-	21	-		
Reverse recovery rise time	t _b		_	18	_	ns	

Notes

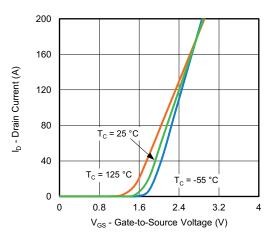
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

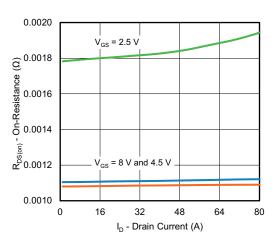




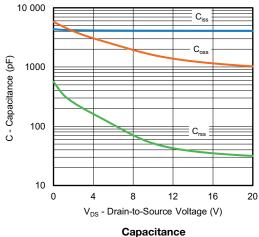
Output Characteristics



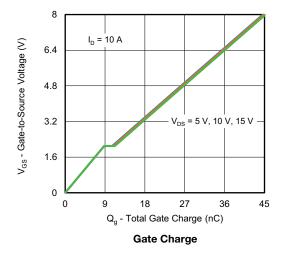
Transfer Characteristics

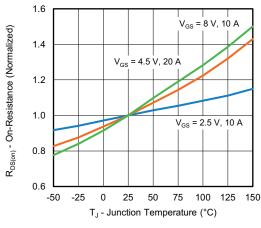


On-Resistance vs. Drain Current and Gate Voltage



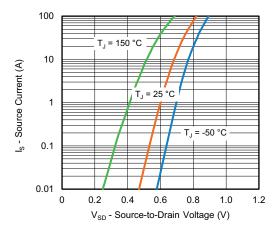
Capacitance



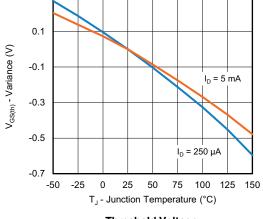


On-Resistance vs. Junction Temperature



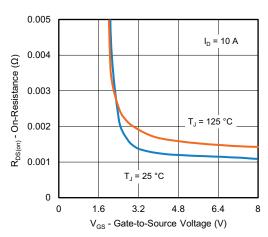


Source-Drain Diode Forward Voltage

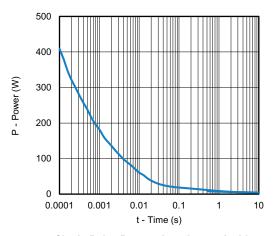


0.3

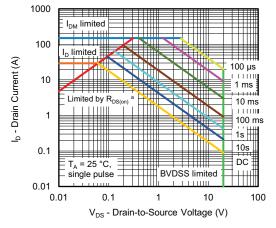
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

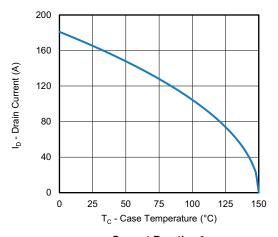


Single Pulse Power, Junction-to-Ambient

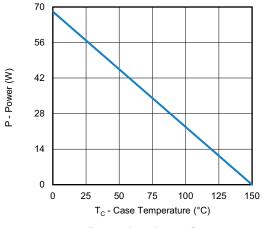


Safe Operating Area, Junction-to-Ambient

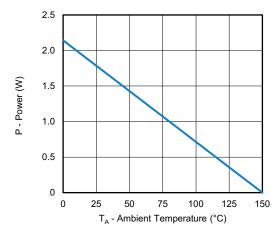




Current Derating a





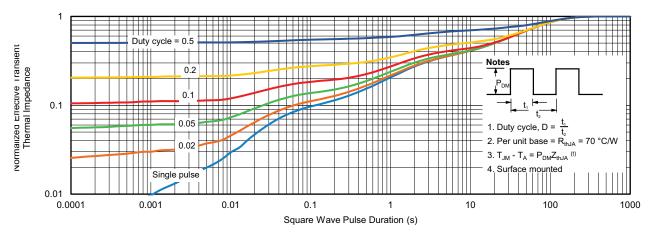


Power, Junction-to-Ambient

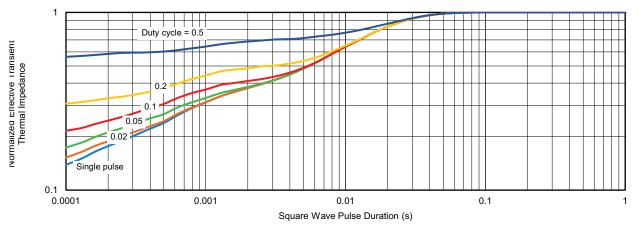
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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