

Thyristor/Thyristor (Super MAGN-A-PAK Power Modules), 570 A



Super MAGN-A-PAK

PRIMARY CHARACTERISTICS				
I _{T(AV)}	570 A			
Туре	Modules - thyristor, standard			
Package	Super MAGN-A-PAK			

FEATURES

- High current capability
- High surge capability
- · Industrial standard package
- 3000 V_{RMS} isolating voltage with non-toxic substrate
- · Designed and qualified for industrial level
- UL approved file E78996
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

TYPICAL APPLICATIONS

- Motor starters
- DC motor controls AC motor controls
- Uninterruptible power supplies

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
I _{T(AV)}	T _C = 74 °C	570			
I _{T(RMS)}	T _C = 74 °C	895	A		
1	50 Hz	17 800	^		
I _{TSM}	60 Hz	18 700			
l ² t	50 Hz	1591	kA ² s		
I ² t	60 Hz	1452	KA ² S		
I ² √t		15 910	kA ^{2√} s		
V _{RRM}	Range	1800	V		
T _{Stg}	Range	-40 to +135	°C		
T _J	Range	-40 to +135			

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS						
TYPE NUMBER	VOLTAGE CODE	V _{RRM} /V _{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$\begin{aligned} I_{RRM}/I_{DRM} & \text{MAXIMUM} \\ \text{AT T}_{J} &= T_{J} & \text{MAXIMUM} \\ & \text{mA} \end{aligned}$		
VS-VSKT570-18PbF	18	1800	1900	120		



ON-STATE CONDUCTION						
PARAMETER	SYMBOL		TEST CONDI	TIONS	VALUES	UNITS
Maximum average on-state current	L	180° conduction	n, half sine wave		570	Α
at case temperature	I _{T(AV)}	180 Conduction	ii, iiaii siile wave		74	°C
Maximum RMS on-state current	I _{T(RMS)}	180° conduction	n, half sine wave	at T _C = 74 °C	895	Α
		t = 10 ms	No voltage		17.8	
Maximum peak, one-cycle,	I _{TSM,}	t = 8.3 ms	reapplied		18.7	kA kA ² s
non-repetitive on-state surge current	I _{FSM}	t = 10 ms	100 % V _{RRM}		15.0	
		t = 8.3 ms	reapplied	Sinusoidal half wave,	15.7	
Marrian 124 for foring		t = 10 ms	No voltage reapplied	initial $T_J = T_J$ maximum	1591	
	l ² t	t = 8.3 ms			1452	
Maximum I ² t for fusing		t = 10 ms	100 % V _{RRM}		1125	
		t = 8.3 ms	reapplied		1027	
Maximum I $^2\sqrt{t}$ for fusing	I²√t	t = 0.1 ms to 10 ms, no voltage reapplied		eapplied	15 910	kA²√s
Low level value or threshold voltage	V _{T(TO)1}	$(16.7 \% \times \pi \times I_{T})$	$(AV) < I < \pi \times I_{T(AV)}$	$T_J = T_J \text{ maximum}$	0.864	V
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.97	v
Low level value on-state slope resistance	r _{t1}	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), $T_J = T_J$ maximum		$T_J = T_J \text{ maximum}$	0.411	mΩ
High level value on-state slope resistance	r _{t2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		0.362	1115.2	
Maximum on-state voltage drop	V_{TM}	$I_{pk} = 1500 \text{ A, T}_{J}$	= 25 °C, t _p = 10	ms sine pulse	1.50	V
Maximum holding current	I _H	T. = 25 °C 222	de supply 12 V re	osistivo load	500	mA
Maximum latching current	ΙL	$I_J = 25$ C, and	ue suppiy iz v re	solotive IOdu	1000] IIIA

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum rate of rise of turned-on current	dl/dt	$T_J = T_J$ maximum, $I_{TM} = 400$ A, V_{DRM} applied	1000	A/µs	
Typical delay time	t _d	Gate current 1 A, $dI_g/dt = 1 A/\mu s$ $V_d = 0.67 \% V_{DRM}, T_J = 25 °C$	2.0	-16	
Typical turn-off time	t _q	I_{TM} = 750 A; T_J = T_J maximum, dI/dt = - 60 A/µs, V_R = 50 V, dV/dt = 20 V/µs, gate 0 V 100 Ω	200	μs	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to $V_D = 80 \% V_{DRM}$	1000	V/µs
RMS insulation voltage	V _{INS}	t = 1 s	3000	V
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	120	mA



TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms	10	W
Maximum peak average gate power	P _{G(AV)}	$T_J = T_J$ maximum, f = 50 Hz, d % = 50	2.0] vv
Maximum peak positive gate current	+I _{GM}		3.0	Α
Maximum peak positive gate voltage	+V _{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms	20	V
Maximum peak negative gate voltage	-V _{GM}		5.0	
Maximum DC gate current required to trigger	I _{GT}	T 05 °C V 10 V	200	mA
DC gate voltage required to trigger	V _{GT}	T _J = 25 °C, V _{ak} 12 V	3.0	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	10	mA
DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	TJ		-40 to +135	°C
Maximum storage temperature range	T _{Stg}		-40 to +135	
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation	0.065	14004
Maximum thermal resistance, case to heatsink per module	R _{thC-hs}	Mounting surface smooth, flat and greased	0.02	K/W
Mounting Super MAGN-A-PAK to heatsing	nk	A mounting compound is recommended and the torque should be rechecked after a period	6 to 8	Nm
torque busbar to super MAGN-A-PA	K	of 3 hours to allow for the spread of the compound	12 to 15	INIII
Approximate weight			1500	g
Case style		See dimensions (link at the end of datasheet)	Super MAGN-	-A-PAK

△R _{thJC} CONDUCTIO	N			
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006		
120°	0.011	0.011		
90°	0.014	0.015	$T_J = T_J$ maximum	K/W
60°	0.021	0.022		
30°	0.037	0.038		

Note

• Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC



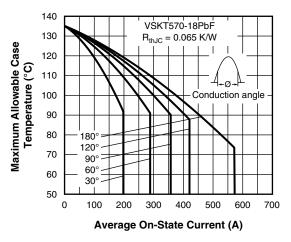


Fig. 1 - Current Ratings Characteristics

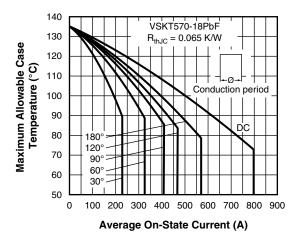


Fig. 2 - Current Ratings Characteristics

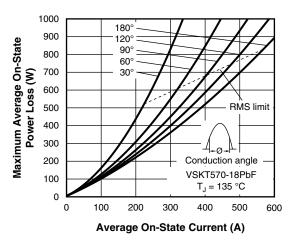


Fig. 3 - On-State Power Loss Characteristics

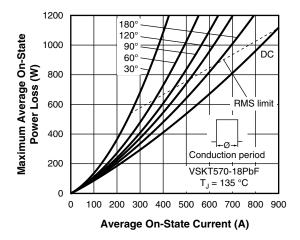


Fig. 4 - On-State Power Loss Characteristics

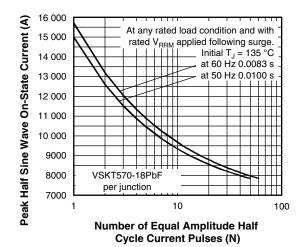


Fig. 5 - Maximum Non-Repetitive Surge Current

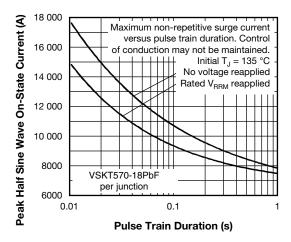
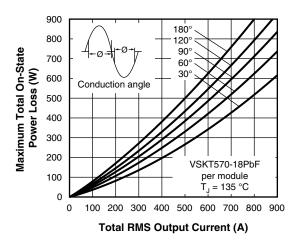


Fig. 6 - Maximum Non-Repetitive Surge Current



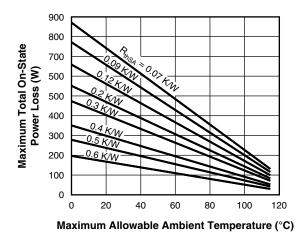


Fig. 7 - On-State Power Loss Characteristics

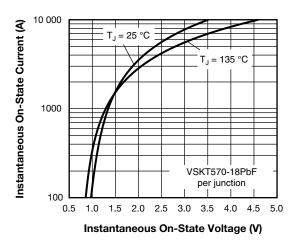


Fig. 8 - On-State Voltage Drop Characteristics

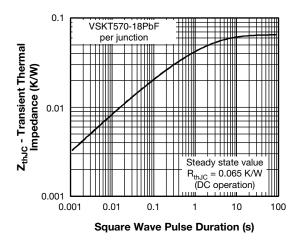


Fig. 9 - Thermal Impedance Z_{thJC} Characteristics

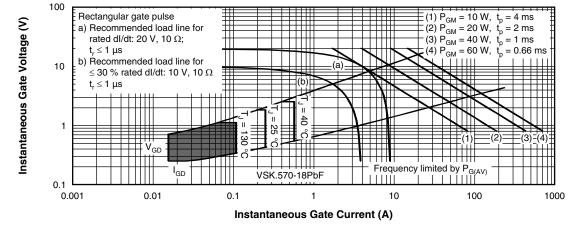
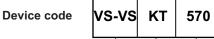
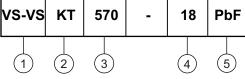


Fig. 10 - Gate Characteristics

ORDERING INFORMATION TABLE





Vishay Semiconductors product

Circuit configuration (see below)

Current rating

Voltage code x 100 = V_{RRM}

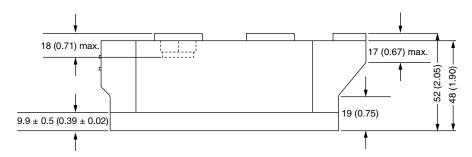
Lead (Pb)-free

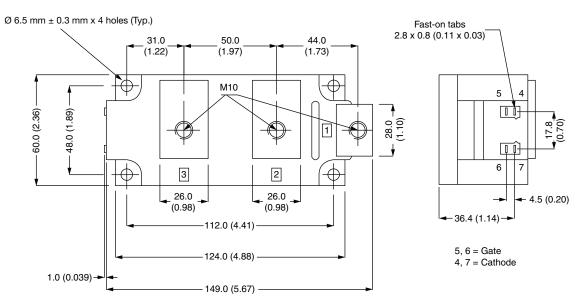
LINKS TO RELAT	ED DOCUMENTS
Dimensions	www.vishay.com/doc?95283



Super MAGN-A-PAK Thyristor/Diode

DIMENSIONS in millimeters (inches)







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