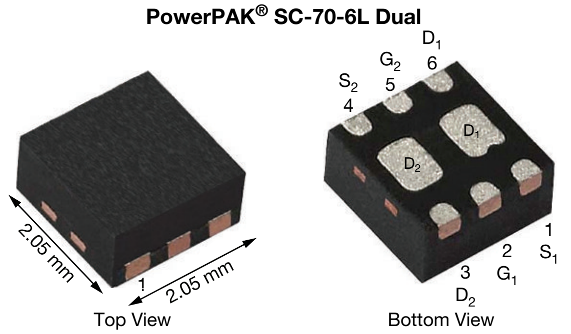
N-Channel 12 V (D-S) and P-Channel 20 V (D-S) MOSFET

PowerPAK® SC-70-6L Dual



Marking code: EK

PRODUCT SUMMARY		
	N-CHANNEL	**P-CHANNEL**
V_{DS} (V)	12	-20
$R_{DS(on)}$ (Ω) at V_{GS} = ± 4.5 V	0.028	0.054
$R_{DS(on)}$ (Ω) at V_{GS} = ± 2.5 V	0.033	0.070
$R_{DS(on)}$ (Ω) at V_{GS} = ± 1.8 V	0.042	0.104
$R_{DS(on)}$ (Ω) at V_{GS} = -1.5 V	-	0.165
Q_g typ. (nC)	6.2	9.5
I_D (A) [a]	4.5	-4.5
Configuration	N- and p-pair	

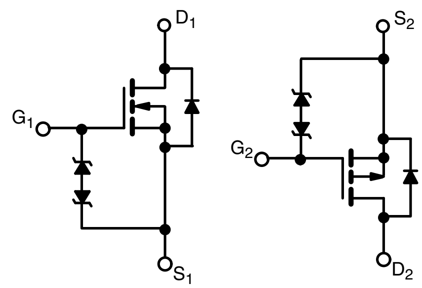
FEATURES

- TrenchFET® power MOSFETs
- Typical ESD protection:
  N-channel 2400 V, P-channel 2000 V
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs and mobile computing
  - Load switches
  - Power management
  - DC/DC converters



N-Channel MOSFET P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA537EDJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		**SYMBOL**	**N-CHANNEL**	**P-CHANNEL**	**UNIT**
Drain-source voltage		V_{DS}	12	-20	V
Gate-source voltage		V_{GS}	± 8	± 8	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	4.5 [a]	-4.5 [a]	A
	T_C = 70 °C		4.5 [a]	-4.5 [a]	
	T_A = 25 °C		4.5 [a, b, c]	-4.5 [a, b, c]	
	T_A = 70 °C		4.5 [a, b, c]	-4.5 [a, b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	20	-15	
Source drain current diode current	T_C = 25 °C	I_S	4.5 [a]	-4.5 [a]	
	T_A = 25 °C		1.6 [b, c]	-1.6 [b, c]	
Maximum power dissipation	T_C = 25 °C	P_D	7.8	7.8	W
	T_C = 70 °C		5	5	
	T_A = 25 °C		1.9 [b, c]	1.9 [b, c]	
	T_A = 70 °C		1.2 [b, c]	1.2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	$t \leq 5$ s	R_{thJA}	52	65	52	65	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	12.5	16	12.5	16	

Notes

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 5 s
d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 110 °C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	N-Ch	12	-	-	V
		V_{GS} = 0 V, I_D = -250 μA	P-Ch	-20	-	-	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	N-Ch	-	8	-	mV/°C
		I_D = -250 μA	P-Ch	-	-15	-	
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 μA	N-Ch	-	-2.5	-	
		I_D = -250 μA	P-Ch	-	2.5	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	N-Ch	0.4	-	1	V
		$V_{DS} = V_{GS}$, I_D = -250 μA	P-Ch	-0.4	-	-1	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	N-Ch	-	-	± 0.5	μA
			P-Ch	-	-	± 3	
		V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch	-	-	± 5	
			P-Ch	-	-	± 30	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 12 V, V_{GS} = 0 V	N-Ch	-	-	1	
		V_{DS} = -20 V, V_{GS} = 0 V	P-Ch	-	-	-1	
		V_{DS} = 12 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch	-	-	10	
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch	-	-	-10	
On-state drain current [b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	N-Ch	10	-	-	A
		$V_{DS} \leq$ -5 V, V_{GS} = -4.5 V	P-Ch	-10	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5.2 A	N-Ch	-	0.023	0.028	Ω
		V_{GS} = -4.5 V, I_D = -3.8 A	P-Ch	-	0.044	0.054	
		V_{GS} = 2.5 V, I_D = 4.8 A	N-Ch	-	0.027	0.033	
		V_{GS} = -2.5 V, I_D = -3.3 A	P-Ch	-	0.057	0.070	
		V_{GS} = 1.8 V, I_D = 2.5 A	N-Ch	-	0.035	0.042	
		V_{GS} = -1.8 V, I_D = -1 A	P-Ch	-	0.075	0.104	
		V_{GS} = -1.5 V, I_D = -0.5 A	P-Ch	-	0.097	0.165	
Forward transconductance [b]	g_{fs}	V_{DS} = 6 V, I_D = 5.2 A	N-Ch	-	23	-	S
		V_{DS} = -6 V, I_D = -3.6 A	P-Ch	-	11	-	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Dynamic [a]							
Input capacitance	C_{iss}	N-Channel V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	-	455	-	pF
			P-Ch	-	770	-	
Output capacitance	C_{oss}		N-Ch	-	190	-	
			P-Ch	-	90	-	
Reverse transfer capacitance	C_{rss}		N-Ch	-	150	-	
			P-Ch	-	81	-	
Total gate charge	Q_g	V_{DS} = 6 V, V_{GS} = 8 V, I_D = 6.8 A	N-Ch	-	10.5	16	nC
		V_{DS} = -10 V, V_{GS} = -8 V, I_D = -4.9 A	P-Ch	-	16.3	25	
		N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 6.8 A P-Channel V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -4.9 A	N-Ch	-	6.2	9.5	
			P-Ch	-	9.5	14.5	
Gate-source charge	Q_{gs}		N-Ch	-	0.8	-	
			P-Ch	-	1.4	-	
Gate-drain charge	Q_{gd}		N-Ch	-	1.6	-	
			P-Ch	-	2.3	-	
Gate resistance	R_g	f = 1 MHz	N-Ch	0.8	4	8	Ω
			P-Ch	1	5.1	10	
Turn-on delay time	$t_{d(on)}$	N-Channel V_{DD} = 6 V, R_L = 1.1 Ω $I_D \cong$ 5.4 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = -10 V, R_L = 2.6 Ω $I_D \cong$ -3.9 A, V_{GEN} = -4.5 V, R_g = 1 Ω	N-Ch	-	10	15	ns
			P-Ch	-	15	25	
Rise time	t_r		N-Ch	-	12	20	
			P-Ch	-	15	25	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	25	40	
			P-Ch	-	30	45	
Fall time	t_f		N-Ch	-	12	20	
			P-Ch	-	10	15	
Turn-on delay time	$t_{d(on)}$	N-Channel V_{DD} = 6 V, R_L = 1.3 Ω $I_D \cong$ 5.4 A, V_{GEN} = 8 V, R_g = 1 Ω P-Channel V_{DD} = -10 V, R_L = 2.6 Ω $I_D \cong$ -3.9 A, V_{GEN} = -8 V, R_g = 1 Ω	N-Ch	-	5	10	
			P-Ch	-	7	16	
Rise time	t_r		N-Ch	-	10	15	
			P-Ch	-	12	20	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	20	30	
			P-Ch	-	25	40	
Fall time	t_f		N-Ch	-	10	15	
			P-Ch	-	10	15	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	N-Ch	-	-	4.5	A
			P-Ch	-	-	-4.5	
Pulse diode forward current [a]	I_{SM}		N-Ch	-	-	20	
			P-Ch	-	-	-15	
Body diode voltage	V_{SD}	I_S = 4.8 A, V_{GS} = 0 V	N-Ch	-	0.8	1.2	V
		I_S = -3.9 A, V_{GS} = 0 V	P-Ch	-	-0.9	-1.2	
Body diode reverse recovery time	t_{rr}	N-Channel I_F = 5.4 A, di/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = -3.9 A, di/dt = -100 A/µs, T_J = 25 °C	N-Ch	-	25	50	ns
			P-Ch	-	13	25	
Body diode reverse recovery charge	Q_{rr}		N-Ch	-	10	20	nC
			P-Ch	-	5.5	12	
Reverse recovery fall time	t_a		N-Ch	-	13	-	ns
			P-Ch	-	7.5	-	
Reverse recovery rise time	t_b		N-Ch	-	12	-	
			P-Ch	-	5.5	-	

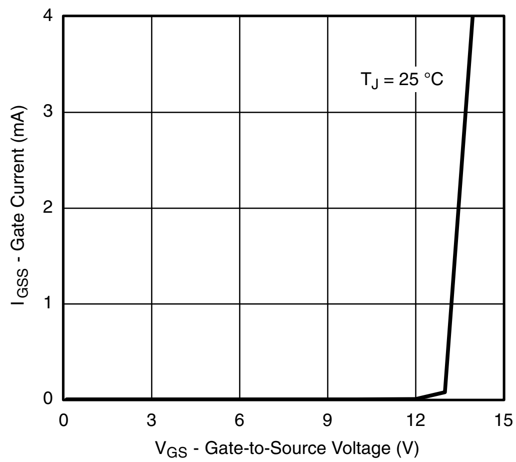
Notes

a. Guaranteed by design, not subject to production testing

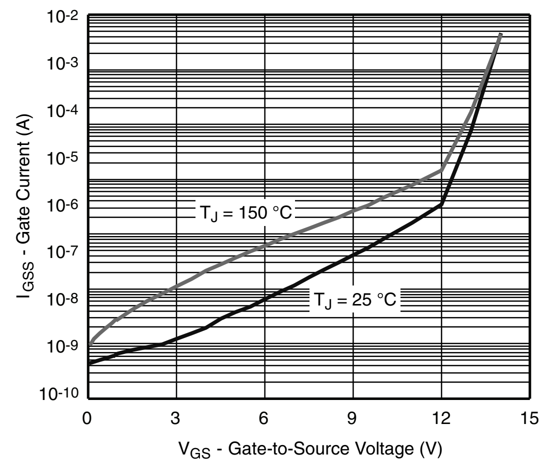
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

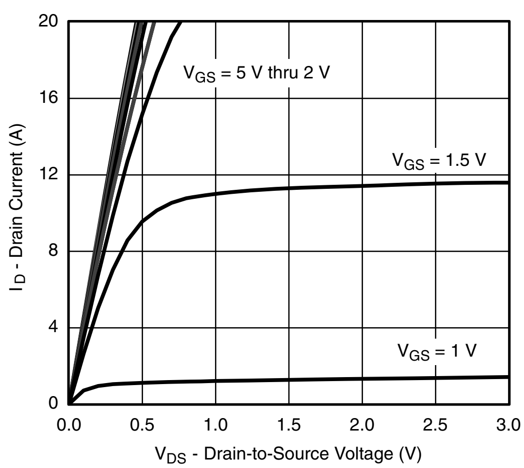
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



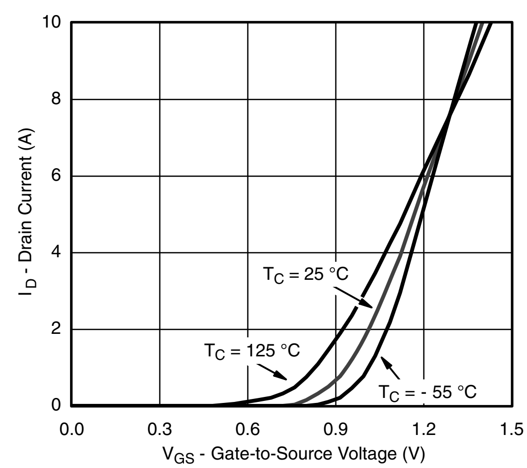
Gate Current vs. Gate-Source Voltage



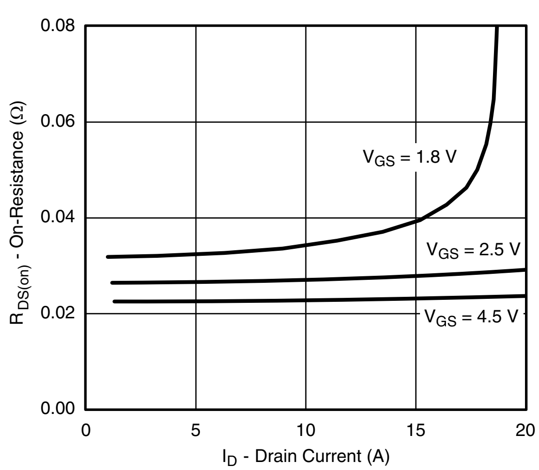
Gate Current vs. Gate-Source Voltage



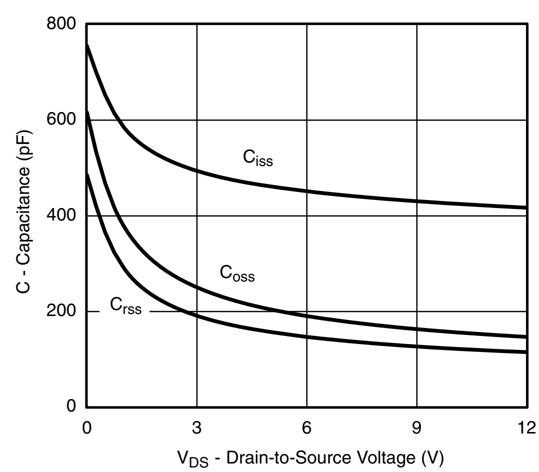
Output Characteristics



Transfer Characteristics

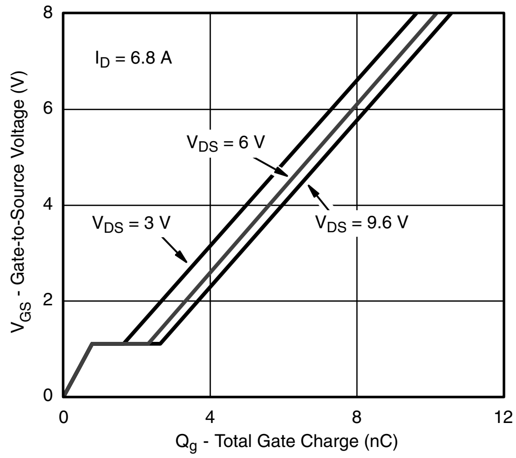


On-Resistance vs. Drain Current and Gate Voltage

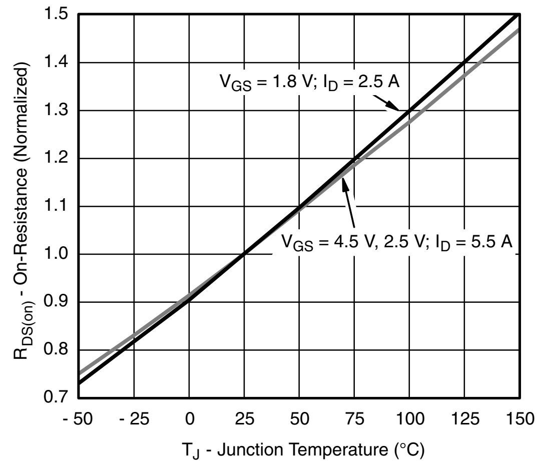


Capacitance

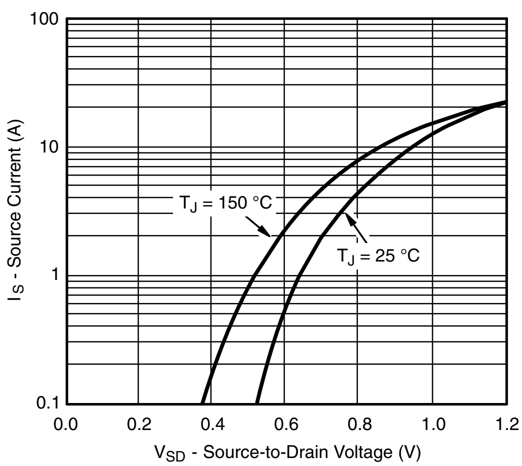
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



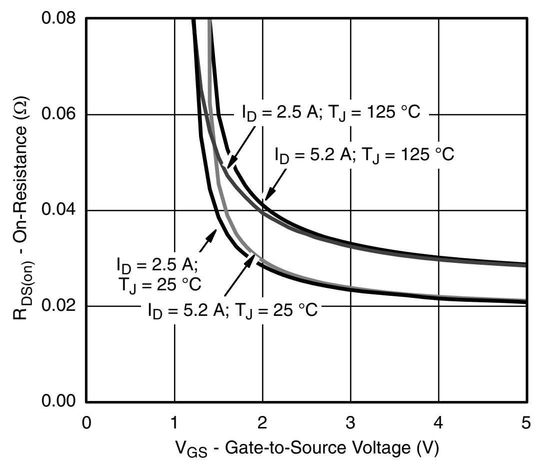
Gate Charge



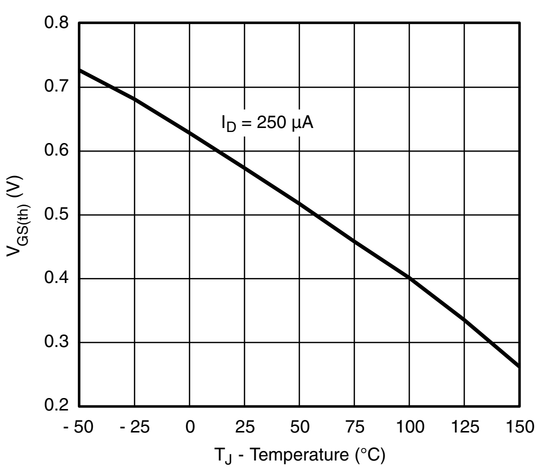
On-Resistance vs. Junction Temperature



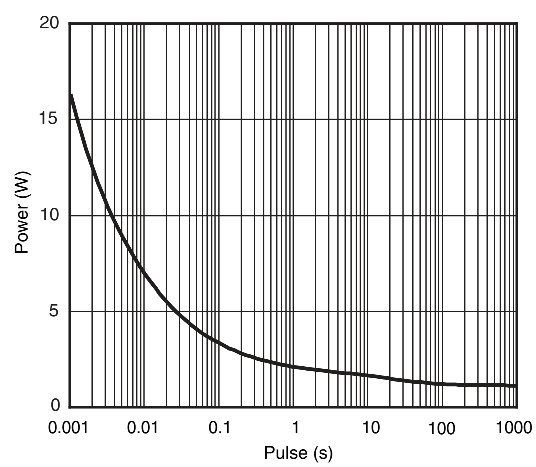
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

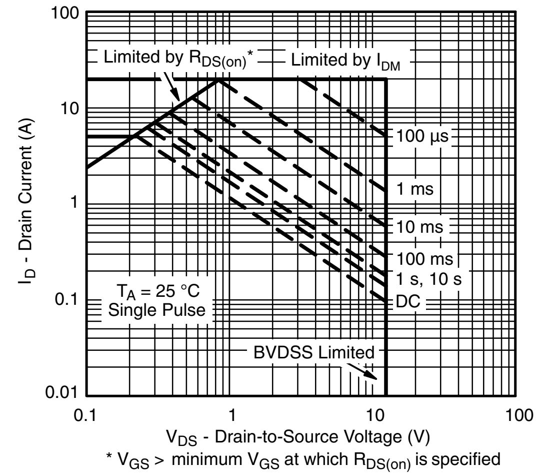


Threshold Voltage

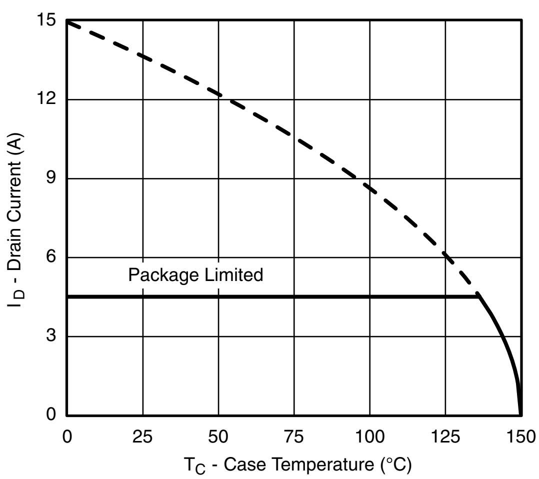


Single Pulse Power (Junction-to-Ambient)

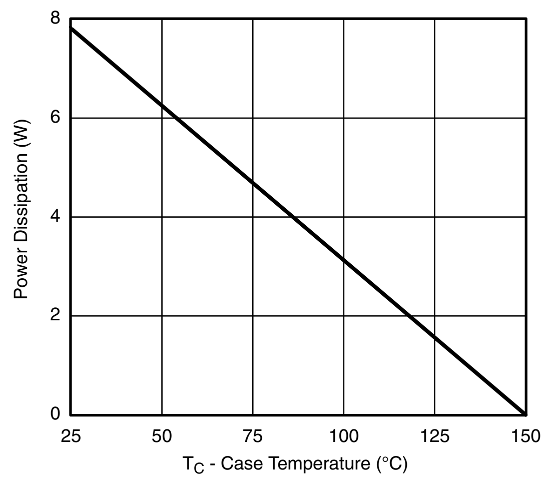
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating [a]

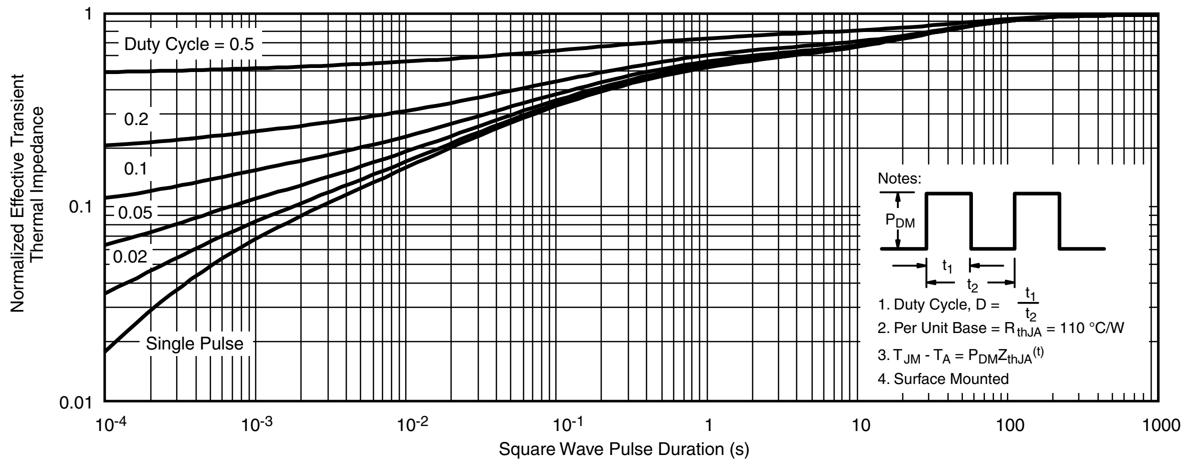


Power Derating

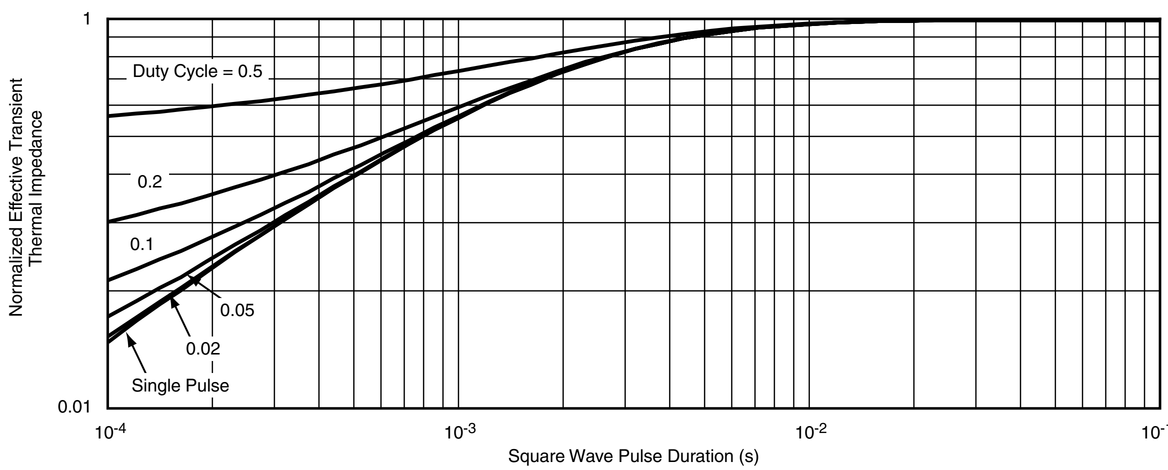
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

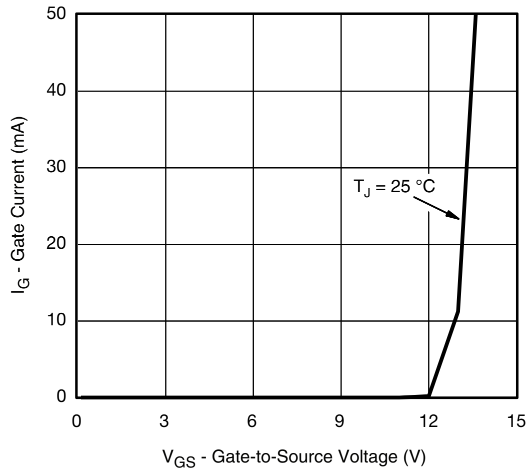


Normalized Thermal Transient Impedance, Junction-to-Ambient

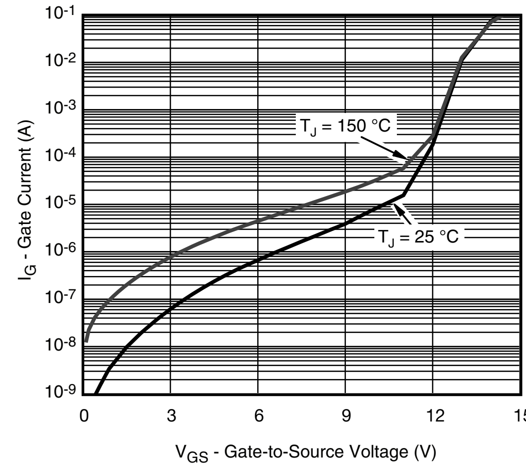


Normalized Thermal Transient Impedance, Junction-to-Case

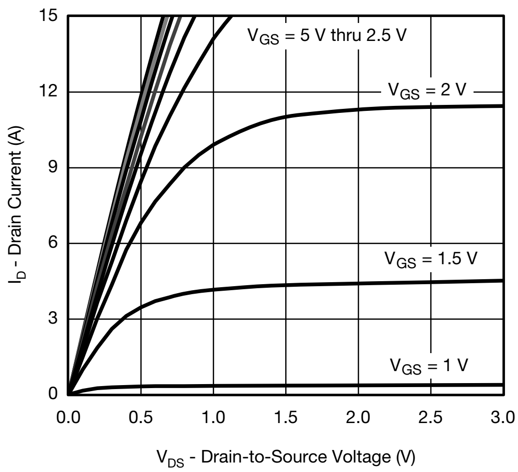
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



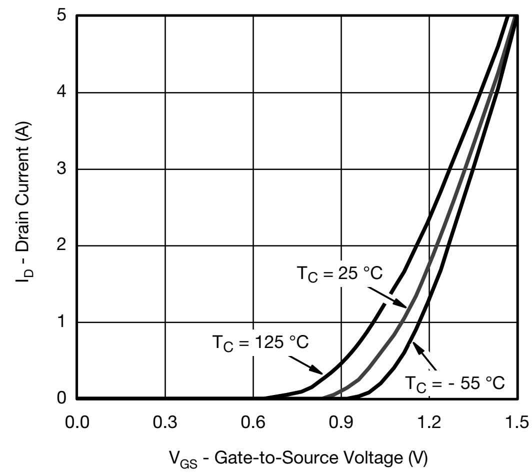
Gate Current vs. Gate-to-Source Voltage



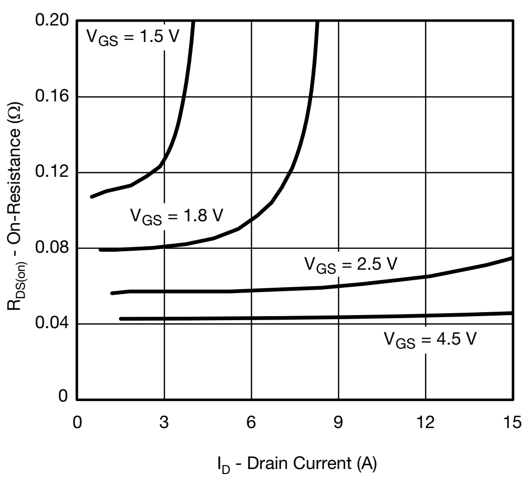
Gate Current vs. Gate-to-Source Voltage



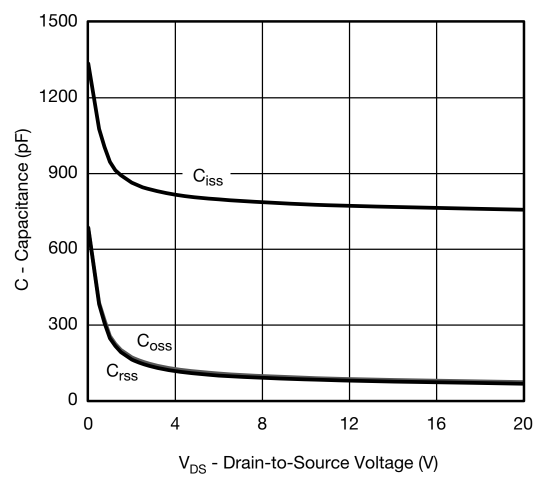
Output Characteristics



Transfer Characteristics

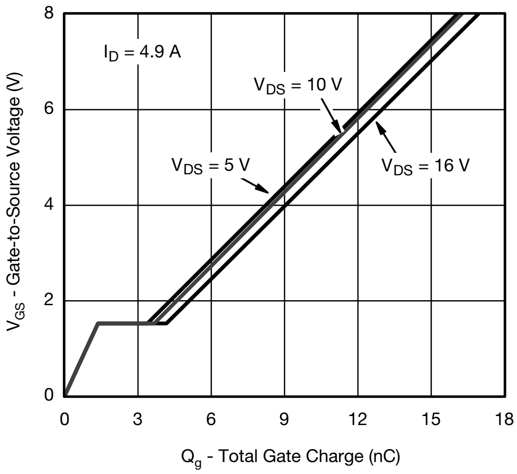


On-Resistance vs. Drain Current and Gate Voltage

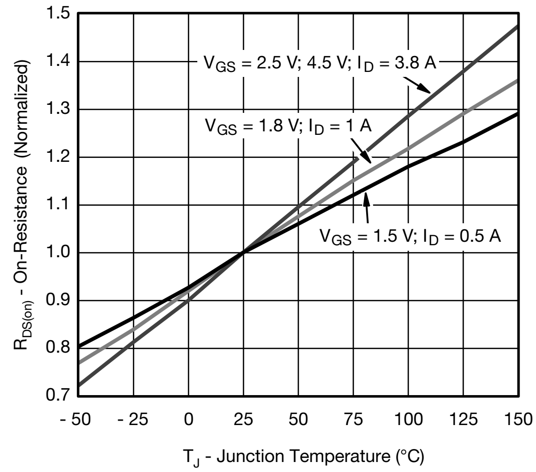


Capacitance

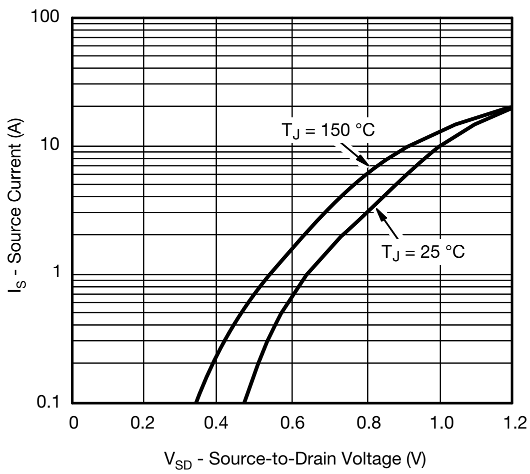
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



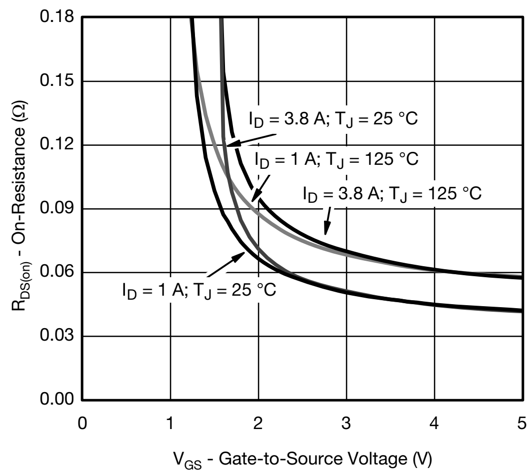
Gate Charge



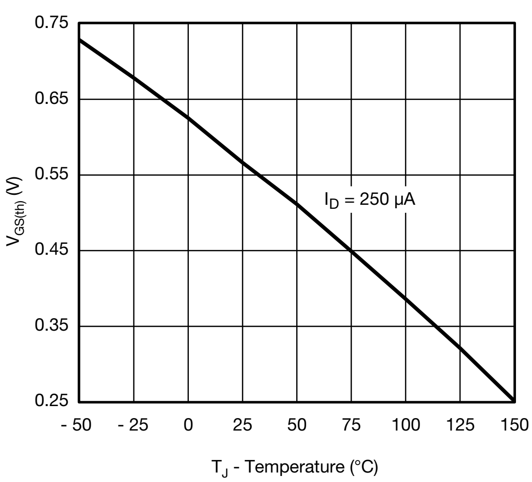
On-Resistance vs. Junction Temperature



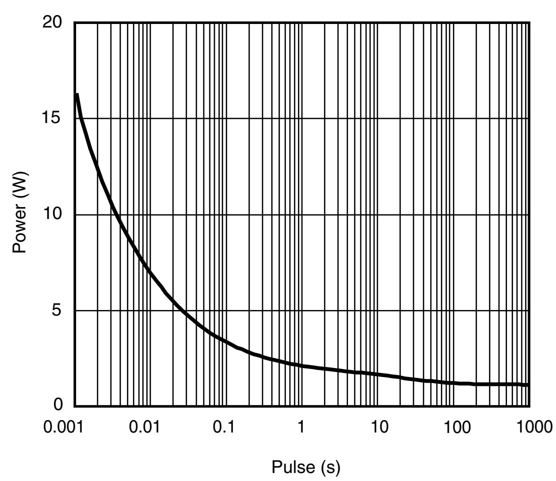
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

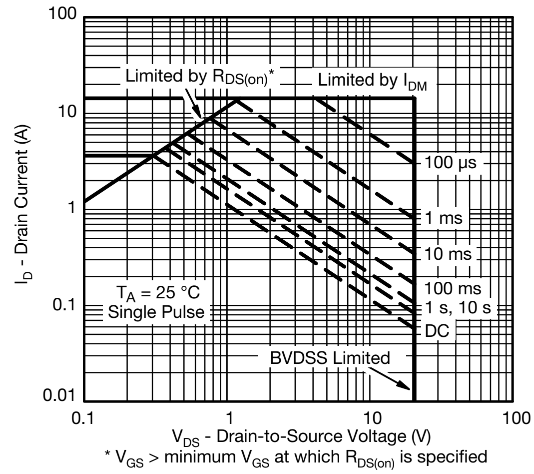


Threshold Voltage

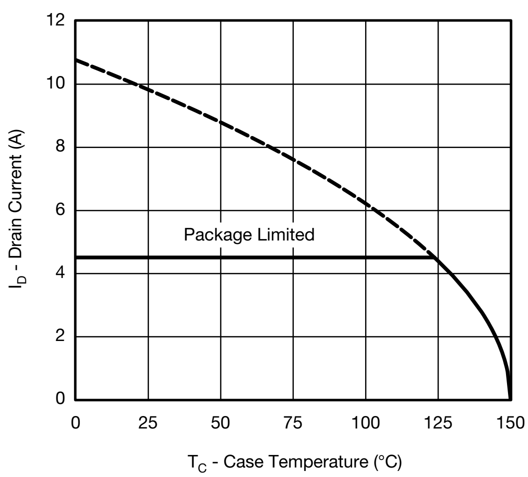


Single Pulse Power, Junction-to-Ambient

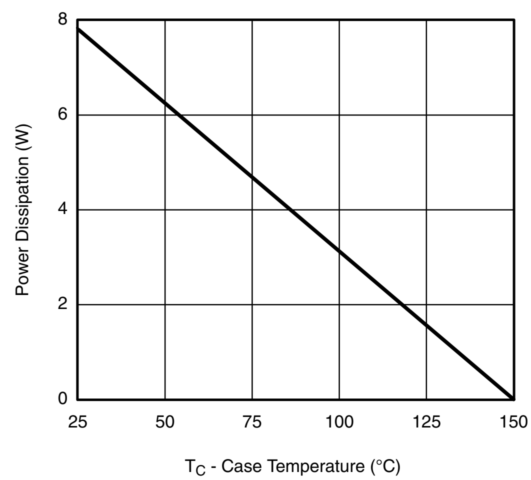
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating [a]

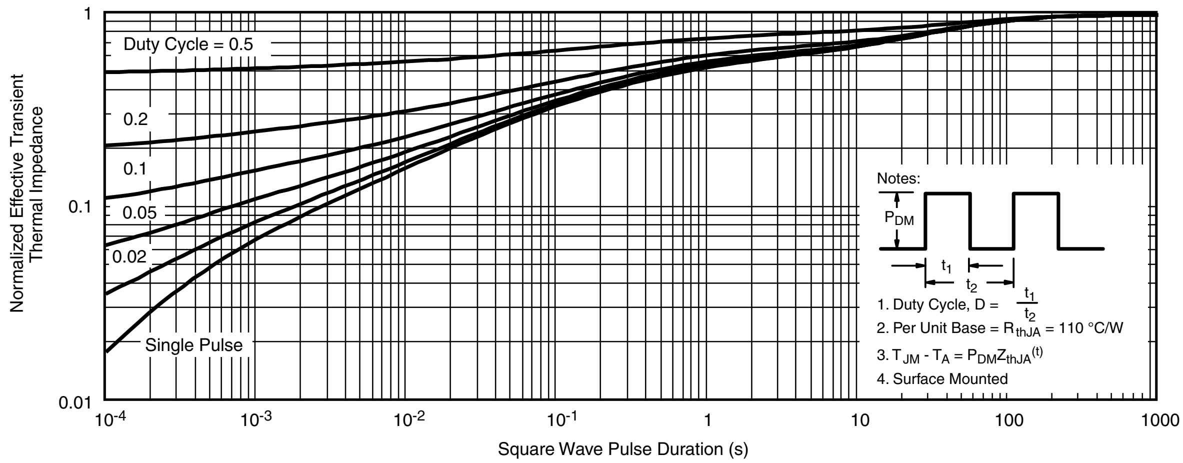


Power Derating

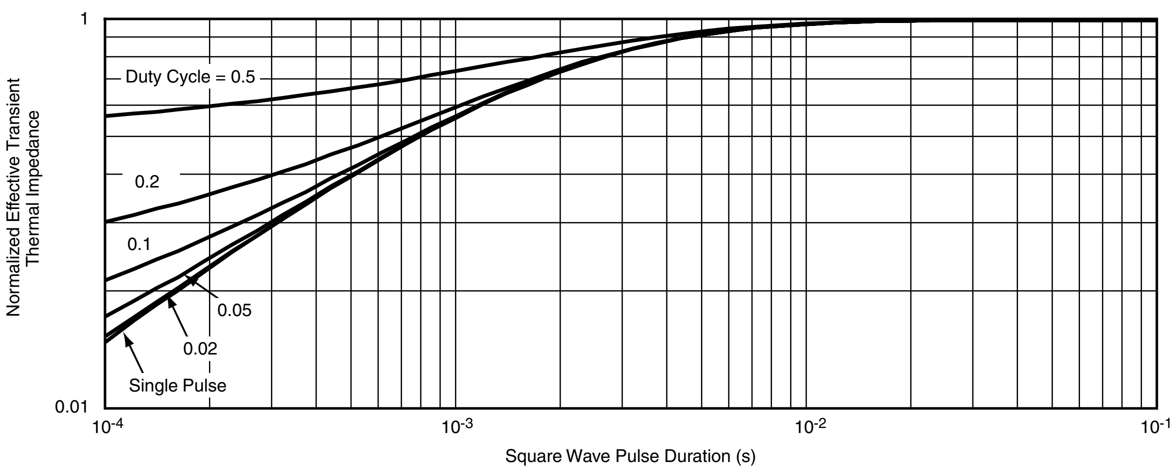
Note

a. The power dissipation P_D is based on T_J max.= 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



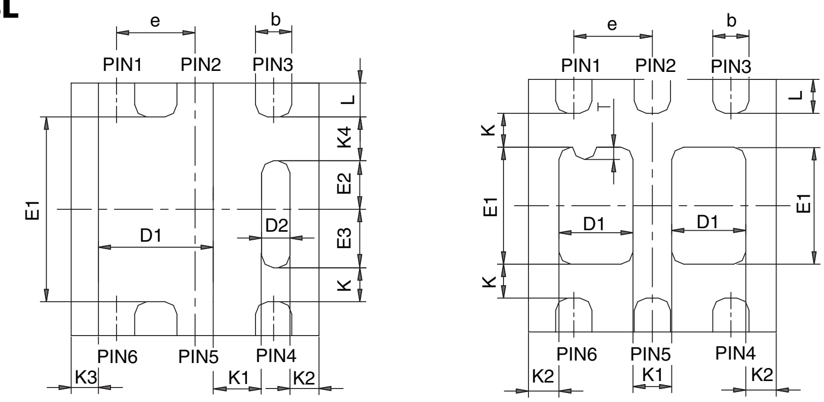
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

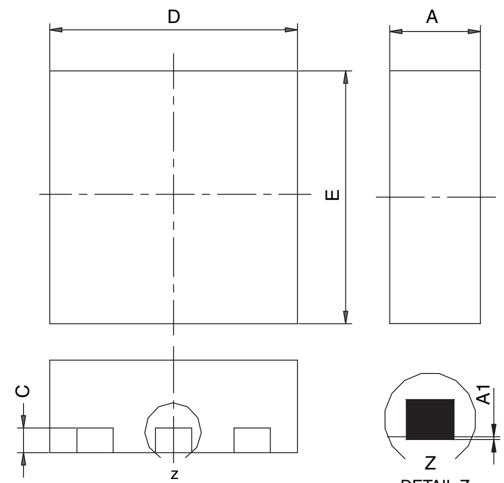
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62934.

PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



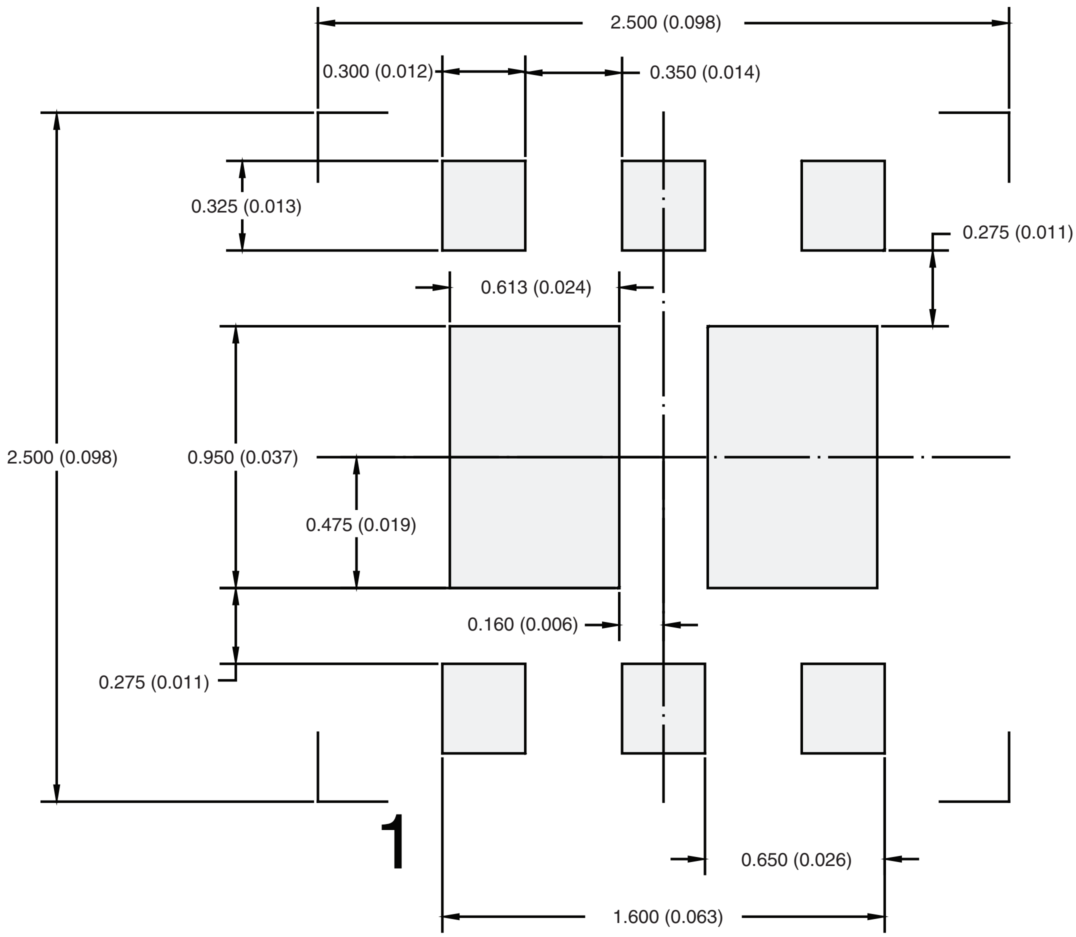
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 − Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

Return to Index

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.