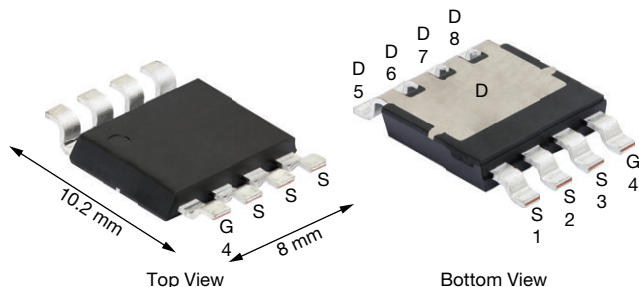


# Automotive N-Channel 100 V (D-S) 175 °C MOSFET

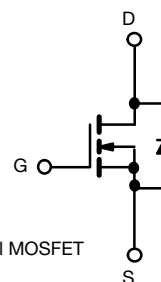
**PowerPAK® 8 x 8LR**


## FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.9 mm height
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



N-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	100
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.00253
$I_D$ (A)	296
Configuration	Single

## ORDERING INFORMATION

Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ112ER (for detailed order number please see <a href="http://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	100	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current	$I_D$	296	A
$T_C = 25$ °C		171	
Continuous source current (diode conduction)	$I_S$	545	
Pulsed drain current <sup>a</sup>	$I_{DM}$	655	
Single pulse avalanche current	$I_{AS}$	69	mJ
Single pulse avalanche energy	$E_{AS}$	242	
Maximum power dissipation	$P_D$	600	W
$T_C = 25$ °C		200	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>c</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	40	°C/W
Junction-to-case (drain)	$R_{thJC}$	0.25	

### Notes

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
b. When mounted on 1" square PCB (FR4 material)  
c. See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257))



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		100	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	3	3.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 175 °C	-	-	500	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	50	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0021	0.00253	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0054	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0068	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	45	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	11388	15 945	pF
Output capacitance	C <sub>oss</sub>			-	1326	1857	
Reverse transfer capacitance	C <sub>rss</sub>			-	80	112	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 20 A	-	181	272	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	48	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	37	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.7	1.5	2.3	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 2.5 Ω, I <sub>D</sub> ≥ 20 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	21	30	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	16	24	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	67	95	
Fall time <sup>c</sup>	t <sub>f</sub>			-	16	24	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	655	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		-	0.7	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 15 A, di/dt = 100 A/μs		-	70	140	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	172	344	nC
Reverse recovery fall time	t <sub>a</sub>			-	44	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	26	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	4.3	-	A

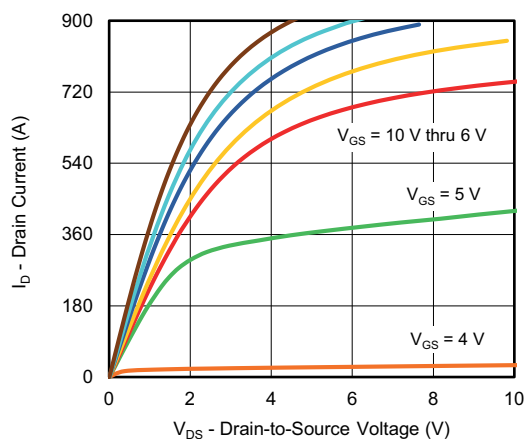
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

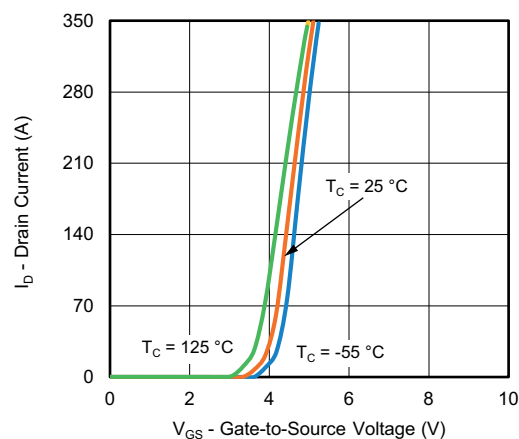
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



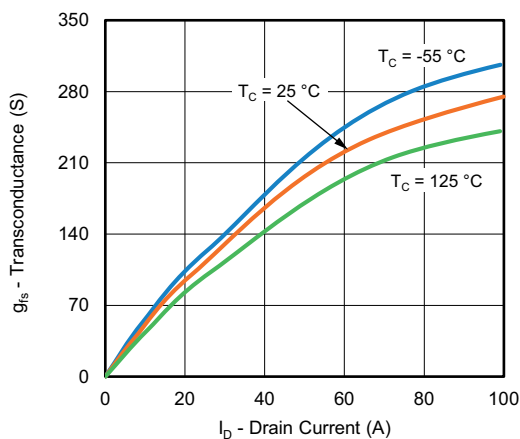
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



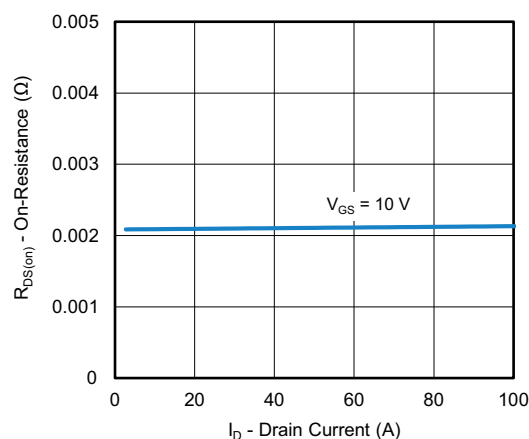
**Output Characteristics**



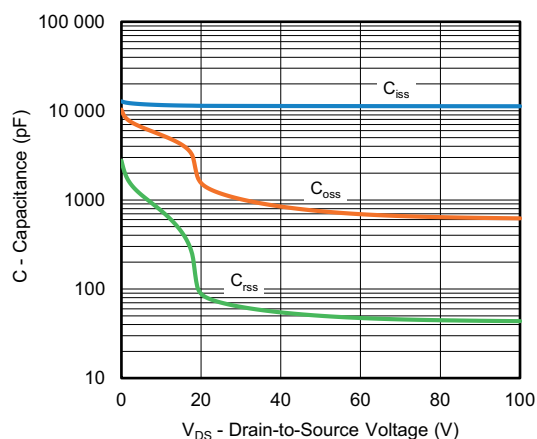
**Transfer Characteristics**



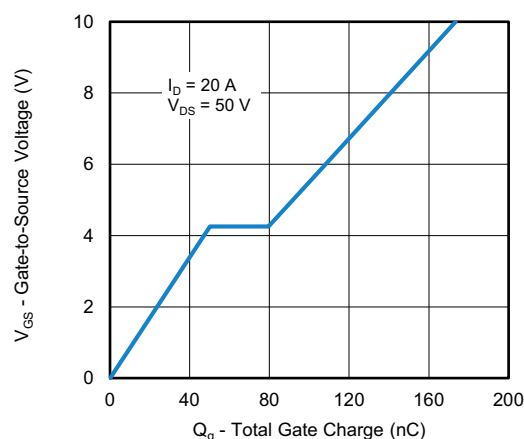
**Transconductance**



**On-Resistance vs. Drain Current**



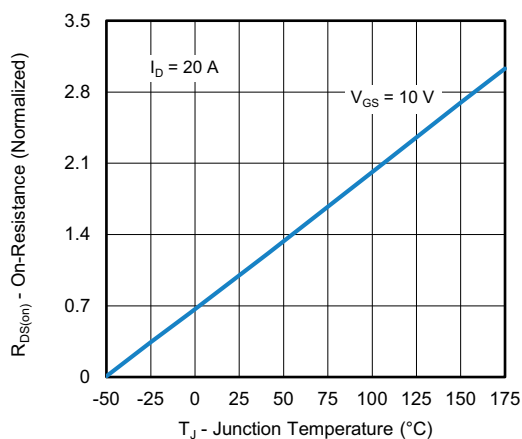
**Capacitance**



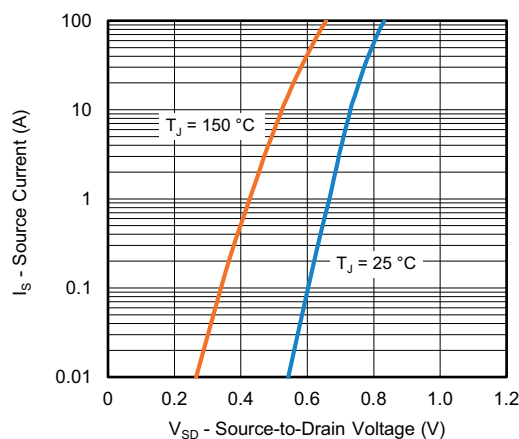
**Gate Charge**



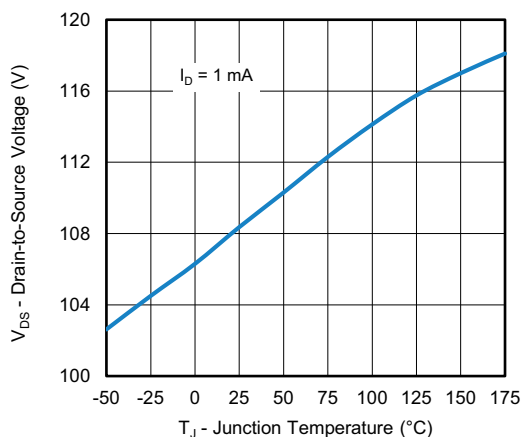
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



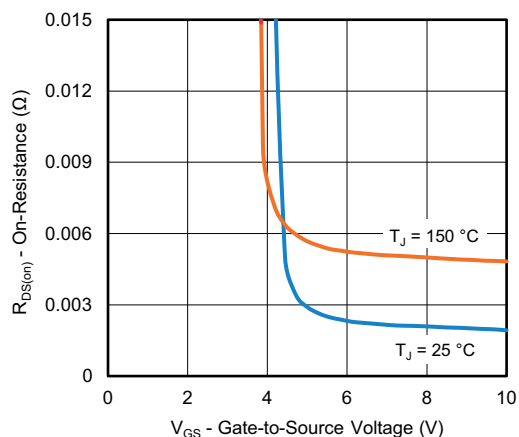
**On-Resistance vs. Junction Temperature**



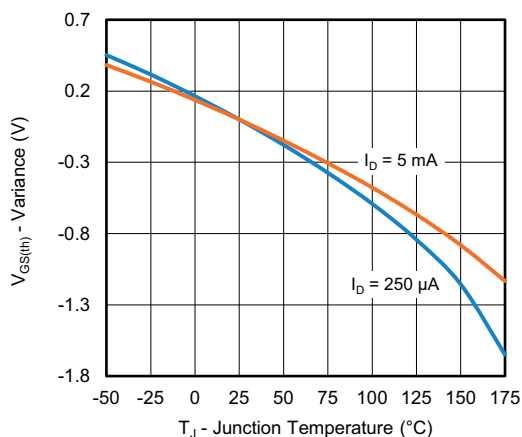
**Source Drain Diode Forward Voltage**



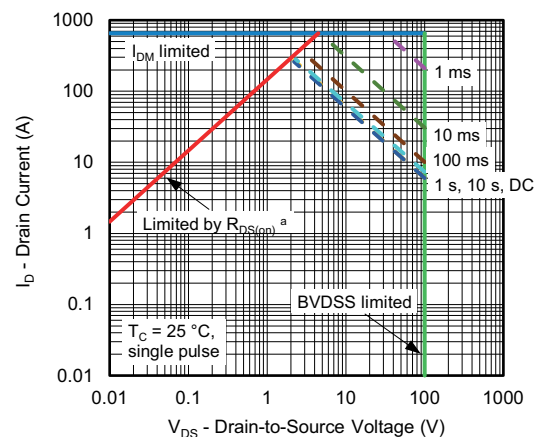
**Drain Source Breakdown vs. Junction Temperature**



**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



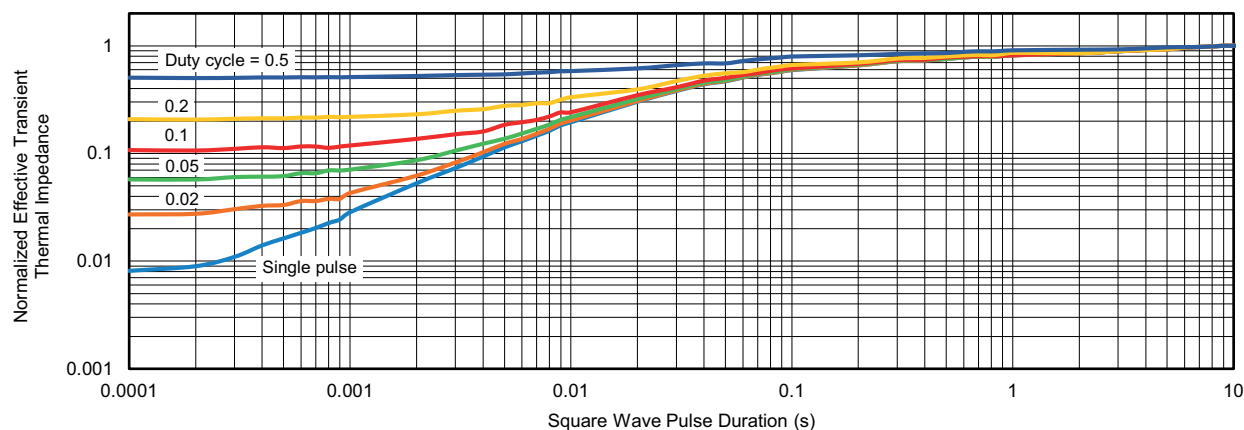
**Safe Operating Area**

**Note**

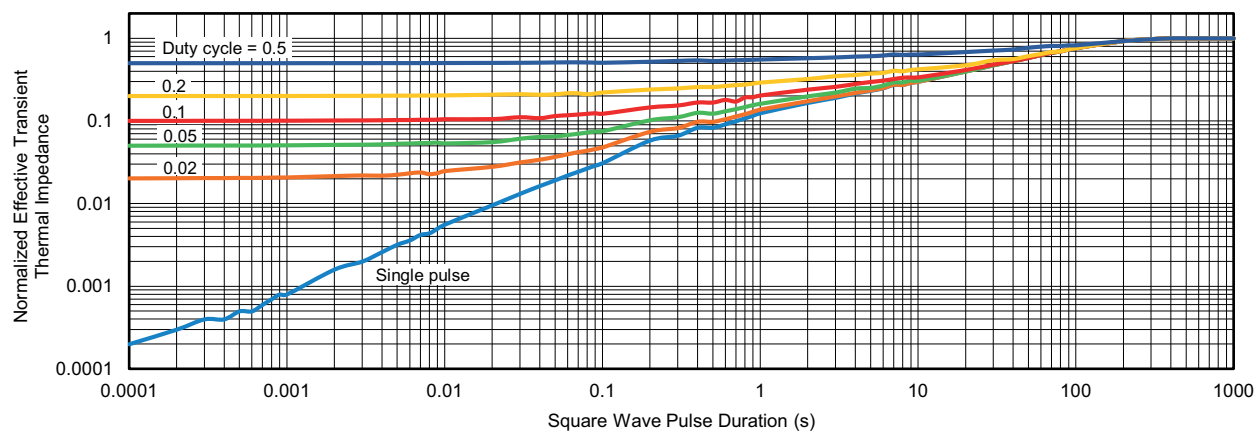
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



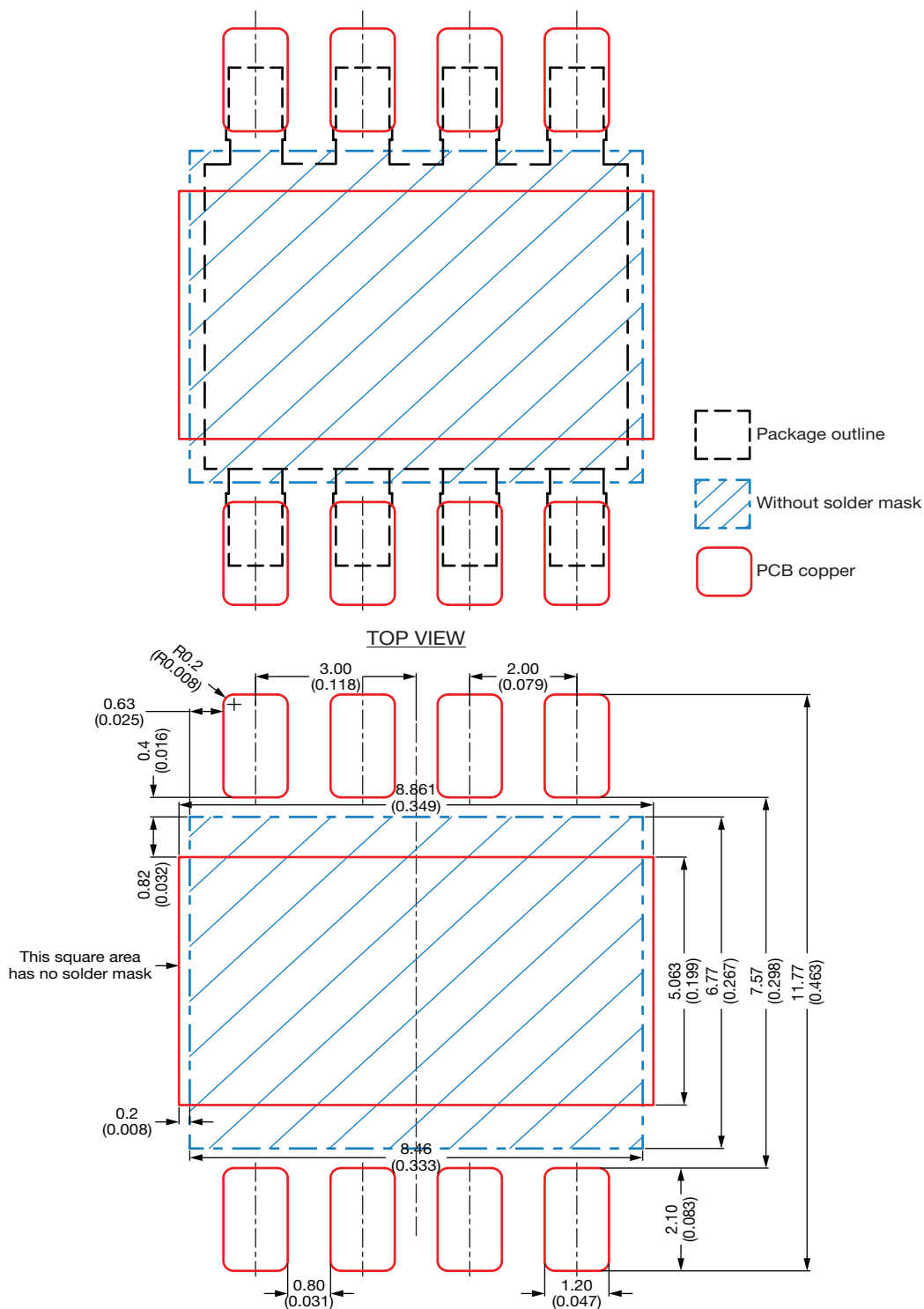
**Normalized Thermal Transient Impedance, Junction-to-Case**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

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# Recommended Land Pattern PowerPAK® 8 x 8LR



## Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023

DWG: 3002



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