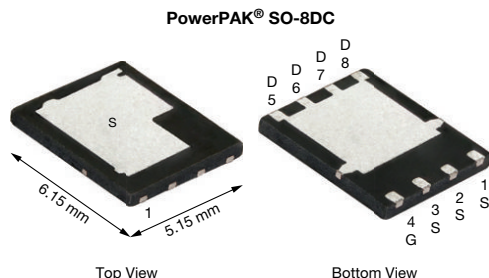


# N-Channel 100 V (D-S) MOSFET



## FEATURES

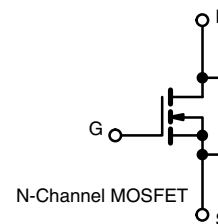
- TrenchFET® Gen IV power MOSFET
- Very low  $R_{DS(on)}$  -  $Q_g$  figure-of-merit (FOM)
- Tuned for the lowest  $R_{DS(on)}$  -  $Q_{oss}$  FOM
- Top side cooling feature provides additional venue for thermal transfer
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- OR-ing
- Power supplies
- Motor drive control
- Battery and load switch



PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00480
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.00505
$Q_g$ typ. (nC)	55
$I_D$ (A)	95
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR668DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	100	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	95	A	
	$T_C = 70^\circ\text{C}$	76		
	$T_A = 25^\circ\text{C}$	23.2 <sup>b, c</sup>		
	$T_A = 70^\circ\text{C}$	18.6 <sup>b, c</sup>		
Pulsed drain current ( $t = 100 \mu\text{s}$ )	$I_{DM}$	200	A	
Continuous source-drain diode current	$T_C = 25^\circ\text{C}$	94		
	$T_A = 25^\circ\text{C}$	5.6 <sup>b, c</sup>	mJ	
Single pulse avalanche current	$L = 0.1$ mH	35		
Single pulse avalanche energy	$E_{AS}$	61.2	W	
Maximum power dissipation	$T_C = 25^\circ\text{C}$	125		
	$T_C = 70^\circ\text{C}$	80		
	$T_A = 25^\circ\text{C}$	6.25 <sup>b, c</sup>		
	$T_A = 70^\circ\text{C}$	4 <sup>b, c</sup>		
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) °		260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$t \leq 10$ s	$R_{thJA}$	15	20	$^\circ\text{C/W}$
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	0.8	1	
Maximum junction-to-case (source)	Steady state	$R_{thJC}$	1.1	1.4	

### Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is  $54^\circ\text{C/W}$
- $T_C = 25^\circ\text{C}$



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	70	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-7.2	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	3.4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00400	0.00480	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 15 A	-	0.00420	0.00505	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	-	85	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	5400	-	pF
Output capacitance	C <sub>oss</sub>		-	280	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	38	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	72	108	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 10 A	-	55	83	
Gate-drain charge	Q <sub>gd</sub>		-	21.6	-	
Output charge	Q <sub>oss</sub>		-	12	-	
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V	-	61	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.3	0.9	1.6	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	17	34	ns
Rise time	t <sub>r</sub>		-	22	44	
Turn-off delay time	t <sub>d(off)</sub>		-	30	60	
Fall time	t <sub>f</sub>		-	11	22	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 7.5 V, R <sub>g</sub> = 1 Ω	-	22	44	
Rise time	t <sub>r</sub>		-	25	50	
Turn-off delay time	t <sub>d(off)</sub>		-	38	76	
Fall time	t <sub>f</sub>		-	28	56	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	94	A
Pulse diode forward current	I <sub>SM</sub>		-	-	200	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.73	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	59	118	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	115	230	nC
Reverse recovery fall time	t <sub>a</sub>		-	37	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	22	-	

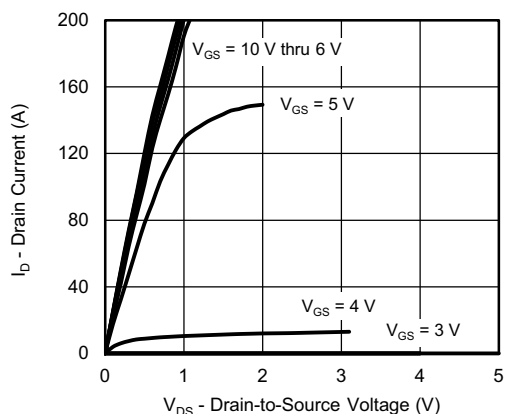
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

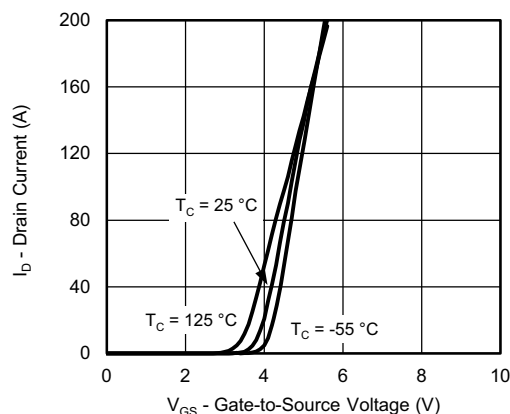
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



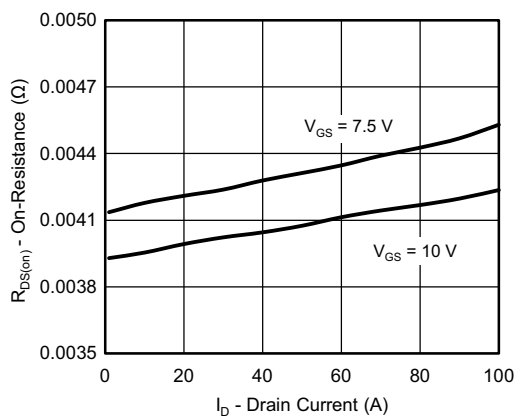
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



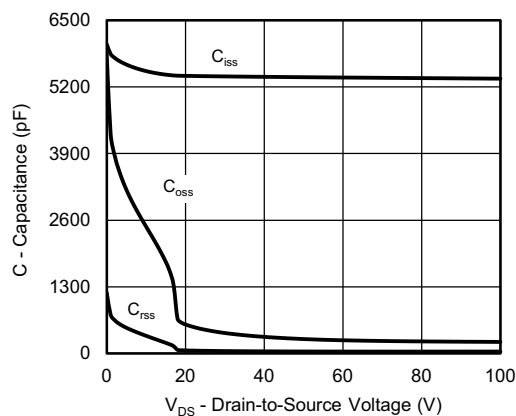
**Output Characteristics**



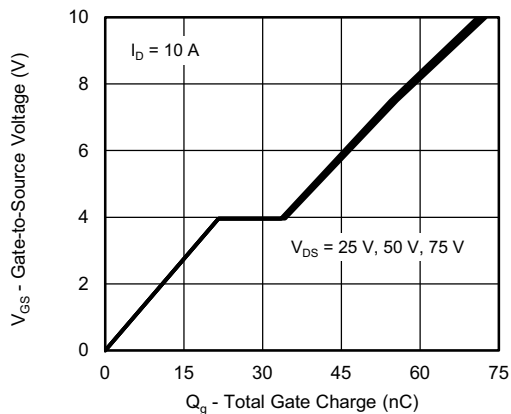
**Transfer Characteristics**



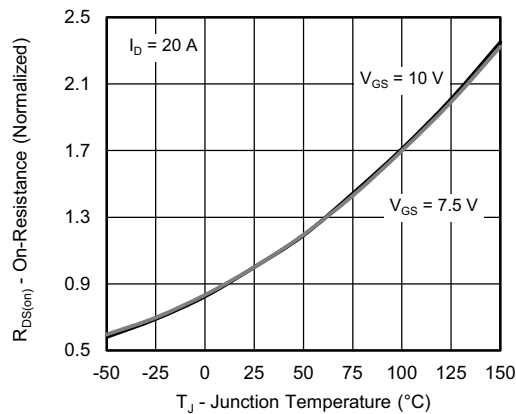
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



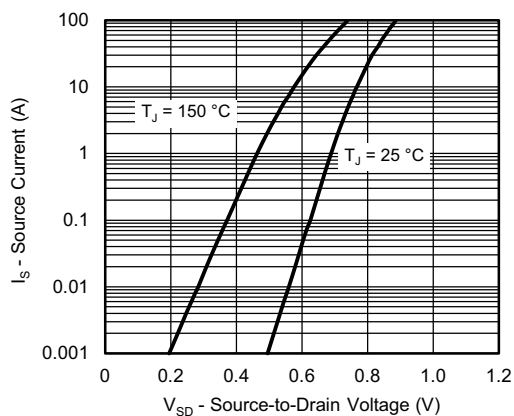
**Gate Charge**



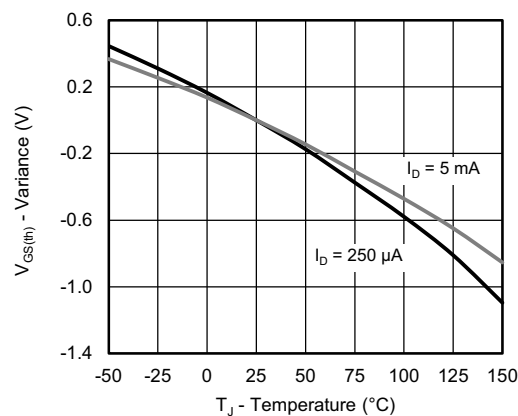
**On-Resistance vs. Junction Temperature**



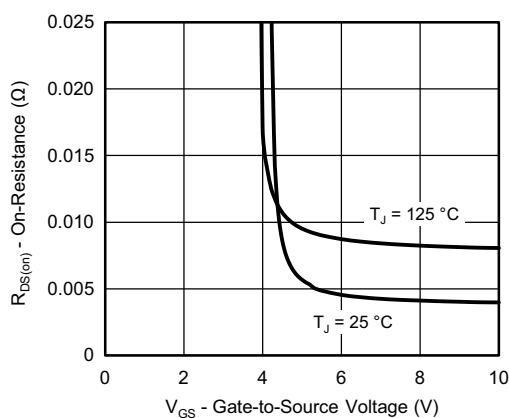
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



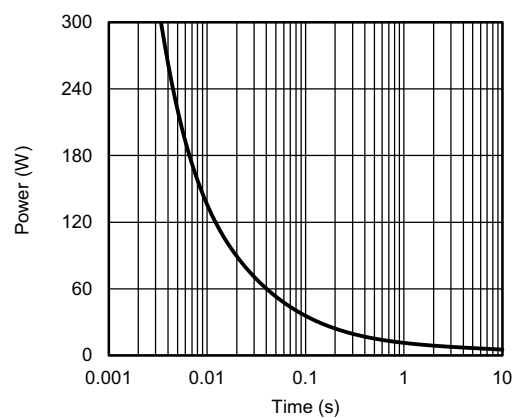
**Source-Drain Diode Forward Voltage**



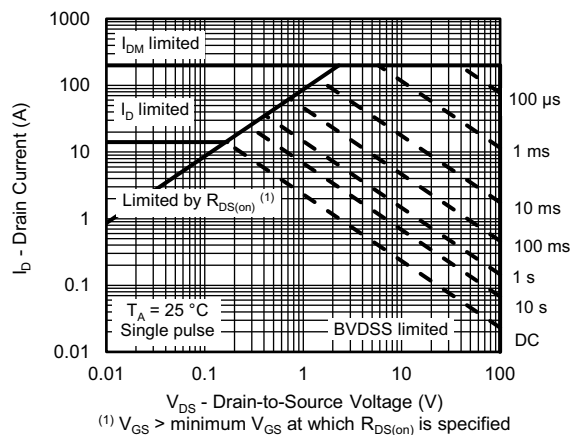
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



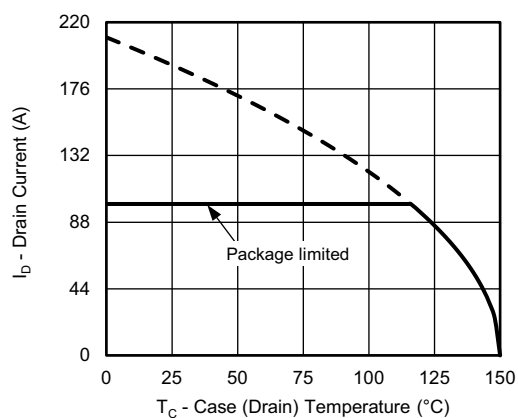
**Single Pulse Power, Junction-to-Ambient**



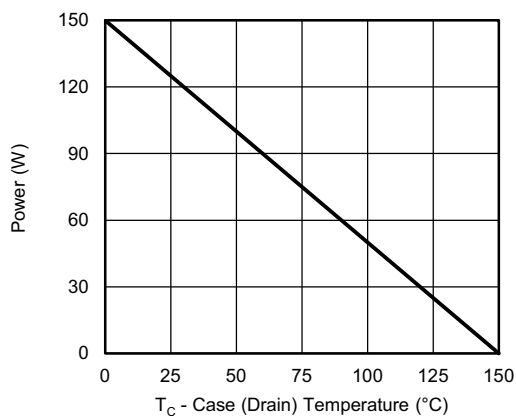
**Safe Operating Area, Junction-to-Ambient**



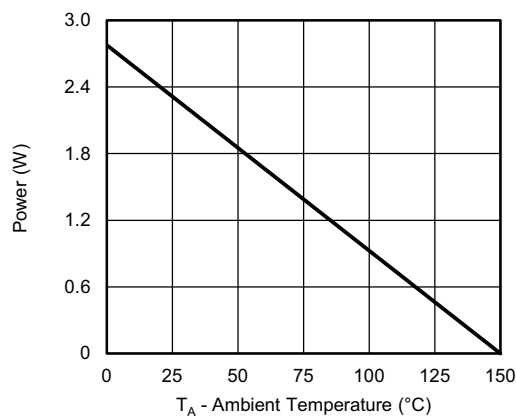
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



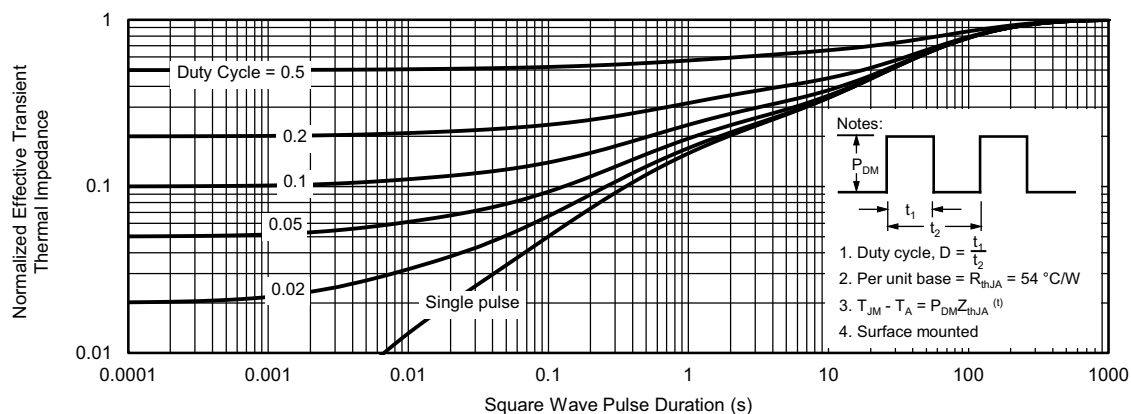
**Power, Junction-to-Ambient**

**Note**

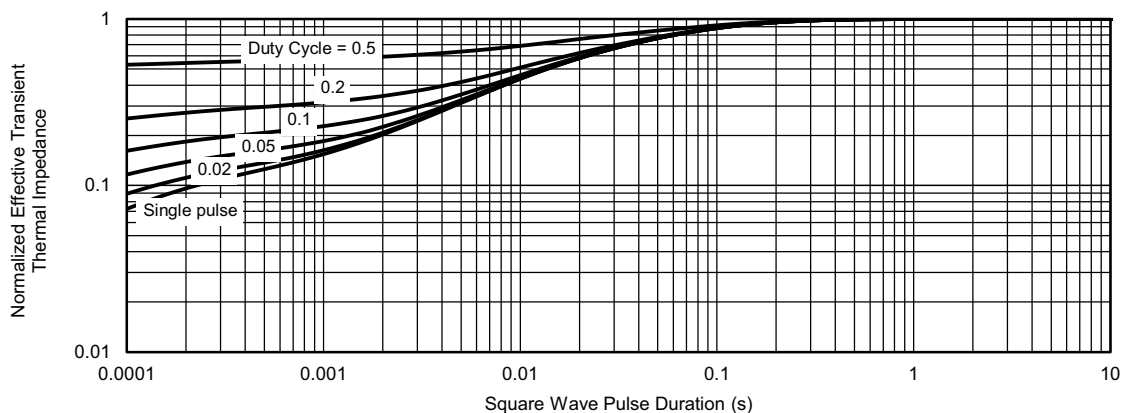
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



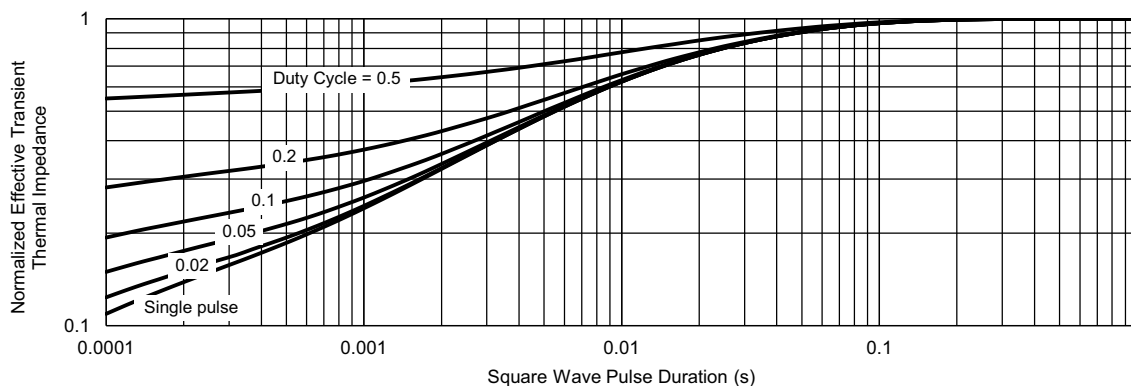
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case (Drain)**



**Normalized Thermal Transient Impedance, Junction-to-Case (Source)**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75751](http://www.vishay.com/ppg?75751).



## PowerPAK® SO-8 Double Cooling Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.51	0.56	0.61	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.36	0.41	0.46	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.71	3.76	3.81	0.146	0.148	0.150
e	1.27 BSC			0.050 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.60	3.65	3.70	0.142	0.144	0.146
E2	0.46 typ.			0.018 typ.		
H	0.49	0.54	0.59	0.019	0.021	0.023
K	1.22	1.27	1.32	0.048	0.050	0.052
K1	0.64 typ.			0.025 typ.		
L	0.49	0.54	0.59	0.019	0.021	0.023
M1	3.85	3.90	3.95	0.152	0.154	0.156
M2	2.74	2.79	2.84	0.108	0.110	0.112
M3	1.06	1.11	1.16	0.042	0.044	0.046
M4	0.56 typ.			0.022 typ.		
N	8			8		
T1	4.51	4.56	4.61	0.178	0.180	0.182
T2	2.58	2.63	2.68	0.102	0.104	0.106
T3	1.88	1.93	1.98	0.074	0.076	0.078
T4	0.97 typ.			0.038 typ.		
T5	0.48 typ.			0.019 typ.		
ECN: T21-0014-Rev. B, 08-Feb-2021						
DWG: 6048						

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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