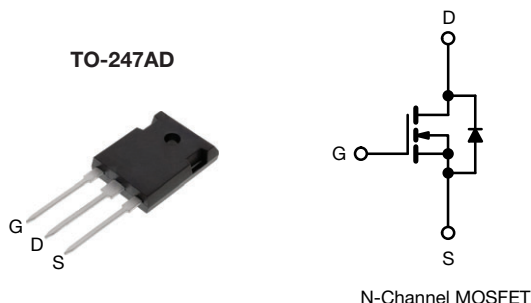


# E Series Power MOSFET With Fast Body Diode



## FEATURES

- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM):  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.095
$Q_g$ typ. (nC)	115	
$Q_{gs}$ (nC)	26	
$Q_{gd}$ (nC)	44	
Configuration	Single	

## APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter

## ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and halogen-free	SQW33N65EF-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	95	
Linear derating factor		2.5	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	508	mJ
Maximum power dissipation	$P_D$	375	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Drain-source voltage slope	$dV/dt$	100	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		50	
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	260	°C


### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6.0$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 160$  A/ $\mu$ s, starting  $T_J = 25$  °C

## THERMAL RESISTANCE RATINGS

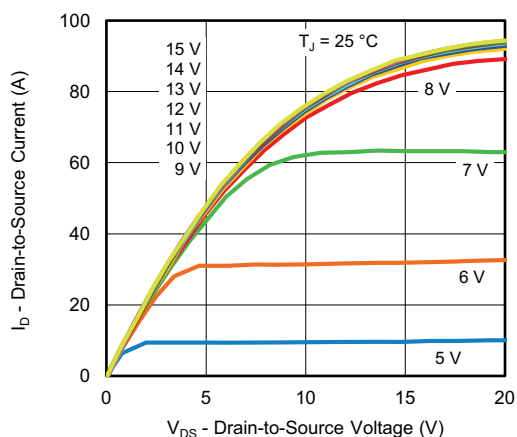
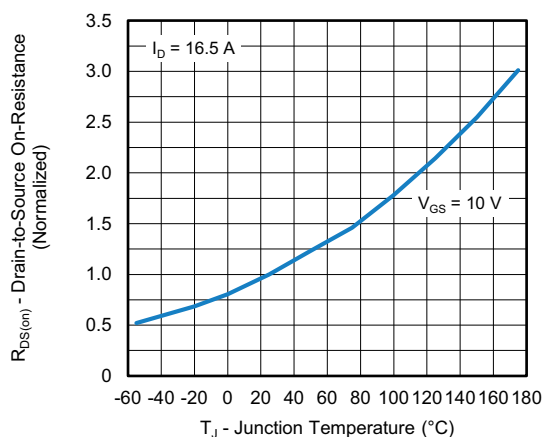
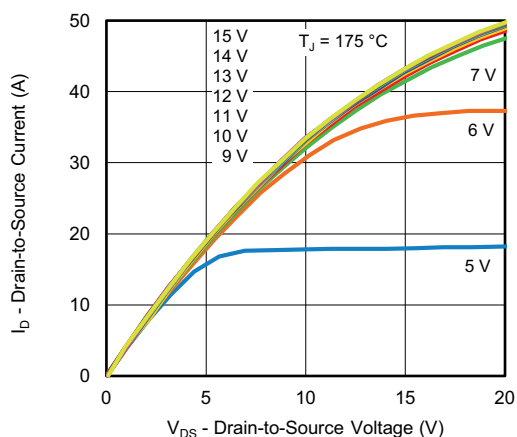
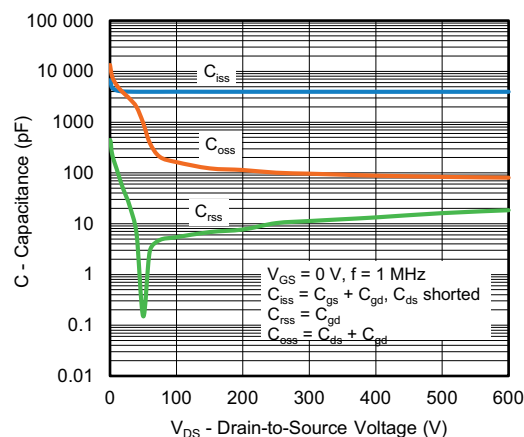
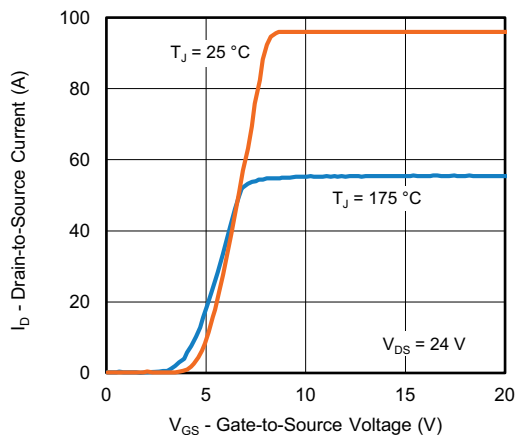
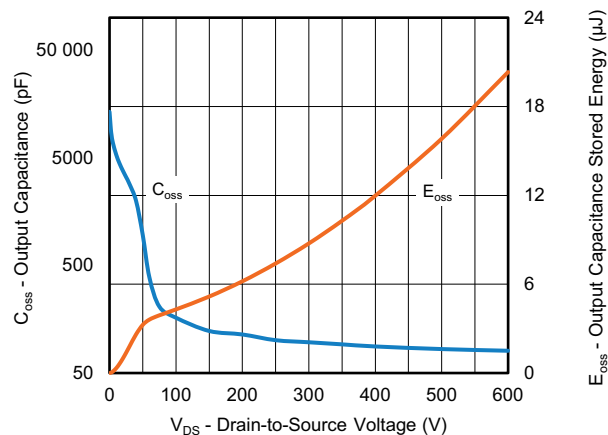
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.4	

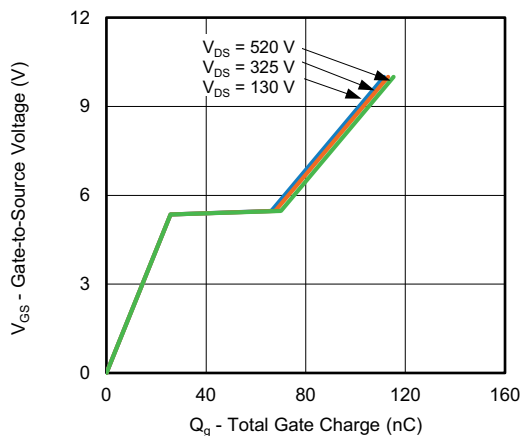
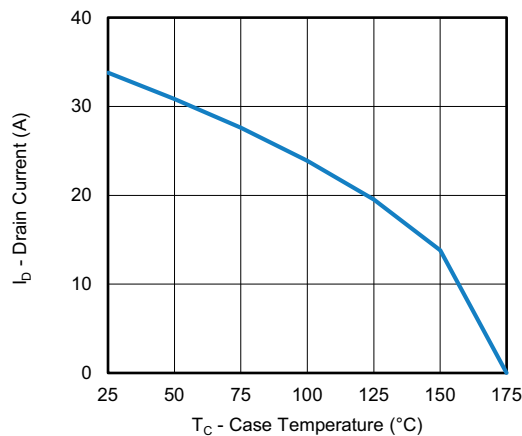
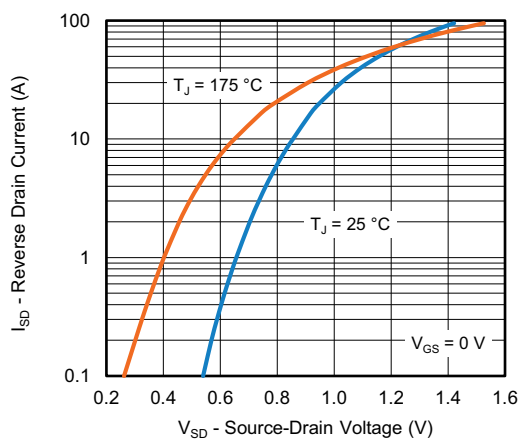
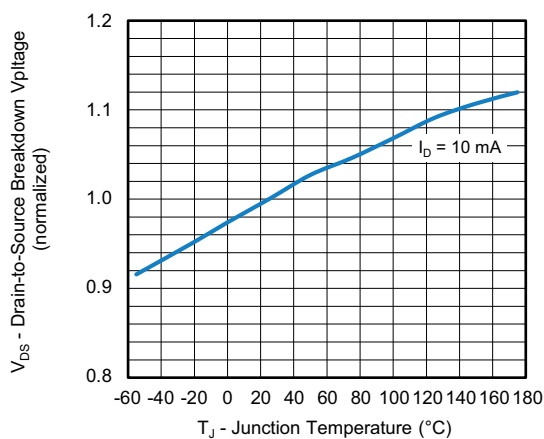
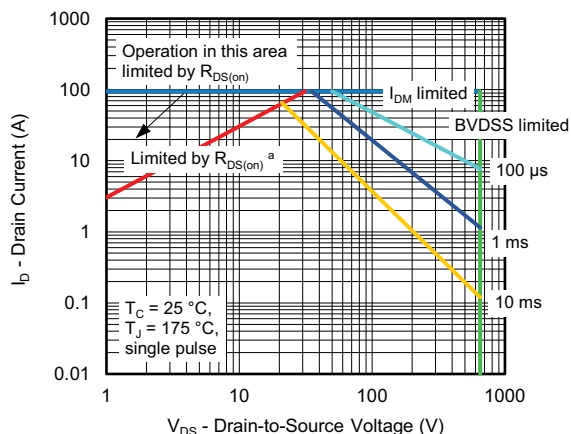


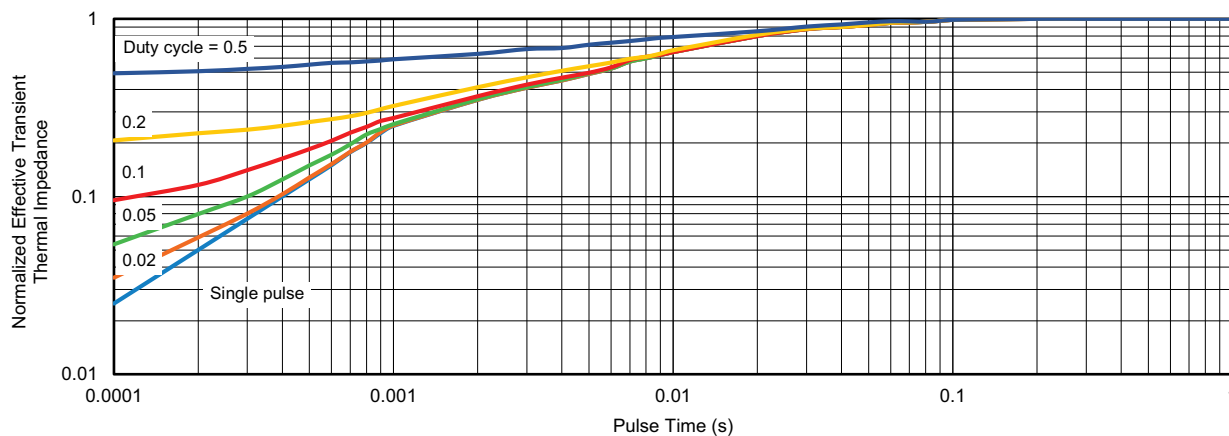
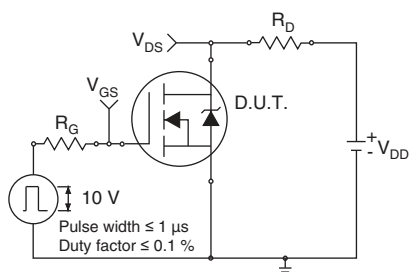
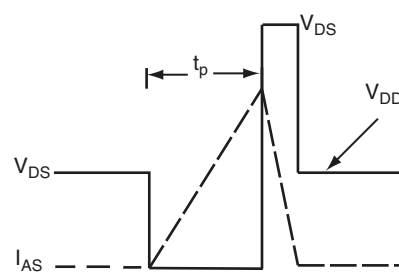
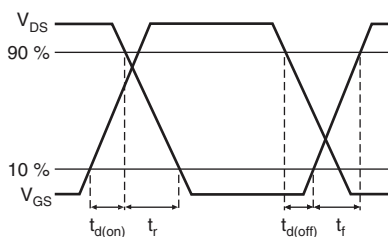
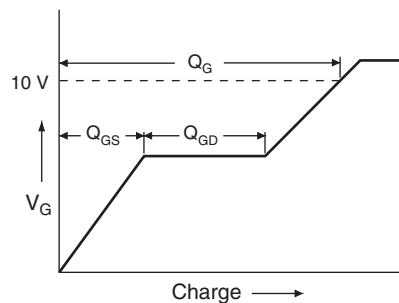
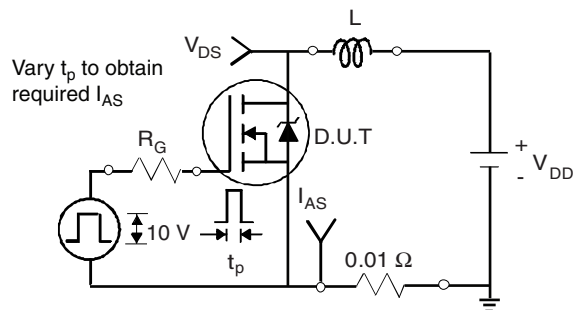
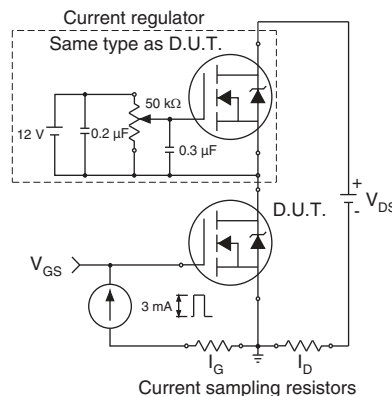
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 10 mA		-	0.69	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 16.5 A	-	0.095	0.109	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 16.5 A		-	13	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	3972	-	pF
Output capacitance	C <sub>oss</sub>			-	163	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	5	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 V to 520 V		-	117	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	482	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 16.5 A, V <sub>DS</sub> = 520 V	-	115	173	nC
Gate-source charge	Q <sub>gs</sub>			-	26	-	
Gate-drain charge	Q <sub>gd</sub>			-	44	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 16.5 A R <sub>g</sub> = 9.1 Ω, V <sub>GS</sub> = 10 V		-	32	64	ns
Rise time	t <sub>r</sub>			-	51	77	
Turn-off delay time	t <sub>d(off)</sub>			-	134	201	
Fall time	t <sub>f</sub>			-	62	93	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	34	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	95	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 16.5 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 16.5 A, dI/dt = 100 A/μs, V <sub>R</sub> = 400 V		-	178	356	ns
Reverse recovery charge	Q <sub>rr</sub>			-	1.4	2.8	μC
Reverse recovery current	I <sub>RRM</sub>			-	17	-	A

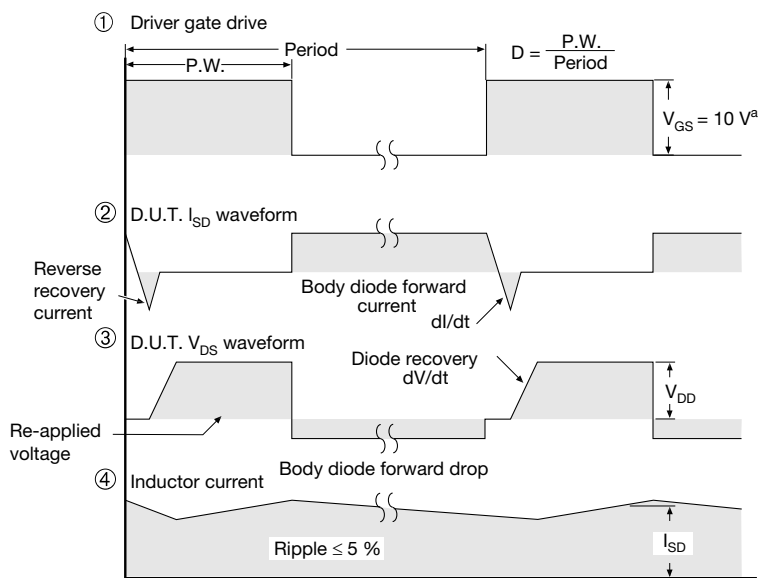
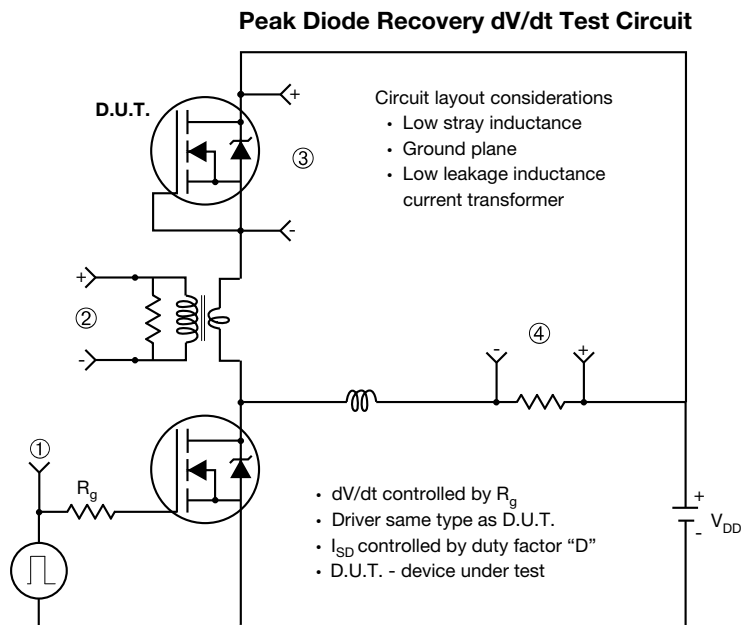
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature**

**Fig. 9 - Maximum Safe Operating Area**


**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**

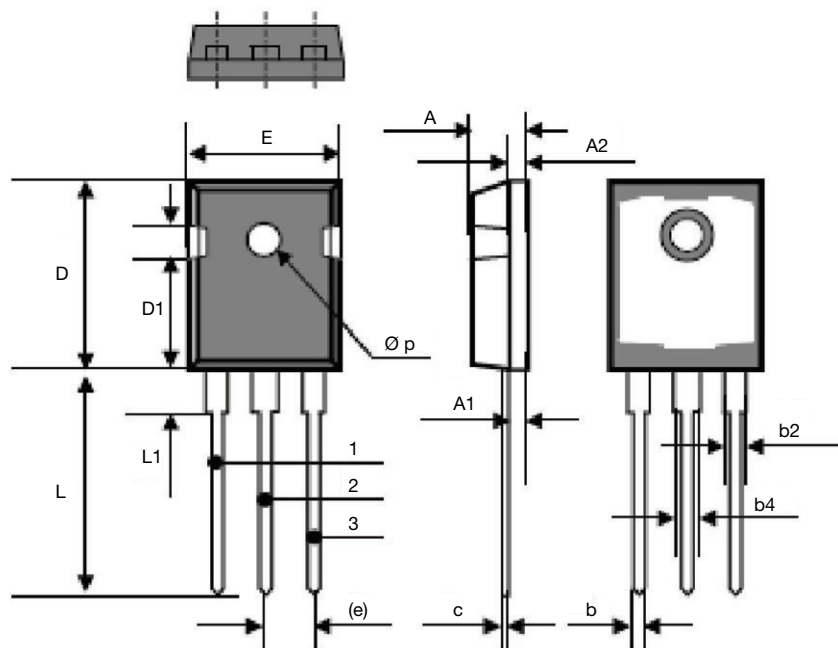

**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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## TO-247AD (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.31	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.41	0.065	0.095
b4	2.59	3.43	0.102	0.135
c	0.61 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	3.68	5.49	0.145	0.216
(e)	5.46 BSC		0.215 BSC	
E	15.49	16.26	0.610	0.640
L	19.81	20.32	0.780	0.800
L1	4.06	4.50	0.160	0.177
$\varnothing p$	3.51	3.66	0.138	0.144
ECN: S17-0178-Rev. B, 06-Feb-17 DWG: 6010				



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