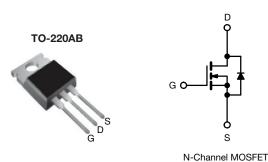


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	500			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	1.5		
Q _g max. (nC)	38			
Q _{gs} (nC)	5.0			
Q _{gd} (nC)	22			
Configuration	Single			

FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF830PbF
Lead (Pb)-free and halogen-free	IRF830PbF-BE3

ABSOLUTE MAXIMUM RATINGS (To	; = 25 °C, ur	less otherw	ise noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V_{DS}	500	V	
Gate-source voltage			V_{GS}	± 20	v	
Continuous drain current	V at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	I _D	4.5		
	V _{GS} at 10 V	T _C = 100 °C		2.9	Α	
Pulsed drain current ^a			I _{DM}	18		
Linear derating factor				0.59	W/°C	
Single pulse avalanche energy b			E _{AS}	280	mJ	
Repetitive avalanche current a			I _{AR}	4.5	А	
Repetitive avalanche energy ^a			E _{AR}	7.4	mJ	
Maximum power dissipation	T _C =	25 °C	P_{D}	74	W	
Peak diode recovery dV/dt ^c			dV/dt	3.5	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	90	
Soldering recommendations (peak temperature) ^d	For 10 s		-	300	°C	
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 24 mH, R_g = 25 Ω , I_{AS} = 4.5 A (see fig. 12)
- c. $I_{SD} \le 4.5$ A, $dI/dt \le 75$ A/ μ s, $V_{DD} \le V_{DS}$, $T_{J} \le 150$ °C
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	1.7		

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static		•					
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		500	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	Reference to 25 °C, I _D = 1 mA		0.61	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = '	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		-	4.0	V
Gate-source leakage	I _{GSS}	V	$V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
7		V _{DS} = 500 V, V _{GS} = 0 V	1	-	25		
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 400 \text{ V},$	V _{GS} = 0 V, T _J = 125 °C	1	-	250	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.7 A b	-	-	1.5	Ω
Forward transconductance	9fs	V _{DS} = 5	50 V, I _D = 2.7 A ^b	2.5	-	-	S
Dynamic		•				•	
Input capacitance	C _{iss}	$V_{GS} = 0 V$,		-	610	-	
Output capacitance	C _{oss}	\	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$		160	-	рF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see fig. 5		-	68	-	1 .
Total gate charge	Qg		$V_{GS} = 10 \text{ V}$ $I_D = 3.1 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 b	-	-	38	nC
Gate-source charge	Q _{gs}	V _{GS} = 10 V		1	-	5.0	
Gate-drain charge	Q_{qd}			1	-	22	
Turn-on delay Time	t _{d(on)}			-	8.2	-	ns
Rise time	t _r	$V_{DD} = 2$	V _{DD} = 250 V, I _D = 3.1 A		16	-	
Turn-off delay time	t _{d(off)}	$R_g = 12 \Omega$, $R_D = 79 \Omega$, see fig. 10 b		1	42	-	
Fall time	t _f			-	16	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	- nH
Internal source inductance	L _S			-	7.5	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.5	-	2.7	Ω
Drain-Source Body Diode Characteristic	es						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.5	A
Pulsed diode forward current ^a	I _{SM}			=	-	18	A
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 4.5 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	1.6	V
Body diode reverse recovery time	t _{rr}	- T _J = 25 °C, I _F = 3.1 A, dl/dt = 100 A/μs b		-	320	640	ns
Body diode reverse recovery charge	Q _{rr}			-	1.0	2.0	μC
Forward turn-on time	t _{on}	Intrinsic turi	-on is dor	minated b	y L _S and	L _D)	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300~\mu s;~duty~cycle \leq 2~\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

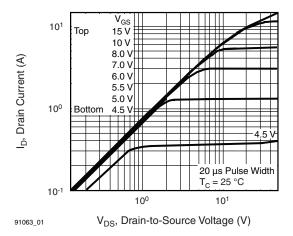


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

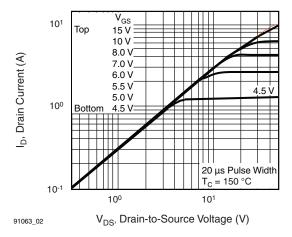


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

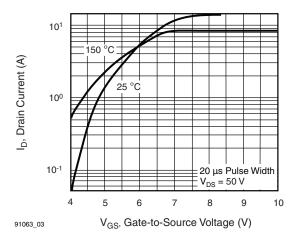


Fig. 3 - Typical Transfer Characteristics

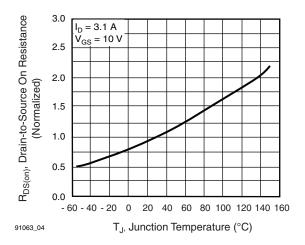


Fig. 4 - Normalized On-Resistance vs. Temperature

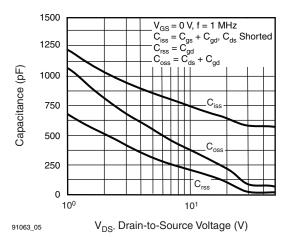


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

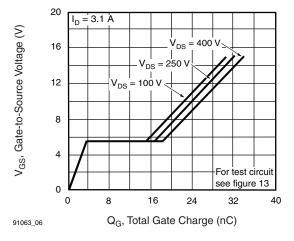


Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage



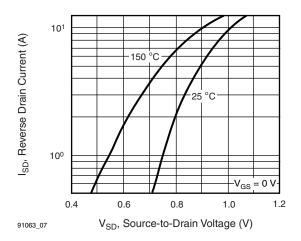


Fig. 7 - Typical Source-Drain Diode Forward Voltage

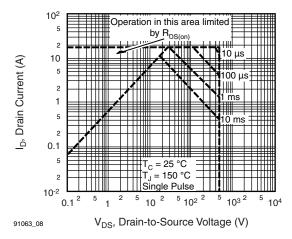


Fig. 8 - Maximum Safe Operating Area

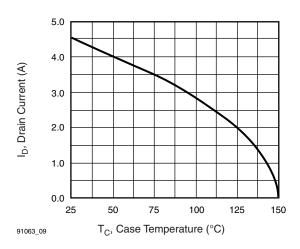


Fig. 9 - Maximum Drain Current vs. Case Temperature

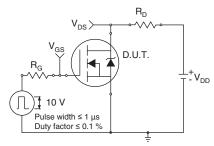


Fig. 10a - Switching Time Test Circuit

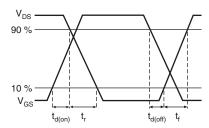


Fig. 10b - Switching Time Waveforms

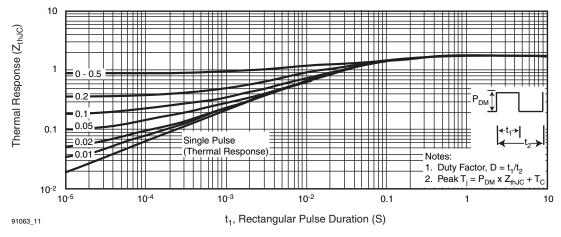


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



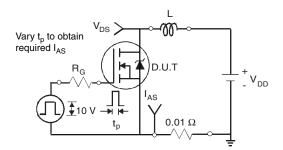


Fig. 12a - Unclamped Inductive Test Circuit

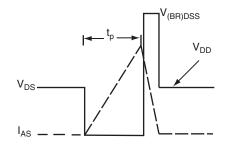


Fig. 12b - Unclamped Inductive Waveforms

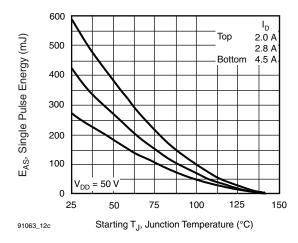


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

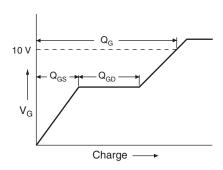


Fig. 13a - Basic Gate Charge Waveform

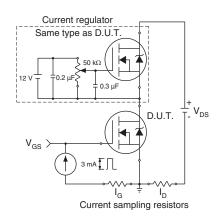
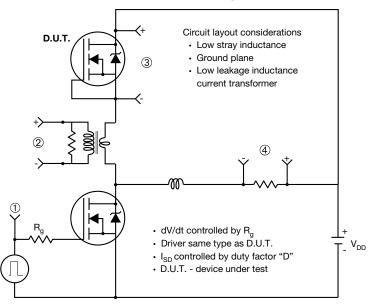


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



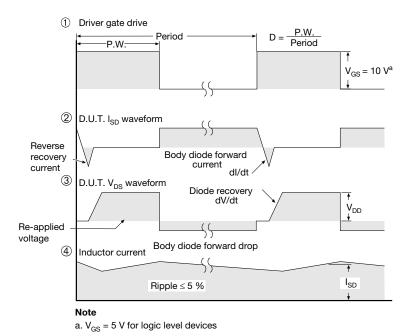


Fig. 14 - For N-Channel

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