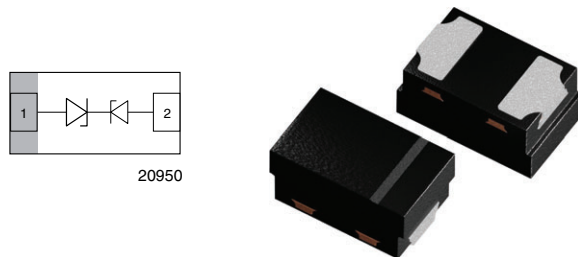


# Bidirectional Asymmetrical (BiAs) Single Line ESD Protection Diode in DFN1006-2A



20950

## MARKING (example only)



Bar = pin 1 marking

Y = type code (see table below)

X = date code

## LINKS TO ADDITIONAL RESOURCES



3D Models



Models



Application Notes

## FEATURES

- Ultra compact DFN1006-2A
- AEC-Q101 qualified available
- Low package height
- 1-line ESD protection
- Working range -7 V up to +14 V or -14 V up to +7 V
- Low leakage current  $< 0.1 \mu\text{A}$
- Low load capacitance typical  $C_D = 8 \text{ pF}$
- ESD immunity acc. IEC 61000-4-2  
 $\pm 25 \text{ kV}$  contact discharge  
 $\pm 30 \text{ kV}$  air discharge
- e3 - Sn  
Tin plated exposed side wall of lead frame  
- Soldering can be checked by standard vision inspection  
- AOI = automated optical inspection  
- No X-ray necessary
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## ORDERING INFORMATION

PART NUMBER (EXAMPLE)	AEC-Q101 QUALIFIED	ENVIRONMENTAL AND QUALITY CODE		PACKAGING CODE	ORDERING CODE
		RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS	TIN PLATED	10K PER 7" REEL (8 mm TAPE)	
		GREEN		MOQ = 10K	
VCUT0714BHD1	-	G	3	-08	VCUT0714BHD1-G3-08
VCUT0714BHD1	H	G	3	-08	VCUT0714BHD1HG3-08

## PACKAGE DATA

DEVICE NAME	PACKAGE NAME	PIN PLATING	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VCUT0714BHD1	DFN1006-2A	e3	2P	0.83 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

## ABSOLUTE MAXIMUM RATINGS

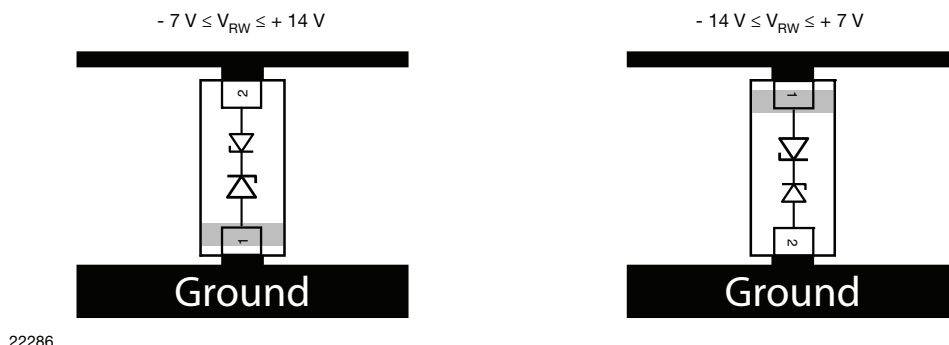
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Pin 1 to pin 2, acc. IEC 61000-4-5, 8/20 $\mu\text{s}$ /single shot	$I_{PPM}$	3.6	A
	Pin 2 to pin 1, acc. IEC 61000-4-5, 8/20 $\mu\text{s}$ /single shot		2	A
Peak pulse power	Pin 1 to pin 2, acc. IEC 61000-4-5, 8/20 $\mu\text{s}$ /single shot	$P_{PP}$	50	W
	Pin 2 to pin 1, acc. IEC 61000-4-5, 8/20 $\mu\text{s}$ /single shot		61	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 25$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 30$	kV
Operating temperature	Junction temperature; for AEC-Q101 qualified devices	$T_J$	-55 to +150	°C
Storage temperature		$T_{stg}$	-65 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

## CUT THE SPIKES

The VCUT0714BHD1 is a bidirectional but asymmetrical (BiAs) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT0714BHD1 offers a high isolation (low leakage current, small capacitance) within the specified working range of -7 V to +14 V or -14 V and +7 V. Due to the short leads and small package size of the tiny DFN1006-2A package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.



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### ELECTRICAL CHARACTERISTICS (pin 2 to pin 1)

(T<sub>amb</sub> = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	V <sub>RWM</sub>	-	-	14	V
Reverse voltage	At I <sub>R</sub> = 0.1 μA	V <sub>R</sub>	14	-	-	V
Reverse current	At V <sub>RWM</sub> = 14 V	I <sub>R</sub>	-	-	0.1	μA
Reverse breakdown voltage	At I <sub>R</sub> = 1 mA	V <sub>BR</sub>	14.5	-	-	V
Reverse clamping voltage	At I <sub>PP</sub> = 1 A	V <sub>C</sub>	-	-	27	V
	At I <sub>PP</sub> = I <sub>PPM</sub> = 2 A	V <sub>C</sub>	-	-	30	V
Capacitance	At V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>D</sub>	-	8	8.5	pF
	At V <sub>R</sub> = 7 V; f = 1 MHz	C <sub>D</sub>	-	4	-	pF

### ELECTRICAL CHARACTERISTICS (pin 1 to pin 2)

(T<sub>amb</sub> = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	V <sub>RWM</sub>	-	-	7	V
Reverse voltage	At I <sub>R</sub> = 0.1 μA	V <sub>R</sub>	7	-	-	V
Reverse current	At V <sub>RWM</sub> = 7 V	I <sub>R</sub>	-	-	0.1	μA
Reverse breakdown voltage	At I <sub>R</sub> = 1 mA	V <sub>BR</sub>	7.3	-	-	V
Reverse clamping voltage	At I <sub>PP</sub> = 1 A	V <sub>C</sub>	-	-	13	V
	At I <sub>PP</sub> = I <sub>PPM</sub> = 3.6 A	V <sub>C</sub>	-	-	15	V
Capacitance	At V = 0 V; f = 1 MHz	C <sub>D</sub>	-	8	8.5	pF
	At V = 3.5 V; f = 1 MHz	C <sub>D</sub>	-	6.4	-	pF

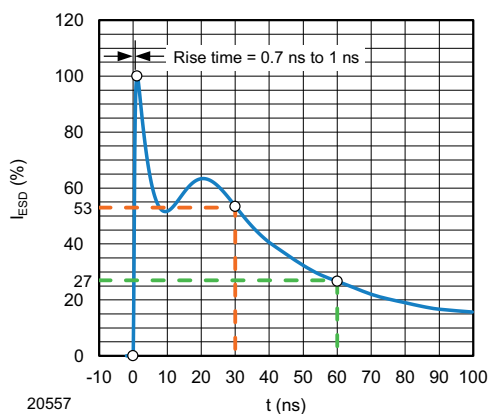
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

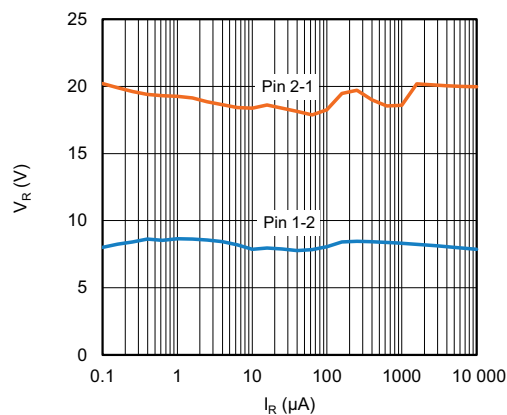


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

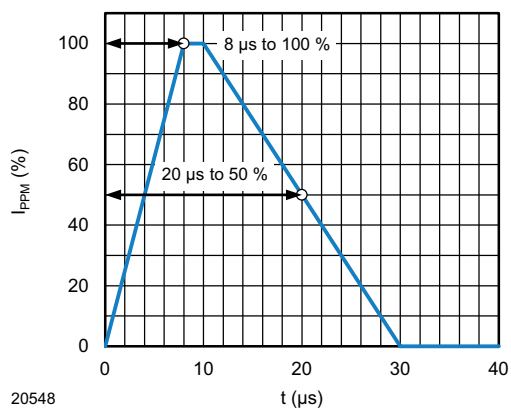


Fig. 2 - 8/20  $\mu$ s Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

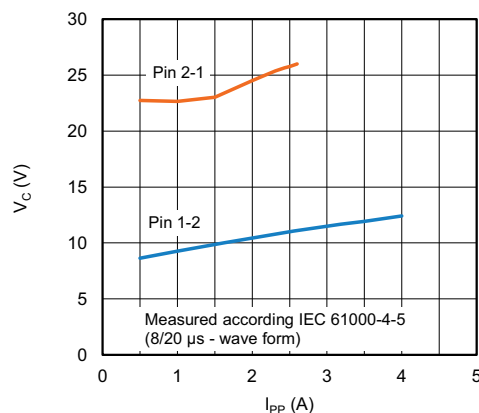


Fig. 5 - Typical Peak Clamping Voltage vs. Peak Pulse Current

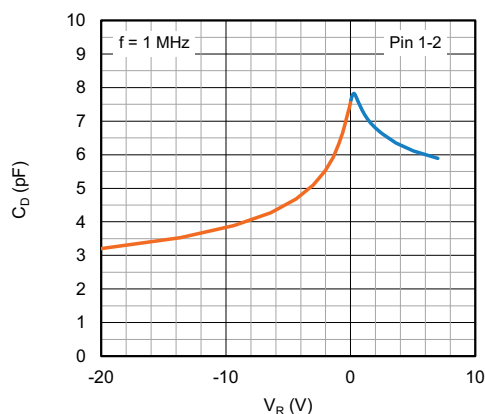


Fig. 3 - Typical Capacitance vs. Reverse Voltage

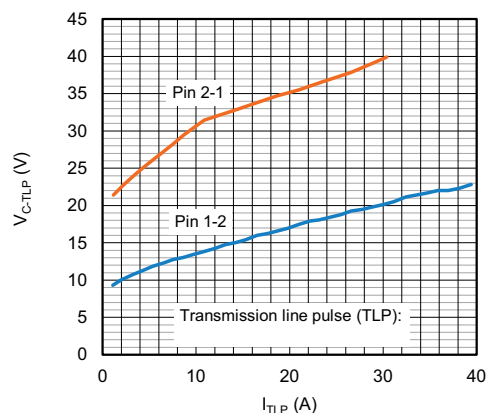
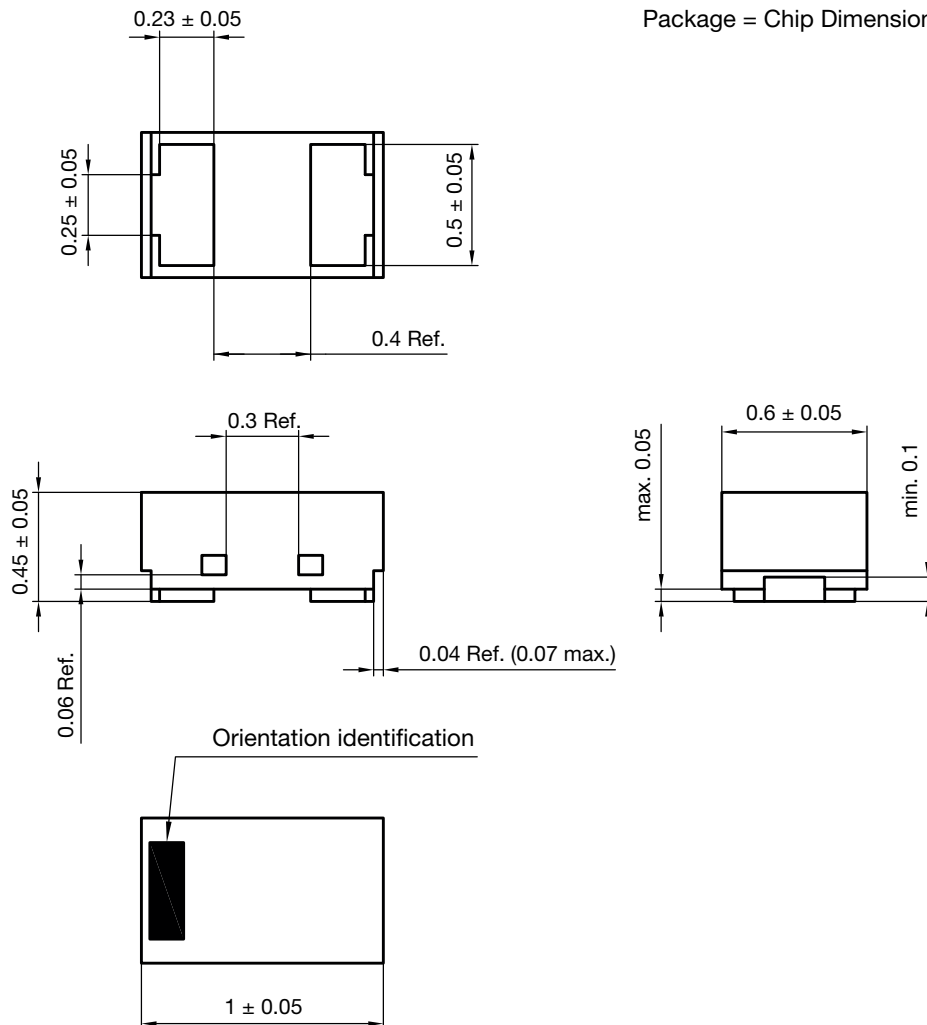
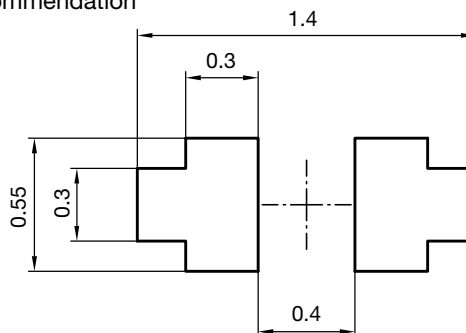


Fig. 6 - Typical Clamping Voltage vs. Peak Pulse Current

**PACKAGE DIMENSIONS** in millimeters (inches): **DFN1006-2A**

Package = Chip Dimension in mm

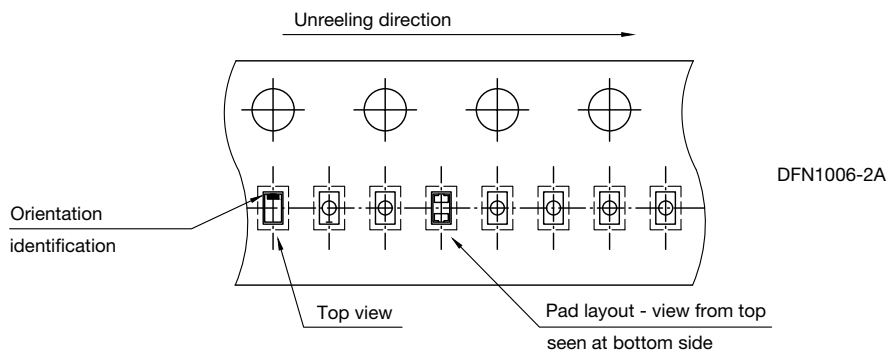

**Footprint recommendation**


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**ORIENTATION IN CARRIER TAPE: DFN1006-2A**



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02.05.2017  
22965



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