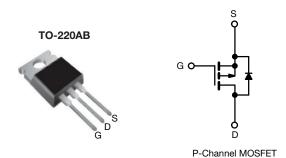


## **Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-200			
$R_{DS(on)}$ max. ( $\Omega$ )	$V_{GS} = -10 \text{ V}$	0.80		
Q <sub>g</sub> max. (nC)	29			
Q <sub>gs</sub> (nC)	5.4			
Q <sub>gd</sub> (nC)	15			
Configuration	Single			

#### **FEATURES**

- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

#### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

#### **DESCRIPTION**

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF9630PbF		
Lead (Pb)-free and halogen-free	IRF9630PbF-BE3		

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V <sub>DS</sub>	-200	V	
Gate-source voltage			V <sub>GS</sub>	± 20	7 v	
Continuous drain current	V -+ 10 V	T <sub>C</sub> = 25 °C		-6.5	А	
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	-4.0		
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	-26	1	
Linear derating factor				0.59	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	500	mJ	
Repetitive avalanche current <sup>a</sup>			I <sub>AR</sub>	-6.4	Α	
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	7.4	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	74	W	
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	-5.0	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 1	0 s		300		
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD}$  = -50 V, starting  $T_J$  = 25 °C, L = 17 mH,  $R_q$  = 25  $\Omega$ ,  $I_{AS}$  = -6.5 A (see fig. 12)
- c.  $I_{SD} \le -6.5 \text{ A}$ ,  $dI/dt \le 120 \text{ A/}\mu\text{s}$ ,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150 \text{ °C}$
- d. 1.6 mm from case



# Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.7	

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static							•
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-200	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	Reference to 25 °C, I <sub>D</sub> = -1 mA		-0.24	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V$	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-	-4.0	V
Gate-source leakage	I <sub>GSS</sub>	Vo	V <sub>GS</sub> = ± 20 V		-	± 100	nA
Zeve gets voltage due in comment	1	V <sub>DS</sub> = -200 V, V <sub>GS</sub> = 0 V		-	-	-100	, . ^
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS} = -160 \text{ V},$	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-500	μA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.9 A <sup>b</sup>	-	-	0.80	Ω
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = -5	50 V, I <sub>D</sub> = -3.9 A <sup>b</sup>	2.8	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = -25 \text{ V},$ f = 1.0  MHz,  see fig. 5		=	700	-	pF
Output capacitance	C <sub>oss</sub>			-	200	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	40	-	
Total gate charge	Qg		I <sub>D</sub> = -6.5 A, V <sub>DS</sub> = -160 V, see fig. 6 and 13 <sup>b</sup>	-	-	29	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V		-	-	5.4	
Gate-drain charge	Q <sub>gd</sub>			-	-	15	
Turn-on delay time	t <sub>d(on)</sub>			-	12	-	
Rise time	t <sub>r</sub>	V <sub>DD</sub> = -1	00 V, I <sub>D</sub> = -6.5 A,	-	27	-	
Turn-off delay time	t <sub>d(off)</sub>	$R_g = 12 \Omega$ , $R_D = 15 \Omega$ , see fig. 10 b		-	28	-	ns
Fall time	t <sub>f</sub>			-	24	-	
Gate input resistance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	- nH
Internal drain inductance	L <sub>S</sub>			-	7.5	-	
Internal source inductance	Rq	f = 1 MHz, open drain		0.6	-	3.7	Ω
Drain-Source Body Diode Characteristic					L	L	
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p -n junction diode		-	-	-6.5	
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	-26	A
Body diode voltage	V <sub>SD</sub>	$T_J = 25$ °C, $I_S = -6.5$ A, $V_{GS} = 0$ V b		-	-	-6.5	V
Body diode reverse recovery time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = -6.5 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}^{\text{b}}$		-	200	300	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	1.9	2.9	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turr	n-on time is negligible (turn	on is do	ninated b	y L <sub>S</sub> and	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq$  300  $\mu$ s; duty cycle  $\leq$  2 %



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

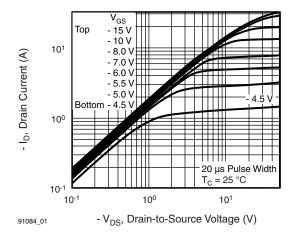


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

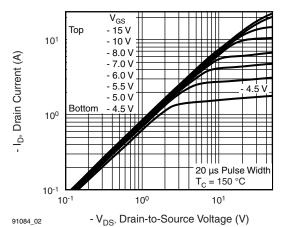


Fig. 2 - Typical Output Characteristics,  $T_C = 150$  °C

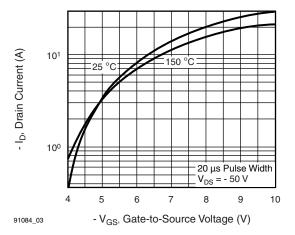


Fig. 3 - Typical Transfer Characteristics

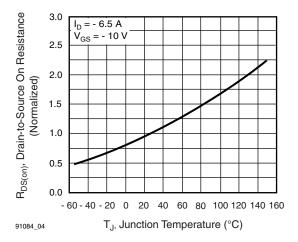


Fig. 4 - Normalized On-Resistance vs. Temperature

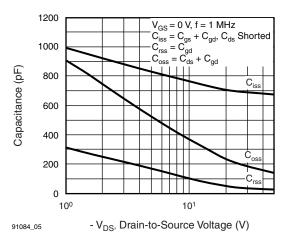


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

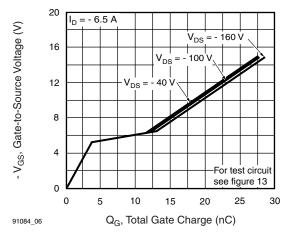


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



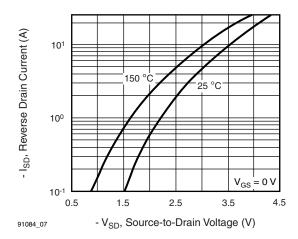


Fig. 7 - Typical Source-Drain Diode Forward Voltage

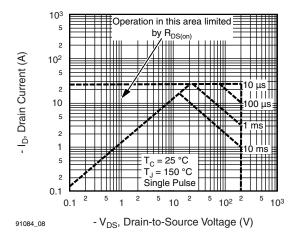


Fig. 8 - Maximum Safe Operating Area

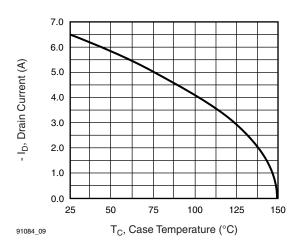


Fig. 9 - Maximum Drain Current vs. Case Temperature

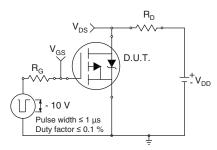


Fig. 10a - Switching Time Test Circuit

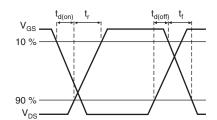


Fig. 10b - Switching Time Waveforms

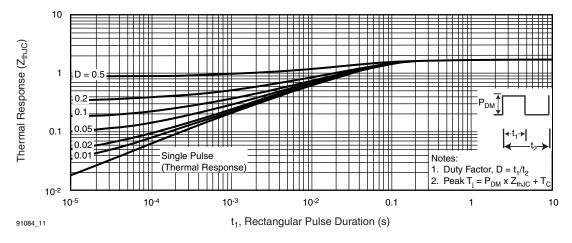


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



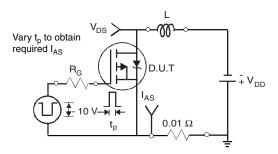


Fig. 12a - Unclamped Inductive Test Circuit

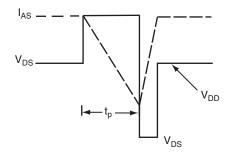


Fig. 12b - Unclamped Inductive Waveforms

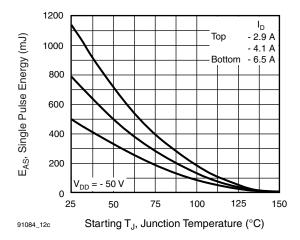


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

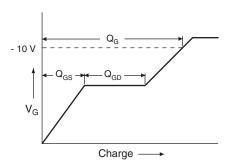


Fig. 13a - Basic Gate Charge Waveform

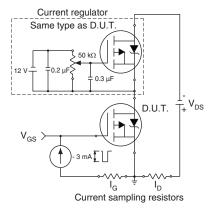
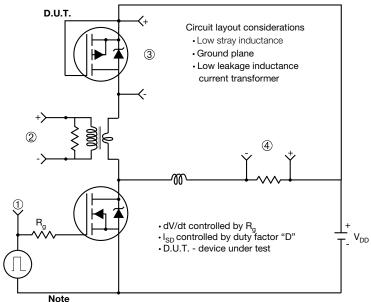


Fig. 13c - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver

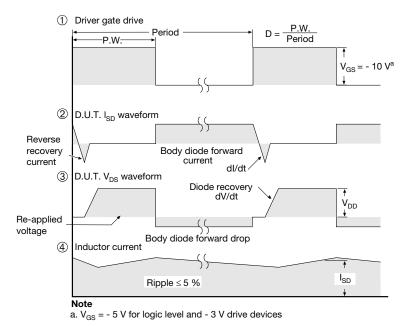


Fig. 14 - For P-Channel

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