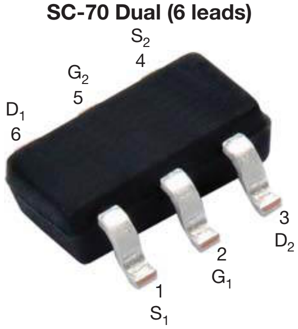
Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFET

SOT-363
SC-70 Dual (6 leads)



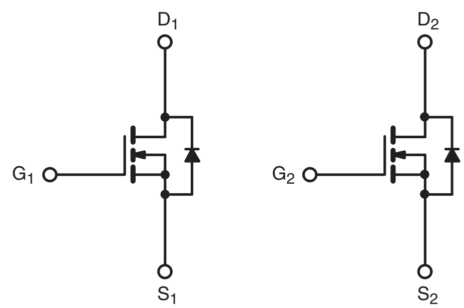
Top View

Marking Code: 9H

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE



PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.280
$R_{DS(on)}$ (Ω) at V_{GS} = 2.5 V	0.360
$R_{DS(on)}$ (Ω) at V_{GS} = 1.8 V	0.450
I_D (A)	0.8
Configuration	Dual
Package	SC-70

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current [a]	T_C = 25 °C	I_D	0.8	A
	T_C = 125 °C		0.8	
Continuous source current (diode conduction) [a]		I_S	0.8	
Pulsed drain current [b]		I_{DM}	3	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	3.8	
Single pulse avalanche energy		E_{AS}	7.2	mJ
Maximum power dissipation [b]	T_C = 25 °C	P_D	1.5	W
	T_C = 125 °C		0.5	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	220	°C/W
Junction-to-foot (drain)		R_{thJF}	100	

Notes
a. Package limited
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)

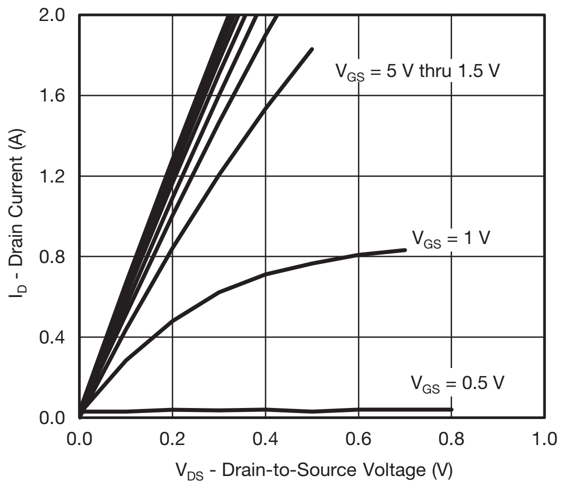
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA		20	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		0.45	0.6	1.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 20 V	-	-	1	μA
		V_{GS} = 0 V	V_{DS} = 20 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 20 V, T_J = 175 °C	-	-	150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 4.5 V	V_{DS} ≥ 5 V	1.5	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 1.2 A	-	0.200	0.280	Ω
		V_{GS} = 4.5 V	I_D = 1.2 A, T_J = 125 °C	-	-	0.423	
		V_{GS} = 4.5 V	I_D = 1.2 A, T_J = 175°C	-	-	0.510	
		V_{GS} = 2.5 V	I_D = 1 A	-	0.261	0.360	
		V_{GS} = 1.8 V	I_D = 0.2 A	-	0.320	0.450	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 0.5 A		-	2.6	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 10 V, f = 1 MHz	-	49	75	pF
Output capacitance	C_{oss}			-	22	32	
Reverse transfer capacitance	C_{rss}			-	8	12	
Total gate charge [c]	Q_g	V_{GS} = 4.5 V	V_{DS} = 10 V, I_D = 1.2 A	-	0.76	1.15	nC
Gate-source charge [c]	Q_{gs}			-	0.13	-	
Gate-drain charge [c]	Q_{gd}			-	0.33	-	
Gate resistance [d]	R_g	f = 1 MHz		5.5	11.1	22.2	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 10 V, R_L = 20 Ω I_D ≅ 0.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω		-	3	5	ns
Rise time [c]	t_r			-	21	31	
Turn-off delay time [c]	$t_{d(off)}$			-	19	29	
Fall time [c]	t_f			-	17	25	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	3	A
Forward voltage	V_{SD}	I_F = 0.5 A, V_{GS} = 0		-	0.8	1.2	V

Notes

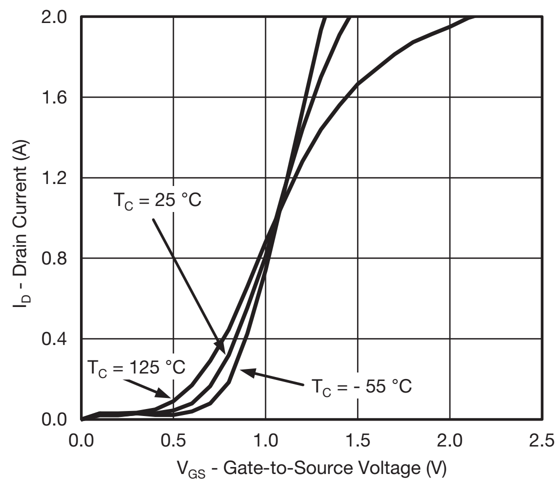
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

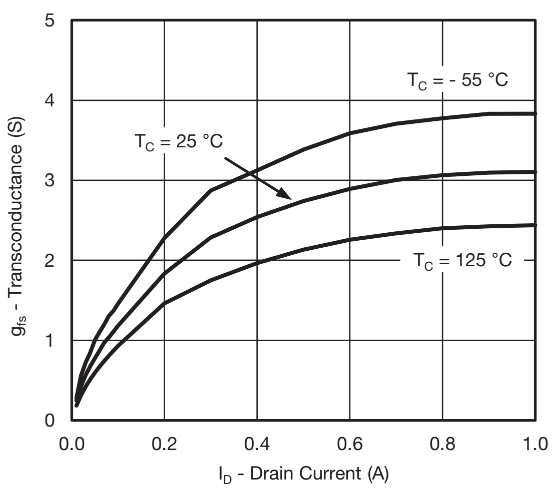
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



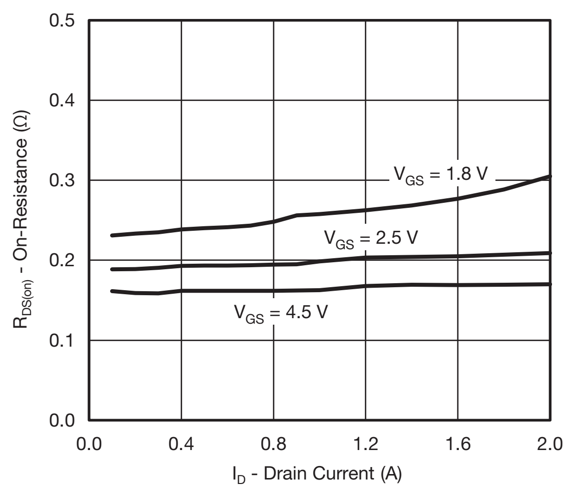
Output Characteristics



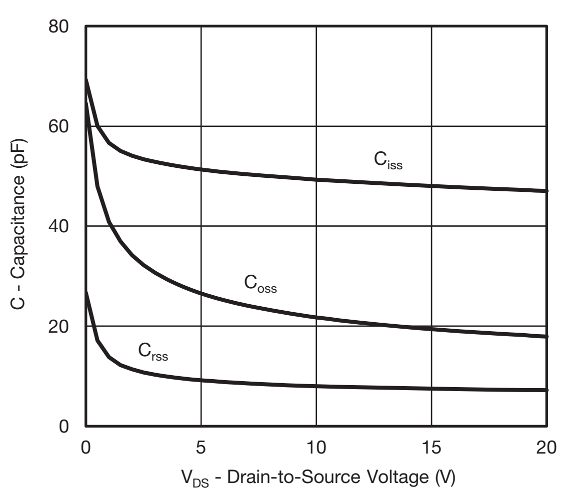
Transfer Characteristics



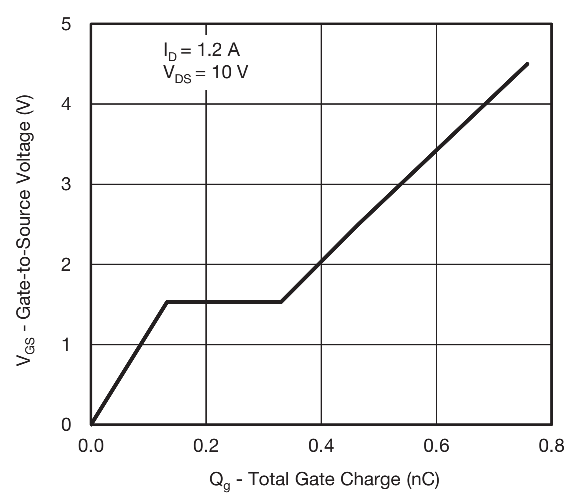
Transconductance



On-Resistance vs. Drain Current

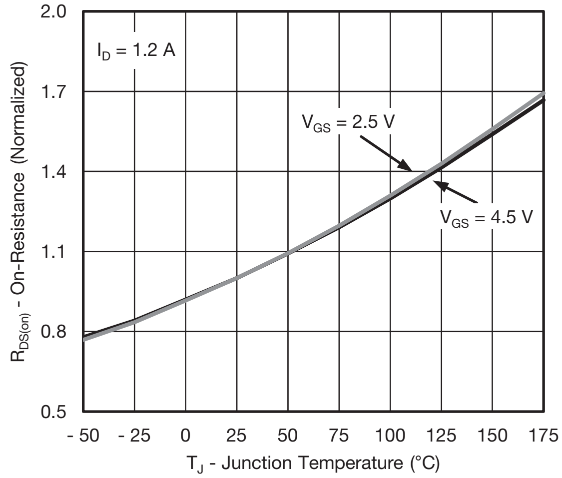


Capacitance

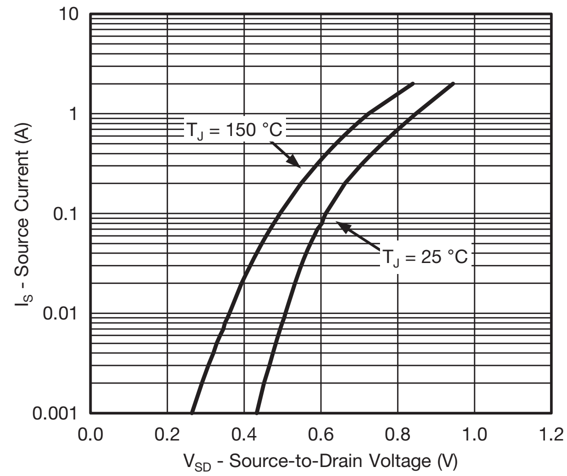


Gate Charge

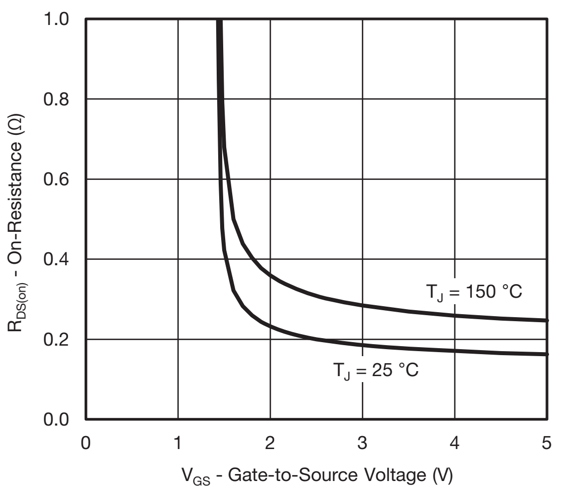
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



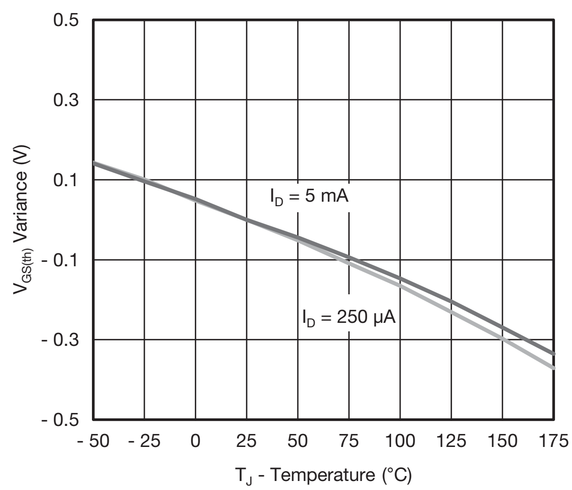
On-Resistance vs. Junction Temperature



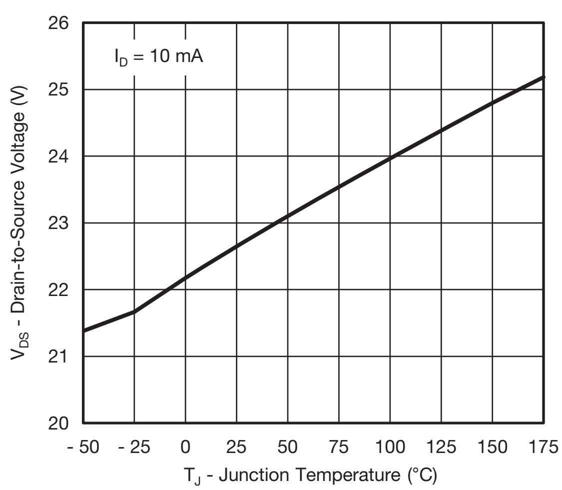
Source Drain Diode Forward Voltage



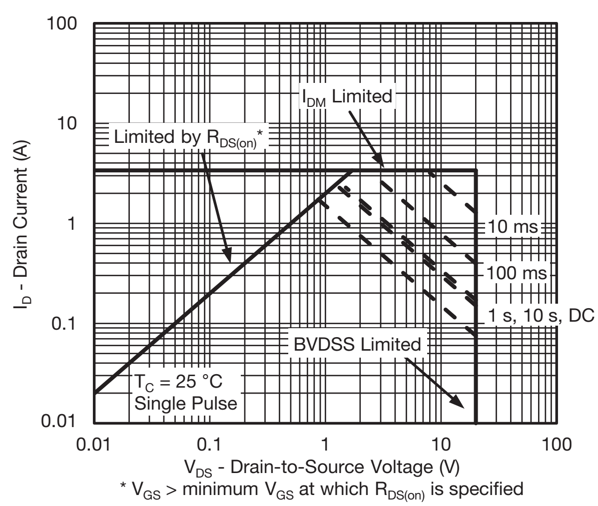
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

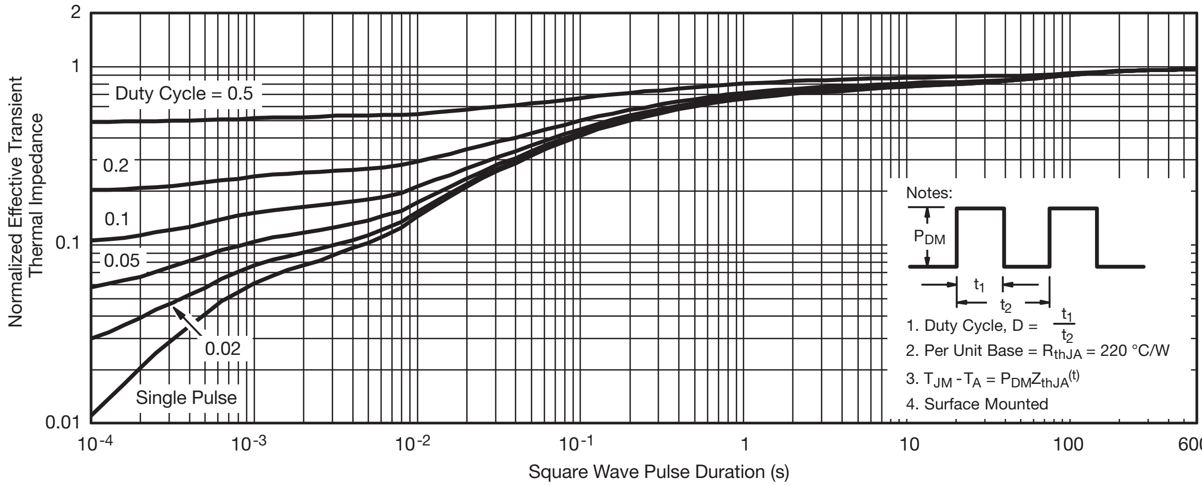


Drain Source Breakdown vs. Junction Temperature

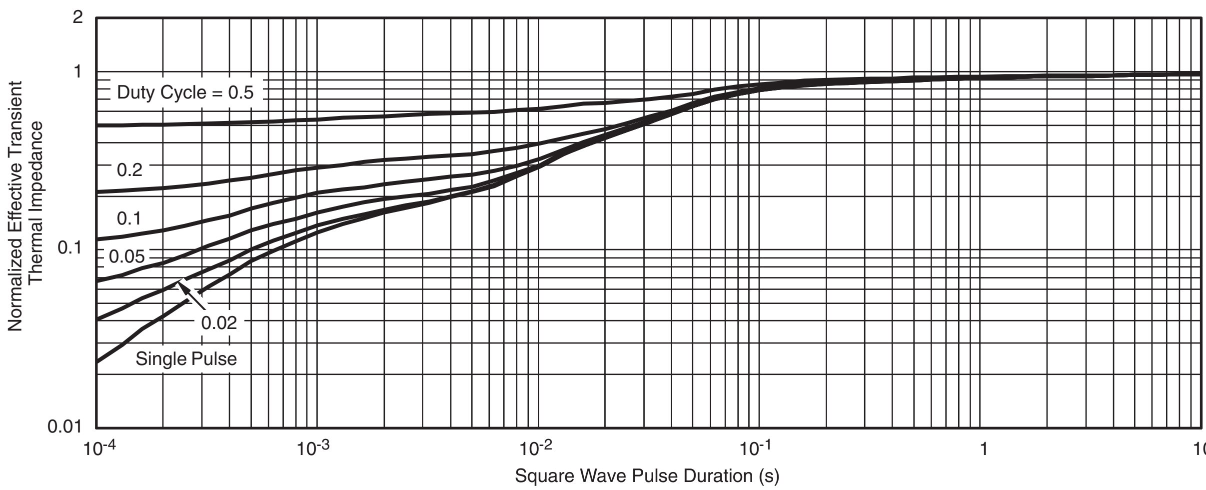


Safe Operating Area

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

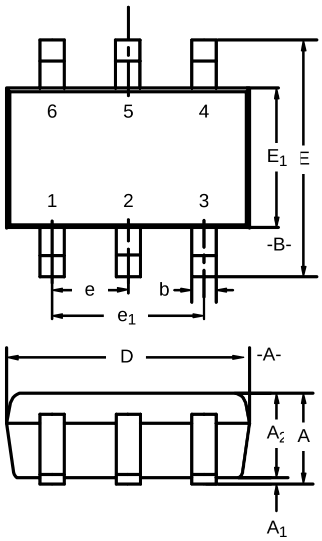
Note

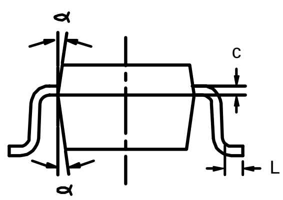
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67394.

SC-70: 6-LEADS

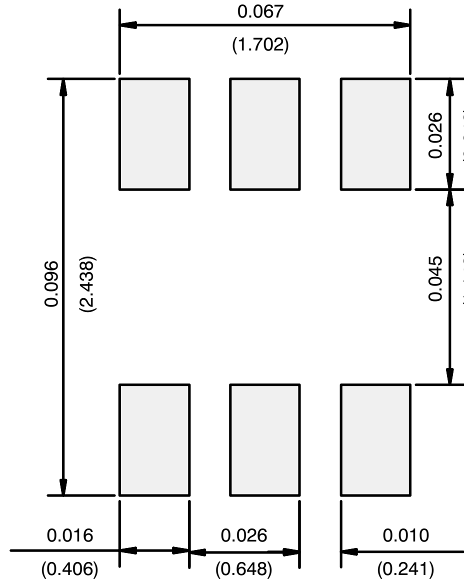




Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

PIN-OUT

Figure 1 shows the pin-out description and pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

SOT-363
SC-70 (6-LEADS)

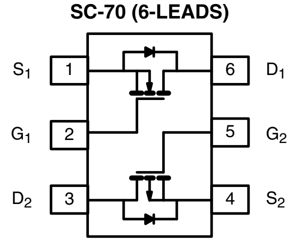


Fig. 1

For package dimensions see outline drawing SC-70 (6-Leads) (www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (www.vishay.com/doc?72286) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (figure 2) yields a reduction in thermal resistance and is a preferred footprint.

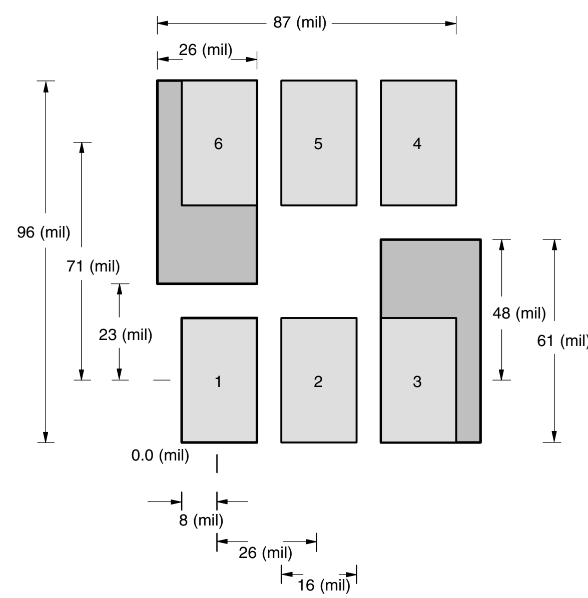


Fig. 2 SC-70 (6 leads) Dual

EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, Basic Pad Patterns. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch^2 PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

Front of Board SC70-6 **Back of Board SC70-6**

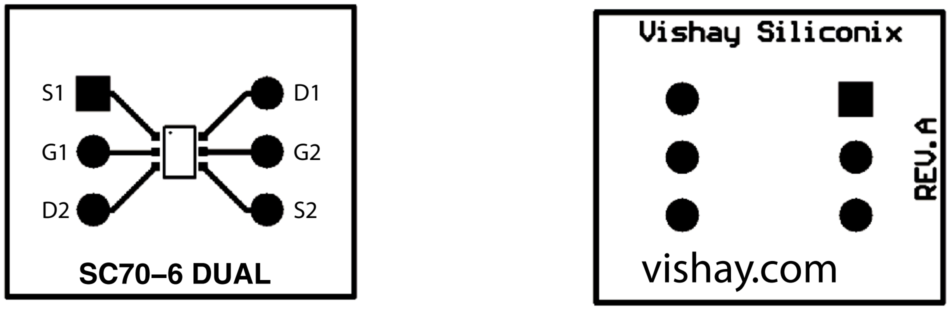


Fig. 3

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the "foot" is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80 °C/W, with a maximum thermal resistance of approximately 100 °C/W. This data compares favorably with another compact, dual-channel package - the dual TSOP-6 - which features a typical thermal resistance of 75 °C/W and a maximum of 90 °C/W.

Power Dissipation for 175 °C Rated Part

The typical RθJA for the dual-channel 6-pin SC-70 with a copper leadframe is 224 °C/W steady-state, compared to 413 °C/W for the Alloy 42 version. All figures are based on the 1-inch^2 FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
ROOM AMBIENT 25 °C	ELEVATED AMBIENT 60 °C
$P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$
$P_D = \frac{175\ °C - 25\ °C}{413\ °C/W}$	$P_D = \frac{175\ °C - 60\ °C}{413\ °C/W}$
$P_D = 363\ mW$	$P_D = 278\ mW$

COOPER LEADFRAME	
ROOM AMBIENT 25 °C	ELEVATED AMBIENT 60 °C
$P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$
$P_D = \frac{175\ °C - 25\ °C}{224\ °C/W}$	$P_D = \frac{175\ °C - 60\ °C}{224\ °C/W}$
$P_D = 669\ mW$	$P_D = 513\ mW$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R\theta_{JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	ALLOY 42	COPPER
1) Minimum recommended pad pattern on the EVB board (see fig. 3).	518 °C/W	344 °C/W
2) Industry standard 1-inch^2 PCB with maximum copper both sides.	413 °C/W	224 °C/W

The results indicate that designers can reduce thermal resistance (θ_{JA}) by 34 % simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174 °C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120 °C/W reduction can be obtained by utilizing a 1-inch^2. PCB area.

Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

The dual copper leadframe versions have the following suffix:

Dual:	Sx19xxEDH or Sx19xxEEH
Compl.:	Sx15xxEDH or Sx15xxEEH

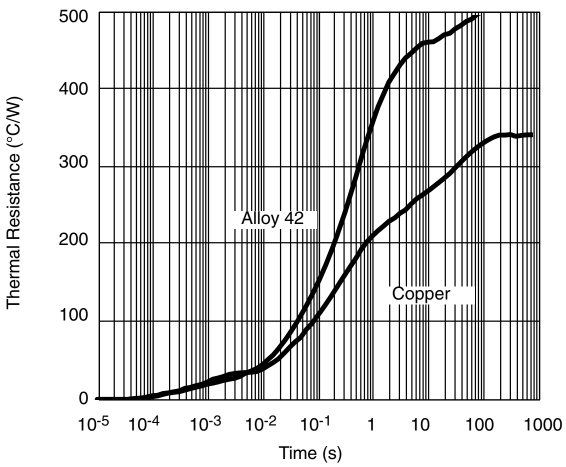


Fig. 4 Dual SC70-6 Thermal Performance on EVB

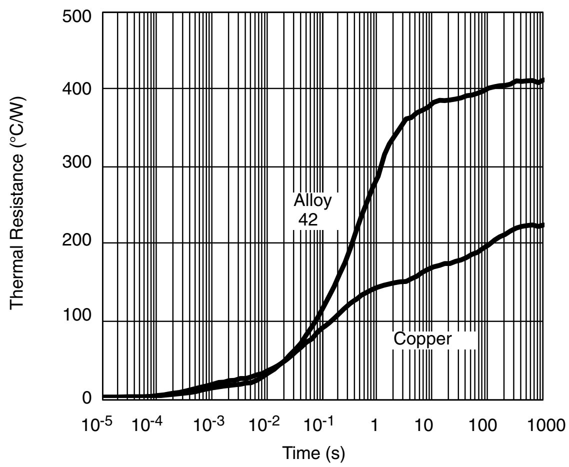


Fig. 5 Dual SC70-6 Comparison on 1-inch^2 PCB

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.