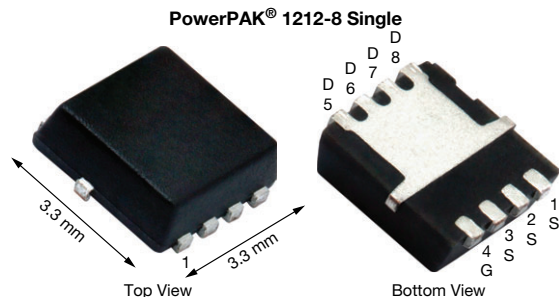


N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0027
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0040
Q_g typ. (nC)	17.5
I_D (A)	40 ^g
Configuration	Single

FEATURES

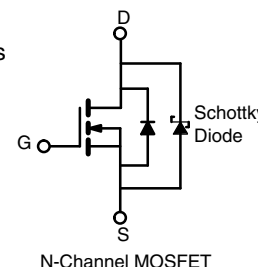
- TrenchFET® Gen IV power MOSFET
- SkyFET® with monolithic Schottky diode
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Personal computers and servers
- Synchronous buck
- Synchronous rectification
- DC/DC conversion



ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSC06DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	+20, -16	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	40 ^g	A
	$T_C = 70$ °C		40 ^g	
	$T_A = 25$ °C		27.6 ^{a, b}	
	$T_A = 70$ °C		25.2 ^{a, b}	
Pulsed drain current ($t = 100$ μ s)		I_{DM}	100	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	40 ^g	
	$T_A = 25$ °C		3.3 ^{a, b}	
Single pulse avalanche current	$L = 0.1$ mH	I_{AS}	15	mJ
Single pulse avalanche energy		E_{AS}	11.25	
Maximum power dissipation	$T_C = 25$ °C	P_D	46.3	W
	$T_C = 70$ °C		29.6	
	$T_A = 25$ °C		3.7 ^{a, b}	
	$T_A = 70$ °C		3.1 ^{a, b}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{c, d}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, e}	$t \leq 10$ s	R_{thJA}	25	33	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2.1	2.7	

Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 81 °C/W
- Based on $T_C = 25$ °C
- Package limited



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Drain-source breakdown voltage (transient) ^c	V _{DSt}	V _{GS} = 0 V, I _{D(aval)} = 15 A, t _{transcient} ≤ 50 ns	36	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.1	
Gate-source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 V, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	0.02	0.20	mA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	0.13	1	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.0022	0.0027	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0032	0.0040	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	120	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	2455	-	pF
Output capacitance	C _{oss}		-	350	-	
Reverse transfer capacitance	C _{rss}		-	60	-	
C _{rss} /C _{iss} ratio			-	0.025	0.050	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	-	38.5	58	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	-	17.5	27	
Q _{gs}	-		6.3	-		
Q _{gd}	-		2.8	-		
Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	-	29	-		
Gate resistance	R _g	f = 1 MHz	0.4	1.15	2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	12	24	ns
Rise time	t _r		-	14	28	
Turn-off delay time	t _{d(off)}		-	23	46	
Fall time	t _f		-	8	16	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	29	58	
Rise time	t _r		-	50	100	
Turn-off delay time	t _{d(off)}		-	20	40	
Fall time	t _f		-	9	18	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	40	A
Pulse diode forward current	I _{SM}		-	-	100	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.47	0.7	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	31	62	ns
Body diode reverse recovery charge	Q _{rr}		-	19	38	nC
Reverse recovery fall time	t _a		-	16	-	ns
Reverse recovery rise time	t _b		-	15	-	

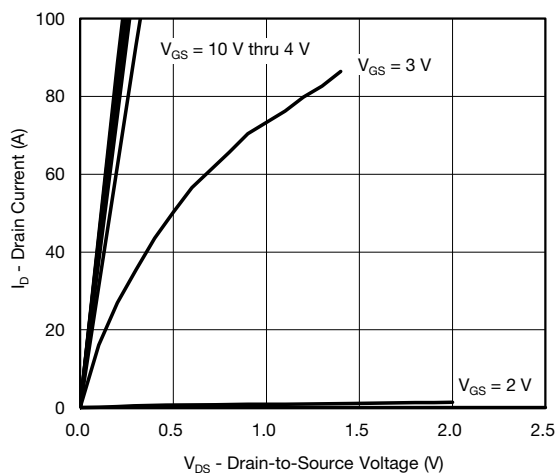
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. T_{CASE} = 25 °C; Expected voltage stress during 100 % UIS test. Production data log is not available

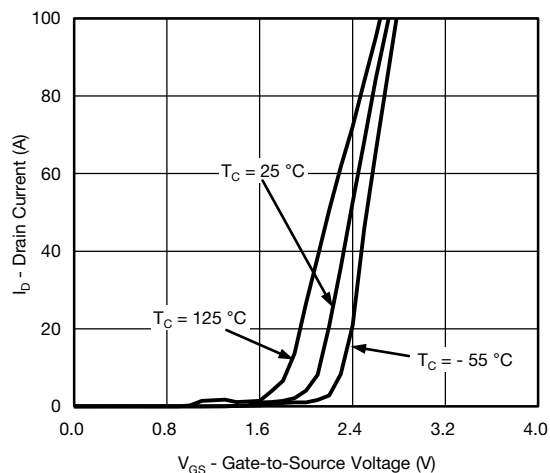
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



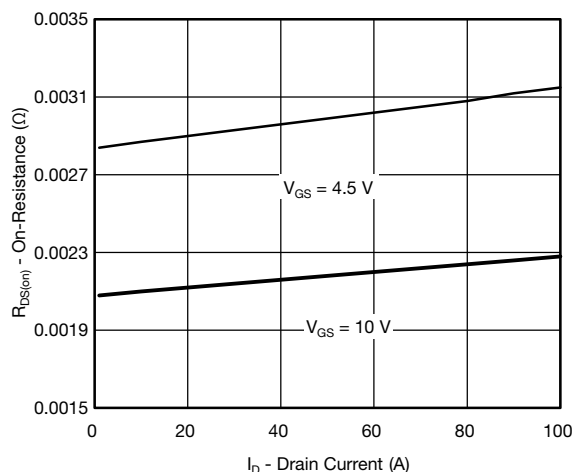
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



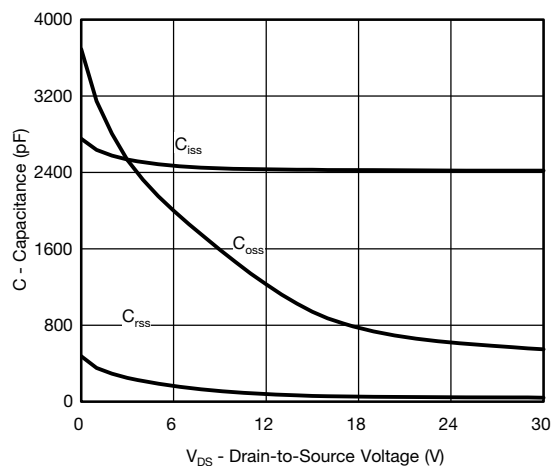
Output Characteristics



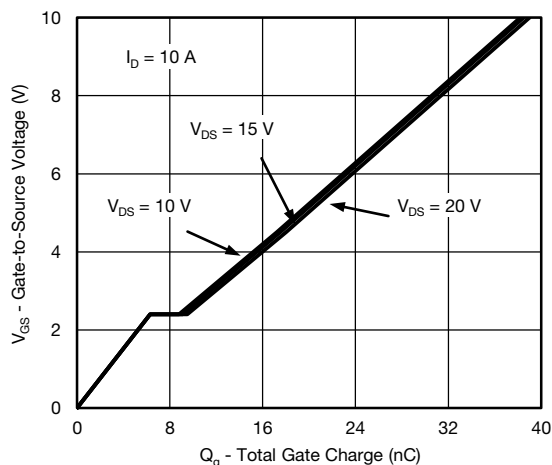
Transfer Characteristics



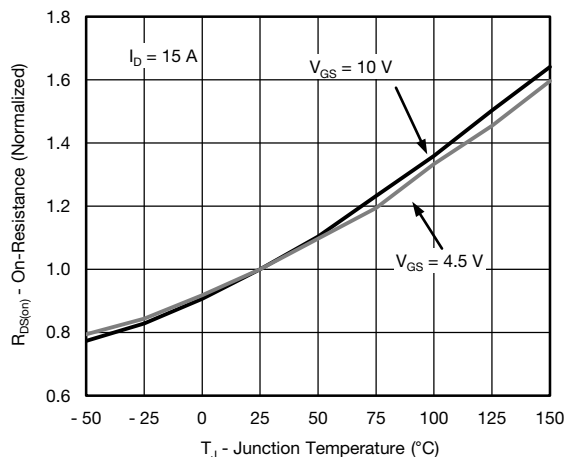
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



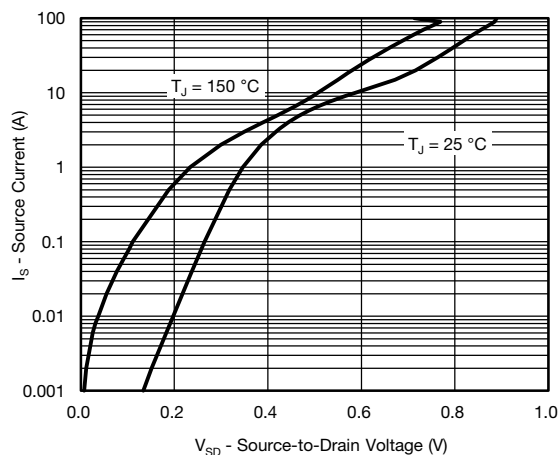
Gate Charge



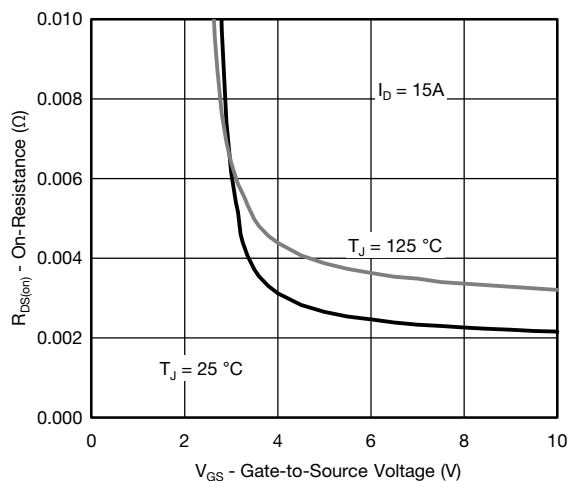
On-Resistance vs. Junction Temperature



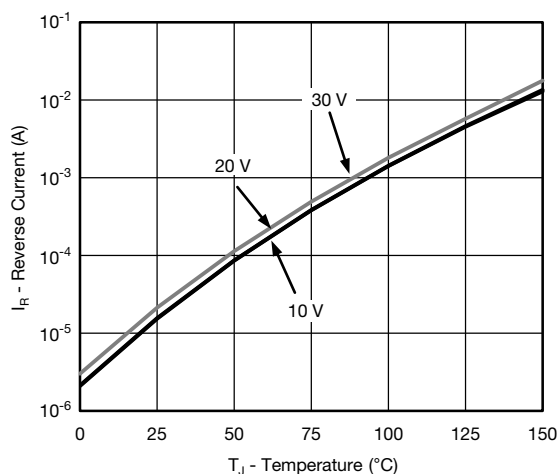
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



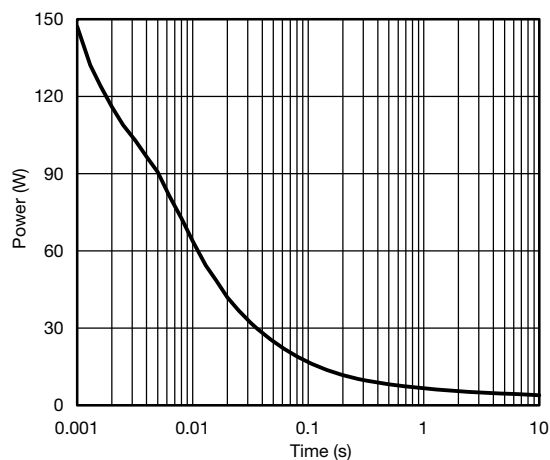
Source-Drain Diode Forward Voltage



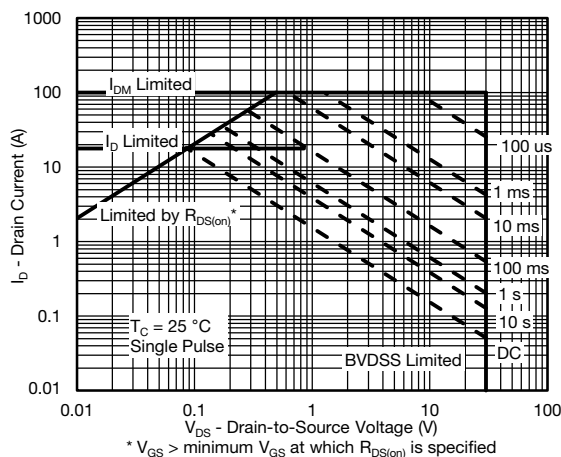
On-Resistance vs. Gate-to-Source Voltage



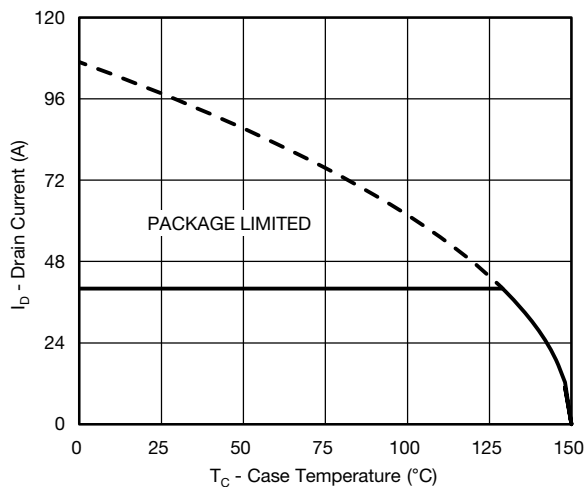
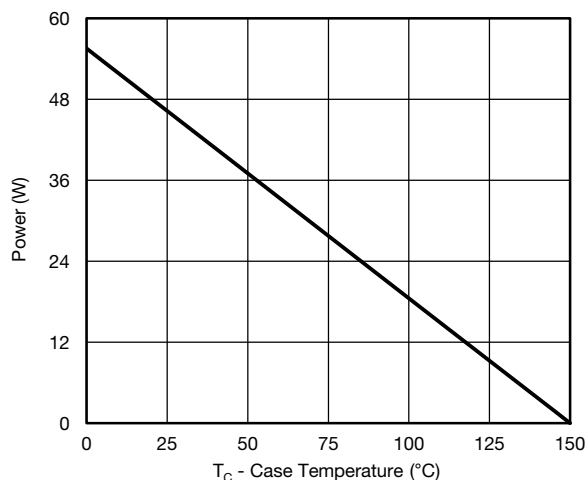
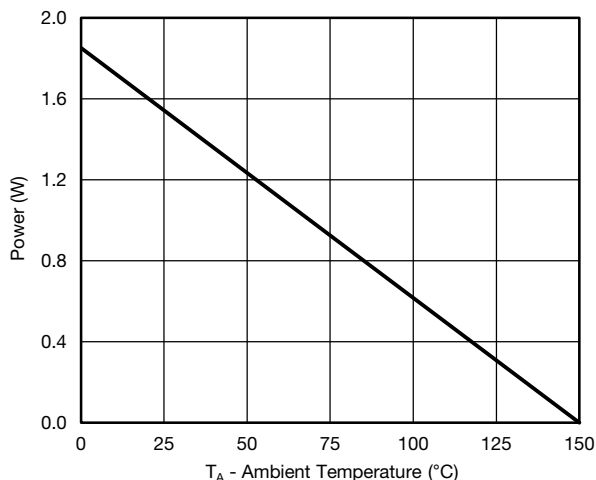
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



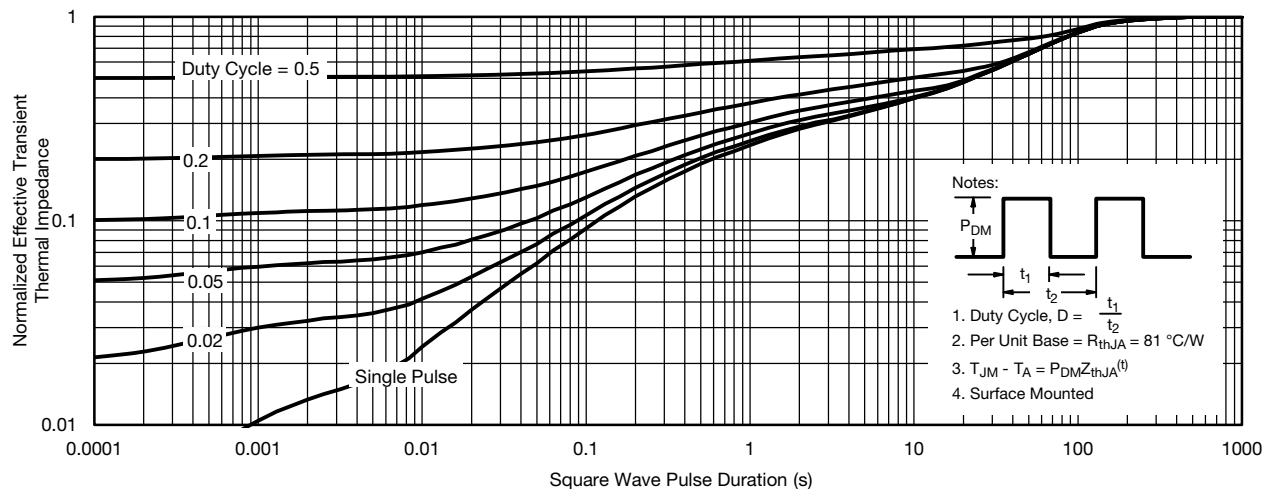
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

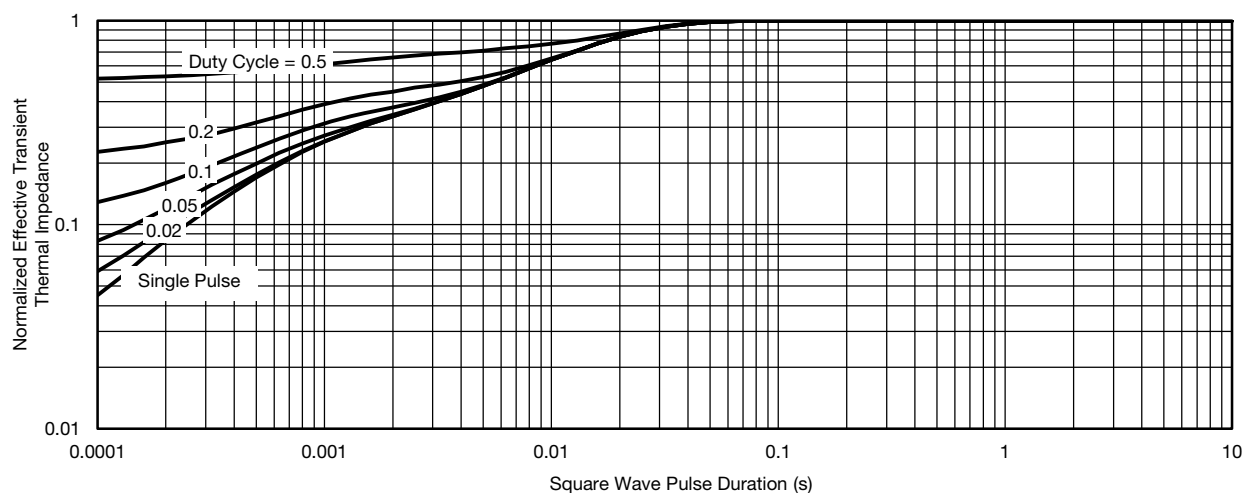
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® 1212-8, (Single / Dual)



Backside view of single pad



Backside view of dual pad

Notes

1. Inch will govern

[2] Dimensions exclusive of mold gate burrs

3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S16-2667-Rev. M, 09-Jan-17						
DWG: 5882						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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