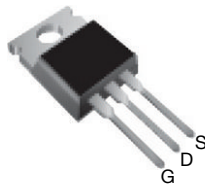


## E Series Power MOSFET

**TO-220AB**


N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Computing
  - PC silver box / ATX power supplies
- Lighting
  - Two stage LED lighting
- Consumer electronics
- Applications using hard switched topologies
  - Power factor correction (PFC)
  - Two switch forward converter
  - Flyback converter
- Switch mode power supplies (SMPS)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	550	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.380
$Q_g$ max. (nC)	50	
$Q_{gs}$ (nC)	6	
$Q_{gd}$ (nC)	10	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP12N50E-BE3 <sup>a</sup>
	SiHP12N50E-GE3

#### Note

a. "-BE3" denotes alternate manufacturing location

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	21	
Linear derating factor		0.91	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	103	mJ
Maximum power dissipation	$P_D$	114	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dV/dt$	70	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		27	
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	300	°C


#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature  
 b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.7$  A  
 c. 1.6 mm from case  
 d.  $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

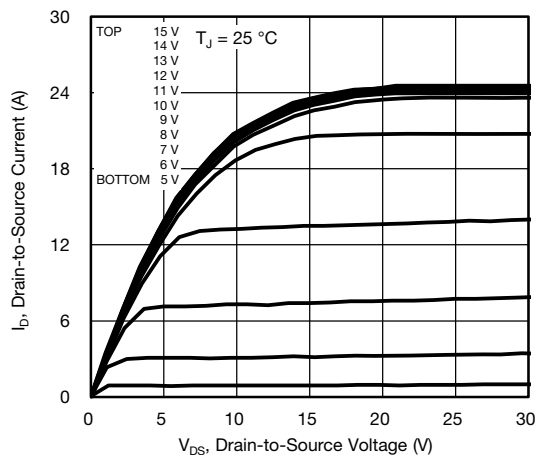
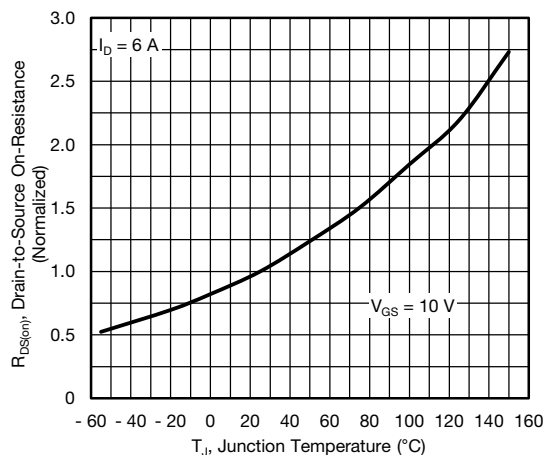
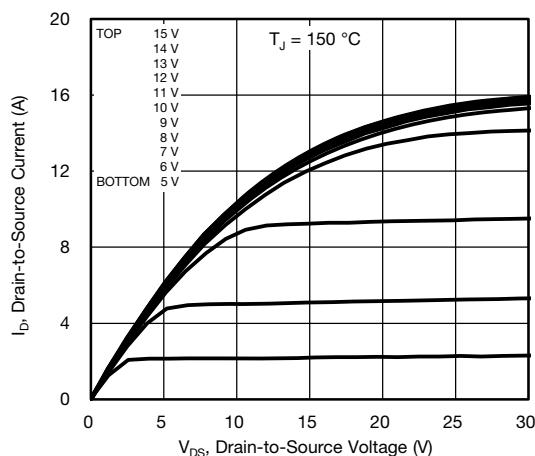
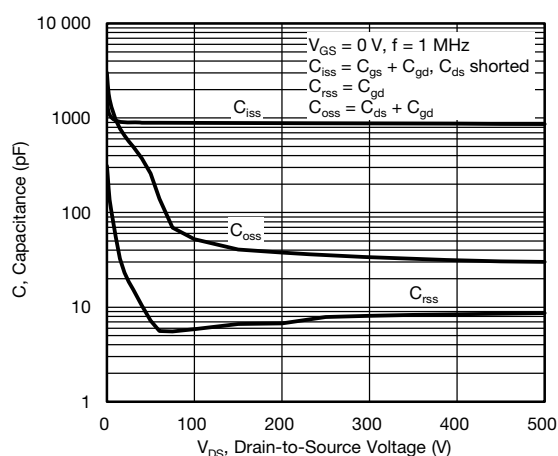
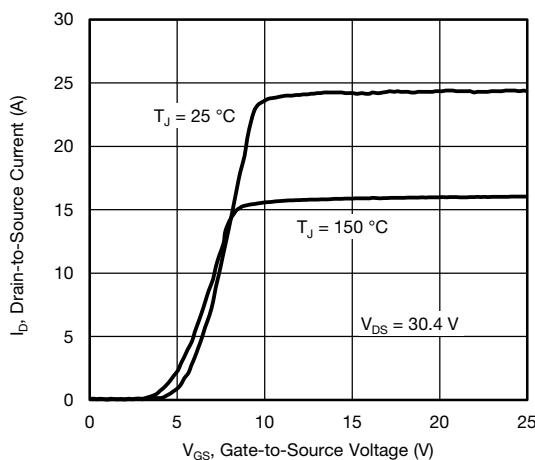
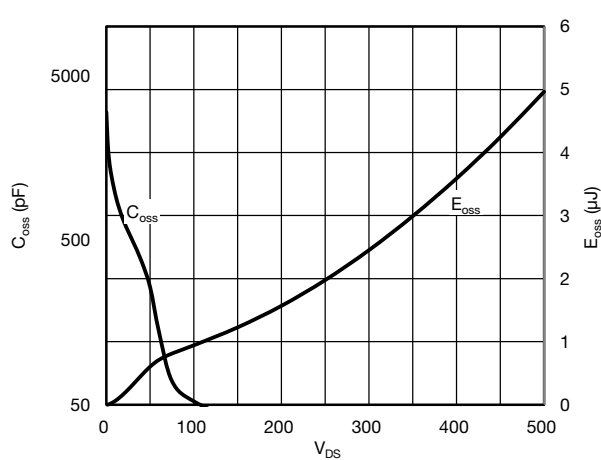
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	1.1	

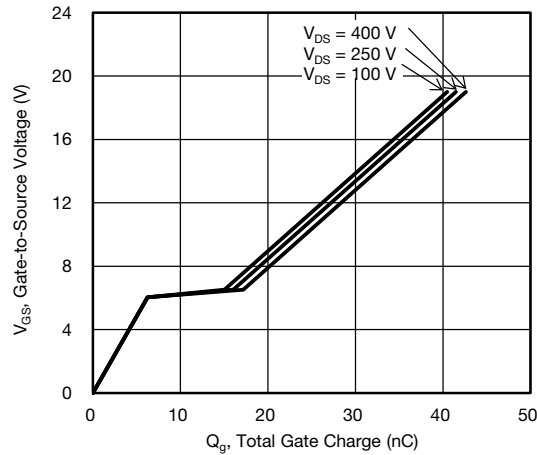
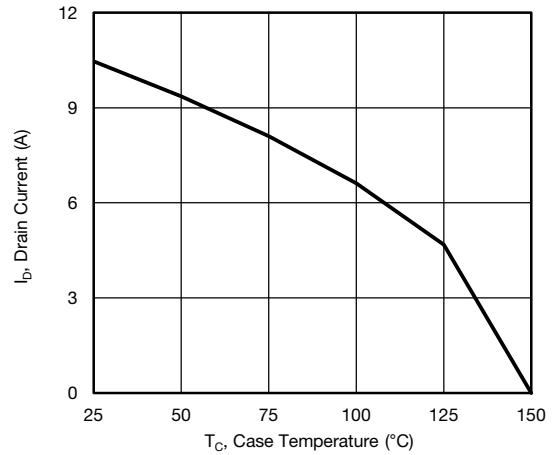
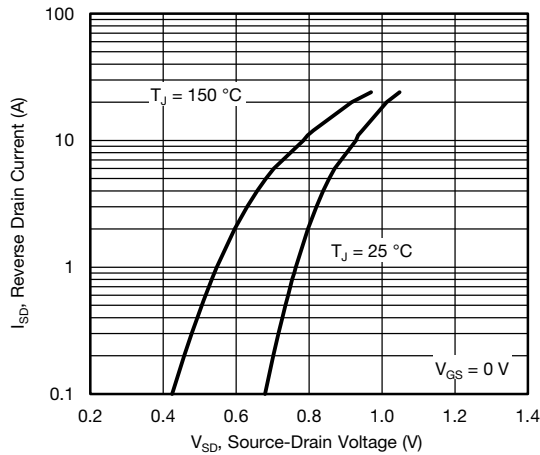
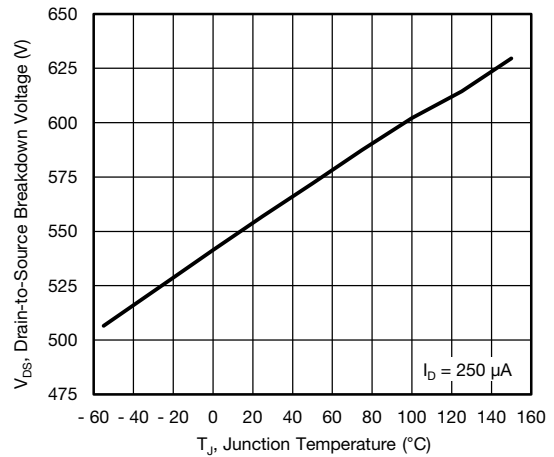
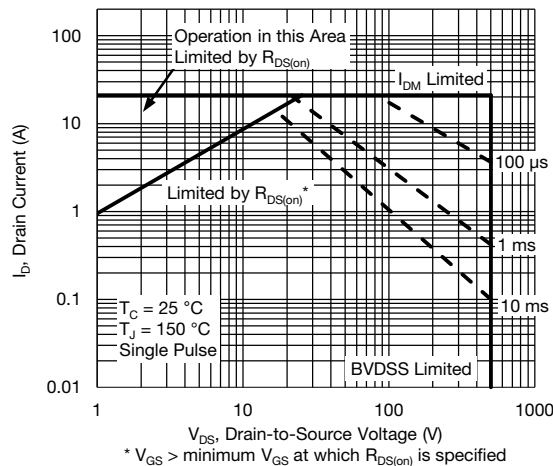
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

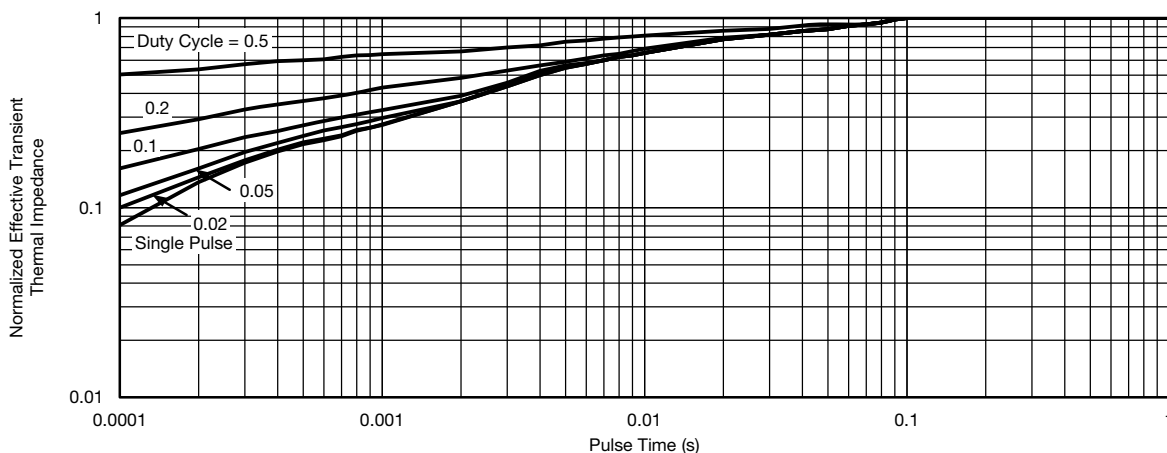
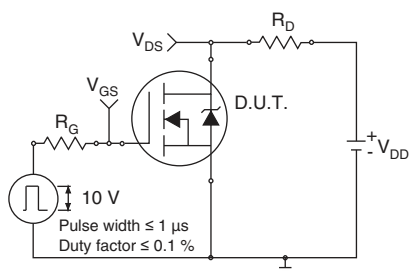
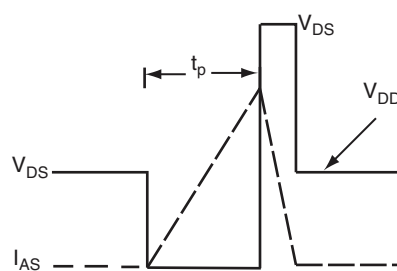
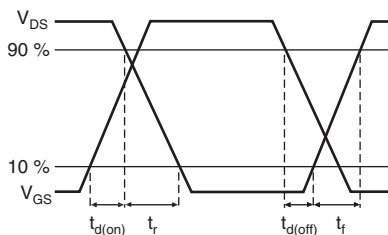
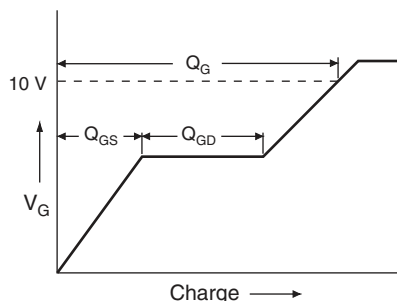
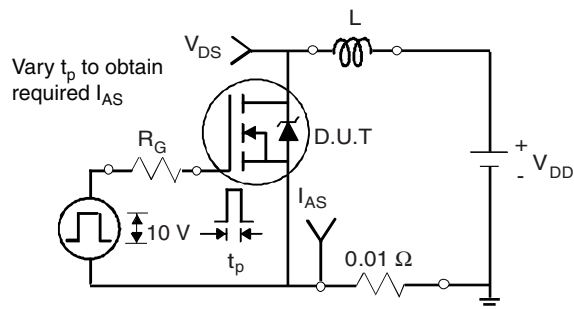
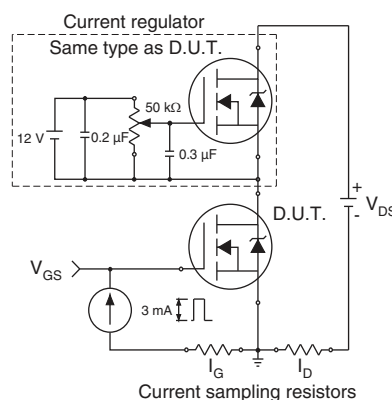
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.60	-	V/°C
Gate-source threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A	-	0.330	0.380	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 6 A		-	3.1	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	886	-	pF
Output capacitance	C <sub>oss</sub>			-	52	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	6	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	45	-	pF
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	131	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A, V <sub>DS</sub> = 400 V	-	25	50	nC
Gate-source charge	Q <sub>gs</sub>			-	6	-	
Gate-drain charge	Q <sub>gd</sub>			-	10	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 6 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	13	26	ns
Rise time	t <sub>r</sub>			-	16	32	
Turn-off delay time	t <sub>d(off)</sub>			-	29	58	
Fall time	t <sub>f</sub>			-	12	24	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.92	-	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10.5	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	21	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 7.5 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 6 A, dI/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	244	-	ns
Reverse recovery charge	Q <sub>rr</sub>			-	2.5	-	μC
Reverse recovery current	I <sub>RRM</sub>			-	19	-	A

**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 10 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

**Fig. 9 - Maximum Safe Operating Area**


**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

**Fig. 13 - Switching Time Test Circuit**

**Fig. 16 - Unclamped Inductive Waveforms**

**Fig. 14 - Switching Time Waveforms**

**Fig. 17 - Basic Gate Charge Waveform**

**Fig. 15 - Unclamped Inductive Test Circuit**

**Fig. 18 - Gate Charge Test Circuit**


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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