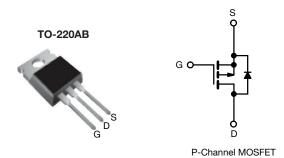


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	-10	-100		
$R_{DS(on)}(\Omega)$	V _{GS} = -10 V	0.60		
Q _g max. (nC)	1	8		
Q _{gs} (nC)	3.	3.0		
Q _{gd} (nC)	9.0			
Configuration	Single			

FEATURES

- Dynamic dv/dt rating
- · Repetitive avalanche rated
- P-channel
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF9520PbF
Lead (Pb)-free and halogen-free	IRF9520PbF-BE3

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	-100	V	
Gate-source voltage			V _{GS}	± 20		
Continuous drain current	V _{GS} at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1	-6.8	А	
		T _C = 100 °C	I _D	-4.8		
Pulsed drain current ^a			I _{DM}	-27	1	
Linear derating factor				0.40	W/°C	
Single pulse avalanche energy b			E _{AS}	300	mJ	
Repetitive avalanche current a			I _{AR}	-6.8	Α	
Repetitive avalanche energy ^a			E _{AR}	6.0	mJ	
Maximum power dissipation	T _C = 25 °C		P _D	60	W	
Peak diode recovery dV/dt ^c			dv/dt	-5.5	V/ns	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +175	- °C	
Soldering recommendations (peak temperature) ^d) d For 10 s		300			
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = -25 V, starting T_J = 25 °C, L = 9.7 mH, R_q = 25 Ω , I_{AS} = -6.8 A (see fig. 12)
- c. $I_{SD} \le -6.8 \text{ A}$, $di/dt \le 110 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \text{ °C}$
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	2.5		

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = -1 mA		-	-0.10	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = \	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$		-	-4.0	V
Gate-source leakage	I _{GSS}	V	V _{GS} = ± 20 V		-	± 100	nA
7	,	V _{DS} = -100 V, V _{GS} = 0 V		-	-	-100	μА
Zero gate voltage drain current	I _{DSS}	$V_{DS} = -80 \text{ V},$	V _{DS} = -80 V, V _{GS} = 0 V, T _J = 150 °C		-	-500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -4.1 A ^b	-	-	0.60	Ω
Forward transconductance	9 _{fs}	V _{DS} = -5	50 V, I _D = -4.1 A ^b	2.0	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = -25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. 5}$		-	390	-	pF
Output capacitance	C _{oss}			-	170	-	
Reverse transfer capacitance	C _{rss}			-	45	-	
Total gate charge	Qg	V _{GS} = -10 V	I _D = -6.8 A, V _{DS} = -80 V, see fig. 6 and 13 ^b	-	-	18	nC
Gate-source charge	Q _{gs}			-	-	3.0	
Gate-drain charge	Q_{gd}			-	-	9.0	
Turn-on delay time	t _{d(on)}			-	9.6	-	
Rise time	t _r	V_{DD} = -50 V, I_D = -6.8 A, R_g = 18 Ω , R_D = 7.1 Ω , see fig. 10 ^b		-	29	-	ns
Turn-off delay time	t _{d(off)}			-	21	-	
Fall time	t _f			=	25	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.8	-	3.9	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		ı	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	''''
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-6.8	
Pulsed diode forward current ^a	I _{SM}			-	-	-27	A
Body diode voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = -6.8 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	-6.3	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = -6.8 A, dl/dt = 100 A/μs b		-	98	200	ns
Body diode reverse recovery charge	Q _{rr}			-	0.33	0.66	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and				L _D)	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

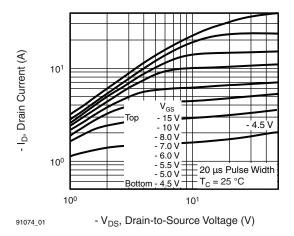


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

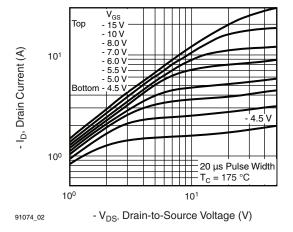


Fig. 2 - Typical Output Characteristics, $T_C = 175$ °C

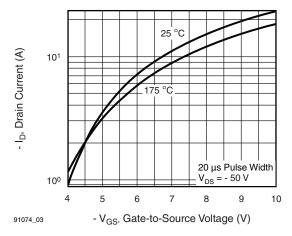


Fig. 3 - Typical Transfer Characteristics

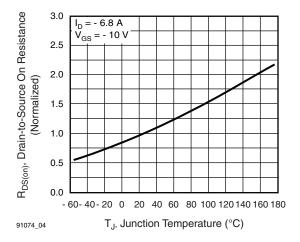


Fig. 4 - Normalized On-Resistance vs. Temperature

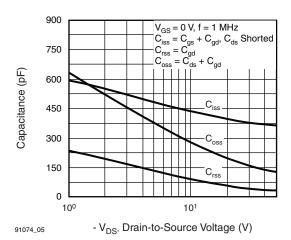


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

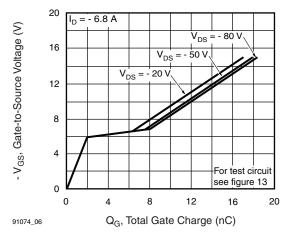


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



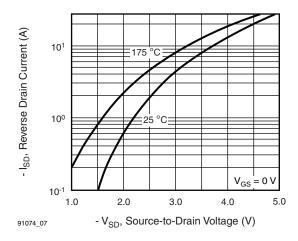


Fig. 7 - Typical Source-Drain Diode Forward Voltage

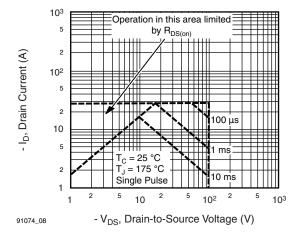


Fig. 8 - Maximum Safe Operating Area

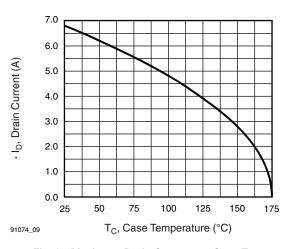


Fig. 9 - Maximum Drain Current vs. Case Temperature

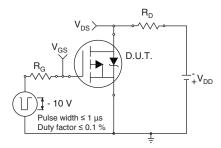


Fig. 10a - Switching Time Test Circuit

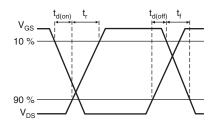


Fig. 10b - Switching Time Waveforms

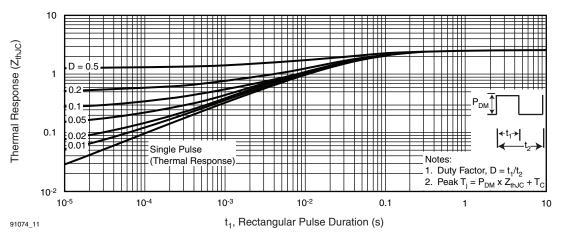


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



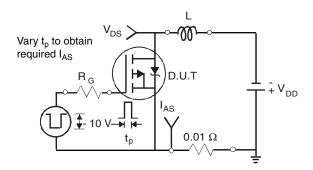


Fig. 12a - Unclamped Inductive Test Circuit

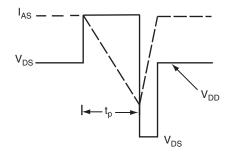


Fig. 12b - Unclamped Inductive Waveforms

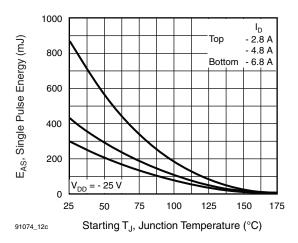


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

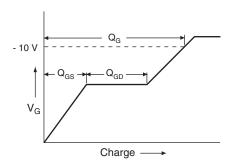


Fig. 13a - Basic Gate Charge Waveform

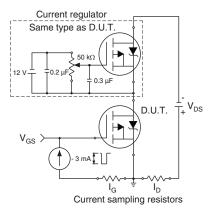
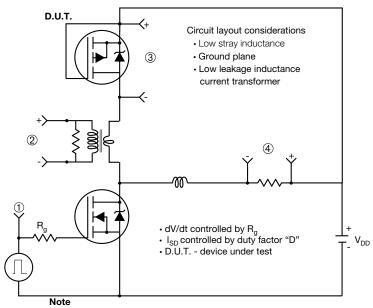


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver

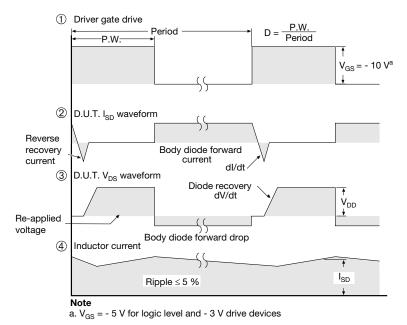


Fig. 14 - For P-Channel

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