www.vishay.com

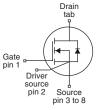
Vishay Siliconix

HALOGEN

FREE

# **EF Series Power MOSFET With Fast Body Diode**





N-Channel MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V) at T <sub>J</sub> max.	65	50		
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	V <sub>GS</sub> = 10 V	0.050		
Q <sub>g</sub> max. (nC)	9	0		
Q <sub>gs</sub> (nC)	26			
Q <sub>gd</sub> (nC)	1	4		
Configuration	Sin	Single		

#### **FEATURES**

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

#### **APPLICATIONS**

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK 10 x 12
Lead (Pb)-free and halogen-free	SiHK055N60EF-T1GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	600	V	
Gate-source voltage			$V_{GS}$	± 30	V	
Continuous drain current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$		40	A	
	VGS at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	26		
Pulsed drain current <sup>a</sup>			$I_{DM}$	110		
Linear derating factor				1.89	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	226	mJ	
Maximum power dissipation			$P_{D}$	236	W	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-source voltage slope $T_J = 125 ^{\circ}\text{C}$		T <sub>J</sub> = 125 °C	dv/dt	100	V/ns	
Reverse diode dv/dt <sup>d</sup>			dv/dt	50	V/115	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b.  $V_{DD}$  = 120 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 4.0 A
- c. 1.6 mm from case
- d.  $I_{SD} \le I_D$ , di/dt = 100 A/ $\mu$ s, starting  $T_J$  = 25 °C



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	50 <sup>c</sup>	°C/W	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	0.53	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	600	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	Reference to 25 °C, I <sub>D</sub> = 1 mA		0.55	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		-	5.0	V
Out and the land	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Gate-source leakage		,	$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
<del>-</del>		V <sub>DS</sub> =	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V		-	1	μΑ
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V	, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	2	mA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 16 A	-	0.050	0.058	Ω
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 16 A		22	-	S
Dynamic					•		
Input capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ $f = 1 \text{ MHz}$		-	3667	-	pF
Output capacitance	C <sub>oss</sub>			-	143	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	5	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		-	146	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			-	749	-	
Total gate charge	Qg			-	60	90	
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 16 \text{ A}, V_{DS} = 480 \text{ V}$		26	-	nC
Gate-drain charge	Q <sub>gd</sub>			-	14	-	]
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 16 A,		-	35	70	- ns
Rise time	t <sub>r</sub>			-	40	80	
Turn-off delay time	t <sub>d(off)</sub>	V <sub>GS</sub> =	$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$		56	84	
Fall time	t <sub>f</sub>			-	29	58	
Gate input resistance	$R_g$	f = 1 MHz		0.3	0.7	1.4	Ω
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous source-drain diode current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	40	
Pulsed diode forward current	I <sub>SM</sub>			-	-	110	Α
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 16 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S = 16 \text{ A},$ $di/dt = 100 \text{ A/µs}, V_R = 400 \text{ V}$		-	126	252	ns
Reverse recovery charge	Q <sub>rr</sub>			-	0.8	1.6	μC
Reverse recovery current	I <sub>RRM</sub>			_	14	_	Α

#### Notes

- e.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 400 V
- f.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to 400 V
- g. When mounted on 1" x 1" FR4 board



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

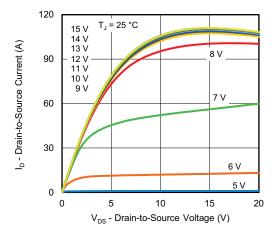


Fig. 1 - Typical Output Characteristics

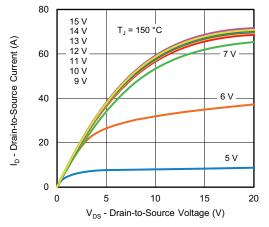


Fig. 2 - Typical Output Characteristics

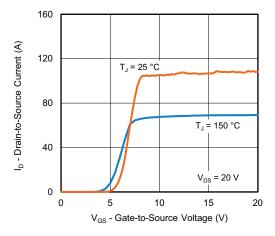


Fig. 3 - Typical Transfer Characteristics

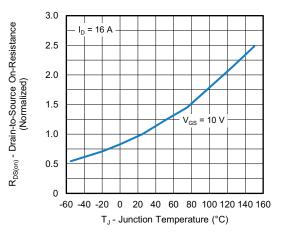


Fig. 4 - Normalized On-Resistance vs. Temperature

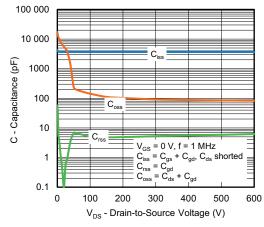


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

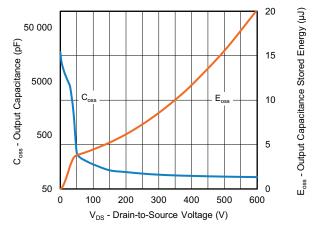


Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$ 



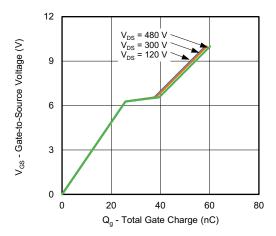


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

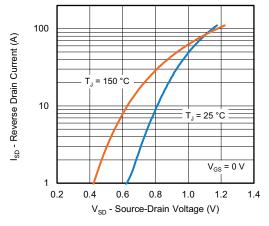


Fig. 8 - Typical Source-Drain Diode Forward Voltage

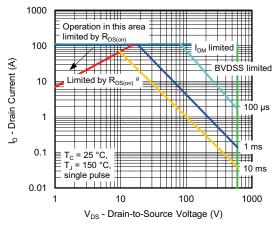


Fig. 9 - Maximum Safe Operating Area

#### Note

h.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

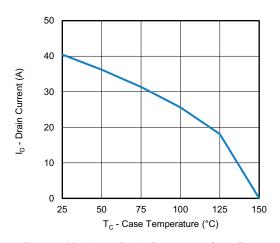


Fig. 10 - Maximum Drain Current vs. Case Temperature

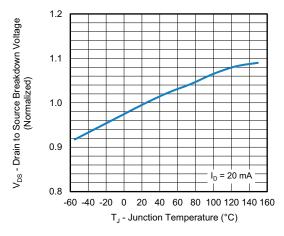


Fig. 11 - Temperature vs. Drain-to-Source Voltage



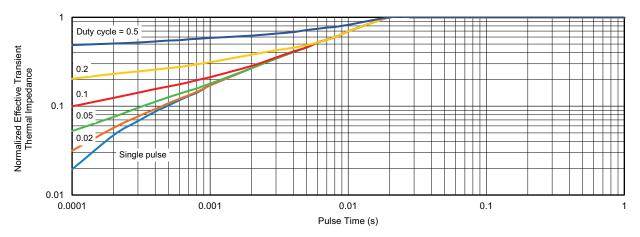


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

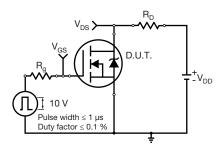


Fig. 13 - Switching Time Test Circuit

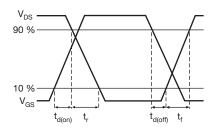


Fig. 14 - Switching Time Waveforms

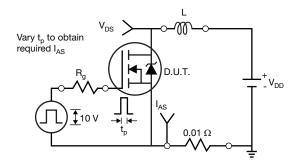


Fig. 15 - Unclamped Inductive Test Circuit

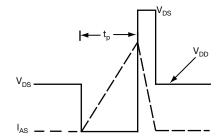


Fig. 16 - Unclamped Inductive Waveforms

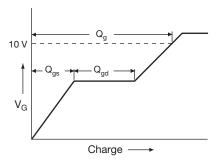


Fig. 17 - Basic Gate Charge Waveform

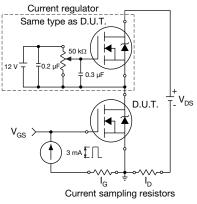
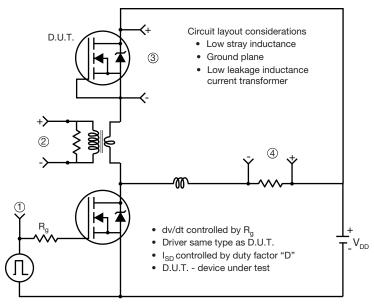


Fig. 18 - Gate Charge Test Circuit



#### Peak Diode Recovery dv/dt Test Circuit



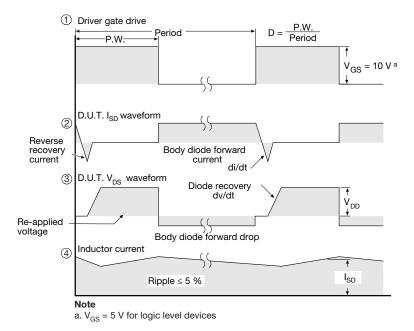
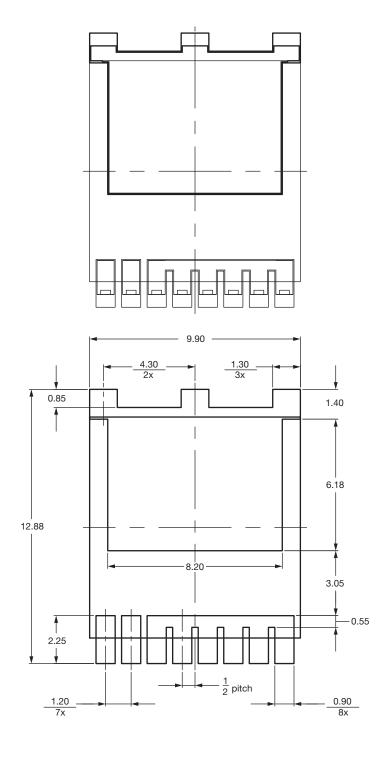


Fig. 19 - For N-Channel

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# Recommended Land Pattern PowerPAK® 10 x 12 (TOLL) (High Voltage)



#### Note

• Dimensions in mm

ECN: S22-1061-Rev. C, 26-Dec-2022

DWG: 3013



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