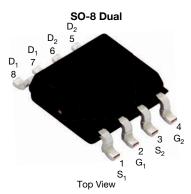
Vishay Siliconix

# **Dual N-Channel 20 V (D-S) MOSFET**



PRODUCT SUMMARY					
V <sub>DS</sub> (V)	20				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.018				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	0.022				
Q <sub>g</sub> typ. (nC)	10				
I <sub>D</sub> (A) <sup>a</sup>	8				
Configuration	Dual				

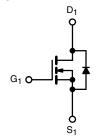
#### **FEATURES**

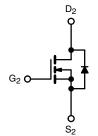
- TrenchFET® power MOSFET
- 100 % UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



#### **APPLICATIONS**

- DC/DC converter
  - Game machine
  - PC





N-Channel MOSFET

N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free	Si9926CDY-T1-E3			
Lead (Pb)-free and halogen-free	Si9926CDY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	20	V
Gate-source voltage		V <sub>GS</sub>	± 12	
	T <sub>C</sub> = 25 °C		8 a	
Continuous dunin suurent (T. 150 °C)	T <sub>C</sub> = 70 °C		8 <sup>a</sup>	
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	8 a, b, c	
	T <sub>A</sub> = 70 °C		6.7 b, c	^
Pulsed drain current		I <sub>DM</sub>	30	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		2.6	
	T <sub>A</sub> = 25 °C	l <sub>s</sub>	1.7 <sup>b, c</sup>	
Single pulse avalanche current	1 01 mll	I <sub>AS</sub>	5	
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	1.25	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		3.1	
	T <sub>C</sub> = 70 °C		2	14/
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2 b, c	W
	T <sub>A</sub> = 70 °C		1.3 b, c	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stq</sub>	-55 to +150	°C

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum junction-to-ambient a, c, d	t ≤ 10 s	$R_{thJA}$	50	62.5	°C/W		
Maximum junction-to-foot (drain)	Steady state	R <sub>thJF</sub>	32	40	]		

#### Notes

- a. Package limited, T<sub>C</sub> = 25 °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. Maximum under steady state conditions is 110 °C/W

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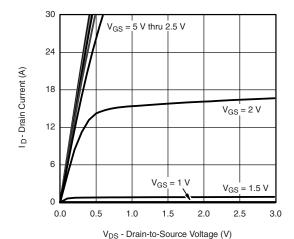
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	25	-	mV/°C	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4	-		
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.6	-	1.5	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	± 100	nA	
Zoro goto voltago droin ourrent		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μА	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C	-	-	10		
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30	-	-	Α	
Drain actives on state registeres 3	В	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8.3 A	-	0.015	0.018		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.5 A	-	0.017	0.022	Ω	
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 8.3 \text{ A}$	-	45	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	1200	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	220	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	100	-		
Total gate charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8.3 \text{ A}$	-	22	33	nC	
			-	10	15		
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 8.3 \text{ A}$	-	2.5	-		
Gate-drain charge	$Q_{gd}$		-	1.7	-		
Gate resistance	$R_{g}$	f = 1 MHz	-	2.4	-	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	15	25		
Rise time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1.5 $\Omega$	-	10	15	1	
Turn-off delay time	t <sub>d(off)</sub>	$I_D\cong 6.7$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$	-	35	55	1	
Fall time	t <sub>f</sub>		-	12	20	1	
Turn-on delay time	t <sub>d(on)</sub>		-	10	15	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 1.5 \Omega$	-	12	20		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 6.7 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	25	40		
Fall time	t <sub>f</sub>		-	10	15	1	
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	2.6		
Pulse diode forward current	I <sub>SM</sub>		-	-	30	A	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 6.7 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	20	40	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 6.7 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	_	10	20	nC	
Reverse recovery fall time	ta	$T_{\rm J} = 25  ^{\circ}{\rm C}$	_	10	-		
Reverse recovery rise time	t <sub>b</sub>		_	10	_	ns	

#### Notes

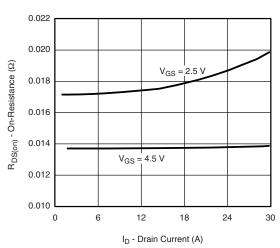
- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

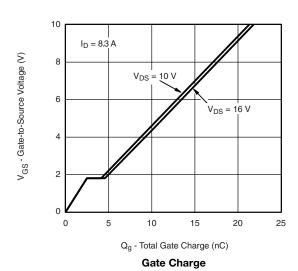


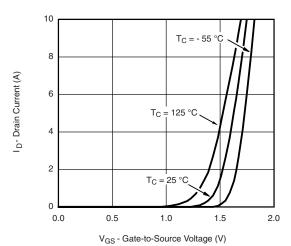


**Output Characteristics** 

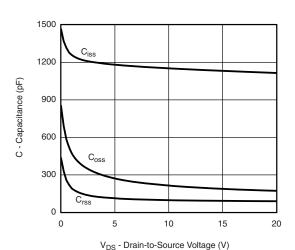


On-Resistance vs. Drain Current

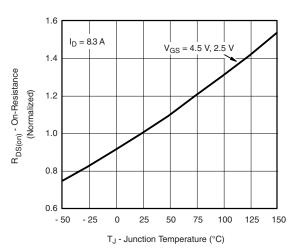




**Transfer Characteristics** 

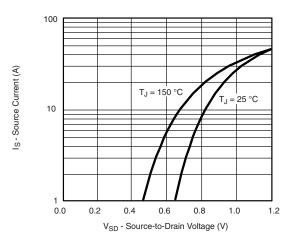


Capacitance

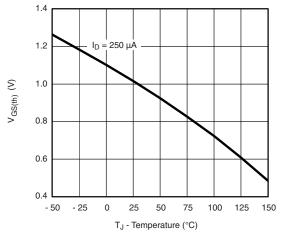


On-Resistance vs. Junction Temperature

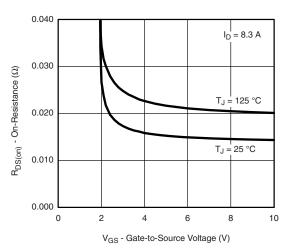




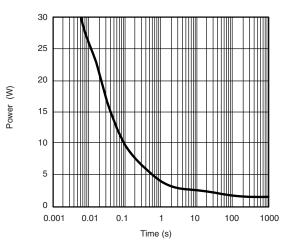
#### Source-Drain Diode Forward Voltage



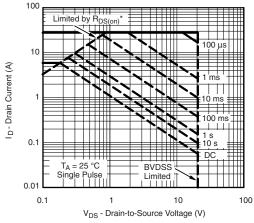
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



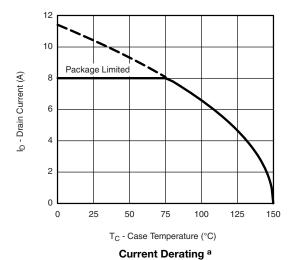
Single Pulse Power

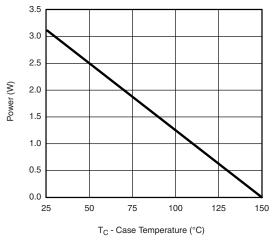


 $^{\star}$  V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

Safe Operating Area, Junction-to-Ambient





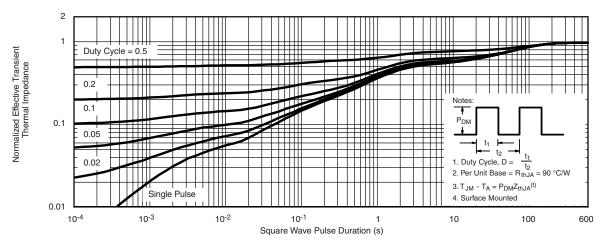


**Power Derating** 

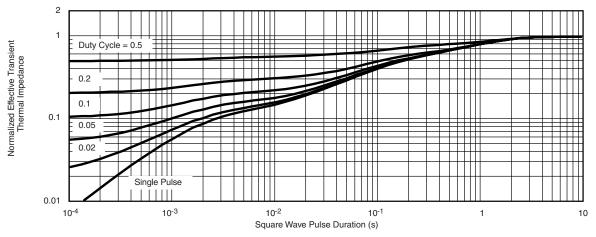
#### Notes

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

# LON NOTE



## **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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