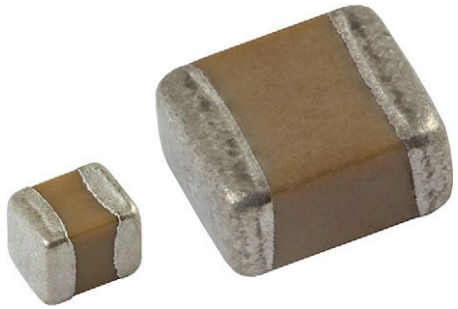
Surface Mount Multilayer Ceramic Capacitors



FEATURES

- Case size 0505 and 1111
- High volumetric energy efficiency
- Low equivalent series resistance
- Lead (Pb)-free terminations code “X”
- Tin / lead termination code “L”
- Reliable noble metal electrode (NME) system
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

RoHS* Available

HALOGEN FREE GREEN (5-2008) Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Bypass coupling decoupling
- DC blocking
- Switching power supplies

ELECTRICAL SPECIFICATIONS

Note

- Electrical characteristics at 25 °C unless otherwise specified

Operating Temperature: -55 °C to +125 °C

Capacitance Range:

0505: 510 pF to 10 nF

1111: 5 nF to 100 nF

Voltage Rating: 50 V_{DC}

Temperature Coefficient of Capacitance (TCC):

BX: ± 15 % from -55 °C to +125 °C, with 0 V_{DC} applied

BX: ± 15 %, -25 % from -55 °C to +125 °C, with 100 % rated V_{DC} applied

Dissipation Factor (DF):

2.50 % maximum at 1 V_{RMS}, 1 kHz

Aging Rate: 1 % maximum per decade

Insulation Resistance (IR):

at +25 °C and rated voltage 100 000 MΩ minimum or 1000 ΩF, whichever is less

at +125 °C and rated voltage 10 000 MΩ minimum or 100 ΩF, whichever is less

Dielectric Strength Test:

performed per method 103 of EIA-198-2-E.

Applied test voltages: min. 250 % of DC rated voltage

QUICK REFERENCE DATA

DIELECTRIC	CASE	MAXIMUM VOLTAGE (V)	CAPACITANCE	
			MINIMUM	MAXIMUM
X = BX	0505	50	510 pF	10 nF
	1111	50	5.0 nF	100 nF

ORDERING INFORMATION

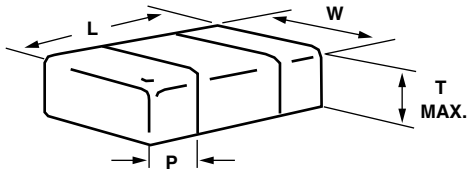
VJ0505	X	102	K	X	A	A	T
CASE CODE	DIELECTRIC	CAPACITANCE NOMINAL CODE	CAPACITANCE TOLERANCE	TERMINATION	DC VOLTAGE RATING (1)	MARKING	PACKAGING
0505 1111	X = BX	Expressed in picofarads (pF). The first two digits are significant, the third is a multiplier. An “R” indicates a decimal point. Examples: 102 = 1000 pF	J = ± 5 % K = ± 10 % M = ± 20 %	X = Ni barrier 100 % tin plate matte finish L = Ni barrier with tin lead plated finish min. 4 % lead	A = 50 V	A = unmarked Q = marked (2)	T = 7" reel / plastic tape J = 7" reel (low quantity) R = 11 1/4" / 13" reel / plastic tape

Notes

(1) DC voltage rating should not be exceeded in application

(2) For case size 1111 only

DIMENSIONS in inches (millimeters)



CASE CODE	STYLE	LENGTH (L)	WIDTH (W)	MAXIMUM THICKNESS (T)	TERMINATIONS PAD (P)	
					MINIMUM	MAXIMUM
0505	VJ0505	0.055 ± 0.025 (1.40 ± 0.64)	0.055 ± 0.015 (1.40 ± 0.38)	0.057 (1.45)	0.004 (0.10)	0.024 (0.60)
1111	VJ1111	0.117 ± 0.028 (2.98 ± 0.70)	0.110 ± 0.030 (2.79 ± 0.76)	0.102 (2.59)	0.012 (0.30)	0.030 (0.76)

SELECTION CHART				
DIELECTRIC (VISHAY CODE)		BX (X)		
STYLE		VJ0505	VJ1111	TOLERANCE
CASE SIZE		0505	1111	
VOLTAGE (V_{DC})		50	50	
VOLTAGE CODE		A	A	
CAP. CODE	CAP.			
101	100 pF			
121	120 pF			
151	150 pF			
181	180 pF			
221	220 pF			
271	270 pF			
331	330 pF			
391	390 pF			
471	470 pF			
511	510 pF	•		J, K, M
561	560 pF	•		J, K, M
681	680 pF	•		J, K, M
821	820 pF	•		J, K, M
102	1.0 nF	•		J, K, M
122	1.2 nF	•		J, K, M
152	1.5 nF	•		J, K, M
182	1.8 nF	•		J, K, M
222	2.2 nF	•		J, K, M
272	2.7 nF	•		J, K, M
332	3.3 nF	•		J, K, M
392	3.9 nF	•		J, K, M
472	4.7 nF	•		J, K, M
502	5.0 nF	•	•	J, K, M
562	5.6 nF	•	•	J, K, M
682	6.8 nF	•	•	J, K, M
822	8.2 nF	•	•	J, K, M
103	10 nF	•	•	J, K, M
123	12 nF		•	J, K, M
153	15 nF		•	J, K, M
183	18 nF		•	J, K, M
223	22 nF		•	J, K, M
273	27 nF		•	J, K, M
333	33 nF		•	J, K, M
473	47 nF		•	J, K, M
563	56 nF		•	J, K, M
683	68 nF		•	J, K, M
823	82 nF		•	J, K, M
104	100 nF		•	J, K, M

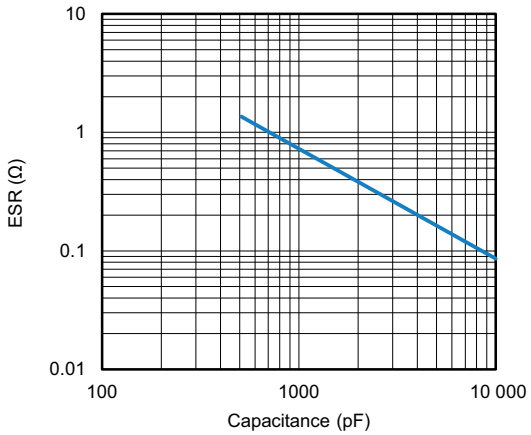
Notes

• Plastic carrier tape

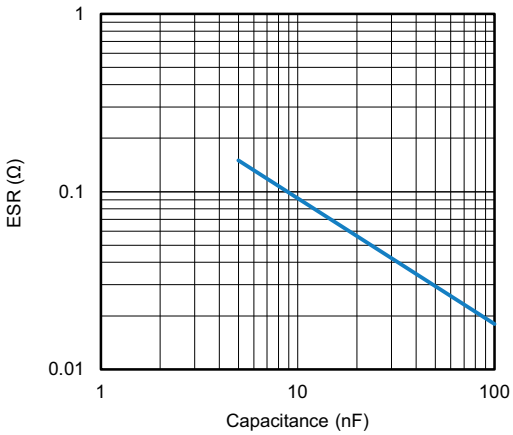
- For soldering conditions see Vishay Soldering Recommendations www.vishay.com/doc?45034

TYPICAL PARAMETERS

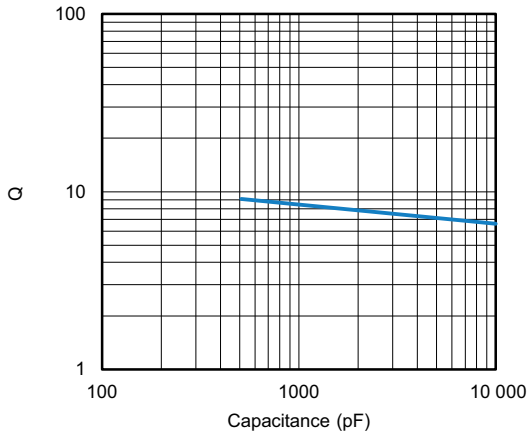
ESR vs. Capacitance at 30 MHz (Size 0505)



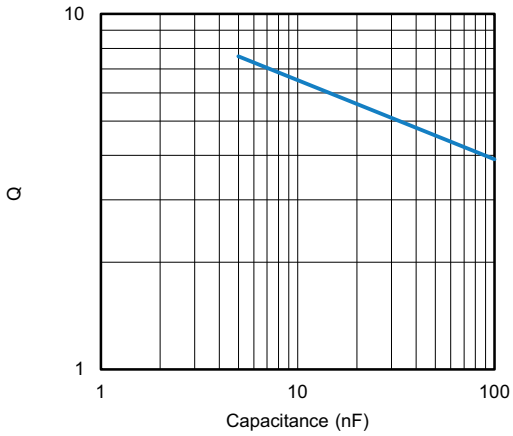
ESR vs. Capacitance at 30 MHz (Size 1111)



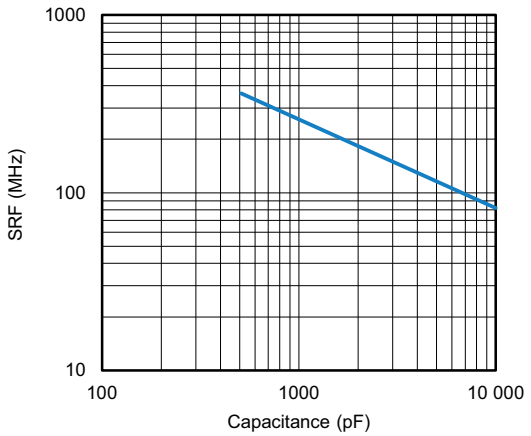
Q vs. Capacitance at 30 MHz (Size 0505)



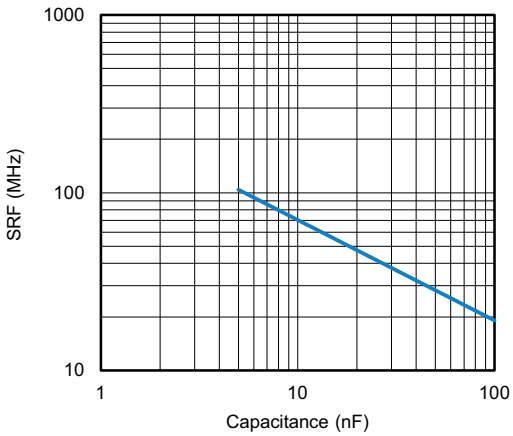
Q vs. Capacitance at 30 MHz (Size 1111)



SRF vs. Capacitance (Size 0505)

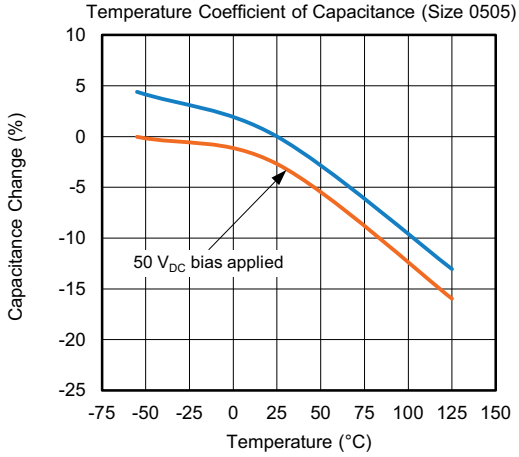


SRF vs. Capacitance (Size 1111)

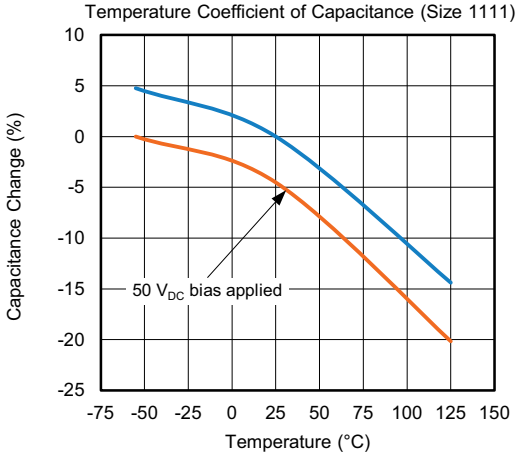


TYPICAL PARAMETERS

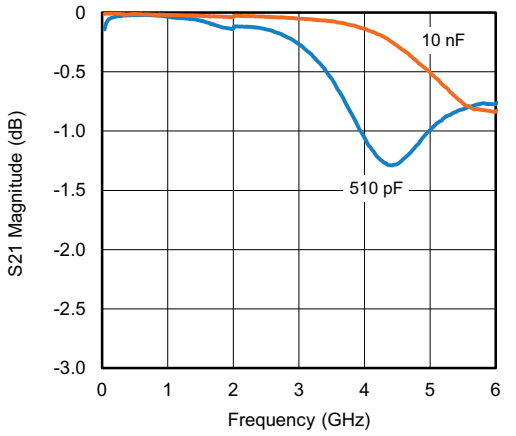
Temperature Coefficient of Capacitance (Size 0505)



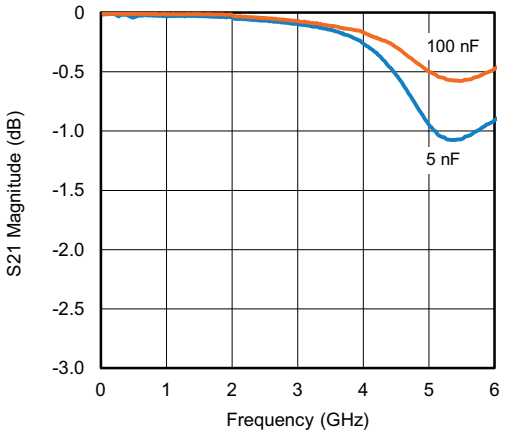
Temperature Coefficient of Capacitance (Size 1111)



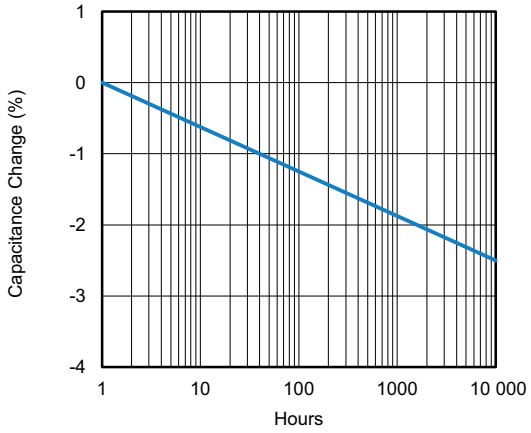
S21 vs. Frequency (Size 0505)



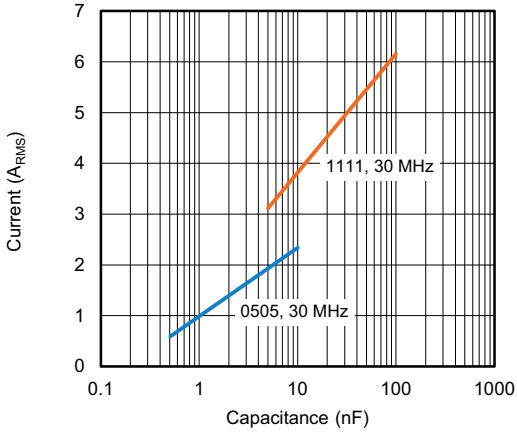
S21 vs. Frequency (Size 1111)



Aging Rate



Current Rating vs. Capacitance (Sizes 0505 and 1111)



STANDARD PACKAGING QUANTITIES (1)(2)(3)

CASE CODE	TAPE SIZE	7" REEL QUANTITIES		11 1/4" AND 13" REEL QUANTITIES
		PLASTIC TAPE PACKAGING CODE "T"	LOW QUANTITY "J"	PLASTIC TAPE PACKAGING CODE "R"
0505	8 mm	3000	1000	10 000
1111 (4)	8 mm	2500	1000	9000

Notes

(1) Vishay Vitramon uses embossed plastic carrier tape
(2) REFERENCE: EIA standard RS 481 - "Taping of Surface Mount Components for Automatic Placement"
(3) n/a = not available
(4) Packaging "T" / "R" or lower quantities can depend from product thickness

STORAGE AND HANDLING CONDITIONS

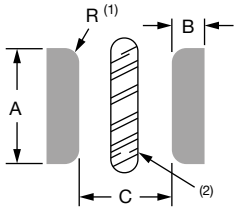
(1) Store the components at 5 °C to +40 °C ambient temperature and ≤ 70 % relative humidity conditions.
(2) The product is recommended to be used within a time-frame of 2 years after shipment.
Check solderability in case extended shelf life beyond the expiry date is needed.

Precautions:

a. Do not store products in an environment containing corrosive elements, especially where chloride gas, sulfide gas, acid, alkali, salt or the like are present. This may cause corrosion or oxidization of the terminations, which can easily lead to poor soldering.
b. Store products on the shelf and avoid exposure to moisture or dust.
c. Do not expose products to excessive shock, vibration, direct sunlight and so on.

Solder Pad Dimensions for Vishay Surface-Mount Multilayer Ceramic Chip Capacitors

DIMENSIONS in millimeters



CASE CODE	A	B	C
0402	0.50	0.50	0.40
0505	1.35	1.00	0.60
0603	0.90	1.00	1.00 (3)
0805	1.30	1.20	1.00
1111	2.90	1.30	1.75
1206	1.80	1.20	2.10
1210	2.80	1.30	1.90
1808	2.40	1.50	3.00
1812	3.60	1.50	3.00
1825	6.50	1.50	3.00
2008	2.70	1.50	4.08
2220	5.50 (4)	1.50	4.20
2225	6.50	1.50	4.20
2525	6.60	1.50	4.50
3040	10.80	2.00	5.50
3640	10.80	2.00	7.00
3838	10.20	2.00	7.50
4044	12.30	2.00	8.00

Notes

(1) For safety capacitors and voltages above 3000 V, corner rounding (R) of 0.5 mm is recommended to suppress arcing
(2) Add a 1 mm slot in PCB between pads to allow cleaning and coating under MLCC
(3) For VJ HiFREQ Series, this dimension is 0.6 mm
(4) For safety capacitors, the A dimension should be 5.80 mm

PRINTED CIRCUIT BOARD PCB DESIGN CONSIDERATIONS FOR HIGH VOLTAGE SURFACE-MOUNT MLCCS

Special assembly process and design considerations should be employed for today's high voltage rating MLCCs. As case sizes remain the same and voltage ratings increase, MLCC manufacturers must design, evaluate, and qualify their capacitors using methods that reduce the occurrence of corona discharge and arcover events. To meet similar capability in high voltage applications, users should employ similar cautionary design and assembly methods.

MLCC PAD LAYOUT

A capacitor's arcover inception point can degrade due to factors such as the MLCC termination, PCB pad design, PCB cleanliness, solder flux residue, surface contamination / deposits and environmental conditions. PCB pads and their design affect the air gap distance between the opposing polarities of the MLCC termination. For voltage rating greater than 1500 V_{DC} add a corner radius to the inward facing edge of the MLCC pads and as large a gap as possible between the pads. Too small of a pad gap distance will reduce the capacitor's own arcover inception voltage level. Refer to the Figure and Table Figure 1.0, MLCC Pad Layout and Table 1.0, Vishay MLCC Solder Pad Dimensions for the recommended MLCC solder pad dimensions.

SLOT OR TRENCH BETWEEN PADS

PCB assembly can deposit dust, trap solder balls, or flux residue underneath the capacitors. These contaminants will reduce conductive clearances and the arcover inception level. Assembly methods must include a final PCB cleaning process. A slot or trench can be cut into the PCB in between the pads to allow cleaners to penetrate underneath the MLCC. The slot will also allow conformal or epoxy coatings to flow underneath the MLCC and build an insulative barrier between pads. Refer to Figure 1.0 MLCC Pad Layout for slot reference location.

COATING PRINTED CIRCUIT BOARD

Coating a printed circuit board with materials such as acrylic, silicone and urethane resins provide a protective dielectric barrier that is non-conductive and will enhance the resistance to arcing. Various processes exist which include dipping, brushing, and spaying. Optimal performance will come from coating the MLCC on all sides, top and bottom. The PCB slot in between the pads should extend slightly beyond the width of the MLCC. Refer to Figure 1.0 MLCC Pad Layout for slot reference location.

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