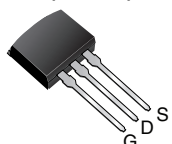
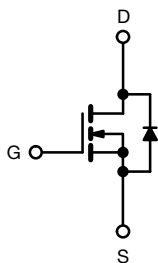
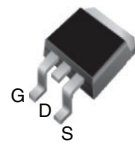


## Power MOSFET

I<sup>2</sup>PAK (TO-262)



D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V  $V_{GS}$  rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Extremely high frequency operation
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### DESCRIPTION

This series of low charge power MOSFETs achieve significantly lower gate charge than conventional Power MOSFETs. Utilizing the new LCDMOS (low charge device Power MOSFETs) technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge Power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that characterize Power MOSFETs offer the designer a new power transistor standard for switching applications.

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.85
$Q_g$ max. (nC)	39	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	19	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF840LCS-GE3	SiHF840LCL-GE3
Lead (Pb)-free	IRF840LCSPbF	IRF840LCLPbF
	IRF840LCSTRPbF	-

### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$	28	W/ $^\circ\text{C}$
Linear Derating Factor		1.0	
Single Pulse Avalanche Energy <sup>b, e</sup>	$E_{AS}$	510	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$	8.0	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	13	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	W
		$T_A = 25^\circ\text{C}$	
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>	$dV/dt$	3.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering Recommendations (Peak temperature) <sup>d</sup>	For 10 s	300	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 14\text{ mH}$ ,  $R_g = 25\ \Omega$ ,  $I_{AS} = 8.0\text{ A}$  (see fig. 12)
- $I_{SD} \leq 8.0\text{ A}$ ,  $dI/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case
- Uses IRF840LC, SiHF840LC data and test conditions




## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mounted, steady-state) <sup>a</sup>	R <sub>thJA</sub>	-	40	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0	

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

## SPECIFICATIONS (T<sub>J</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>c</sup>	-	0.63	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	25	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.8 A <sup>b</sup>	-	-	0.85	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 4.8 A <sup>b</sup>	4.0	-	-	S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5 <sup>c</sup>	-	1100	-	pF
Output Capacitance	C <sub>oss</sub>		-	170	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	18	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.0 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b, c</sup>	-	-	39	nC
Gate-Source Charge	Q <sub>gs</sub>		-	-	10	
Gate-Drain Charge	Q <sub>gd</sub>		-	-	19	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 8.0 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b, c</sup>	-	12	-	ns
Rise Time	t <sub>r</sub>		-	25	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	27	-	
Fall Time	t <sub>f</sub>		-	19	-	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain	0.7	-	3.7	Ω
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.0	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		-	-	28	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 8.0 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 8.0 A, dI/dt = 100 A/μs <sup>b, c</sup>	-	490	740	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	3.0	4.5	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )				

### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

c. Uses SiHF840LC data and test conditions



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

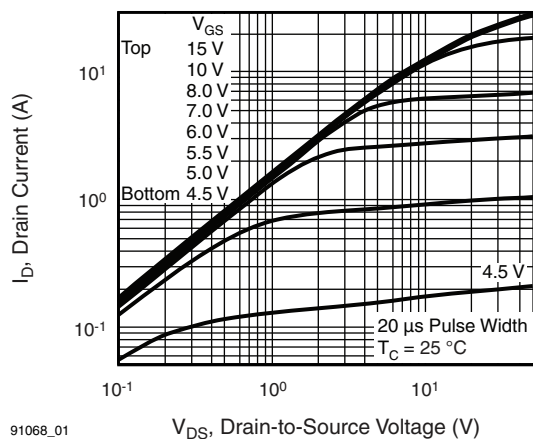


Fig. 1 - Typical Output Characteristics

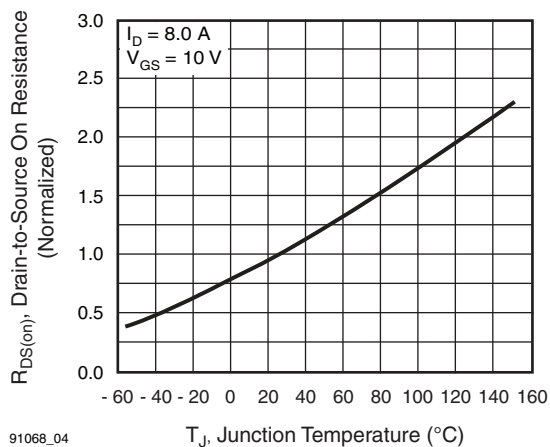


Fig. 4 - Normalized On-Resistance vs. Temperature

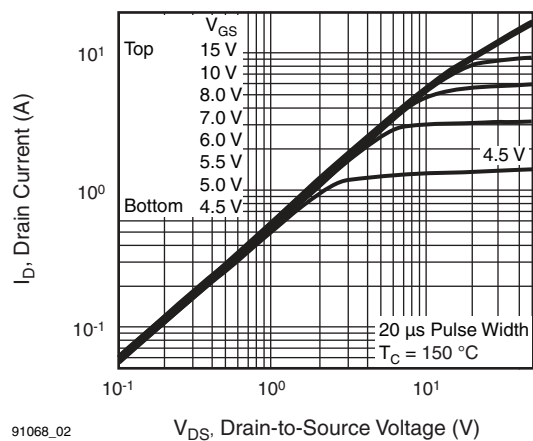


Fig. 2 - Typical Output Characteristics

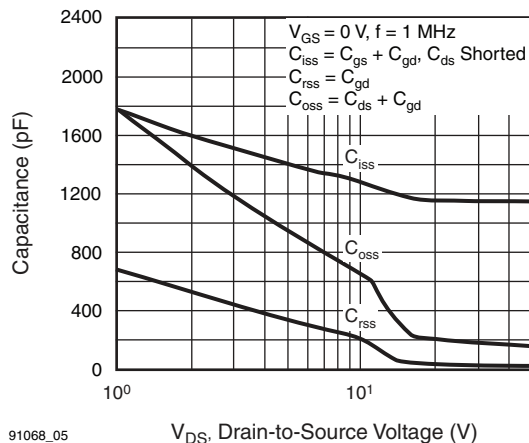


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

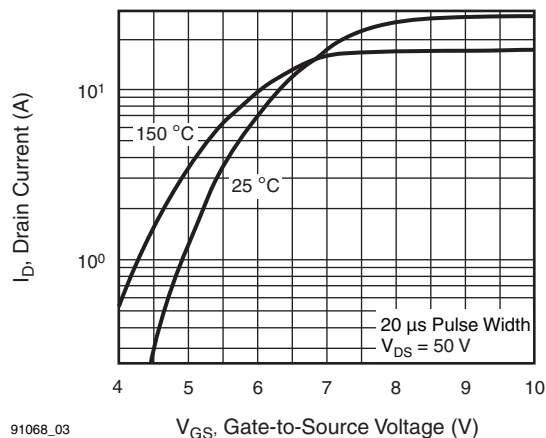


Fig. 3 - Typical Transfer Characteristics

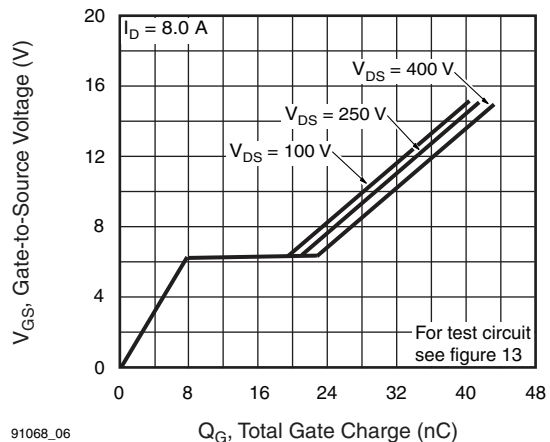
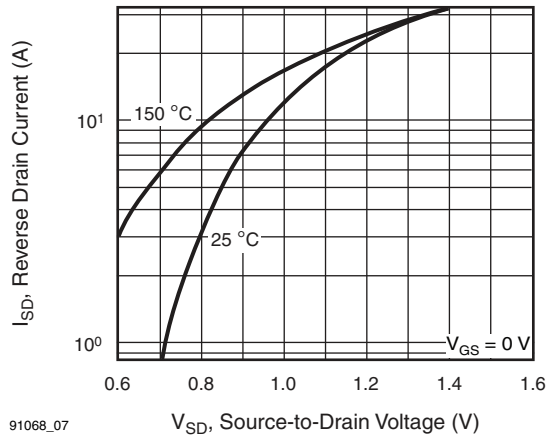
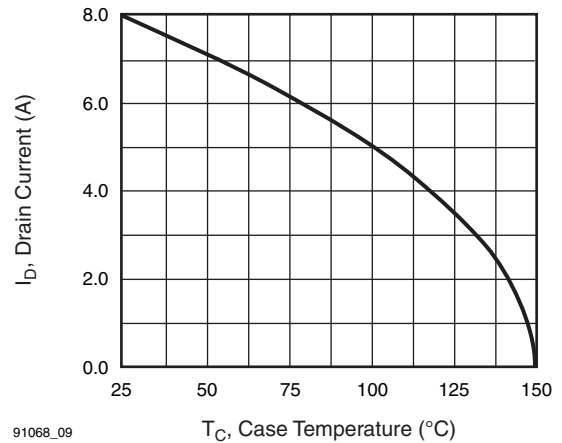


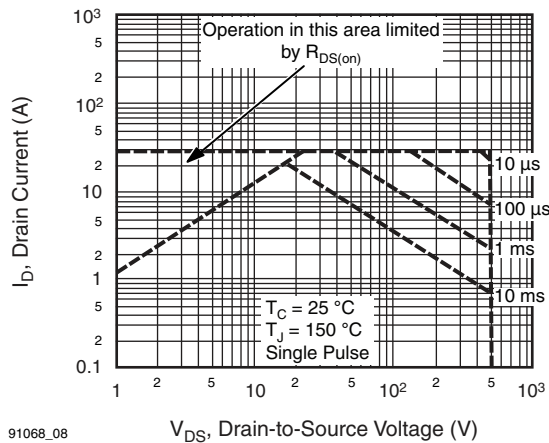
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



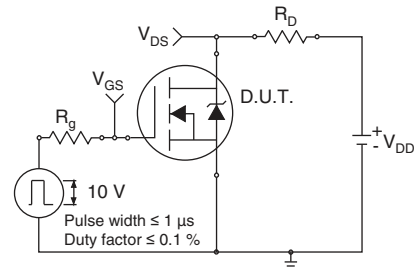
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



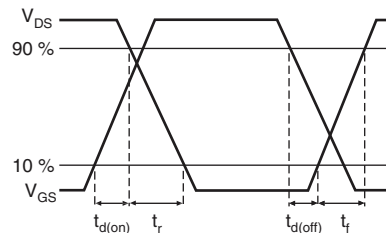
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



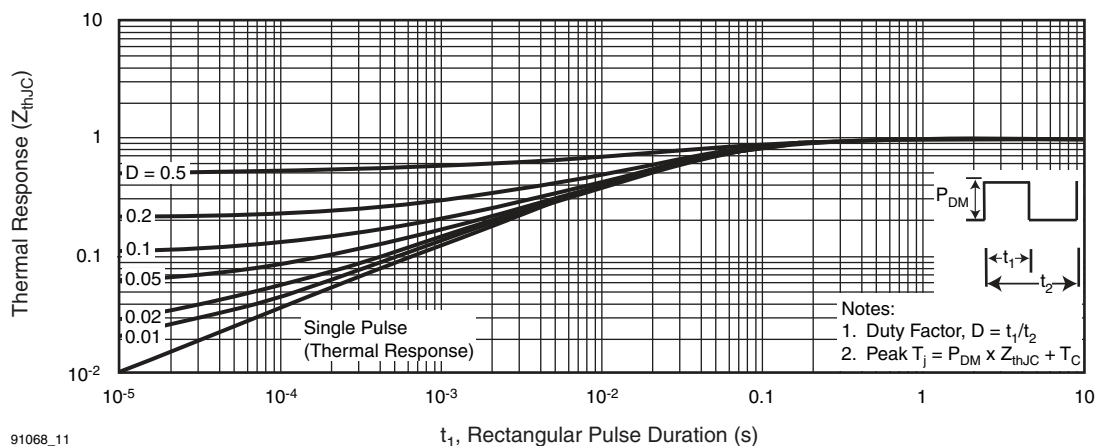
**Fig. 8 - Maximum Safe Operating Area**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

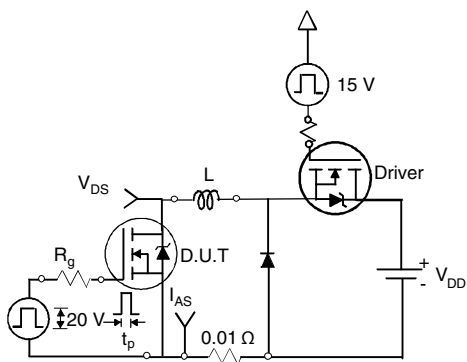


Fig. 12a - Unclamped Inductive Test Circuit

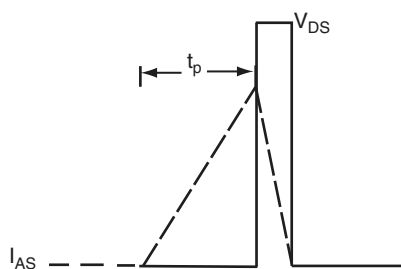
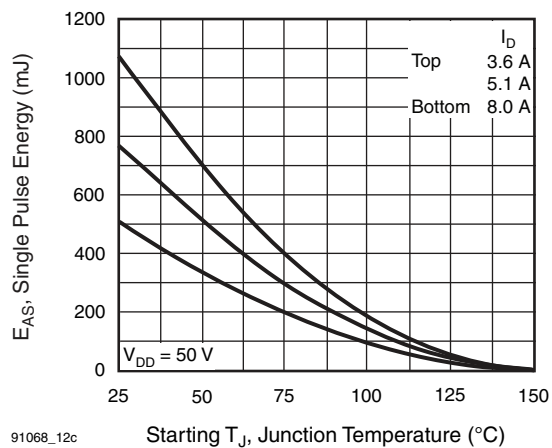


Fig. 12b - Unclamped Inductive Waveforms



91068\_12c

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

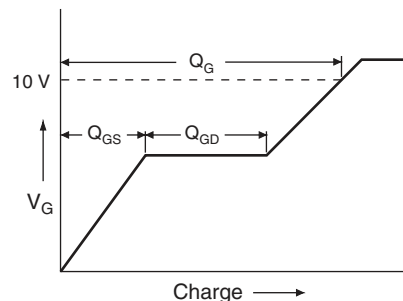


Fig. 13a - Basic Gate Charge Waveform

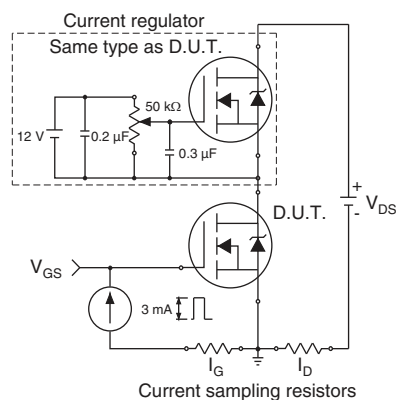
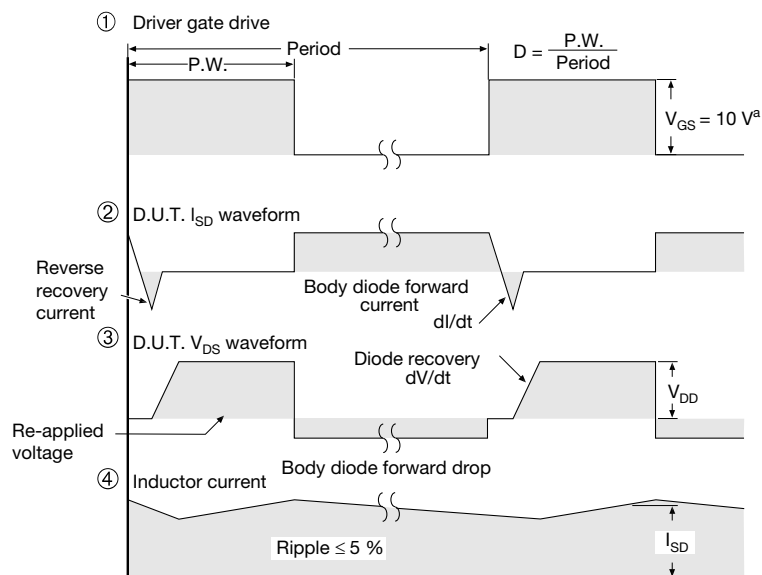
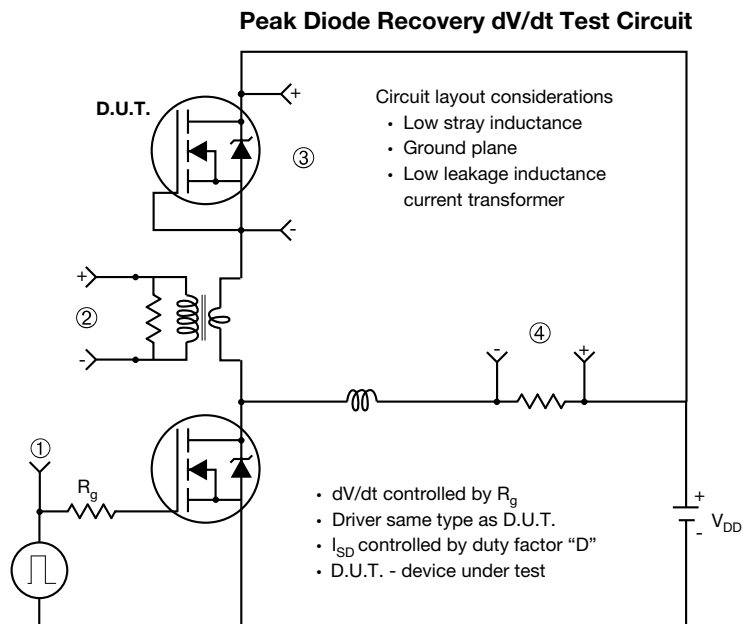


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

## TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

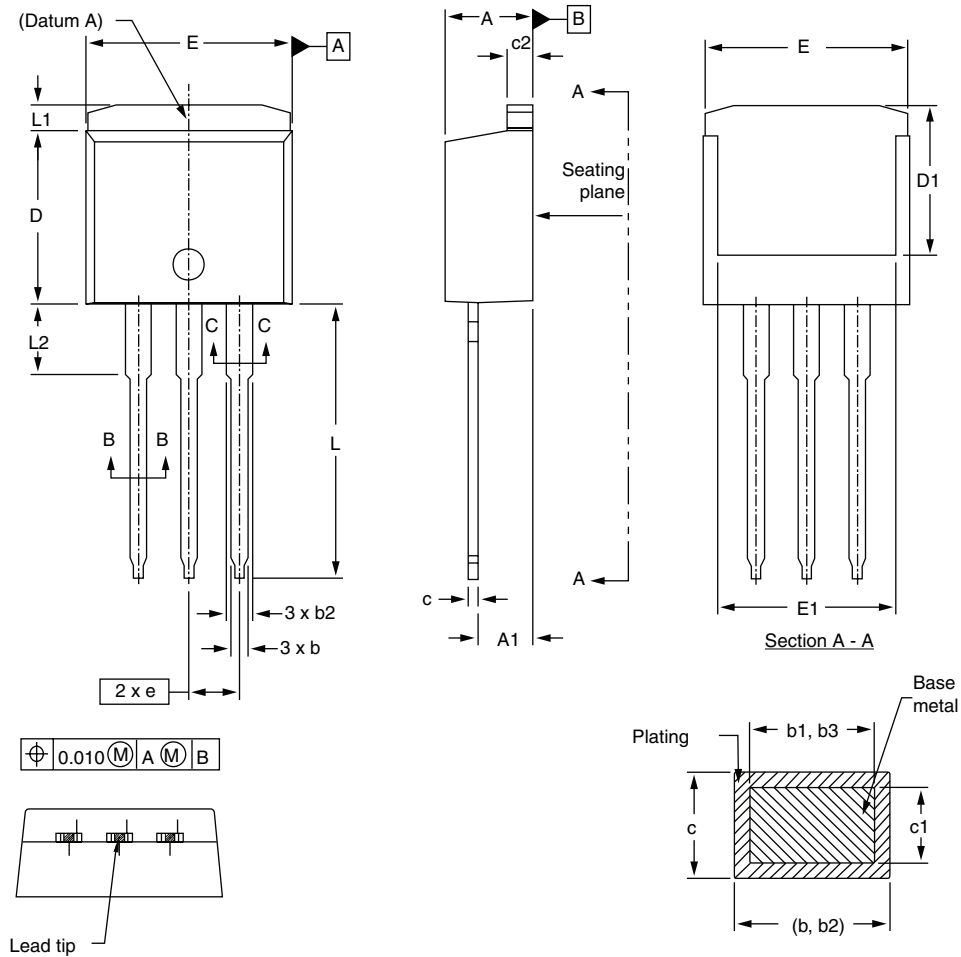
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## I<sup>2</sup>PAK (TO-262) (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08  
DWG: 5977

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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