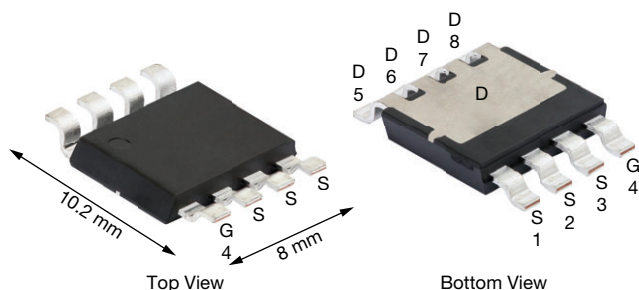


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

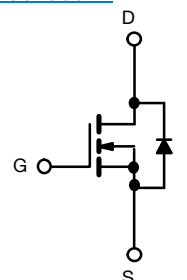
**PowerPAK® 8 x 8LR**


## FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



N-Channel MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0015
$I_D$ (A)	372
Configuration	Single

## ORDERING INFORMATION

Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ148ER (for detailed order number please see <a href="http://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current	$I_D$	372	A
$T_C = 25$ °C		214	
Continuous source current (diode conduction)	$I_S$	360	
Pulsed drain current <sup>b</sup>	$I_{DM}$	670	
Single pulse avalanche current	$I_{AS}$	46	mJ
Single pulse avalanche energy	$E_{AS}$	105	
Maximum power dissipation	$P_D$	394	W
$T_C = 25$ °C		131	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	44	°C/W
Junction-to-case (drain)	$R_{thJC}$	0.38	

### Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		40	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	3	3.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	200	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.00125	0.0015	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0025	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0031	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 60 A		-	120	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	4170	5750	pF
Output capacitance	C <sub>oss</sub>			-	1566	2193	
Reverse transfer capacitance	C <sub>rss</sub>			-	131	184	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 20 A	-	68	102	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	20	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	15	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.8	1.6	2.4	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	17	26	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	88	132	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	30	45	
Fall time <sup>c</sup>	t <sub>f</sub>			-	12	18	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Reverse recovery time	t <sub>rr</sub>	V <sub>DD</sub> = 32 V, I <sub>FM</sub> = 15 A, di/dt = 100 A/μs		-	47	94	ns
Reverse recovery charge	Q <sub>rr</sub>			-	47	94	nC
Reverse recovery current	I <sub>RM</sub>			-	-	1.8	A
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	1600	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0		-	0.8	1.1	V

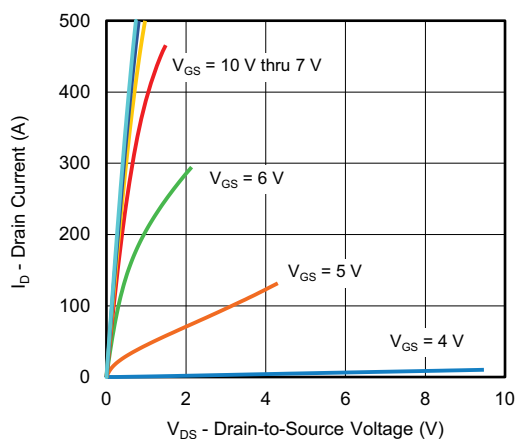
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

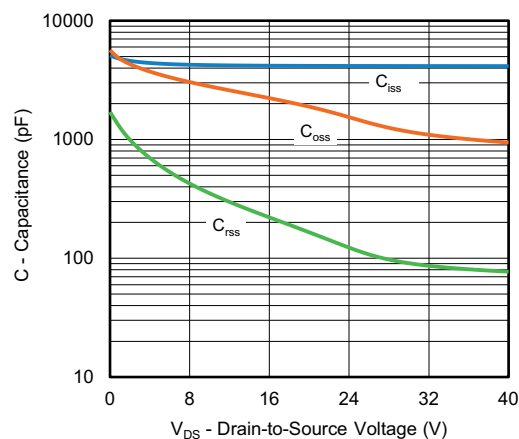
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



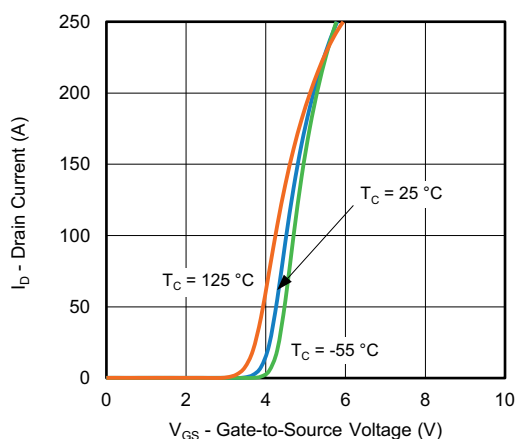
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



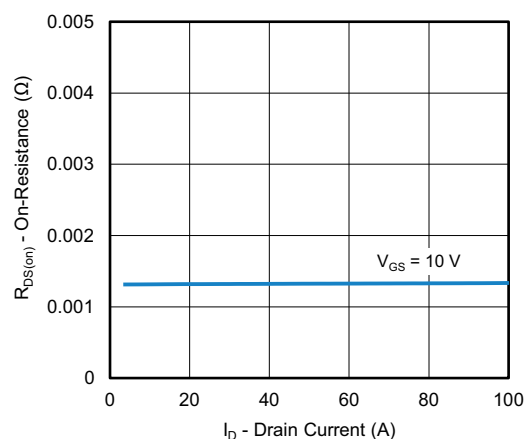
**Output Characteristics**



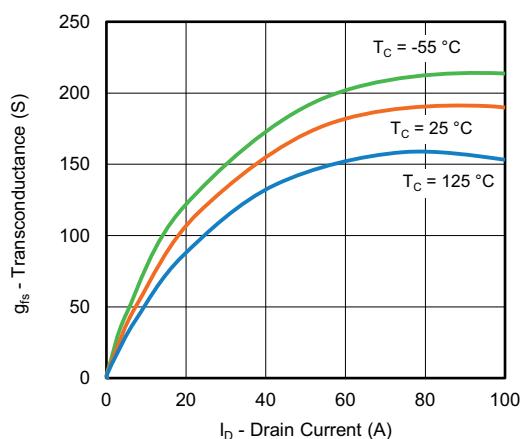
**Capacitance**



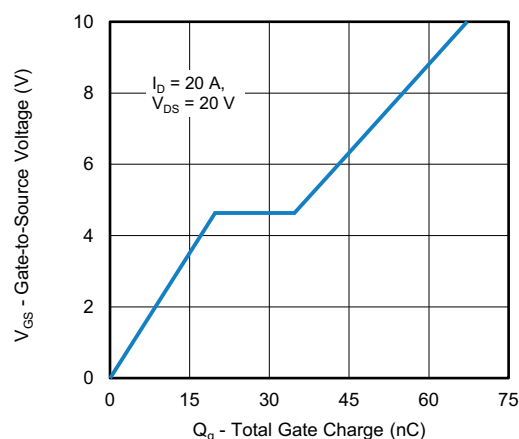
**Transfer Characteristics**



**On-Resistance vs. Drain Current**



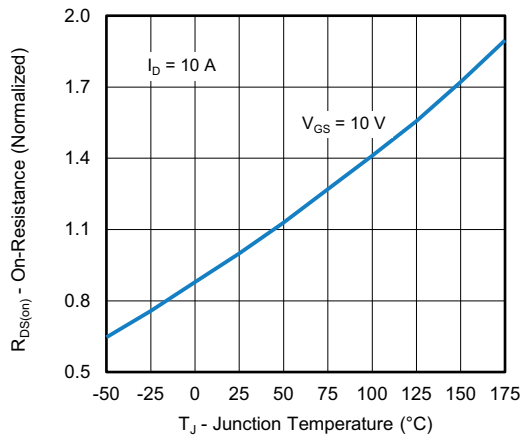
**Transconductance**



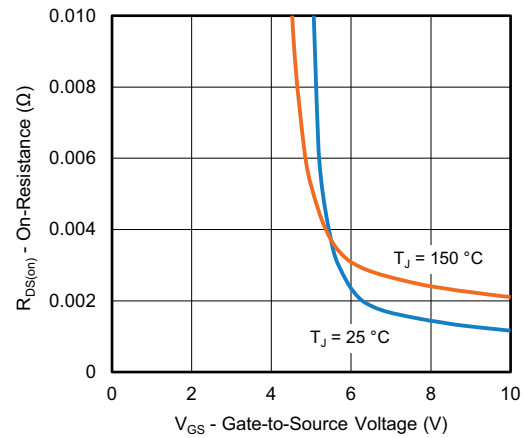
**Gate Charge**



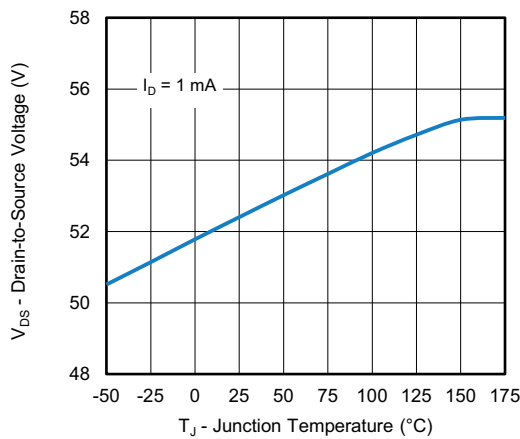
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



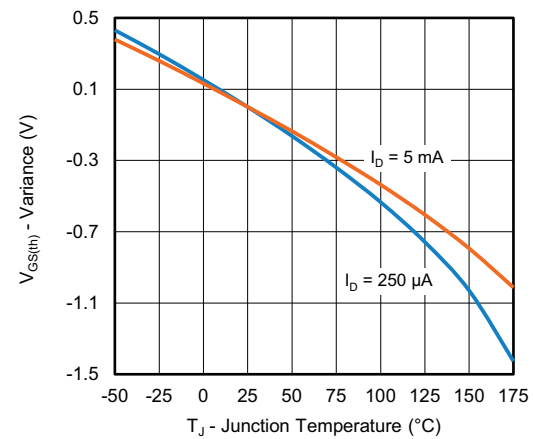
**On-Resistance vs. Junction Temperature**



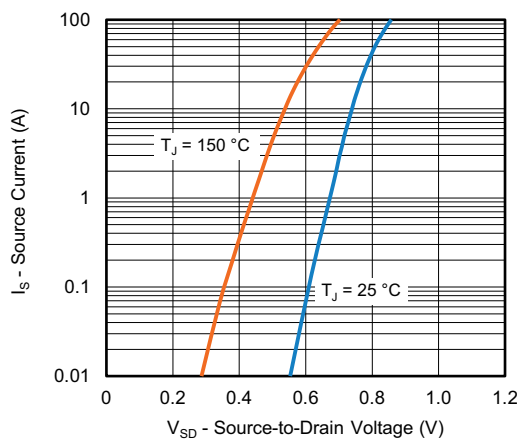
**On-Resistance vs. Gate-to-Source Voltage**



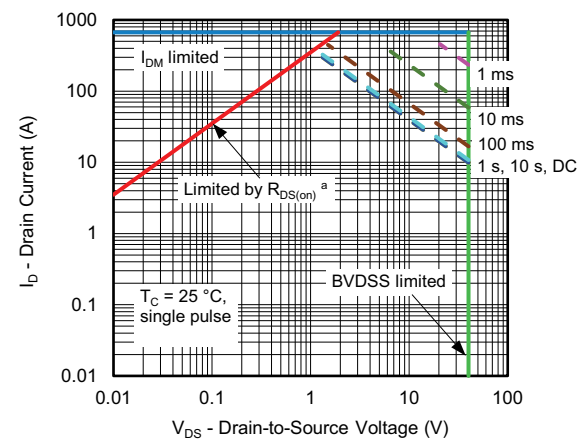
**Drain Source Breakdown vs. Junction Temperature**



**Threshold Voltage**



**Source Drain Diode Forward Voltage**



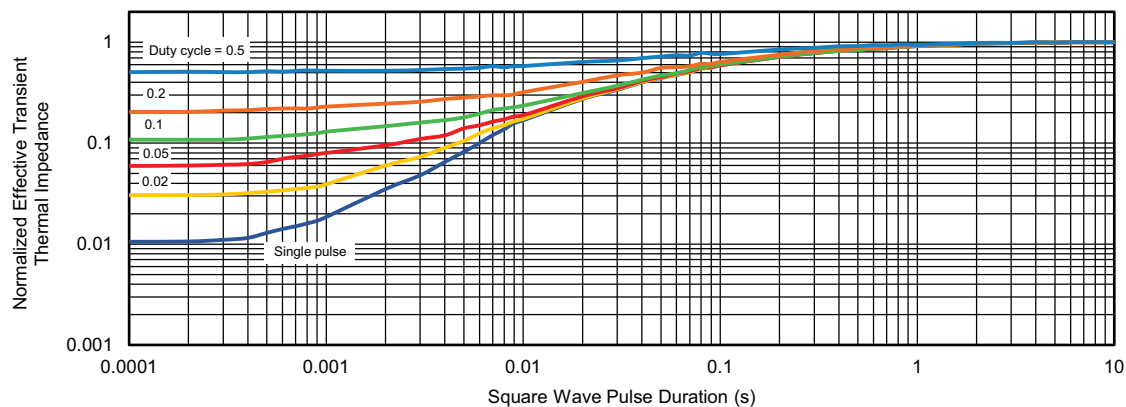
**Safe Operating Area**

**Note**

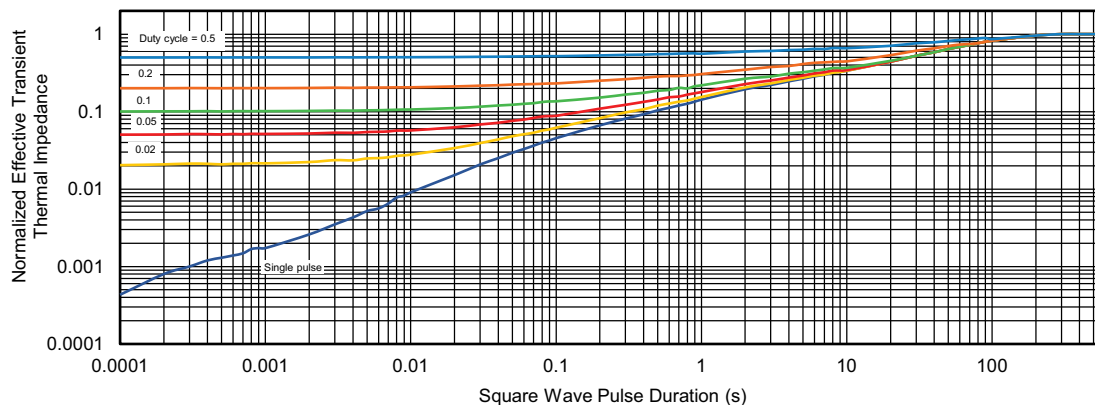
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



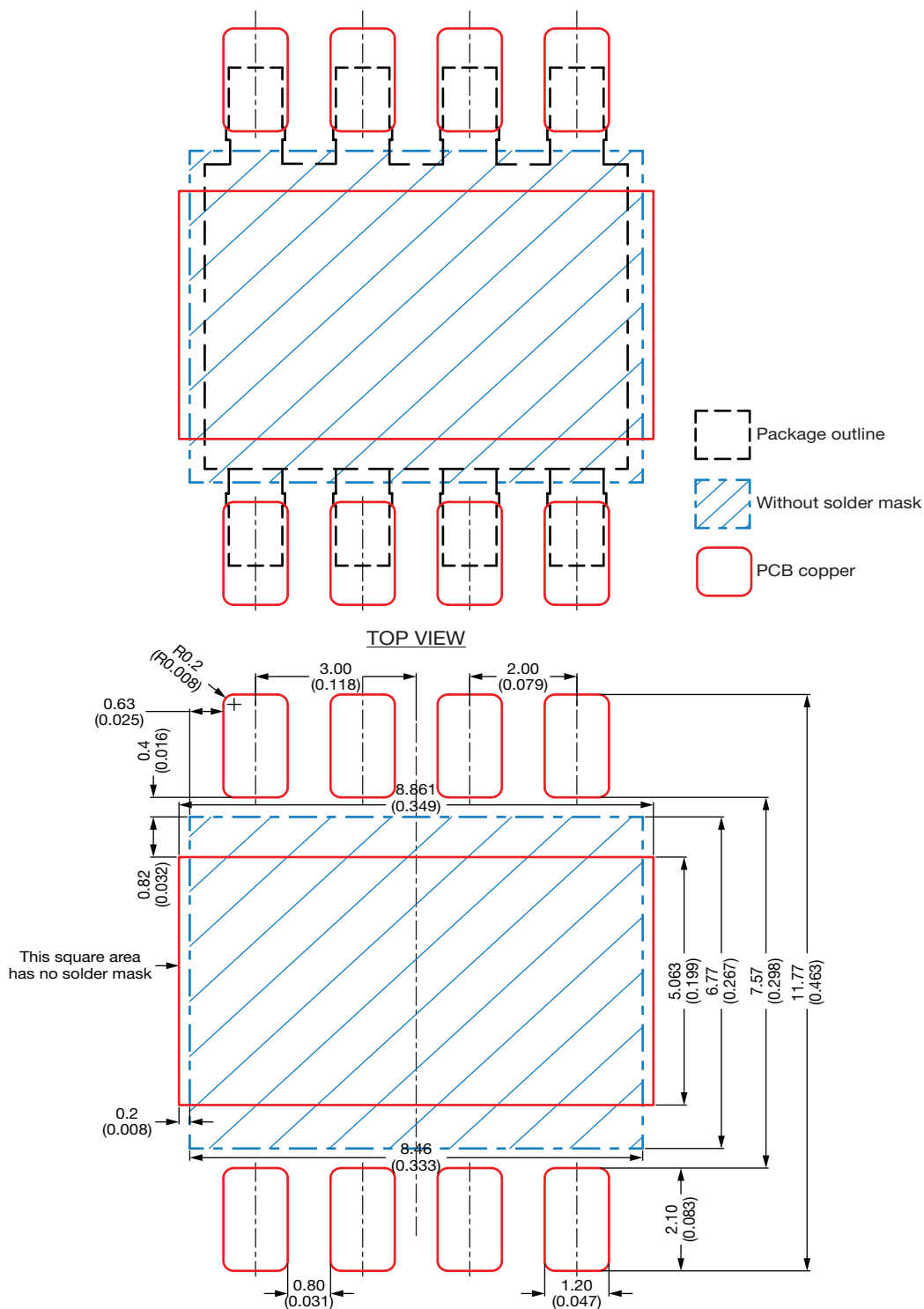
**Normalized Thermal Transient Impedance, Junction-to-Case**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

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# Recommended Land Pattern PowerPAK® 8 x 8LR



## Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023

DWG: 3002



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