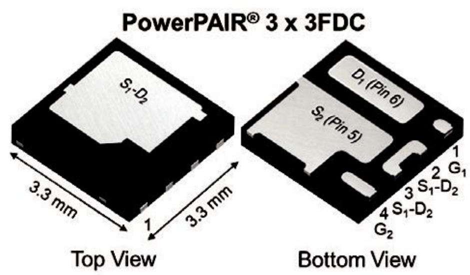
Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode



PRODUCT SUMMARY

	CHANNEL-1	CHANNEL-2
V_{DS} (V)	30	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00450	0.00190
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00750	0.00260
Q_g typ. (nC)	6.9	19.4
I_D (A) [a]	83	143
Configuration	Dual	

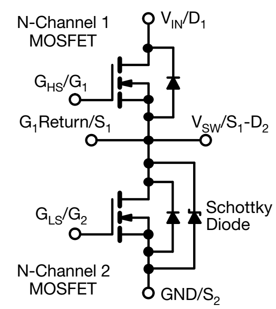
FEATURES

- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky
- 100 % R_g and UIS tested
- Double cooled feature provides additional avenue for thermal transfer
- Internally connected half-bridge configuration in 3.3 mm-by-3.3 mm footprint
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



ORDERING INFORMATION

Package	PowerPAIR 3 x 3FDC
Lead (Pb)-free and halogen-free	SiZF360DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT
Drain-source voltage		V_{DS}	30	30	V
Gate-source voltage		V_{GS}	+20, -16	+16, -12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	83	143	A
	T_C = 70 °C		66	114	
	T_A = 25 °C		23 [b, c]	34 [b, c]	
	T_A = 70 °C		18 [b, c]	27 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	150	200	
Continuous source-drain diode current	T_C = 25 °C	I_S	47	111	
	T_A = 25 °C		3.4 [b, c]	6.2 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	14	16	
Single pulse avalanche energy		E_{AS}	9.8	12.8	mJ
Maximum power dissipation	T_C = 25 °C	P_D	52	78	W
	T_C = 70 °C		33	50	
	T_A = 25 °C		3.8 [b, c]	4.3 [b, c]	
	T_A = 70 °C		2.4 [b, c]	2.8 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	26	33	23	29	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.8	2.4	0.76	1	
Maximum junction-to-case (source)	Steady state	R_{thJC}	2.6	3.4	1.2	1.6	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3FDC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 66 °C/W for channel-1 and 67 °C/W for channel-2

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	Ch-1	30	-	-	V
			Ch-2	30	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	Ch-1	1.1	-	2.2	
			Ch-2	1.0	-	2.2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V, -16 V	Ch-1	-	-	± 100	nA
		V_{DS} = 0 V, V_{GS} = +16 V, -12 V	Ch-2	-	-	± 100	
Zero Gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch-1	-	-	1	μA
			Ch-2	-	30	350	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1	-	-	5	
			Ch-2	-	150	3000	
On-state drain current [b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	Ch-1	10	-	-	A
			Ch-2	10	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	Ch-1	-	0.00330	0.00450	Ω
		V_{GS} = 10 V, I_D = 10 A	Ch-2	-	0.00160	0.00190	
		V_{GS} = 4.5 V, I_D = 7 A	Ch-1	-	0.00490	0.00750	
		V_{GS} = 4.5 V, I_D = 7 A	Ch-2	-	0.00210	0.00260	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 20 A	Ch-1	-	60	-	S
		V_{DS} = 10 V, I_D = 20 A	Ch-2		90	-	
Dynamic [a]							
Input capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	-	1100	-	pF
			Ch-2	-	3150	-	
Output capacitance	C_{oss}		Ch-1	-	530	-	
			Ch-2	-	1550	-	
Reverse transfer capacitance	C_{rss}		Ch-1	-	40	-	
			Ch-2	-	170	-	
C_{rss}/C_{iss} ratio			Ch-1	-	0.036	0.072	
			Ch-2		0.054	0.108	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	Ch-1	-	14.4	22	nC
			Ch-2	-	41	62	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-1		6.9	10.5	
			Ch-2	-	19.4	29	
Gate-source charge	Q_{gs}		Ch-1	-	3.1	-	
			Ch-2	-	7.1	-	
Gate-drain charge	Q_{gd}		Ch-1	-	1.5	-	
			Ch-2	-	3.8	-	
Output charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	Ch-1	-	13	-	
			Ch-2	-	40	-	
Gate resistance	R_g	f = 1 MHz	Ch-1	0.14	0.7	1.4	Ω
			Ch-2	0.12	0.62	1.2	
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1	-	17	35	ns
			Ch-2	-	25	50	
Rise time	t_r		Ch-1	-	40	80	
			Ch-2	-	53	110	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	23	45	
			Ch-2	-	30	60	
Fall time	t_f		Ch-1	-	7	15	
			Ch-2	-	12	25	
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1	-	11	20	
			Ch-2	-	13	25	
Rise time	t_r		Ch-1	-	5	10	
			Ch-2	-	20	40	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	23	45	
			Ch-2	-	32	65	
Fall time	t_f		Ch-1	-	5	10	
			Ch-2	-	6	15	

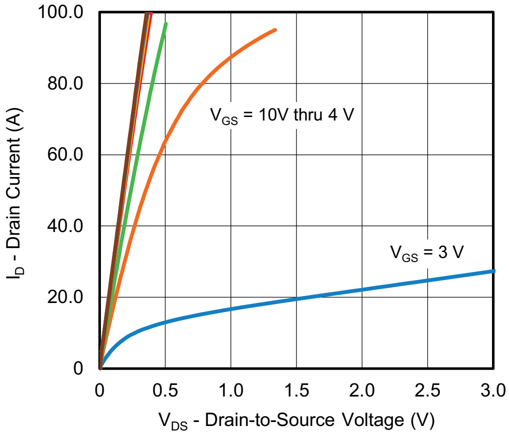
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	Ch-1	-	-	47	A
			Ch-2	-	-	111	
Pulse diode forward current [a]	I_{SM}		Ch-1	-	-	150	
			Ch-2	-	-	200	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	Ch-1	-	0.75	1.1	V
		I_S = 5 A, V_{GS} = 0 V	Ch-2	-	0.44	0.7	
Body diode reverse recovery time	t_{rr}	Channel-1 I_F = 10 A, di/dt = 100 A/μs, T_J = 25 °C	Ch-1	-	36	75	ns
			Ch-2	-	46	90	
Body diode reverse recovery charge	Q_{rr}		Ch-1	-	26	55	nC
			Ch-2	-	40	80	
Reverse recovery fall time	t_a	Channel-2 I_F = 10 A, di/dt = 100 A/μs, T_J = 25 °C	Ch-1	-	16	-	ns
			Ch-2	-	18	-	
Reverse recovery rise time	t_b		Ch-1	-	20	-	
			Ch-2	-	28	-	

Notes

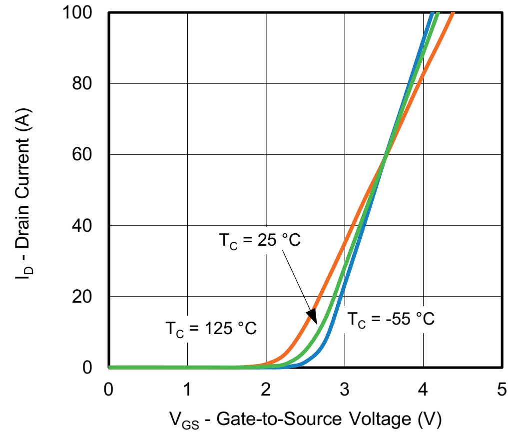
a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

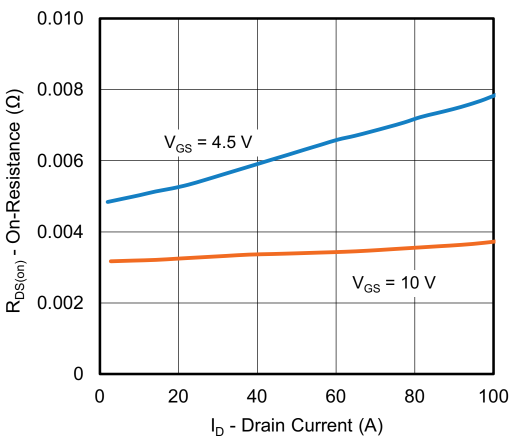
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



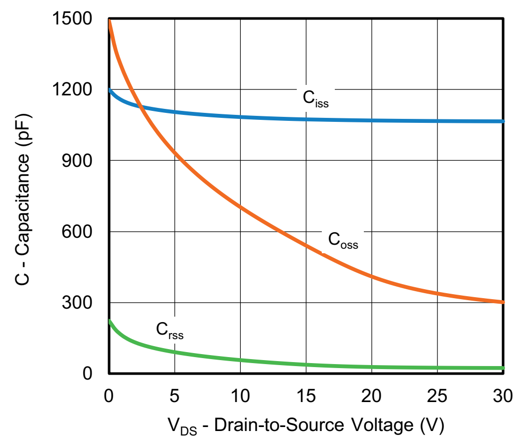
Output Characteristics



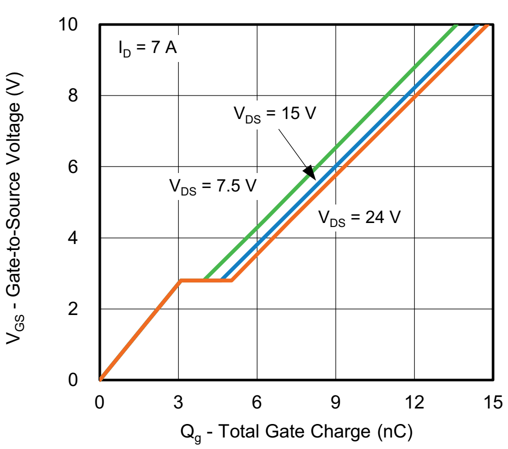
Transfer Characteristics



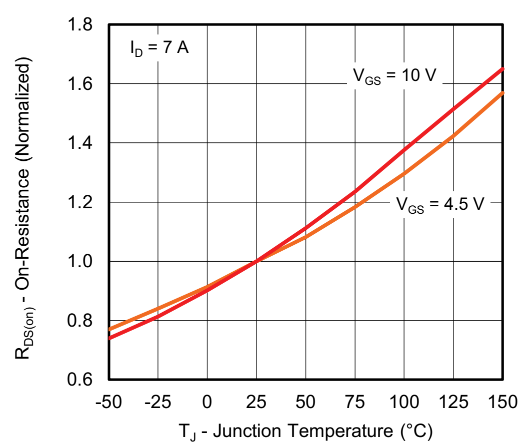
On-Resistance vs. Drain Current



Capacitance

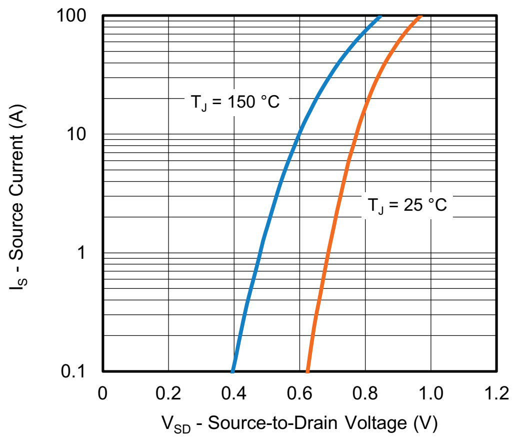


Gate Charge

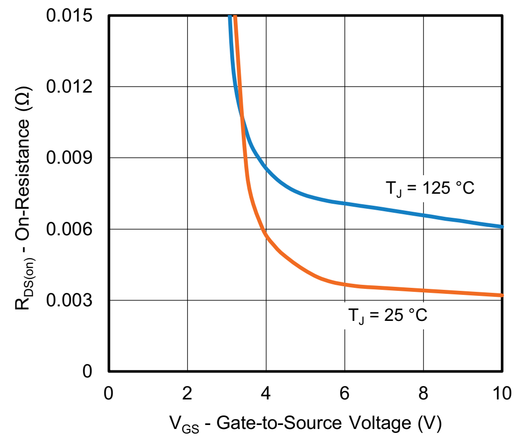


On-Resistance vs. Junction Temperature

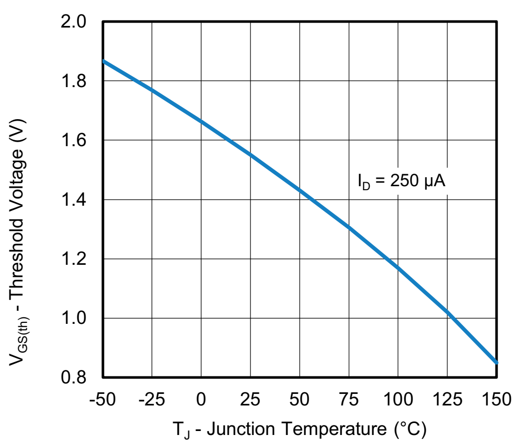
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



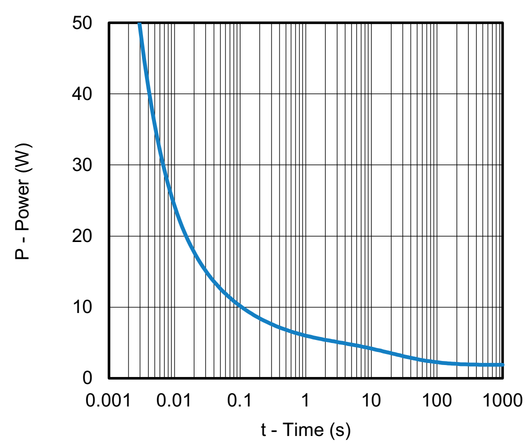
Source-Drain Diode Forward Voltage



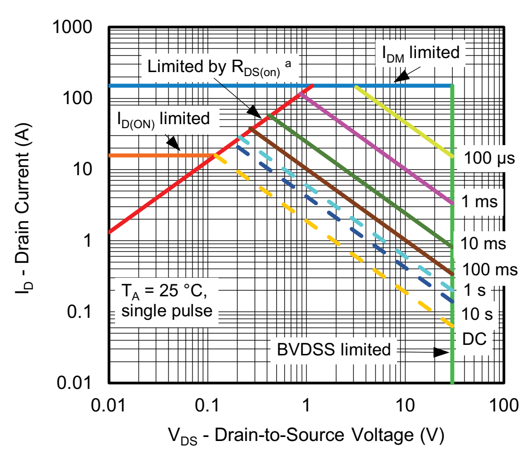
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

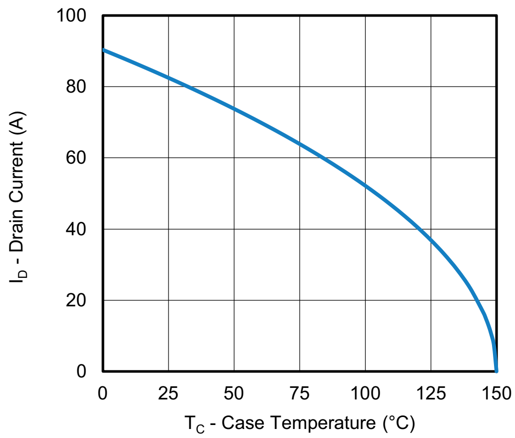


Safe Operating Area, Junction-to-Ambient

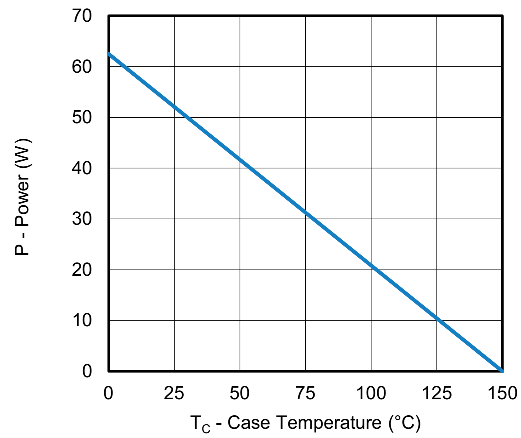
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

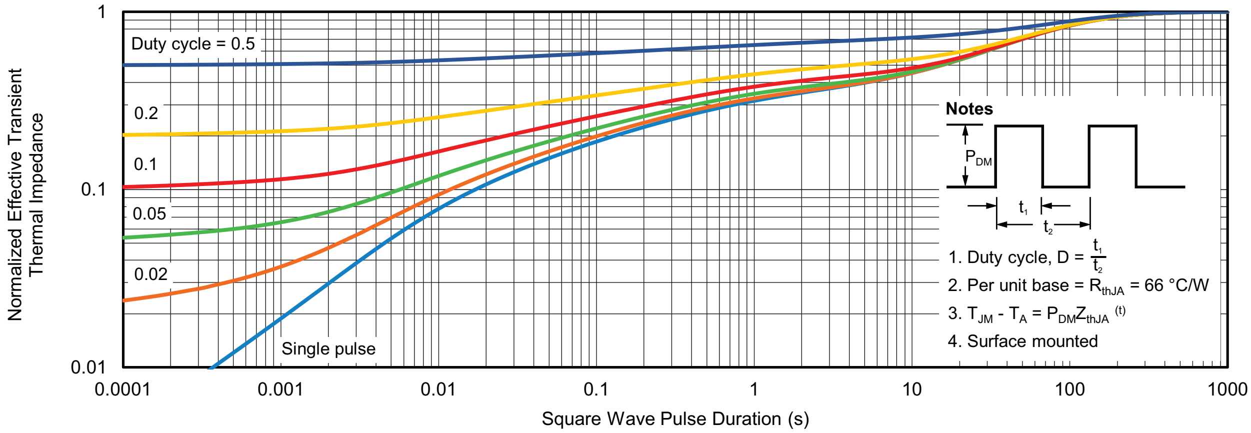


Power, Junction-to-Case

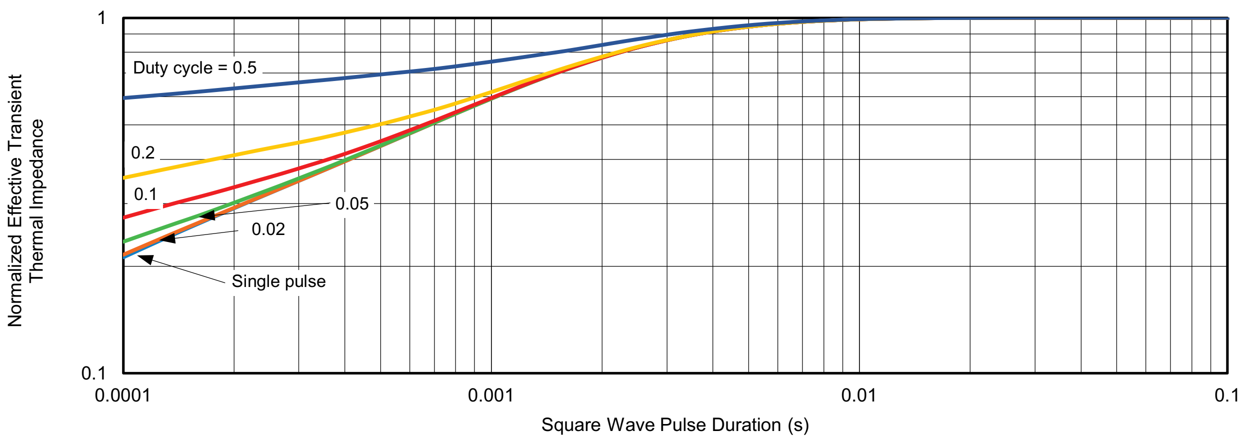
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

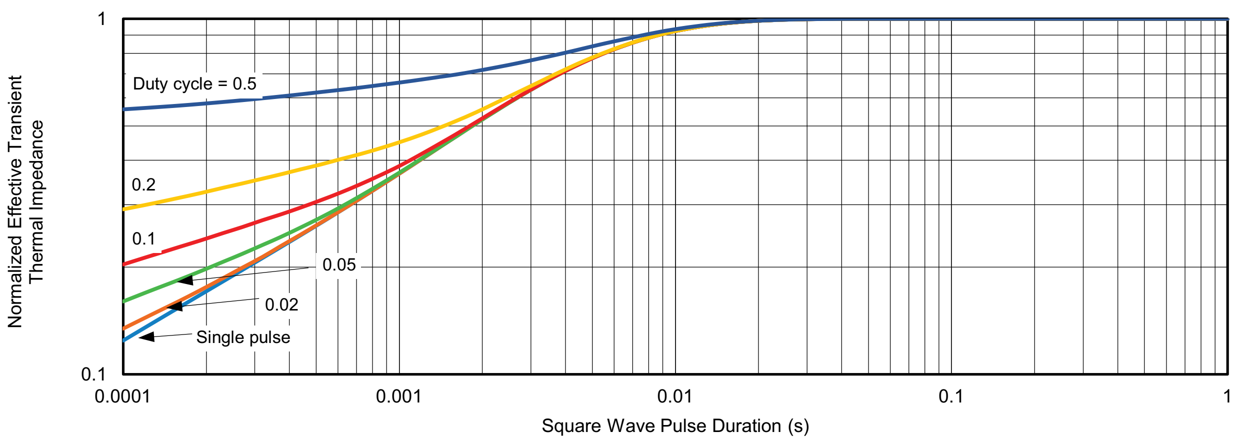
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

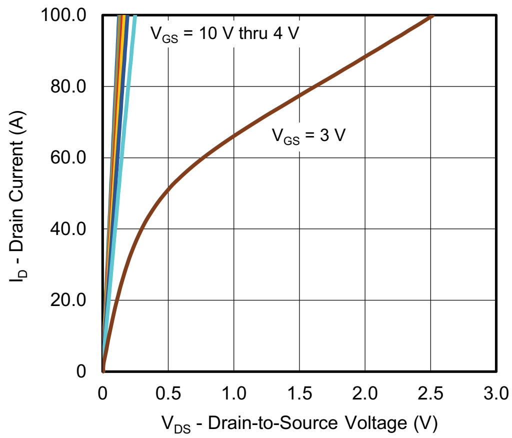


Normalized Thermal Transient Impedance, Junction-to-Case (Drain)

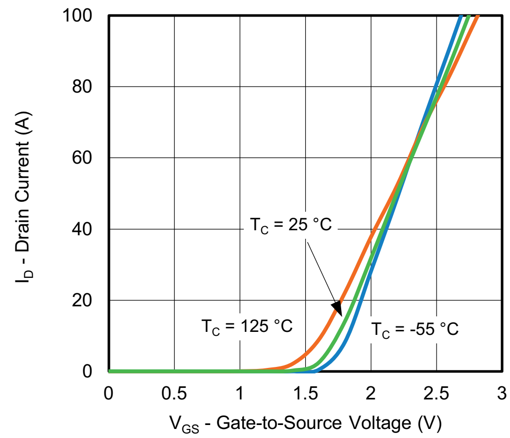


Normalized Thermal Transient Impedance, Junction-to-Case (Source)

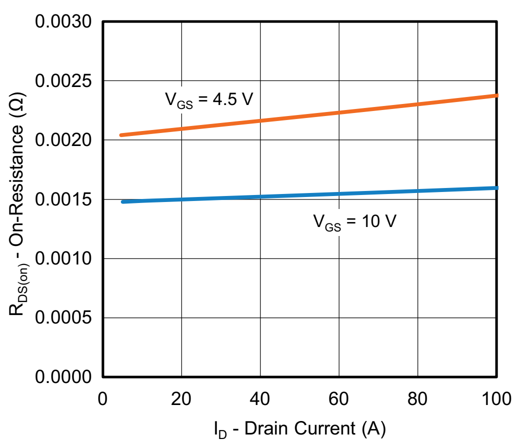
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



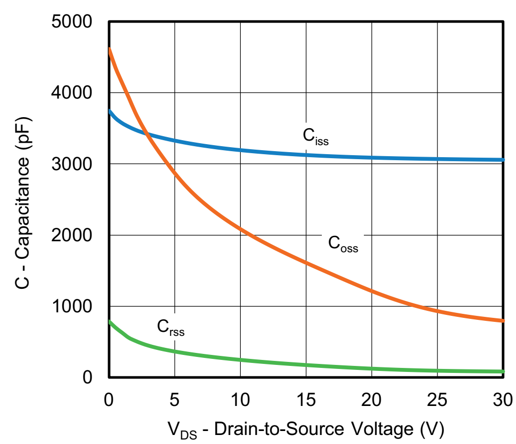
Output Characteristics



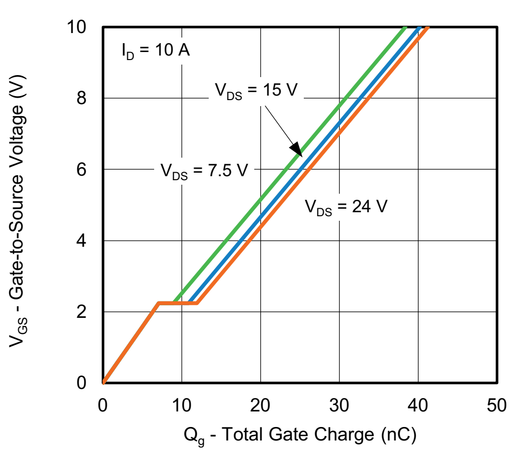
Transfer Characteristics



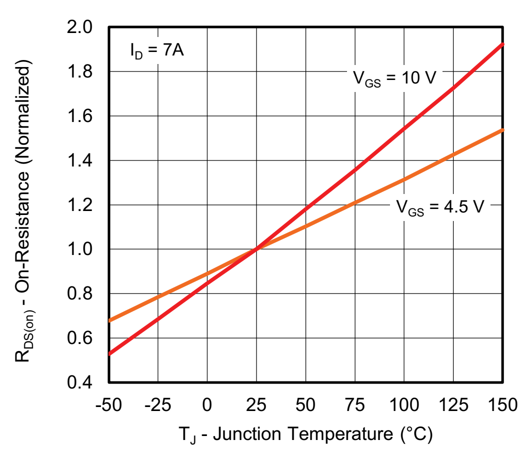
On-Resistance vs. Drain Current



Capacitance

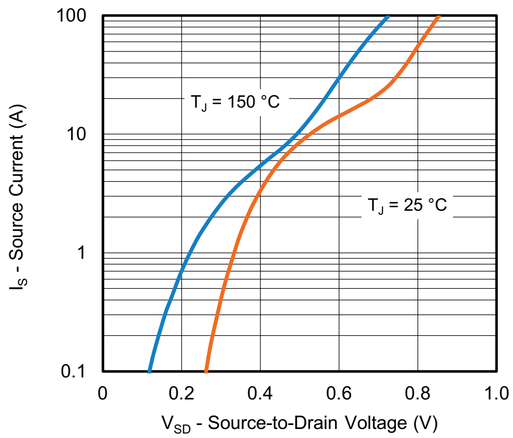


Gate Charge

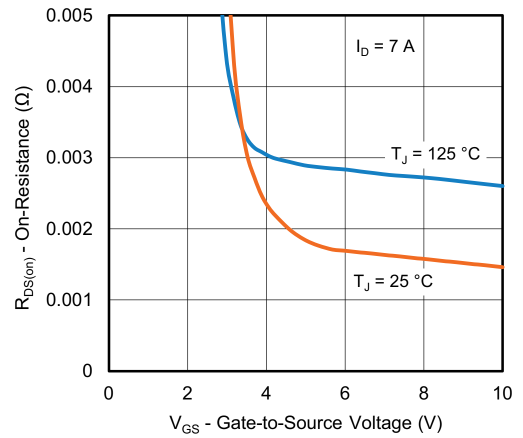


On-Resistance vs. Junction Temperature

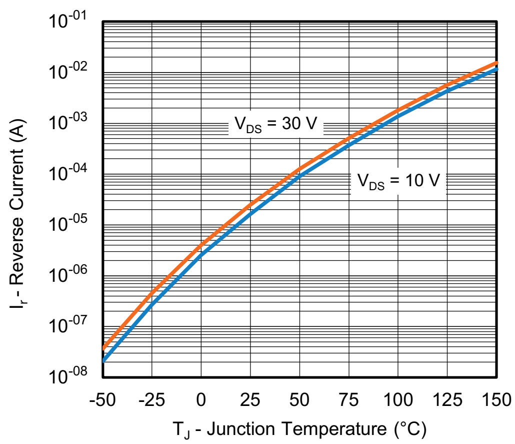
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



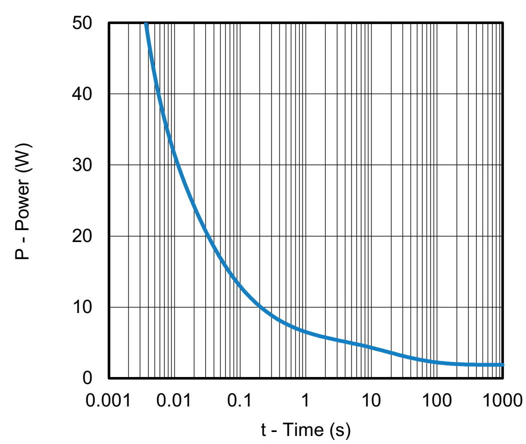
Source-Drain Diode Forward Voltage



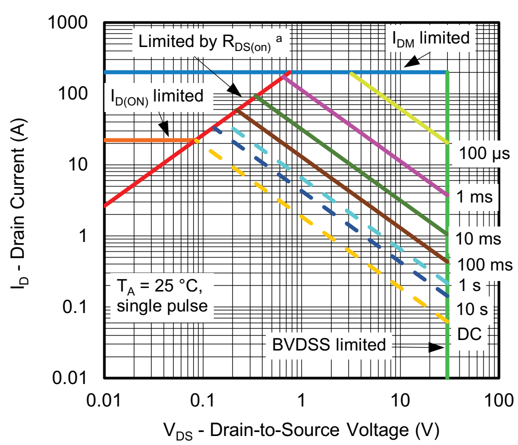
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



Single Pulse Power, Junction-to-Ambient

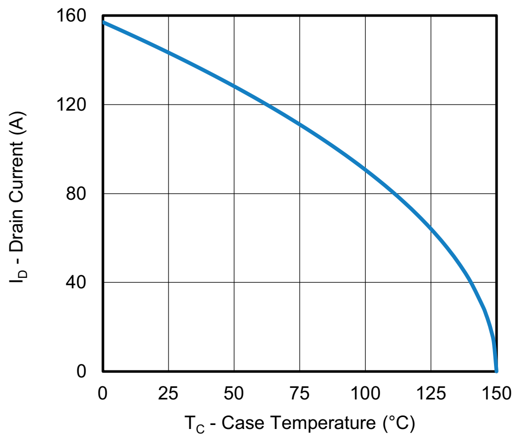


Safe Operating Area, Junction-to-Ambient

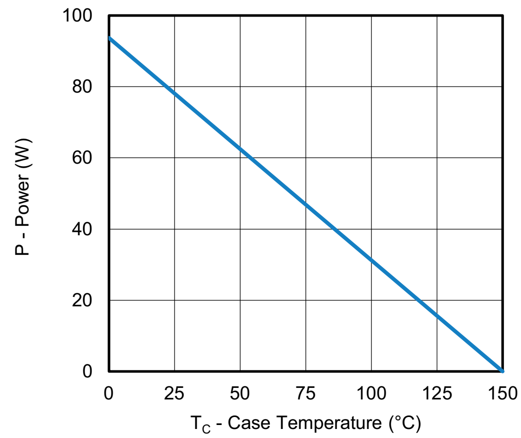
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

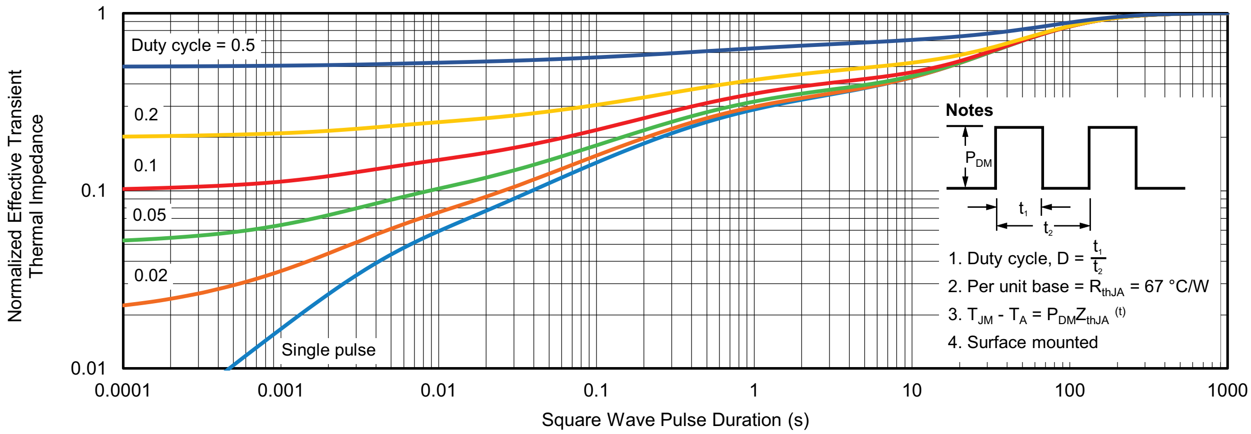


Power, Junction-to-Case

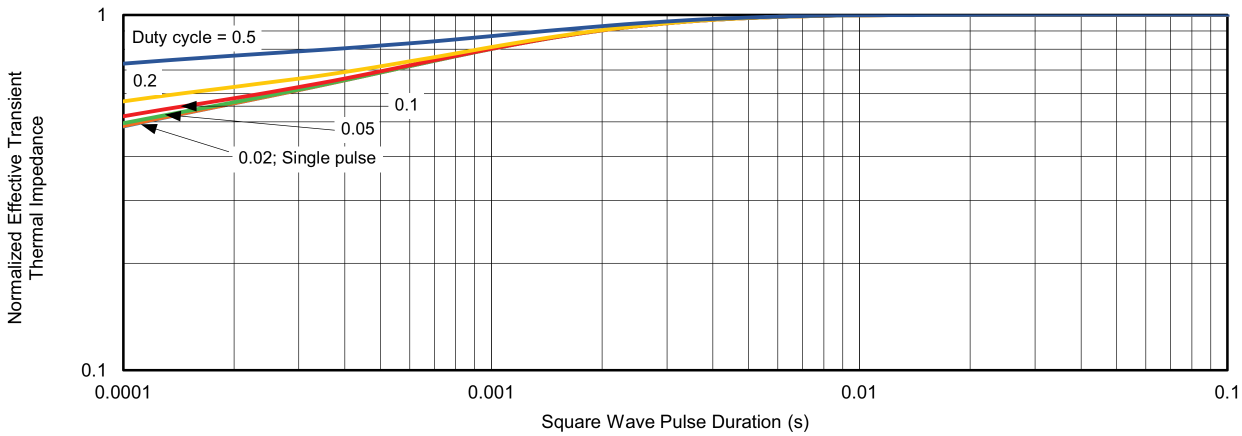
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

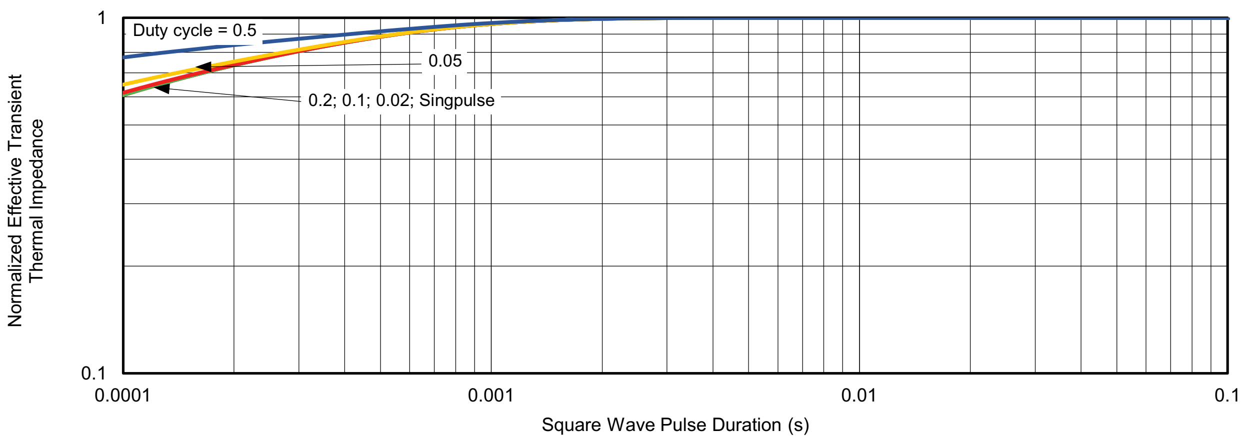
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



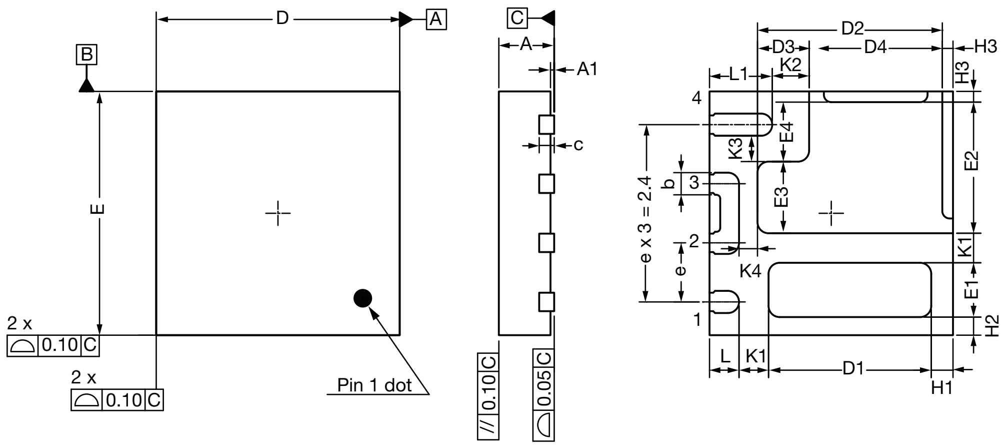
Normalized Thermal Transient Impedance, Junction-to-Case (Source)



Normalized Thermal Transient Impedance, Junction-to-Case (Drain)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77233.

PowerPAIR® 3 x 3F Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
c		0.20 ref.			0.008 ref.	
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.20	2.25	0.085	0.087	0.089
D2	2.45	2.50	2.55	0.096	0.098	0.100
D3	0.65	0.70	0.75	0.026	0.028	0.030
D4	1.75	1.80	1.85	0.069	0.071	0.073
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	0.69	0.74	0.79	0.027	0.029	0.031
E2	1.73	1.78	1.93	0.068	0.070	0.072
E3	0.92	0.97	1.02	0.036	0.038	0.040
E4	0.76	0.81	0.86	0.030	0.032	0.034
e		0.80 BSC			0.031 BSC	
K1		0.40 ref.			0.016 ref.	
K2		0.50 ref.			0.020 ref.	
K3		0.35 ref.			0.014 ref.	
K4		0.25 ref.			0.010 ref.	
H1		0.30 ref.			0.012 ref.	
H2		0.25 ref.			0.010 ref.	
H3		0.15 ref.			0.006 ref.	
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.80	0.85	0.90	0.031	0.033	0.035
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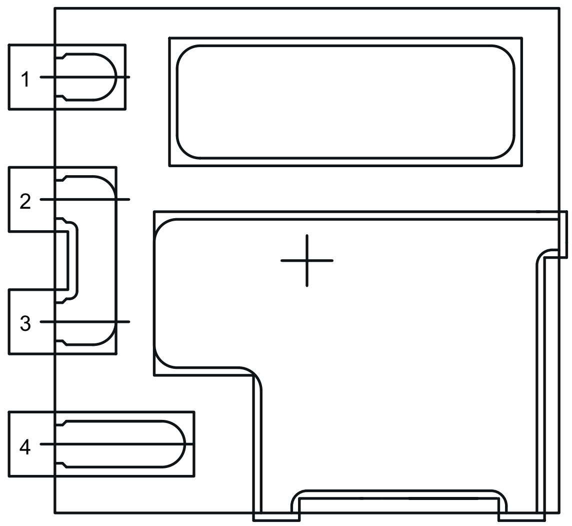
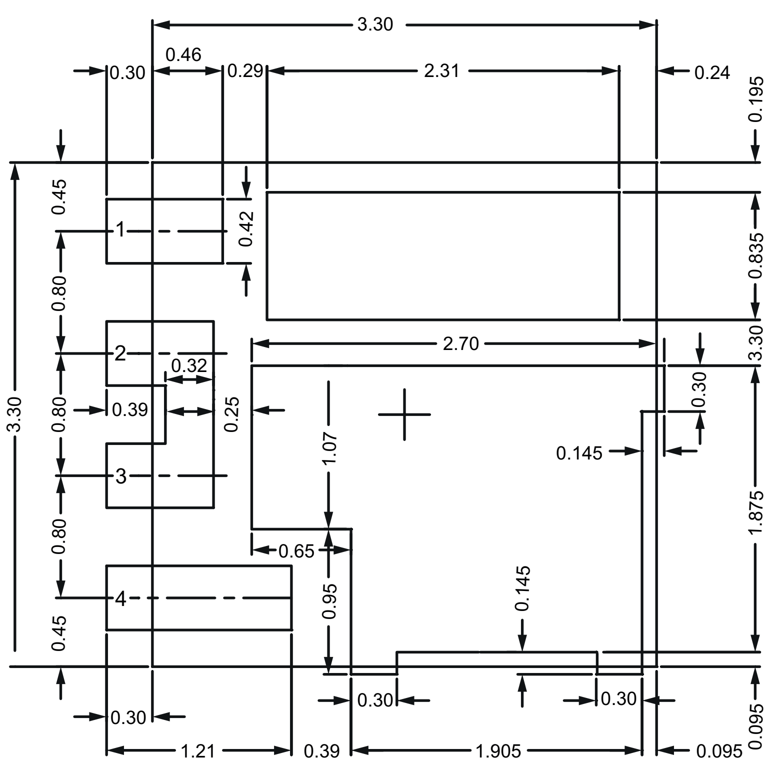
Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M - 1994
(3) N is the number of terminals; Nd is the numer of terminals in X-direction; Ne is the number of terminals in Y-direction
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin # 1 identifier must be existed on the top surface of the package by using identation mark or other feature of package body
(6) Exact shape and size of this features is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

Recommended Land Pattern for PowerPAIR® 3.3 x 3.3F BWL





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