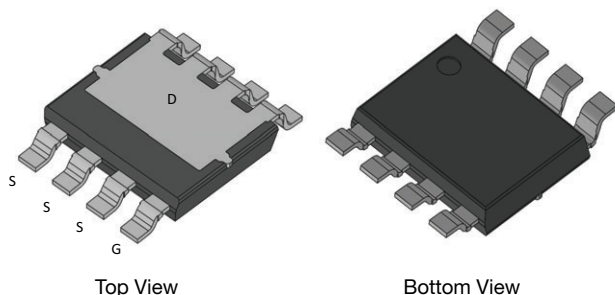


Automotive N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L Reverse Single



Top View

Bottom View

PRODUCT SUMMARY

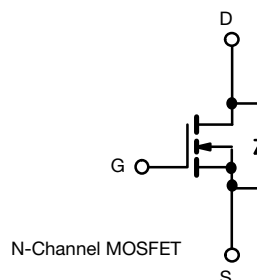
V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0014
I_D (A)	430
Configuration	Single
Package	PowerPAK 8 x 8L Reverse

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.9 mm height
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Continuous source current (diode conduction)	I_S	450	
Pulsed drain current ^a	I_{DM}	1200	
Single pulse avalanche current	I_{AS}	65	mJ
Single pulse avalanche energy	E_{AS}	211	
Maximum power dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 125$ °C	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	40	°C/W
Junction-to-case (drain)	R_{thJC}	0.25	

Notes

- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

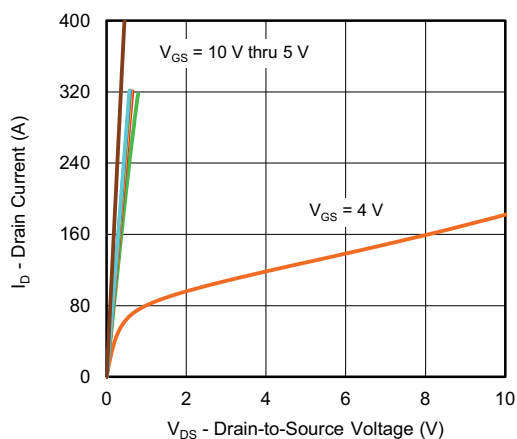
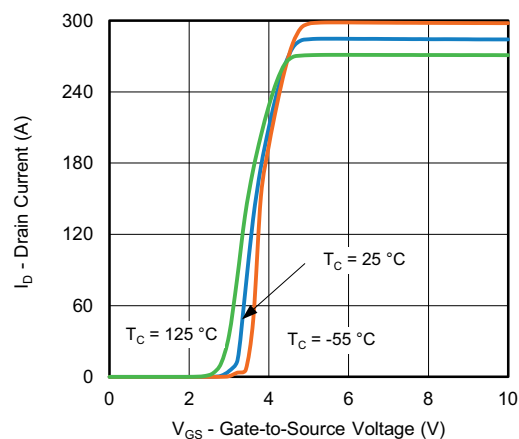
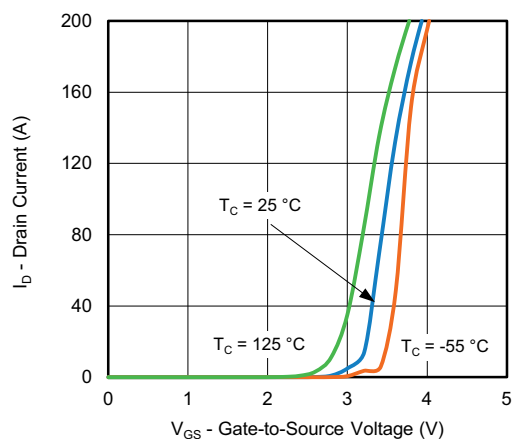
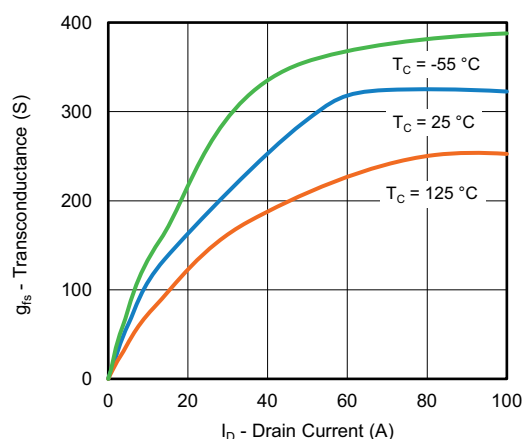
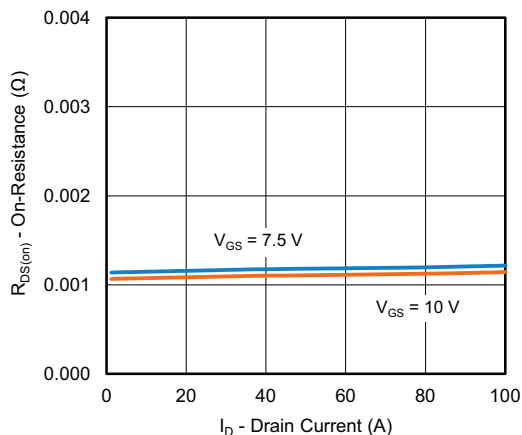
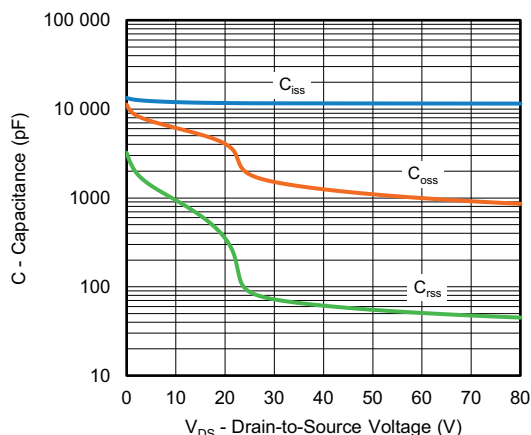


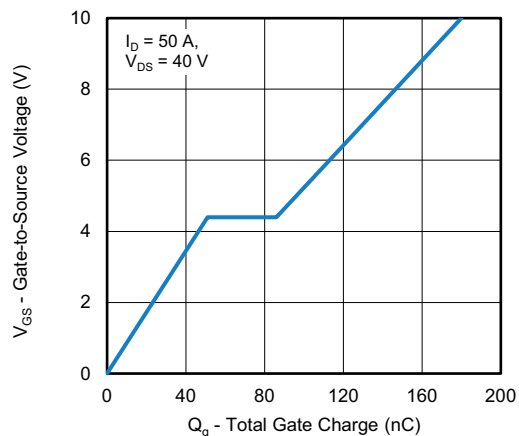
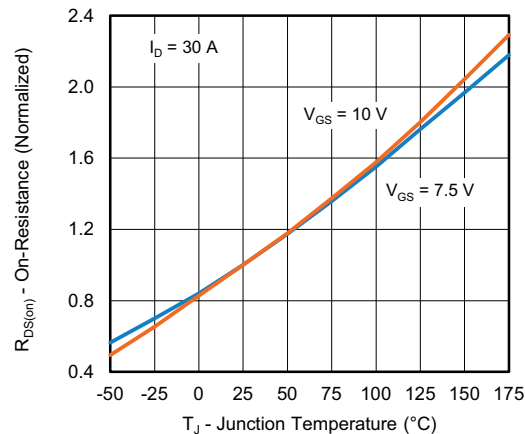
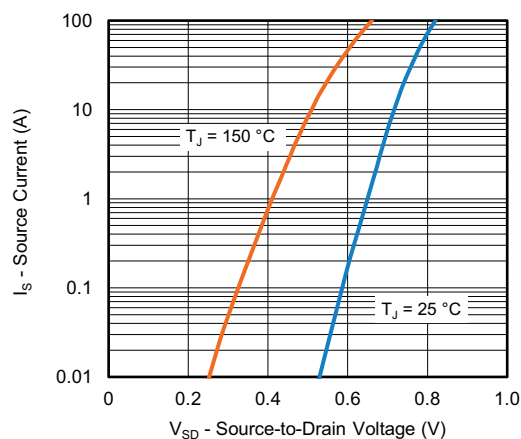
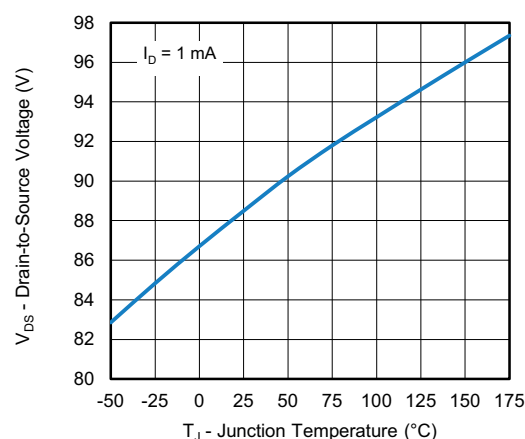
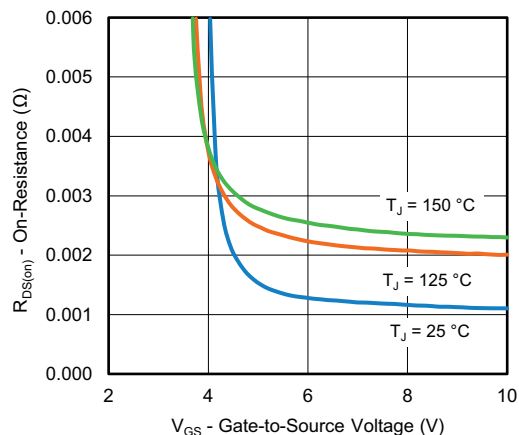
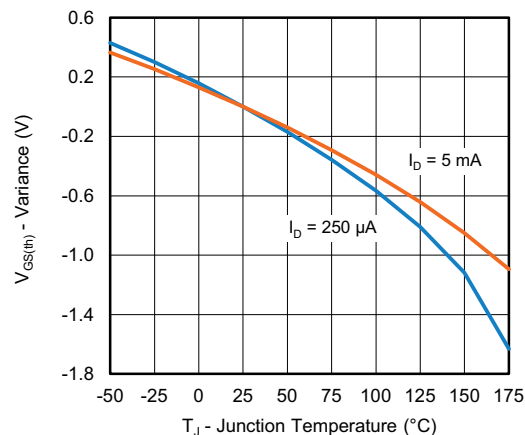
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	3	3.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 80 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	500	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	50	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A	-	0.0012	0.0014	Ω
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.00281	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0037	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 15 A		-	82	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	11 435	16 009	pF
Output capacitance	C _{oss}			-	1896	2655	
Reverse transfer capacitance	C _{rss}			-	92	129	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 40 V, I _D = 10 A	-	183	240	nC
Gate-source charge ^c	Q _{gs}			-	47	-	
Gate-drain charge ^c	Q _{gd}			-	85	-	
Gate resistance	R _g	f = 1 MHz		0.7	1.3	2	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 40 V, R _L = 0.8 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1 Ω		-	21	28	ns
Rise time ^c	t _r			-	80	105	
Turn-off delay time ^c	t _{d(off)}			-	65	85	
Fall time ^c	t _f			-	20	28	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	1100	A
Forward voltage	V _{SD}	I _F = 40 A, V _{GS} = 0 V		-	0.7	1.2	V

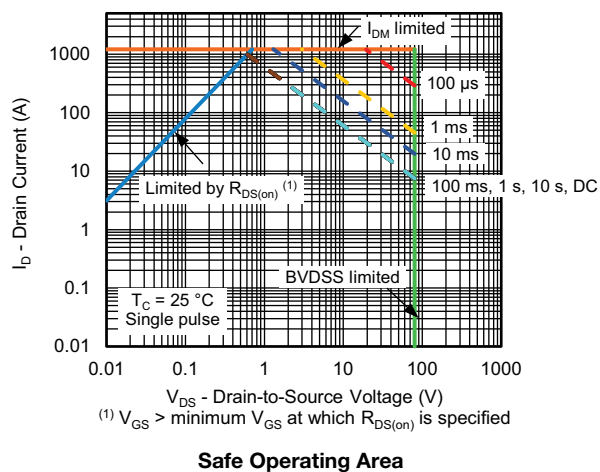
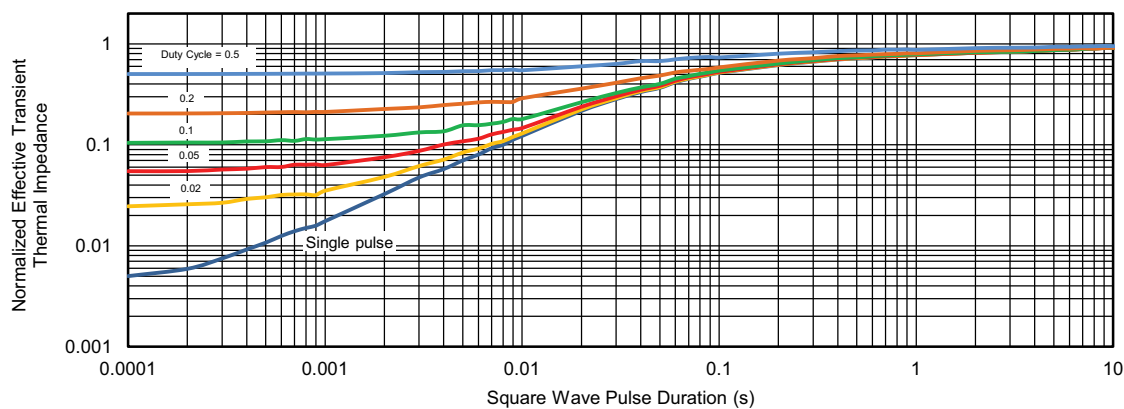
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

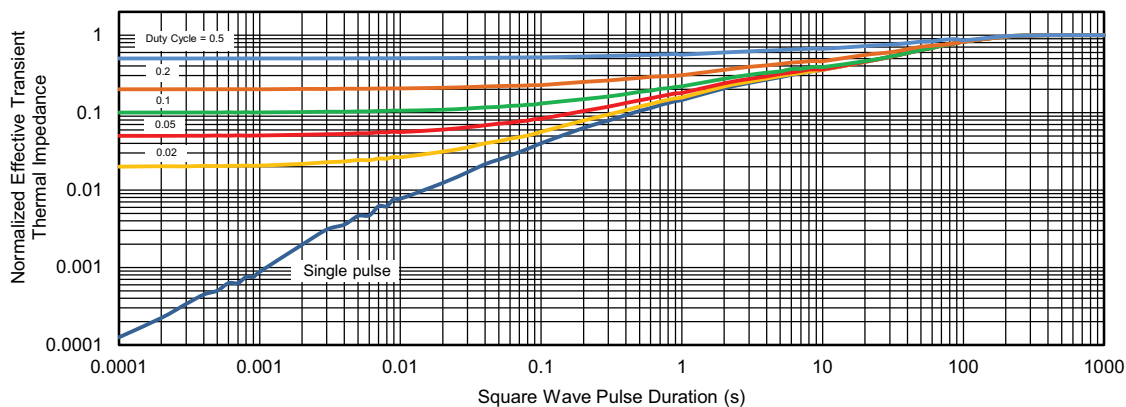
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

Drain Source Breakdown vs. Junction Temperature

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)


Normalized Thermal Transient Impedance, Junction-to-Case



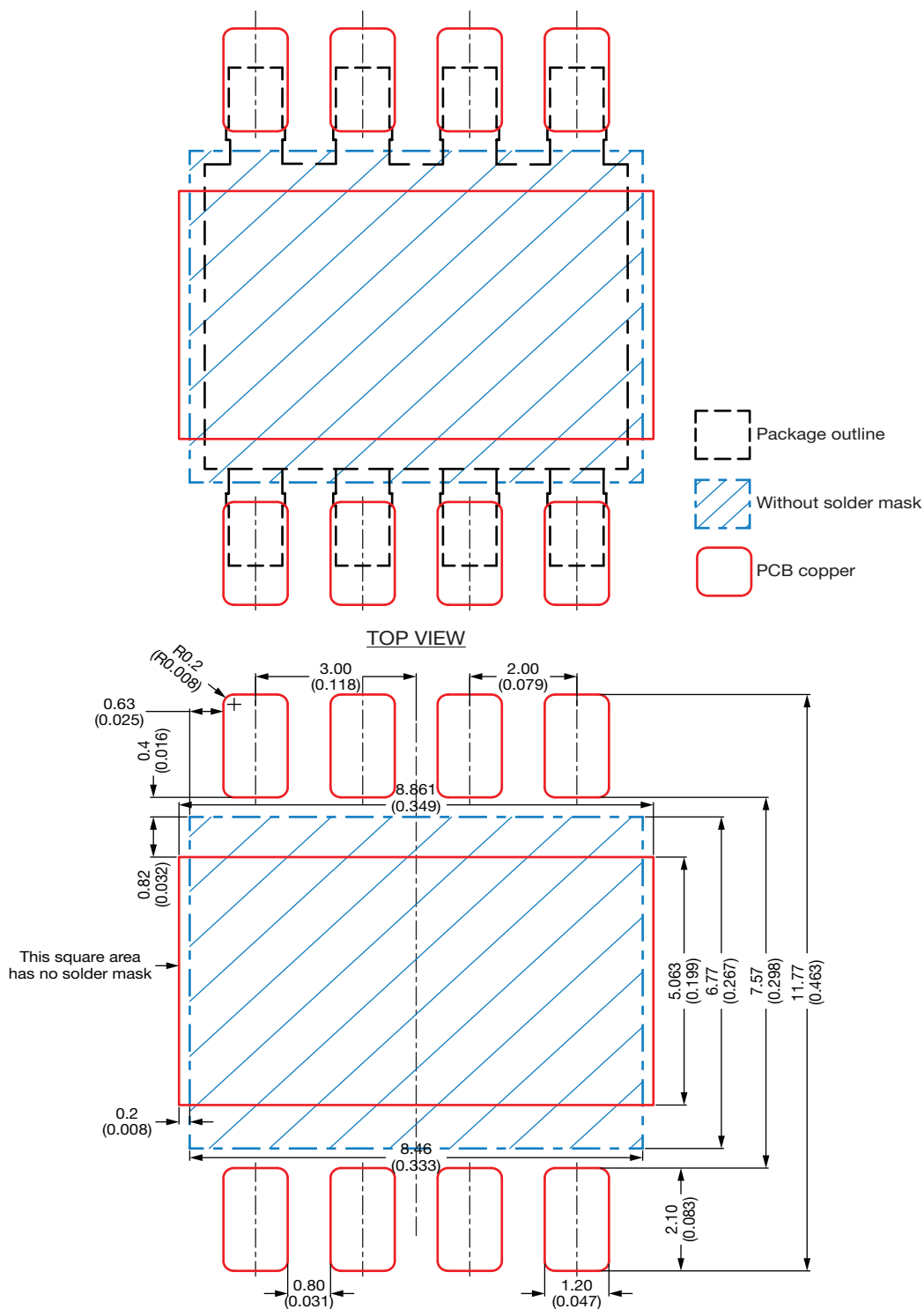
THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71298.

Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023

DWG: 3002



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