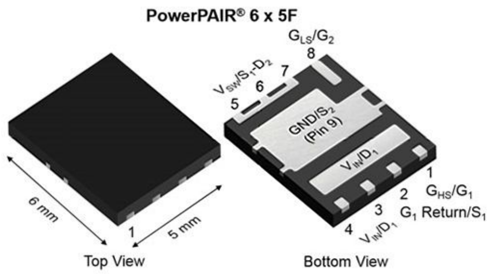
Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode



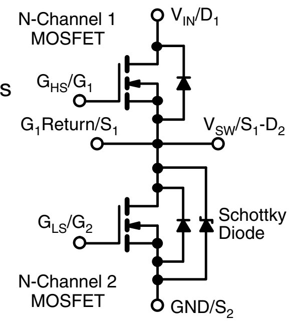
FEATURES

- TrenchFET® Gen IV power MOSFET
- SkyFET® low-side MOSFET with integrated Schottky
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V_{DS} (V)	30	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00400	0.00125
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00670	0.00175
Q_g typ. (nC)	7	29.3
I_D (A) [a]	40	60
Configuration	Dual	

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5F
Lead (Pb)-free and halogen-free	SiZF916DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT
Drain-source voltage		V_{DS}	30	30	V
Gate-source voltage		V_{GS}	+20, -16	+16, -12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	40 [a]	60 [a]	A
	T_C = 70 °C		40 [a]	60 [a]	
	T_A = 25 °C		23 [b, c]	45 [b, c]	
	T_A = 70 °C		18.4 [b, c]	36 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	130	110	
Continuous source-drain diode current	T_C = 25 °C	I_S	22	60 [a]	
	T_A = 25 °C		2.8 [b, c]	7 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	15	25	
Single pulse avalanche energy		E_{AS}	11.3	31	mJ
Maximum power dissipation	T_C = 25 °C	P_D	26.6	60	W
	T_C = 70 °C		17	38	
	T_A = 25 °C		3.4 [b, c]	4 [b, c]	
	T_A = 70 °C		2.2 [b, c]	2.6 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	30	37	25	31	°C/W
Maximum junction-to-case (source)	Steady state	R_{thJC}	3.8	4.7	1.7	1.7	

Notes

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 77 °C/W for channel-1 and 68 °C/W for channel-2

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	Ch-1	30	-	-	V
			Ch-2	30	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	1.1	-	2.4	
			Ch-2	1.1	-	2.2	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V, -16 V	Ch-1	-	-	± 100	nA
		V_{DS} = 0 V, V_{GS} = +16 V, -12 V	Ch-2	-	-	± 100	
Zero Gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	Ch-1	-	-	1	µA
			Ch-2	-	35	350	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	Ch-1	-	-	5	
			Ch-2	-	250	3000	
On-state drain current [b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	Ch-1	20	-	-	A
			Ch-2	20	-	-	
Drain-source on-state resistance [b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	Ch-1	-	0.00290	0.00400	Ω
		V_{GS} = 10 V, I_D = 10 A	Ch-2	-	0.00090	0.00125	
		V_{GS} = 4.5 V, I_D = 5 A	Ch-1	-	0.00470	0.00680	
		V_{GS} = 4.5 V, I_D = 5 A	Ch-2	-	0.00125	0.00175	
Forward transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 20 A	Ch-1	-	53	-	S
		V_{DS} = 10 V, I_D = 20 A	Ch-2		91	-	
Dynamic [a]							
Input capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	-	1060	-	pF
			Ch-2	-	4320	-	
Output capacitance	C_{oss}		Ch-1	-	600	-	
			Ch-2	-	1840	-	
Reverse transfer capacitance	C_{rss}		Ch-1	-	45	-	
			Ch-2	-	260	-	
C_{rss}/C_{iss} ratio			Ch-1	-	0.042	0.085	
			Ch-2		0.060	0.120	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	Ch-1	-	14.6	22	nC
			Ch-2	-	62	95	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	Ch-1		7	11	
			Ch-2	-	29.3	45	
Gate-source charge	Q_{gs}		Ch-1	-	3	-	
			Ch-2	-	10.2	-	
Gate-drain charge	Q_{gd}		Ch-1	-	1.5	-	
			Ch-2	-	5.2	-	
Output charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	Ch-1	-	14	-	
			Ch-2	-	46	-	
Gate resistance	R_g	f = 1 MHz	Ch-1	0.2	1	2	Ω
			Ch-2	0.1	0.41	0.82	

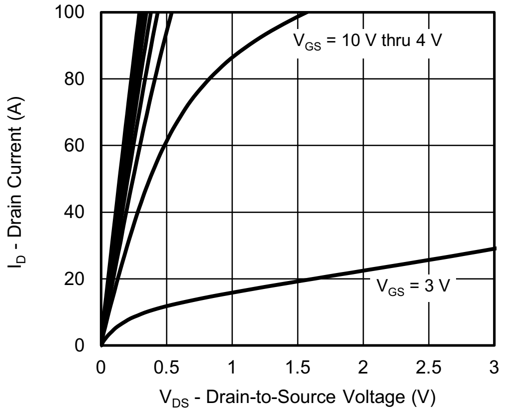
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Dynamic [a]							
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 4.5 V, R_g = 1 Ω	Ch-1	-	17	35	ns
			Ch-2	-	30	60	
Rise time	t_r		Ch-1	-	45	90	
			Ch-2	-	60	120	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	20	40	
			Ch-2	-	45	90	
Fall time	t_f		Ch-1	-	10	20	
			Ch-2	-	20	40	
Turn-on delay time	$t_{d(on)}$	Channel-1 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω Channel-2 V_{DD} = 15 V, R_L = 3 Ω $I_D \cong$ 5 A, V_{GEN} = 10 V, R_g = 1 Ω	Ch-1	-	10	20	
			Ch-2	-	15	30	
Rise time	t_r		Ch-1	-	5	10	
			Ch-2	-	25	50	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	20	40	
			Ch-2	-	40	80	
Fall time	t_f		Ch-1	-	5	10	
			Ch-2	-	10	20	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	T_C = 25 °C	Ch-1	-	-	22	A
			Ch-2	-	-	60	
Pulse diode forward current [a]	I_{SM}		Ch-1	-	-	130	
			Ch-2	-	-	110	
Body diode voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V	Ch-1	-	0.8	1.2	V
		I_S = 3 A, V_{GS} = 0 V	Ch-2	-	0.38	0.58	
Body diode reverse recovery time	t_{rr}	Channel-1 I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C Channel-2 I_F = 10 A, di/dt = 100 A/µs, T_J = 25 °C	Ch-1	-	32	70	ns
			Ch-2	-	55	110	
Body diode reverse recovery charge	Q_{rr}		Ch-1	-	24	50	nC
			Ch-2	-	72	150	
Reverse recovery fall time	t_a		Ch-1	-	18	-	ns
			Ch-2	-	27	-	
Reverse recovery rise time	t_b		Ch-1	-	14	-	
			Ch-2	-	28	-	

Notes

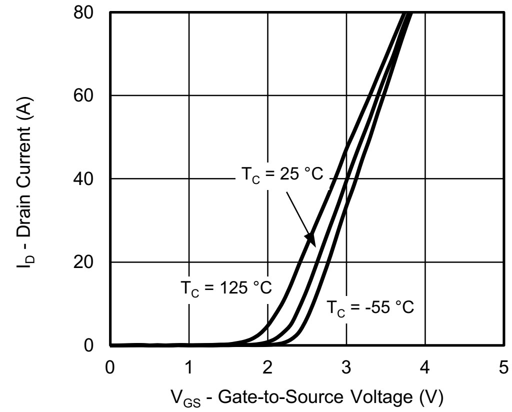
a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

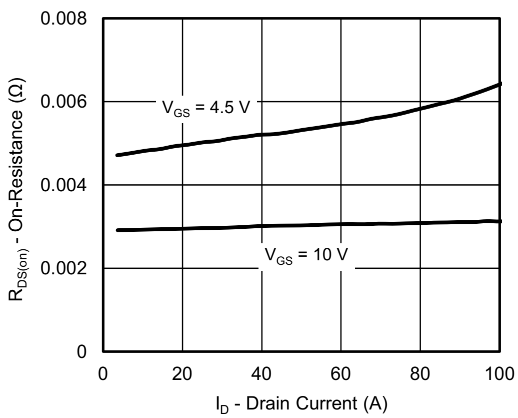
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



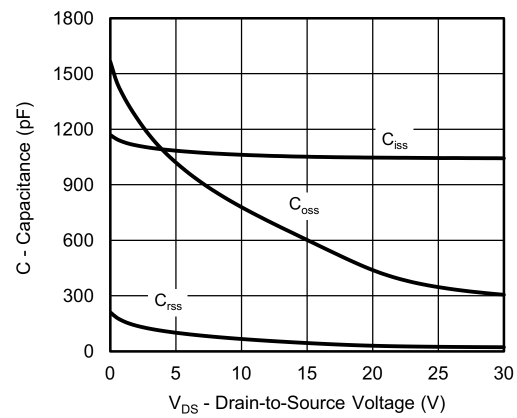
Output Characteristics



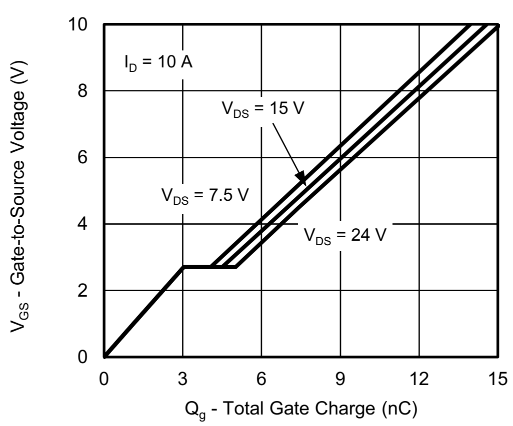
Transfer Characteristics



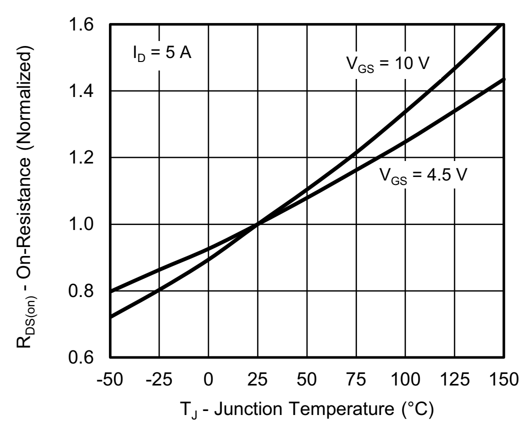
On-Resistance vs. Drain Current



Capacitance

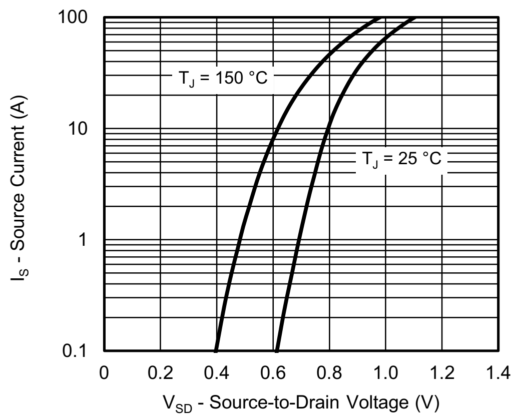


Gate Charge

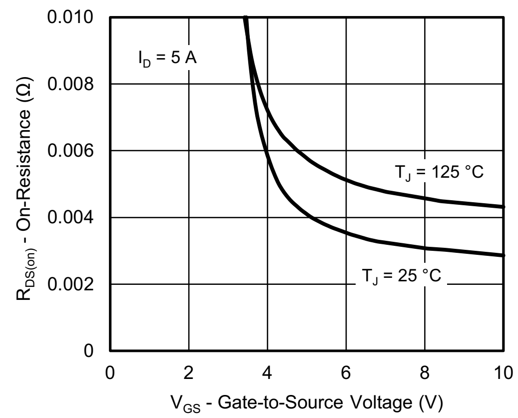


On-Resistance vs. Junction Temperature

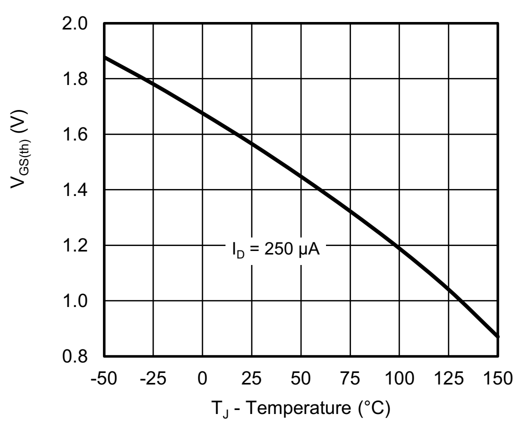
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



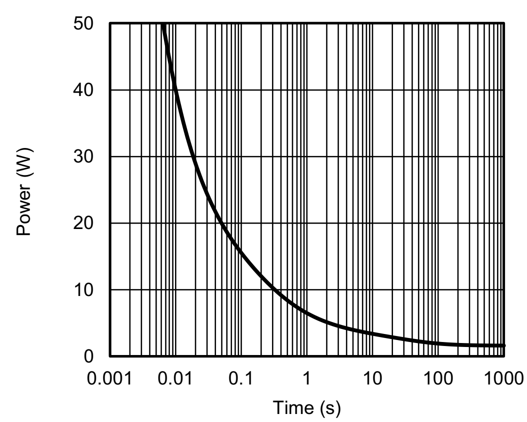
Source-Drain Diode Forward Voltage



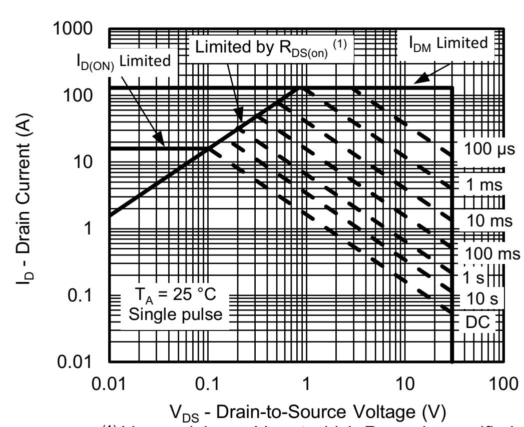
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



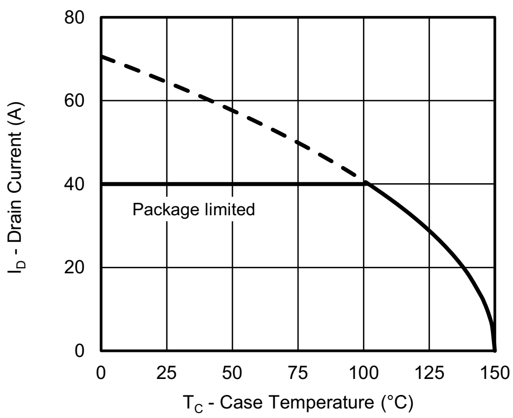
Single Pulse Power, Junction-to-Ambient



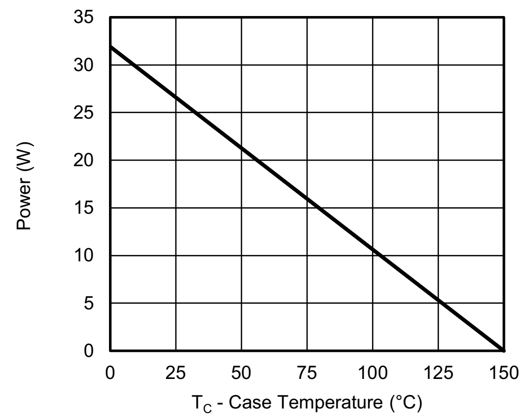
(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

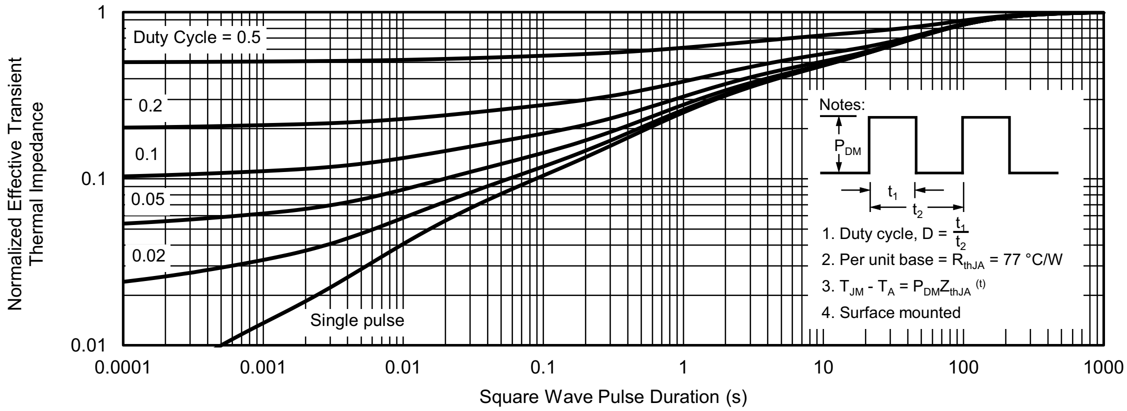


Power, Junction-to-Case

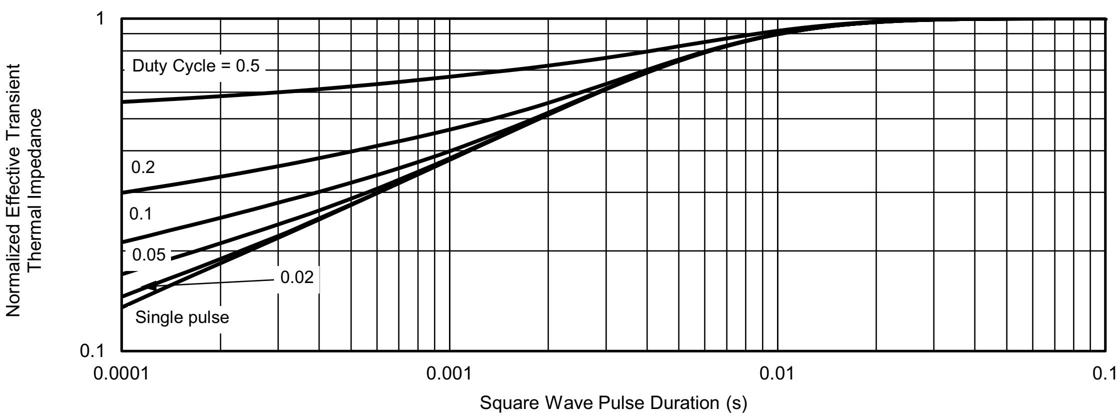
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

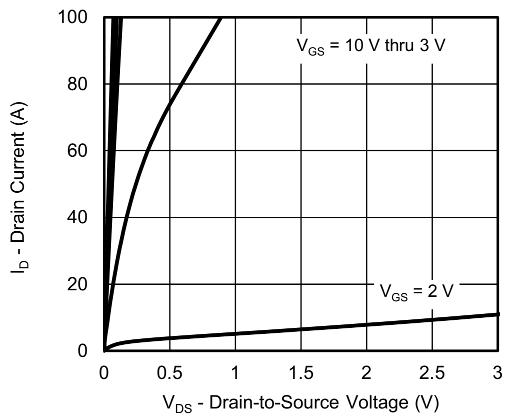


Normalized Thermal Transient Impedance, Junction-to-Ambient

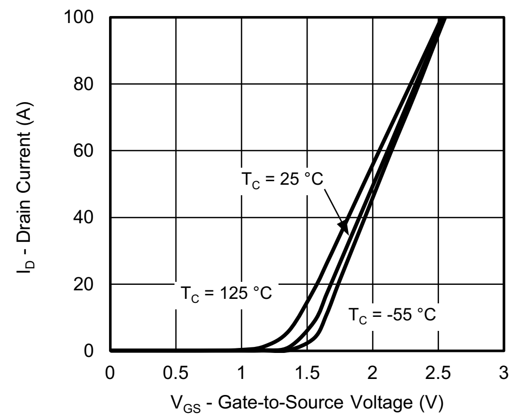


Normalized Thermal Transient Impedance, Junction-to-Case

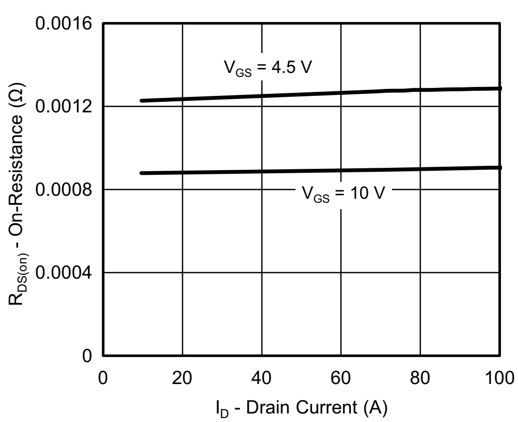
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



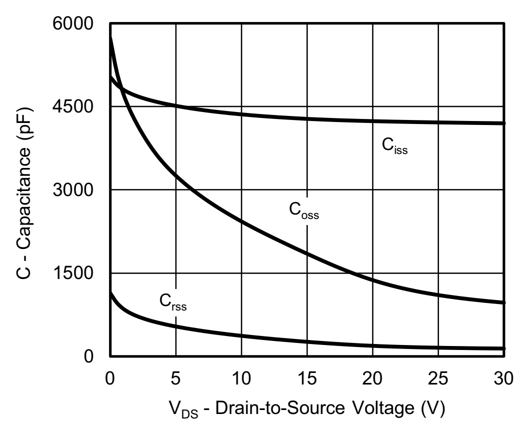
Output Characteristics



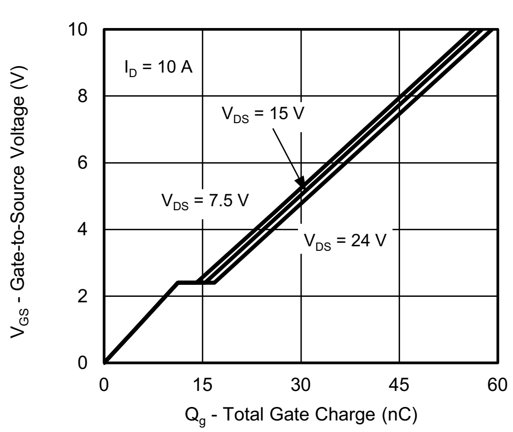
Transfer Characteristics



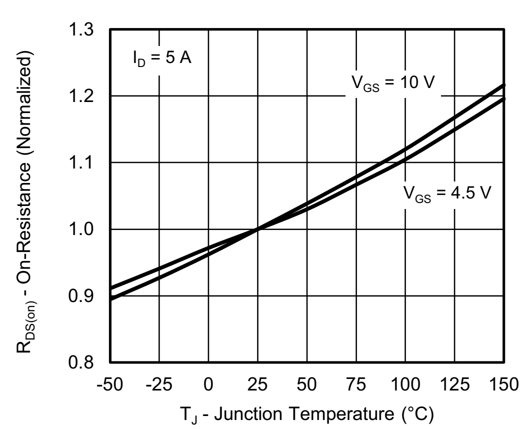
On-Resistance vs. Drain Current



Capacitance

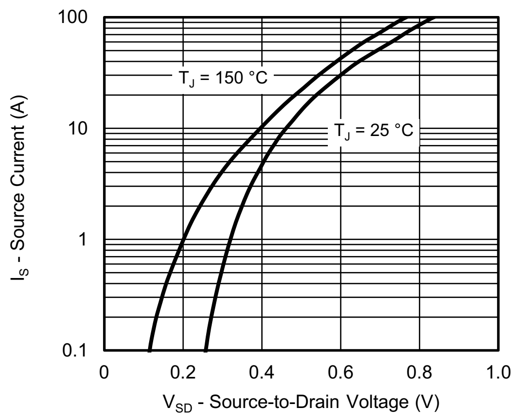


Gate Charge

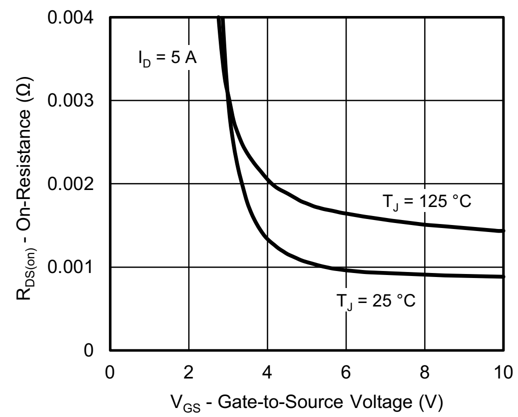


On-Resistance vs. Junction Temperature

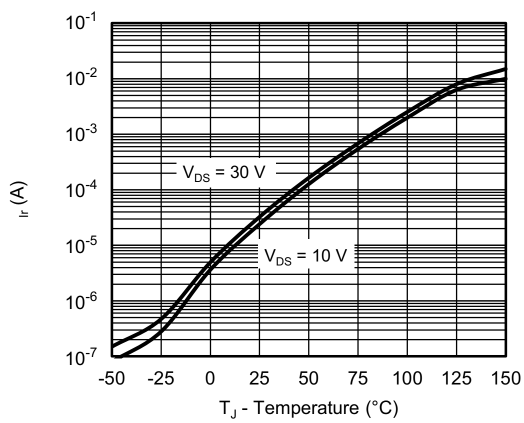
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



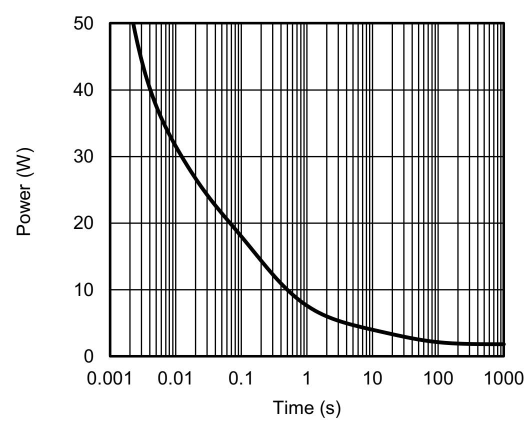
Source-Drain Diode Forward Voltage



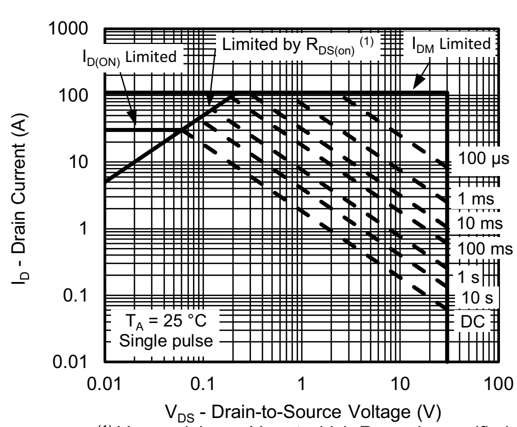
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



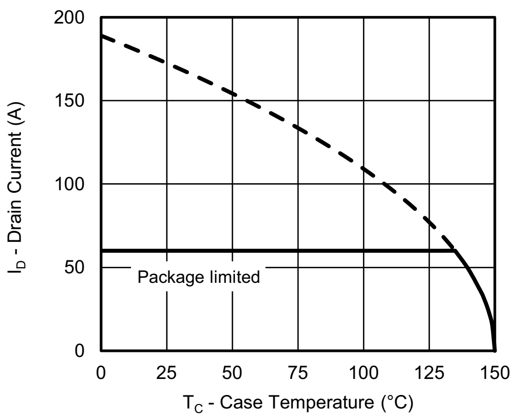
Single Pulse Power, Junction-to-Ambient



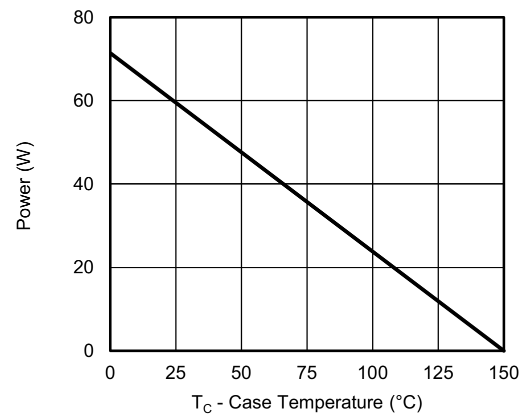
(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

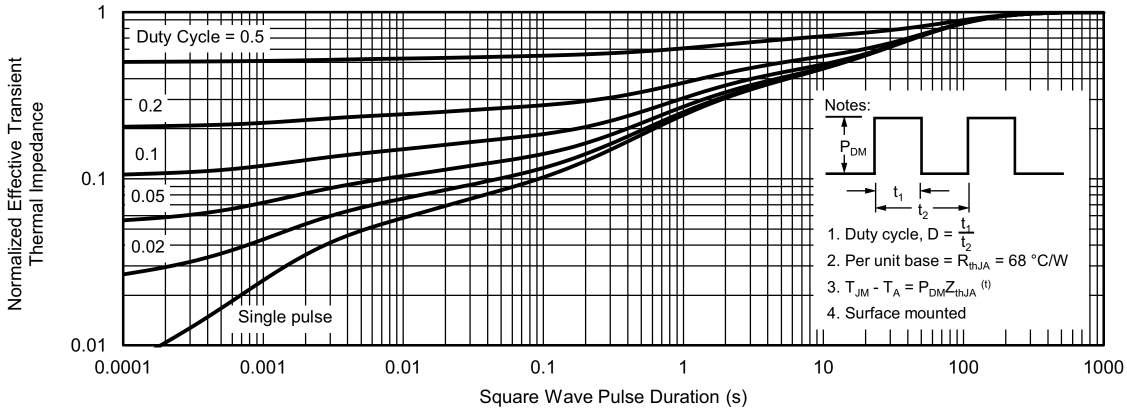


Power, Junction-to-Case

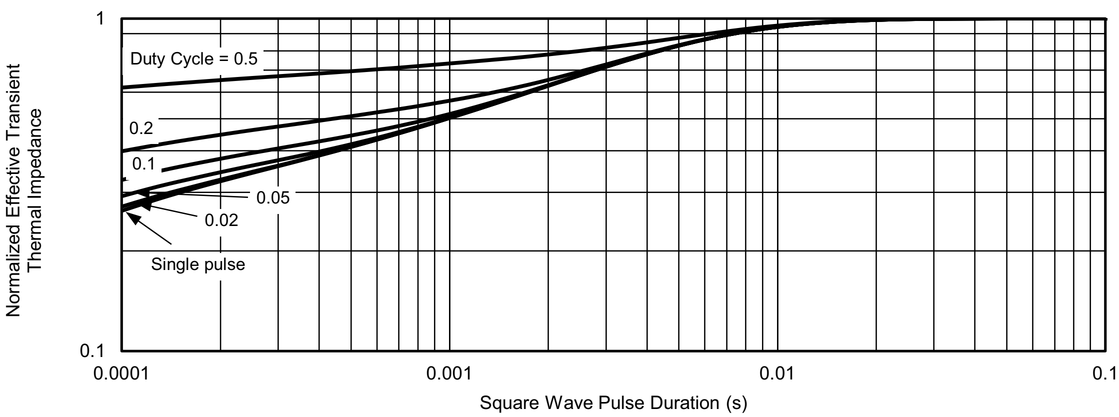
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



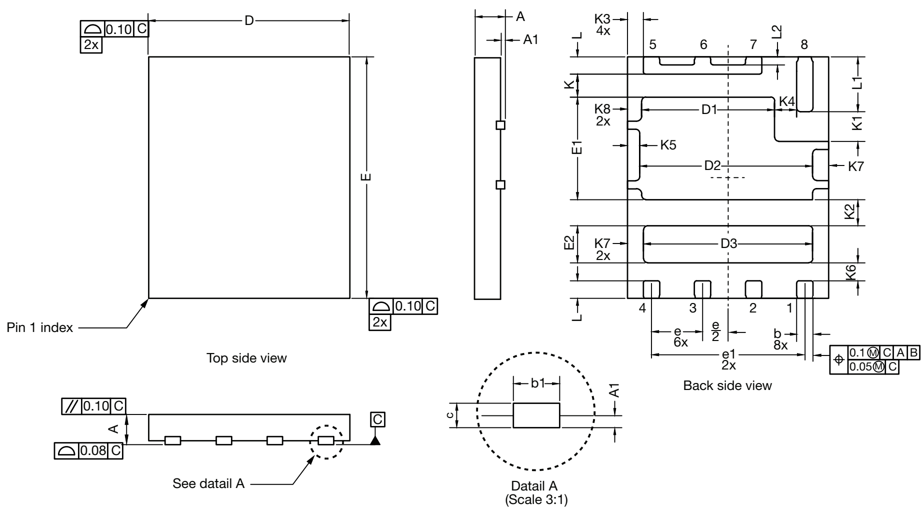
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75698.

PowerPAIR® 6 x 5 F Case Outline



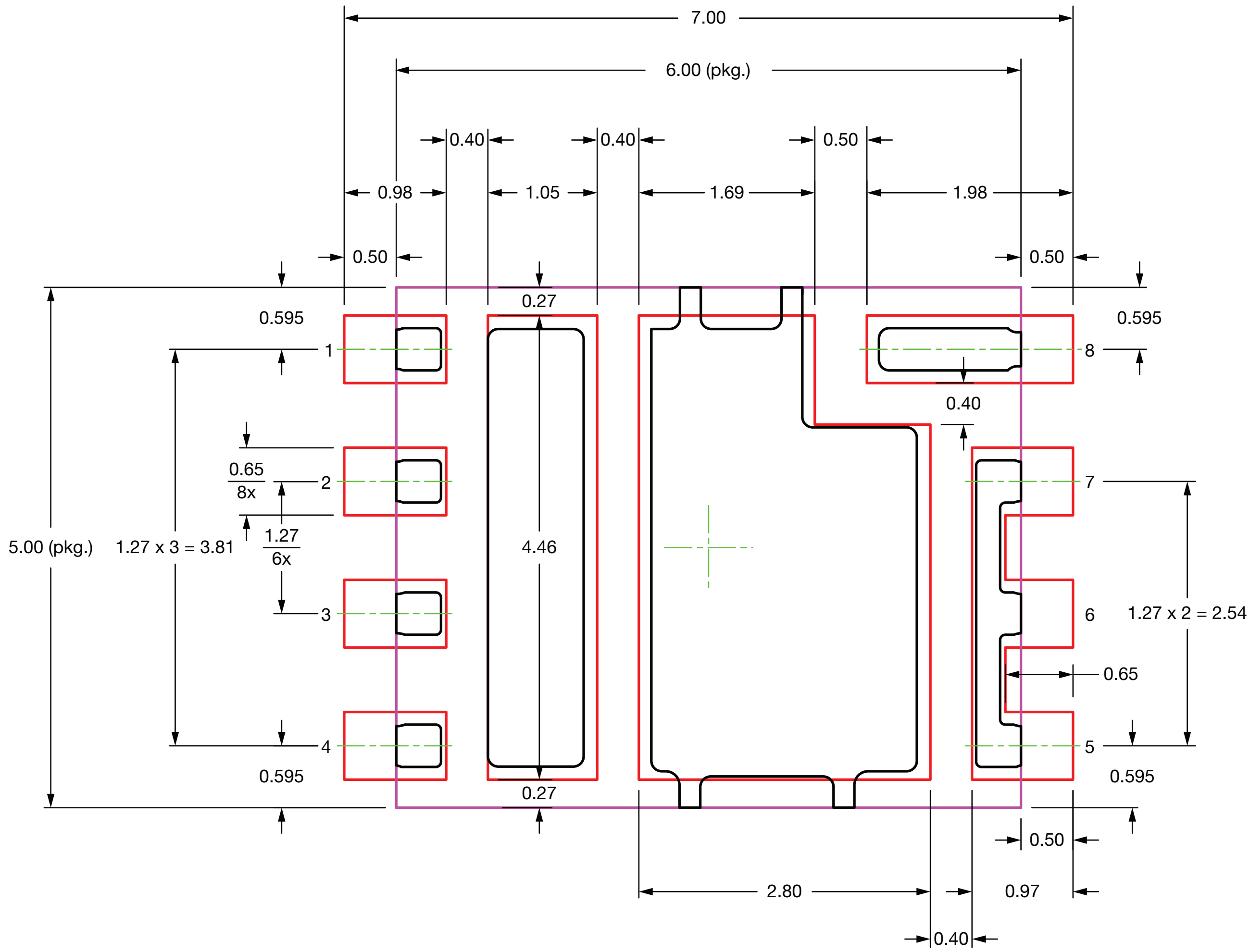
DIMENSION	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.10	0.000	-	0.004
b	0.35	0.41	0.46	0.014	0.016	0.018
b1	0.38 ref.			0.015 ref.		
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.26	3.31	3.36	0.128	0.130	0.132
D2	4.20	4.30	4.40	0.165	0.169	0.173
D3	4.15	4.20	4.25	0.163	0.165	0.167
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	2.50	2.55	2.60	0.098	0.100	0.102
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
e1	3.81 BSC			0.150 BSC		
K	0.52	0.57	0.62	0.020	0.022	0.024
K1	0.69	0.74	0.79	0.027	0.029	0.031
K2	0.60	0.65	0.70	0.024	0.026	0.028
K3	0.39 BSC			0.015 BSC		
K4	0.50	0.55	0.60	0.020	0.022	0.024
K5	0.25	0.30	0.35	0.010	0.012	0.014
K6	0.40	0.45	0.50	0.016	0.018	0.020
K7	0.35	0.40	0.45	0.014	0.016	0.018
K8	0.30	0.35	0.40	0.012	0.014	0.016
L	0.33	0.43	0.53	0.013	0.017	0.021
L1	1.31	1.36	1.41	0.052	0.054	0.056
L2	0.20 ref.			0.008 ref.		

ECN: T20-0097-Rev. C, 25-Feb-2020
DWG: 6043

Note

- Millimeters will govern

Recommended Minimum PADs for PowerPAIR® 6 x 5F



Component for PowerPair 6 x 5F

Land Pattern for PowerPair 6 x 5F

Note

- Dimensions in millimeters

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