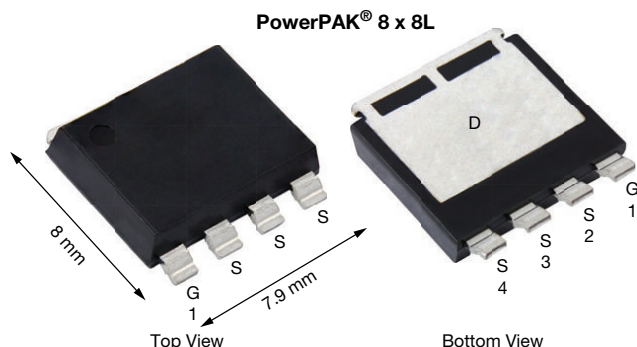


# N-Channel 40 V (D-S) 175 °C MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



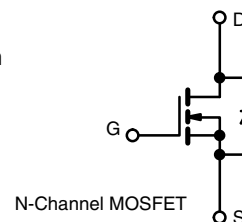
PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00065
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.00094
$Q_g$ typ. (nC)	75
$I_D$ (A) <sup>a</sup>	450
Configuration	Single

## FEATURES

- TrenchFET® Gen IV power MOSFET
- Fully lead (Pb)-free device
- Very low  $R_{DS} \times Q_g$  figure of merit (FOM)
- 50 % smaller footprint than D<sup>2</sup>PAK (TO-263)
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



ORDERING INFORMATION	
Package	PowerPAK® 8 x 8L
Lead (Pb)-free and halogen-free	SIJH402E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	40	V	
Gate-source voltage	$V_{GS}$	+20, -16		
Continuous drain current ( $T_J = 175$ °C)	$T_C = 25$ °C	450	A	
	$T_C = 70$ °C	376		
	$T_A = 25$ °C	46 <sup>b</sup>		
	$T_A = 70$ °C	38 <sup>b</sup>		
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	800		
Continuous source-drain diode current	$T_C = 25$ °C	240		
	$T_A = 25$ °C	2.4 <sup>b</sup>		
Single pulse avalanche current	$L = 0.1$ mH	73		
Single pulse avalanche energy	$E_{AS}$	269	mJ	
Maximum power dissipation	$T_C = 25$ °C	263	W	
	$T_C = 70$ °C	184		
	$T_A = 25$ °C	2.6 <sup>b</sup>		
	$T_A = 70$ °C	1.8 <sup>b</sup>		
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C	
Soldering recommendations (peak temperature) <sup>c</sup>		260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	Steady state	$R_{thJA}$	42	57	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	0.41	0.57	

### Notes

a.  $T_C = 25$  °C

b. Surface mounted on 1" x 1" FR4 board

c. See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

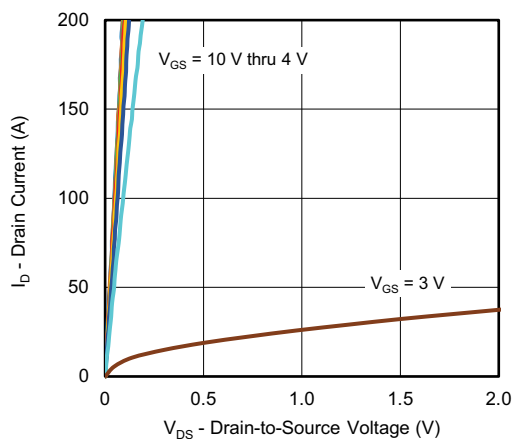
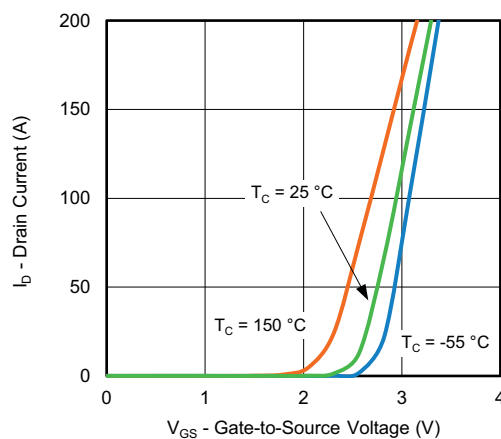
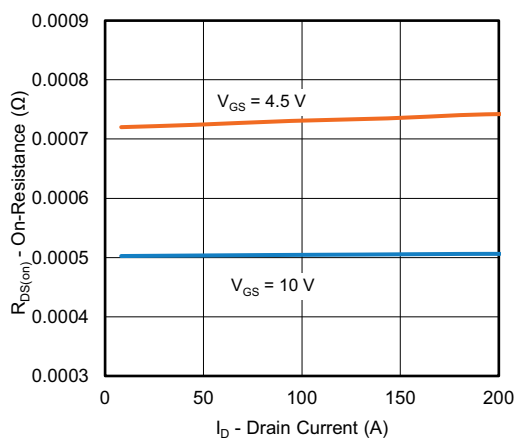
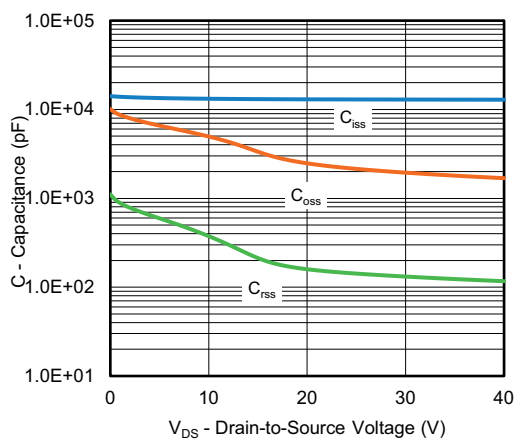
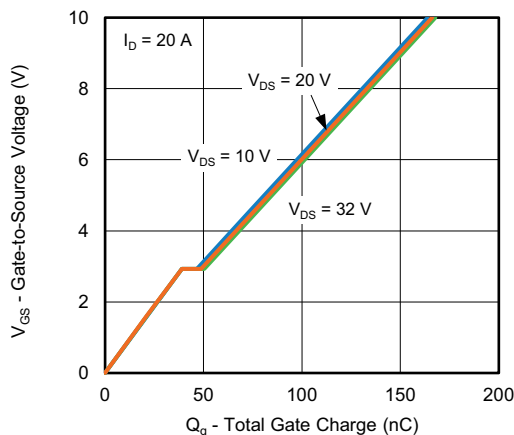
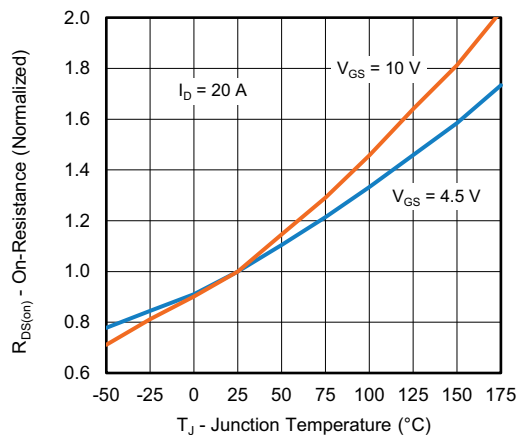


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	25	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-7.1	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250 μA	1.1	-	2.4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +20, -16	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> =0 V	-	-	1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.00050	0.00065	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	0.00071	0.00094	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 40 A	-	215	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	13 105	-	pF
Output capacitance	C <sub>oss</sub>		-	2470	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	165	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	166	250	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	-	75	115	
Gate-drain charge	Q <sub>gd</sub>		-	39	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	22	45	ns
Rise time	t <sub>r</sub>		-	16	30	
Turn-off delay time	t <sub>d(off)</sub>		-	72	145	
Fall time	t <sub>f</sub>		-	12	25	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	72	145	
Rise time	t <sub>r</sub>		-	128	260	
Turn-off delay time	t <sub>d(off)</sub>		-	90	180	
Fall time	t <sub>f</sub>		-	90	180	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	240	A
Pulse diode forward current	I <sub>SM</sub>		-	-	800	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	70	140	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	122	245	nC
Reverse recovery fall time	t <sub>a</sub>		-	41	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	29	-	

**Notes**

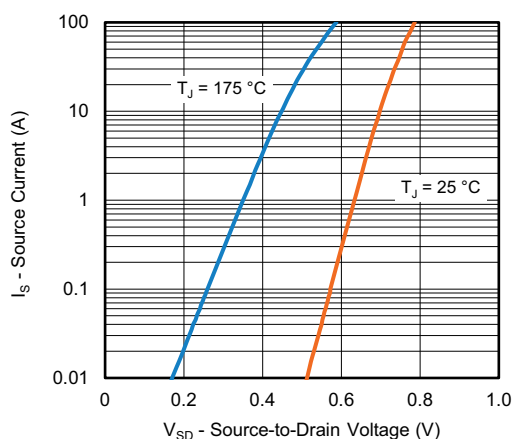
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

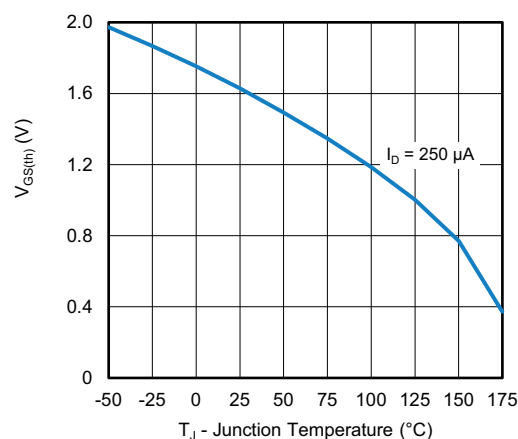
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**



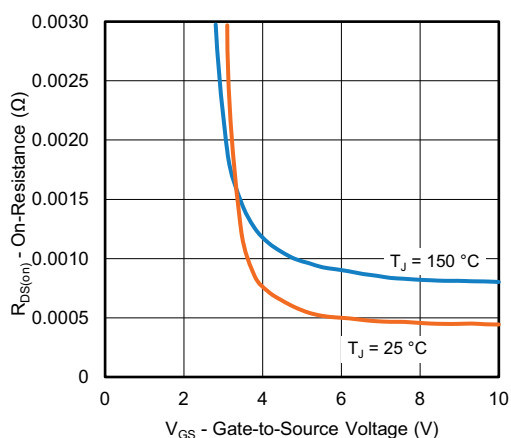
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



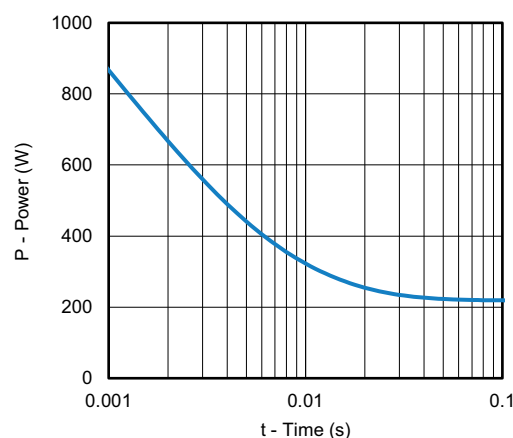
Source-Drain Diode Forward Voltage



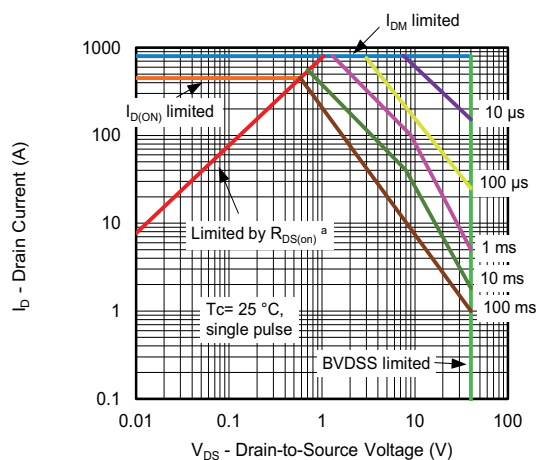
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



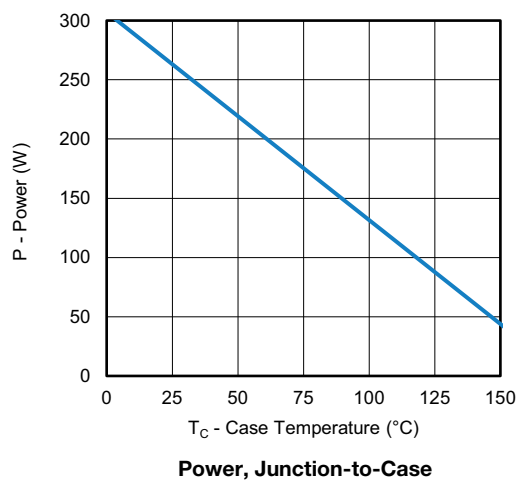
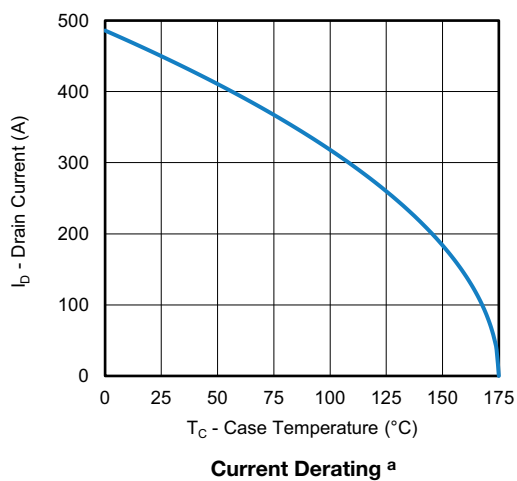
Safe Operating Area, Junction-to-Case

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

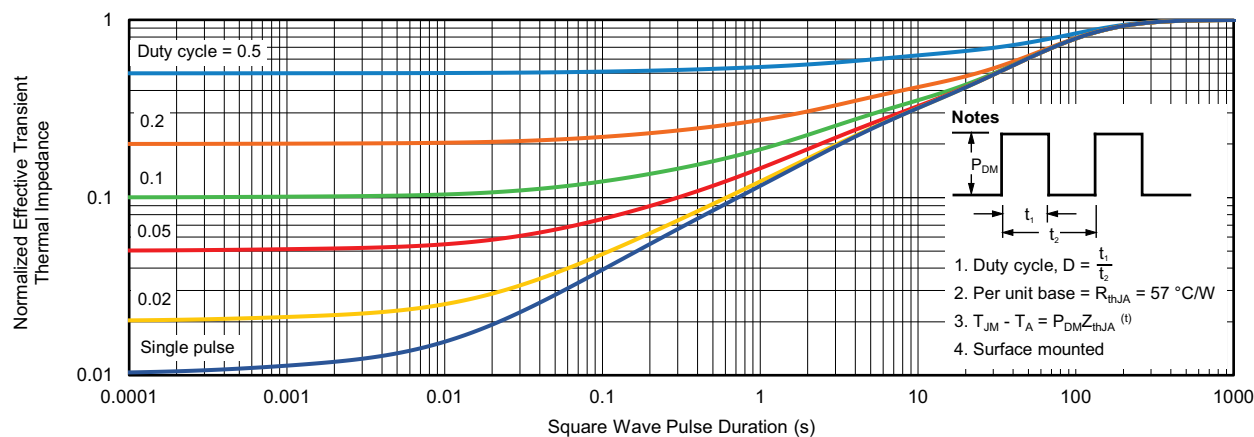


**Note**

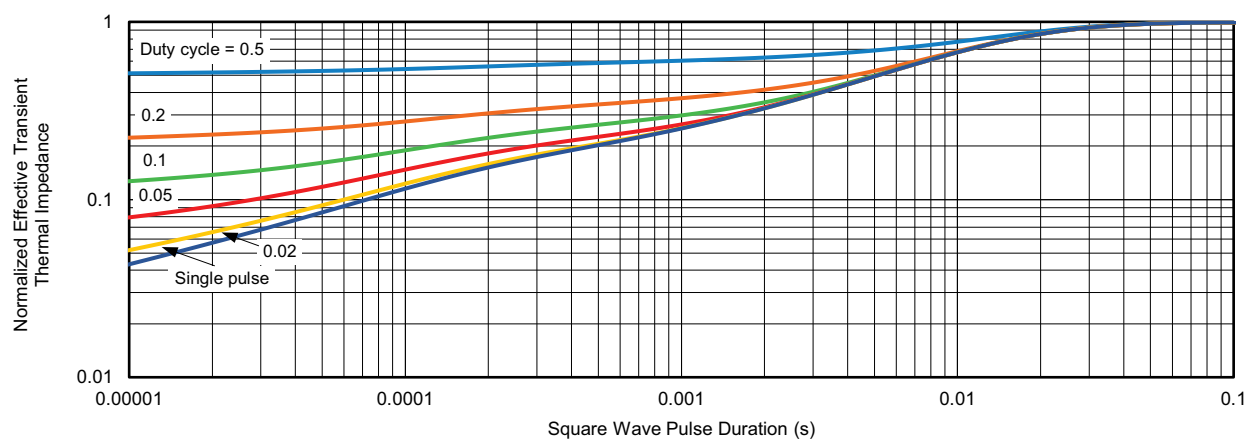
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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