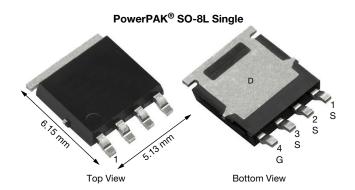


www.vishay.com

Vishay Siliconix

Automotive N-Channel 80 V (D-S) 175 °C MOSFET



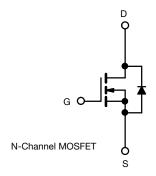
PRODUCT SUMMARY	
V _{DS} (V)	80
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0070
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0100
I _D (A)	60
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912







ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJA80EP-T1 (for detailed order number please see www.vishay.com/doc?79771)

PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V _{DS}	80	.,		
Gate-source voltage	V _{GS}	± 20	V		
Continuous drain current	T _C = 25 °C a	1	60		
	T _C = 125 °C	I _D	39		
Continuous source current (diode conduction	n) ^a	I _S	60	Α	
Pulsed drain current ^b		I _{DM}	120		
Single pulse avalanche current		I _{AS}	35	1	
Single pulse avalanche energy		E _{AS}	61	mJ	
Maximum power dissipation ^b	T _C = 25 °C	D	68	w	
	T _C = 125 °C	P_{D}	22	VV	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e		-	260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	R _{thJA}	68	°C/W
Junction-to-case (drain)		R_{thJC}	2.2	G/ VV

Notes

- a. Package limited
- b. Pulse test; pulse width $\leq 300 \,\mu\text{s}$, duty cycle $\leq 2 \,\%$
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257) The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	80	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 80 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
Drain-source on-state resistance ^a		V _{GS} = 10 V	I _D = 10 A	-	0.0058	0.0070	Ω
	Б	V _{GS} = 4.5 V	I _D = 8 A	-	0.0077	0.0100	
	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	-	-	0.0099	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0122	
Forward transconductance b	9fs	V _{DS}	= 15 V, I _D = 10 A	-	78	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	2800	3800	
Output capacitance	Coss	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	1400	2000	рF
Reverse transfer capacitance	C _{rss}			-	73	100	
Total gate charge ^c	Q_{g}			-	40	75	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 40 \text{ V}, I_{D} = 5 \text{ A}$	-	8	-	nC
Gate-drain charge ^c	Q _{gd}			-	6	-	
Gate resistance	R_{g}		f = 1 MHz	0.20	0.41	0.65	Ω
Turn-on delay time ^c	t _{d(on)}			-	16	30	
Rise time ^c	t _r	V _{DD}	= 40 V, $R_L = 8 \Omega$	-	5	10	
Turn-off delay time c	t _{d(off)}		$I_{\text{GEN}} = 10 \text{ V}, R_{\text{g}} = 1 \Omega$	-	31	50	ns
Fall time ^c	t _f			-	16	30	1
Source-Drain Diode Ratings and Chara	acteristics ^b						
Pulsed current ^a	I _{SM}			-	-	120	Α
Forward voltage	V _{SD}	l _F :	= 10 A, V _{GS} = 0	-	0.8	1.2	V
Body diode reverse recovery time	t _{rr}			-	65	135	ns
Body diode reverse recovery charge	Q _{rr}] , ,,	A -1:/-1+ 100 A/	-	110	225	nC
Reverse recovery fall time	ta	$\int I_F = 10$	A, di/dt = 100 A/μs	-	32	-	
Reverse recovery rise time	t _b	1		-	34	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}			-	-3.1	-7	Α

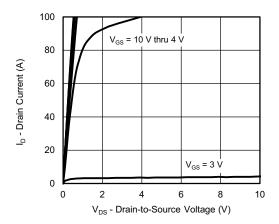
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

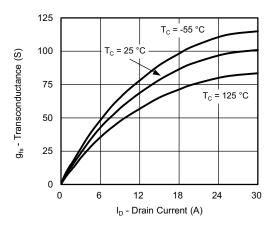
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



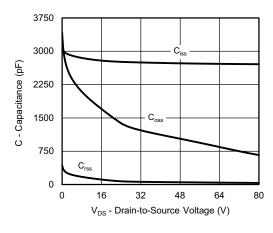
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



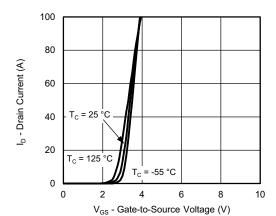
Output Characteristics



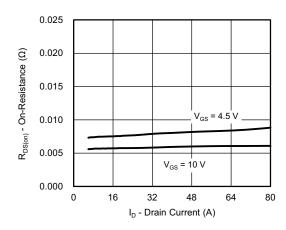
Transconductance



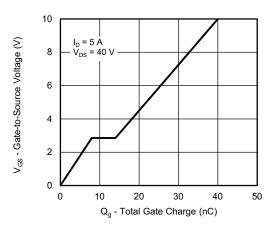
Capacitance



Transfer Characteristics



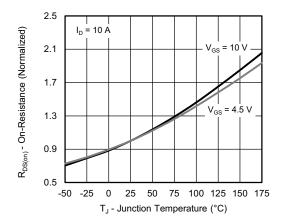
On-Resistance vs. Drain Current



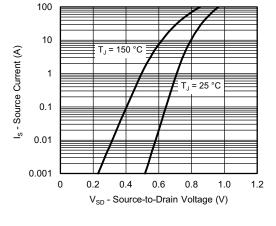
Gate Charge



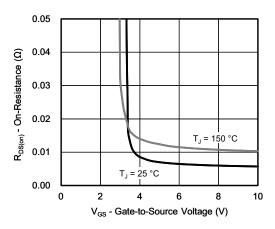
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



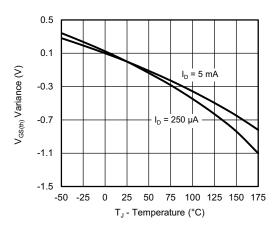
On-Resistance vs. Junction Temperature



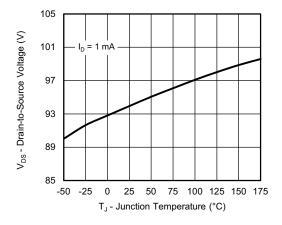
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



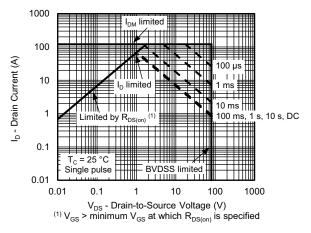
Threshold Voltage



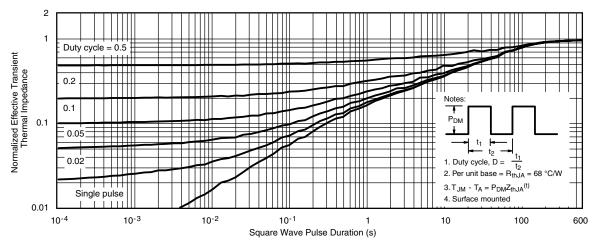
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



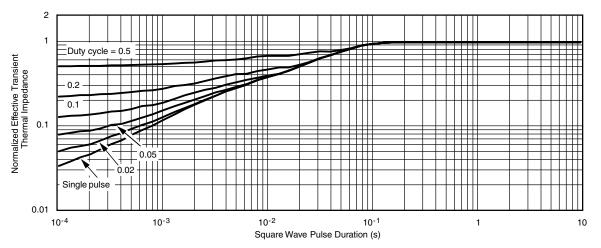
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg275519.



PowerPAK® SO-8L Case Outline 2



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DIM	MILLIMETERS			INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX		
Α	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094		0.004				
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC			0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	2.75	2.85	2.95	0.108	0.112	0.116		
E3	6.05	6.22	6.40	0.238	0.245	0.252		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
K		0.51		0.020				
W	0.23			0.009				
W1		0.41			0.016			
W2	2.82			0.111				
W3		2.96			0.117			
θ	0°	-	10°	0°	-	10°		

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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