# 8-Ch/Dual 4-Ch High-Performance CMOS Analog Multiplexers

## DESCRIPTION

The DG408 is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address ($A_0$, $A_1$, $A_2$). The DG409 is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address ($A_0$, $A_1$). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address ($A_x$) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408, DG409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see Technical Article TA201.

## FEATURES

- Low on-resistance - $R_{DS(on)}$: 100 Ω
- Low charge injection - Q: 20 pC
- Fast transition time - $t_{TRANS}$: 160 ns
- Low power - $I_{SUPPLY}$: 10 µA
- Single supply capability
- 44 V supply max. rating
- TTL compatible logic
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS* Available

HALOGEN FREE

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## BENEFITS

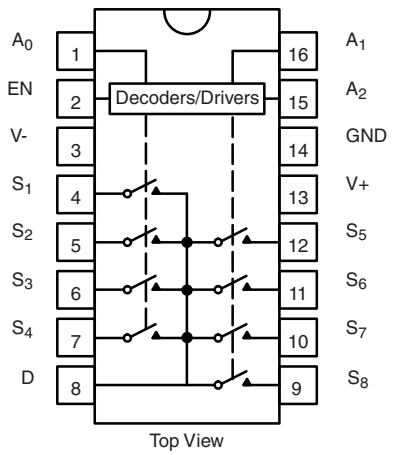
- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges
  - Single supply: +5 V to 36 V
  - Dual supplies: ± 5 V to ± 20 V

## APPLICATIONS

- Data acquisition systems
- Audio signal routing
- ATE systems
- Battery powered systems
- Single supply systems
- Medical instrumentation

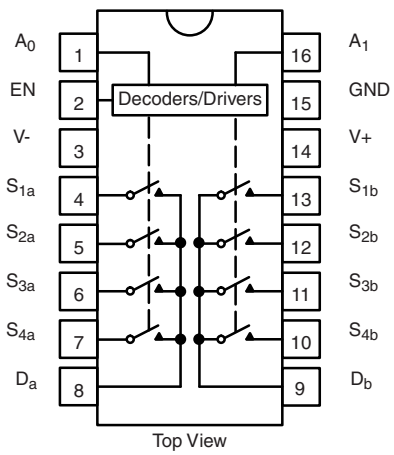
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG408** Dual-In-Line, SOIC and TSSOP




Top View

**DG409** Dual-In-Line, SOIC and TSSOP




Top View

| TRUTH TABLE (DG408) | | | | |
|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | EN | ON SWITCH |
| X | X | X | 0 | None |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

| TRUTH TABLE (DG409) | | | |
|---|---|---|---|
| $A_1$ | $A_0$ | EN | ON SWITCH |
| X | X | 0 | None |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 4 |

**Notes**

- Logic “0” = $V_{AL} \leq 0.8$ V
- Logic “1” = $V_{AH} \geq 2.4$ V
- X = do not care

| ORDERING INFORMATION (Commercial) | | | | |
|---|---|---|---|---|
| PART | CONFIGURATION | TEMP. RANGE | PACKAGE | ORDERING PART NUMBER |
| DG408 | 8:1 x 1 | -40 °C to +85 °C | 16-pin plastic DIP | DG408DJ-E3 |
| | | | 16-pin SOIC | DG408DY-E3 |
| | | | | DG408DY-T1-E3 |
| | | | 16-pin TSSOP | DG408DQ-E3 |
| | | | | DG408DQ-T1-E3 |
| DG409 | 4:1 x 2 | -40 °C to +85 °C | 16-pin plastic DIP | DG409DJ-E3 |
| | | | 16-pin SOIC | DG409DY-E3 |
| | | | | DG409DY-T1-E3 |
| | | | 16-pin TSSOP | DG409DQ-E3 |
| | | | | DG409DQ-T1-E3 |

**Note**

- -T1 indicates tape and reel, -E3 indicates lead (Pb)-free and RoHS-compliant, NO -E3 indicates standard tin/lead finish

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| PARAMETER | | LIMIT | UNIT |
| Voltages referenced to V- | V+ to V- [e] | 44 | V |
| | GND to V- | -25 | |
| Digital inputs [a], $V_S$, $V_D$ | | (V-) - 2 to (V+) + 2<br>or 20 mA, whichever occurs first | |
| Current (any terminal) | | 30 | mA |
| Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.) | | 100 | |
| Storage temperature | (DJ, DY suffix) | -65 to +125 | °C |
| Power dissipation (package) [b] | 16-pin plastic DIP [c] | 450 | mW |
| | 16-pin narrow SOIC and TSSOP [d] | 600 | |

**Notes**

a. Signals on $S_X$, $D_X$ or $IN_X$ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads soldered or welded to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 7.6 mW/°C above 75 °C
e. Also applies when V- = GND

## SPECIFICATIONS [a]

| PARAMETER | | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED<br>V+ = 15 V, V- = -15 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V [f] | TEMP. [b] | TYP. [c] | D SUFFIX -40 °C to +85 °C<br>MIN. [d] | <br>MAX. [d] | UNIT |
|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | |
| Analog signal range [e] | | $V_{ANALOG}$ | | Full | - | -15 | 15 | V |
| Drain-source on-resistance | | $R_{DS(on)}$ | $V_D$ = ± 10 V, $I_S$ = -10 mA | Room | 40 | - | 100 | Ω |
| | | | | Full | - | - | 125 | |
| $R_{DS(on)}$ matching between channels [g] | | $\Delta R_{DS(on)}$ | $V_D$ = ± 10 V | Room | - | - | 15 | |
| Source off leakage current | | $I_{S(off)}$ | $V_S$ = ± 10 V, $V_D$ = ± 10 V, $V_{EN}$ = 0 V | Room | - | -0.5 | 0.5 | nA |
| | | | | Full | - | -5 | 5 | |
| DG408 | Drain off leakage current | $I_{D(off)}$ | $V_D$ = ± 10 V, $V_S$ = ± 10 V, $V_{EN}$ = 0 V | Room | - | -1 | 1 | |
| DG408 | | | | Full | - | -20 | 20 | |
| DG409 | | | | Room | - | -1 | 1 | |
| DG409 | | | | Full | - | -10 | 10 | |
| DG408 | Drain on leakage current | $I_{D(on)}$ | $V_S$ = $V_D$ = ± 10 V, sequence each switch on | Room | - | -1 | 1 | |
| DG408 | | | | Full | - | -20 | 20 | |
| DG409 | | | | Room | - | -1 | 1 | |
| DG409 | | | | Full | - | -10 | 10 | |
| **Digital Control** | | | | | | | | |
| Logic high Input voltage | | $V_{INH}$ | | Full | - | 2.4 | - | V |
| Logic low Input voltage | | $V_{INL}$ | | Full | - | - | 0.8 | |
| Logic high Input current | | $I_{AH}$ | $V_A$ = 2.4 V, 15 V | Full | - | -10 | 10 | µA |
| Logic low Input current | | $I_{AL}$ | $V_{EN}$ = 0 V, 2.4 V, $V_A$ = 0 V | Full | - | -10 | 10 | |
| Logic input capacitance | | $C_{in}$ | f = 1 MHz | Room | 8 | - | - | pF |
| **Dynamic Characteristics** | | | | | | | | |
| Transition time | | $t_{TRANS}$ | See Fig. 2 | Full | 160 | - | 250 | ns |
| Break-before-make interval | | $t_{OPEN}$ | See Fig. 4 | Room | - | 10 | - | |
| Enable turn-on time | | $t_{on(EN)}$ | See Fig. 3 | Room | 115 | - | 150 | |
| | | | | Full | - | - | - | |
| Enable turn-off time | | $t_{off(EN)}$ | | Room | 105 | - | 150 | |
| Charge injection | | Q | $C_L$ = 10 nF, $V_S$ = 0 V | Room | 20 | - | - | pC |
| Off isolation [h] | | OIRR | $V_{EN}$ = 0 V, $R_L$ = 1 kΩ, f = 1 MHz | Room | -75 | - | - | pF |
| Source off capacitance | | $C_{S(off)}$ | $V_{EN}$ = 0 V, $V_S$ = 0 V, f = 1 MHz | Room | 3 | - | - | |
| DG408 | Drain off capacitance | $C_{D(off)}$ | $V_{EN}$ = 0 V, $V_D$ = 0 V, f = 1 MHz | Room | 26 | - | - | |
| DG409 | | | | Room | 14 | - | - | |
| DG408 | Drain on capacitance | $C_{D(on)}$ | | Room | 37 | - | - | |
| DG409 | | | | Room | 25 | - | - | |
| Power Supplies | | | | | | | | |
| Positive supply current | | I+ | $V_{EN}$ = $V_A$ = 0 V or 5 V | Full | 10 | - | 75 | µA |
| Negative supply current | | I- | | Full | 1 | -75 | - | |
| Positive supply current | | I+ | $V_{EN}$ = $V_A$ = 0 V or 5 V | Room | 0.2 | - | 0.5 | mA |
| | | | | Full | - | - | 2 | |
| Negative supply current | | I- | | Full | - | -500 | - | µA |

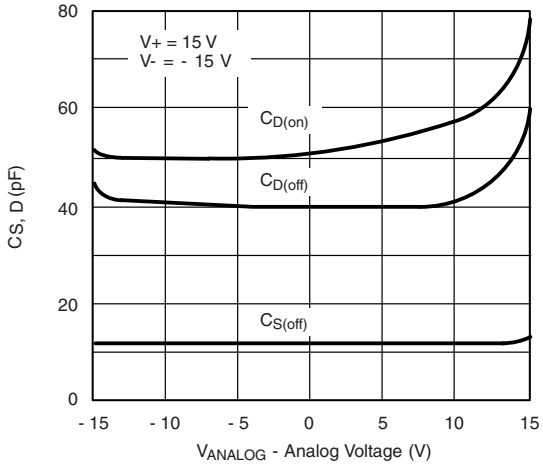
| SPECIFICATIONS [a] (single supply) | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED<br>V+ = 12 V, V- = 0 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V [f] | TEMP. [b] | TYP. [c] | D SUFFIX -40 °C to +85 °C<br>MIN. [d] | <br>MAX. [d] | UNIT |
| **Analog Switch** | | | | | | | |
| Drain-source on-resistance [e, f] | $R_{DS(on)}$ | $V_D$ = 3 V, 10 V, $I_S$ = -1 mA | Room | 90 | - | - | Ω |
| **Dynamic Characteristics** | | | | | | | |
| Switching time of multiplexer [e] | $t_{TRANS}$ | $V_{S1}$ = 8 V, $V_{S8}$ = 0 V, $V_{IN}$ = 2.4 V | Room | 180 | - | - | ns |
| Enable turn-on time [e] | $t_{on(EN)}$ | $V_{INH}$ = 2.4 V, $V_{INL}$ = 0 V, $V_{S1}$ = 5 V | Room | 180 | - | - | |
| Enable turn-off time [e] | $t_{off(EN)}$ | | Room | 120 | - | - | |
| Charge injection [e] | Q | $C_L$ = 1 nF, $V_S$ = 0 V, $R_S$ = 0 | Room | 5 | - | - | pC |

**Notes**

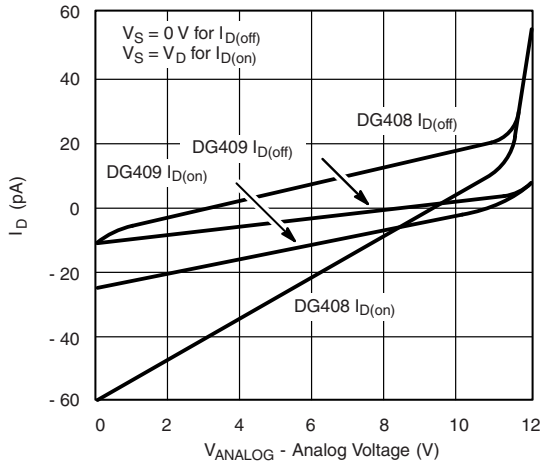
a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. $V_{IN}$ = input voltage to perform proper function
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 due to proximity to the drain pin

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

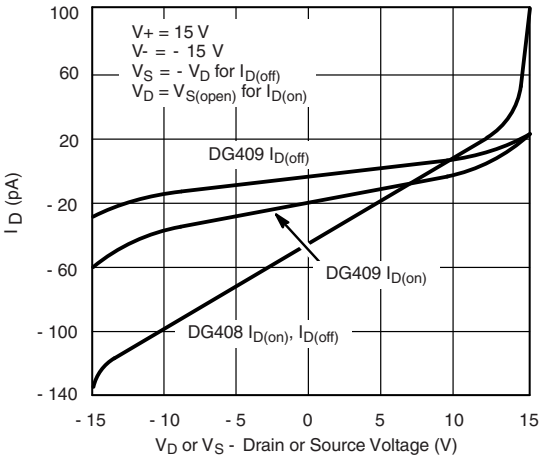
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



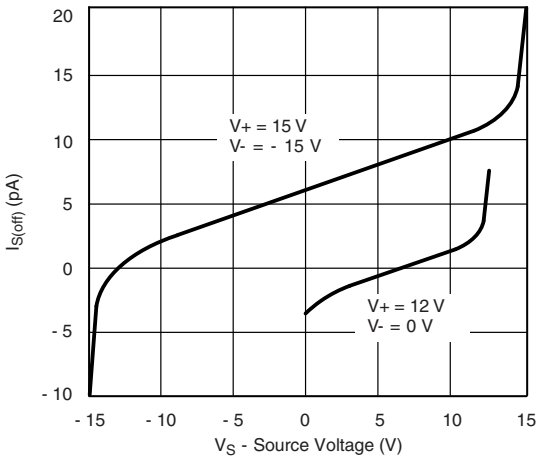

**Source/Drain Capacitance vs. Analog Voltage**



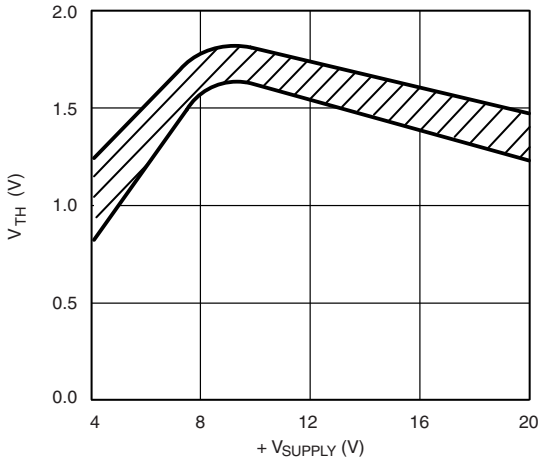

**Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)**



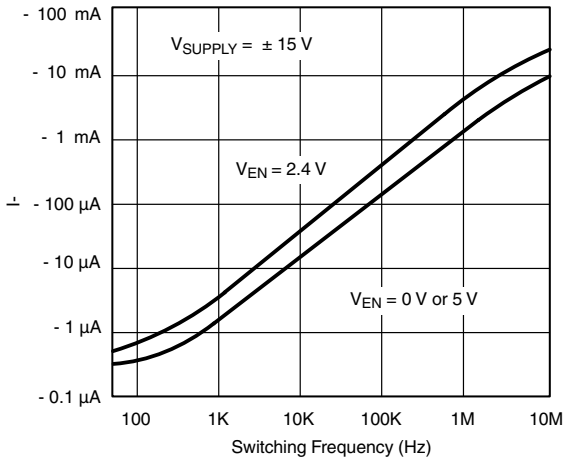

**Drain Leakage Current vs. Source/Drain Voltage**




**Source Leakage Current vs. Source Voltage**

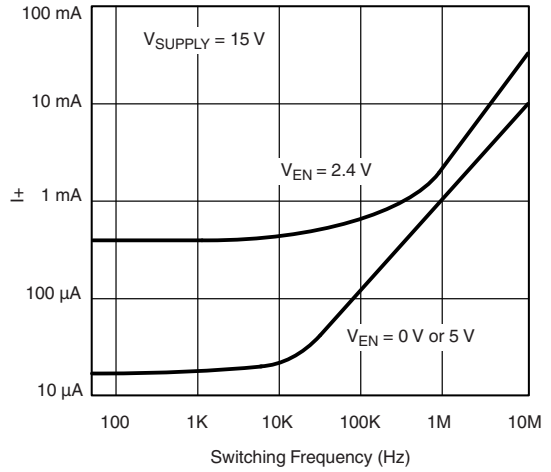



**Input Switching Threshold vs. Supply Voltage**

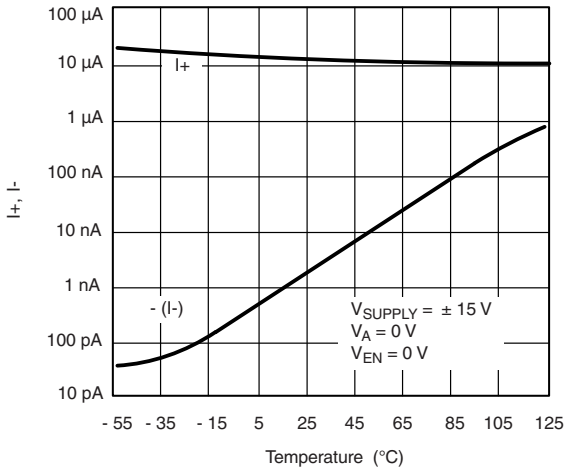



**Negative Supply Current vs. Switching Frequency**

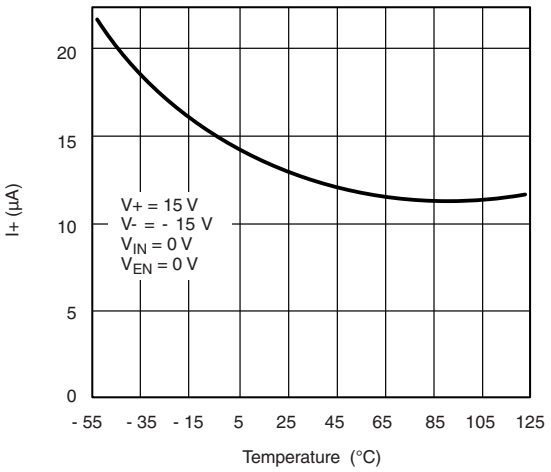
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



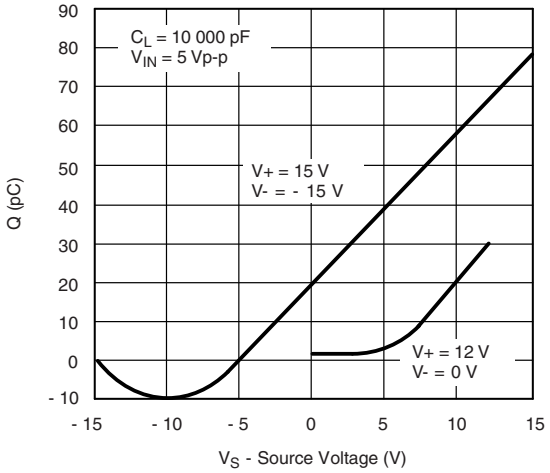

**Positive Supply Current vs. Switching Frequency**



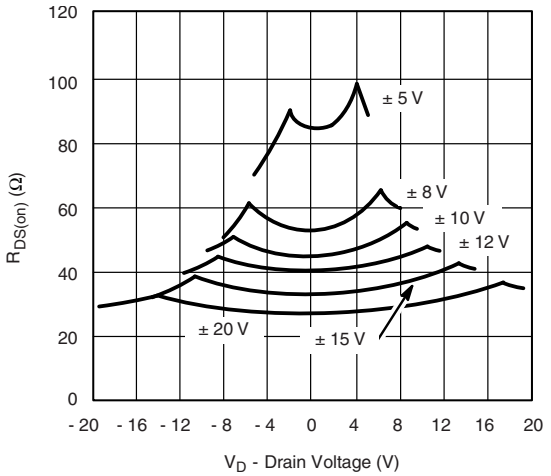

**$I_{SUPPLY}$ vs. Temperature**



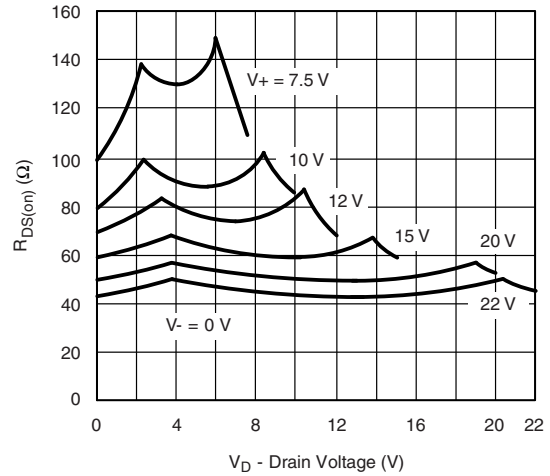

**Positive Supply Current vs. Temperature (DG408)**




**Charge Injection vs. Analog Voltage**

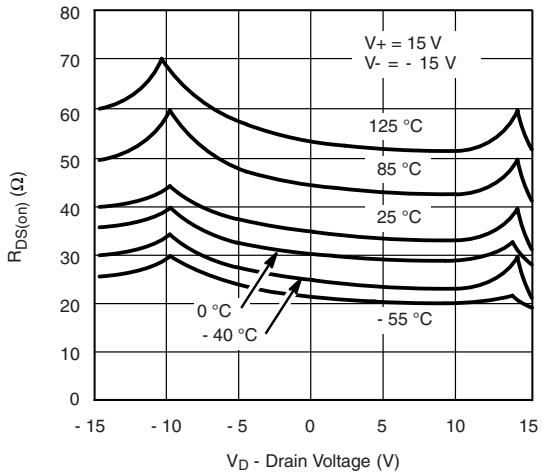



**$R_{DS(on)}$ vs. $V_D$ and Supply**

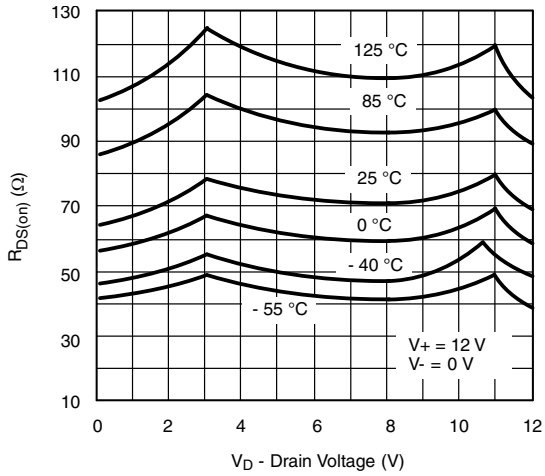



**$R_{DS(on)}$ vs. $V_D$ and Supply (Single Supply)**

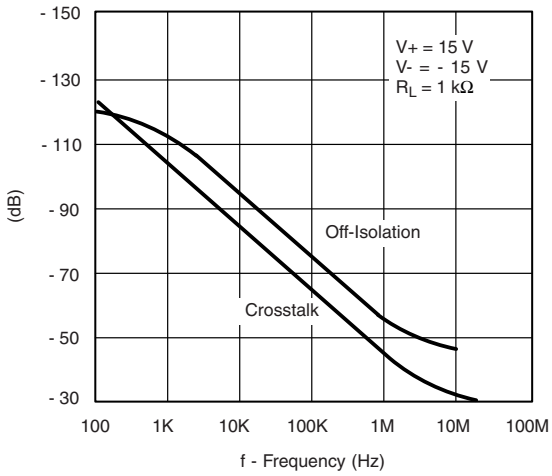
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



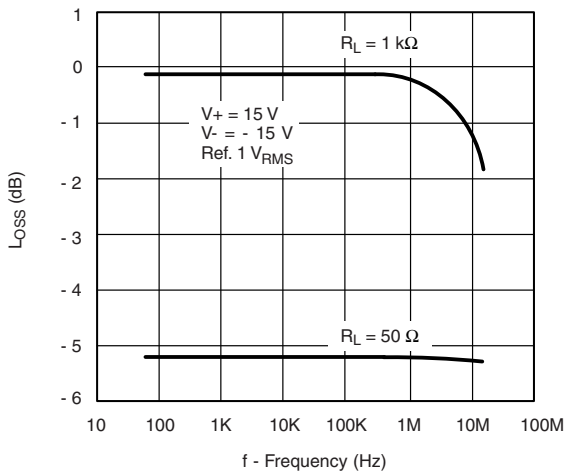

**$R_{DS(on)}$ vs. $V_D$ and Temperature**



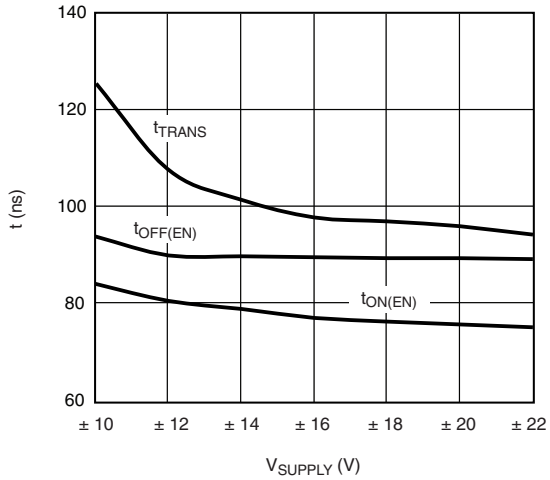

**$R_{DS(on)}$ vs. $V_D$ and Temperature (Single Supply)**



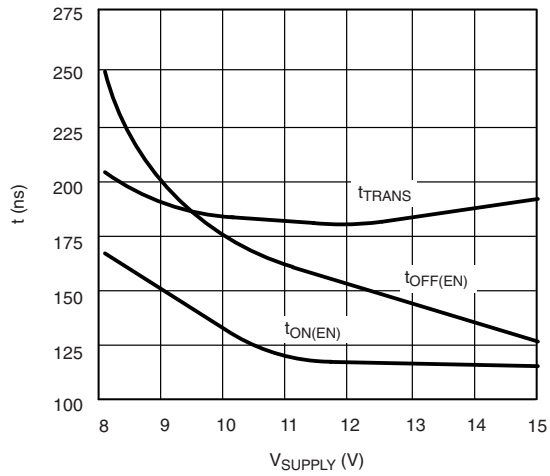

**Off Isolation and Crosstalk vs. Frequency**




**Insertion Loss vs. Frequency**




**Switching Time vs. Bipolar Supply**




**Switching Time vs. Single Supply**

## SCHEMATIC DIAGRAM (Typical Channel)

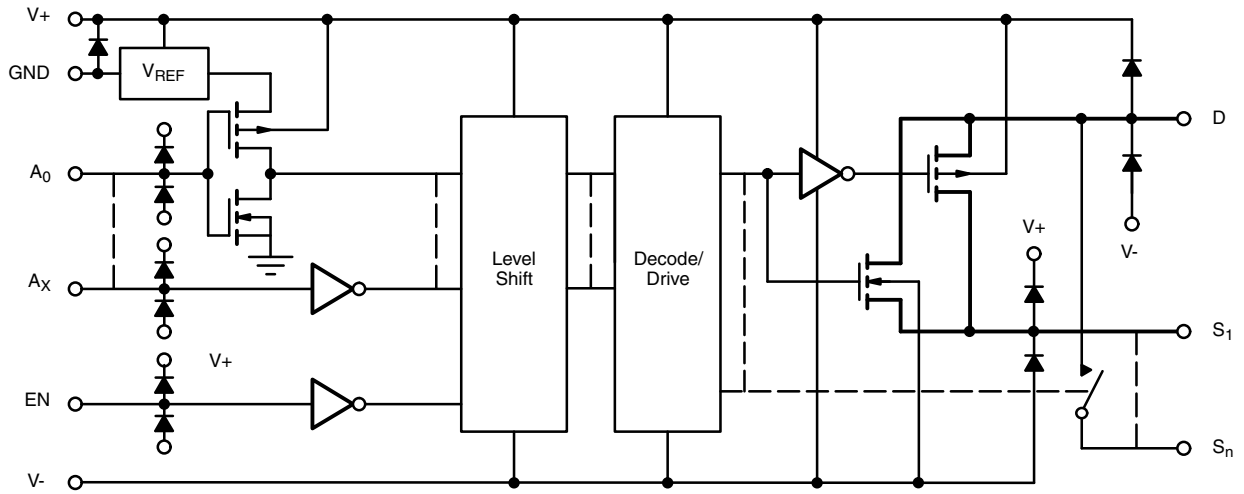



**Fig. 1**

## TEST CIRCUITS

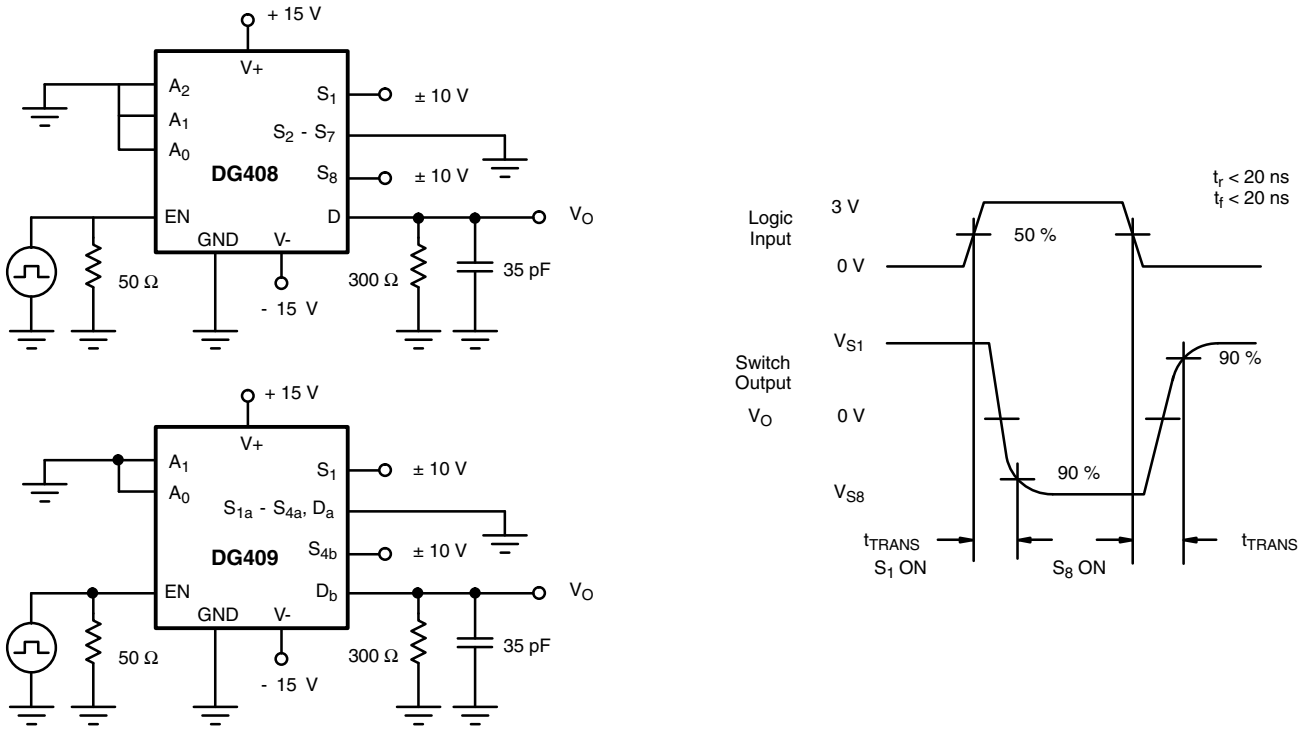



**Fig. 2 - Transition Time**

## TEST CIRCUITS

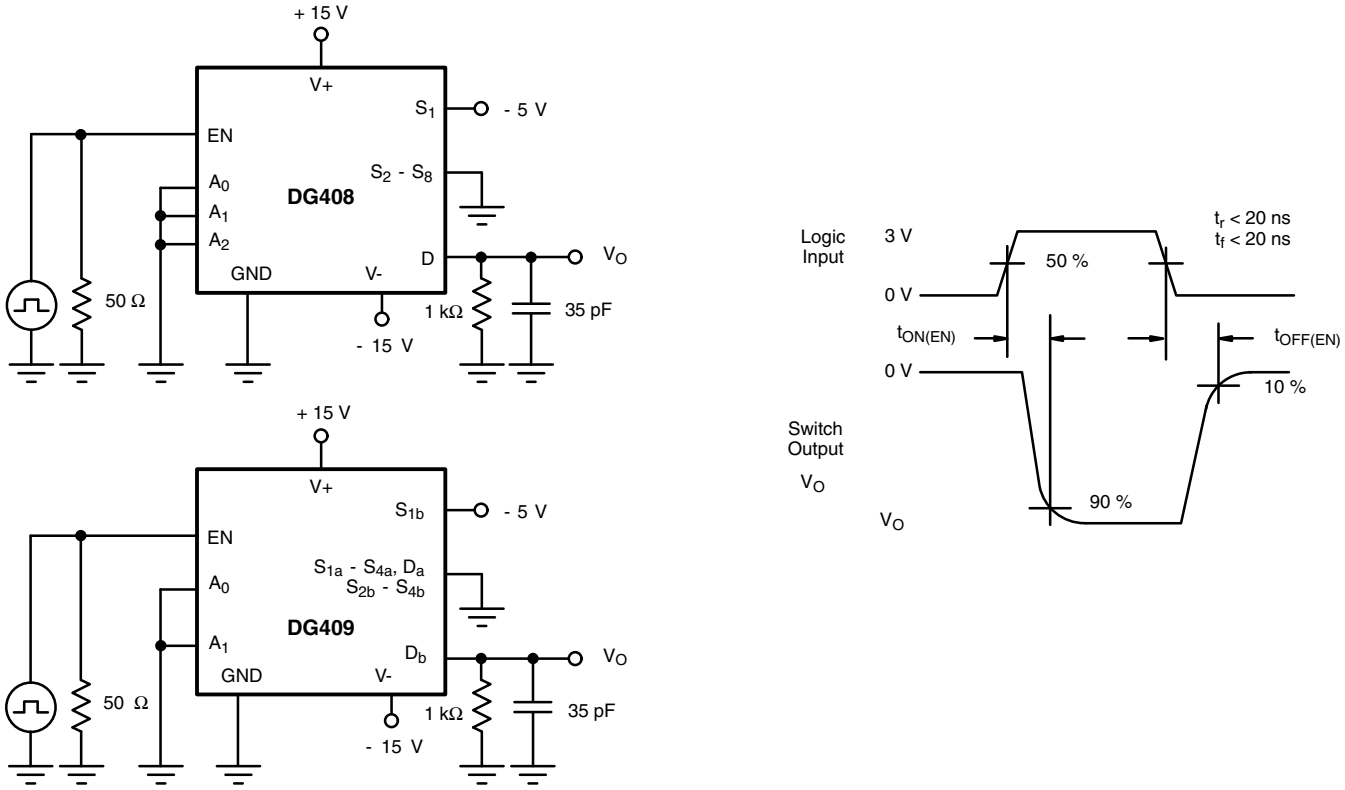



**Fig. 3 - Enable Switching Time**

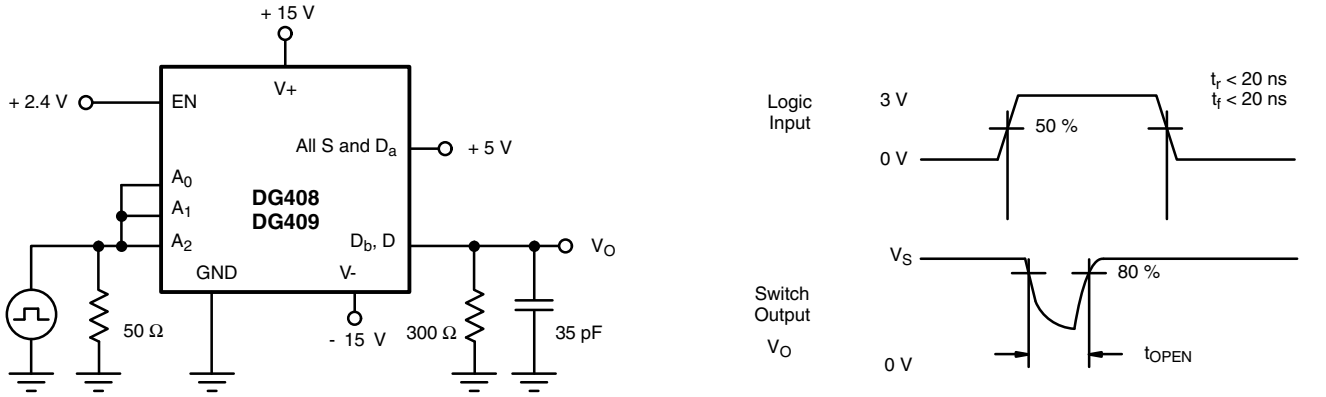



**Fig. 4 - Break-Before-Make Interval**

## TEST CIRCUITS

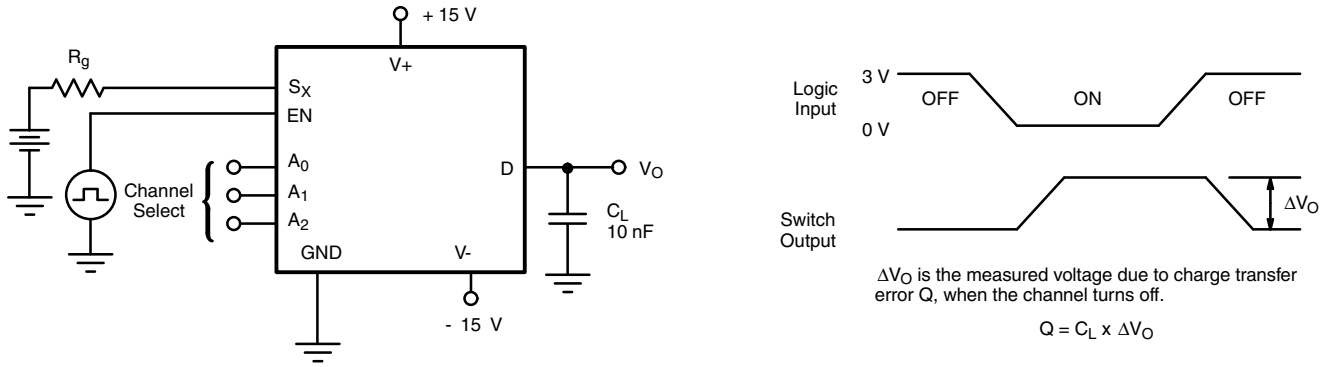



**Fig. 5 - Charge Injection**

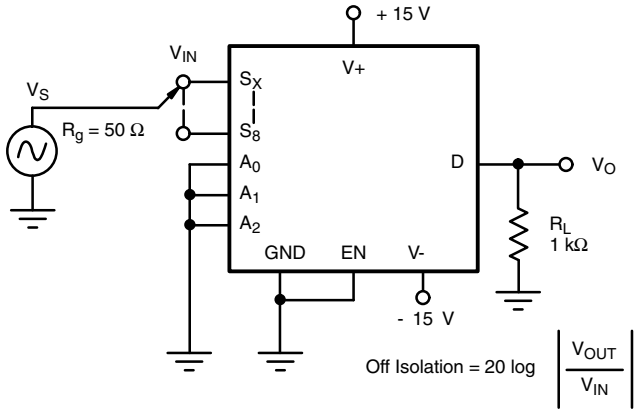



**Fig. 6 - Off Isolation**

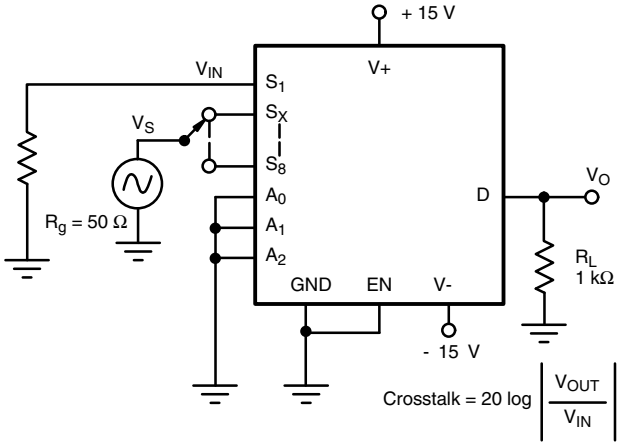



**Fig. 7 - Crosstalk**

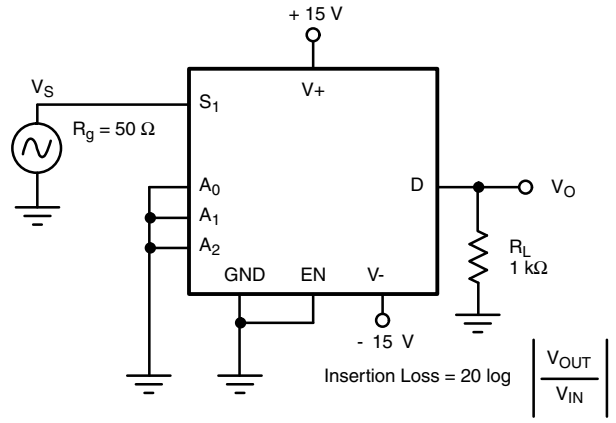



**Fig. 8 - Insertion Loss**

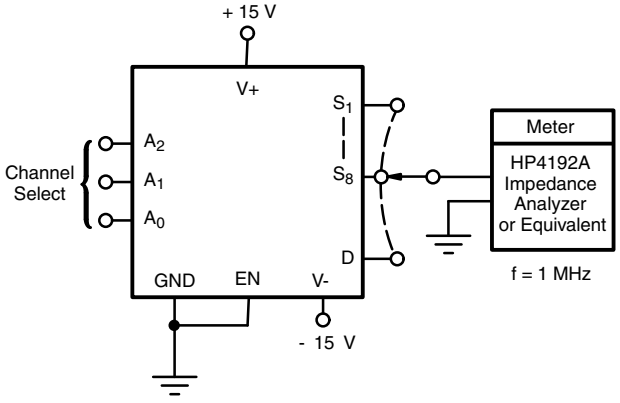



**Fig. 9 - Source Drain Capacitance**

## APPLICATION HINTS

### Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference VS - (V-) does not exceed + 44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

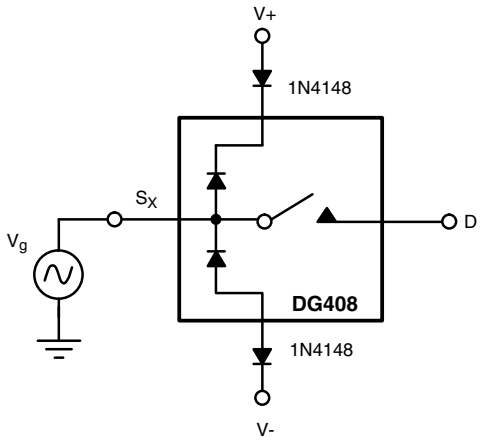
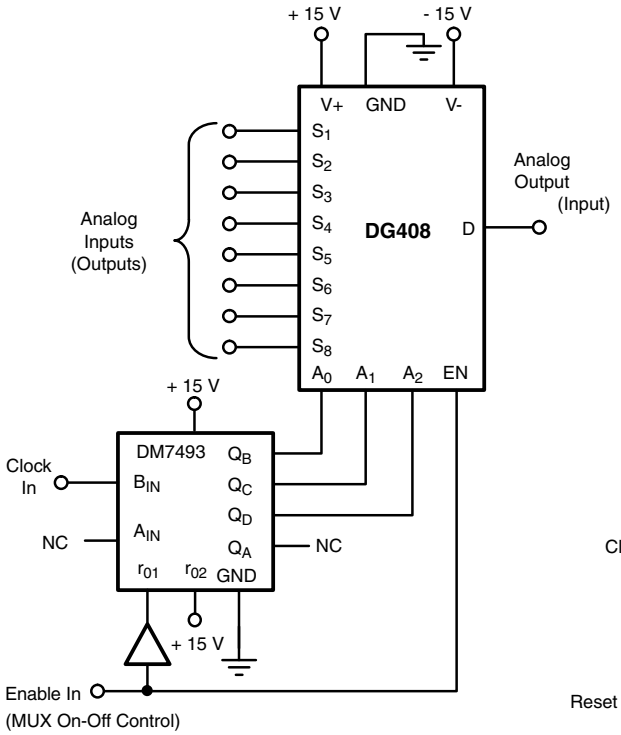



**Fig. 10 - Overvoltage Protection Using Blocking Diodes**

**8-Channel Sequential Multiplexer/Demultiplexer**




**Differential 4-Channel Sequential Multiplexer/Demultiplexer**

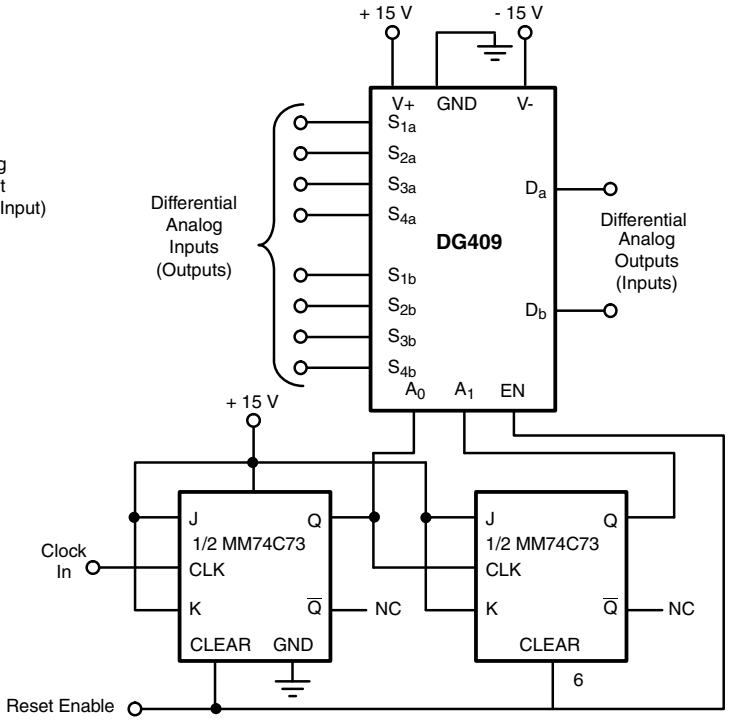



**Fig. 11**

| PRODUCT SUMMARY | | | | | | |
|---|---|---|---|---|---|---|
| Part number | DG408 | DG408 | DG408 | DG409 | DG409 | DG409 |
| Status code | 2 | 2 | 2 | 2 | 2 | 2 |
| Configuration | 8:1 x 1 | 8:1 x 1 | 8:1 x 1 | 4:1 x 2 | 4:1 x 2 | 4:1 x 2 |
| Single supply min. (V) | 5 | 5 | 5 | 5 | 5 | 5 |
| Single supply max. (V) | 36 | 36 | 36 | 36 | 36 | 36 |
| Dual supply min. (V) | 5 | 5 | 5 | 5 | 5 | 5 |
| Dual supply max. (V) | 20 | 20 | 20 | 20 | 20 | 20 |
| On-resistance (Ω) | 40 | 40 | 40 | 40 | 40 | 40 |
| Charge injection (pC) | 20 | 20 | 20 | 20 | 20 | 20 |
| Source on capacitance (pF) | 37 | 37 | 37 | 25 | 25 | 25 |
| Source off capacitance (pF) | 3 | 3 | 3 | 3 | 3 | 3 |
| Leakage switch on typ. (nA) | - | - | - | - | - | - |
| Leakage switch off max. (nA) | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| -3 dB bandwidth (MHz) | - | - | - | - | - | - |
| Package | SO-16 (narrow) AS | TSSOP-16 | Plastic DIP-16 | TSSOP-16 | SO-16 (narrow) AS | Plastic DIP-16 |
| Functional circuit / applications | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare | Multi purpose, instrumentation, medical and healthcare |
| Interface | Parallel | Parallel | Parallel | Parallel | Parallel | Parallel |
| Single supply operation | Yes | Yes | Yes | Yes | Yes | Yes |
| Dual supply operation | Yes | Yes | Yes | Yes | Yes | Yes |
| Turn on time max. (ns) | 150 | 150 | 150 | 150 | 150 | 150 |
| Crosstalk and off isolation | -75 | -75 | -75 | -75 | -75 | -75 |

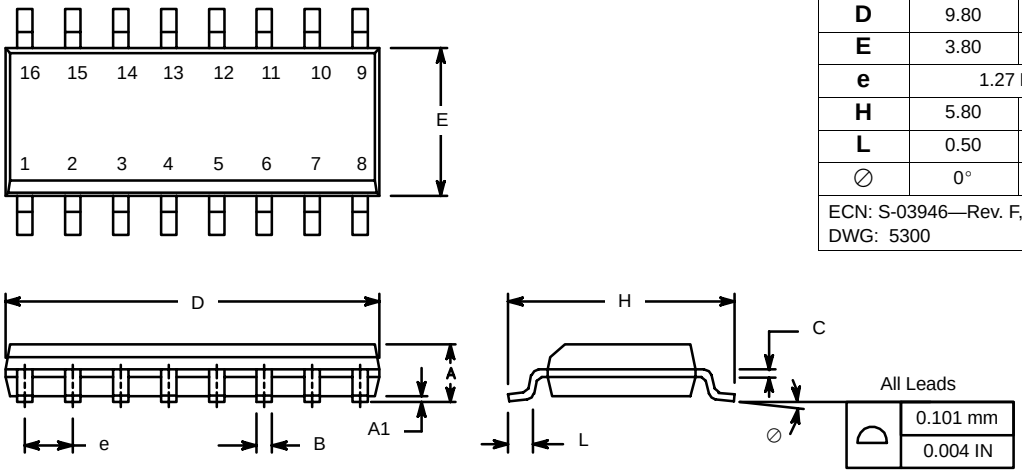
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70062.*

## SOIC (NARROW): 16-LEAD

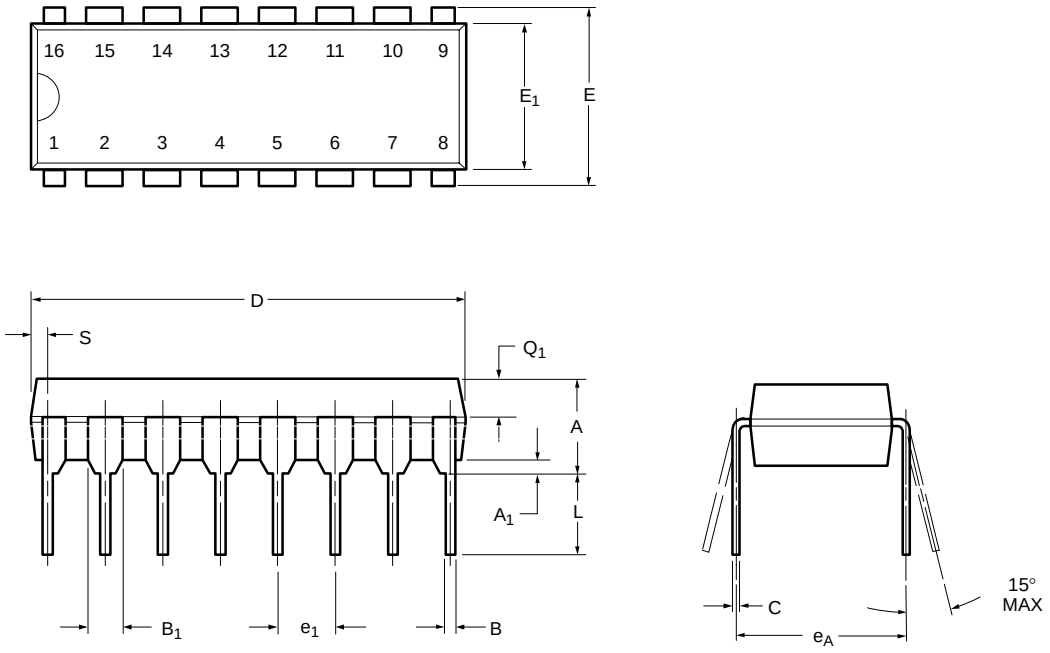
**JEDEC Part Number: MS-012**

| Dim | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ⊘ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

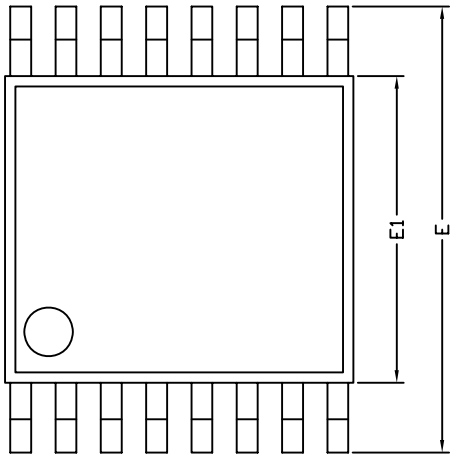


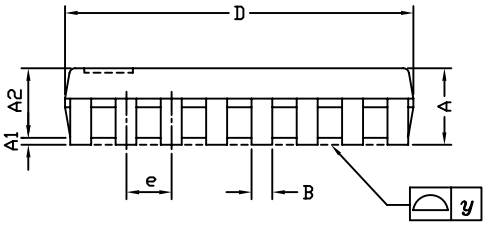
## PDIP: 16-LEAD

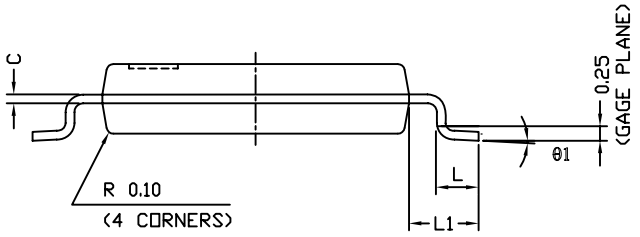



| Dim | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| **A** | 3.81 | 5.08 | 0.150 | 0.200 |
| **$A_1$** | 0.38 | 1.27 | 0.015 | 0.050 |
| **B** | 0.38 | 0.51 | 0.015 | 0.020 |
| **$B_1$** | 0.89 | 1.65 | 0.035 | 0.065 |
| **C** | 0.20 | 0.30 | 0.008 | 0.012 |
| **D** | 18.93 | 21.33 | 0.745 | 0.840 |
| **E** | 7.62 | 8.26 | 0.300 | 0.325 |
| **$E_1$** | 5.59 | 7.11 | 0.220 | 0.280 |
| **$e_1$** | 2.29 | 2.79 | 0.090 | 0.110 |
| **$e_A$** | 7.37 | 7.87 | 0.290 | 0.310 |
| **L** | 2.79 | 3.81 | 0.110 | 0.150 |
| **$Q_1$** | 1.27 | 2.03 | 0.050 | 0.080 |
| **S** | 0.38 | 1.52 | .015 | 0.060 |
| ECN: S-03946—Rev. D, 09-Jul-01<br>DWG: 5482 | | | | |

**TSSOP: 16-LEAD**

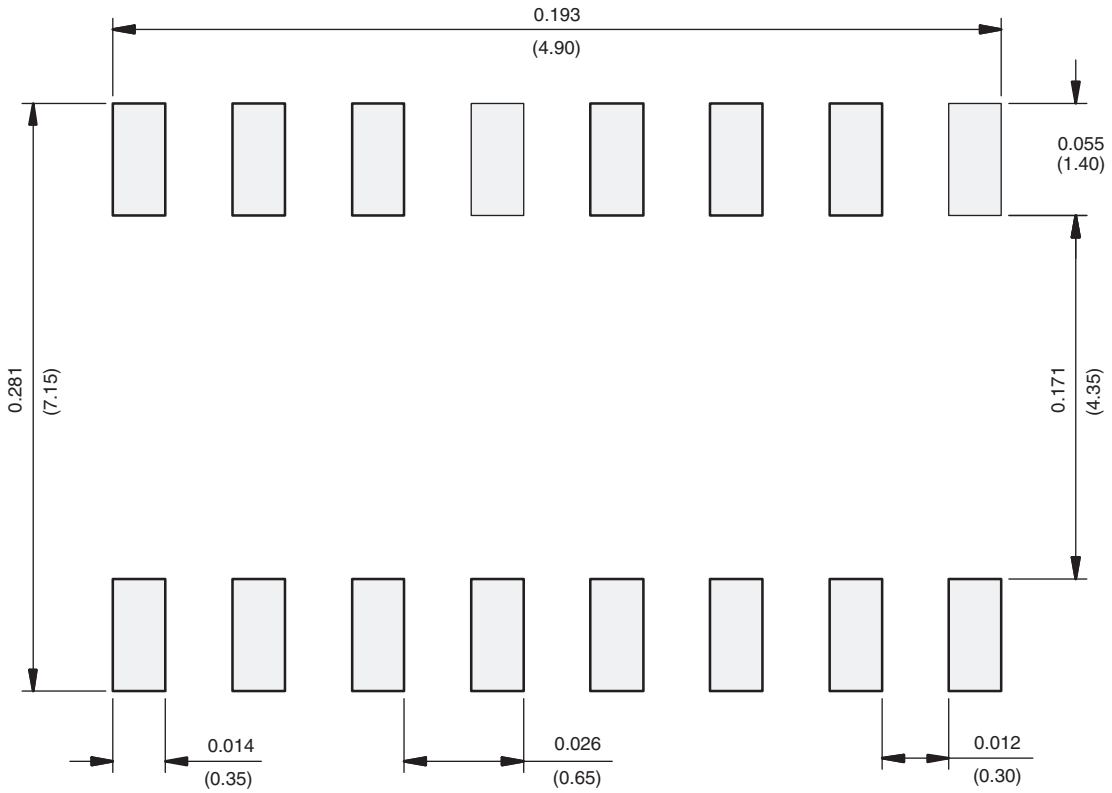


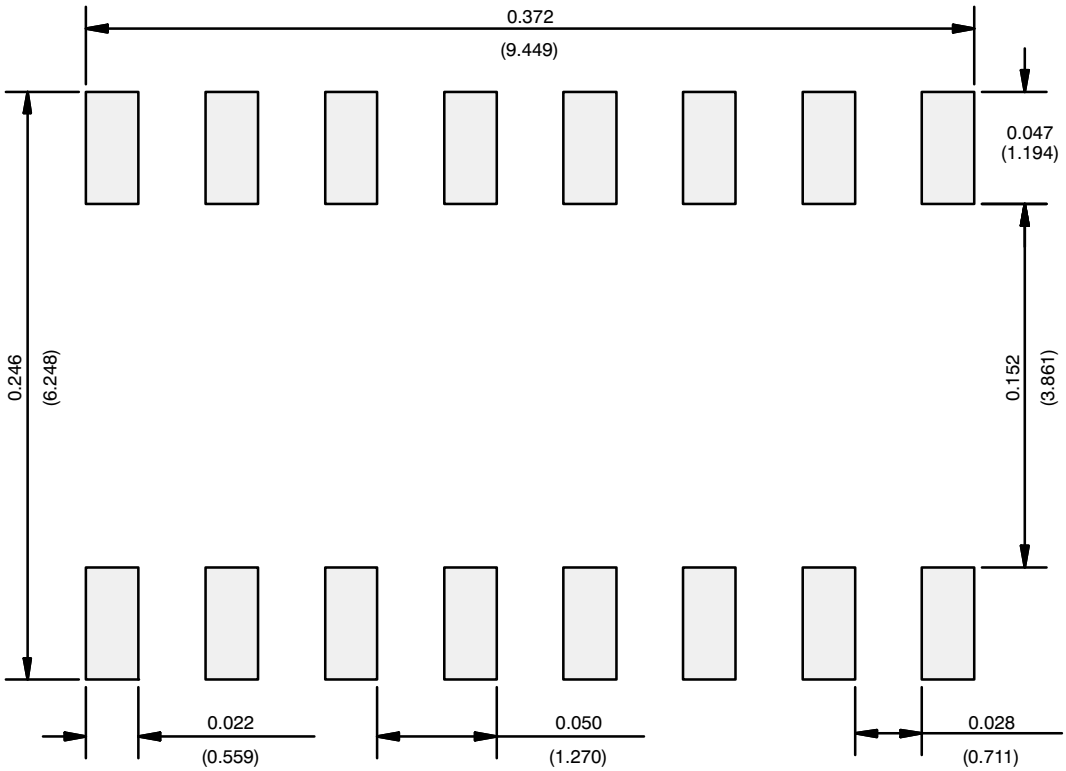

| Symbols | DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | 1.10 | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | - | 1.00 | 1.05 |
| B | 0.22 | 0.28 | 0.38 |
| C | - | 0.127 | - |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.10 | 6.40 | 6.70 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | - | 0.65 | - |
| L | 0.50 | 0.60 | 0.70 |
| L1 | 0.90 | 1.00 | 1.10 |
| y | - | - | 0.10 |
| θ1 | 0° | 3° | 6° |
| ECN: S-61920-Rev. D, 23-Oct-06<br>DWG: 5624 | | | |

## RECOMMENDED MINIMUM PAD FOR TSSOP-16




Recommended Minimum Pads
Dimensions in inches (mm)

## RECOMMENDED MINIMUM PADS FOR SO-16




Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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