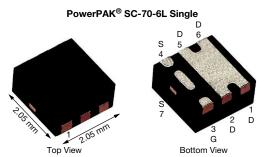


# Vishay Siliconix

# N-Channel 200 V (D-S) MOSFET



#### Marking code: AG

· ·	
PRODUCT SUMMARY	
V <sub>DS</sub> (V)	200
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	1.38
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 2.5 \text{ V}$	1.50
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 1.8 \text{ V}$	3.50
Q <sub>g</sub> typ. (nC)	5
I <sub>D</sub> (A) <sup>a</sup>	2.6
Configuration	Single

#### **FEATURES**

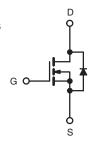
- TrenchFET® power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Low on-resistance
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912">www.vishav.com/doc?99912</a>



ROHS COMPLIANT HALOGEN FREE

# APPLICATIONS

• Boost converter for portable devices



N-Channel MOSFET

ORDERING INFORMATION						
Package	PowerPAK SC-70					
Lead (Pb)-free and halogen-free	SiA456DJ-T1-GE3					

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	200	.,	
Gate-source voltage		V <sub>GS</sub>	±16	v	
	T <sub>C</sub> = 25 °C		2.6		
Continuous dusin suggest /T 150 °C)	T <sub>C</sub> = 70 °C	1 .	2.1		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	1.1 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		0.9 <sup>b, c</sup>	Α	
Pulsed drain current		I <sub>DM</sub>	2		
Continuous autorio dia da autorio	T <sub>C</sub> = 25 °C		3.6		
Continuous source-drain diode current	T <sub>A</sub> = 25 °C	ls –	2.9 <sup>b, c</sup>		
	T <sub>C</sub> = 25 °C		19		
Marriago de accesa disensa esta de	T <sub>C</sub> = 70 °C	1 5 [	12	14/	
Maximum power dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5 <sup>b, c</sup>	W	
	T <sub>A</sub> = 70 °C	1	2.2 <sup>b, c</sup>		
Operating junction and storage temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C		
Soldering recommendations (peak tempera	ture) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient b, f	t ≤ 5 s	$R_{thJA}$	28	36	°C/W				
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	5.3	6.5	C/ VV				

#### Notes

- a. T<sub>C</sub> = 25 °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 80 °C/W



www.vishay.com

# Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						•
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200	-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	265	-	>//0C
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-3.5	-	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.6	-	1.4	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$	-	-	±100	nA
Zava gata valtaga duain avuunnt	1	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μA
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	2	-	-	Α
		$V_{GS} = 4.5 \text{ V}, I_D = 0.75 \text{ A}$	-	1.08	1.38	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 0.5 \text{ A}$	-	1.12	1.5	Ω
		$V_{GS} = 1.8 \text{ V}, I_D = 0.1 \text{ A}$	-	1.2	3.5	
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 4 \text{ V}, I_D = 0.75 \text{ A}$	-	5	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>		-	350	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	12	-	рF
Reverse transfer capacitance	C <sub>rss</sub>		-	6	-	1
Tatal asta shaves	Qg	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.1 A	-	9.5	14.5	nC
Total gate charge			-	5	7.5	
Gate-source charge	$Q_{gs}$	$V_{DS} = 100 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 1.1 \text{ A}$	-	0.7	-	
Gate-drain charge	$Q_{gd}$		-	1.7	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	-	2	-	Ω
Turn-on delay time	t <sub>d(on)</sub>		-	10	15	ns
Rise time	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_L = 111 \Omega,$	-	25	40	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 0.9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	30	45	
Fall time	t <sub>f</sub>		-	20	30	
Turn-on delay time	t <sub>d(on)</sub>		-	5	10	
Rise time	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_1 = 111 \Omega,$	-	20	30	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 0.9 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	16	25	
Fall time	t <sub>f</sub>		-	12	20	1
Drain-Source Body Diode Characteristic	s					
Continuous source-drain diode current	inuous source-drain diode current I <sub>S</sub>		-	-	3.6	
Pulse diode forward current	I <sub>SM</sub>		-	-	2	A
Body diode voltage V <sub>SD</sub>		I <sub>S</sub> = 0.9 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body diode reverse recovery time t <sub>rr</sub>			-	40	80	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	I <sub>F</sub> = 0.9 A, di/dt = 100 A/μs,	-	40	80	nC
Reverse recovery fall time	t <sub>a</sub>	T <sub>J</sub> = 25 °C	-	21	-	1
Reverse recovery rise time	t <sub>b</sub>		_	19	_	ns

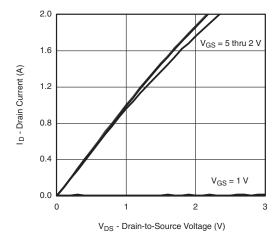
### Notes

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing

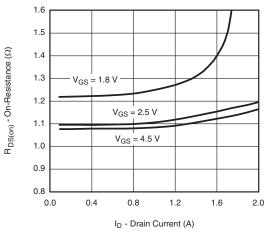
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



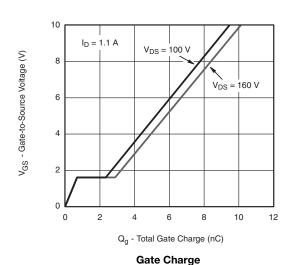
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

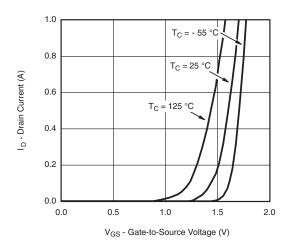


### **Output Characteristics**

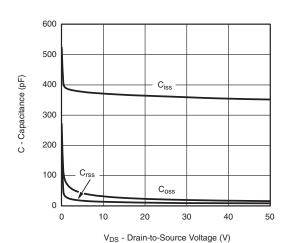


### On-Resistance vs. Drain Current and Gate Voltage

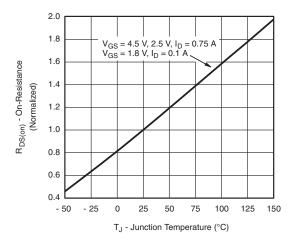




**Transfer Characteristics** 



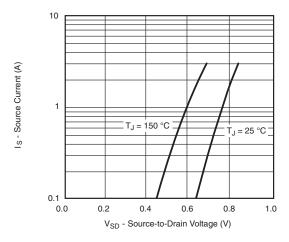
Capacitance



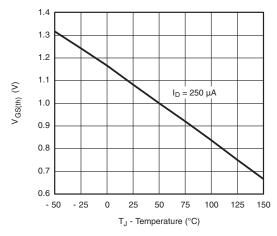
On-Resistance vs. Junction Temperature



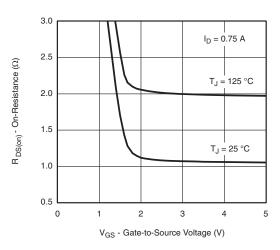
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



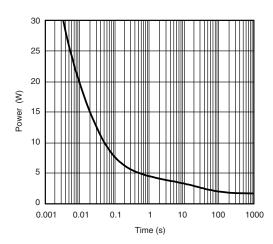
### Source-Drain Diode Forward Voltage



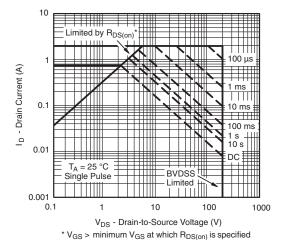
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



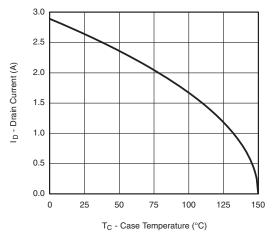
Single Pulse Power (Junction-to-Ambient)

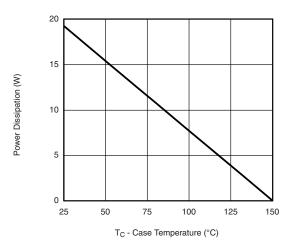


Safe Operating Area, Junction-to-Ambient



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



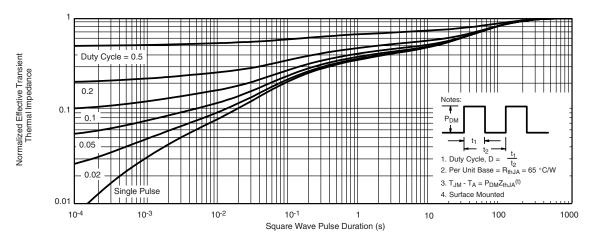


Current Derating a

**Power Derating** 

#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



Normalized Thermal Transient Impedance, Junction-to-Ambie

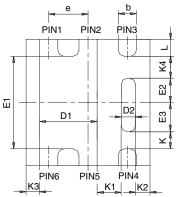
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?68642">www.vishay.com/ppg?68642</a>.





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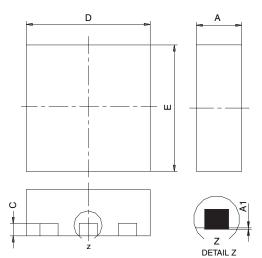
# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

	SINGLE PAD						DUAL PAD						
DIM	M	ILLIMETER	RS	INCHES		MILLIMETERS			INCHES				
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
<b>A</b> 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP	ı	0.275 TYP			0.011 TYP			
K1		0.400 TYP	1		0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP	1	0.009 TYP			0.252 TYP			0.010 TYP			
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP	1	0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
=011 0 0		0 00 1											

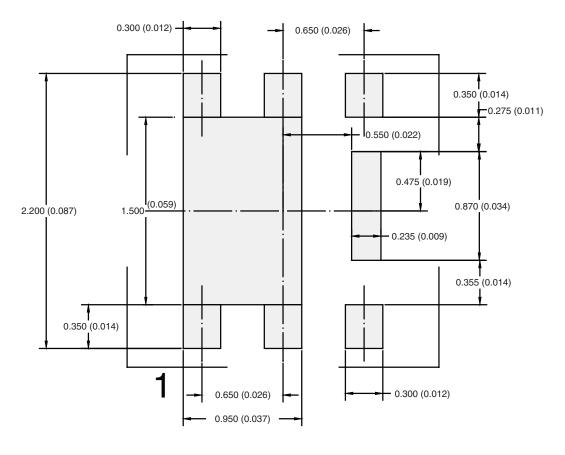
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

Document Number: 73001 06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

Return to Index

ATTLICA ION NO



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Vishay

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