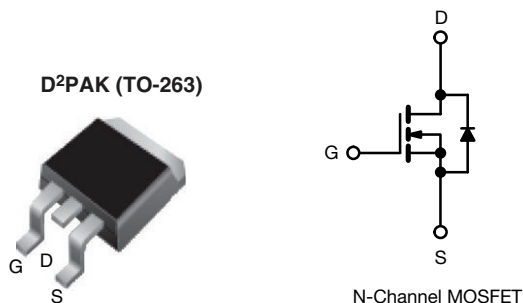


Power MOSFET

PRODUCT SUMMARY

| | | |
|--------------------------|------------------------|------|
| V _{DS} (V) | 60 | |
| R _{DS(on)} (Ω) | V _{GS} = 10 V | 0.10 |
| Q _g max. (nC) | 25 | |
| Q _{gs} (nC) | 5.8 | |
| Q _{gd} (nC) | 11 | |
| Configuration | Single | |



FEATURES

- Advanced process technology
- Surface mount (IRFZ24S, SiHFZ24S)
- 175 °C operating temperature
- Fast switching
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the last lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

| | | |
|---------------------------------|-----------------------------|-----------------------------|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) |
| Lead (Pb)-free and Halogen-free | SiHFZ24S-GE3 | SiHFZ24STRR-GE3 |
| Lead (Pb)-free | IRFZ24SPbF | IRFZ24STRRPbF |
| | - | IRFZ24STRLPbF |

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|-----------------------------------|-------------------------|------|
| Drain-Source Voltage | V _{DS} | 60 | V |
| Gate-Source Voltage | V _{GS} | ± 20 | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 25 °C | A |
| | | T _C = 100 °C | |
| Pulsed Drain Current ^{a, e} | I _{DM} | 68 | |
| Linear Derating Factor | | 0.40 | W/°C |
| Single Pulse Avalanche Energy ^{b, e} | E _{AS} | 100 | mJ |
| Maximum Power Dissipation | P _D | T _C = 25 °C | W |
| | | T _A = 25 °C | |
| Peak Diode Recovery dV/dt ^{c, e} | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | -55 to +175 | °C |
| Soldering Recommendations (Peak temperature) ^d | for 10 s | 300 | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 400 μH, R_g = 25 Ω, I_{AS} = 17 A (see fig. 12).
- I_{SD} ≤ 17 A, dI/dt ≤ 140 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.
- Uses IRFZ24, SiHFZ24 data and test conditions.


**THERMAL RESISTANCE RATINGS**

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|--|------------|------|------|------|
| Maximum Junction-to-Ambient (PCB mounted, steady-state) ^a | R_{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 2.5 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------|---|------|-------|-----------|---------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$ | 60 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$ ^c | - | 0.061 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | 25 | μA |
| | | $V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$ ^b | - | - | 0.10 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 25\text{ V}$, $I_D = 10\text{ A}$ ^d | 5.5 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 ^d | - | 640 | - | pF |
| Output Capacitance | C_{oss} | | - | 360 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 79 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^{b, c} | - | - | 25 | nC |
| Gate-Source Charge | Q_{gs} | | - | - | 5.8 | |
| Gate-Drain Charge | Q_{gd} | | - | - | 11 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30\text{ V}$, $I_D = 17\text{ A}$, $R_g = 18\text{ }\Omega$, $R_D = 1.7\text{ }\Omega$, see fig. 10 ^{b, c} | - | 13 | - | ns |
| Rise Time | t_r | | - | 58 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 25 | - | |
| Fall Time | t_f | | - | 42 | - | |
| Internal Source Inductance | L_S | Between lead, and center of die contact | - | 7.5 | - | nH |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 17 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 68 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 17\text{ A}$, $V_{GS} = 0\text{ V}$ ^b | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 17\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$ ^{b, c} | - | 88 | 180 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 0.29 | 0.64 | nC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. Uses IRFZ24/SiHFZ24 data and test conditions.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

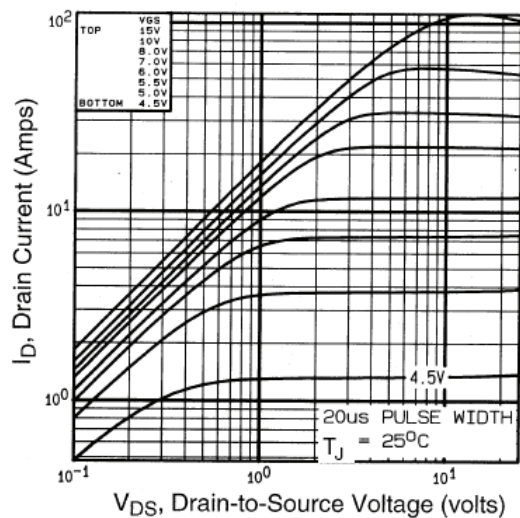


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

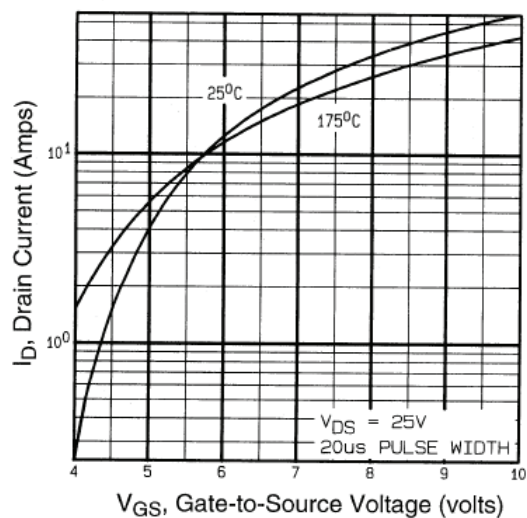


Fig. 3 - Typical Transfer Characteristics

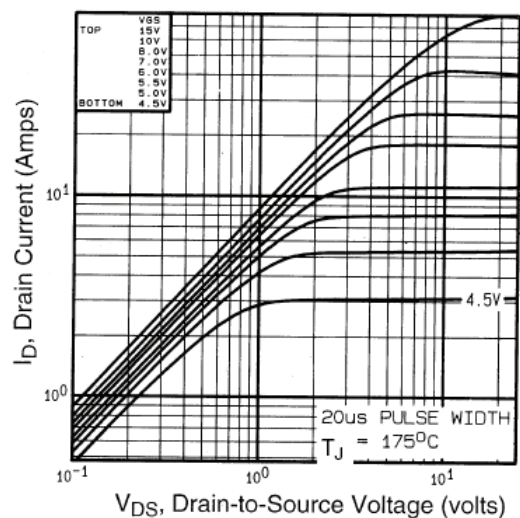


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^{\circ}\text{C}$

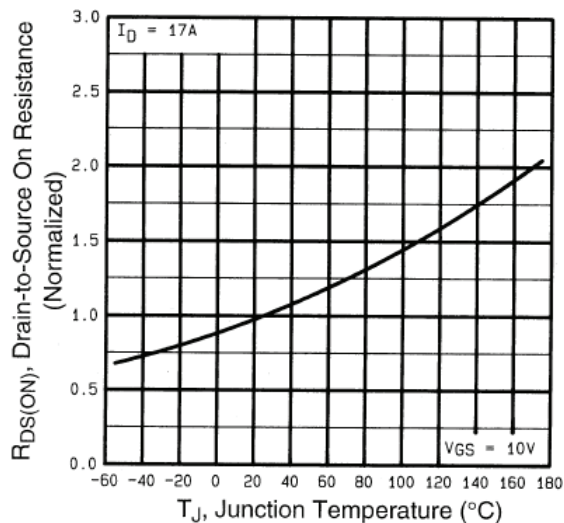
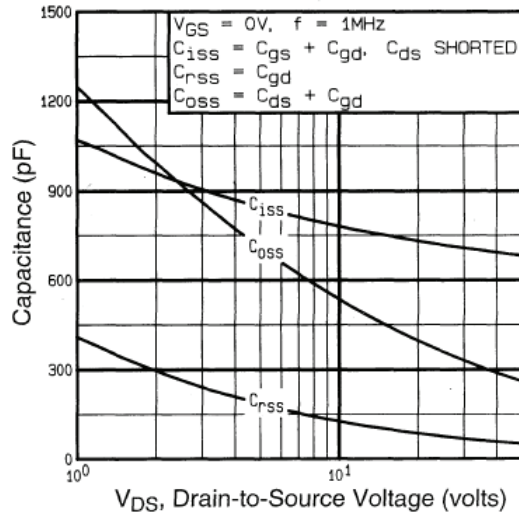
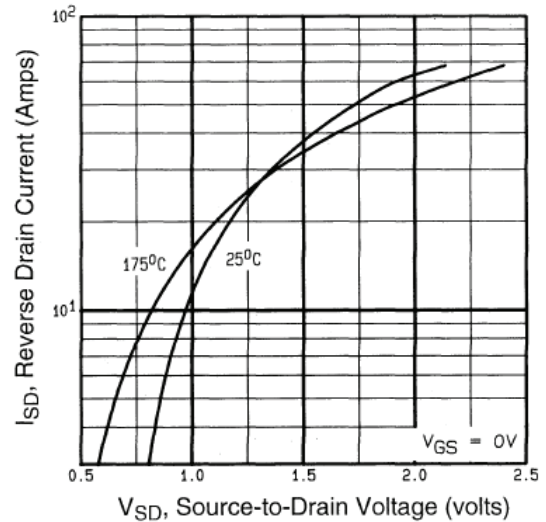
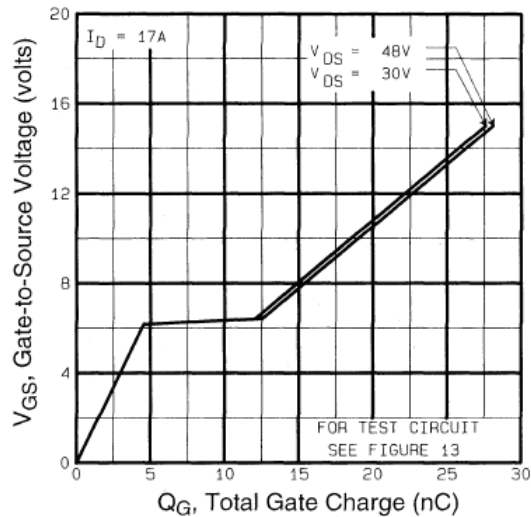
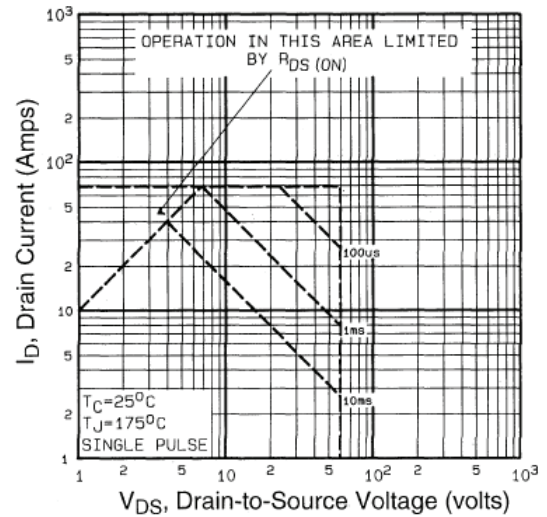


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

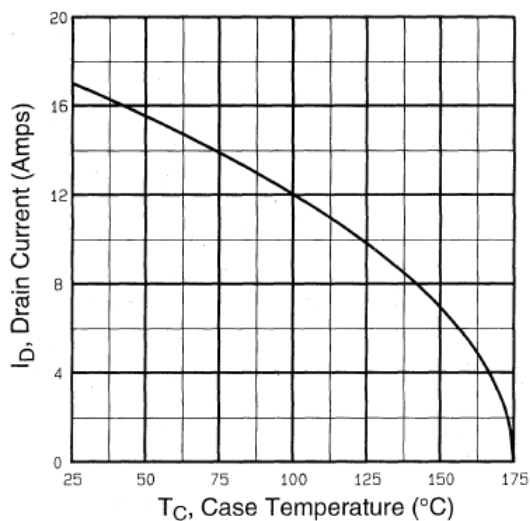
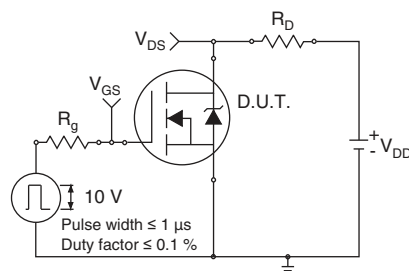
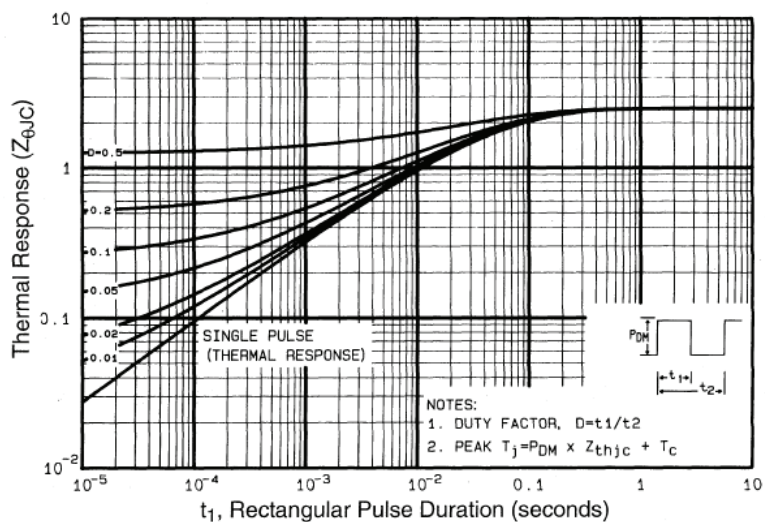
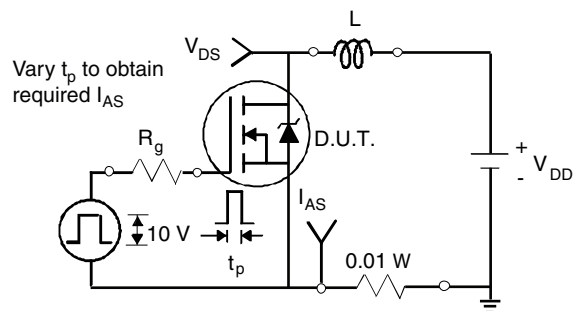
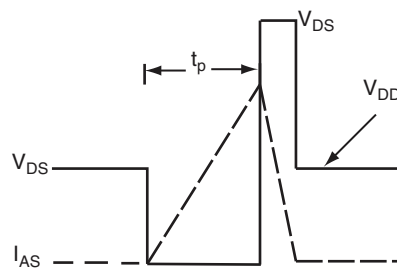

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

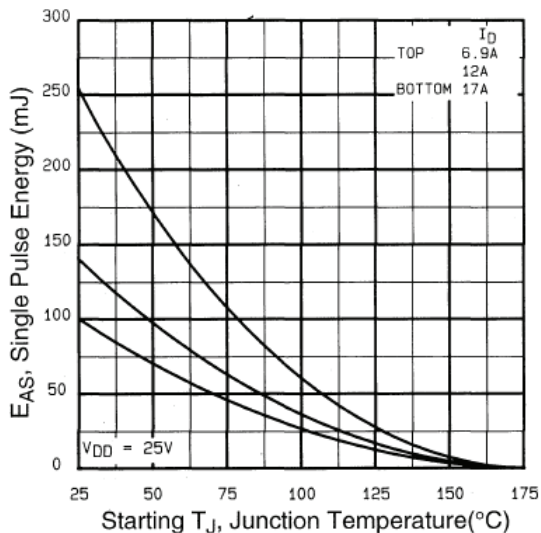


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

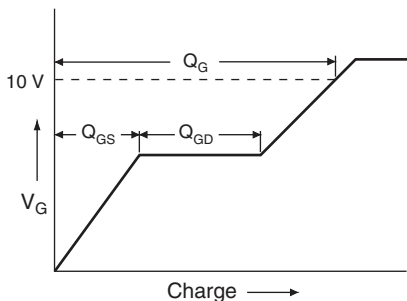


Fig. 13a - Basic Gate Charge Waveform

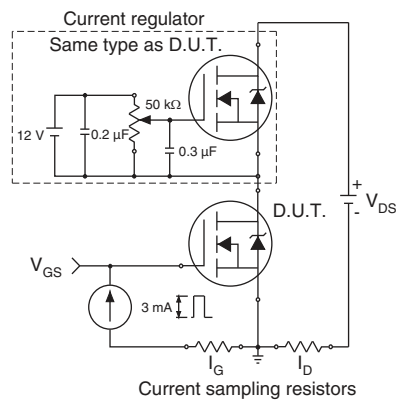
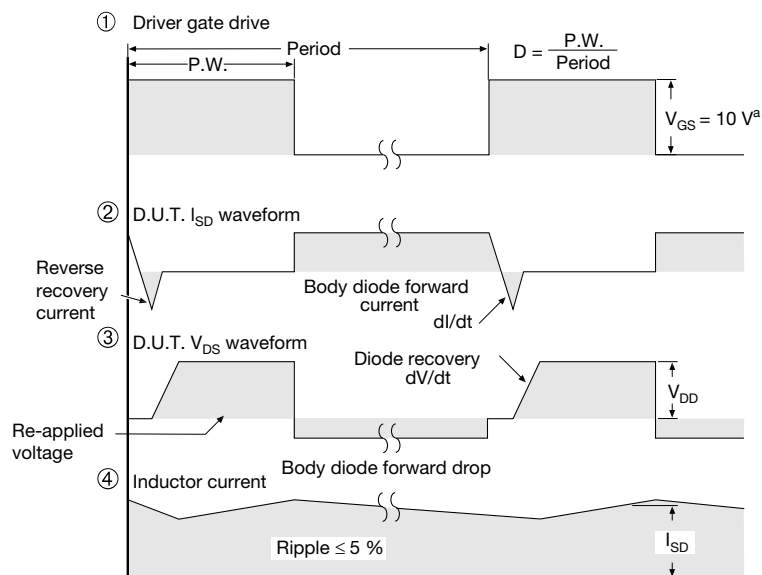
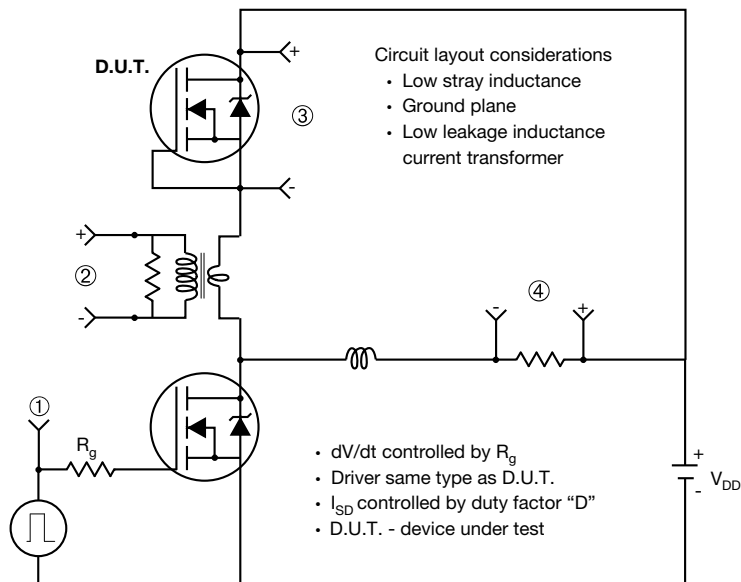


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

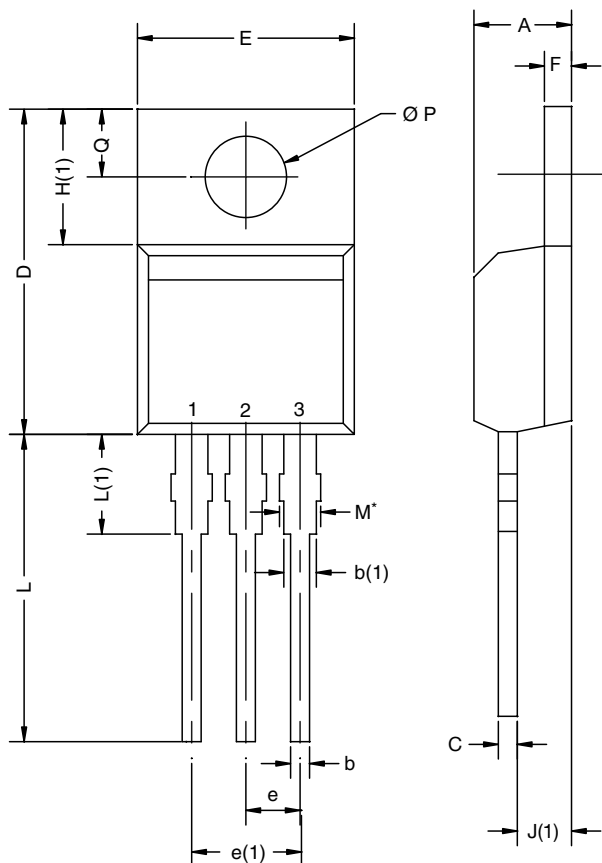
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220AB

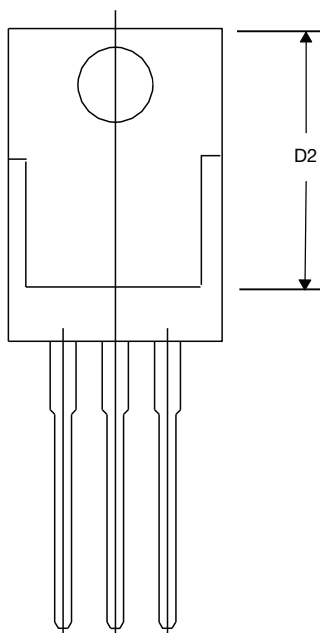


| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.25 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.01 | 0.027 | 0.040 |
| b(1) | 1.20 | 1.73 | 0.047 | 0.068 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.85 | 15.49 | 0.585 | 0.610 |
| D2 | 12.19 | 12.70 | 0.480 | 0.500 |
| E | 10.04 | 10.51 | 0.395 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.09 | 6.48 | 0.240 | 0.255 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.35 | 14.02 | 0.526 | 0.552 |
| L(1) | 3.32 | 3.82 | 0.131 | 0.150 |
| Ø P | 3.54 | 3.94 | 0.139 | 0.155 |
| Q | 2.60 | 3.00 | 0.102 | 0.118 |

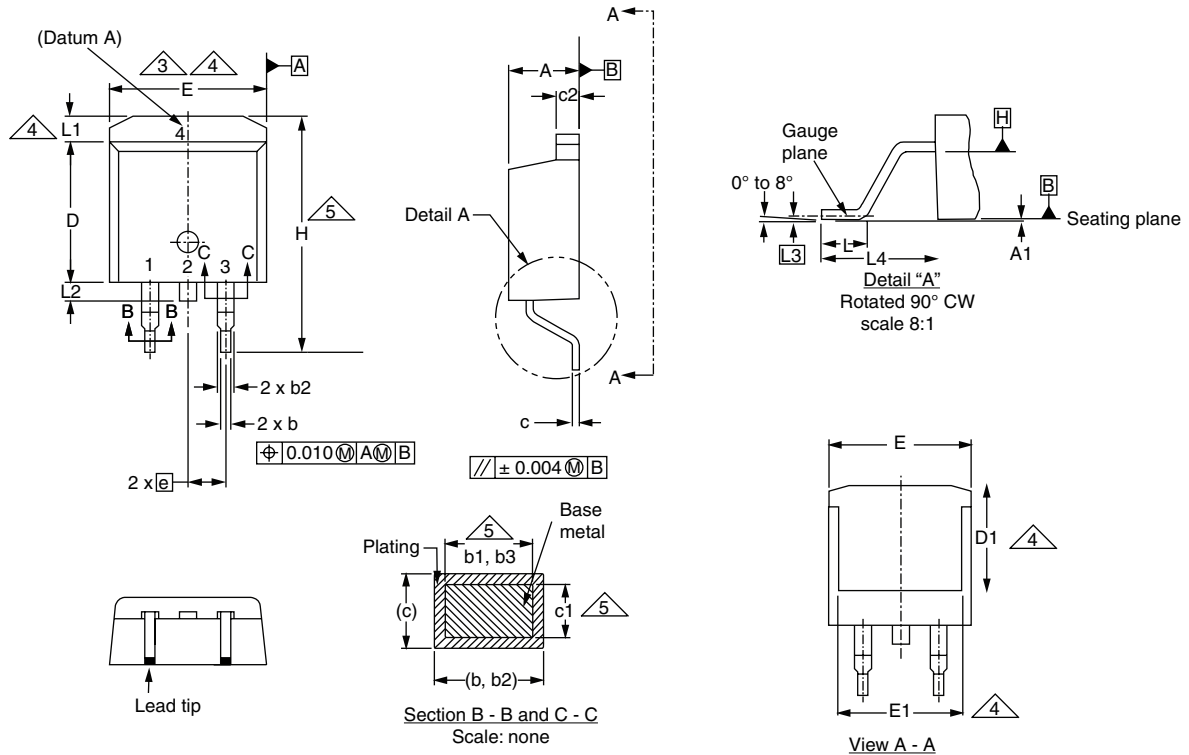
ECN: T14-0413-Rev. P, 16-Jun-14
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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