COMPLIANT

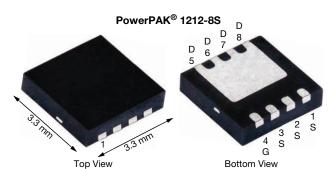
HALOGEN

FREE



Vishay Siliconix

N-Channel 80 V (D-S) MOSFET



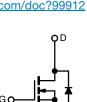
PRODUCT SUMMARY					
V _{DS} (V)	80				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00850				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.01220				
Q _g typ. (nC)	15.2				
I _D (A)	55.5				
Configuration	Single				

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} x Q_g figure-of-merit (FOM)
- Tuned for the lowest R_{DS} x Q_{oss} FOM
- 100 % R_a and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Synchronous rectification
- · Primary side switch
- DC/DC converter
- · Solar micro inverter
- · Motor drive switch
- · Battery and load switch
- Industrial



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS30LDN-T1-GE3
Lead (Pb)-free and halogen-free, BLR and IOL	SiSS30LDN-T1-UE3

PARAMETER Drain-source voltage		SYMBOL	LIMIT	UNIT	
		V_{DS}	80	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		55.5		
	T _C = 70 °C	1 . [44		
	T _A = 25 °C	l _D	16 ^{b, c}		
	T _A = 70 °C	†	12.6 ^{b, c}		
Pulsed drain current (t = 100 µs)		I _{DM}	120	A	
Continuous anno durin dia de comont	T _C = 25 °C		51.8		
Continuous source-drain diode current	T _A = 25 °C	I _S	4.3 b, c		
Single pulse avalanche current		I _{AS}	20		
Single pulse avalanche energy L = 0.1 mH		E _{AS}	20	mJ	
	T _C = 25 °C		57		
Maximum power dissipation	T _C = 70 °C	T , [36	w	
	T _A = 25 °C	P _D	4.8 ^{b, c}	VV	
	T _A = 70 °C		3 b, c		
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATI	NGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	21	26	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.7	2.2	

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 70 °C/W
- $T_C = 25 \,^{\circ}C$

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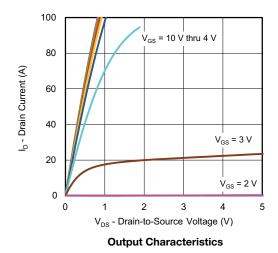
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				<u>'</u>	•	
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	64	-	1400
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-4.6	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	-	2.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA
		V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α
	= (0.1)	V _{GS} = 10 V, I _D = 10 A	-	0.00705	0.00850	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10 A	-	0.00980	0.01220	Ω
Forward transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	_	37	-	S
Dynamic ^b	313					
Input capacitance	C _{iss}		-	2070	_	
Output capacitance	C _{oss}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	205	-	pF
Reverse transfer capacitance	C _{rss}	-		14	-	i .
-		$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	32.5	50	
Total gate charge	Q_g		-	15.2	23	
Gate-source charge	Q_{gs}	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	6.7	-	nC
Gate-drain charge	Q _{gd}		-	3.9	-	
Output charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V	-	27	-	
Gate resistance	R_g	f = 1 MHz	0.3	0.82	1.5	Ω
Turn-on delay time	t _{d(on)}		-	10	20	
Rise time	t _r	V_{DD} = 40 V, R_L = 4 Ω , I_D \cong 10 A,	-	6	12	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	26	52	
Fall time	t _f		-	6	12	ns
Turn-on delay time	t _{d(on)}		-	21	42	113
Rise time	t _r	V_{DD} = 40 V, R_L = 4 $\Omega,I_D\cong$ 10 A,	-	25	50	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	28	56	
Fall time	t _f		-	8	16	
Drain-Source Body Diode Characterist	ics		_	_		
Continuous source-drain diode current	I _S	$T_C = 25 ^{\circ}C$	-	-	51.8	Α
Pulse diode forward current	I _{SM}		-	-	120	
Body diode voltage	V _{SD}	$I_S = 5 A, V_{GS} = 0 V$	-	0.77	1.1	V
Body diode reverse recovery time	t _{rr}		-	35	76	ns
Body diode reverse recovery charge	Q _{rr}	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	49	98	nC
Reverse recovery fall time	t _a	T _J = 25 °C	-	27	-	ns
Reverse recovery rise time	t _b		-	11	-	113

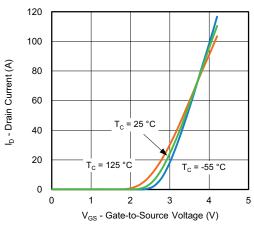
Notes

- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

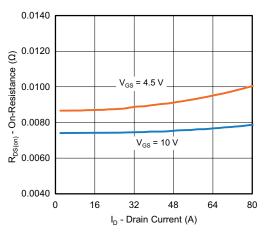
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

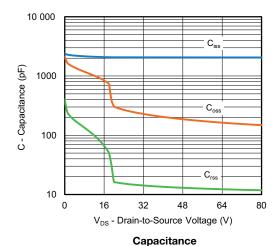




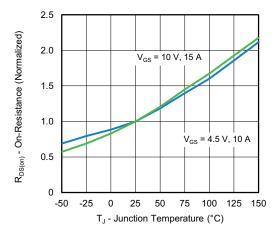


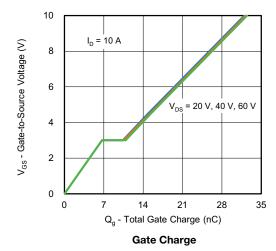






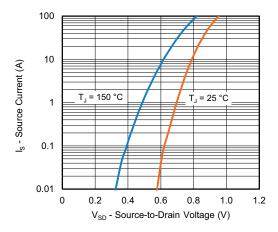
On-Resistance vs. Drain Current and Gate Voltage



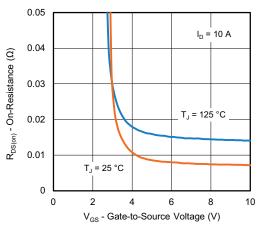


On-Resistance vs. Junction Temperature

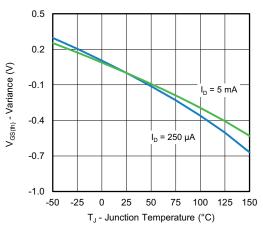




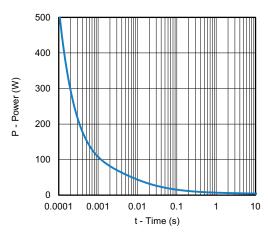
Source-Drain Diode Forward Voltage



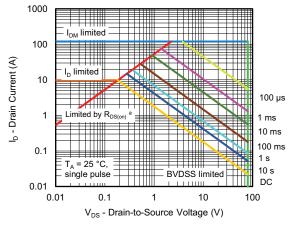
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

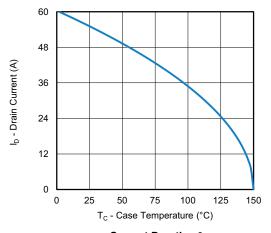


Safe Operating Area, Junction-to-Ambient

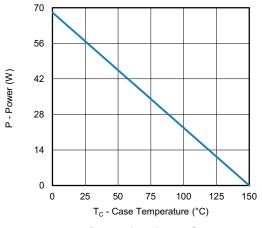
Note

a. $V_{GS} > minimum V_{GS}$ at which $R_{DS(on)}$ is specified

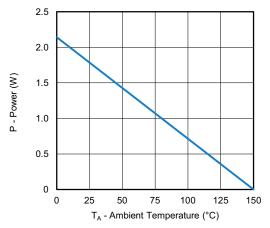




Current Derating a



Power, Junction-to-Case

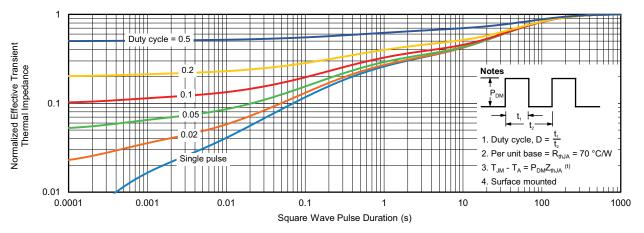


Power, Junction-to-Ambient

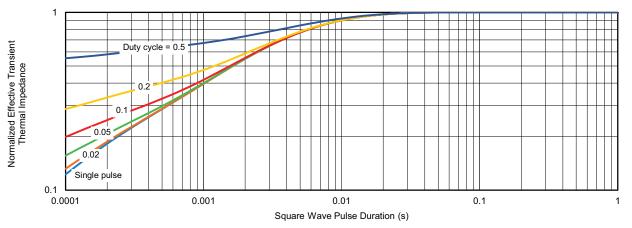
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79691.





Case Outline for PowerPAK® 1212-8S





DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.67	0.75	0.83	0.026	0.030	0.033	
A1	0.00	-	0.05	0.000	-	0.002	
A3		0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.15	2.25	2.35	0.085	0.089	0.093	
E	3.20	3.30	3.40	0.126	0.130	0.134	
E1	1.60	1.70	1.80	0.063	0.067	0.071	
е		0.65 bsc.			0.026 bsc.		
K		0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.			
L	0.33	0.43	0.53	0.013	0.017	0.021	
Z	0.525 ref.			0.021 ref.			

ECN: C20-0862-Rev. B, 20-Jul-2020

DWG: 6008



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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