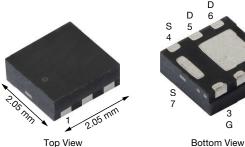
www.vishay.com

Vishay Siliconix

## Automotive P-Channel 60 V (D-S) 175 °C MOSFET

### PowerPAK® SC-70W-6L Single



Mar

## **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R<sub>a</sub> and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





HALOGEN FREE

Marking Code: Q8XXXX		
PRODUCT SUMMARY		G 🖳
V <sub>DS</sub> (V)	-60	]
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.1550	
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.2130	]
I <sub>D</sub> (A)	-6.46	D
Configuration	Single	P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA411CEJW (for detailed order number please see <a href="https://www.vishay.com/doc?79776">www.vishay.com/doc?79776</a> )

<b>ABSOLUTE MAXIMUM RATIN</b>	<b>GS</b> (T <sub>C</sub> = 25 °C, unles	s otherwise noted	)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	-60	V	
Gate-source voltage		V <sub>GS</sub>	± 20	V	
Continuous dusin suurent	T <sub>C</sub> = 25 °C		-6.46		
Continuous drain current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-3.73		
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	-9	Α	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	-20		
Single pulse avalanche current		I <sub>AS</sub>	-14		
Single pulse avalanche energy  L = 0.1 mH		E <sub>AS</sub>	9.8	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C	D	13.6	W	
	T <sub>C</sub> = 125 °C	$P_{D}$	4.5		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175		
Soldering recommendations (peak temperature) d, e		-	260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	$R_{thJA}$	90	°C/W
Junction-to-case (drain)		$R_{thJC}$	11	C/VV

#### Notes

- a. Package limited
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %
- c. When mounted on 1" square PCB (FR4 material)
- See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	0 V, I <sub>D</sub> = -250 μA	-60	-	-	V	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-1.5	-2.0	-2.5	V	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = -60 V	-	-	-1		
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = -60 V, T <sub>J</sub> = 125 °C	-	-	-50	μΑ	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -60 V, T <sub>J</sub> = 175 °C	-	-	-250		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≥ -5 V	-6	-	-	Α	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A	-	0.1255	0.1550		
Drain acurae an etate	В	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 125 °C	-	-	0.2639		
Drain-source on-state resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -3.5 A, T <sub>J</sub> = 175 °C	-	-	0.3261 45 0.2130 - S 1 590 90 p	1 12	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -3 A	-	0.1645	0.2130	-	
Forward transconductance b	9fs	V <sub>DS</sub> =	-15 V, I <sub>D</sub> = -3.5 A	-	6	-	S	
Dynamic <sup>b</sup>								
Input capacitance	C <sub>iss</sub>			-	421	590		
Output capacitance	Coss	$V_{GS} = 0 V$	V <sub>DS</sub> = -25 V, f = 1 MHz	-	64	90	pF	
Reverse transfer capacitance	C <sub>rss</sub>	1		-	35	50		
Total gate charge <sup>c</sup>	Qg			-	10.2	15.5		
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	$V_{DS} = -30 \text{ V}, I_D = -6.5 \text{ A}$	-	2.2	-	nC	
Gate-drain charge <sup>c</sup>	$Q_{gd}$	1		-	2.6	-		
Gate resistance	$R_g$		f = 1 MHz	2.50	5.18	7.80	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	7	12		
Rise time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> =	-30 V, R <sub>I</sub> = 12 Ω	-	4	7	ns	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -2.5 \text{ A},$	$V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	17	29		
Fall time <sup>c</sup>	t <sub>f</sub>	1		-	4	7		
Source-Drain Diode Ratings and Charact	eristics <sup>b</sup>				•			
Pulsed current a	I <sub>SM</sub>			-	-	-20	Α	
Forward voltage	$V_{SD}$	I <sub>F</sub> = ·	-3.5 A, V <sub>GS</sub> = 0 V	-	-0.88	-1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>			-	24	48	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	- I <sub>F</sub> = -2 A, di/dt = 100 A/μs		-	28	56	nC	
Reverse recovery fall time	ta			-	21	-		
Reverse recovery rise time	t <sub>b</sub>			-	3	-	ns	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3.4	-	Α	

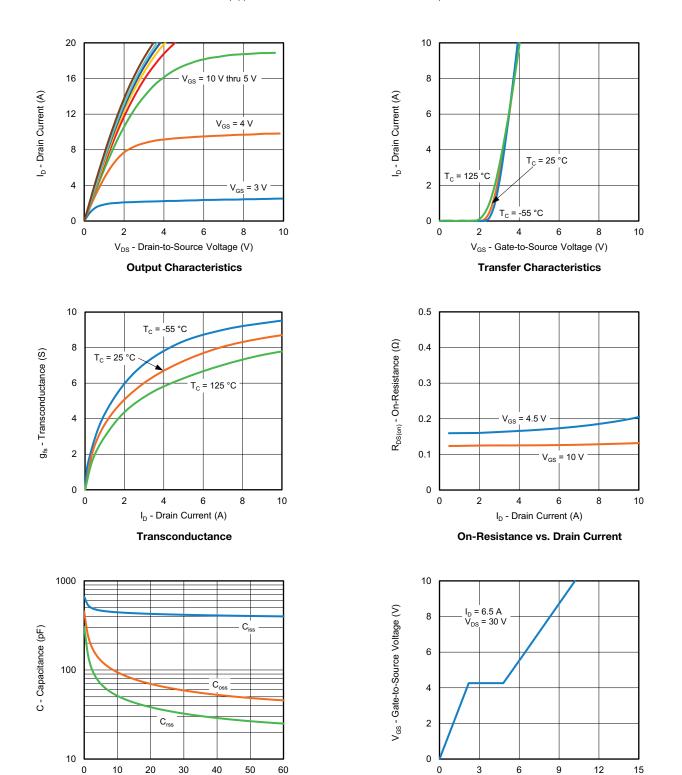
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Q<sub>q</sub> - Total Gate Charge (nC)

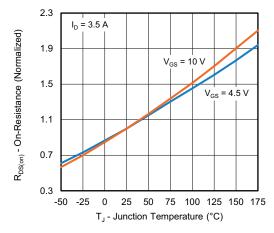
**Gate Charge** 

V<sub>DS</sub> - Drain-to-Source Voltage (V)

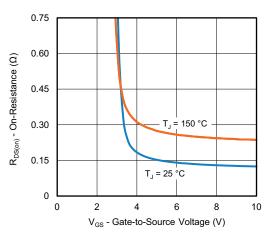
Capacitance



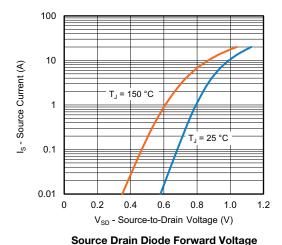
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



1.0

0.7  $I_D = -250 \,\mu\text{A}$   $I_D = -5 \,\text{mA}$ 

25 50 75

-0.2

-0.5

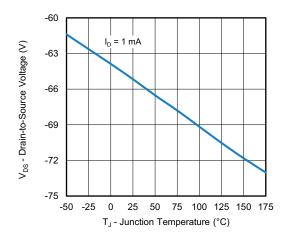
-50 -25

T<sub>J</sub> - Junction Temperature (°C)

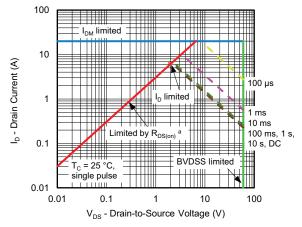
Threshold Voltage

100 125

150 175



**Drain Source Breakdown vs. Junction Temperature** 



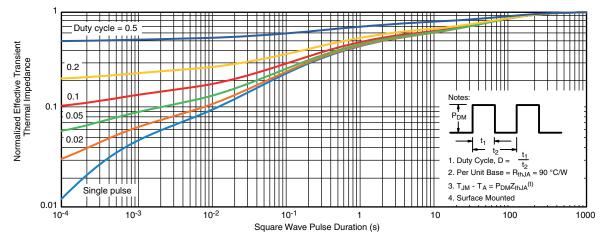
Safe Operating Area

### Note

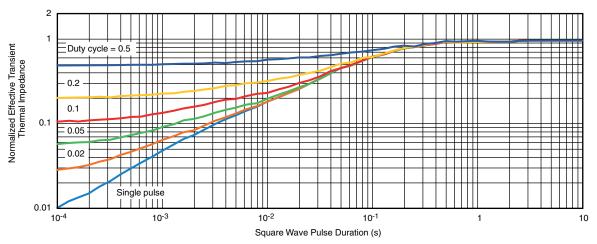
a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



### Normalized Thermal Transient Impedance, Junction-to-Ambient

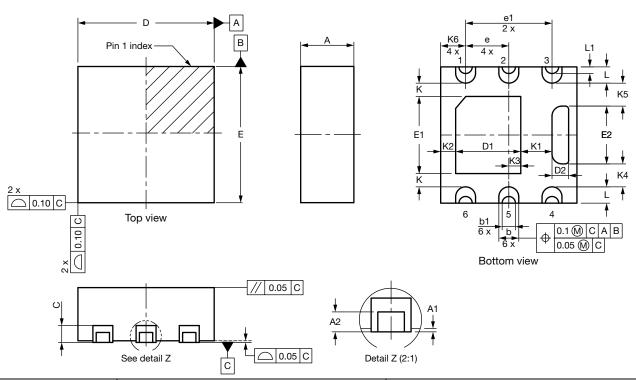


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?63171">www.vishay.com/ppg?63171</a>.



# PowerPAK® SC70W-6L SIDEWETTABLE



DIM.		MILLIMETERS			INCHES		
Dilvi.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.70	0.80	0.90	0.027	0.031	0.035	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
A2	0.10	-	-	0.004	-	-	
b	0.25	0.30	0.35	0.010	0.012	0.014	
b1	0.15	0.20	0.23	0.006	0.008	0.009	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	1.95	2.05	2.15	0.077	0.081	0.085	
D1	0.88	0.98	1.08	0.035	0.039	0.043	
D2	0.20	0.25	0.30	0.008	0.010	0.012	
Е	1.95	2.05	2.15	0.077	0.081	0.085	
E1	1.06	1.16	1.26	0.042	0.046	0.050	
E2	0.82	0.87	0.92	0.032	0.034	0.036	
е		0.65 BSC		0.026 BSC			
e1		1.30 BSC			0.051 BSC		
K		0.20 typ.			0.008 typ.		
K1		0.47 typ.			0.019 typ.		
K2		0.23 typ.		0.009 typ.			
K3		0.18 typ.			0.007 typ.		
K4		0.35 typ.			0.014 typ.		
K5		0.35 typ.		0.014 typ.			
K6		0.38 typ.		0.015 typ.			
L	0.15	0.25	0.35	0.006	0.010	0.014	
L1	-	0.10	-	-	0.004	-	

## DWG: 6076

**Notes** 

- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating

Revison: 10-Jan-2020 Document Number: 77413



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