COMPLIANT

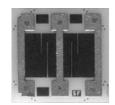
GREEN

(5-2008)





Thin Film, 1010 Center-Tapped Resistor Divider Network on Alumina



Product may not be to scale

The CCC series resistor chips offer good 400 mW power, low shunt capacitance and a center tap feature.

The CCCs nichrome resistor material offers excellent stability. The CCCs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology.

The CCCs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or K.

FEATURES

- Wire bondable
- Larger single size for extended value range
- Resistance range total: 100 Ω to 1 M Ω Custom values: $R_{\rm A}$ or $R_{\rm B}$ 50 Ω to 500 k Ω
- Chip size: 0.100" x 0.100"
- Case: 1010
- Power: 400 mW
- Alumina substrate
- Low stray capacitance: < 0.2 pF
- Resistor material: Nichrome
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

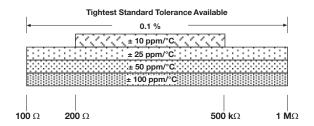
Vishay EFI CCC chip resistors provide excellent high-frequency response and are ideally suited for prototyping.

Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES		
PARAMETER	VALUE	UNIT
Total Resistance Range	100 to 1M	Ω
Standard Tolerances	± 0.1	%
TCR	± 10, ± 25, ± 50, ± 100	ppm/°C

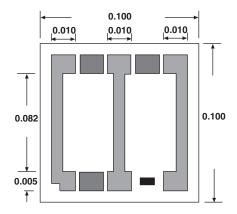


STANDARD ELECTRICAL SPECIFICATIONS		
PARAMETER	VALUE	UNIT
Noise, MIL-STD-202, Method 308	- 20 typ.	dB
Center Tap Ratio, R _A /R _B : Tolerance	1 ± 1	%
Stability, 1000 h, + 125 °C, 400 mW	± 0.1 max. Δ <i>R/R</i>	%
Operating Temperature Range	- 55 to + 125	°C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. ΔR/R	%
High Temperature Exposure, + 150 °C, 100 h	± 0.25 max. ΔR/R	%
Dielectric Voltage Breakdown	400	V
Insulation Resistance	10 ¹² min.	Ω
Operating Voltage	200 max.	V
DC Power Rating at 125 °C	0.4 max.	W
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 max. Δ <i>R/R</i>	%

Revision: 20-Mar-13 Document Number: 61010



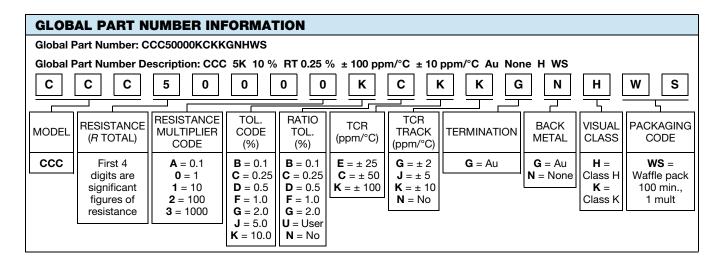
DIMENSIONS in inches



SCHEMATIC

$$R_{T} = R_{A} + R_{B}$$
 R_{A}
 R_{B}

MECHANICAL SPECIFICATIONS	
PARAMETER	VALUE
Chip Size	0.100" x 0.100" ± 0.003" (2.5 mm x 2.5 mm ± 0.08 mm)
Chip Thickness	0.010" ± 0.002" (0.25 mm ± 0.03 mm)
Chip Substrate Material	99.6 % alumina, 2 microinch to 4 microinch finish
Resistor Material	Nichrome
Bonding Pad Size	0.005" x 0.010" (0.12 mm x 0.24 mm) min.
Number of Pads	6
Pad Material	25 kÅ minimum gold standard
Backing	None (Au optional)





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Vishay

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