RoHS

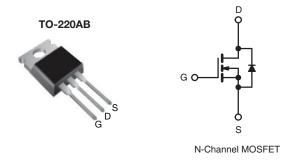
COMPLIANT HALOGEN

FREE

Vishay Siliconix

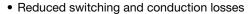
E Series Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	700			
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.6		
Q _g max. (nC)	48			
Q _{gs} (nC)	6			
Q _{gd} (nC)	11			
Configuration	Single			



FEATURES

- Low figure-of-merit (FOM) Ron x Qq
- Low input capacitance (Ciss)



- Ultra low gate charge (Q_q)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

OORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free and Halogen-free	SiHP6N65E-GE3		

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V_{GS}	± 30	v
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C	- I _D	7	
	V _{GS} at 10 V	T _C = 100 °C		5	Α
Pulsed Drain Current ^a			I _{DM}	18	
Linear Derating Factor				0.63	W/°C
Single Pulse Avalanche Energy b			E _{AS}	56	mJ
Maximum Power Dissipation			P _D	78	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	T _J = 125 °C		-1) //-14	37	1//20
Reverse Diode dV/dt ^d		dV/dt	27	- V/ns	
Soldering Recommendations (Peak Temperature) c	for 10 s			300	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 2 A.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, dI/dt = 100 A/ μ s, starting $T_J = 25$ °C.



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.6	C/ VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		-					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		650	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA		-	0.73	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-Source Leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
			$V_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zava Cata Valtaga Dvain Cuwant		V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 520 \	V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3 A	-	0.5	0.6	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 30 V, I _D = 3 A		-	2	-	S
Dynamic		•		•		•	
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	820	-	pF
Output Capacitance	C _{oss}			-	40	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	36	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	117	-	
Total Gate Charge	Q_g			-	24	48	nC
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 3 \text{ A}, V_{DS} = 520 \text{ V}$		6	-	
Gate-Drain Charge	Q _{gd}	1			11	-	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 520 V, I_{D} = 3 A, V_{GS} = 10 V, R_{g} = 9.1 Ω		-	14	28	ns
Rise Time	t _r			-	12	24	
Turn-Off Delay Time	t _{d(off)}			-	30	60	
Fall Time	t _f			-	20	40	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	1.4	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	7	
Pulsed Diode Forward Current	I _{SM}			-	-	18	A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 3 A, V _{GS} = 0 V		-	-	1.3	V
Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 3 \text{ A},$ $dI/dt = 100 \text{ A/µs}, V_R = 25 \text{ V}$		-	237	-	ns
Reverse Recovery Charge	Q _{rr}			-	2.2	-	μC
Reverse Recovery Current	I _{RRM}			_	16	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

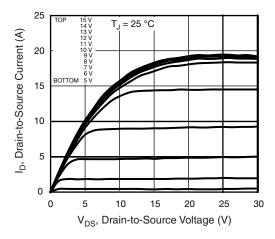


Fig. 1 - Typical Output Characteristics

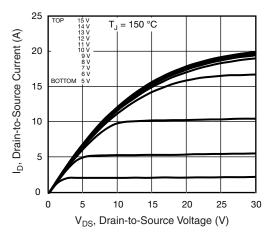


Fig. 2 - Typical Output Characteristics

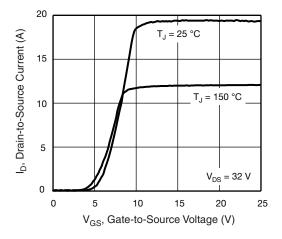


Fig. 3 - Typical Transfer Characteristics

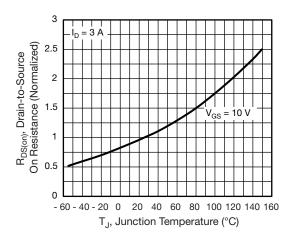


Fig. 4 - Normalized On-Resistance vs. Temperature

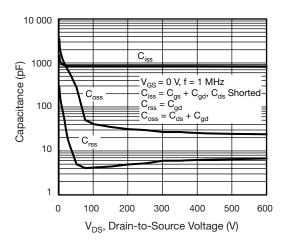


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

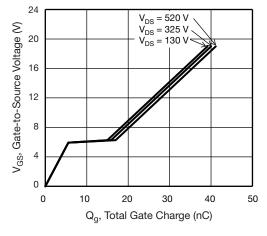


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



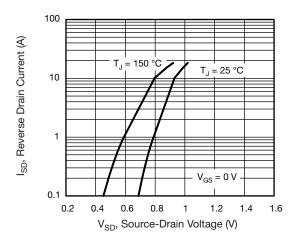


Fig. 7 - Typical Source-Drain Diode Forward Voltage

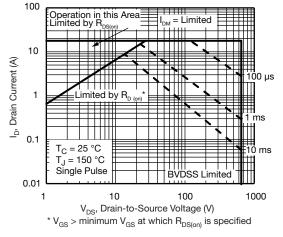


Fig. 8 - Maximum Safe Operating Area

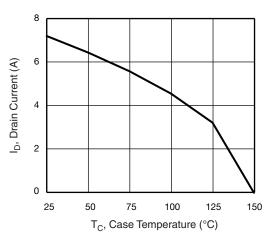


Fig. 9 - Maximum Drain Current vs. Case Temperature

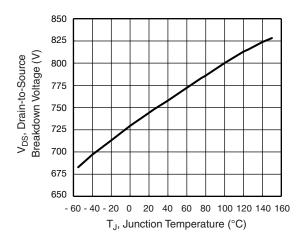


Fig. 10 - Temperature vs. Drain-to-Source Voltage

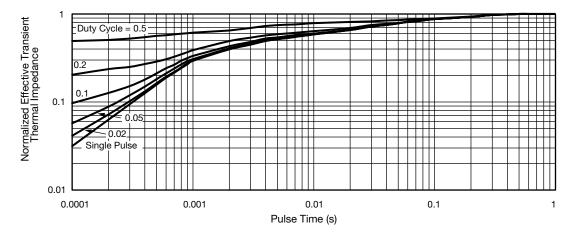


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

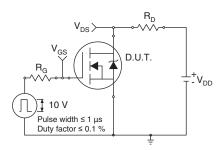


Fig. 12 - Switching Time Test Circuit

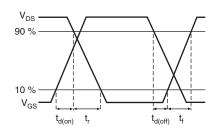


Fig. 13 - Switching Time Waveforms

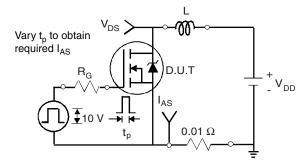


Fig. 14 - Unclamped Inductive Test Circuit

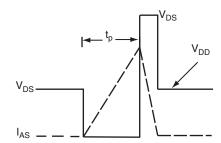


Fig. 15 - Unclamped Inductive Waveforms

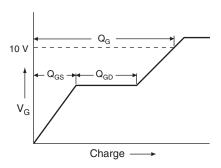


Fig. 16 - Basic Gate Charge Waveform

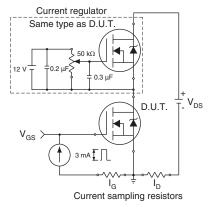
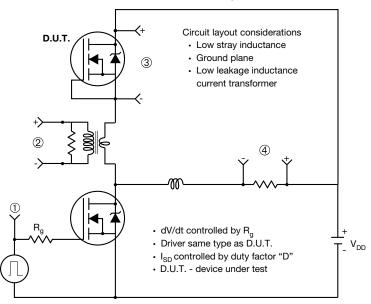


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



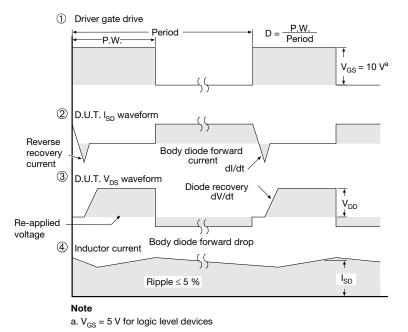


Fig. 18 - For N-Channel

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