

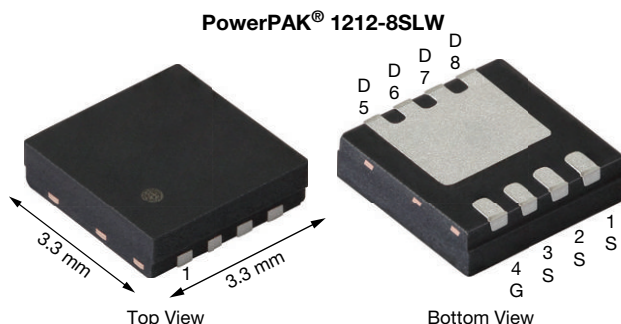
# Automotive P-Channel 80 V (D-S) 175 °C MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

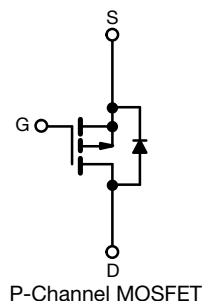
## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



Marking code: Q060

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	-80
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = -10 V	0.0310
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = -4.5 V	0.0480
I <sub>D</sub> (A) <sup>e</sup>	-44
Configuration	Single



ORDERING INFORMATION	
Package	PowerPAK® 1212-8SLW
Lead (Pb)-free and halogen-free	SQS181ELNW (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	-80	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current <sup>e</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-44	A
	T <sub>C</sub> = 125 °C		-25	
Continuous source current (diode conduction) <sup>e</sup>		I <sub>S</sub>	-55	
Pulsed drain current <sup>a, e</sup>		I <sub>DM</sub>	-85	
Single pulse avalanche current		I <sub>AS</sub>	-30.5	
Single pulse avalanche energy		E <sub>AS</sub>	-46	mJ
Maximum power dissipation <sup>a, e</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	119	W
	T <sub>C</sub> = 125 °C		39	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	R <sub>thJA</sub>	54	°C/W
Junction-to-case (drain) <sup>d</sup>		R <sub>thJC</sub>	1.26	

## Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8SLW is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- As per on JESD51-14
- Values based on R<sub>thJC</sub> and T<sub>C</sub> of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = -250 μA		-80	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V	-	-	-10	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -80 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≤ -5 V	-15	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A	-	0.0241	0.0310	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 125 °C	-	-	0.0496	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 175 °C	-	-	0.0593	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -6 A	-	0.0370	0.0480	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -15 A		-	26	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -25 V, f = 1 MHz	-	1979	2771	pF
Output capacitance	C <sub>oss</sub>			-	852	1193	
Reverse transfer capacitance	C <sub>rss</sub>			-	42	59	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -40 V, I <sub>D</sub> = -4 A	-	30	45	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	7	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	4	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.6	1.5	3.0	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -40 V, R <sub>L</sub> = 16 Ω, I <sub>D</sub> ≅ -2.5 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	13	20	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	3	6	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	29	44	
Fall time <sup>c</sup>	t <sub>f</sub>			-	20	30	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-85	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -10 A, V <sub>GS</sub> = 0		-	-0.82	-1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -3.5 A, di/dt = 100 A/μs		-	33	66	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	36	72	nC
Reverse recovery fall time	t <sub>a</sub>			-	18	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	15	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-2.1	-	A

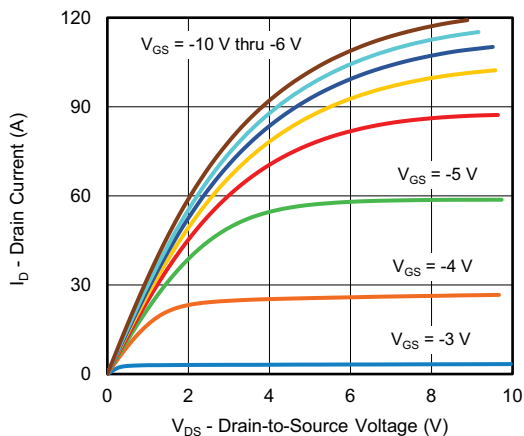
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

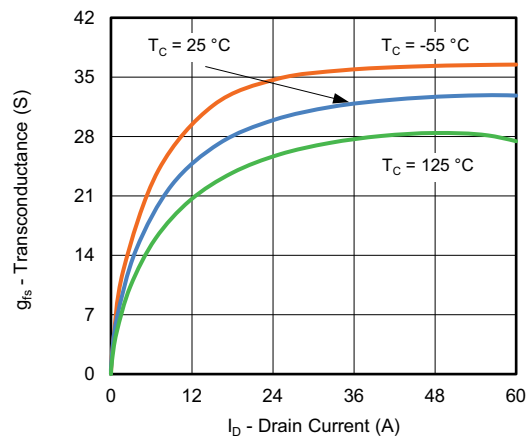
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



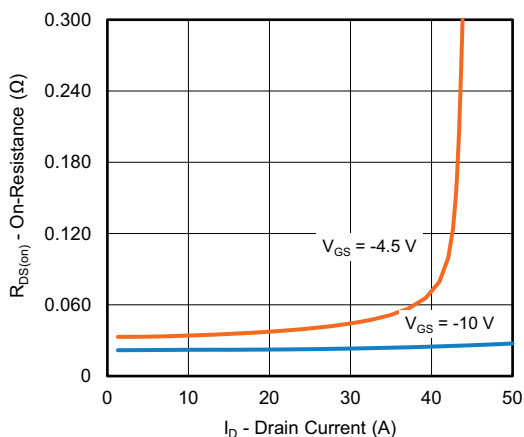
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



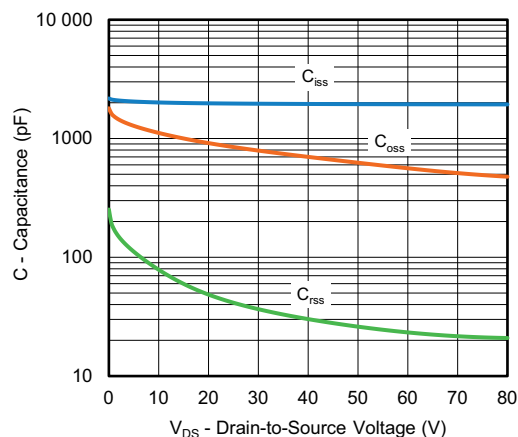
**Output Characteristics**



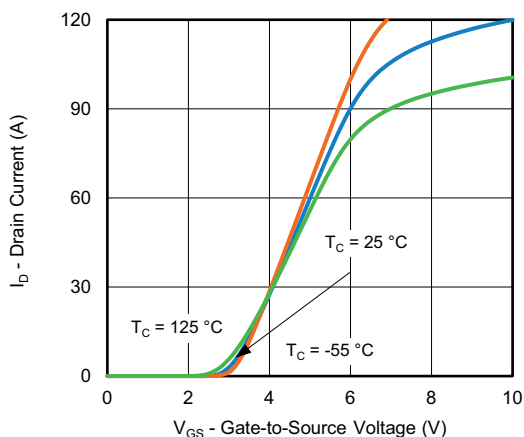
**Transconductance**



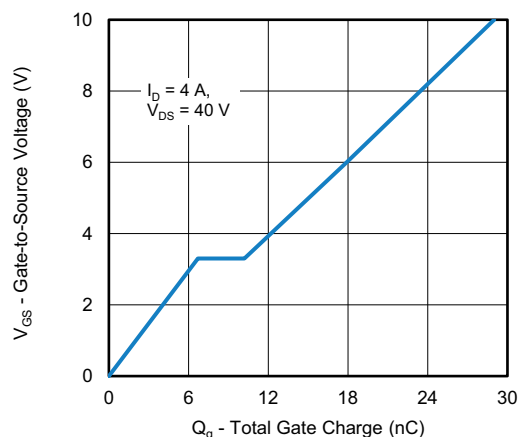
**On-Resistance vs. Drain Current**



**Capacitance**



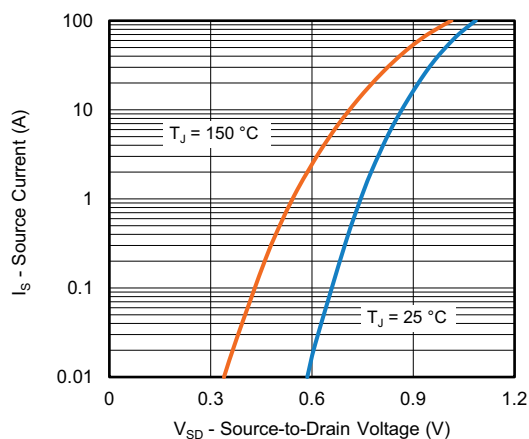
**Transfer Characteristics**



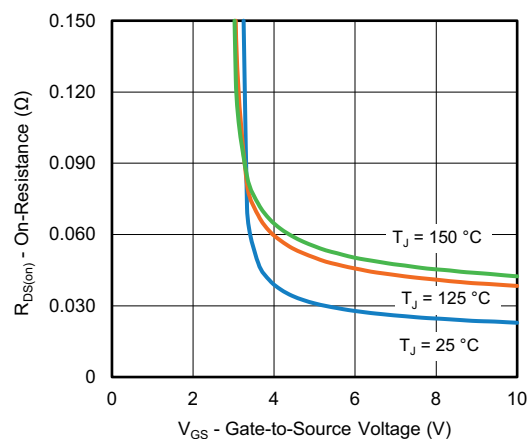
**Gate Charge**



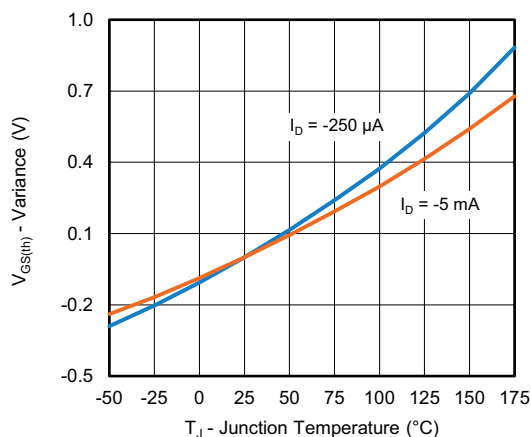
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



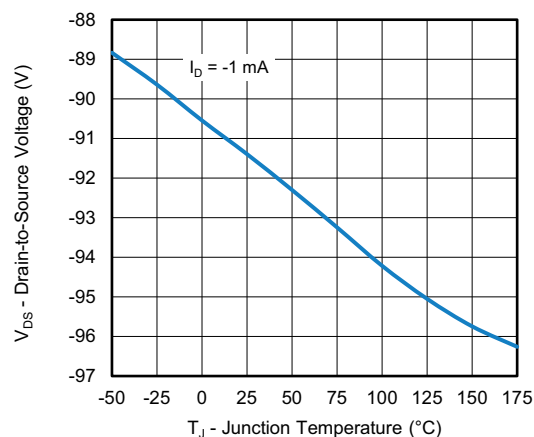
Source Drain Diode Forward Voltage



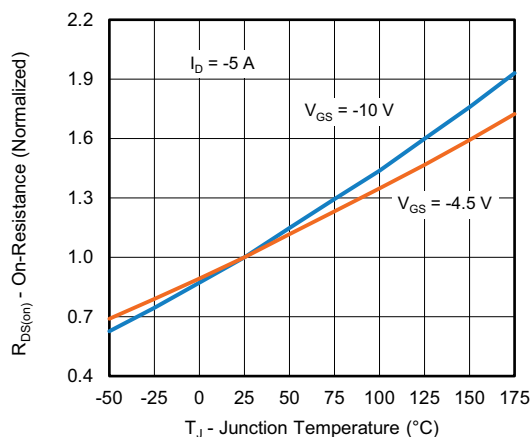
On-Resistance vs. Gate-to-Source Voltage



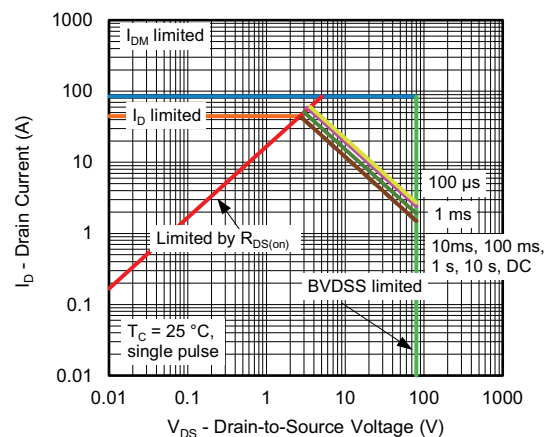
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature



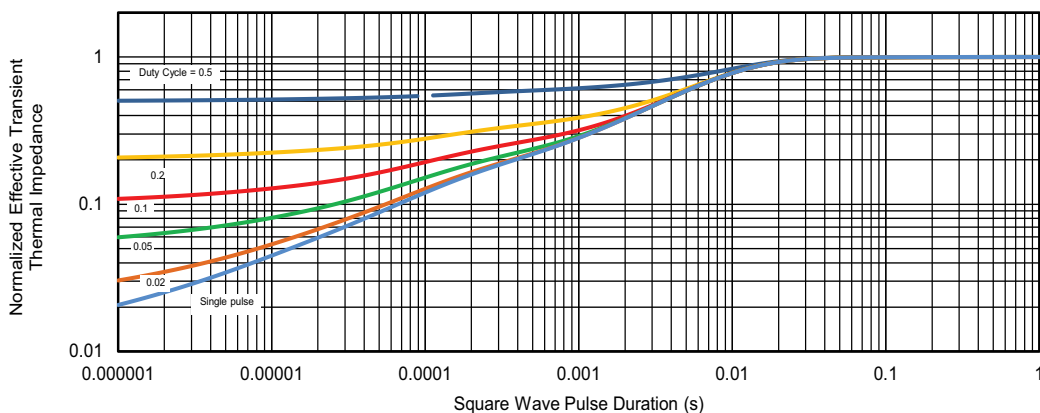
Safe Operating Area

**Note**

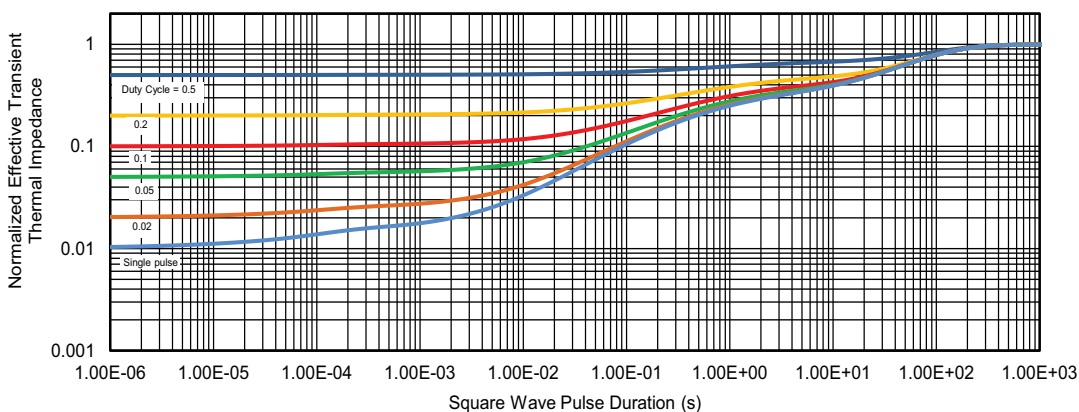
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**



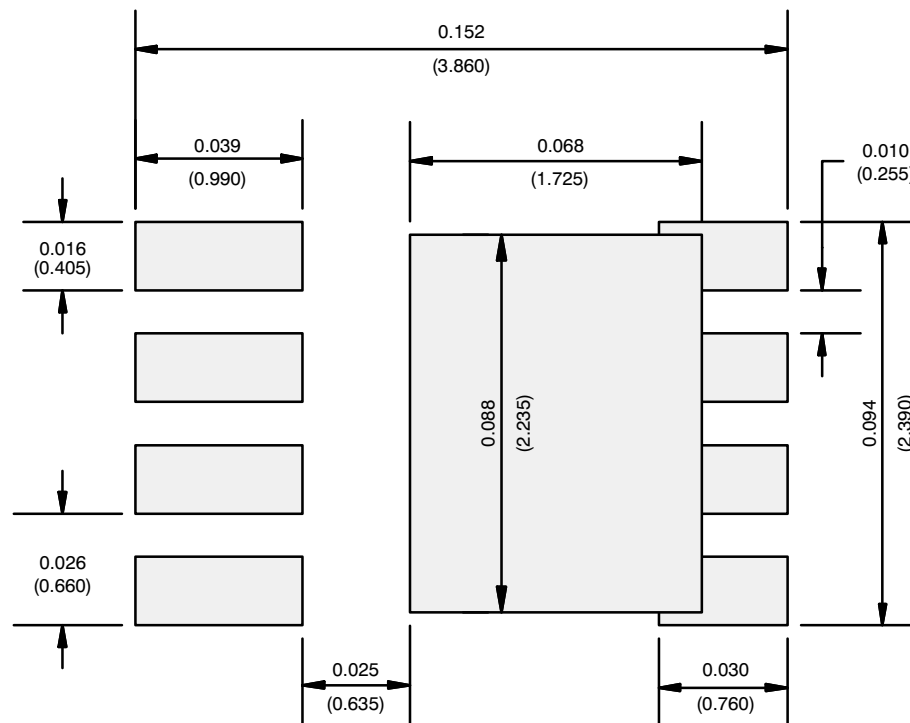
**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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