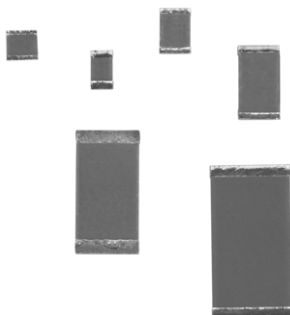


ESCC 4001/026 Qualified (Ⓒ) High Stability Thick Film Resistor Chips



FEATURES

- SMD wraparound chip resistor
- Generic specification ESCC 4001
- Detailed specification ESCC 4001/026
- Robust terminations
- Large ohmic value range 1 Ω to 10 MΩ
- HCHP option 0.55: For high frequency applications (up to 10 GHz)
- ESA (Ⓒ) qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

**HALOGEN
FREE**

LINKS TO ADDITIONAL RESOURCES



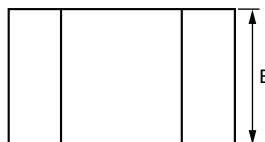
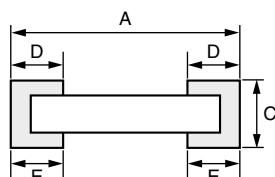
Vishay Sfernice thick film chip resistors CHPHR are specially designed to meet the requirements of the ESA 4001/026 specification. They have undergone the CNES evaluation (Space French National Agency). They are in level 1 of the ESA EPPL (European Preferred Part List) and ESA qualification is on-going.

Thin film technology terminations, with nickel barrier, are very convenient for high operating conditions. They can withstand thousands of very severe thermal shocks.

B (W/A) type is for solder reflow assembly (variant 01 to 05)

G (W/A) type is for gluing (variant 06 to 10)

DIMENSIONS in millimeters



VARIANT NUMBER	STYLE	DIMENSIONS in millimeters									
		A		B		C		D		E	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
01, 06	0603	1.36	1.68	0.72	0.98	0.38	0.53	0.17	0.51	0.25	0.51
02, 07	0805 ⁽¹⁾	1.75	2.07	1.14	1.4	0.38	0.53	0.17	0.51	0.25	0.51
03, 08	1206	2.89	3.21	1.47	1.73	0.38	0.53	0.17	0.51	0.25	0.51
04, 09	2010	4.92	5.24	2.41	2.67	0.5	0.63	0.25	0.64	0.25	0.64
05, 10	2512	6.19	6.51	2.93	3.32	0.5	0.63	0.25	0.64	0.25	0.64

Note

⁽¹⁾ Model CHPHR0805 being same size than case 0705 with same performances, only codification of CHPHR0805 remains

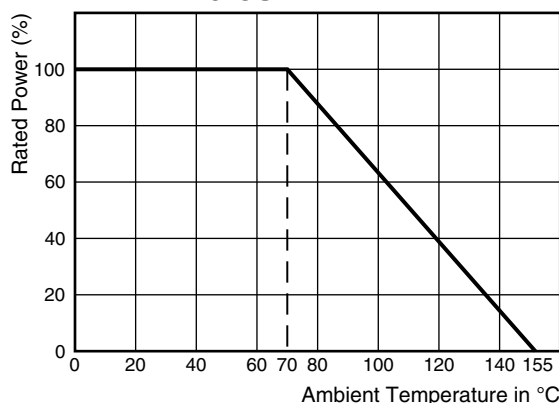
MECHANICAL SPECIFICATIONS	
Substrate	Alumina
Technology	Thick film (Ruthenium oxyde)
Protection	Epoxy coating
Terminations	B (W/A): SnPb over nickel barrier for solder reflow G (W/A) type: gold over nickel barrier for gluing

CHIPS FOR HIGH FREQUENCY APPLICATIONS

High frequency option available up to 10 GHz

3 sizes: 0603, 0805, 1206

POWER DERATING CURVE



SUGGESTED LAND PATTERN (please refer to IPC-7351A)


CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0603	2.38	0.34	0.98
0805	2.77	0.73	1.40
1206	3.91	1.87	1.73
2010	5.94	3.64	2.67
2512	7.21	4.91	3.32

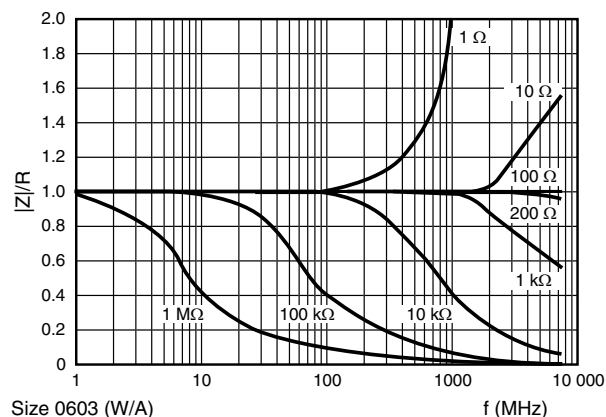
PACKAGING

Waffle-pack or tape and reel when specified

SIZE	NUMBER OF PIECES PER PACKAGE		TAPE WIDTH
	WAFFLE PACK 2" x 2"	TAPE AND REEL (1)	
		MIN.	MAX.
0603	100	100	5000
0805			4000
1206	140		2000
2010	60		
2512	45		12 mm

Note

(1) MOQ for tape and reel: 50 pieces

TYPICAL HF PERFORMANCE OF HCHP

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE (1) R_n Ω	POWER RATING (1) W	TOLERANCE (2) $\pm \%$	TEMPERATURE COEFFICIENT (2) $(\pm 10^{-6}/^{\circ}\text{C})$	CRITICAL RESISTANCE $k\Omega$	TERMINAL MATERIAL AND FINISH
CHPHR	0603	1 to 10M	0.1	1, 2, 5	100, 200	25	E4
CHPHR	0805	1 to 10M	0.2	1, 2, 5	100, 200	50	E4
CHPHR	1206	1 to 10M	0.25	1, 2, 5	100, 200	160	E4
CHPHR	2010	1 to 10M	0.5	1, 2, 5	100, 200	180	E4
CHPHR	2512	1 to 10M	0.8	1, 2, 5	100, 200	112.5	E4
CHPHR	0603	1 to 10M	0.1	1, 2, 5	100, 200	25	E2
CHPHR	0805	1 to 10M	0.2	1, 2, 5	100, 200	50	E2
CHPHR	1206	1 to 10M	0.25	1, 2, 5	100, 200	160	E2
CHPHR	2010	1 to 10M	0.5	1, 2, 5	100, 200	180	E2
CHPHR	2512	1 to 10M	0.8	1, 2, 5	100, 200	112.5	E2

Notes

(1) At $T_{amb} \leq +70\ ^{\circ}\text{C}$. For $T_{amb} > +70\ ^{\circ}\text{C}$ derate linearly to 0 W at $T_{amb} = +155\ ^{\circ}\text{C}$

(2) Restrictions might apply depending on ohmic value please refer to Table 1

TABLE 1

RESISTANCE (Ω)	VALUE SERIES	AVAILABLE TOLERANCE ($\pm \%$)	AVAILABLE TEMPERATURE COEFFICIENT ($\pm 10^{-6}/^{\circ}\text{C}$)
$1 \leq R_n < 10$	Any value in the resistance range to 3 significant figures	2, 5	200
$10 \leq R_n < 1\text{M}$		1, 2, 5	100, 200
$R_n \geq 1\text{M}$		2, 5	200



MAXIMUM RATINGS						
CHARACTERISTICS	VARIANT NUMBER	STYLE	SYMBOLS	LIMITS	UNITS	REMARKS
Limiting element voltage	01, 06	0603	U_L	50	V	-
	02, 07	0805		100		
	03, 08	1206		200		
	04, 09	2010		300		
	05, 10	2512		300		
Rated voltage	All	All	U_R	$\sqrt{(P_n \times R_n)}$	V	(1)
Isolation voltage	01, 06	0603	U_i	100	V	-
	02, 07	0805		200		
	03, 08	1206		300		
	04, 09	2010		300		
	05, 10	2512		300		
Operating temperature range	All	All	T_{op}	-65 to +155	°C	T_{amb}
Storage temperature range	All	All	T_{stg}	-65 to +155	°C	-
Soldering temperature	All	All	T_{sol}	+260	°C	(2)
Maximum weight	01, 06	0603		0.002	g	-
	02, 07	0805		0.004		
	03, 08	1206		0.008		
	04, 09	2010		0.026		
	05, 10	2512		0.042		

Notes(1) Shall never exceed limiting element voltage. R_n = rated resistance

(2) Duration 10 s maximum

PERFORMANCE		
TEST	CONDITIONS	LIMITS REQUIRED BY THE ESCC4001/026 SPECIFICATION
Insulation resistance	ESCC4001 § 8.3.1.2 V = 100 V	1000 MΩ
Low temperature electrical measurement	ESCC4001 § 8.3.1.1 TC = 100 ppm/°C TC = 200 ppm/°C	± 0.8 % ± 1.6 %
High temperature electrical measurement	ESCC4001 § 8.3.3 TC = 100 ppm/°C TC = 200 ppm/°C	± 1.36 % ± 2.72 %
Rapid change of temperature	ESCC4001 § 8.8	± 0.25 + (0.05 Ω × 100/ R_n) %
Robustness of terminations	ESCC4001 § 8.11.2	± 0.25 + (0.05 Ω × 100/ R_n) %
Resistance to solder heat	ESCC4001 § 8.12	± 0.5 + (0.05 Ω × 100/ R_n) %
Climatic sequence	ESCC4001 § 8.10	± 1 + (0.05 Ω × 100/ R_n) %
Load life	ESCC4001 § 8.13 1000 h 2000 h	± 1 + (0.05 Ω × 100/ R_n) % ± 1.5 + (0.05 Ω × 100/ R_n) %



GLOBAL PART NUMBER INFORMATION

LIMITED TO 18 DIGITS: if more digits are necessary a codification of some digits might be necessary

C	H	P	H	R	0	6	0	3	K	1	0	0	1	F	B	T	
GLOBAL MODEL		SIZE		TCR		VALUE				TOLERANCE		TERMINATION		PACKAGING			
CHPHR		0603 0805 1206 2010 2512		K = 100 ppm L = 200 ppm		The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. Example: 1R50 = 1.5 Ω 22R1 = 22.1 Ω 3901 = 3900 Ω 1004 = 1 M Ω				F = $\pm 1\%$ G = $\pm 2\%$ J = $\pm 5\%$		B: SnPb over nickel barrier G: gold		For more information see Codification of Packaging table			

GLOBAL PART NUMBER INFORMATION

ESA Part Numbering: 4001026011001F4

4	0	0	1	0	2	6	0	1	1	0	0	1	F	4
DETAILED SPECIFICATION NUMBER			VARIANT NUMBER			RESISTANCE VALUE					TOLERANCE		TEMPERATURE COEFFICIENT	
			01 to 10			The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. Example: 1R50 = 1.5 Ω 22R1 = 22.1 Ω 3901 = 3900 Ω 1004 = 1 MΩ					F = ± 1 % G = ± 2 % J = ± 5 %		4 = 100 ppm 6 = 200 ppm	

Note

- MOQ for tape and reel: 50 pieces

CROSS REFERENCE BETWEEN ESA PART NUMBER AND VISHAY PART NUMBER

ESA PART NUMBER	VISHAY PART NUMBER	EXPLANATIONS				
4001026011001F4	CHPHR0603K1001FB	4001026 = CHPHR	01 = 0603 with B terminations	1001 = 1001 (1 k Ω)	F = F (tol. 1 %)	4 = K (TCR 100 ppm/ $^{\circ}$ C)

CROSS REFERENCE BETWEEN ESA PART NUMBER AND CHPHR PART NUMBER

VARIANT ESA	VISHAY MODELS
01	CHPHR0603/B terminations
02	CHPHR0805/B terminations
03	CHPHR1206/B terminations
04	CHPHR2010/B terminations
05	CHPHR2512/B terminations
06	CHPHR0603/G terminations
07	CHPHR0805/G terminations
08	CHPHR1206/G terminations
09	CHPHR2010/G terminations
10	CHPHR2512/G terminations

**HYPER FREQUENCY OPTION**

Hyper Frequency Option Numbering: HCHP0603K1001FBT55

H	C	H	P	0	6	0	3	K	1	0	0	1	F	B	T	5	5
GLOBAL MODEL	SIZE		TCR	VALUE				TOLERANCE	TERMINATION	PACKAGING	OPTION						
HCHP	0603 0805 1206		K = 100 ppm L = 200 ppm	The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. Example: 1R50 = 1.5 Ω 22R1 = 22.1 Ω 3901 = 3900 Ω 1004 = 1 MΩ				F = ± 1 % G = ± 2 % J = ± 5 %	B: SnPb over nickel barrier G: gold	Blank = waffle pack T = tape and reel	055 = HiRel production						

Note

- MOQ for taping: 50 pieces

CODIFICATION OF PACKAGING

WAFFLE PACK	
W	100 min., 1 mult.
WA	100 min., 100 mult. (available only in size 1206)
PLASTIC TAPE	
T	100 min., 1 mult.
TA	100 min., 100 mult.
TB	250 min., 250 mult.
TC	500 min., 500 mult.
TD	1000 min., 1000 mult.
TE	2500 min., 2500 mult.
TF	Full tape (quantity depending on size of chips)
PAPER TAPE	
PT	100 min., 1 mult.
PA	100 min., 100 mult.
PB	250 min., 250 mult.
PC	500 min., 500 mult.
PD	1000 min., 1000 mult.
PE	2500 min., 2500 mult.
PF	Full tape (quantity depending on size of chips)

CODIFICATION OF OPTIONS ON TWO DIGITS

OPTION	OPTION 2 DIGITS
..	..
0099	99
0100	0A
0101	0B
0102	0C
0103	0D
0104	0E
0105	0F
..	..
0124	0Y
0125	0Z
0126	1A
0127	1B
0128	1C
..	..
0320	8M
0321	8N
0322	8O
0323	8P
0324	8Q
0325	8R
..	..

CODIFICATION OF SIZES

CODE 18	CODE 40
7	02016
8	0302
9	0402
A	0502
B	0505
C	0603
D	0805
E	1005
F	1010
G	1020
H	1206
I	1505
J	2010
K	2208
L	2512
M	22
N	33
O	44
P	55
Q	515
R	48
S	408
T	816
U	914
V	073
W	074
X	100
Y	135
Z	182



TRACEABILITY DEFINITIONS

The two major traceability elements are defined as:

- The primary process lot number named Front End lot (FE lot). One “FE lot” is composed of several wafers issued from the same thin film deposition sequence.
- The date code named Batch Number (BN). The “BN” is defined after completion of the end of production testing sequence.

The lot homogeneity is given by the “FE lot” and not by the “BN”.

According to the applied rules validated by the ESCC through the product qualification, the following situations are agreed:

- Parts coming from different “FE lot” might have the same “BN”.
- A maximum of two different “BN” might be applied to the same “FE lot” to enable the use of overruns from a previous PO.
- Unless requested / approved by the customer the “BN” will be 2 years old maximum.

SPECIFIC TRACEABILITY REQUIREMENTS

The following specific requirements have to be treated as:

- A customer who requires “Lot Homogeneity” has to mention it on the PO as “SINGLE PRODUCTION LOT”.
- A customer who requires “Lot Homogeneity” in addition to a “Single Batch Number” has to mention it on the PO as “SINGLE PRODUCTION LOT AND OPTION R0101”.

END OF PRODUCTION TESTING

Mandatory testing performed at the end of the production process:

- 100 % overload: voltage $\sqrt{(6.25 P_n \times R_n)}$ or $2 U_L$ whichever is less - duration 2 s
- 100 % burn in: 168 h at P_n at 70 °C

OPTIONS

LOT VALIDATION TESTING

For procurement of qualified components, lot validation testing is not required and shall only be performed if specifically stipulated in the purchase order.

For procurement of unqualified components, lot validation testing shall be performed as stipulated in the purchase order. The need for lot validation testing shall be determined by the orderer.

When lot validation testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of chart F4 indicated in the ESA generic specification ESCC 4001. The testing to be performed and the sample size shall be as stipulated in the purchase order. When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the purchase order.

Lot validation testing will be composed of one LVT charges and LVT samples:

Lot validation test charges has to be ordered separately on purchase order.

Lot validation samples have to be ordered separately on purchase order.

FINAL INSPECTION

If requested by the orderer a final inspection can be performed on site.

Final inspection has to be stipulated separately on purchase order.



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