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Vishay Siliconix

# Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0336
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0444
I <sub>D</sub> (A) per leg	23.5
Configuration	Dual
Package	PowerPAK SO-8L

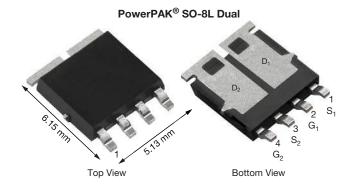
## **FEATURES**

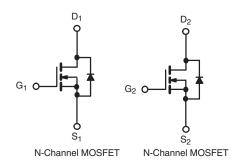
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE





ABSOLUTE MAXIMUM RATINGS	(T <sub>C</sub> = 25 °C, unles	ss otherwise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	$V_{GS}$	± 20	V	
Continuous Drain Current a	T <sub>C</sub> = 25 °C	1	23.5	
Continuous Drain Current "	T <sub>C</sub> = 125 °C	l <sub>D</sub>	13.5	
Continuous Source Current (Diode Conduction	n) <sup>a</sup>	I <sub>S</sub>	23	Α
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	72	
Single Pulse Avalanche Current  L = 0.1 mH		I <sub>AS</sub>	9	
Single Pulse Avalanche Energy	L=0.11IIII	E <sub>AS</sub>	4	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	D	42	W
Waximum Fower Dissipation =	Power Dissipation b $T_C = 125 ^{\circ}C$ $P_D$ 14	VV		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering Recommendations (Peak Temperatu		260		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	85	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	3.5	C/W

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	, v
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1	μА
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.8 A	-	0.0280	0.0336	Ω
Drain Course On State Besistance 8		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.8 A, T <sub>J</sub> = 125 °C	-	-	0.0900	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.8 A, T <sub>J</sub> = 175 °C	-	-	0.1430	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 4.2 A	-	0.0370	0.0444	
Forward Transconductance b	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.8 A		-	16		S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	571	714	
Output Capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$	-	98	123	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	38	48	
Total Gate Charge <sup>c</sup>	Qg			-	12.3	18.5	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 \text{ V}$	$V_{DS} = 30 \text{ V}, I_D = 4.5 \text{ A}$	-	1.9	-	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	2.6	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.3	-	6	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	8	12	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 30 \text{ V, } R_L = 30 \Omega$ $I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 1 \Omega$		-	9	13.5	- ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	19.5	29	
Fall Time <sup>c</sup>	t <sub>f</sub>	]	-	6.5	10		
Source-Drain Diode Ratings and Chara	icteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	32	Α
Forward Voltage	$V_{SD}$	I <sub>F</sub> =	_	0.8	1.1	V	

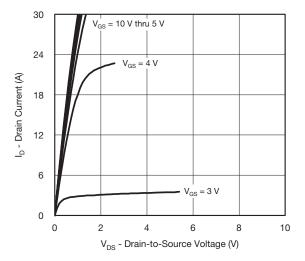
## Notes

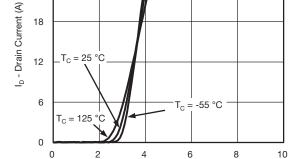
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

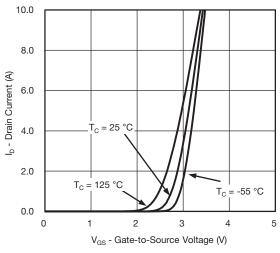


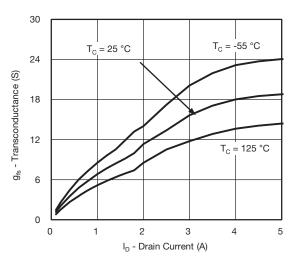


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## **Output Characteristics**

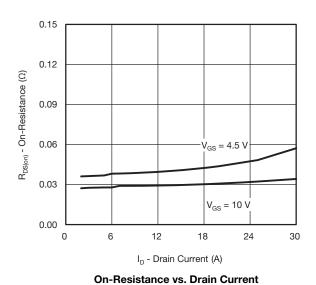
V<sub>GS</sub> - Gate-to-Source Voltage (V) **Transfer Characteristics** 

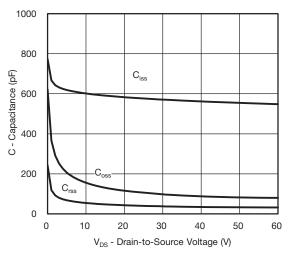




## Transfer Characteristics

Transconductance

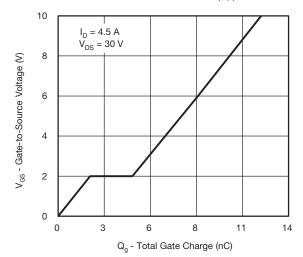




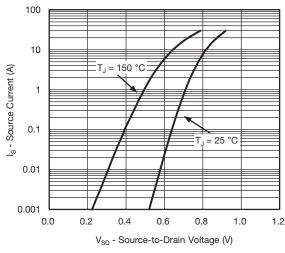
Capacitance



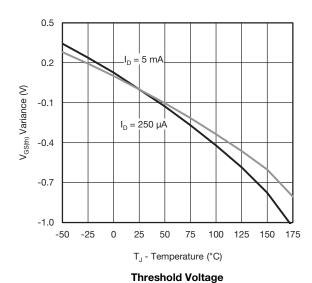
# **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

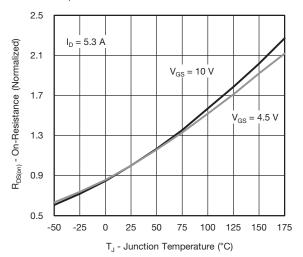


#### **Gate Charge**

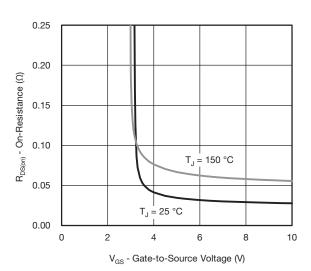


# **Source Drain Diode Forward Voltage**

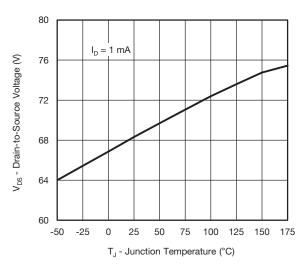




## On-Resistance vs. Junction Temperature



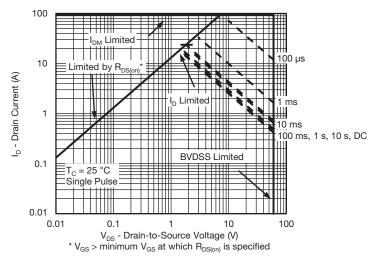
## On-Resistance vs. Gate-to-Source Voltage



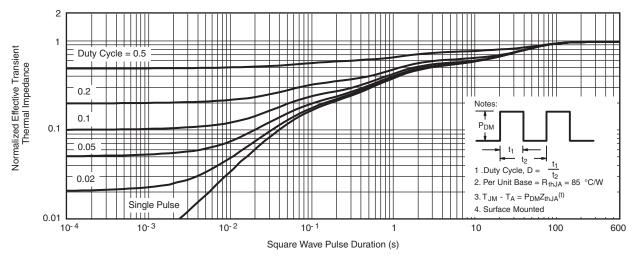
Drain Source Breakdown vs. Junction Temperature



# **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



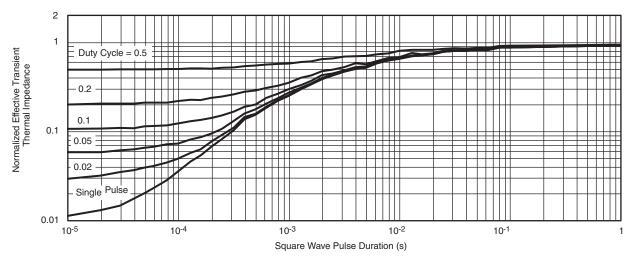
## Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg262817">www.vishay.com/ppg262817</a>.





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REVISION	HISTORY a	
REVISION	DATE	DESCRIPTION OF CHANGE
В	04-Aug-15	Revised R <sub>g</sub> minimum limit
С	14-Jun-16	I <sub>D</sub> and P <sub>D</sub> corrected

## Note

a. As of April 2014



# PowerPAK® SO-8L Case Outline 2



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DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
E3	6.05	6.22	6.40	0.238	0.245	0.252	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51			0.020		
W	0.23			0.009			
W1	0.41			0.016			
W2	2.82			0.111			
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

DWG: 6044

## Note

• Millimeters will govern



## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads Dimensions in mm (inches) Keep-out 6.75 (0.266) x 7.75 (0.305)



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