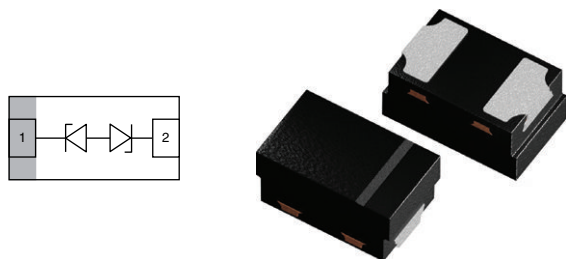


Single-Line Bidirectional ESD-Protection Diode in DFN1006-2B



MARKING (example only)



Bar = pin 1 marking

X = date code

YY = type code (see table below)

LINKS TO ADDITIONAL RESOURCES



3D Models

SPICE

Models



Application Notes

FEATURES

- Compact DFN1006-2B package
- Low package height < 0.5 mm
- 1-line bidirectional ESD-protection
- AEC-Q101 qualified available
- Working range 16 V and 26 V
- ESD immunity acc. IEC 61000-4-2
± 30 kV contact and air discharge
- ESD immunity acc. ISO10605 (330 pF / 330 Ω)
± 30 kV contact discharge
- Lead plating: Sn (e3)
Tin plated exposed side wall of lead frame
 - Soldering can be checked by standard vision inspection
 - AOI = Automated Optical Inspection
 - No X-ray necessary
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Soldering Recommendations for DFN Packages:

please see Application Note: www.vishay.com/doc?86198

APPLICATIONS

For automotive network such as LIN-BUS

ORDERING INFORMATION

PART NUMBER (EXAMPLE)	AEC-Q101 QUALIFIED	ENVIRONMENTAL AND QUALITY CODE			ORDERING CODE (EXAMPLE)
		RoHS COMPLIANT + LEAD (Pb)-FREE TERMINATIONS	TIN PLATED	10K PER 7" REEL (8 mm TAPE)	
		GREEN		MOQ = 10K/BOX	
VLIN1626-DD1	-	G	3	-08	VLIN1626-DD1-G3-08
VLIN1626-DD1	H	G	3	-08	VLIN1626-DD1HG3-08

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VLIN1626-DD1	DFN1006-2B	5E	0.83 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

**ABSOLUTE MAXIMUM RATINGS - PIN 1 TO PIN 2 (16 V)** ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5, 8/20 μs /single shot ⁽¹⁾	I_{PPM}	5	A
Peak pulse power	Acc. IEC 61000-4-5, 8/20 μs /single shot ⁽¹⁾	P_{PP}	160	W
Peak pulse current	$t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾	I_{PPM}	0.6	A
Peak pulse power	$t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾	P_{PP}	18	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses ⁽¹⁾	V_{ESD}	30	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses ⁽¹⁾		30	kV
	Contact discharge acc. ISO10605 (330 pF / 330 Ω); 10 pulses ⁽¹⁾		30	kV
Operating temperature	Junction temperature	T_J	-55 to +150	$^{\circ}\text{C}$
Storage temperature		T_{stg}	-55 to +150	$^{\circ}\text{C}$

ABSOLUTE MAXIMUM RATINGS - PIN 2 TO PIN 1 (26 V) ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5, 8/20 μs /single shot ⁽¹⁾	I_{PPM}	3.9	A
Peak pulse power	Acc. IEC 61000-4-5, 8/20 μs /single shot ⁽¹⁾	P_{PP}	175	W
Peak pulse current	$t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾	I_{PPM}	0.4	A
Peak pulse power	$t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾	P_{PP}	17	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses ⁽¹⁾	V_{ESD}	30	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses ⁽¹⁾		30	kV
	Contact discharge acc. ISO10605 (330 pF / 330 Ω); 10 pulses ⁽¹⁾		30	kV
Operating temperature	Junction temperature	T_J	-55 to +150	$^{\circ}\text{C}$
Storage temperature		T_{stg}	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS - PIN 1 TO PIN 2 (16 V) ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS / REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand off voltage	Max. reverse working voltage	V_{RWM}	-	-	16	V
Reverse voltage	At $I_R = 50\text{ nA}$	V_R	16	-	-	V
Reverse current	At $V_R = 16\text{ V}$	I_R	-	< 1	0.05	μA
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	V_{BR}	17.4	18.5	20.0	V
	At $I_R = 1\text{ mA}$; $T_J = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$ ⁽¹⁾		16	-	22.5	V
Reverse clamping voltage	At $I_{PP} = I_{PPM} = 5\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$ ⁽¹⁾	V_C	-	26	32	V
	At $I_{PP} = I_{PPM} = 0.6\text{ A}$, $t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾		-	25	30	V
	$t_p = 100\text{ ns}$ (TLP); $I_{TLP} = 16\text{ A}$ ⁽¹⁾	V_{C_TLP}	-	26	-	V
Dynamic resistance	$t_p = 100\text{ ns}$ (TLP); $I_{TLP} = 0\text{ A}$ to 50 A ⁽¹⁾	r_{dyn}	-	0.28	-	Ω
Capacitance	At $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	16	20	pF

ELECTRICAL CHARACTERISTICS - PIN 2 TO PIN 1 (26 V) ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS / REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand off voltage	Max. reverse working voltage	V_{RWM}	-	-	26	V
Reverse voltage	At $I_R = 50\text{ nA}$	V_R	26	-	-	V
Reverse current	At $V_R = 26\text{ V}$	I_R	-	< 1	0.05	μA
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	V_{BR}	28	30	32	V
	At $I_R = 1\text{ mA}$; $T_J = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$ ⁽¹⁾		26	-	36	V
Reverse clamping voltage	At $I_{PP} = I_{PPM} = 3.9\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$ ⁽¹⁾	V_C	-	39	45	V
	At $I_{PP} = I_{PPM} = 0.4\text{ A}$, $t_p = 10/1000\text{ }\mu\text{s}$ ⁽¹⁾		-	37	43	V
	$t_p = 100\text{ ns}$ (TLP); $I_{TLP} = 16\text{ A}$ ⁽¹⁾	V_{C_TLP}	-	37	-	V
Dynamic resistance	$t_p = 100\text{ ns}$ (TLP); $I_{TLP} = 20\text{ A}$ to 50 A ⁽¹⁾	r_{dyn}	-	0.36	-	Ω
Capacitance	At $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	16	20	pF

Note

⁽¹⁾ Guaranteed by design; tested during device characterization

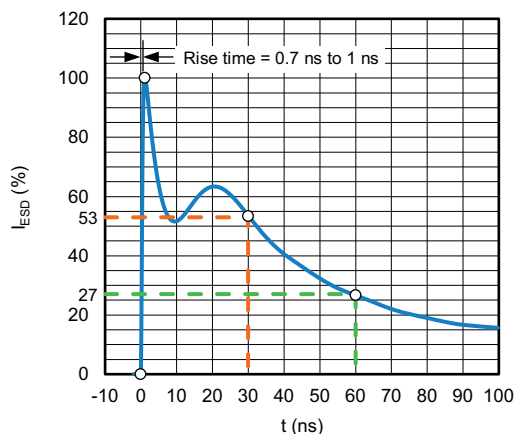


Fig. 1 - ESD Discharge Current Wave Form Acc. IEC 61000-4-2 (330 Ω / 150 pF)

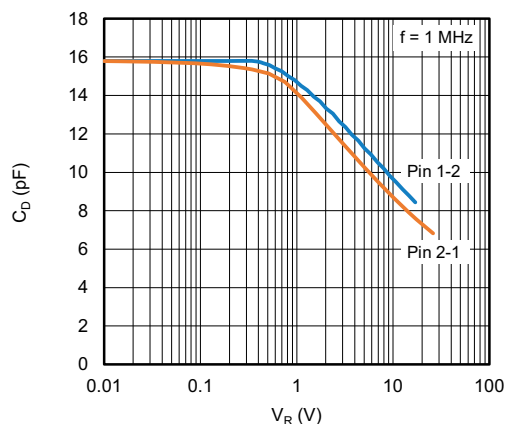


Fig. 4 - Typical Capacitance vs. Reverse Voltage

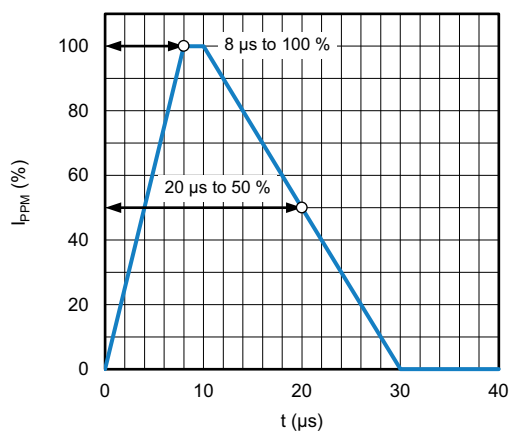


Fig. 2 - 8/20 μ s Peak Pulse Current Wave Form Acc. IEC 61000-4-5

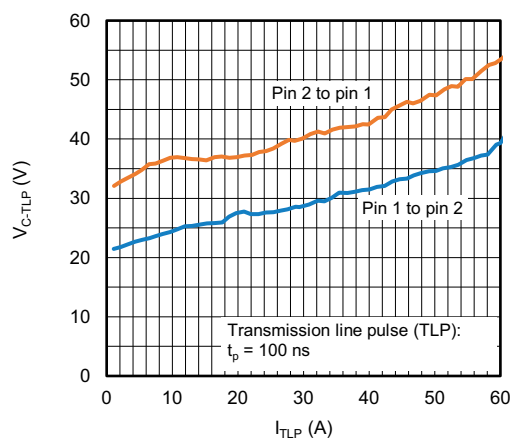


Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current

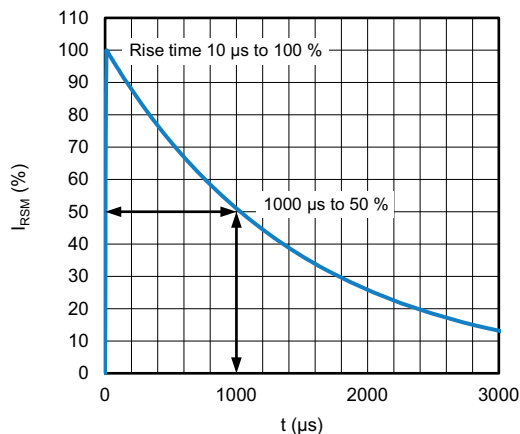


Fig. 3 - 10/1000 μ s Peak Pulse Current Wave Form

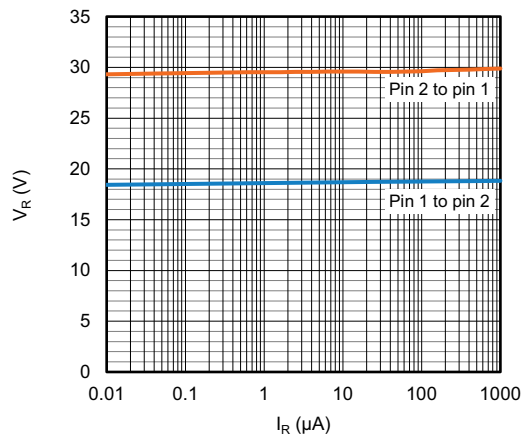


Fig. 6 - Typical Reverse Voltage vs. Reverse Current

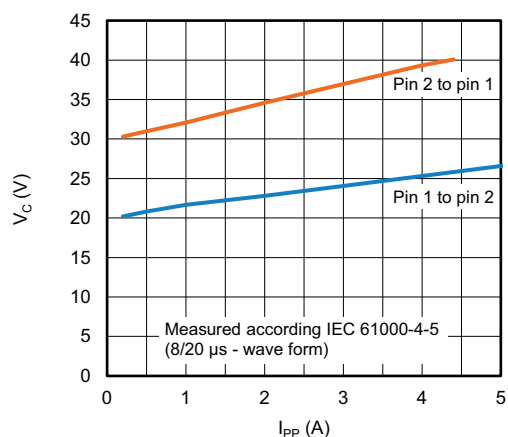


Fig. 7 - Typical Peak Clamping Voltage vs. Peak Pulse Current

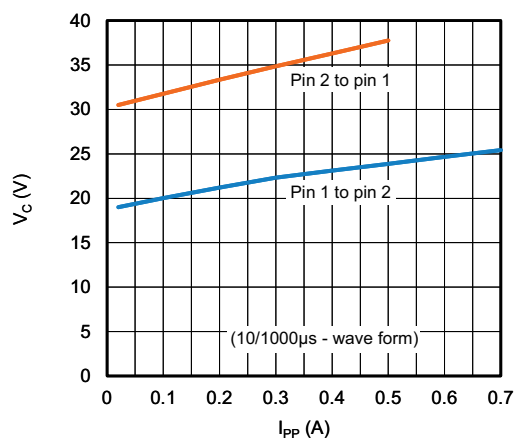
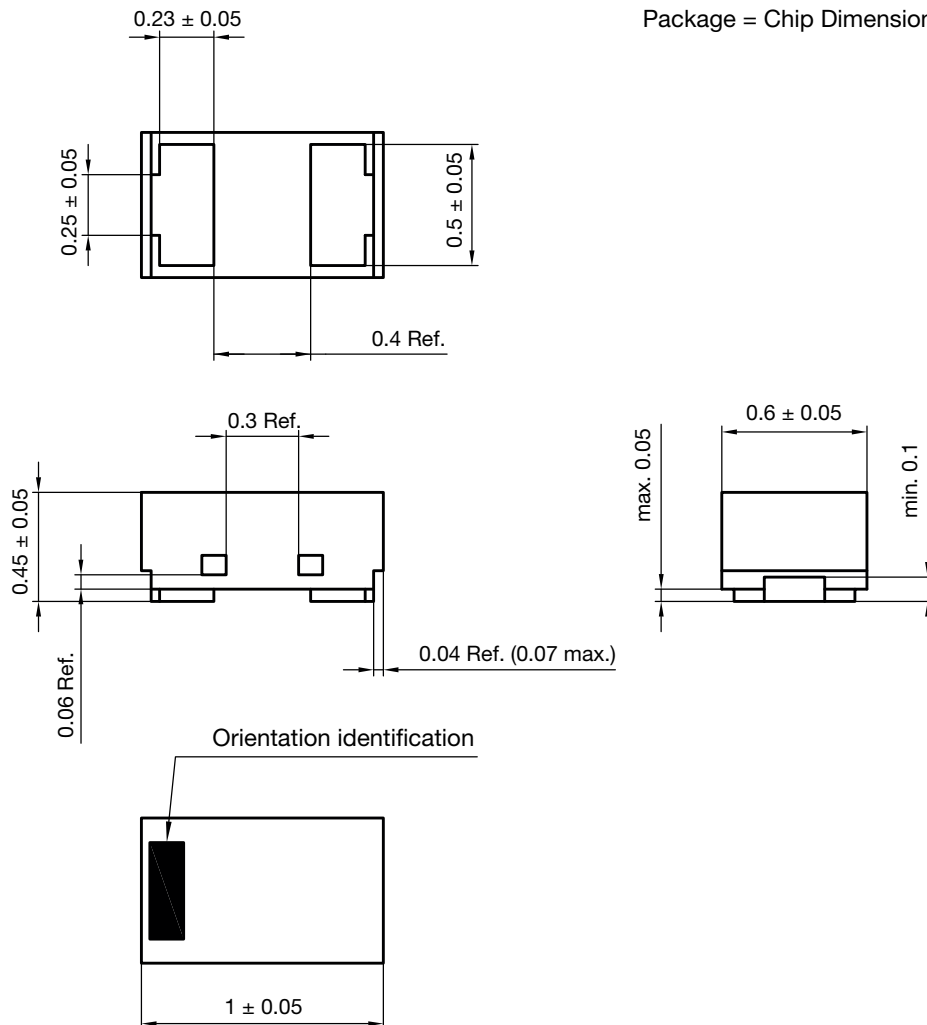
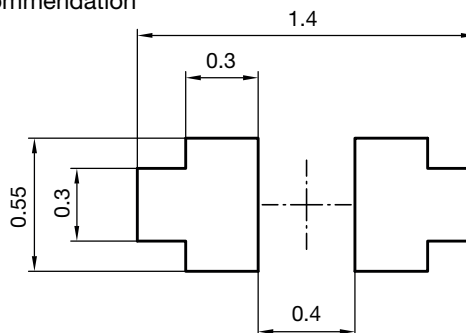


Fig. 8 - Typical Peak Clamping Voltage vs. Peak Pulse Current

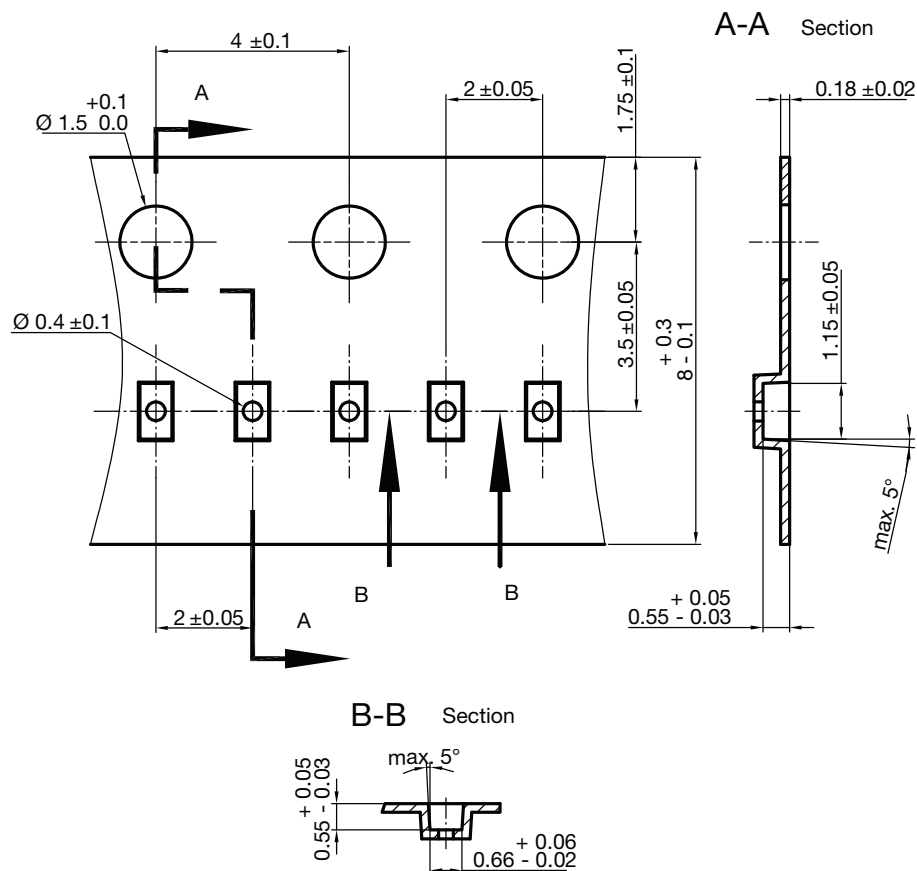
PACKAGE DIMENSIONS in millimeters (inches): **DFN1006-2B**

Package = Chip Dimension in mm


Footprint recommendation


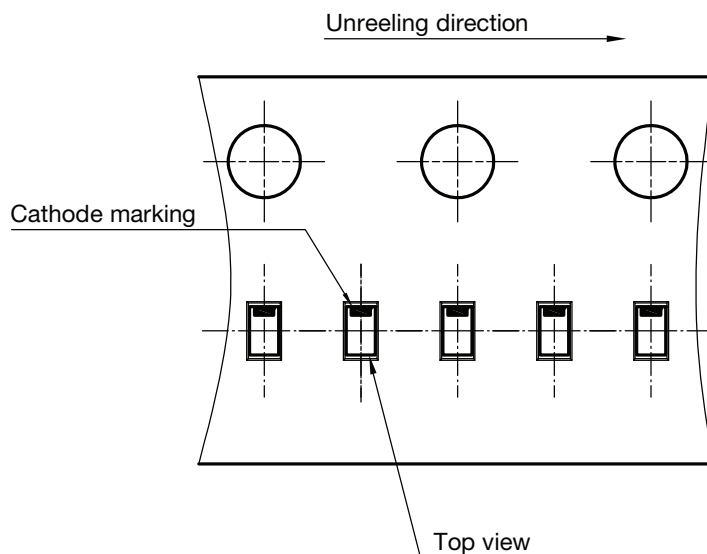
Document no.: S8-V-3906.04-059 (4)
Created - Date: 11-Jul-2018
Rev.5 - Date: 17-Sep-2021

23191

CARRIER TAPE DFN1006-2B


S8-V-3906.04-063 (4)
created 28.10.2019

surface resistance: $10^5 - 10^{11} \frac{\text{OHMS}}{\text{SQ}}$
Cumulative tolerances of 10 sprocket holes is $\pm 0.2 \text{ mm}$

ORIENTATION IN CARRIER TAPE DFN1006-2B


S8-V-3906.04-064 (4)
created 28.10.2019



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