

EL Series Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. at 25 °C (Ω)	$V_{GS} = 10$ V	0.171
Q_g max. (nC)	74	
Q_{gs} (nC)	15	
Q_{gd} (nC)	15	
Configuration	Single	

FEATURES

- Reduced figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

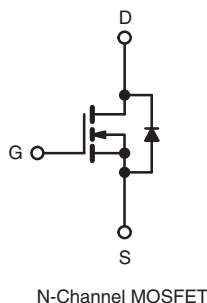
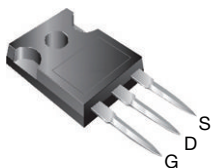


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
 - Switch mode power supplies (SMPS)
 - Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

TO-247AC



ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free and Halogen-free	SiHG22N60EL-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	45	
Linear Derating Factor		1.8	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	286	mJ
Maximum Power Dissipation	P_D	227	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	62	V/ns
Reverse Diode dV/dt ^d		22	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C


Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.55	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.71	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	-	5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$	-	0.171	0.197	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 20\text{ V}$, $I_D = 11\text{ A}$	-	6.5	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	1690	-	pF
Output Capacitance	C_{oss}		-	95	-	
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	85	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	296	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$, $V_{DS} = 480\text{ V}$	-	37	74	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	15	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	22	44	ns
Rise Time	t_r		-	46	92	
Turn-Off Delay Time	$t_{d(off)}$		-	27	54	
Fall Time	t_f		-	24	48	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	0.65	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	21	A
Pulsed Diode Forward Current	I_{SM}		-	-	45	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 11\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = I_S = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	365	-	ns
Reverse Recovery Charge	Q_{rr}		-	5.8	-	μC
Reverse Recovery Current	I_{RRM}		-	29	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

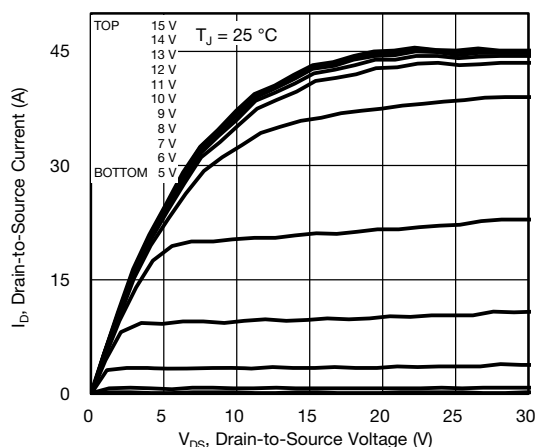


Fig. 1 - Typical Output Characteristics

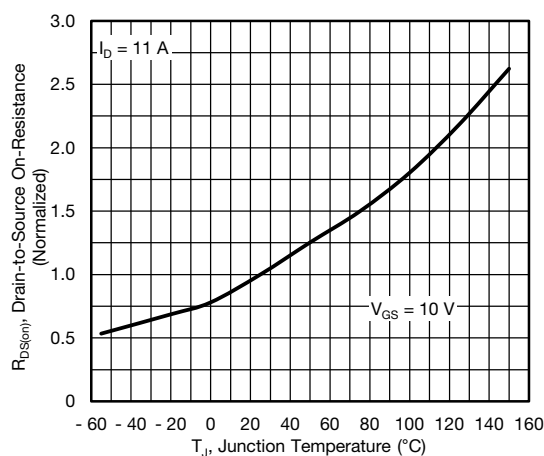


Fig. 4 - Normalized On-Resistance vs. Temperature

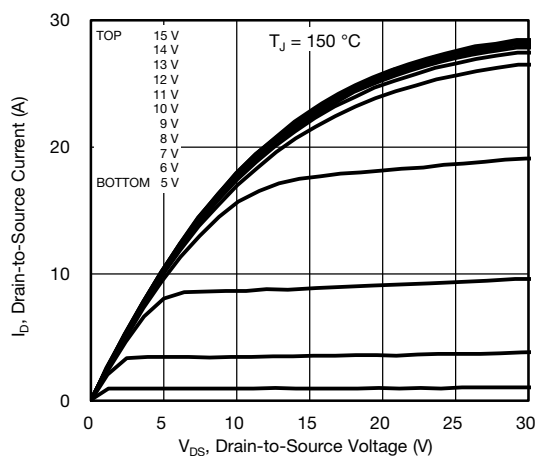


Fig. 2 - Typical Output Characteristics

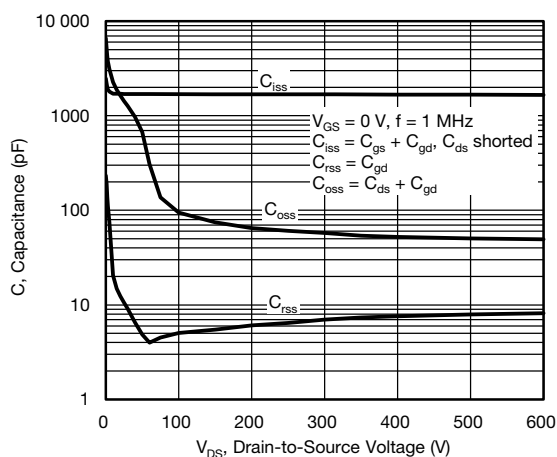


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

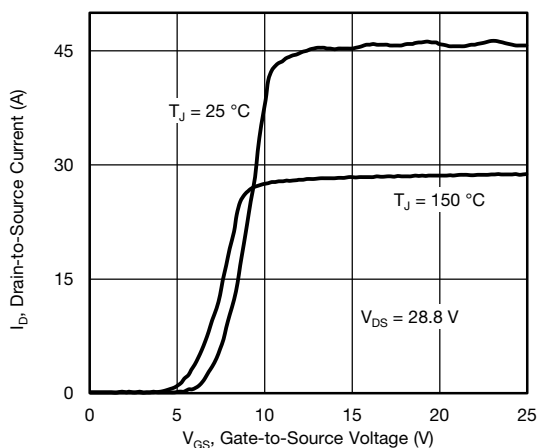


Fig. 3 - Typical Transfer Characteristics

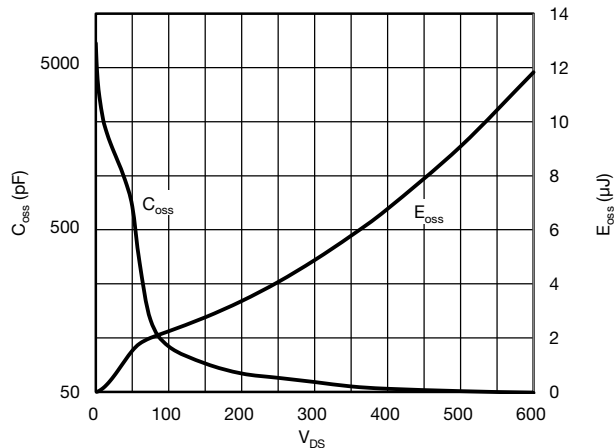
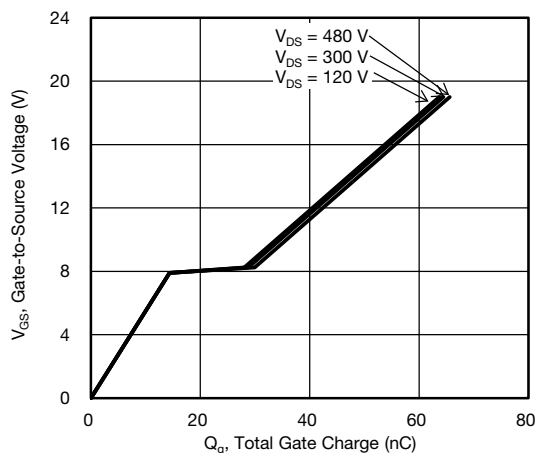
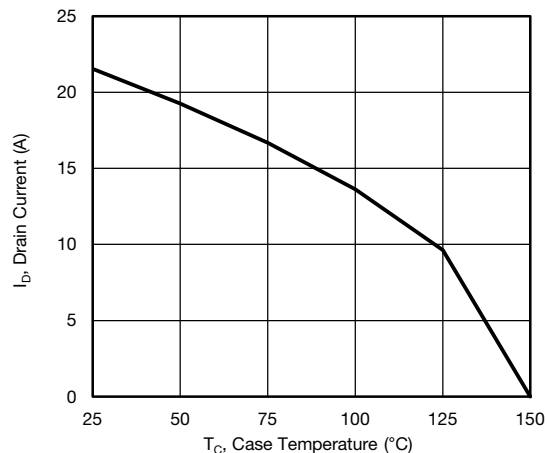
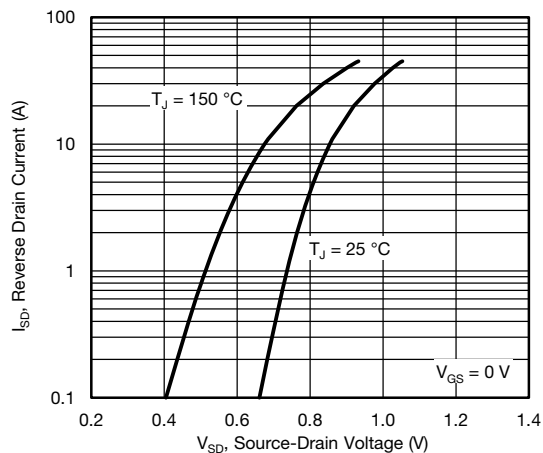
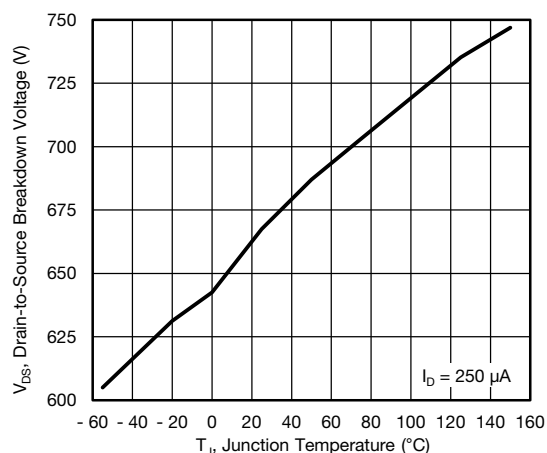
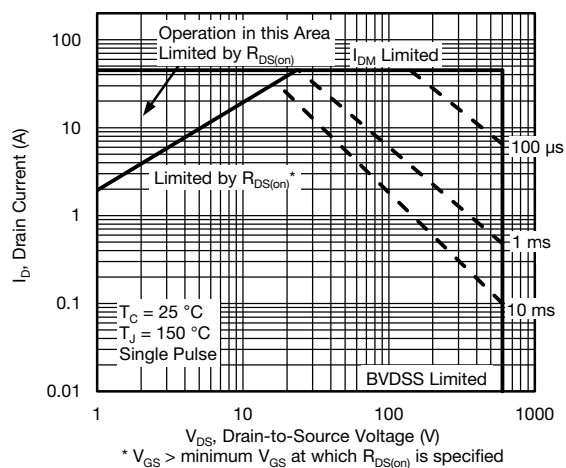
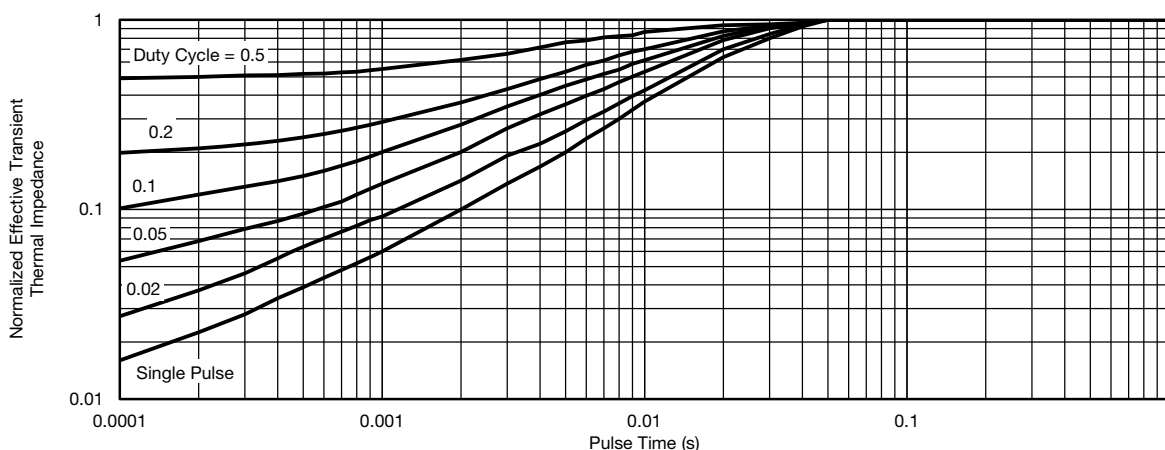
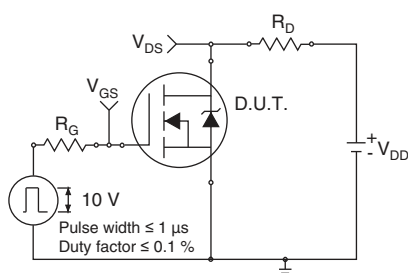
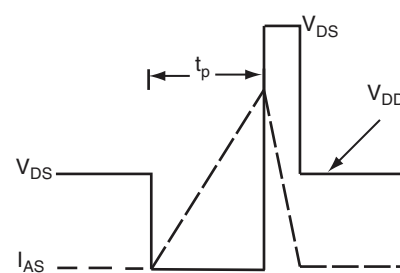
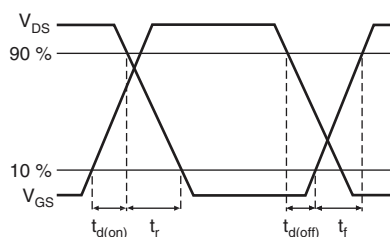
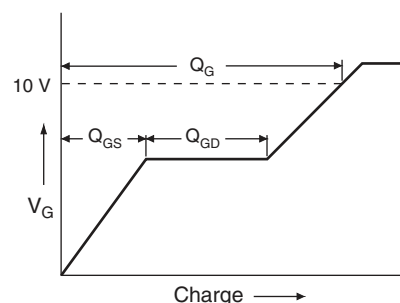
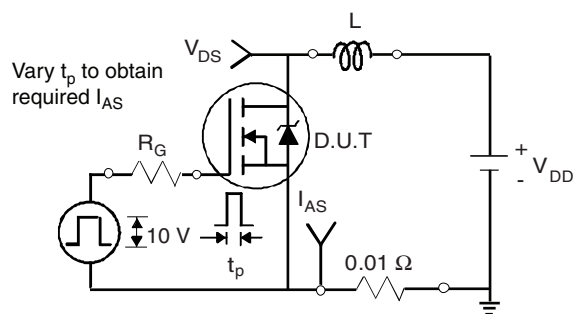
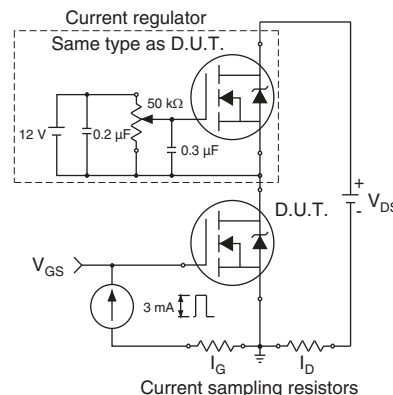
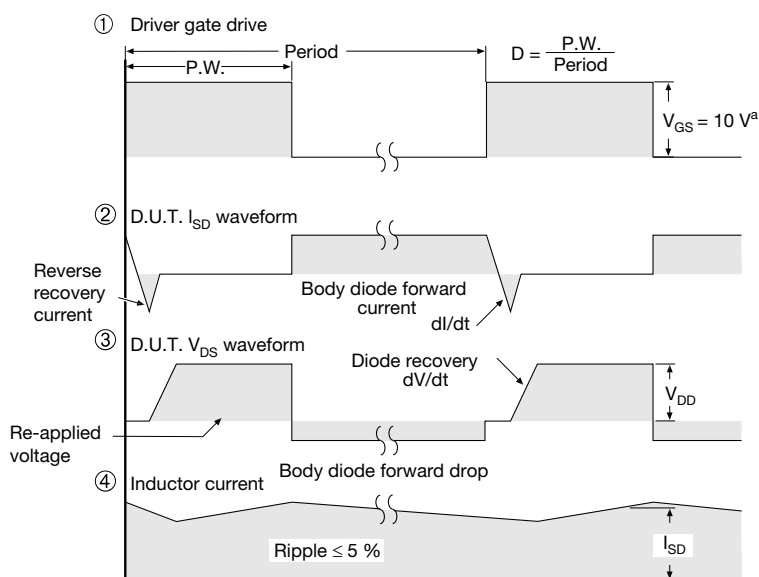
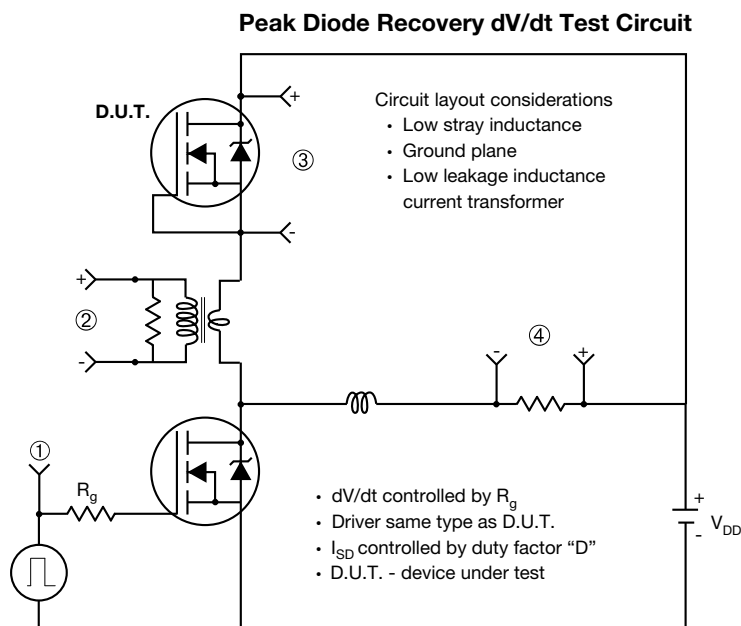


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

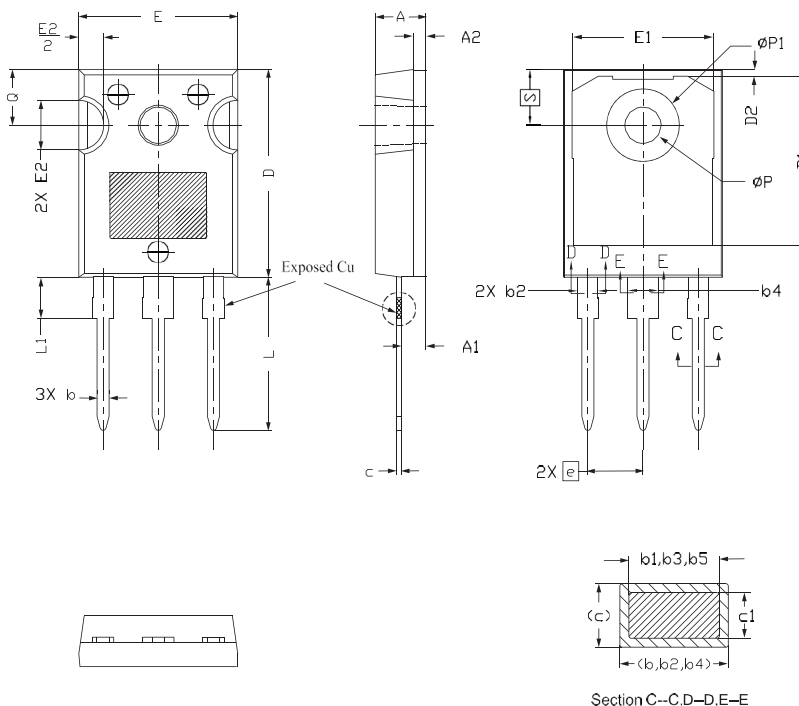

Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91641.

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9

Section C--C,D-D,E-E

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			



VERSION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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