Assignment 3 (EC39004: VLSI Laboratory)

Deadline: Upto 26^{th} March, 2 pm

Instruction: You are required to submit a neatly labeled circuit diagram of the CSD Recoding circuit and answer the associated questionnaire in hard copy (one per group), and demonstrate the working of the verilog codes and simulation outputs in your respective laptops or computer. Kindly zip your Verilog codes and test bench codes in a folder named by GROUP$<$ NO $:>$ and email it to $<$ *ayanpc@ece.iitkgp.ernet.in* $>$ and $<$ *sudiptabose*1991@*gmail.com* $>$ before coming to class on 26^{th} March 2018.

1 Problem Statement

The CSD code is a ternary number system with the digit set $\{\overline{1}, 0, 1\}$, where $\overline{1}$ stands for -1. Given a constant, the corresponding CSD representation is unique and has two main properties: (1) the number of nonzero digits is minimal, and (2) no two consecutive digits are both nonzero, that is, two nonzero digits are not adjacent. The first property implies a minimal Hamming weight, which leads to a reduction in the number of additions in arithmetic operations. The second property provides its uniqueness characteristic. The conversion process from binary to CSD code, i.e., from 001010111 to $010\overline{1}0\overline{1}00\overline{1}$ was illustrated in class; i.e. $001010111 \rightarrow 00101100\overline{1} \rightarrow 00110\overline{1}00\overline{1} \rightarrow 010\overline{1}0\overline{1}00\overline{1}$

This means that a string of 1's can be replaced by a 1, followed by 0s, followed by a $\overline{1}$. Isolated 1s are left unchanged, but isolated 0s are re-examined in such a way that pairs of type $1\overline{1}$ are changed to 01. Traditionally, this encoding is performed from LSB to MSB using two adjacent bits and a carry signal according to the recoding algorithm. The carry-out $c_i = 1$ if and only if there are two of three 1s among the three inputs x_{i+1}, x_i and c_{i-1}, indicating that there exists a stream of 1s from the $(i-1)$th index to a lower value index. The truth table description is given in the next page.

Take a 16-bit unsigned input number and demonstrate its CSD output. Give exhaustive post route simulation outputs for specific inputs that covers all the possible input combinations for the given truth table. Consider the encoding for $\{0, 1, -1\}$ as $\{00, 01, 10\}$ in binary representation.

2 Answer the following questions

1. Assume you have a 5-digit CSD number X ($X = \{x_4x_3x_2x_1x_0\}$) with the encoding for $\{0, 1, -1\}$ as $\{00, 01, 10\}$. Derive –X from X with minimal hardware.

2. Derive the most optimized converter possible that accepts a 5-bit two's complement number as input and outputs a redundant signed digit equiv-

alent that has digit set $\{0, 1, -1\}$ which need not obey the two CSD properties of sparse non-zero occurrences and no two consecutive digits being non-zero.

x_{i+1}	x_i	c_{i-1}	y_i	c_i	Comments (Status upto i-th position)
0	0	0	0	0	String of 0s
0	0	1	1	0	i-th unsigned input position is zero; however owing to previous carry, i-th CSD output digit is 1
0	1	0	1	0	A single 1 in the midst of zeros
0	1	1	0	1	A string of 1s from i-th index to a lower index value hence i-th CSD digit output is zero
1	0	0	0	0	A string of 0s from i-th index to a lower index value
1	0	1	$\overline{1}$	1	String of 1s from (i-1)th position to lower index, 0 at index i, and 1 at index (i+1) (or beyond) leads to CSD output $\overline{1}$ at i-th position for eg. $11011 \rightarrow 1110\overline{1} \rightarrow 100\overline{1}01$
1	1	0	$\overline{1}$	1	Beginning of 1s from i-th position and beyond
1	1	1	0	1	String of 1's leading to i-th CSD output digit=0