(EC39004: VLSI Laboratory)
Mini Project Problems
Deadline: Upto 11th April, 2018

General Instructions for all groups:

You are required to submit the report typed in Word document or Latex. The contents of the report will be as follows:

i) Title and objective
ii) Brief description of the algorithm
iii) Hardware architecture implementation details of the algorithm; how you have derived the architecture (algorithm-to-architecture translation)
iv) Implementation results: area, speed and related design statistics
v) Discussions: challenges faced, novelty of your architecture (if any)
vi) Additional features implemented if any (may bring you extra credit) :-)
vii) References: book(s), conference and journal papers (if any)

Please note that the references attached with this mail are only a snapshot of the algorithm to be implemented. You are particularly encouraged to use the Google Search engine to get even more illustrative and easy-to-read references. You may refer some Hardware for Computer Arithmetic text books such as Digital Arithmetic by Ercegovac Lang and Computer Arithmetic by Israel Koren. The second book in my opinion is easier to read and understand. You may download them from the free ebook websites or DC++.... There are many other books as well.

Please adopt Structural Verilog Modelling where the hardware implementation details are clearly pronounced.

Problem Statement:

1. Derive the architecture of apipelined CORDIC (Co-ordinate Rotation Digital Computer) processor working in Circular Rotation Mode for computing sine and cosine of a user given angle Θ the range of -90^0 to 90^0. In the rotation mode the input vector (X, Y) is rotated by an angle θ. The architecture has 16 bit input dataand 14 cascaded stages each performing a specific micro-rotation i.e. the first stage always performs the first micro rotation of 45^0.The user given initial input data value is x_0=K=0.607252935, y_0=0, z_0=θ**.** Thus,after final 14^{th} stage of the pipelined CORDIC, the results are as follows: $x_{14} = \cos\theta$, $y_{14} = \sin\theta$, $z_{14} \rightarrow 0$.

   Write the Verilog Code for the above pipelined CORDIC (Co-ordinate Rotation Digital Computer) processor working in Circular Rotation Mode which accepts 16 bit input X, Y, Θ and has 14 cascaded stages. Demonstrate the functionality of the pipelined CORDIC processor with exhaustive post route simulation outputs for a varied possible set ofgiven input angle Θ that leads to computation of sine and cosine of user given angle Θ. Follow a structural style of Verilog coding.

2. Derive the architecture for a Sequential Multiplication (through add-shift approach) procedure following Booth's Algorithm for multiplying 2 two's complement numbers, each 16-bit wide. *(Please note that we **do not need an Array Multiplier** like the Baugh Wooley Multiplier)* You must clearly explain in your architecture the datapath, controlpath and characterize the control signals. You may also possibly derive an FSM based model to characterize your circuit if you wish; however credit will go to how you properly synchronize the operations and optimize your circuit. Reference of the paper originally written by Booth is provided and another reference from a book by Hayes is also provided. However you may look up many such references available in the Internet.