Assignment 2 (EC39004: VLSI Laboratory)

Deadline: Upto 19^{th} March, 2 pm

Instruction: You are required to submit a neatly labeled circuit diagram of the combined unsigned and two's complement array multiplier and answer the associated questionnaire in hard copy (one per group), and demonstrate the working of the verilog codes and simulation outputs in your respective laptops or computer. Kindly zip your Verilog codes and test bench codes in a folder named by GROUP$<$ NO $:>$ and email it to $<$ *ayanpc@ece.iitkgp.ernet.in* $>$ and $<$ *sudiptabose*1991@*gmail.com* $>$ before coming to class on 19^{th} March 2018.

1 Problem Statement

Refer to the Modified Baugh Wooley Multiplier discussed in the lab today. Modify the architecture which has an additional control input t. When $t = 0$, the multiplier treats the real time inputs as unsigned numbers and functions as Braun's array multiplier. When $t = 1$, the multiplier treats the real time inputs as two's complement numbers and functions as the modified Baugh Wooley Multiplier. The most optimized array multiplier in terms of hardware shall fetch full credit.

Write the Verilog Code for the above $m \times n$ combined unsigned and two's complement array multiplier accepting 6-bit multiplicand input a ($m = 6$), 7-bit multiplier input b ($n = 7$) and the control signal t, with exhaustive post route simulation outputs. Instantiate the requisite number of half adders and full adders in the code along with other logic gates as deemed necessary.

2 Answer the following questions

1. For an $m \times n$ multiplier with an m-bit multiplicand and n-bit multiplier accepting the additional control signal t, compute the following:
   - The number of half adders and full adders required as a function of m and n.
   - The computation time necessary to obtain the product bits in terms of the propagation delay of half adder (t_{HA}) and full adder (t_{FA}). You may ignore the propagation delay of the logic gates performing the logic operation to generate the partial products in your estimate and neglect interconnection delays.
2. Assume a 5×5 multiplier with both the multiplicand and multiplier inputs following signed-magnitude number system. Using basic logic gates, half

adders and full adders, draw the most optimized combinational architecture in terms of area and speed for the multiplier array.