Batch: B1 Roll No.: 16010124080

Experiment 1

**TITLE:** Study of PCI and SCSI.

**AIM: To Study and learn PCI and SCSI**

**Expected OUTCOME of Experiment : CO1 : Describe and define the structure of a computer with buses structure and detail working of the ALU**

**Books/ Journals/ Websites referred:**

1. https://www.techopedia.com/definition/8815/peripheral-component-interconnect-bus-pci-bus
2. https://www.techopedia.com/definition/331/small-computer-system-interface-scsi
3. http://www.csun.edu/~edaasic/roosta/BUS_Structures.pdf
4. W.Stallings William "Computer Organization and Architecture: Designing for Performance", Pearson Prentice Hall Publication, 7thEdition. C.

**Pre Lab/ Prior Concepts:**

Microcomputer buses which communicate with a peripheral devices or a memory location through communication lines called buses.

The major parts of microcomputers are central processing unit (CPU), memory, and input and output unit. To connect these parts together through three sets of parallel lines, called buses. These three buses are Address bus, data bus, and Control bus.

**Address Bus:**

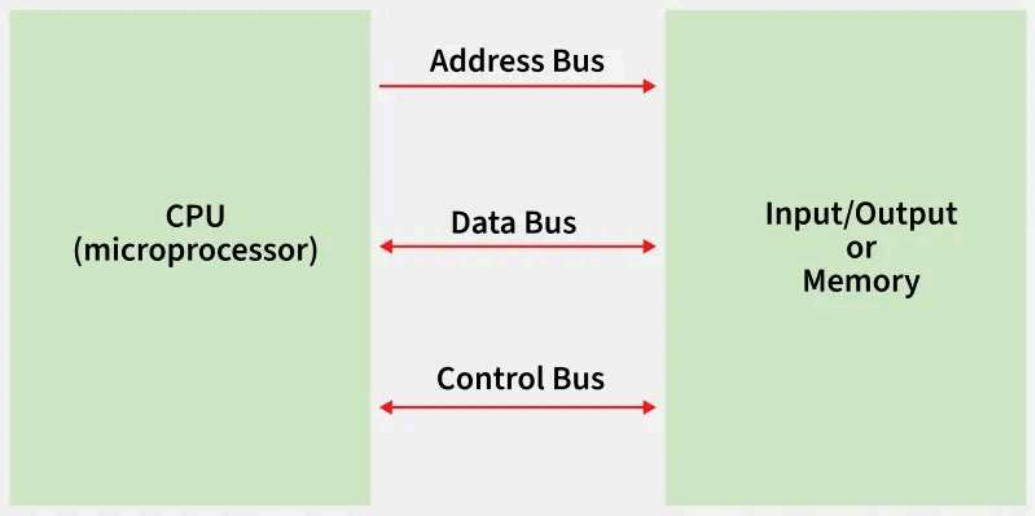
The address bus consists of 16, 20, 24, or more parallel signal lines, through which the CPU sends out the address of the memory location. This memory location is used for to written to or read from. The number of memory location is depends on 2 to the power N address lines. Example, a CPU with 16 address lines can address 216 or 65,536 memory locations. When the CPU reads data from or writes data to a port. The port address is also sent out on the address bus. This is unidirectional. This means that the CPU can send data to a memory location or I/O ports.

**Data Bus:**

The data bus consists of 8, 16, 32 or more parallel signal lines. The data bus lines are bidirectional. This means that the CPU can read data from memory or from a I/O port as well as send data to a memory location or to a I/O port. In a system, many output devices are connected to the data bus, but only one device at a time will be enabled to fthe output.

**Control Bus:**

The control bus consists of 4-10 parallel signal lines. The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or port devices. Typically control bus signals are memory read, memory write, I/O read and I/O write. To read a data from a memory location, the CPU sends out the address of the desired data on the address bus and then sends out a memory read signal on the control bus. The memory read signal enables the addressed memory device to output the data onto the data bus where it is read by the CPU.



| Bus Type | Direction | Purpose | Key Role |
|---|---|---|---|
| Address Bus | Unidirectional | Carries memory addresses | Identifies where data should go |
| Data Bus | Bidirectional | Carries actual data | Moves data between components |
| Control Bus | Bidirectional | Carries control and sync signals | Coordinates CPU and device actions |

**PCI Bus**

Peripheral Component Interface is a general computer bus introduced by Intel in early 1990's used for connecting internal components like sound, network and graphics cards. It is a common bus, a parallel communication interface which allows the device to take control of the bus and communicate directly with memory or other devices without needing the CPU to manage every data transfer.

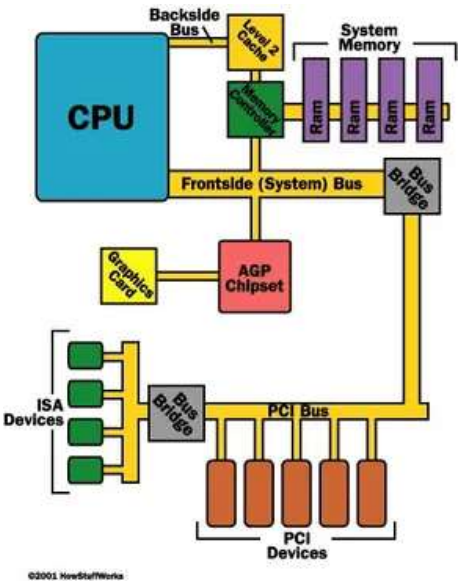
1. Parallel, Multiplexed Bus Architecture
   PCI uses a 32-bit or 64-bit wide bus that carries both addresses and data on the same lines. This lets the CPU and devices share the same connection to send information efficiently.
2. Bus Mastering Support
   Usually, the CPU controls all data transfers — it tells devices when to send or receive data, and moves data between devices and memory. But with bus mastering, the device itself can initiate data transfers on the bus and this frees up the CPU to do other tasks.
3. Plug and Play (PnP) Capability
   PCI supports automatic device configuration, enabling dynamic assignment of resources such as IRQs(Interrupt Request, ie. basically asking for attention from the CPU) , memory address ranges, and I/O ports without manual settings or jumpers.

4. Synchronous Operation with Clock Speeds up to 66 MHz
   PCI operates at the same time with the system clock, typically running at 33 MHz or

66 MHz, enabling data transfer rates up to 133 MB/s for 32-bit at 33 MHz or higher with wider buses and faster clocks.

5. 32-bit and 64-bit Data Path Support
   PCI supports both 32-bit and 64-bit wide data buses, providing flexibility in bandwidth to meet the needs of different device types and performance requirements.

Block Diagram




- The CPU talks directly to system memory and Level 2 cache over the frontside bus.
- The bus bridge connects the faster frontside bus to the slower PCI bus where PCI devices communicate.
- Older devices connect via the ISA bus through another bus bridge.
- Graphics data flows through the AGP chipset and dedicated graphics card for better performance.
- This layered approach balances speed, expandability, and compatibility.

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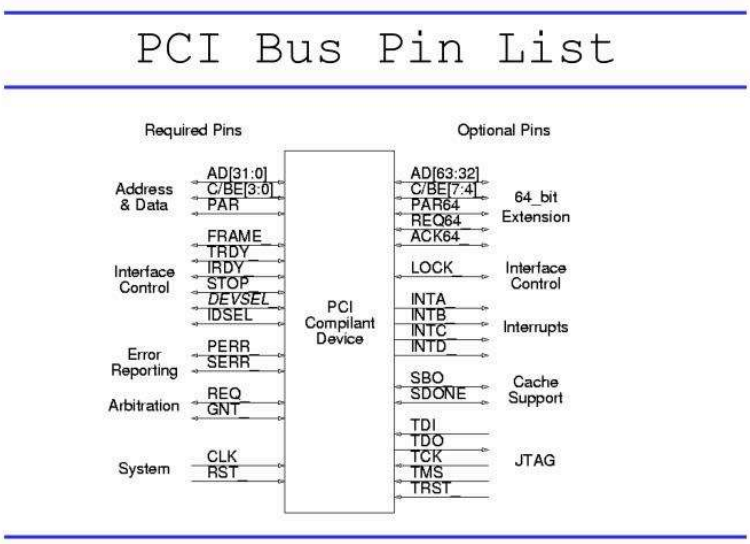
Experiment 1




32-bit PCI slot: Has 124 pins arranged in two rows (Row A and Row B) with 62 pins each.

64-bit PCI slot: Has 188 pins (124 pins for the first 32-bit portion + an additional 64 pins for the extended 64-bit portion).

There are majorly 5 required pins namely(32 bit) :

- Address and Data pins : a total of 32 pins : Transmit the memory or I/O address during the beginning of a PCI transaction, then carry the actual data to be read or written.
- Interface Control Pins : 5 pins : Manage the start, progress, and end of PCI transactions and handshake readiness between initiator and target.

- Error Reporting pins: 2 pins : Detect and report parity errors (PERR#) or more serious system errors (SERR#) on the PCI bus.

- Arbitration pins : 2 pins : Detect and report parity errors (PERR#) or more serious system errors (SERR#) on the PCI bus.
- System pins : clock and reset pins : CLK: Provides the timing reference that synchronizes all PCI bus operations. RST: Resets all devices on the bus to a known initial state.

**SCSI bus:**

SCSI is a set of standards for connecting and transferring data between computers and peripheral devices, primarily focused on storage devices like hard drives, tape drives, and scanners. It allows multiple devices—commonly up to 7 or 15—to be connected on a single bus or chain, each identified by a unique SCSI ID

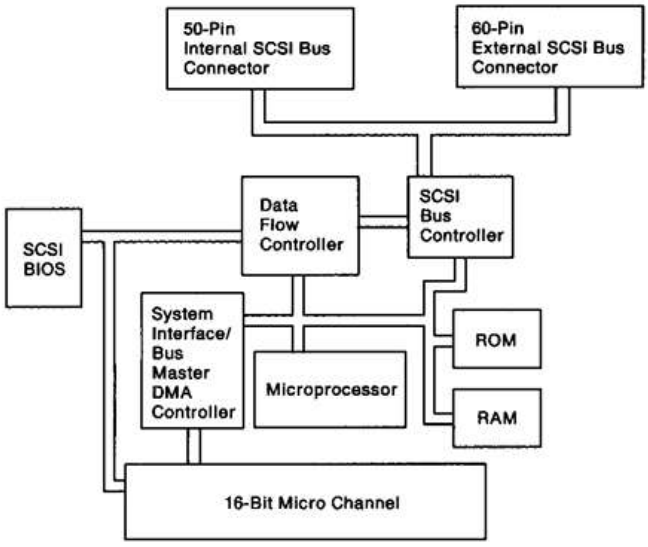
1. Multiple Device Support
   SCSI can connect up to 7 devices (in narrow SCSI) or 15 devices (in wide SCSI) on a single bus, each with a unique SCSI ID, allowing flexible and expandable device configurations.

2. Bus Arbitration
   Devices compete for control of the bus using an arbitration process, ensuring orderly access and preventing data collisions on the shared bus.

3. Command Queuing
   Supports out-of-order execution of commands through Tagged Command Queuing (TCQ : the storage device doesn't have to process commands strictly in the order they were received.), improving performance by optimizing the order of read/write requests.

4. High Data Transfer Rates
   Originally parallel, SCSI supports speeds from a few MB/s up to hundreds of MB/s, and with serial versions like SAS(Serial Attached SCSI uses serial data transmission, which allows faster speeds and longer cables without signal degradation.) speeds now reach multiple gigabits per second.

5. Robust Error Checking and Recovery
   When data moves between devices over a SCSI bus, it can sometimes get corrupted because of electrical noise, signal issues, or other problems. To make sure the data received is exactly the same as what was sent, SCSI uses error checking and recovery mechanisms.



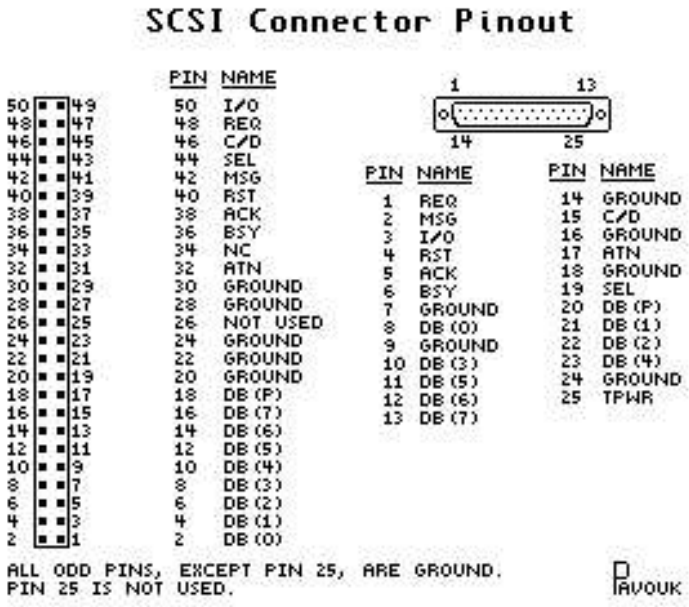

- **SCSI Bus Controller:**
  Manages communication on the SCSI bus itself — it handles sending and receiving commands, data, and control signals to/from devices.

- **DataFlow Controller:**
  Oversees the flow of data between the SCSI bus and the rest of the computer system, ensuring smooth transfer and coordination.

**Microprocessor:**
The brain of the SCSI controller, running firmware/software that manages SCSI operations, protocols, and data transfers.
**System Interface / Bus Master DMA Controller:** Interfaces with the main system bus. It can directly transfer data between system memory and devices using **DMA (Direct Memory Access)** without burdening the CPU.

- **SCSI BIOS:**
  Software that helps the system recognize and communicate with SCSI devices during startup and normal operation.

- **16-Bit Micro Channel:**
  The system bus standard connecting the SCSI controller to the computer's main memory and CPU.




1. **Data Pins (8, 16, or 32 pins):**
   Bidirectional lines (e.g., pins 1–8 for 8-bit) carrying commands, data, and status. Carry actual data transferred between initiator and target devices.

2. **Control Pins (9 pins):**
   Signals like BSY, SEL, ATN, ACK, RST, MSG, CD, IO, and REQ control bus phases and communication. Coordinate bus activity, device selection, and communication phases.

3. **Parity Pin (1 pin):**
   Single line for error detection. Detects data transmission errors, improving

reliability.

4. **Arbitration Pins (4 pins):**
   Lines used for bus arbitration to decide device control.

5. **Ground & Power Pins (varies, 8-12 pins):**
   Provide voltage reference and power for stable operation.

**Post Lab Descriptive Questions**

**Q1 . Differentiate between PCI and SCSI Bus**

| Feature | PCI (Peripheral Component Interconnect) | SCSI (Small Computer System Interface) |
|---|---|---|
| **Purpose** | Connects internal computer components and peripherals (e.g., graphics cards, network cards). | Connects computers to external/internal peripheral devices, mainly storage devices. |
| **Bus Type** | Parallel bus, 32-bit or 64-bit wide data transfer lines. | Originally parallel, also available in serial versions (SAS). |
| **Device Support** | Supports multiple devices but limited to motherboard slots. | Supports up to 7 or 15 devices on a single bus or chain. |
| **Data Transfer Speed** | Up to several hundred MB/s depending on version. | Varies from a few MB/s (older) to several GB/s (SAS). |
| **Bus Mastering** | Supports bus mastering allowing devices to transfer data independently. | Supports bus arbitration for controlling access among devices. |
| **Typical Use** | Internal expansion cards like GPUs, network cards. | Storage devices like hard drives, tape drives, scanners. |

**Q2. List two applications each of PCI and SCSI Bus**

PCI Bus Applications:

1. Connecting graphics cards (GPUs) inside a PC.
2. Network interface cards (NICs) for wired or wireless connectivity.

SCSI Bus Applications:

1. Connecting enterprise hard drives and RAID arrays in servers.
2. Attaching scanners or tape backup devices in professional environments.