COMSATS University Islamabad, Lahore Campus
Block–B, Department of Electrical and Computer Engineering
COMSATS University Islamabad, Lahore Campus 1.5KM Defence Road, Off Raiwind Road, Lahore.

Course Descriptive File

1	**Course Title**	DLD
2	**Course Code**	EEE 241
3	**Credit Hours**	4(3,1)
4	**Prerequisites**	N/A
S,	**Co requisites**	N/A
6	**Semester**	Fall 2024
7	**Resource** Person	Jawwad Gillani
8	**Contact Hours (Theory)**	3 hours per week
9	**Contact Hours (Lab)**	3 hours per week
10	**Office Hours**	Friday 10:30-1:30 Hrs
11	**Email**	jawwadgillani@cuilahore.edu.pk
12	**Course Outline as per SoS**	

The course is designed to teach students, Digital Computer and Systems, Number Systems, Binary Arithmetic, Boolean Algebra, Algebraic Manipulation, Canonical and Standard Form & Conversions, Logical Operations and Gates, Simplification of Functions, Karnaugh Map Methods, Two Level Implementations, Don't Care Conditions, Prime Implicants, Combinational Logic Design, Arithmetic Operations and Circuits, Analysis Procedures, Multilevel NAND/NOR Circuits, Decoders, Encoders, Multiplexers, Demultiplexers, Sequential Logic, Flip-Flops, Clocked Sequential Circuits, State Machine Concept, Design of Sequential Circuits using State Machines, Counters and their Design, Synchronous Counters, Asynchronous Counters, Shift Registers etc.

13	**Course Objectives as per SoS**

The main goals of this course are to teach students the fundamental concepts of basic digital logic circuits and the methodologies of designing. The course is designed to teach students binary arithmetic, Boolean algebra, logic gates, combinational and sequential logic circuits.

14	**Books**

Textbook

1. M. Morris R. Mano and Michael D. Ciletti, *Digital Design*, 5th ed.: Pearson Education, 2012. [Online]. https://books.google.com.pk/books?id=LhZUngEACAAJ

Reference Books

1. Thomas L. Floyd, *Digital Fundamentals*, 10th ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2008.Co-requisites
2. Ronald J. and Widmer, Neal Tocci, *Digital Systems: Principles and Applications*, 7th ed.: Prentice Hall Professional Technical Reference.

15	**Course Learning Outcomes (CLOs)**

After successful completion of this module, you will be able to:

Theory CLOs:

1. CLO1: Comprehend the working with different number systems, Boolean algebra and mapping methods using standard mathematical rules. (PLO1-C2)
2. CLO2: Analyze the working of combinational and sequential logic circuits using digital logic principles and Boolean algebra. (PLO2-C4)
3. CLO3: Plan and design the combinational and sequential logic circuits using digital logic principles, Boolean algebra and mapping methods. (PLO3-C5)

Lab CLOs:

4. CLO4: To analyze and design combinational and sequential logic circuits using software and hardware platforms. (PLO3-C5)
5. CLO5: Follow the software and hardware tools to reproduce the response of the digital logic circuits using software and hardware platforms. (PLO5-P3)
6. CLO6: To explain and write an effective report open-ended lab performed during lab. (PLO10-A3)
7. CLO7: To demonstrate the working of a digital logic circuit designed individually and by teamwork using software and hardware platforms. (PLO9-A3)

16	**Marks Breakup**

Theory

Quizzes (minimum 4)	15%
Homework assignments (minimum4)	10%
Midterm exam(1.5 hours)	25%
Terminal exam(3 hours)	50%

Total (theory) 100%

Lab

• Lab Assignment 1 marks = Lab report marks from experiment 1-3. • Lab Assignment 2 marks = Lab report marks from experiment 4-6. • Lab Assignment 3 marks = Lab report marks from experiment 7-9. • Lab Assignment 4 marks = Lab report marks from experiment 10-12.	25%
0.5*(Mid Term Exam result out of 25) + 0.5* (average of lab evaluation of Lab 1-6 out of 25)	25%
0.1*[(OEP marks out of 50)] +0.4*(Terminal Exam result out of 40) +0.375*(average of lab evaluation of Lab 7-12) + 0.125*(average of lab evaluation of Lab 1-6)	50%

Total (lab) 100%

Final marks	Theory marks * 0.75 + Lab marks * 0.25

17	Lecture Plan						
Week	**Topic**	**CLO**	**Bloom Taxonomy**	**Specific Outcome**	**Contact Hours**	**Students Learning Hours**	**Assessment**
1	Digital Systems, Number Systems	CLO1	C2	Comprehend the theoretical knowledge of number systems such asBinary, Octal, Decimal and Hexadecimalnumbers using standard conversion methods.	1.5	2	Assignment 1 Quiz 1 Midterm Terminal
	Number Systems Conversions Binary Arithmetic	CLO1	C2		1.5	2	
2	Compliment of Numbers Signed and unsigned Binary Numbers	CLO1	C2	Explains the Binary, Gray, BCD and Excess-3 coding techniques and binary conversion of singed & unsigned numbers using standard mathematical techniques.	1.5	2	
	Binary Codes	CLO1	C2		1.5	2	
3	Boolean Algebra, Boolean Functions	CLO1	C2	Explain the Boolean algebra using its theorems and properties based on canonical and standard forms of Boolean functions.	1.5	2	
	Canonical and Standard Forms	CLO1	C2		1.5	2	
4	Digital Logic Gates	CLO1	C2	Explain the use of logic operations and truth tables using Boolean functions based on AND, OR and NOT gates.	1.5	2	
	Auxiliary Logic Gates	CLO1	C2		1.5	2	
5	The Karnaugh-Map (K-Map) Method	CLO1	C2	Comprehend the optimization of Boolean functions based on K-Map approach.	1.5	2	Assignment 2 & 3 Quiz 2& 3 Midterm Terminal
	2, 3, 4 and 5 Variable K-Map	CLO1	C2		1.5	2	
6	Implementation of combinational circuits on POS and SOP forms	CLO2	C2	Explain the implementation and optimization of combinational circuits based on product of sum simplification and Don’t-Care conditions methods.	1.5	2	
	Implementation of combinational circuits using NAND and NOR gates	CLO3	C5	Design and modify the combinational circuit using basic logic gates and universal gates (NAND and NOR) based on product of sum simplification and Don’t-Care conditions methods.	1.5	2	
7	Analysis of Binary Adder-Subtractor, Decimal and BCD Adder	CLO2	C4	Analysis and design of combinational circuits such as 4-bit parallel adder-subtractor, carry propagation, look-ahead carry generation, decimal and adder based on block diagram approach.	1.5	2	

	Design of Binary Adder-Subtractor, Decimal and BCD Adder	CLO3	C5		1.5	2	
8	Magnitude Comparator, Decoders	CLO2	C4	Explain and illustrate the implementation of magnitude comparator and a simple decoder based on gate-level approach.	1.5	2	
	Design of Magnitude Comparator, Decoders	CLO3	C5	Design the magnitude comparator and decoders of different sizes based on block diagram approach.	1.5	2	
9	Encoders, Multiplexers, Demultiplexers	CLO2	C4	Explain and illustrate the implementation of encoders, multiplexers and demultiplexers based on gate-level approach.	1.5	2	
	Design of Encoders, Multiplexers, Demultiplexers	CLO3	C5	Design and integrate combinational circuits using multiplexer, demultiplexers and encoders based on block diagram approach	1.5	2	
10	Sequential Circuits, Storage Elements: Latches	CLO2	C4	Explain and illustrate the working of latches and flip-flops based on universal gates (NAND and NOR).	1.5	2	Assignment 4 Quiz 4 Terminal
	Storage Elements: Flip-Flops	CLO2	C4		1.5	2	
11	Clocked Sequential Circuits	CLO2	C4	Explains and illustrate the implementation and optimization of clocked sequential circuits using S-R, D, J-K and T flip-flops based on state machines and sate-reduction approach	1.5	2	
	State Reduction and Assignment	CLO2	C2		1.5	2	
12	Design Procedure	CLO3	C5	Design and modify the sequential circuit using state reduction and assignment approach.	1.5	2	
13	Registers, Shift Registers	CLO2	C2	Comprehend the working of sequential circuits such as registersand counters using logic gates and flip-flops**.**	1.5	2	
	Ripple Counters, Synchronous Counters	CLO2	C2		1.5	2	
14	Design of Counters	CLO3	C5	Design and optimize the synchronous binary counters such as 4-bit synchronous binary counterusing D, J-K, and T flip-flops.	3	4	

18 **Course LearningOutcomes(CLOs)and AssessmentPlan**

CLO / Activity	CLO 1	CLO2	CLO3	CLO4 (LAB)	CLO5 (LAB)	CLO6 (LAB)	CLO7 (LAB)	Cognitive Domain						Affective Domain					Psychomotor Domain						
								C1	C2	C3	C4	C5	C6	A1	A2	A3	A4	A5	P1	P2	P3	P4	P5	P6	P7
Quiz 1	X							X	X																
Quiz 2		X	X					X	X	X	X	X													
Quiz 3		X	X								X	X													
Quiz 4		X	X								X	X													
Assignment 1	X							X	X																
Assignment 2		X	X					X	X	X	X	X													
Assignment 3		X	X								X	X													
Assignment 4		X	X								X	X													
Midterm	X	X	X					X	X	X	X	X													
Lab Midterm				X	X		X	X	X	X	X	X		X	X	X			X	X	X				
Terminal	X	X	X					X	X	X	X	X													
Lab Terminal				X	X	X	X	X	X	X	X	X		X	X	X			X	X	X				

19	Laboratory Experiences
There is a Laboratory component in all 3+1 credit courses taught at the department. Lab work consists of a minimum of 14 experiments, semester project and related assignments, which constitute 25% of the overall course-grade. The laboratory experiments include hands-on exercises as well as computer analysis of the concepts taught in class. This course familiarizes the students with the Proteus analysis and design software tool, which is a part of all laboratory experiments. Laboratory components covers the Lab-CLO1 (PLO3-C5) and Lab-CLO2 (PLO5-P3).	
20	**Laboratory Resources**
The relevant laboratory is equipped with workbenches and computers to facilitate the experimentsoutlined in the lab handbook(s) that are periodically updated. A current list of the 14 lab experiments performed in this course is provided as Annexure-I. The list of software and equipment available is also posted in all labs and is managed by staff dedicated for this purpose	
21	**Computer Resources**
For the purposes of this course the Proteus analysisand designsoftwareisused throughout the course	
22	**Mapping of CLOs to PLOs**
PLO1	**EngineeringKnowledge:**Anabilitytoapplyknowledgeofmathematics,science, engineering fundamentals and anengineering specializationto the solutionof complexengineeringproblems.**(Cognitive)**
PLO2	**ProblemAnalysis:**Anabilitytoidentify,formulate,researchliterature,andanalyze complex engineering problems reaching substantiated conclusions using first principlesofmathematics,naturalsciencesandengineeringsciences.**(Cognitive)**
PLO3	**Design/Development of Solutions:** An abilityto designsolutionsforcomplex engineeringproblemsanddesignsystems,componentsorprocessesthatmeet specifiedneedswithappropriateconsideration forpublichealthandsafety,cultural, societal,andenvironmentalconsiderations.**(Cognitive)**
PLO4	**Investigation:** An ability to investigatecomplexengineering problemsin a methodical wayincluding literaturesurvey,designandconductofexperiments, analysisand interpretationof experimentaldata,and synthesisof informationto derivevalidconclusions.**(Cognitive, Psychomotor)**
PLO5	**ModernToolUsage:**Anabilitytocreate,selectandapplyappropriatetechniques, resources,andmodernengineeringandITtools,includingpredictionandmodeling,to complexengineeringactivities,withanunderstandingofthelimitations. **(Psychomotor)**
PLO6	**TheEngineerandSociety:**Anabilitytoapplyreasoninginformedbycontextual knowledge toassesssocietal,health,safety,legalandculturalissuesandthe consequentresponsibilitiesrelevanttoprofessionalengineeringpracticeandsolution tocomplexengineeringproblems. **(Cognitive)**
PLO7	**EnvironmentandSustainability:**Anabilityto understandtheimpactof professional engineeringsolutionsinsocietalandenvironmental contextsanddemonstrate knowledgeofandneedforsustainabledevelopment.**(Cognitive)**
PLO8	**Ethics:**Applyethicalprinciplesandcommittoprofessionalethicsandresponsibilities andnormsofengineeringpractice.**(Affective)**
PLO9	**IndividualandTeamWork:**Anabilitytoworkeffectively,asanindividualorina team,on multifacetedand/or multidisciplinarysettings.**(Affective)**
PLO10	**Communication:**Anabilitytocommunicate effectively,orallyaswellasinwriting, on complexengineeringactivitieswiththeengineeringcommunityandwithsocietyat large, suchasbeingable to comprehendand write effectivereports and designdocumentation,makeeffectivepresentations,andgiveandreceiveclearinstructions.**(Affective)**
PLO11	**Project Management:** An ability to demonstrate management skills and apply engineeringprinciplestoone'sownwork,asamemberand/orleaderinateam,to

	manageprojectsinamultidisciplinaryenvironment.**(Affective)**
PLO12	**Lifelong Learning:** An ability to recognizeimportanceof,andpursue lifelong learninginthebroadercontextofinnovationandtechnologicaldevelopments.**(Affective)**

CLOs – PLOs Mapping

PLO / CLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10	PLO11	PLO12	Cognitive Domain						Affective Domain					Psychomotor Domain						
													C1	C2	C3	C4	C5	C6	A1	A2	A3	A4	A5	P1	P2	P3	P4	P5	P6	P7
CLO1	X												X	X																
CLO2		X											X	X	X	X														
CLO3			X										X	X	X	X	X													
CLO4 (LAB)			X										X	X	X	X	X													
CLO5 (LAB)					X																			X	X	X				
CLO6(LAB)										X									X	X	X									
CLO7(LAB)									X				X	X	X				X	X	X									

23	PLOs Coverage Explanation
PLO1	**EngineeringKnowledge:**Knowledge of number systems, Boolean algebra, K-Map and digital logic gates is required in the course and laboratory experiments.
PLO2	**ProblemAnalysis:**Students learn to analyze the combinational and sequential logic system using the basic engineering knowledge.
PLO3	**Design/Development of Solutions:** Students learn to design the combinational and sequential logic system using the basic engineering knowledge.
PLO5	**ModernToolUsage:**Proteus software tool and digital logic trainer board is used in the laboratory experiments. The usage of software and trainer board help the students to verify the result of their designs.
PLO9	**IndividualandTeamWork:**Anabilitytoworkeffectively,asanindividualorina team,on multifacetedand/or multidisciplinarysettings
PLO10	**Communication:**Students explain and write a report of lab experiment performed in the lab.

24	List of Experiment with Objectives as Per OBE Format

List of Lab Experiments
(EEE/CPE241 Digital Logic Design Lab)

LAB # 1: To Identify the Responses of Different Logic Gates using Hardware and Software Platforms

- To identify the basic Boolean functions of logic gates
- To identify various ICs used to perform basic functionality of logic gates

LAB # 2: To Explain the Universality of NAND and NOR GATES in Order to Design Other Logic Gates

- To construct various logic gates using NAND gates
- To construct various logic gates using NOR gates

LAB # 3: To Show the Behavior of Binary Adder/Subtractor and reproduce its circuit using Universal Gates

- To identify basic functionality of a Binary Adder using logic gates
- To identify basic functionality of a Binary Subtractor using logic gates
- To design a binary adder using universal gates (NAND, NOR)
- To design a binary subtractor using universal gates (NAND, NOR)

LAB # 4: To Follow the Steps of BCD to Excess 3 Code Conversion and Reproduce the Results using Dedicated IC

- To understand and respond to the steps required to transform a four-bit BCD to Excess 3 code conversion.
- To reproduce the steps required to transform Excess 3 code to BCD using IC 7483

LAB # 5: To Follow the Steps of BCD to Gray Code Conversion and Reproduce the Results using Logic Gates

- To understand and respond to the steps required to convert a four-bit BCD to Gray code conversion.
- To reproduce the steps required to convert Gray code to BCD using IC 7483.

LAB # 6: To Show the Response of a Multiplexer/Demultiplexer and to Reproduce Adder/Subtractor using Multiplexer

- To explain the basic functionality and working of multiplexer using logic gates
- To explain the basic functionality and working of demultiplexer using logic gates
- To display the results of various applications of multiplexer using hardware and software platforms

LAB # 7: To Show the response of Binary Comparator(s) using hardware and software tools and to Reproduce the Comparator using dedicated IC

- To compare two input signals using logic gates

- To analyze the working of 4-bit magnitude comparator's IC 7485

LAB # 8: To Show the response of an Encoder/Decoder and to Reproduce the binary converters using basic logic gates

- To explain the basic functionality and working of Encoder using logic gates
- To explain the basic functionality and working of decoder using logic gates
- To display the results of various applications of encoder using hardware and software platforms
- To display the results of various applications of decoder using hardware and software platforms

LAB # 9: Introduction to VHDL and Altera Quartus

- How to program in hardware descriptive language in general and VHDL in particular.
- How the software tool Quartus works and its interface.

LAB # 10: To Identify the Response of Sequential Circuit(s) using Hardware and Software Platforms

- To describe the basic functions of sequential circuits
- To differentiate between various types of Flip Flops
- To identify various ICs used to perform basic functionality of various Flip Flops

LAB # 11: To show the Response of Shift Registers using 7495 IC and Reproduce the shift registers using D-Flip-Flops

- To explain the working of a shift register using 7495 IC
- To differentiate between the different types of shift register

LAB # 12: To Reproduce a Synchronous Sequence Detector using hardware and software tools

- To analyze working principle of a sequence detector