Lesson plan Session: 2022-2023 Semester: 1st

Subject: ACOA

Paper Code : INF 1026

Month	Topics	Remarks
August	Instruction set design, addressing modes, representation of data (character, integral, floating point) Computer Arithmetic: - Serial adder, parallel adder, ripple carry adder, carry look-ahead adder, multiplication of signed and unsigned numbers, Booth's algorithm, division of integer, floating point arithmetic.	
September	Processor Design: Register transfer language, one, two and three bus data path, ALU Design, control unit, hardwired control unit, micro programmed control unit. Memory: - Classification and types. Cache memory, direct mapped, associative mapped and set associative mapped cache. cache replacement policies, write policy, unified, split and multilevel cache, virtual memory, paging, segmentation.	
October	Input Output System: I/O buses, device controller, Interrupt and DMA. Interrupt driven I/O, Program controlled and DMA transfer.	Assignment 1
November	Parallel Architectures: Classification, SISD, SIMD, MISD, MIMD, Scalar, vector, superscalar and pipelined processor, Pipelining, Instruction pipeline, pipeline bubbles, Hazards: -resource conflicts, data dependency, branch difficulty. Vector computing, arithmetic pipeline, vector and scalar register, chaining, vector-register processor, memory- memory, vector processor, Array processor	- Assignment 2
December	Advanced concepts: Branch prediction, super pipelining, Branch delay slot, Register file, superscalar architecture, superscalar pipelines, superscalar branch prediction, out of order execution, register renaming, Pipeline scheduling, dynamic scheduling and static scheduling algorithms, reorder buffer and register renaming, Thronton technique and scoreboard. Tomasulo algorithm and reservation stations. VLIW architecture: - EPIC architecture, Multiprocessor systems: - Interconnection types. Cache coherence problem	

Name:

Lesson plan Session: 2022-2023 Semester: 1st

Subject: ACOA Paper Code : CSC 1026

Month	Topics	Remarks
August	Instruction set design, addressing modes, representation of data (character, integral, floating point) Computer Arithmetic: - Serial adder, parallel adder, ripple carry adder, carry look-ahead adder, multiplication of signed and unsigned numbers, Booth's algorithm, division of integer, floating point arithmetic.	
September	Processor Design: Register transfer language, one, two and three bus data path, ALU Design, control unit, hardwired control unit, micro programmed control unit. Memory: - Classification and types. Cache memory, direct mapped, associative mapped and set associative mapped cache. cache replacement policies, write policy, unified, split and multilevel cache, virtual memory, paging, segmentation.	
October	Input Output System: I/O buses, device controller, Interrupt and DMA. Interrupt driven I/O, Program controlled and DMA transfer.	Assignment 1
November	Parallel Architectures: Classification, SISD, SIMD, MISD, MIMD, Scalar, vector, superscalar and pipelined processor, Pipelining, Instruction pipeline, pipeline bubbles, Hazards: -resource conflicts, data dependency, branch difficulty. Vector computing, arithmetic pipeline, vector and scalar register, chaining, vector-register processor, memory- memory, vector processor, Array processor	- Assignment 2
December	Advanced concepts: Branch prediction, super pipelining, Branch delay slot, Register file, superscalar architecture, superscalar pipelines, superscalar branch prediction, out of order execution, register renaming, Pipeline scheduling, dynamic scheduling and static scheduling algorithms, reorder buffer and register renaming, Thronton technique and scoreboard. Tomasulo algorithm and reservation stations. VLIW architecture: - EPIC architecture, Multiprocessor systems: - Interconnection types. Cache coherence problem	

Name: