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Fabrication of graphene *p-n-p* junctions with contactless top gates

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We developed a multilevel lithography process to fabricate graphene *p-n-p* junctions with contactless, suspended top gates. This fabrication procedure minimizes damage or doping to the single atomic layer, which is only exposed to conventional resists and developers. The process does not require special equipment for depositing gate dielectrics or releasing sacrificial layers, and is compatible with annealing procedures that improve device mobility. Using this technique, we fabricate graphene devices with suspended local top gates, where the creation of high quality graphene *p-n-p* junctions is confirmed by transport data at zero and high magnetic fields. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2928234]

Graphene, a single-layer honeycomb lattice of carbon atoms, has recently emerged as a fascinating system for fundamental studies in condensed-matter physics.[1–4] Single-layer graphene is a zero-gap semiconductor with a linear energy dispersion relation, where charges behave as massless Dirac fermions. Charge transport in graphene exhibit a number of phenomena, such as the half-integer quantum Hall effect.[1,3] Technologically, graphene is a two-dimensional material with exceptional mobility, current-carrying capacity, and thermal conductivity, attracting significant attention as a promising postsilicon electronic material.[5–11]

A remarkable electronic property of graphene is that both carrier type and density can be electrostatically controlled. Via the employment of a local gate and a global back gate, this feature also enables *in situ* creation and control of *p-n* junctions in graphene,[11–15] which have been demonstrated or predicted to give rise to quantum Hall plateaus with fractional values,[13–15] Veselago lensing[16,17] and Klein tunneling.[18] In most of the experiments to date, either an organic or a metal oxide layer has been used as the local gate dielectric, yet its deposition on a single atomic layer remains a delicate process that may lead to additional dopants and/or scattering sites. Moreover, dramatically enhanced mobility has been recently observed in suspended graphene devices,[19,20] but fabrication of suspended graphene *p-n* junctions using conventional techniques could prove difficult, since direct deposition of local gate dielectrics may considerably stress or even collapse the atomic layer.

Here, we report an innovative multilevel lithography technique to fabricate contactless top gates that are suspended ~100 nm above the graphene layers. Only conventional electron-beam resists and developers are used, thus minimizing the damage to the atomic layer. The vacuum insulated gap between the "air bridge-styled" top gate and the device is not susceptible to pinholes or dielectric breakdown. Unlike the standard graphene *p-n* junctions, devices fabricated using this technique are still amiable to annealing procedures that have been shown to be effective in improving device mobility and contact resistance.[19,21]Using this technique, we demonstrate the fabrication of a graphene *p-n-p* junction and its quality is established by the presence of the $2e^2/h$ conductance plateau at high magnetic fields. In the

long term, combination of this technique with suspended graphene may enable experimental realization of phenomena such as the Veselago lensing effect.

This fabrication process of suspended structures takes advantage of the different exposure, developing, and lift-off properties of different resists. Figure 1 illustrates the fabrication process, which consists of two lithography steps and a single metal deposition step. The goal of the first lithography step is twofold: (1) to create a temporary support for the suspended portion of the air bridge and (2) to create windows for the electrical leads that contact the suspended structure. To achieve these goals, lift-off resist (LOR)/polymethyl methacrylate (PMMA) bilayer resists are spun and baked on Si/SiO$_2$ substrates [Fig. 1(a)]. We then use an electron beam
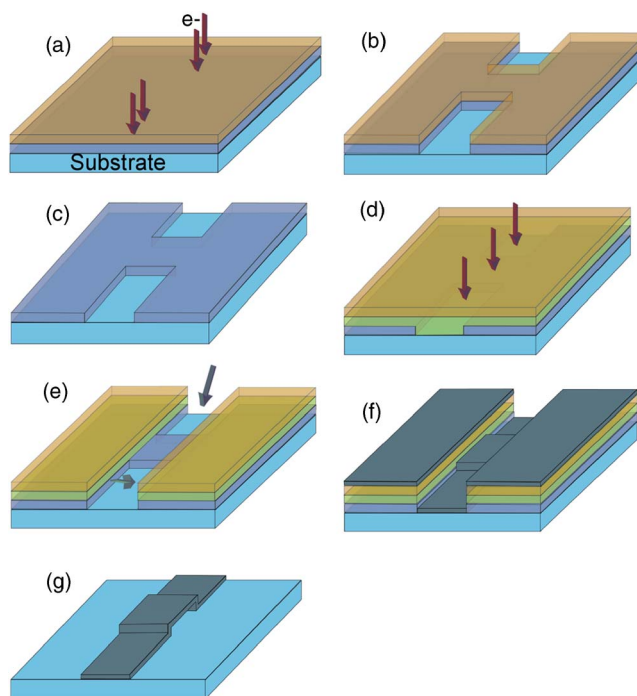
FIG. 1. (Color online) Schematics of fabrication process. (a) LOR (blue) and PMMA (brown) are deposited onto the substrate and exposed to electron beams (arrows). (b) Developing in MIBK and MIF319 solutions opens windows for the electrodes. (c) Lift-off in acetone removes PMMA but leaves LOR layer intact. (d) MMA (green) and PMMA (brown) are deposited, and exposed to *e* beam (arrows). (e) Developing in MIBK opens windows for the electrodes and the suspended structure. (f) Metals are evaporated at 45° and −45° [in directions indicated by arrows in (e)]. (g) Resists are lifted off in PG remover, leaving an air bridge contacted to electrodes.

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FIG. 2. SEM images of suspended air bridges with different spans, widths, and heights. Scale bars: 2 μm.

to expose the patterns for the electrical leads. The chips are developed twice—first in methylisobutylketone (MIBK)/isopropyl alcohol (IPA) to dissolve the exposed PMMA, then in MF319 to dissolve portions of LOR via the PMMA windows [Fig. 1(b)]. Subsequently, acetone is used to lift-off the top PMMA layer while leaving LOR intact [Fig. 1(c)]. The final outcome of the first lithography step is a LOR layer with windows for electrical contacts for the air bridge.
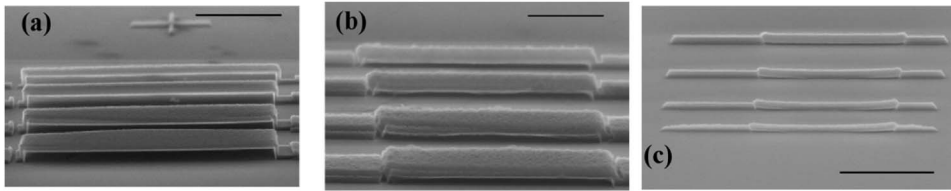
During the second lithography step, MMA/PMMA bilayer resists are spun and baked on top of the LOR layer, followed by electron-beam exposure of patterns for both the air bridge and the electrical leads [Fig. 1(d)]. The chips are developed in MIBK that removes exposed MMA and PMMA, leaving windows in MMA/PMMA bilayer for the air bridge and windows in all three resist layers for the leads [Fig. 1(e)]. Lastly, the device is completed by two metal depositions at 45° and −45° [Fig. 1(f)], so as to deposit metals onto the sidewalls of the windows and ensure contact between the suspended structure and the electrical leads. For the final lift-off process, the three resist layers are removed by PG remover [Fig. 1(g)] and the chips are rinsed in isopropyl alcohol and dried in nitrogen gas.

Examples of completed suspended structures are shown in Fig. 2. The fabrication procedure is quite robust. By controlling the lithography conditions, we are able to fabricate suspended air bridges with considerable ranges in dimensions, including span (l), width (w), and height above the substrate (h). For our purpose of using a suspended bridge as a local top gate, an important parameter is h as it determines the gate efficiency. It can be controlled by LOR's thickness, which may range from 50 nm to 3 μm. Figures 2(a) and 2(b) display two bridges that are suspended 300 and 100 nm above the substrates, respectively. On the other hand, we find that l increases with w and the material's strength. A few bridges with different w are shown in Fig. 2(c). From top to bottom, the bridges are 250, 200, 150, and 100 nm wide, respectively. Clearly, the 100 nm wide bridge sags in the center, while the 250 nm wide bridge remains straight. We note that we are able to create titanium air bridges ~7 μm long *without critical point drying*. Such bridges, or similarly suspended structures, can be used for a number of applications such as local injection of current and nanoelectromechanical devices.

To demonstrate an application of this technique, we fabricate graphene junctions with local top gates (Fig. 3). A completed *p-n-p* device, similar to that shown in Fig. 3(c), is

measured at 260 mK using standard lock-in techniques. The device's source-drain separation is 3.5 μm, with a top gate that covers a ~0.5 μm long segment in the center and is suspended ~100 nm above the substrate.

The device's differential resistance R is plotted in Fig. 4(a) as functions of the back gate voltage V_{bg} (vertical axis) and top gate voltage V_{tg} (horizontal axis). The most visible feature is the red horizontal band at $V_{bg} \sim 14$ V, corresponding to the Dirac point of the entire graphene sheet between the source and drain electrodes. The device mobility is estimated to be ~8500 cm^2/V s. Another notable feature is the diagonal white band, indicating the Dirac point for the top-gated region. The presence of two Dirac points is more easily seen in Fig. 4(b), which plots R versus V_{bg} at three fixed V_{tg}, corresponding to cuts along the dotted lines in Fig. 4(a). Apart from the prominent center peak, the orange curve has an additional shoulder at $V_{bg} \sim -14$ V, and the blue curve at $V_{bg} \sim 28$ V, corresponding to the Dirac point of the top-gated portion. We note that shoulders, rather than full-blown side peaks, are observed at the second Dirac point. This is because the top gate controls less than 15% of the entire device's area. Our results clearly demonstrate individual control of separate regions in the graphene device.

The slope of the white line in Fig. 4(a) yields the ratio of the coupling efficiencies η of the two gates to graphene, and is determined to be ~1.27. From simple geometry consideration, η is given by the gate-device capacitance per unit area, $C = \varepsilon \varepsilon_0 / d$, where ε is the dielectric constant of the gate dielectric (3.9 for SiO$_2$), ε_0 is the permittivity of free space, and d is the gate-device separation. Hence, the coupling ratio is given by $C_{bg}/C_{tg} = (\varepsilon_{bg}/\varepsilon_{tg})/(d_{tg}/d_{bg}) \approx (3.9)(100/300) \approx 1.3$, in excellent agreement with the data. Furthermore, the typical voltage range that the top gates can sustain is ~50–75 V, which is expected increase as the fabrication process is optimized.

Further evidence for the formation of graphene *p-n-p* junctions is provided by transport data at magnetic field of 8 T. For a graphene device with uniform carrier density in high magnetic fields, the formation of quantum Hall edge states leads to a series of conductance plateaus at half integer values of $4e^2/h$. In graphene *p-n-p* junctions, we observe additional conductance plateaus at fractional values (such as 6/5 and 2/3) of e^2/h (Figs. 4(c) and 4(d)), similar to those reported by Ozyilmaz *et al.*[15] As shown in Fig. 4(e), such fractional plateau values arise from the partial and full equilibration of the edge states at the *p-n* interfaces,[15] depending
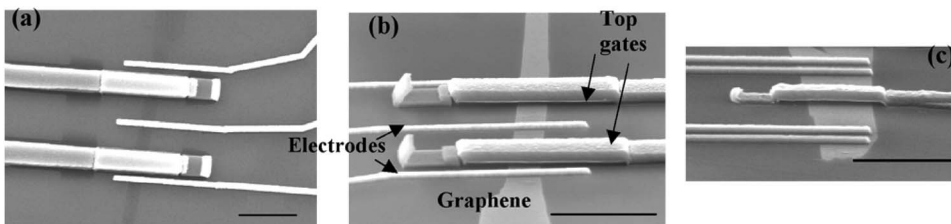

FIG. 3. SEM images of graphene devices with suspended air bridges. [(a) and (c)] Top view. (b) angled view (60°) of the device in (a). Scale bars: 2 μm.
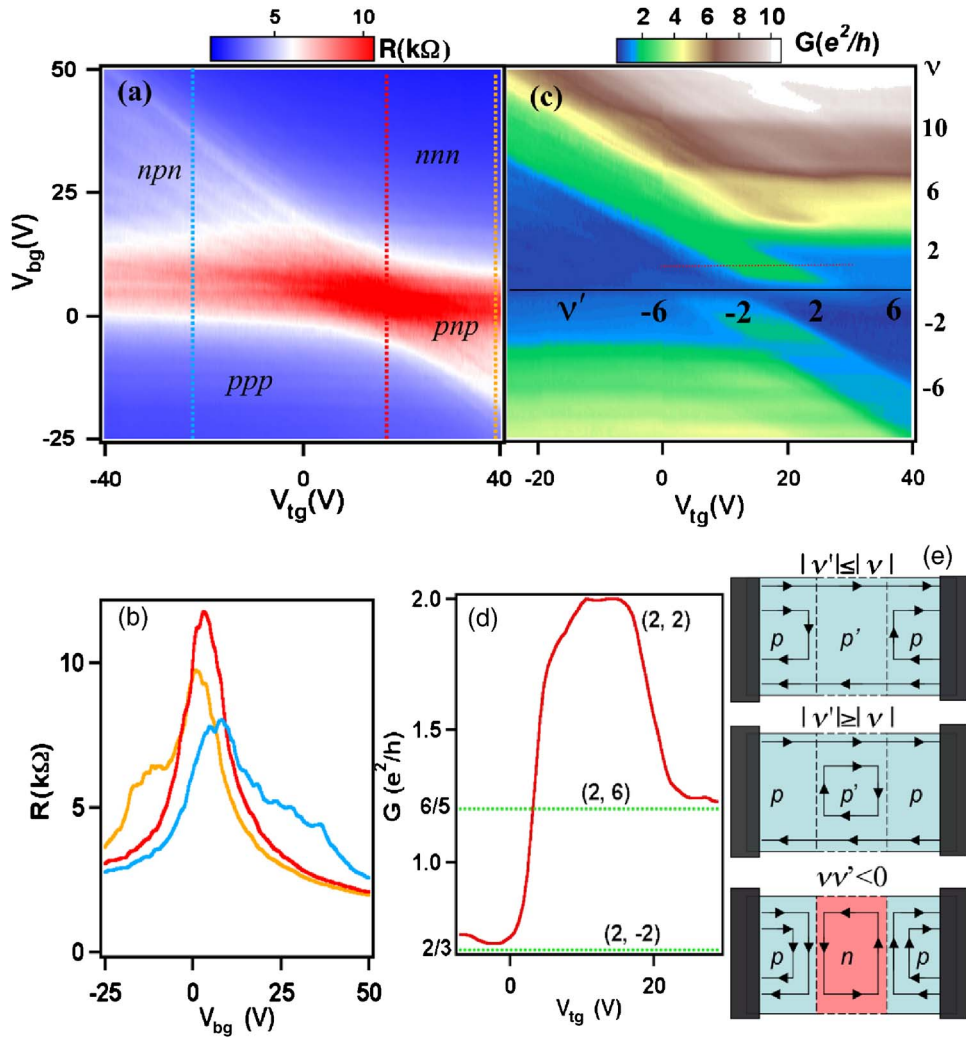
FIG. 4. (Color online) (a) Differential resistance of a graphene device with a center top gate covering $\sim$15% of the device area as functions of V_{bg} and V_{tg}. The dotted lines correspond to the line traces in (b). Doping combinations for different regions are labeled. (b) Differential resistance as a function of V_{bg} at different V_{tg}. (c). Device conductance at 8 T magnetic field as functions of V_{bg} and V_{tg}. For reference, the filling factors ν and ν' are also labeled (the latter at $\nu=0$). They are related to the gate voltages by $n_c h/eB$, where h is the Planck's constant, e is the electron charge, and n_c is the charge density, given by $C_{bg}V_{bg}/e$ in the uncovered region, and $(C_{bg}V_{bg}+C_{tg}V_{tg})/e$ in the top-gated region. (d). Line trace along the red line in (c). The bracketed numbers correspond to (ν, ν') for the plateaus. (e). Schematics of edge state propagation for different values of (ν, ν').

on the signs and magnitudes of ν and ν' and the filling factors in the uncovered and top-gated regions, respectively. The values of ν' (at $\nu=0$) and ν are labeled at corresponding gate voltages in Fig. 4(d). In particular, we note that the conductance plateau with the full value of $2e^2/h$ was not observed in Ref. 15, due to the strong effect of backscattering on states with $|\nu|=|\nu'|$. In contrast, we observed a clear plateau at $2e^2/h$ [Fig. 4(d)], establishing that transport in our p-n-p junctions experiences relatively weak backscattering.

In conclusion, we have developed a multilevel lithography process to fabricate graphene p-n-p junctions with suspended top gates, which exhibit high mobility and local control of doping density and type. Observation of the previously unreported $2e^2/h$ quantum Hall plateau in similar p-n-p junctions demonstrates that our procedure produces clean junctions. In the long term, this versatile technique can also be significantly improved and extended to fabricate other types of suspended structures such as moving parts in microelectromechanical devices.

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