

Airgap Local Gating of Graphene

pnp junctions with contactless top gates

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P-N Junctions

- Doping silicon with impurities to form n-type and p-type semiconductor
- The diffusion potential due to different carriers forms an electric field through equilibrium

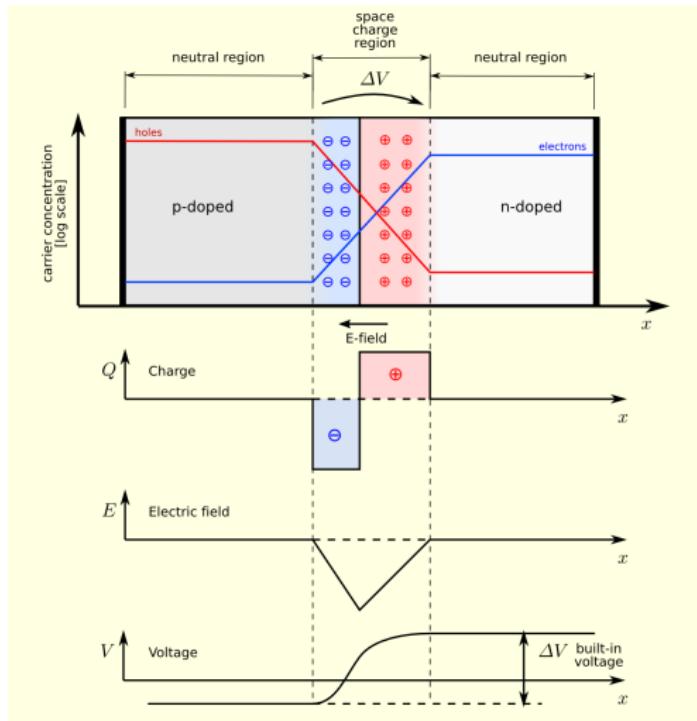


Figure 1: P-N Junctions

Graphene: Semimetal

- Zero-gap semiconductor with linear energy dispersion relation
- Dirac cones, massless Dirac fermions
- Exceptional mobility, current-carrying capacity and thermal conductivity

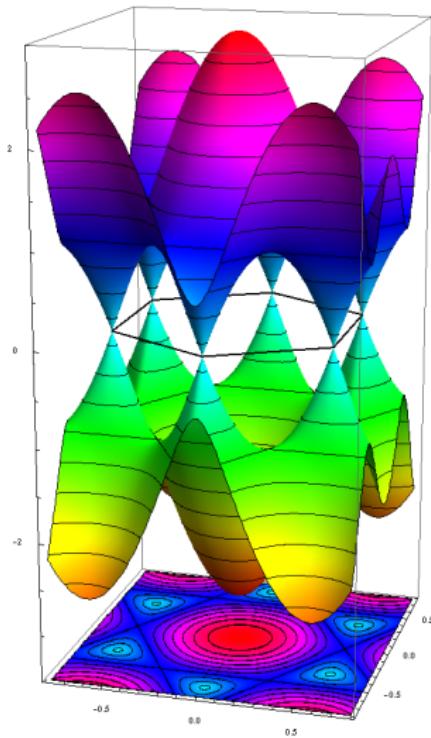


Figure 2: Graphene Band Structure

P-N Junctions in Graphene

- Both carrier type and density can be electrostatically controlled
- In situ creation and control of p-n junctions (by a local top gate and a global back gate)
- Quantum Hall plateaus with fractional values, Veselago lensing and Klein tunneling

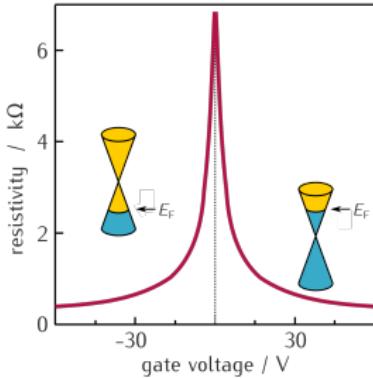


Figure 3: Graphene carrier control

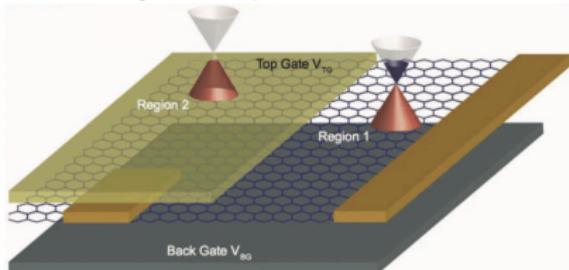


Figure 4: Graphene P-N Junctions[1]

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Why Graphene?

- Advantages of graphene p-n junctions
- A fascinating system for fundamental studies in condensed matter physics (at that time)
- Relatively mature technics: MOSFET?

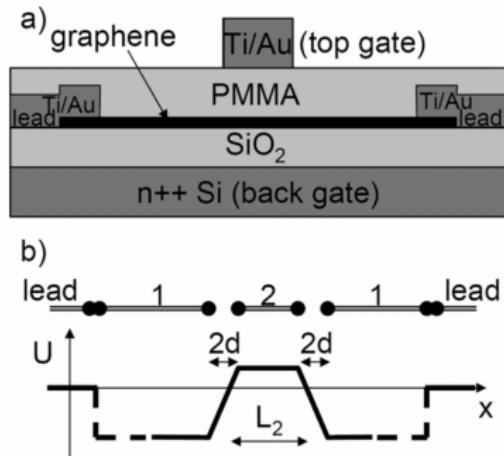


Figure 5: Device which realizes p-n-p junctions in graphene and the simplified model for the electrochemical potential[2]

Why Suspended top gates?

- Organic/metal oxide layer VS airgap?
- Dramatically enhanced mobility in suspended graphene devices
- Damage or doping to the single atomic layer

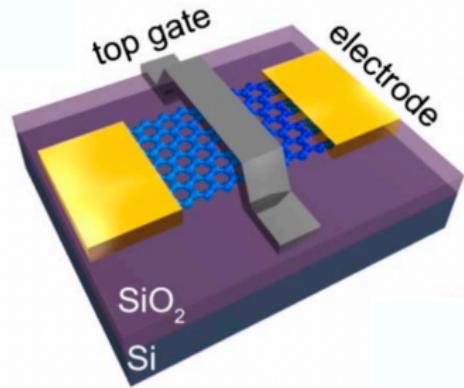


Figure 6: Graphene p-n-p junctions with suspended local top gate[3]

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Fabrication Procedure

- Two lithography steps and a single metal deposition step
- Only exposed to conventional resists and developers
- No special equipment for depositing gate dielectrics/releasing sacrificial layers
- Compatible with annealing procedures that improve device mobility

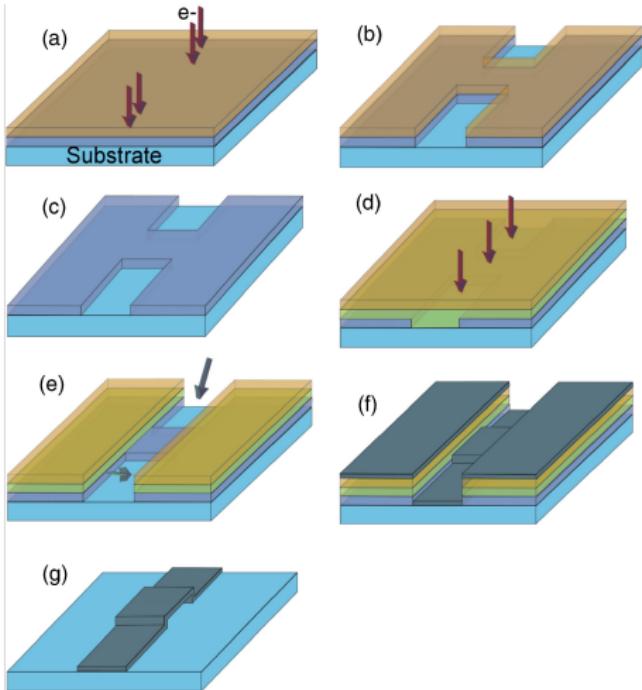


Figure 7: Fabrication Procedure[4]

Samples

- Fabricate suspended air bridges with considerable ranges in dimensions (l , w , h)
- Gate efficiency can be controlled by LOR's thickness (h ranges from 50 nm to 3 μm)
- Robust, can be used for a number of applications (local injection of current, nanoelectromechanical devices)

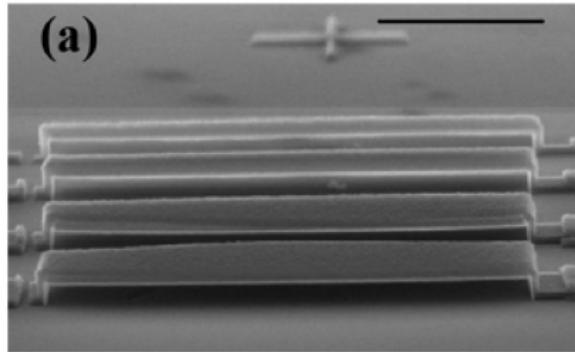


Figure 8: Top Gate Sample[4]

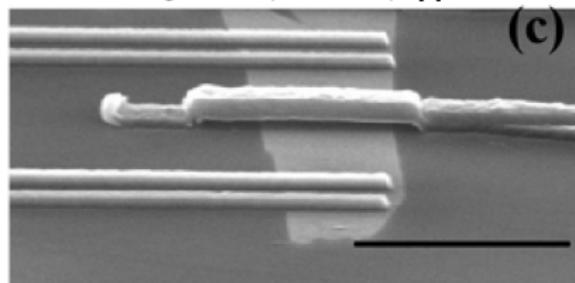


Figure 9: Device Sample[4]

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Differential Resistance

- Corresponding to the Dirac point of the entire/local graphene
- Individual control of separate regions in the graphene device
- $k = \eta = C_{BG}/C_{LG} = \varepsilon_{BG}d_{LG}/d_{BG}$

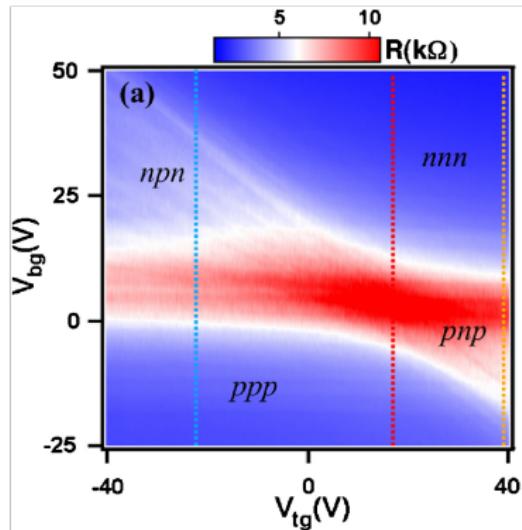


Figure 10: Differential Resistance Control[4]

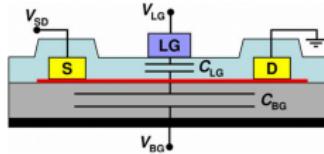


Figure 11: Gate-device Capacitance[5]

Quantum Hall Effect

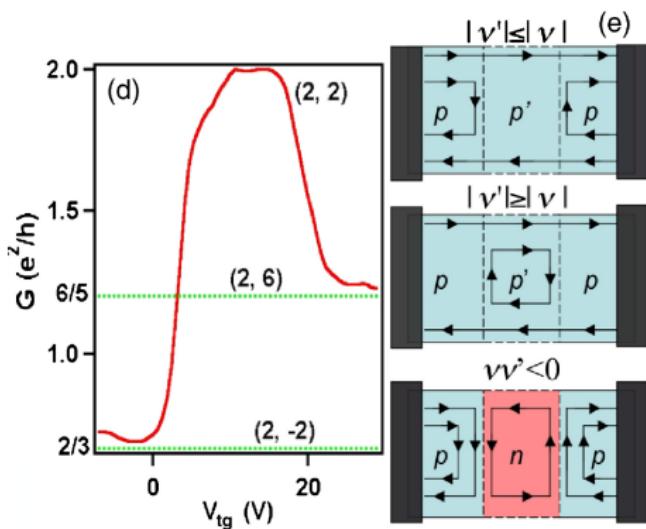
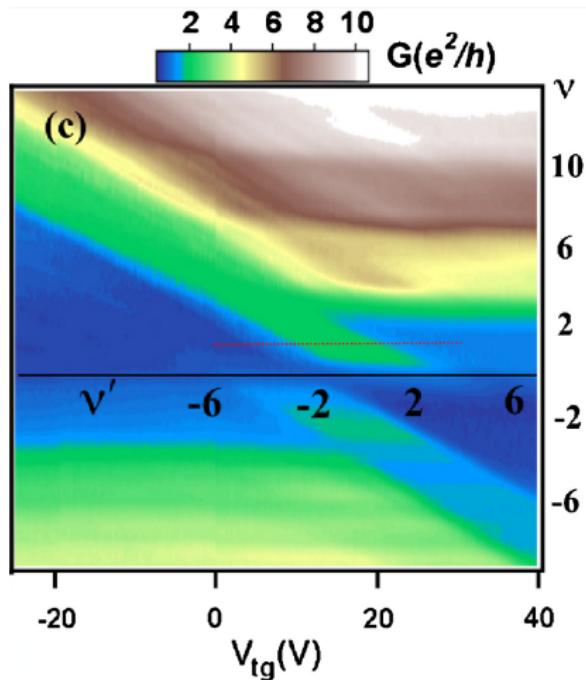


Figure 12: Quantum Hall edge states at magnetic field of 8T[4]

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- In conclusion, we have developed a multilevel lithography process to fabricate graphene p-n-p junctions with suspended top gates, which exhibit high mobility and local control of doping density and type.
- Observation of the previously unreported $2e^2/h$ quantum Hall plateau in similar p-n-p junctions demonstrates that our procedure produces clean junctions.
- In the long term, this versatile technique can also be significantly improved and extended to fabricate other types of suspended structures such as moving parts in microelectromechanical devices.

Reference:

- [1]J. R. Williams, L. DiCarlo, and C. M. Marcus, Science 317, 638 (2007).
- [2]B. Huard, J. A. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, Phys. Rev. Lett. 98, 236803 (2007).
- [3]Velasco, J.; Liu, G.; Jing, L.; Kratz, P.; Zhang, H.; Bao, W.; Bockrath,M.; Lau, C. N. Phys. Rev. B 2010, 81 (12), 121407.
- [4]G. Liu, J. Velasco, Jr., W. Bao, and C. N. Lau, Appl. Phys. Lett. 92, 203103 (2008).
- [5]B. Ozyilmaz, P. Jarillo-Herrero, D. Efetov, D. A. Abanin, L. S. Levitov, and P. Kim, Phys. Rev. Lett. 99, 166804 (2007).