

## Connectors, I/O Conditioning

The diagram illustrates the hardware connections for the BPS and CT modules. It includes three main sections: connector wiring, power supply filtering, and signal conditioning.

### Connector J1: BPS SUPPLY

Connector J1 (Molex 43045-1200) is used for the BPS supply and signals. The wiring is as follows:

- Pin 1: +12V
- Pin 2: BPS.FRONT.PwR
- Pin 3: BPS.FRONT.SIG
- Pin 4: BPS.REAR.PwR
- Pin 5: BPS.REAR.SIG
- Pin 6: BPS.FRONT.GND
- Pin 7: BPS.FRONT.GND
- Pin 8: BPS.FRONT.GND
- Pin 9: BPS.FRONT.OUT
- Pin 10: Key Pin 10
- Pin 11: BPS.REAR.GND
- Pin 12: BPS.REAR.OUT

### Connector J2: Main I/O

Connector J2 (Molex 43045-1200) is used for the Main I/O signals. The wiring is as follows:

- Pin 1: +12V
- Pin 2: SHUTDOWN\_IN
- Pin 3: BSPD.CUR\_SEN.EXC
- Pin 4: CT\_SIG\_IN
- Pin 5: BSPD\_SDC
- Pin 6: SDC\_IND\_A
- Pin 7: SHUTDOWN\_OUT
- Pin 8: BSPD.CUR\_SEN.GND
- Pin 9: CT\_SIG
- Pin 10: SDC\_IND\_K
- Pin 11: Key Pin 12
- Pin 12: GND

### Power Supply Filtering

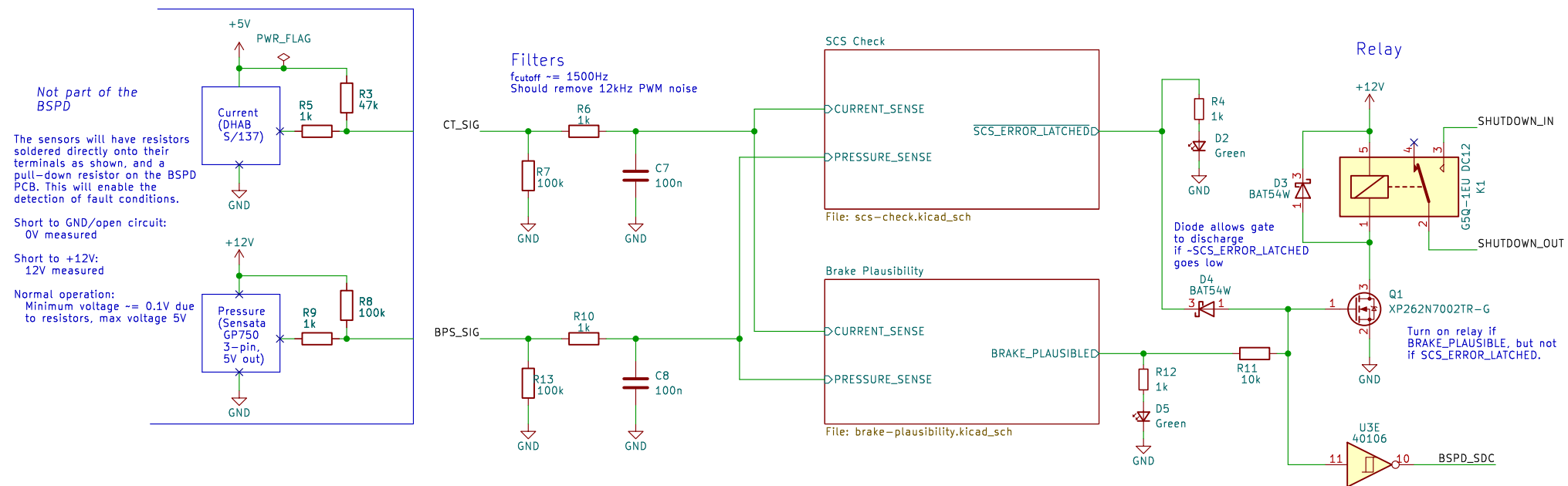
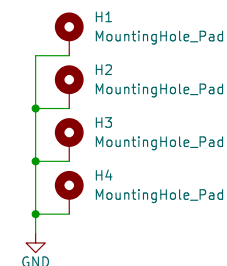
The power supply section shows a +12V source connected to a 100uF capacitor (C6) and a PWR\_FLAG signal. The PWR\_FLAG signal is also connected to the BPS module.

### Signal Conditioning

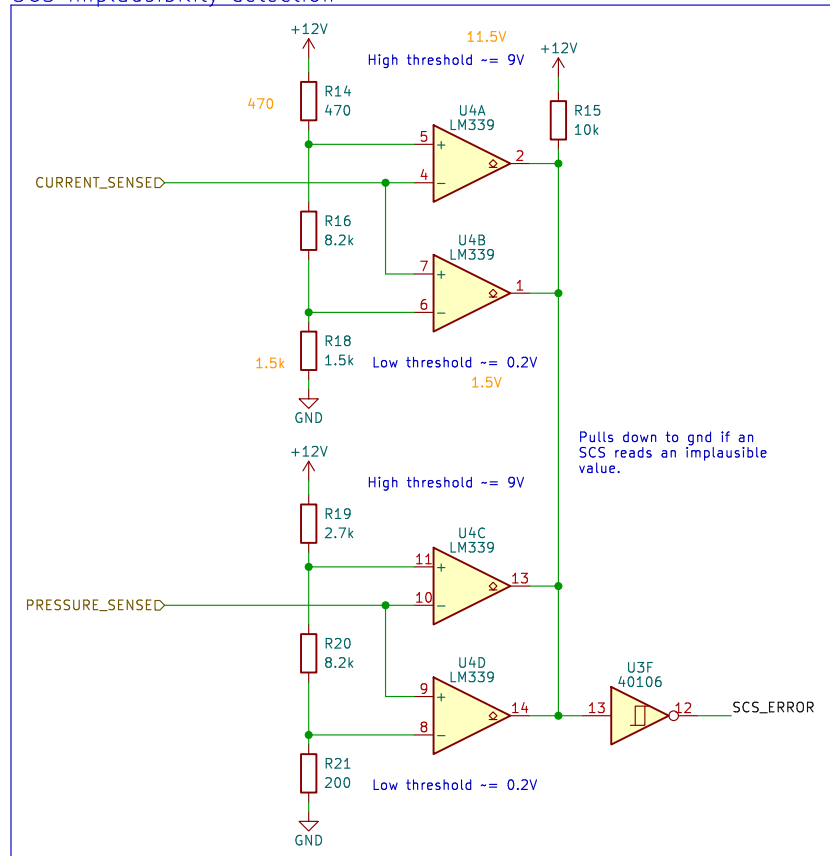
The signal conditioning section shows three op-amp chips (U3C, U3D, U3A) used for signal processing:

- U3C (TLV9104IRUCR):** Buffers the CT\_SIG\_IN signal to CT\_SIG.
- U3D (TLV9104IRUCR):** Buffers the BPS.FRONT.SIG signal to BPS.FRONT.OUT.
- U3A (TLV9104IRUCR):** Buffers the BPS.REAR.SIG signal to BPS.REAR.OUT.

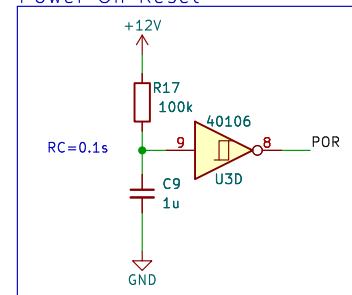
The BPS module also includes a Solder Jumper (JP1) for the BPS\_SIG signal, which is connected to the BPS module's output.



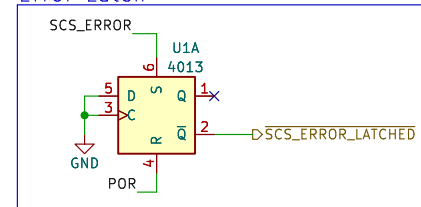
## SCS implausibility detection



## Power On Reset



## Error Latch



Vehicle: STAG 12

Drawn By: Ray Wang, Joe Pater

Checked By: Marek Frodyma, Tim Brewis

CAD Part:

**SUFST – Southampton University Formula Student Team**

Sheet: SCS Check

File: scs-check.kicad\_sch

**Title: BSPD**

Size: A4

Date: 2025-12-14

KiCad E.D.A. 9.0.4

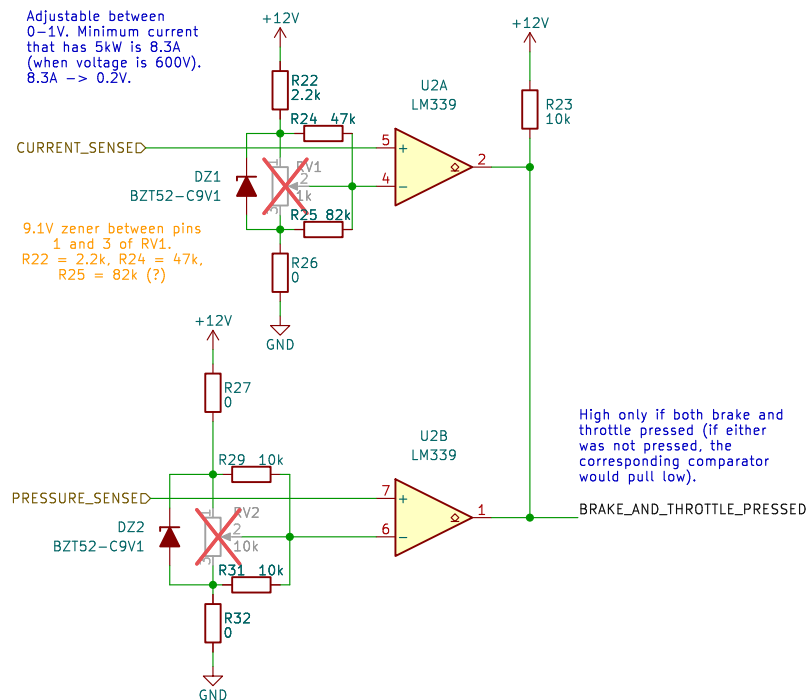
**Rev: 1.3.0**

Id: 4/3

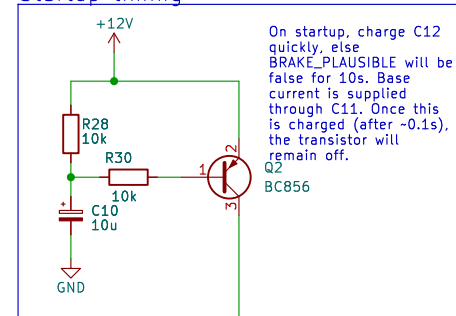


## Comparators

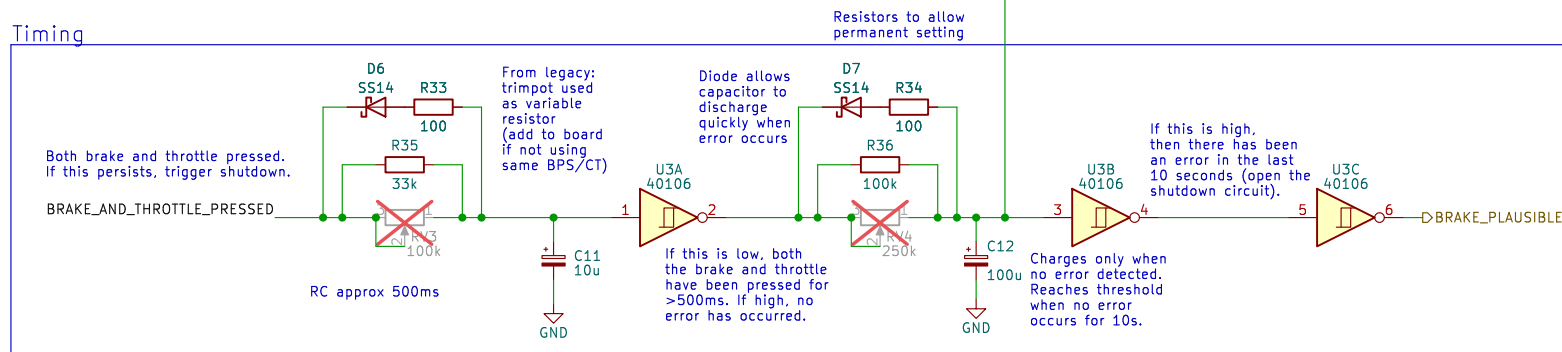
Adjustable between  
0-1V. Minimum current  
that has 5kW is 8.3A  
(when voltage is 600V).  
8.3A  $\rightarrow$  0.2V.



## Startup timing



### Timing



Vehicle: STAG 12

Drawn By: Ray Wang, Joe Pater

Checked By: Marek Frodyma, Tim Brewis

CAD Part:

**SUFST – Southampton University Formula Student Team**

Sheet: Brake Plausibility

File: brake-plausibility.kicad\_sch

Title: BSPD

Size: A4

Date: 2025-12-14

KiCad E.D.A. 9.0.4

Rev: 1.3.0

Id: 5/3

