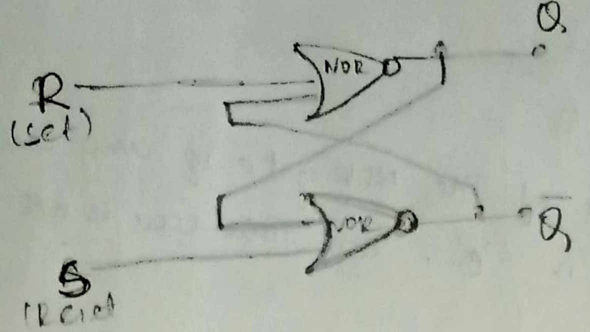
4/1/2023

SR LATCHE (Active High set)



	Input		output	
	S	R	Q	$\bar{Q}$
	0	0	Q	$\bar{Q}$
	0	1	0	1
1st	1	0	1	0
	1	1	Not valid	

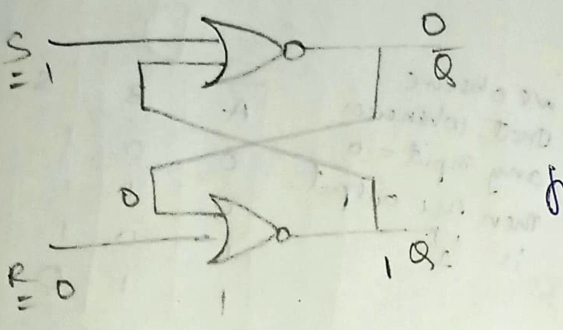
NOTE:
whenever,
The input = 1
the output is '0'

Truthtable for
NOR Gate.

A	B	D
0	0	1
0	1	0
1	0	0
1	1	0

case I :-

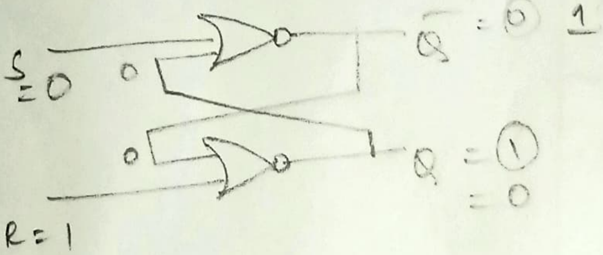
S = 1 & R = 0



from this
$Q = 1$, $\bar{Q} = 0$

case II :-

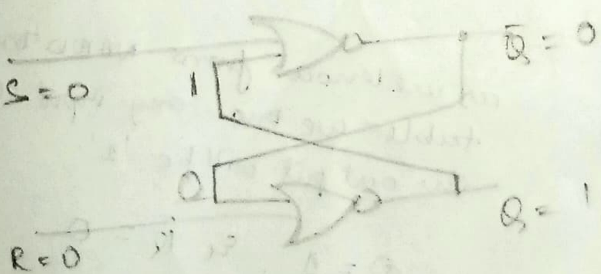
S = 0 & R = 1



from this
$Q = 0$, $\bar{Q} = 1$

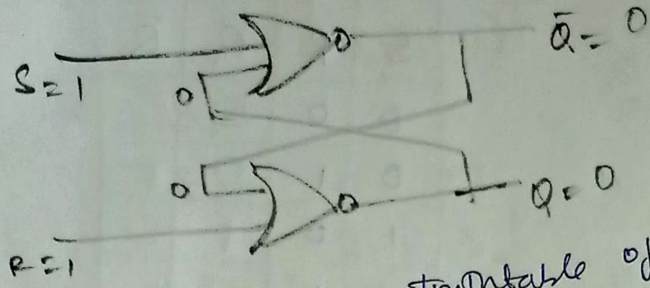
case III :-

S = 0 & R = 0



from this, $Q = Q$; $\bar{Q} = 0$
whenever The inputs are 0 & 0
the previous Q & $\bar{Q}$ values
are retained.

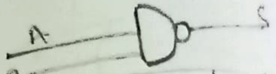
Case - IV : S = 1 & R = 1



as we know from the truthtable of the NOR gate if any one the input is '1' then the output is '0'. So This case is not valid in D.E.

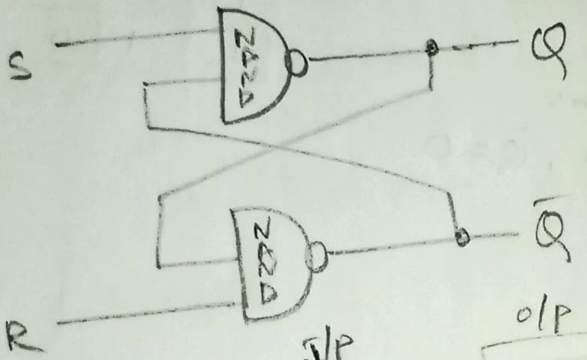
SR - Latch with NAND Gates (Active low set)

Truth table for NAND Ga



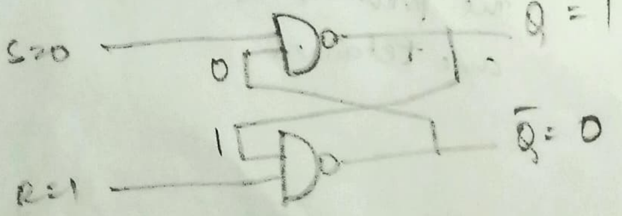
A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

we observe that whenever any input = 0 then the output is '1'



I/P		O/P	
S	R	Q	$\bar{Q}$
0	0	-invalid-	
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

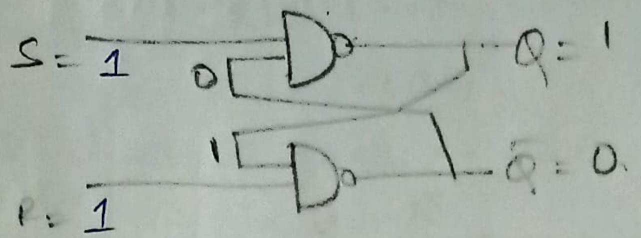
case(1) : S = 0 , R = 1



as we know from NAND truth table we know any input = 0 the output will be '1'

Q = 1 & $\bar{Q}$ = 0

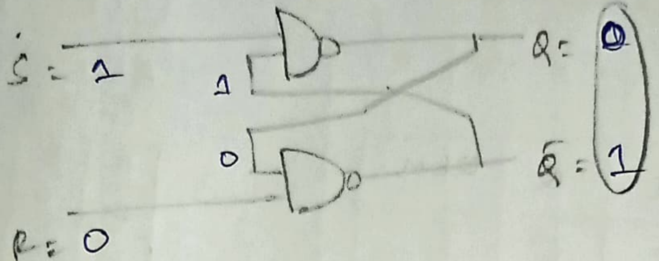
case (2) : S = 1 , R = 1



whenever the inputs are 1 & 1 the previous Q & Q̄ values are retained.

Q = 1 , Q̄ = 0

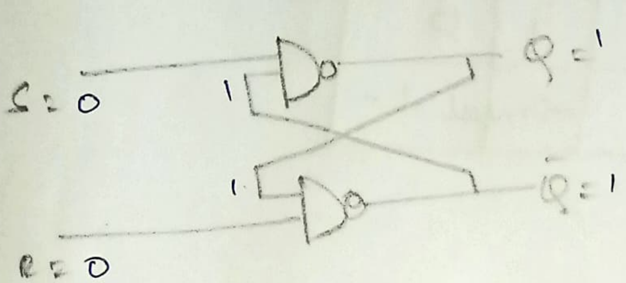
case (3) : S = 1 , R = 0



① 0 = Q

② 1 = Q̄

case (4) : S = 0 , R = 0.

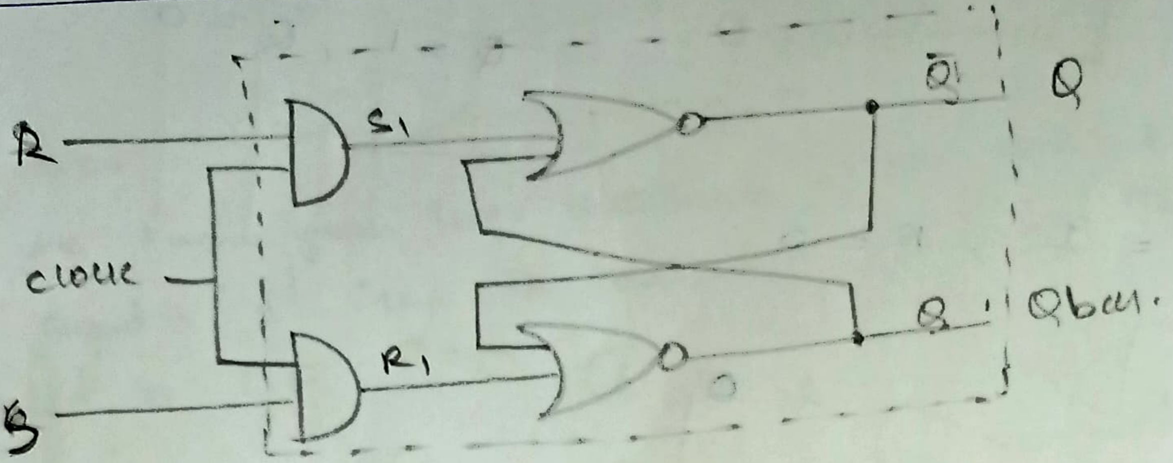


we know that from truth table of NAND Gate we say any input 0 Then output is '1'. So this case is not valid.

Q = 1 & Q̄ = 1

SR - FLIP-FLOP

SR - FLIP FLOP for (NOR Gate)



NOR Gate
Truthtable

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

AND Gate
Truthtable

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

CLK	S	R	Q	Qbar.
0	X	X	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1.	1	—Invalid —	

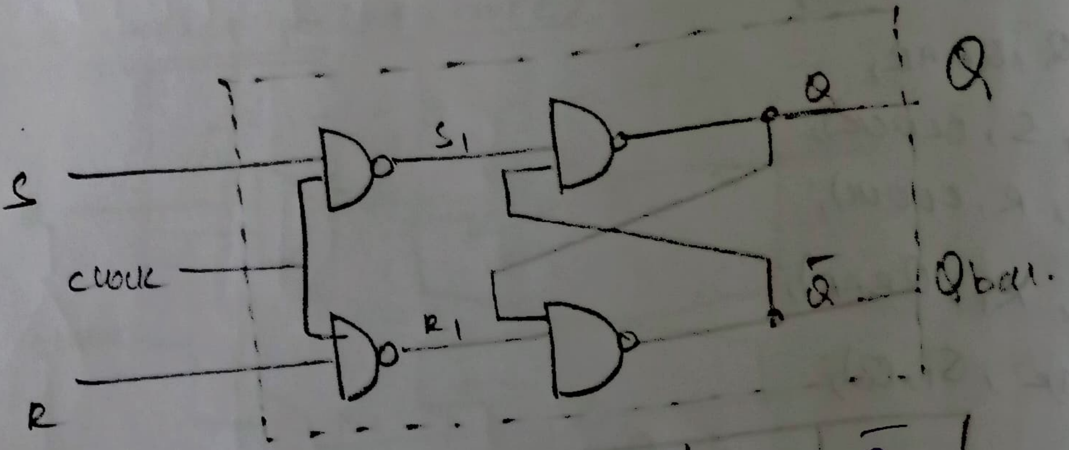
Verilog code for SRFLIPFLOP

```
module SRFF (S, R, CLOCK, Q, QBAR);
   input S, R, CLOCK;
   output Q, QBAR;
  and (R1, S, CLOCK);
  and (S1, R, CLOCK);
   nor (Q, R1, QBAR);
   nor (QBAR, S1, Q);
 end module.
```

SR- FLIP-FLOP for NAND Gate

NAND Gate Truth table

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

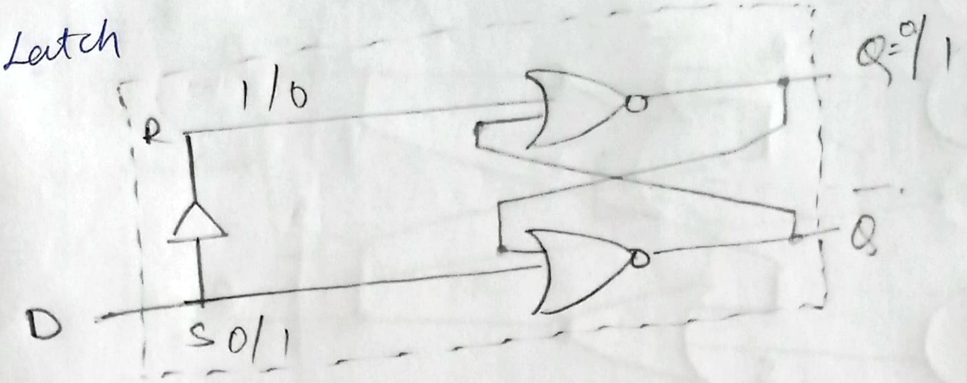


CLK	S	R	Q	$\overline{Q}$
0	X	X	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	-Invalid-	

6/1/2023

D-Latch

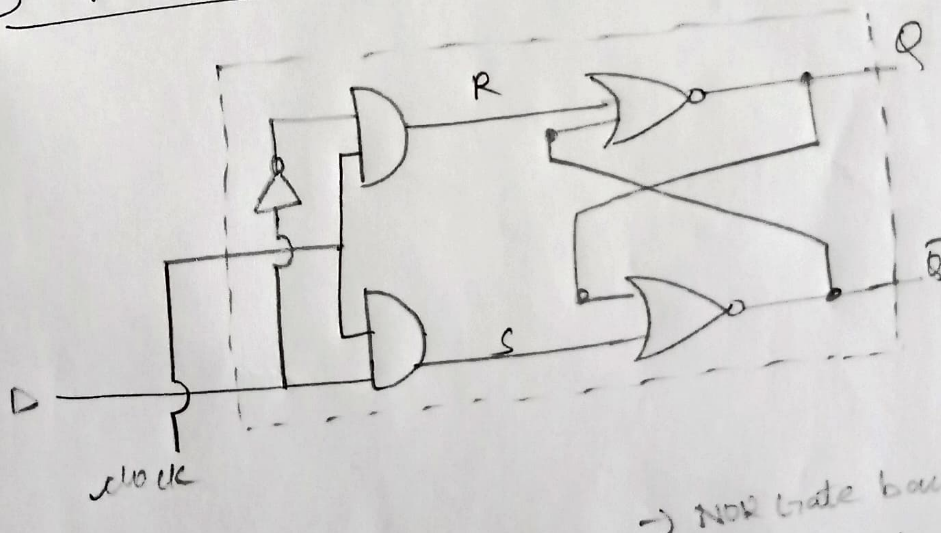
also called as Data latch, Delay latch, Transparent Latch



Truthtable:

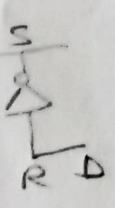
D	Q
0	0
1	1

D-FLIP-FLOP

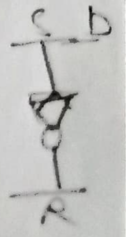


CLOCK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

-> NOR Gate based latch.
(Invertor goes from R to S)

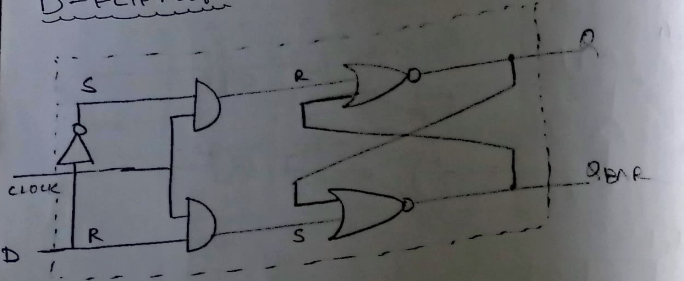


-> NAND Gate based latch
(Inverter goes from S to R)

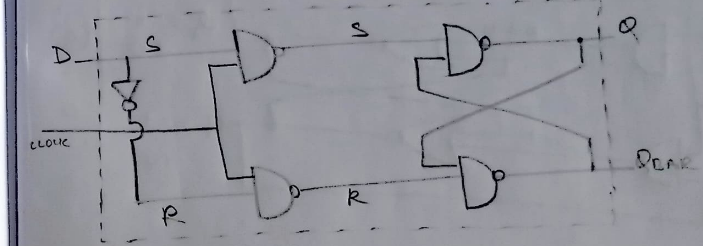


D-Latch

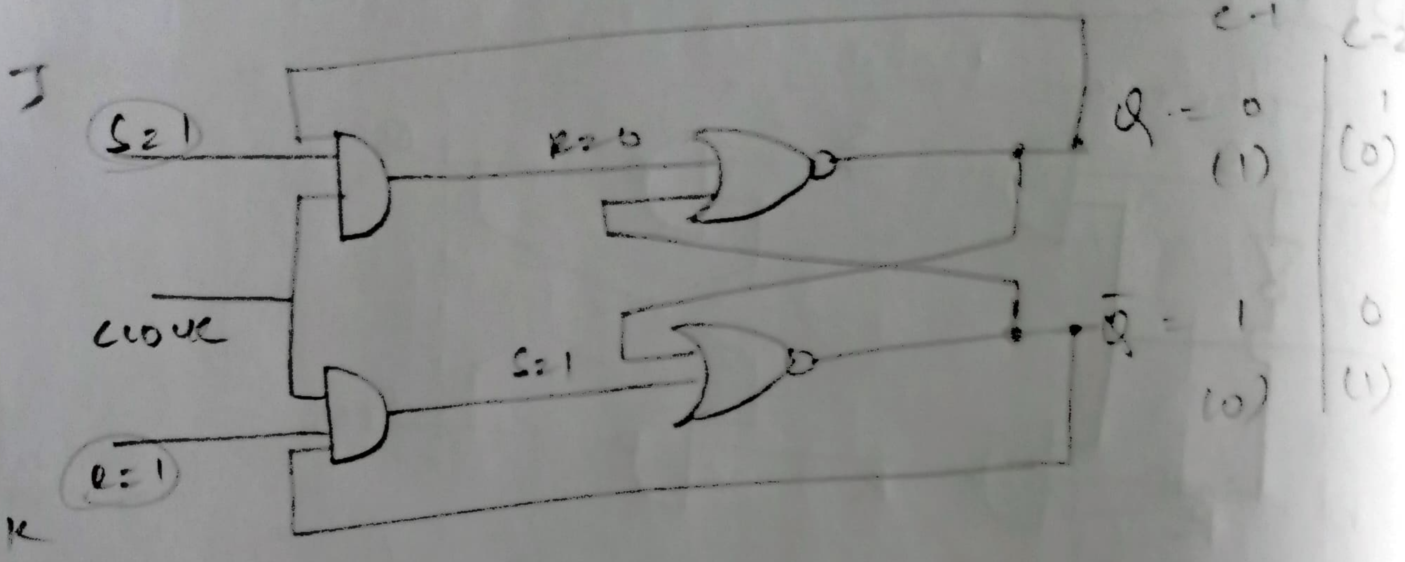
D-FLIPFLOP (NOR GATE)



D-FLIP FLOP (NAND GATE)



JK - FLIP FLOP



J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	Q̄

FULL ADDER USING PAL & PLA

Truth Table:

A	B	C	sum	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Kmaps:

for sum:

C \ AB	00	01	11	10
0		1		1
1	1		1	

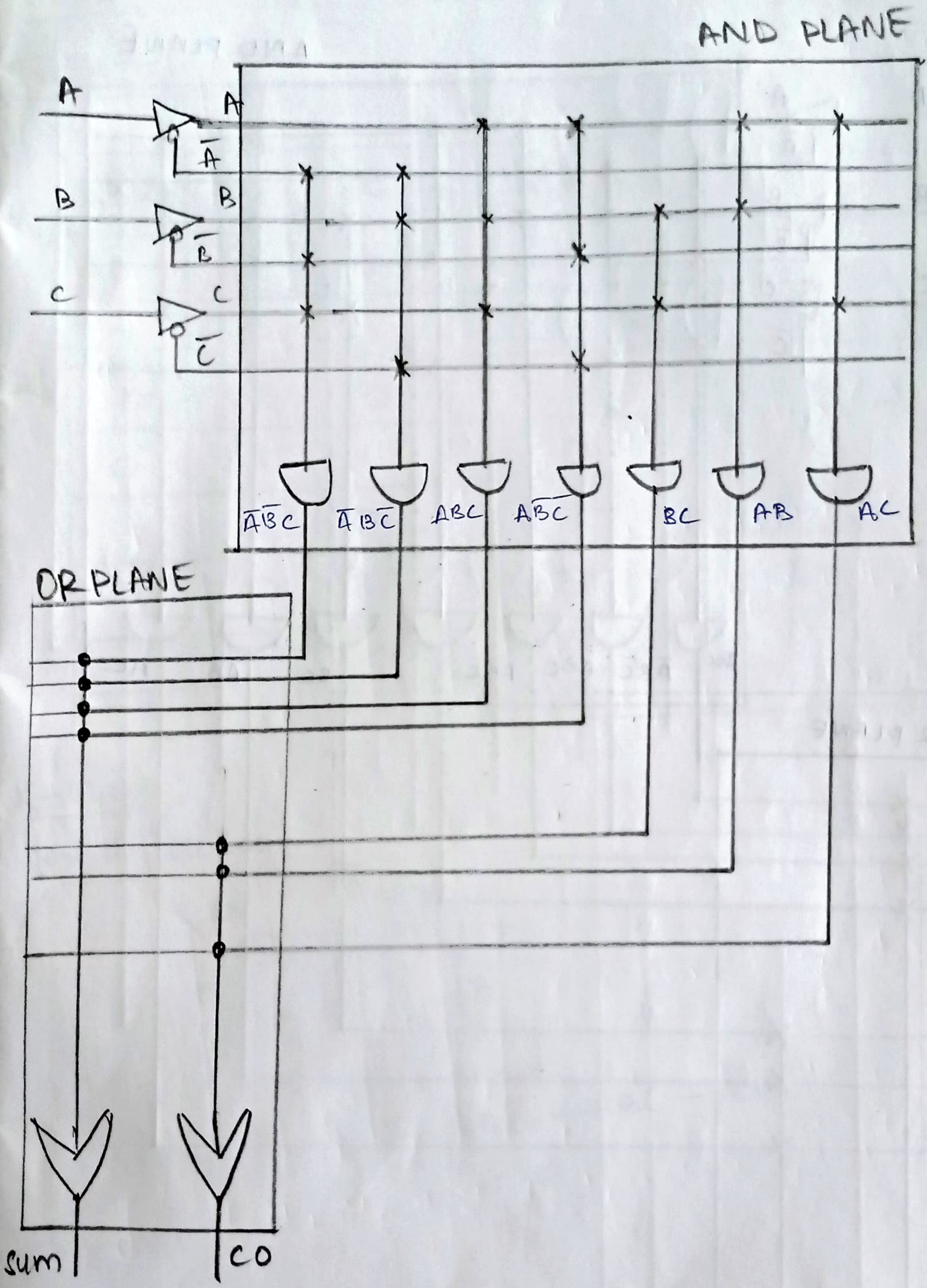
$$sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$$

for co:

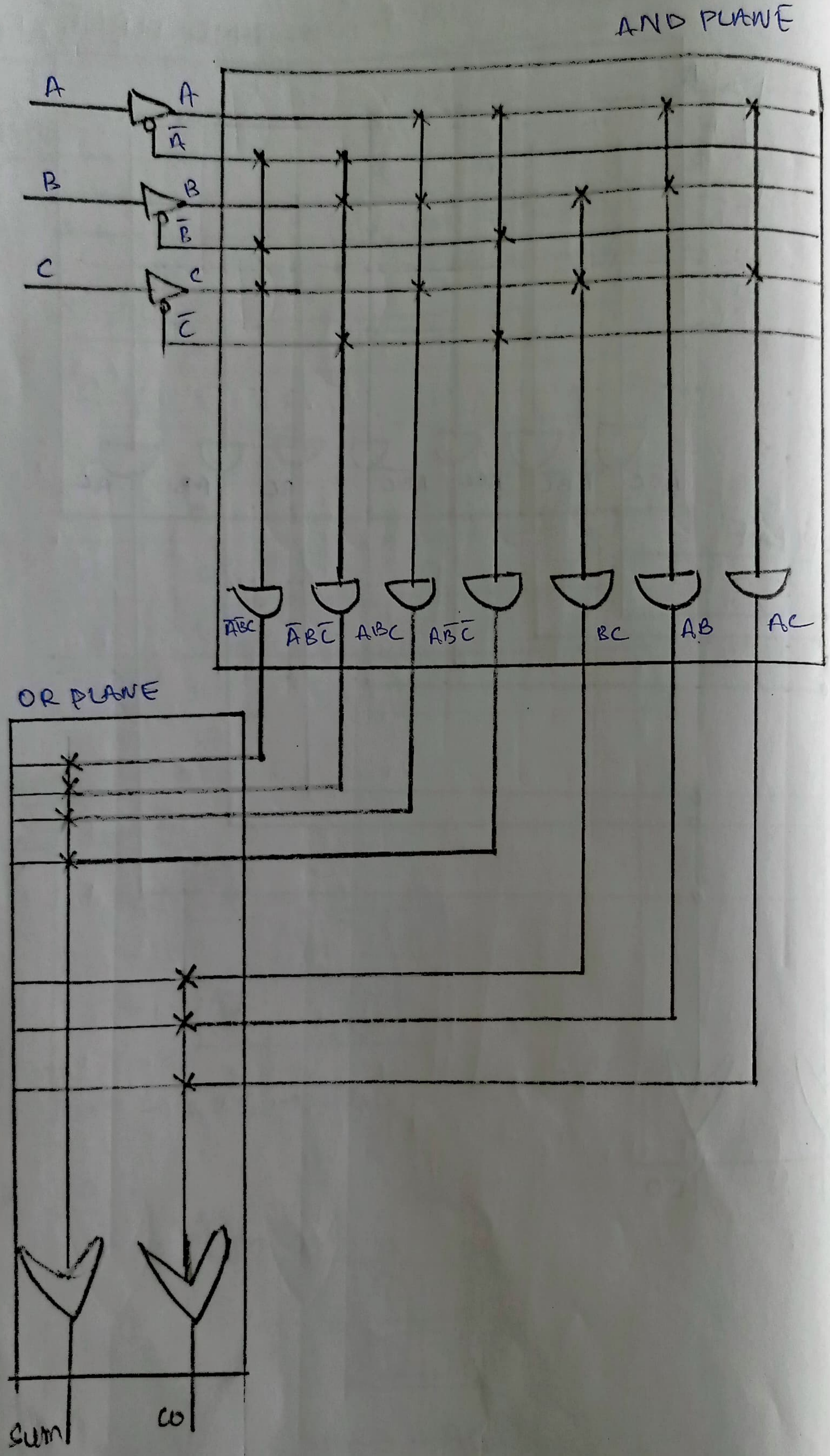
C \ AB	00	01	11	10
0			1	
1		1	1	1

$$CO = BC + AB + AC$$

PAL:


AND PLANE
A
A
$\bar{A}$
B
B
$\bar{B}$
C
C
$\bar{C}$
$\bar{A}\bar{B}C$
$\bar{A}B\bar{C}$
ABC
$A\bar{B}\bar{C}$
BC
AB
AC
OR PLANE
sum
CO

PLA :


AND PLANE
A
A
$\bar{A}$
B
B
$\bar{B}$
C
C
$\bar{C}$
$\bar{A}\bar{B}C$
$\bar{A}B\bar{C}$
ABC
$A\bar{B}\bar{C}$
BC
AB
AC
OR PLANE
sum
co

FULL SUBTRACTOR USING PAL & PLA

Truthtable:

A	B	C	Difference	Borrow.
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-maps:

for difference:

C \ AB	00	01	11	10
0		1		1
1	1		1	

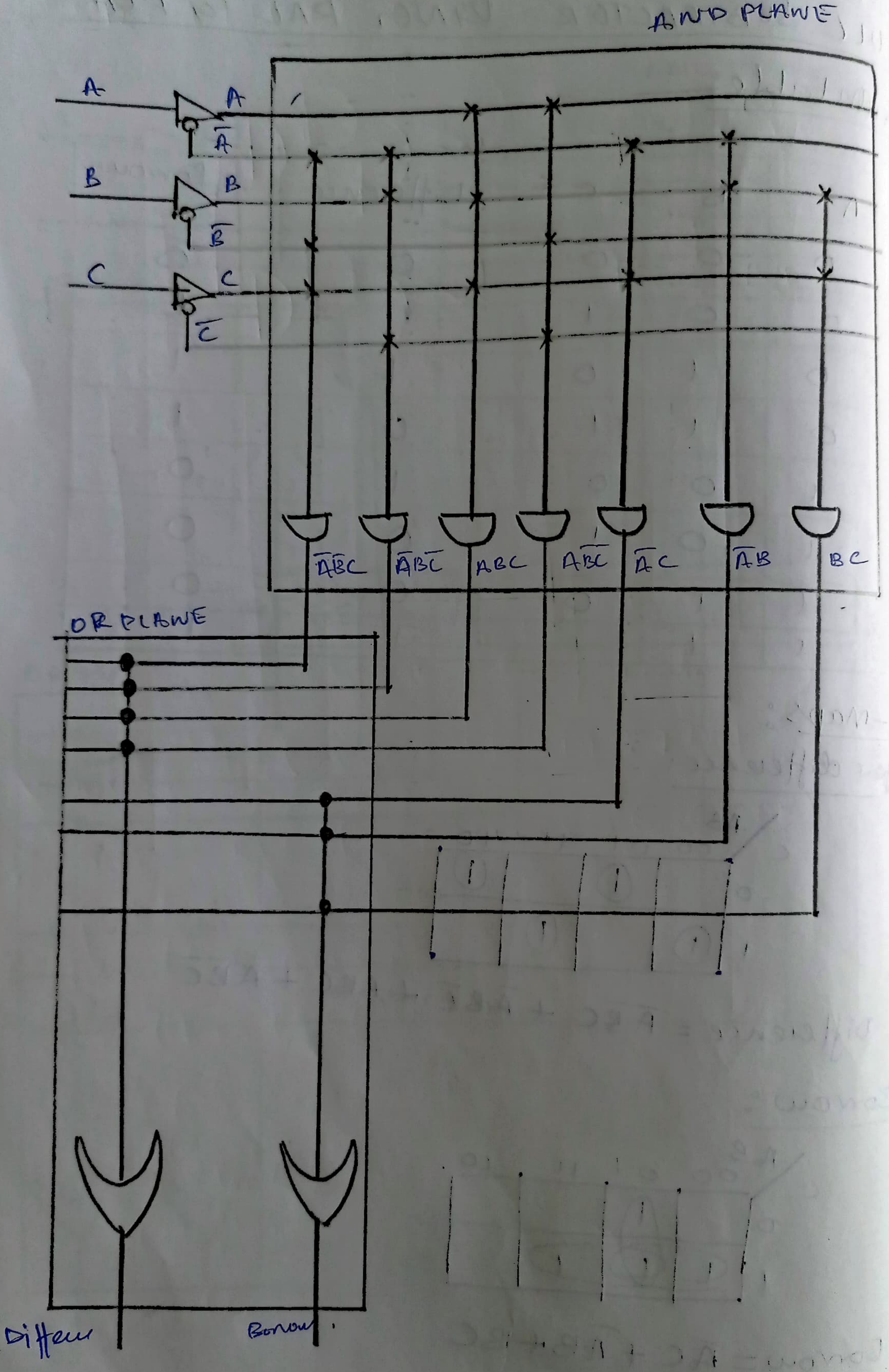
Difference = $\bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + A\bar{B}\bar{C}$

Borrow:

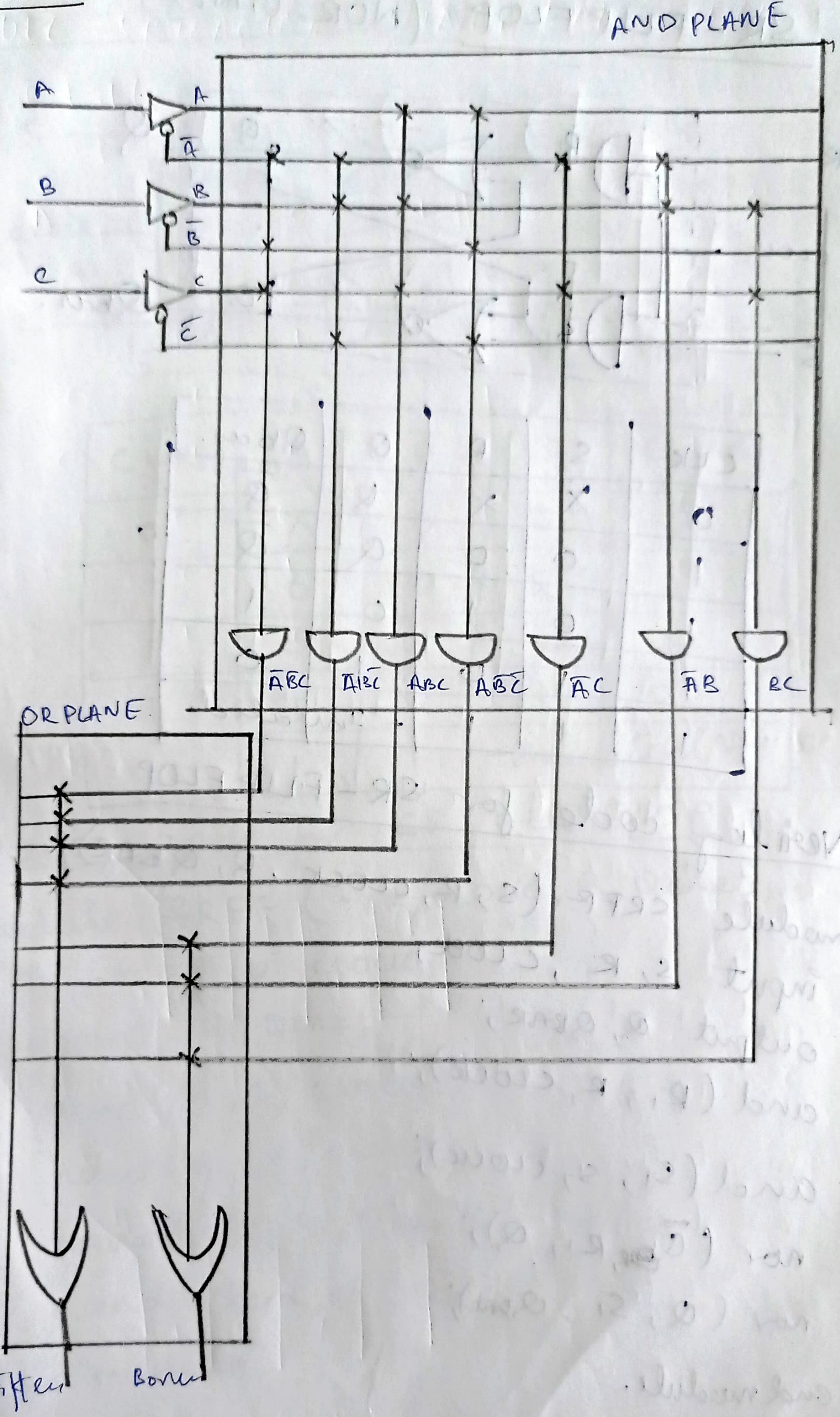
C \ AB	00	01	11	10
0		1		
1	1	1	1	

Borrow = $\bar{A}C + \bar{A}B + BC$.

PAL :


AND PLANE
A
A
$\bar{A}$
B
B
$\bar{B}$
C
C
$\bar{C}$
$\bar{A}\bar{B}C$
$\bar{A}B\bar{C}$
ABC
$A\bar{B}\bar{C}$
$\bar{A}C$
$\bar{A}B$
BC
OR PLANE
Differ
Borrow

PLA:


AND PLANE
A
A
$\bar{A}$
B
B
$\bar{B}$
C
C
$\bar{C}$
$\bar{A}\bar{B}C$
$\bar{A}B\bar{C}$
ABC
$A\bar{B}\bar{C}$
$\bar{A}C$
$\bar{A}B$
BC
OR PLANE
Differ
Borrow