

Q MARKS QUESTIONS & ANSWERS

UNIT-1

Q) Prove that $AB\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} = \bar{C}$.

sol Let $y = AB\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$
 $= \bar{A}\bar{C}(B+\bar{B}) + \bar{A}\bar{C}(B+\bar{B})$
 $= \bar{A}\bar{C} + \bar{A}\bar{C}$
 $= \bar{C}(\bar{A}+A) \Rightarrow y = \bar{C}$

Hence proved.

2) convert the given function into other canonical form.
 $F(a, b, c) = \bar{a}b + \bar{b}c + ac$

sol Given, $F(a, b, c) = \bar{a}b + \bar{b}c + ac$

Truth table for given function

a	b	c	$\bar{a}b$	$\bar{b}c$	ac	f
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	1	0	0	1
0	1	1	1	0	0	0
1	0	0	0	0	1	1
1	0	1	0	1	0	0
1	1	0	0	0	1	1
1	1	1	0	0	1	1

$$\begin{aligned}
 F(a, b, c) &= \text{IM}(0, 4, 6) \\
 &= (a+b+c)(\bar{a}+\bar{b}+c)(\bar{a}+b+c)
 \end{aligned}$$

3) Define minterms & Maxterms:

Minterms: (m_i) (2^m)

The product of the input variables, either in true or complemented form is called a minterm.

Maxterms: (M_j) (2^m)

The sum of the input variables, either in true or complemented form is known as maxterms.

4) Define the terms implicant & prime implicant?

Implicant:

A product term of a function is said as implicant.

Prime Implicant:

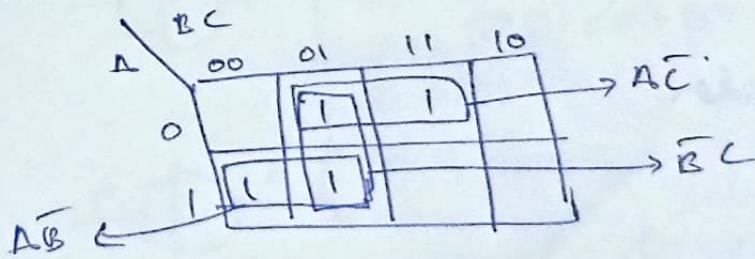
A prime implicant is a product term obtained by combining the maximum possible number of adjacent cells in the map.

Q) Define prime implicant & essential prime implicant with exp?

Essential prime Implicant:

The prime implicant is said to be essential PI if it is the only prime implicant that covers the minterm.

Example: express $F = AB + \bar{A}C + \bar{B}C$



$\bar{A}B$ & $A\bar{C}$ are essential prime implicant.
 $\bar{B}C$ is redundant.

6) Given Boolean function $F = xy\bar{z} + \bar{x}\bar{y}z + xy^2$
Simplify the algebraic expression using Boolean algebra.

Ans
$$\begin{aligned} F &= xy\bar{z} + \bar{x}\bar{y}z + xy^2 \\ &= \bar{y}z [x + \bar{x}] + xy^2 \\ &= \bar{y}z + xy^2 \\ &= z [\bar{y} + xy] \\ F &= z [\bar{y} + x] \end{aligned}$$

(from distributive law:
 $A + \bar{A}B = \bar{A} + B$)

7) State & prove DeMorgan's Law?

Ans Statement:
Two theorems that are important part of Boolean algebra were proposed by DeMorgan.
→ The first theorem states that the COMPLEMENT of a PRODUCT is EQUAL to the SUM of the COMPLEMENTS

$$\overline{AB} = \overline{A} + \overline{B}$$

→ The second theorem states that the COMPLEMENT of SUM is equal to PRODUCT of the complements.

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

Proof:

\leftarrow Backside.

2) Represent the Boolean Expression in Kmap

$$f = \bar{b} + a\bar{c} + \bar{a}cd.$$

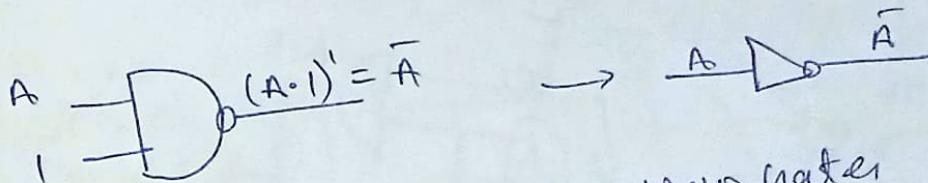
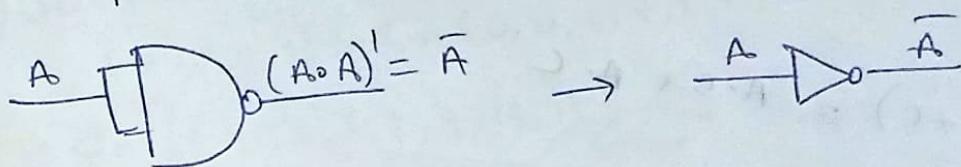
Sol) Given, $f = \bar{b} + a\bar{c} + \bar{a}cd$.

3-input - a, b, c $= 0 + 10 + 011$

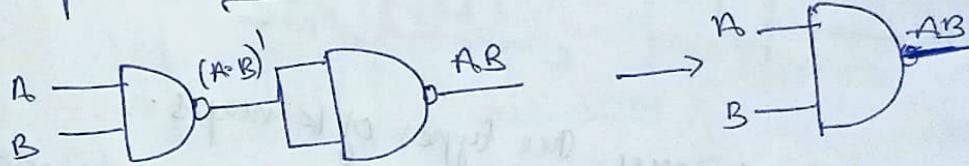
		ab	00	01	11	10
		c	0			
			0			
0						
1				1		

a) Prove that NAND gates are universal gates?

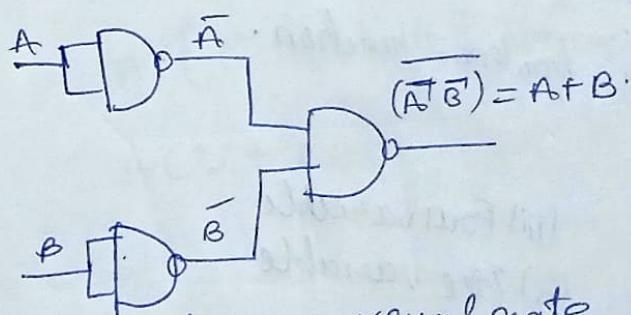
Sol (i) Implementing an Inverter using only NAND gates



(ii) Implementing AND using only NAND gates



(iii) Implementing OR using only NAND gates.

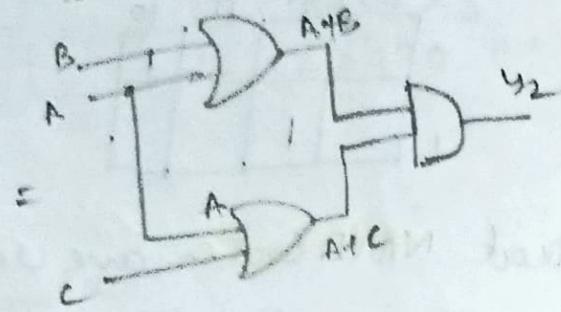
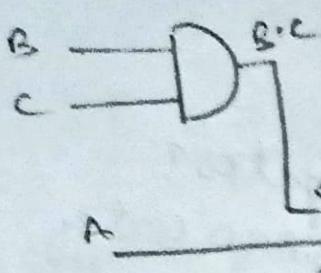


Thus, NAND gate is universal gate since it can implement ONE AND, OR, NOT functions.

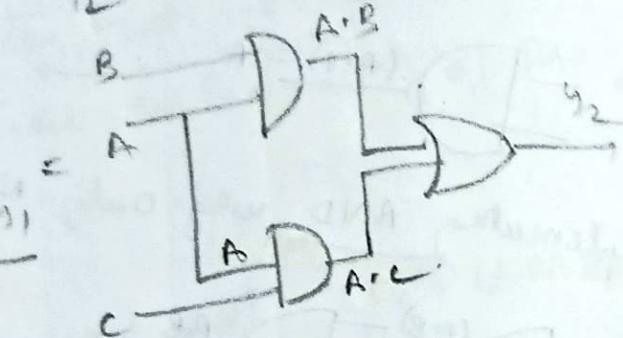
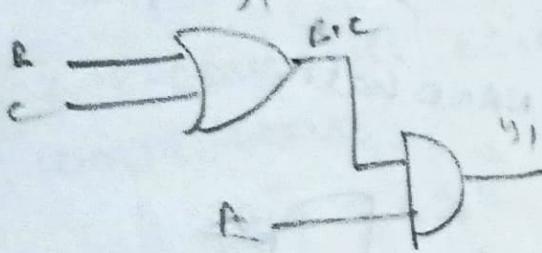
10) State & prove distributive laws & show their implementation using fundamental gates.

All proof \leftarrow back stroke

$$(i) A + B \cdot C = (A + B) \cdot (A + C)$$



$$(ii) A \cdot (B + C) = A \cdot B + A \cdot C$$



ii) What is Kmap? Discuss one types of K-maps.

All Kmap is a reduction method for a boolean function. we perform manipulations in the boolean algebra to minimize the given boolean function.

Types of Kmaps:

- (i) Two variable
- (ii) Three variable

(iii) Four variable

(iv) Five variable

Q12) What are don't cares?

Ans In DE, a "don't care" state is a condition in which the output of a logic circuit doesn't matter.

This can be used for minimizing the number of states/terms in a Boolean function.

Q13) Find the one complement of 1010?

Ans $\{1010\} = \text{complement of } \text{this}$
 $= 1010$
 $= \underline{0101}$

Q14) Determine minimal SOP of the function
 $(w, x, y, z) = \Sigma m(0, 4, 6, 7, 8, 9, 13, 15)$

Ans $\Sigma m(0, 4, 6, 7, 8, 9, 13, 15)$

		AB	CD	00	01	11	10
		CD	00	1	1		
		01	00			1	1
		11	00	1	1	1	1
		10	00	1	1	1	1
		01	01			1	1
		11	01	1	1	1	1
		10	01	1	1	1	1

$$\begin{aligned}f &= \bar{A}\bar{C}\bar{D} + C\bar{A}B + \bar{C}A\bar{B} + ABD \\&= A[\bar{C}\bar{B} + BD] + \bar{A}[\bar{D}\bar{C} + CB] \\&= A[\bar{C} \cdot D] + \bar{A}[\bar{D} \cdot B] \\&= A\bar{C}D + \bar{A}B\bar{D}\end{aligned}$$

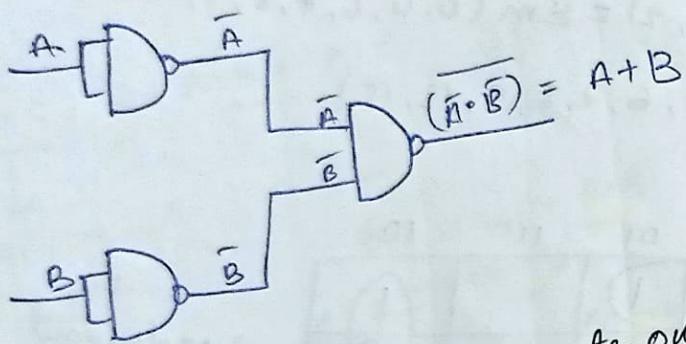
Q) Reduce the following expression using Boolean algebra:

$$f = xy + yz + \bar{x}z$$

Sol:

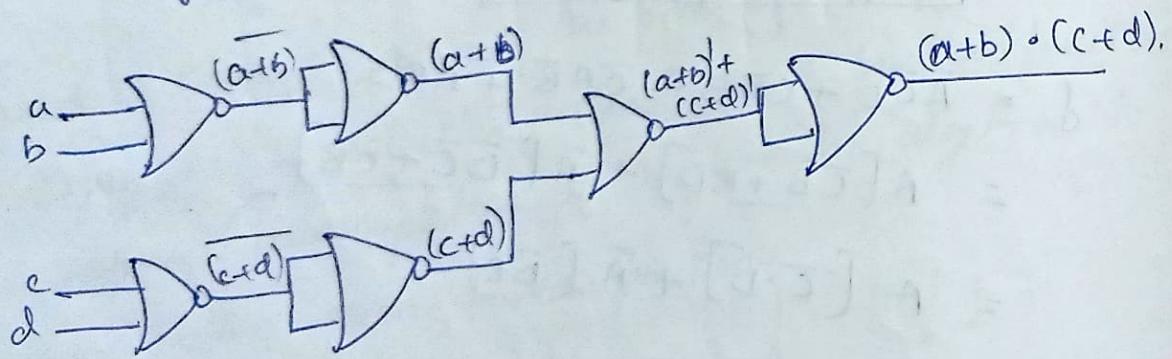
16) Realize an Exclusive OR gate using minimum number of
NAND gates only.

Sol:

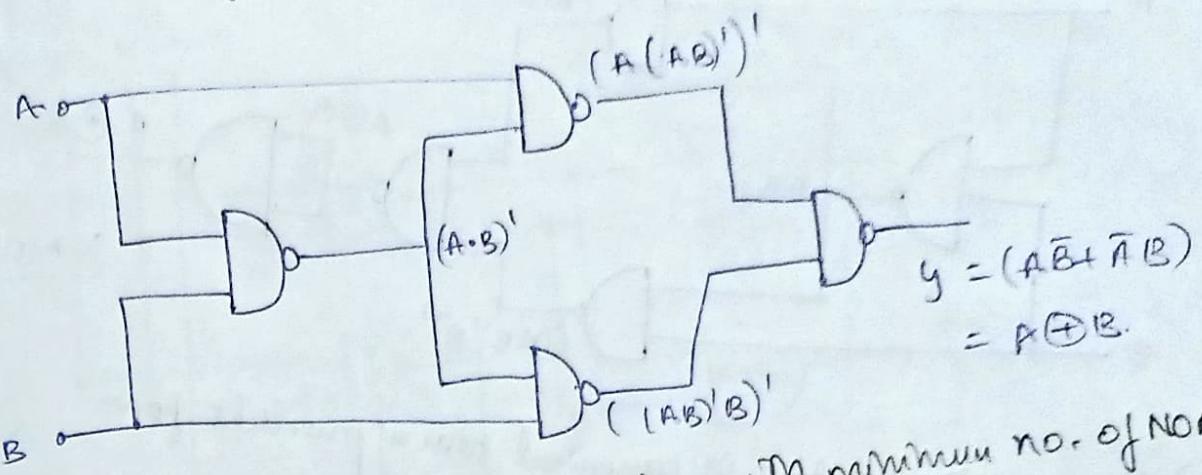


Q) Realize $f = (a+b) \cdot (c+d)$ using NOR gates only

Sol Cmns $f = (a+b) \cdot (c+d)$

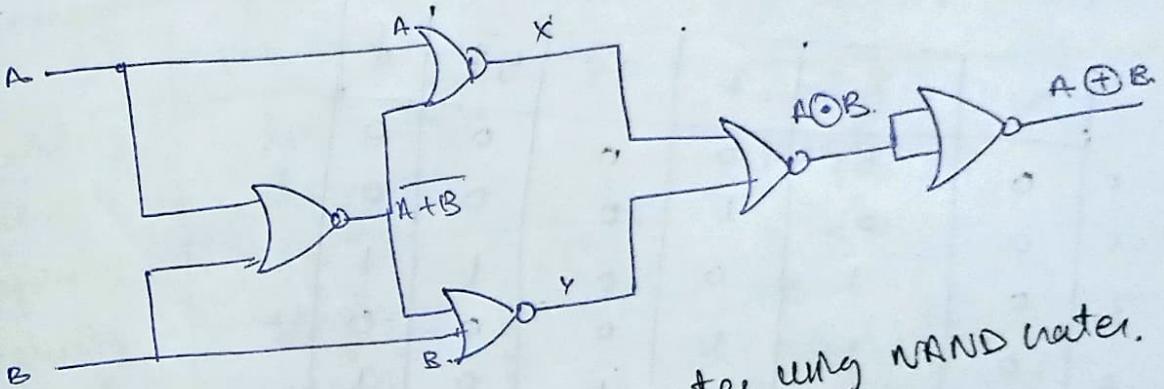


R) Realize two input XOR gate using NAND gates only/
 Ans XOR gate using four NAND gates.



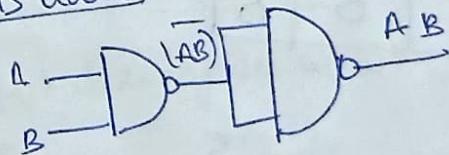
(a) Realize two input XNOR gate with minimum no. of NOR.

Ans

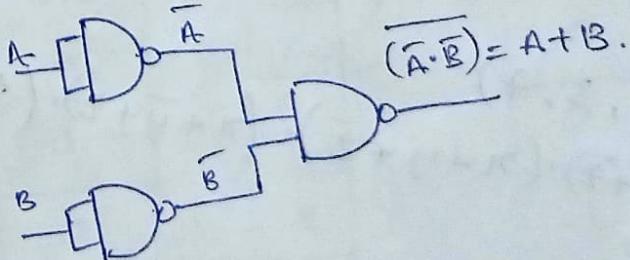


20) Draw the equivalent AND OR gate using NAND gates.

Ans AND gate

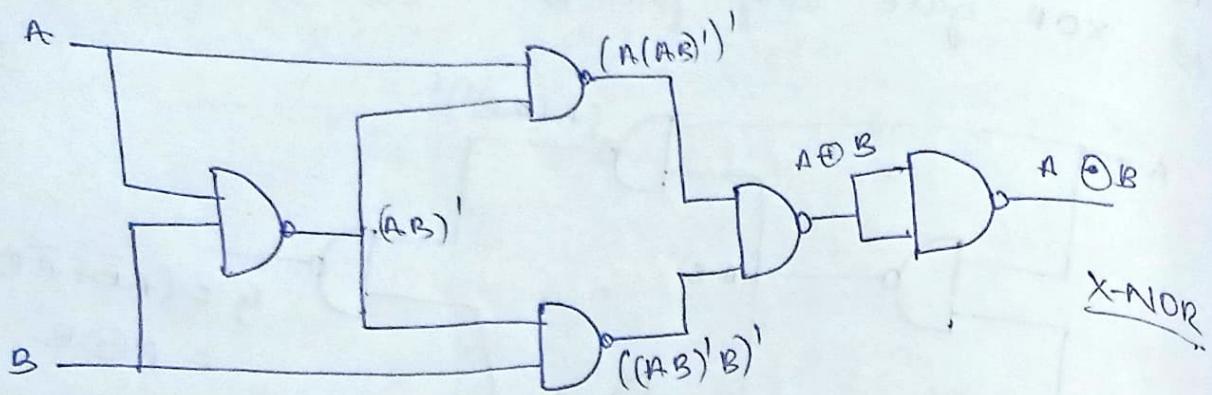


OR gate



Q1) Realize X-NOR gate using NAND gates

Ans



Q2) Express the function in canonical sum of products form

$$f(x, y, z) = xy + \cancel{xy} y\bar{z}$$

Sol Given $f(x, y, z) = xy + y\bar{z}$

x	y	z	xy	$y\bar{z}$	f
0	0	0	0	0	0
1	0	1	0	1	1
2	0	1	0	0	0
3	0	1	0	0	1
4	1	0	0	1	1
5	1	0	1	0	1
6	1	1	0	1	1
7	1	1	1	0	0

$$\Sigma m = (2, 4, 5, 6) \\ = \bar{x}y\bar{z} + xy\bar{z} + x\bar{y}z + xy\bar{z}$$

$$\Pi M = (0, 1, 3, 7)$$

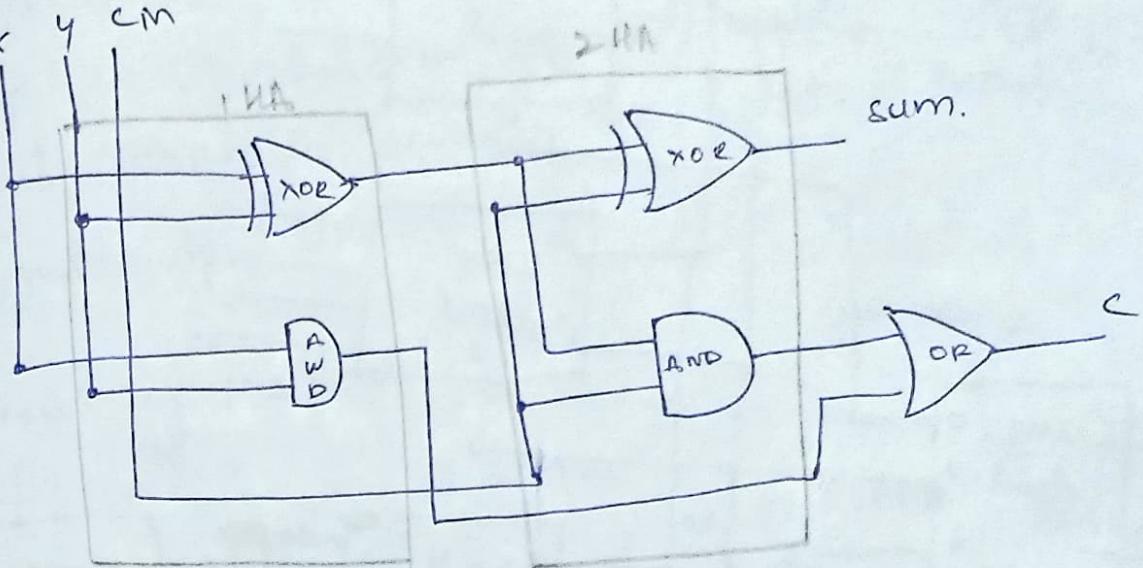
$$= (\bar{x} + \bar{y} + \bar{z}) \cdot (x + y + \bar{z}) \cdot (x + \bar{y} + \bar{z}) \cdot (\bar{x} + y + \bar{z})$$

Question paper wise

2022

(a) Draw circuit of full adder using half adder

sol)



(b) compare b/w CPLD & FPGAs?

sol)

CPLD

FPGAs

flexibility

low

high

price

low

high

capacity

low

high

security

high

low.

speed

high

high

Application

simple

complex.

power

less amount of power

high enough of power

(c) Excitation tables of SR & JK flipflops

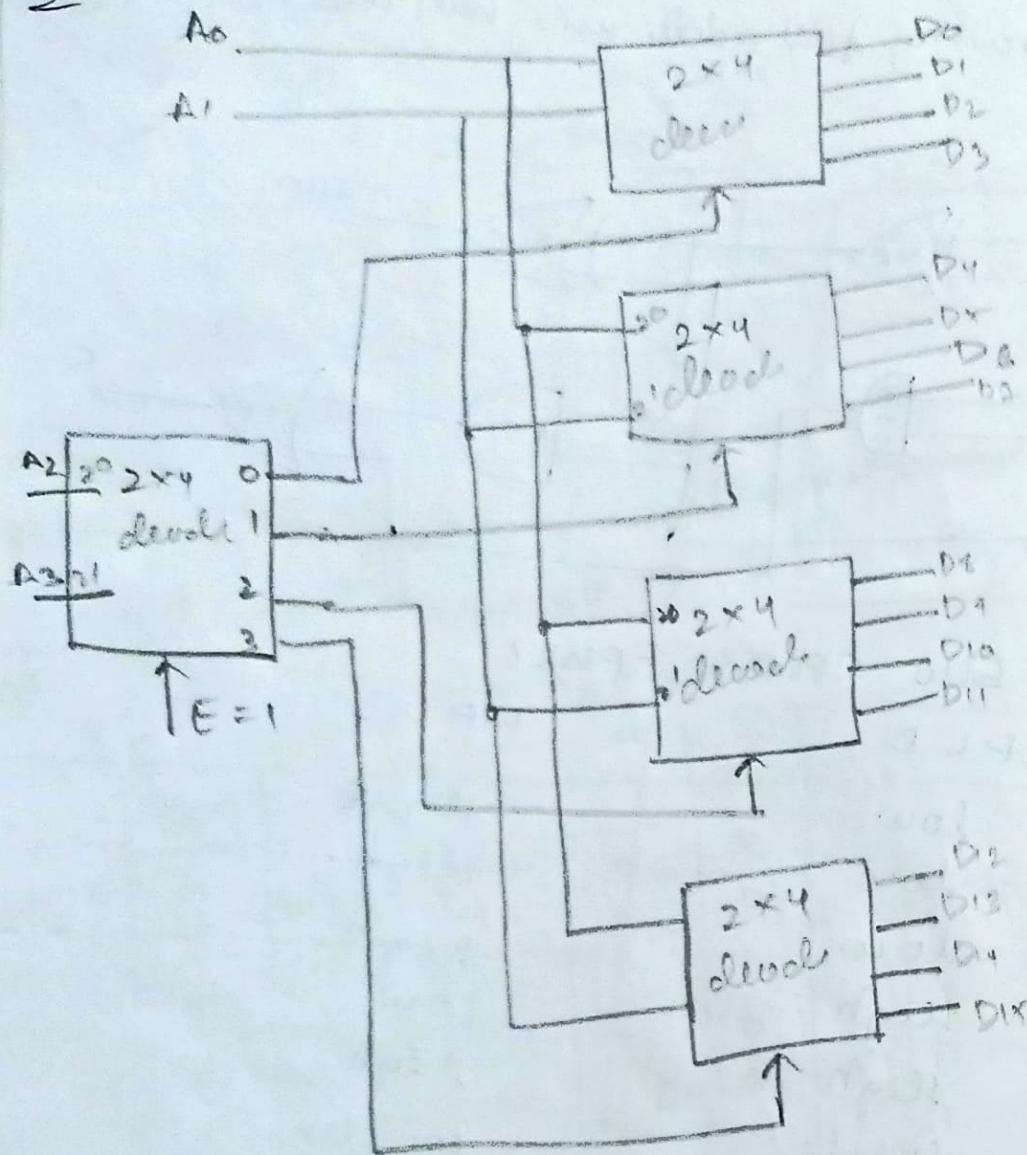
P.Stat	JK		Inputs	
	Q _n	Q _{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	X	1	1
1	1	X	0	0

SR

Q _n	Q _{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q1 Design 4×16 decoder using 2×4 decoder

A1



Q2 what is state Assignment?

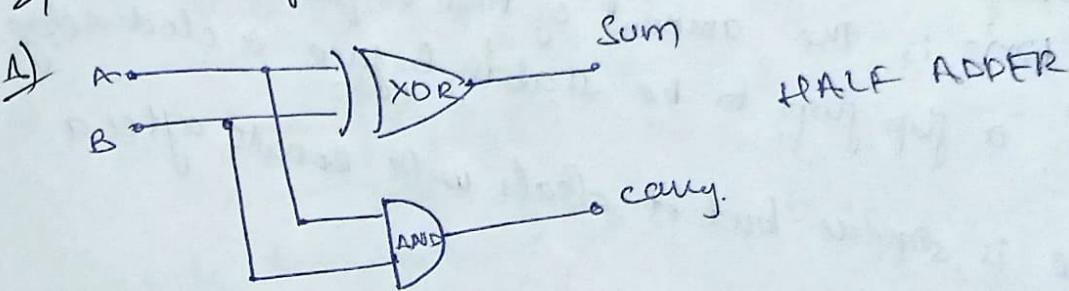
A2 To generate the derived next state for a particular present state and inputs it is necessary to have specific flip-flop inputs. These flip-flop inputs functions, it is necessary to represent states in the state diagram using binary values.

20/21

1) What is Multiplexer?

A) It is known as Data selector, is a device that selects between several analog or digital input signals and forwards the selected input to a single output line.

2) Circuit of Half adder?



3) Diff b/w PLA & PAL?

A) PLA

- 1) Programmable AND & OR.
- 2) AND array can be programmed to get derived minterms.
- 3) costlier than PAL
- 4) complex
- 5) Extremely flexible

PAL

- 1) programmable AND & fixed OR
- 2) AND array can be programmed to get desired minterms.
- 3) cost is low.
- 4) simple to use
- 5) moderate flexible.

4) What is State diagram?

A) It is a representation of the relationships b/w the present state, the input state, the next state, & the output state of a sequential circuit.

Q1 write VHDL code for half adder }

By module half-adder (A, B, S, C);

input A, B ;

output S, C ;

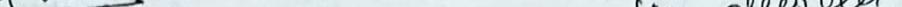
xor (S, A, B);

and (C, A, B);

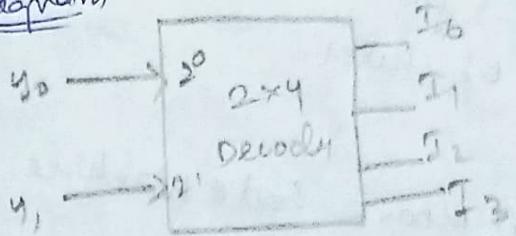
end module

- c) Define setup time & hold time of flip flop.
- i) Setup time is the amount of time required for the input to a flip flop to be stable before a clock edge. Hold time is similar but it deals with events after a clock edge occurs.
- 7) Explain about Mealy machine:
- i) When the output of the sequential circuit depends on the present state of the flip-flop as well as on the inputs then the sequential circuit is referred as a mealy machine.
- It requires less no. of states for implementing some function

2019 Dec.

2019 Dec 1) Draw & write T-T for 2×4 one class.
 Ans: 

a) Diagram

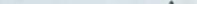


eventable:

100

y_0	y_1	I_3	I_2	I_1	I_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

2) write VHDL code for 3 input AND gate.

A) 

module Three-input-and (A, B, C, S);

input A, B, C;

output S;

and (c, a, b, c) ;

end module .

3) end module.
compare in contrast b/w latches & flip flops.

flip flops.

5) Latches

A) Latches
i) They are the building blocks of sequential circuits & are built from logic gates.

gather.

2) If checks its inputs & changes output correspondingly

consequently
3) a latch doesn't have clock
this is a level triggered clear

e) Ex: ~~dog~~ ~~example~~

~~Def~~ ~~new~~ SR catch. O catch

1) There are also building blocks of several events but are built from the latches.

2) It checks inputs & changes of
only at time determined by clock.

3) A flip flop has clock

4) It is a edge trapezoid.

5) Ex: D F.F
JKFF.

Q) What is FSM? Classify FSM's

A) The Finite State Machine is an abstract mathematical model of a sequential logic function. It has finite inputs, outputs and number of states.

FSM are of two types

(i) Mealy state machine (ii) Moore state machine.

c) Define ASM chart?

An ASM chart consists of an interconnection of four types of basic elements : State name , State box , decision box and conditional outputs box.

d) Excitation Table for T - flipflop

<u>Qn</u>	<u>Qn+1</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

2) Diff between combinational & sequential circuits.

A) COMBINATIONAL

i) Output depends only on present input

2) Easier to design

3) Speed of operation is high

4) Memory unit is not required

Example: Parallel adder.

SEQUENTIAL

1) Output depends on one previous input & past output also.

2) Harder to design

3) Speed of operation is low.

4) Memory unit is required to store old outputs.

Example: serial adder.

Q) Define ASM (Algorithmic State Machine).

A) The state diagrams or state tables described earlier are convenient for describing the behaviour of FSM. But only a few inputs & outputs.

For larger machines, we often use a different form of representation, known as Algorithmic State Machine.

2018 - Dec

i) Differ b/w synchronous & Asynchronous counters.

A) Asynchronous counter
(Ripple counter)

synchronous
counters.

i) In this type of counter FF are connected in such way that output of first FF drives the clock for the next FF.

ii) All the FF are not clocked simultaneously.

iii) Logic circuit is very simple

i) In this type of counter no. connection b/w o/p of 1st FF & clock input of the next FF.

ii) All the FF are clocked simultaneously.

iii) complex logic circuit

④

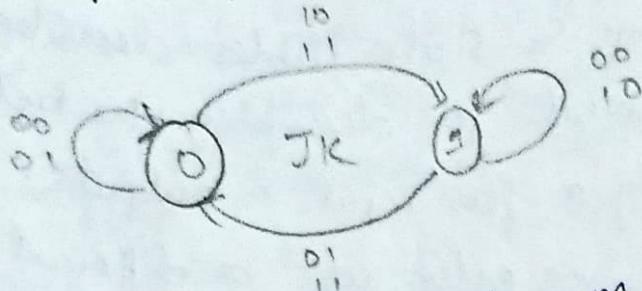
2) Applications of Multiplexer & De-multiplexer.

A) Multiplexers are commonly used in
→ communication systems, telephone networks, computer memories.

De-multiplexers are used in communication systems,
reconstruction of parallel data, ALU etc.

3) State diagram for JK FF?

A)



JK Flip flop state diagram

a) significance of priority encoder?

a) It compresses multiple binary inputs into a smaller number of outputs.

In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

→ characteristics of flip flops?

a) (i) supply voltage

(iv) low level output current

(ii) operating current

(v) high level output current

(iii) power dissipation

(vi) max clocking frequency.

b) Distinguish b/w decoders & demultiplexers.

A) Decoder

1) A decoder has input lines & a menu of 2^n output lines.

2) used to detect bits, encoding of data

3) Decoder has n selection lines

4) used in networking applications

5) Decoder's inverse is encoder

Demultiplexer

1) A demux has single input, selection lines for max 2^n outputs.

2) used in switching, data distribution.

3) It contains select lines.

4) used in communication system.

5) Demux is inverse of multiplexer.

7) List out applications of shift registers.

- A) (i) Sequence generator
(ii) Parallel to serial converter
(iii) Serial to parallel converter

8) Distinguish between a Decoder & Encoder?

Encoder

Decoder

a)

1) Input: Original message signal

2) OP: Coded binary output

3) IP (out): 2^n

4) OP (in): n

5) Operation: Simple

6) OR gate

1) Coded binary input

2) Original message

3) n

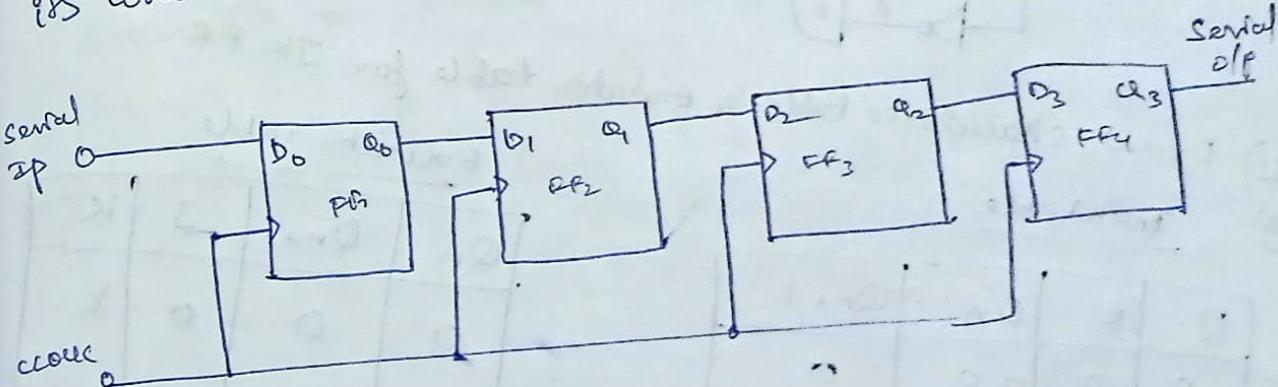
4) 2^n

5) Complex

6) AND Gate along with not gate

9) What is shift registers? Explain with diagram

A) A register that is designed to allow the bits of its contents to be moved to left or right.



10) Distinguish b/w Mealy & Moore model:

A) Moore Model

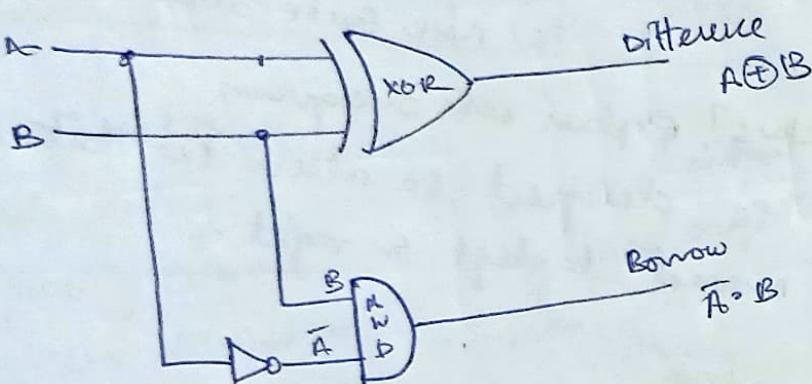
Mealy Model

- 1) Its output is a function of present state only
- 2) Input changes does not affect the output
- 3) It requires more number of states for implementing same function

- 1) Its output is a function of present state as well as previous input
- 2) Input changes may affect the output of the circuit
- 3) It requires less number of states for implementing same function

11) Realize half subtractor?

A)



(2) Draw characteristic table: Excitation table for JK FR.

A) Truth table:

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation table

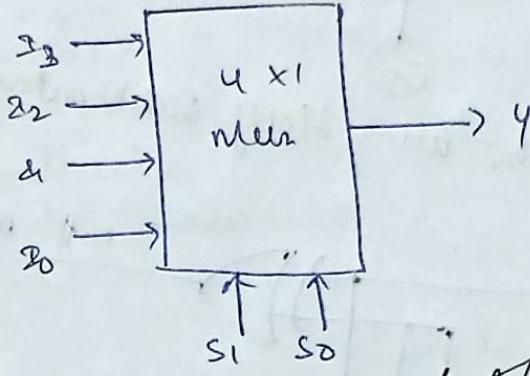
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(B) Define symmetric networks?

(i) A symmetric network has a single route for incoming & outgoing network traffic.

(ii) Define Multiplexer with diagram. (data selector)

Ans: A device that selects b/w several digital signal (sp) & forwards the selected input to a single output line.



(C) State & prove idempotent law.

A) Boolean logic has idempotent w.r.t. both AND & OR gates.

An AND or OR gate with two inputs 'A' will also have an output 'A'

Proof: (i) $A \cdot A = A$

Proof: If $A = 0$; then $0 \cdot 0 = 0 = A$
If $A = 1$; then $1 \cdot 1 = 1 = A$

(ii) $A + A = A$

Proof: If $A = 0$; then $0 + 0 = 0 = A$
If $A = 1$; then $1 + 1 = 1 = A$

Q8) Realize the 4×1 Mem using 2×1 Mem.

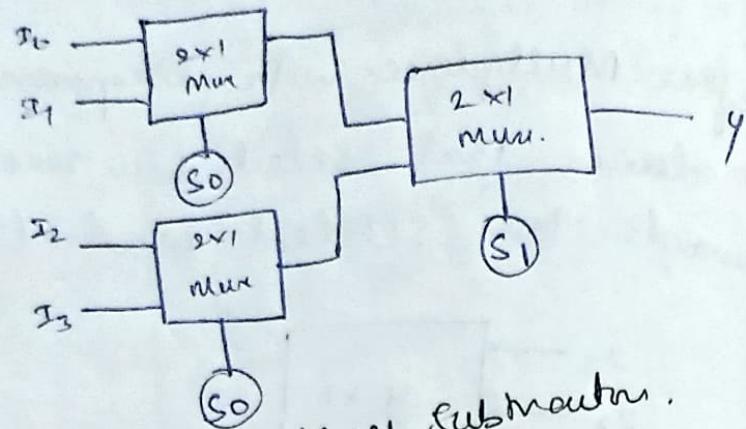
A)

$$\frac{4}{2} = 2$$

$$\frac{2}{2} = 1$$

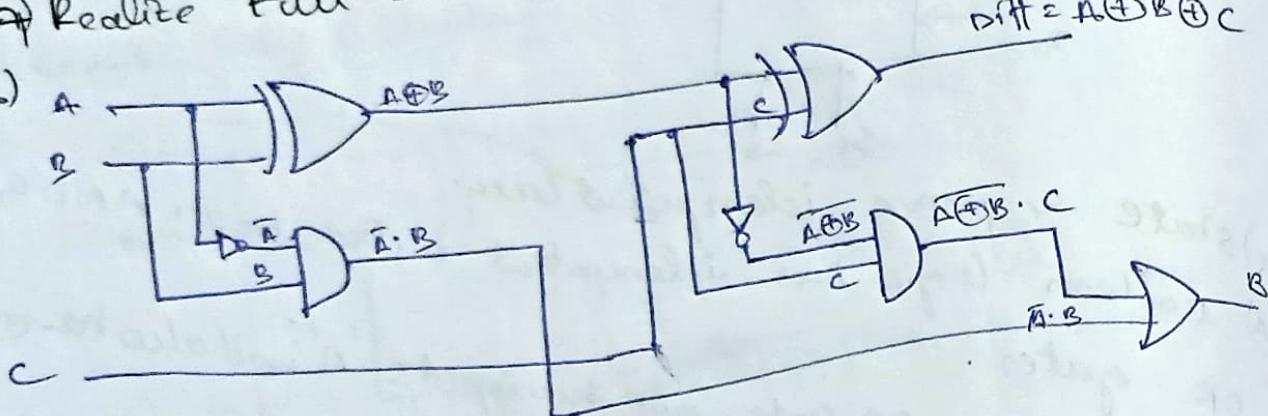
No of 2×1 Mem req = 2 + 1

S_1	S_0	4
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



17) Realize Full Subtractor using Half Subtractor.

A)



Q18) What are registers & counters.

A) Registers: Is a set of FF with combinational logic to implement state transitions that allows information to be stored & retrieved from them.

Counters: Is a set of FF connected in a suitable manner to count the sequence of the input pulses arrived at its clock input.

(Q1) What are code converters?
A) A code converter is a circuit, which accepts one input information in one binary code, converts it and produces an output into binary code. i.e. which makes the two system compatible even though each uses a different binary code.

(Q2) Applications of FCSPS?

- A) (i) Aerospace & defense
- (ii) Automotive
- (iii) Broadcast
- (iv) wireless communications
- (v) wired communications.

(Q2) Define the terms characteristic equation, characteristic table or excitation table.

A) Characteristic Equation:

It defines the next state of the FF as a function of the FF inputs in the current state.

Characteristic Table:

It defines the next state of the FF in terms of FF inputs in current state.

Excitation Tables:

If defines the FF input variables values as function of the current state and next state.