Code No: 15037/AICTE

FACULTY OF ENGINEERING

BE III – Semester (AICTE) (Main & Backlog) Examination, July 2021

Subject: Digital Electronics

Time: 2 Hours **Max .Marks: 70**

Note: Missing data, if any, may be suitably assumed

PART – A

Answer any five questions. **(5x2=10 Marks)**

1 Convert the binary number 11011101 to gray code.
2 Prove that NAND gates are universal gates.
3 What is Multiplexer?
4 Draw the circuit of half adder.
5 List the comparison between a PLA and PAL.
6 Write the VHDL code for an half adder?
7 Give the Excitation table for J-K Flip-flop.
8 Define set up and hold time of flip flop.
9 Explain about Mealy state machine.
10 What is a state diagram?

PART – B

Answer any four questions. **(4x15= 60 Marks)**

11 (a) What is the basic law of Boolean algebra. Explain any two
(b) Simplify the Boolean function F using the don't care conditions d, in
(i) Sum of products and (ii) Product of sums. $F = A\bar{B}\bar{D} + \bar{A}CD + \bar{A}\bar{B}C$

12 (a) Realize the function f(A,B,C,D)=Σ(1,4,6,10,14)+d(0,8,11,15) using:
(i) 16:1 MUX (ii) 8:1 MUX
(b) What is full adder? Explain full adder using two half adder circuits using basic Gates.

13 (a) Explain about decoder and write a VHDL of simple decoder.
(b) Explain the structure of CPLDs.

14 (a) Draw the circuit of a JK master slave flip-flop and explain its operation.
(b) Explain about decoder.

15 (a) Reduce the number of states in the following state table and tabulate the reduced state Table.

PS	NS, O/P	
	X=0	X=1
a	f, 0	b,0
b	d,0	c,0
c	f, 0	e,0
d	g,1	a,0
e	d,0	c,0
f	f,1	b,0
g	g,0	h,1
h	g,1	a,1

(b) What are the limitations of FSM?

16 Design a circuit to convert Excess-3 code to BCD code using basic Logic gates.

17 (a) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal.
(b) Minimize the following expression using K-map and realize using NOR gate $f = \pi M(0,4,6,7,8,12,13,14,15)$.