| *Course Code* | *Course Title* | *Core/Elective* |
|---|---|---|
| ***ES216EC*** | ***Digital Electronics*** | ***Core*** |

## Unit - 3

1. Design 3 bit Binary to gray code converter using PLA
2. Differentiate between PLA , PAL and PROM
3. Implement Full adder circuit using PAL.
4. Explain Architectures of CPLD and FPGA
5. Define concept of LUT with one example.
6. Implement the following function using PLA and PAL

   $F1(a,b,c,d)= \sum m(0,2,3,6,9,12)$

   $F2(a,b,c,d)= \sum m(0,1,7,9,10)$

   $F3(a,b,c,d)= \sum m(2,3,5,8,11)$
7. Write Verilog Code for Basic Logic gates
8. Write Verilog Code for Adders and Decoders

## Unit - 4

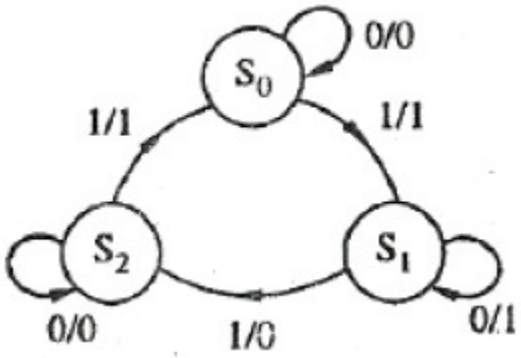
1. Differentiate between Flip flop and Latch
2. Draw structure of Gated SR and D latch.
3. Explain the operation of Master slave Flip flop with timing wave form.
4. Draw neat diagrams, Excitation table and Characteristics equations of SR, JK, D and T flip flop.
5. Explain shift registers with example (3 bit)
6. Explain Synchronous and Asynchronous Counters with example
7. Write Verilog code for T and D flip flop
8. Write Verilog Code for JK Flip flop.

## Unit - 5

1. Differentiate between combinational and sequential circuits.
2. Differentiate between Mealy and Moore FSM models.
3. Draw Mealy and Moore FSM models with example state diagram and state table.
4. List out basic design steps of Sequential circuits.
5. Differentiate between synchronous and A synchronous sequential circuits .
6. Implement Sequential circuit using a) D FF b) T FF and C) JK FF

| | 0 | 1 |
|---|---|---|
| A | A/0 | B/0 |
| B | A/0 | C/1 |
| C | B/0 | D/0 |
| D | C/1 | D/0 |

7. Describe Component of ASM and Explain Advantages of ASM
8. Draw ASM chart for the given FSM

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