Q1) List the different types of programmable logic devices.

Answer :

Different types of programmable logic devices are,

(1) Simple Programmable Logic Devices (SPLD).

- (i) Programmable ROM (PROM).
- (ii) Programmable Logic Array (PLA).
- (iii) Programmable Array Logic (PAL).
- (iv) Generic Array Logic (GAL).

(2) Complex Programmable Logic Devices (CPLD).

(3) Field Programmable Gate Array (FPGA).

Q3) Why was PAL developed?

Answer :

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional and fusible links that result from using two programmable arrays and more circuit complexity.

Q4) Write the advantages of PLA.

Answer :

Following are the advantages of PLA,

(1) PLA can have large number of inputs N and output M, permitting implementation of optimized func that are impractical for a ROM.

(2) Any product can be shared by output functions (sums).

(3) Some PLAs have outputs that can be complemented, to give F expressions in terms of POS.

Q5) What are the applications of PLA?

Answer :

Following are the applications of PLA,

(1) PLA is used to provide control over data path.

(2) PLA is used as a counter and decoders.

(3) PLA is used as a bus interface in programmed I/O.

Q6) What are the difference between PLA and PAL.

Answer :

Table Difference Between PLA and PAL

S.No	PLA	PAL
(1)	Programmable AND and programmable OR array.	Programmable AND and fixed OR array.
(2)	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
(3)	Any Boolean functions in SOP form can be implemented.	Any Boolean functions is SOP form can be implemented.
(4)	Costlier than PAL.	Cost is low.
(5)	Complex than PAL.	Simple to use.

Q8) Write the applications of FPGAs.

Answer :

Following are the applications of FPGAS,

(1) Aerospace and defense.

(2) Automotive.

(3) Broadcast.

(4) Full featured consumer applications.

(5) Fulfilling industrial/scientifc/medical needs.

(6) Wireless communications.

(7) Wired communications.

Q9) What are the applications of PLA?

Answer :

The PLAs are used to replace ROMs in many applications. They are used for implementing combinational logic functions and this results in compact circuitry and high switching speed.

The following are the steps used for implementing the combinational logic functions,

(1) Prepare the truth table.

(2) Write the boolean relations in SOP form.

(3) Simplify the equations to obtain minimum SOP form.

(4) Determine the input connections of AND matrix to generate the required product terms.

(5) Determine the input connections of OR matrix to generate the required sum-of-product terms.

(6) Determine the connections of Ex-OR matrix required for invert/non-invert matrix to set the active logic level of the outputs.

(7) Program the PLA.

Q1) **Draw the characteristic table and excitation table of a JK flip-flop.**

Answer :

[Nov./Dec. - 2016], [Nov./Dec. - 2012]

Present State (PS)			Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a) Truth Table of J-K and Flip-Flop

Present State	Next State	Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) Excitation Table

Q2) **Distinguish between a latch and flip-flop.**

[July - 2016], [Jan. - 2012]

Answer :

S.No.	Latches	Flip-flops
(1)	Latches are building blocks of sequential circuits and these can be built from logic gates.	Flip-flops are also building blocks of sequential circuits. But, these can be built from the latches.
(2)	Latch continuously checks its inputs and changes its output correspondingly.	Flip-flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal.

(3)	The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on.	Flip-flop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip-flop are used as a register.
(4)	It is based on the enable function input.	It works on the basis of clock pulses.
(5)	It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a positive or negative clock pulse.

Q3) Distinguish between synchronous and asynchronous sequential circuit. [July - 2

Answer :

S.No.	Synchronous Sequential Circuits	Asynchronous Sequential Circuits
(1)	In synchronous circuits, memory elements are clocked flip-flops.	In asynchronous circuits, memory elements are either unclocked flip-flops or time delay elements.
(2)	In synchronous circuits, the change in input signals can affect memory element upon activation of clock signal.	In asynchronous circuits change in input signals can affect memory element at any instant of time.
(3)	The maximum operating speed of clock depends on time delays involved.	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits.
(4)	Easier to design.	More difficult to design.

Q4) Define the terms characteristic equation, characteristic table and excitation table. [June/July - 20

Answer :

Characteristic Equation : It defines the next state of the flip-flop as a boolean function of the flip-flop inp and the current state.

Characteristic Table : It defines the next state of the flip-flop in terms of flip-flop inputs and current sta

Excitation Table : It defines the flip-flop input variable values as function of the current state and ne state.

Q5) Write the excitation and characteristic tables of SR flip-flop. [July - 20

Answer :

Flip-Flop Inputs		Present Output	Next Output
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

(a) Characteristic Table of SR Flip-flop

Present State		Next State	Inputs
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(b) Excitation Table

Q6) Draw the JK-flip-flop and write the characteristic table and excitation table.

[Dec. - 2013]

Answer :

The JK-flip-flop is shown in below figure.

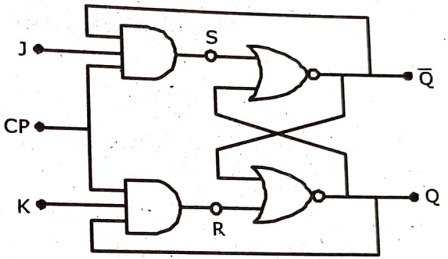

Figure Clock JK Flip-Flop

The characteristic table and excitation table.

38) **Difference between edge-triggered and level triggered?**

Answer :

S.No.	Edge Triggering	Pulse Triggering
(1)	Edge triggered storage element is called flip-flop.	Pulse triggered storage element is called latch.
(2)	Edge triggering occurs for positive (or) negative pulse.	Pulse trigger occurs for whole pulse.
(3)	The input signal is sampled at the rising edge (or) falling edge of the clock signal.	The input signal is sampled when the clock signal is either high (or) low.
(4)	It is not sensitive to glitches.	It is sensitive to glitches.

Q1) List the comparison between Moore and Mealy model.

Answer :

S.No.	Moore Model	Mealy Model
(1)	Its output a is function of present state only.	Its output is a function of present state as well as past input.
(2)	Input changes does not affect the output.	Input changes may affect the output of the circuit.
(3)	Moore model requires more number of states for implementing same function.	It requires less number of states for implementing same function.

Q3) **What is state assignment?**

Answer :

To generate the desired next state for a particular present state and inputs, it is necessary to have specific flip-flop inputs. These flip-flop inputs functions, it is necessary to represent states in the state diagram using binary values instead of alphabets. This procedure is known as "state assignment".

to the binary ...

Q7) Write the advantages of FSM.

Answer :

The advantages of Finite State Machine include the following,

(1) Finite state machines are flexible.

(2) Easy to move from a significant abstract to a code execution.

(3) Low processor overhead.

(4) Easy determination of reach ability of a state.