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Code No.D-2370 /N/AICTE

FACULTY OF ENGINEERING

BE (CSE/IT) III – Semester (AICTE) (Main) (New) Examination, March / April 2022

Subject: Digital Electronics

Time: 3 Hours **Max. Marks: 70**

Note: (i) First question is compulsory and answer any four questions from the remaining six questions. Each Questions carries 14 Marks.
(ii) Answer to each question must be written at one place only and in the same order as they occur in the question paper.
(iii) Missing data, if any, may be suitably assumed.

1. (a) State and prove DeMorgan's theorem.
   (b) Represent the Boolean expression in k-map b'+ac'+a'cd.
   (c) Draw a circuit of full adder using half adders.
   (d) Write the comparision between CPLD and FPGA.
   (e) Design 4X16 decoder using 2X4 decoders.
   (f) Write the excitation table of RS and JK FF.
   (g) What is state assignment?

2 (a) Simplify the Boolean function to a minimum no. of literals
   i) xy+x'z+yz ii) ABC+A'B+ABC'
   (b) Simplify the function using k-map
   F(V,W,X,Y,Z)= ∑m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)
   Realize the circuit using NAND gates.

3 (a) Design a BCD –to-Decimal code converter with circuit diagram.
   (b) Define magnitude comparator. Draw the block diagram and truth table of a one-bit magnitude comparator. Show the implementation using logic gates.

4 (a) With a neat diagram explain FPGA architecture.
   (b) Realize the given logic functions using PAL
   $F1=x_1x_2x_3'+x_1'x_2x_3$
   $F2=x_1'x_2'+x_1x_2x_3$

5 (a) Construct a 4-bit shift register with parallel load facility.
   (b) Show that a SR FF can be converted to JK FF.

6 (a) Explain the steps required to design synchronous sequential circuits.
   (b) Implement the function F(A,B,C,D)= ∑m(1,3,4,11,12,13,14,15) using
   i) 8:1 MUX and ii)16:1 MUX.

7 (a) Simplify using Quine Mc Cluskey tabular method
   F(A,B,C,D)=∑m(0,2,4,6,7,9)+∑d(10,11)
   (b) Write the Verilog code for 3X8 decoders.

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