Course Code	*Course Title*	*Core/Elective*
ES216EC	***Digital Electronics***	***Core***

Unit-1

1. Explain design process in digital system with flow chart.
2. What are the commonly used digital hardware components in digital electronics?
3. Prepare a table showing various laws of Boolean algebra.
4. State and prove Demorgan's theorem
5. How is logic circuit designed?
6. State whether the following are true or false, use theorem in Boolean algebra
   a) A+B = B+A
   b) A.A=1
   c) A+A = A'
   d) A+AB = A
   e) A'+AB' =A'+B
   f) (A+B+C)' = A.B.C

7. What is the meant by min term and max term in digital logic.
8. Use Karnaugh map to simplify Y= ABCD+AB'CD+ABCD'+ABC'D+ABC'D' and draw logic circuit.
9. Use tabular method to simplify the following function
   F(A,B,C,D) = A'B'C'D'+AB'C'D'+A'BC+A'CD'+A'C'D'
10. Simplify following Boolean function using Q-M method
    F(a,b,c,d) = ∑M(2,3,5,7,9,11,12,13,14,15)

Unit - 2

1. Design Half Adder using only NAND gate.
2. Design Full adder using half adder.
3. Design Decoder and Encoder circuits.
4. Implement 4: 1 Multiplexer using 2:1 Multiplexer
5. Design 2 bit comparator circuits.
6. Design BCD to 7 segment converter.
7. Describe Number systems in Digital system , Explain with examples
8. Explain Binary addition and Subtraction of signed and unsigned numbers.

Unit - 3

1. Design 3 bit Binary to gray code converter using PLA
2. Differentiate between PLA , PAL and PROM
3. Implement Full adder circuit using PAL.
4. Explain Architectures of CPLD and FPGA
5. Define concept of LUT with one example.
6. Implement the following function using PLA and PAL

   $F1(a,b,c,d)= \sum m(0,2,3,6,9,12)$

   $F2(a,b,c,d)= \sum m(0,1, 7,9,10)$

   $F3(a,b,c,d)= \sum m(2,3,5,8,11)$
7. Write Verilog Code for Basic Logic gates
8. Write Verilog Code for Adders and Decoders

Unit - 4

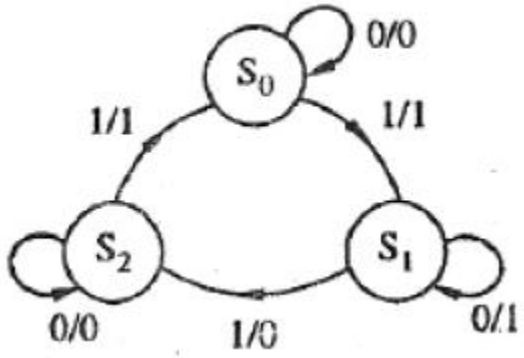
1. Differentiate between Flip flop and Latch
2. Draw structure of Gated SR and D latch.
3. Explain the operation of Master slave Flip flop with timing wave form.
4. Draw neat diagrams, Excitation table and Characteristics equations of SR, JK, D and T flip flop.
5. Explain shift registers with example (3 bit)
6. Explain Synchronous and Asynchronous Counters with example
7. Write Verilog code for T and D flip flop
8. Write Verilog Code for JK Flip flop.

Unit - 5

1. Differentiate between combinational and sequential circuits.
2. Differentiate between Mealy and Moore FSM models.
3. Draw Mealy and Moore FSM models with example state diagram and state table.
4. List out basic design steps of Sequential circuits.
5. Differentiate between synchronous and A synchronous sequential circuits .
6. Implement Sequential circuit using a) D FF b) T FF and C) JK FF

	0	1
A	A/0	B/0
B	A/0	C/1
C	B/0	D/0
D	C/1	D/0

7. Describe Component of ASM and Explain Advantages of ASM
8. Draw ASM chart for the given FSM



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