Digital Design and Computer Organization Laboratory

UE19CS206

3rd Semester, Academic Year 2020-21

Date:15—09—2020

Name:Suhan.B.Revankar	SRN: PES2UG19CS412	Section G

Week #2

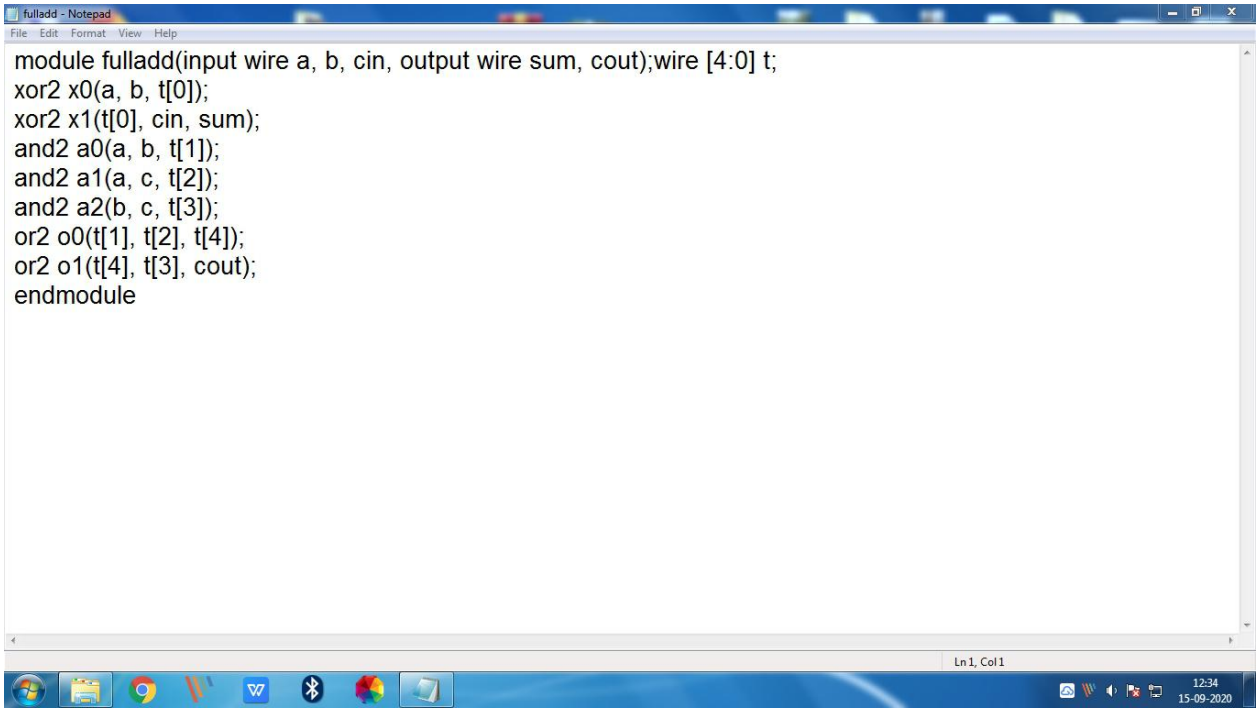
Program #1

Title : FULL ADDER USING BASIC GATES

Aim :

DESIGN A FULL ADDER USING BASIC GATES AND VERIFY THE FULL ADDER TRUTH TABLE

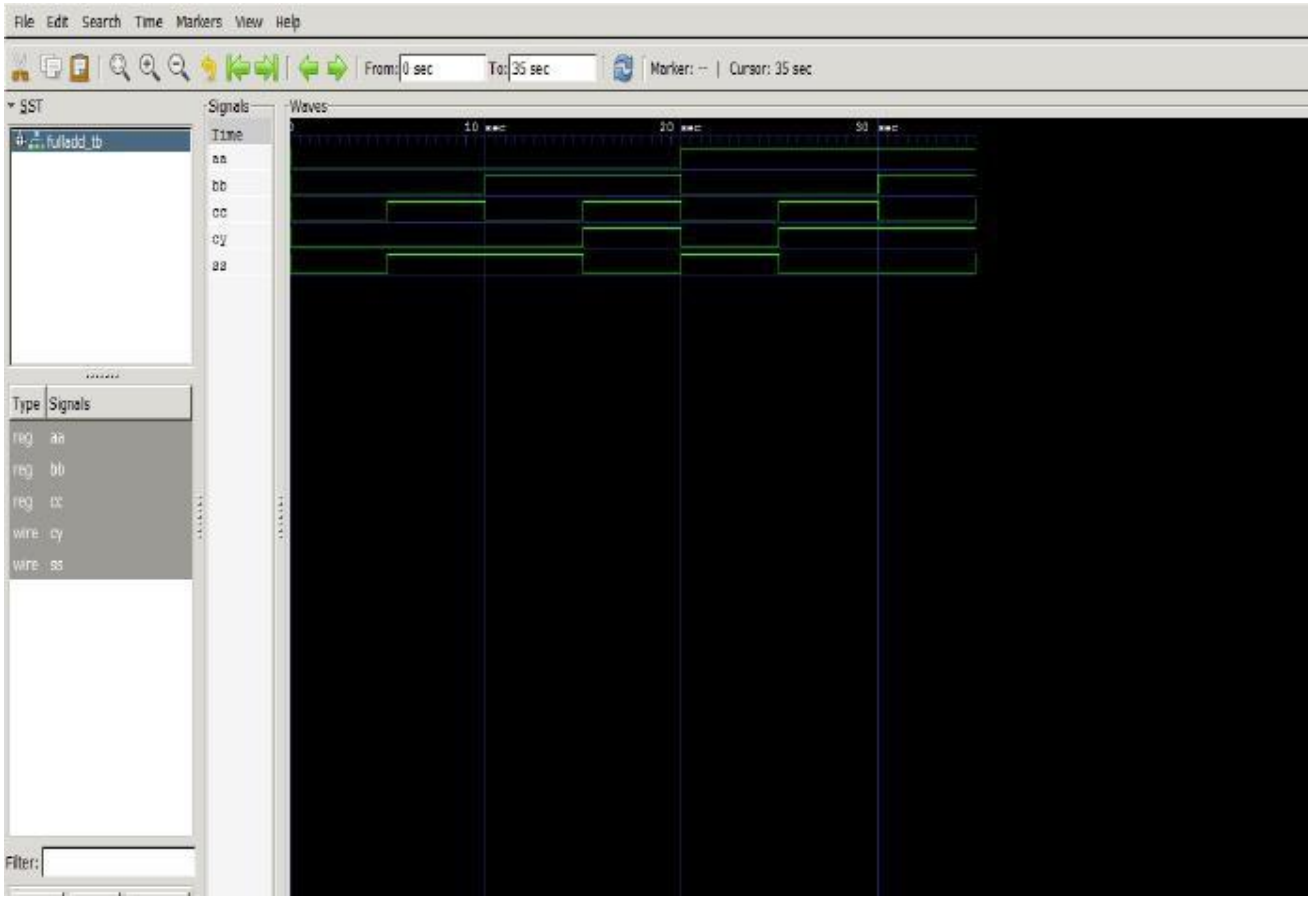
1: Screen Shot of the source code



2: Screen Shot of the VVP command output

```
D:\DDCO LAB PROGRAMS>iverilog -o testfa basic.v fulladd.v fulladd_tb.v

D:\DDCO LAB PROGRAMS>vvp testfa
VCD info: dumpfile fulladd_test.vcd opened for output.
                    0a=0, b=0, c=0,sum=0,carry=0
                    5a=0, b=0, c=1,sum=1,carry=0
                   10a=0, b=1, c=0,sum=1,carry=0
                   15a=0, b=1, c=1,sum=0,carry=1
                   20a=1, b=0, c=0,sum=1,carry=0
                   25a=1, b=0, c=1,sum=0,carry=1
                   30a=1, b=1, c=0,sum=0,carry=1
                   35a=1, b=1, c=1,sum=1,carry=1

D:\DDCO LAB PROGRAMS>gtkwave fulladd_test.vcd

GTKWave Analyzer v3.3.71 (w)1999-2016 BSI

[0] start time.
[35] end time.
WM Destroy
```

3: Screen shot of the GTKWave form



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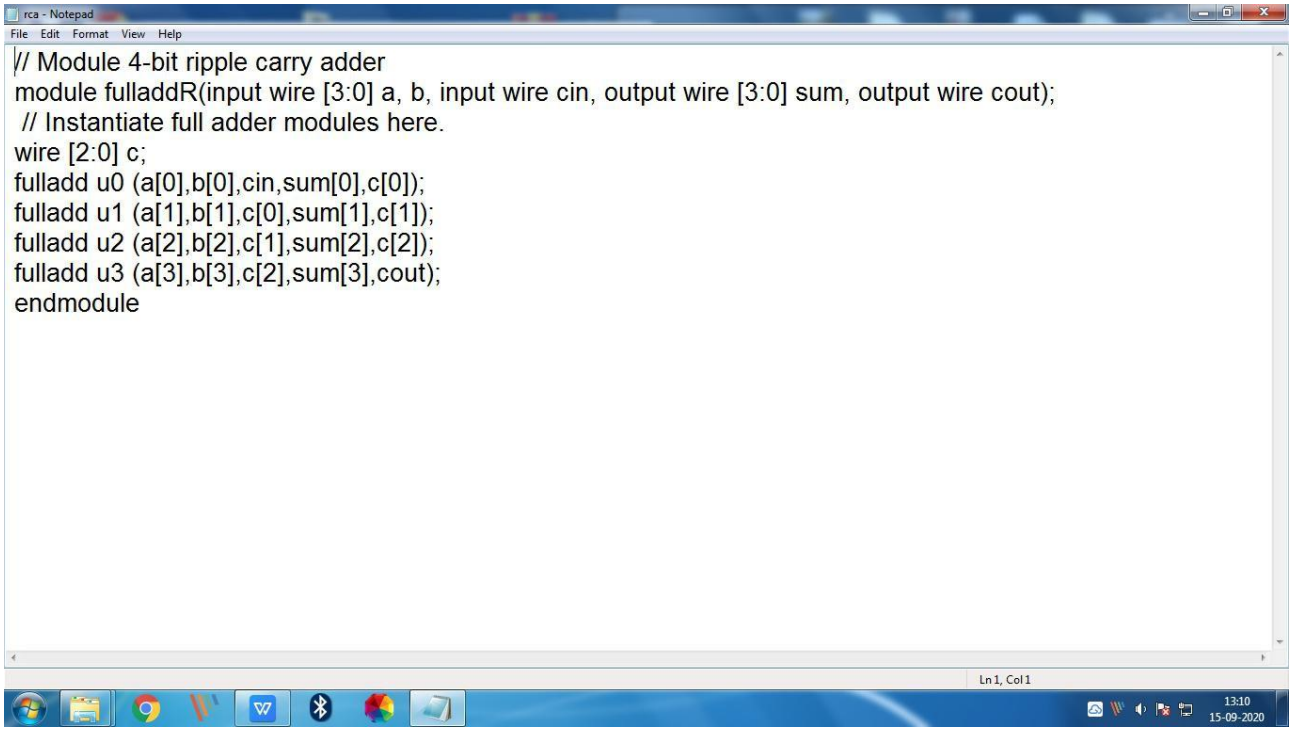
Program #2

Title :
4 BIT RIPPLE CARRY ADDER

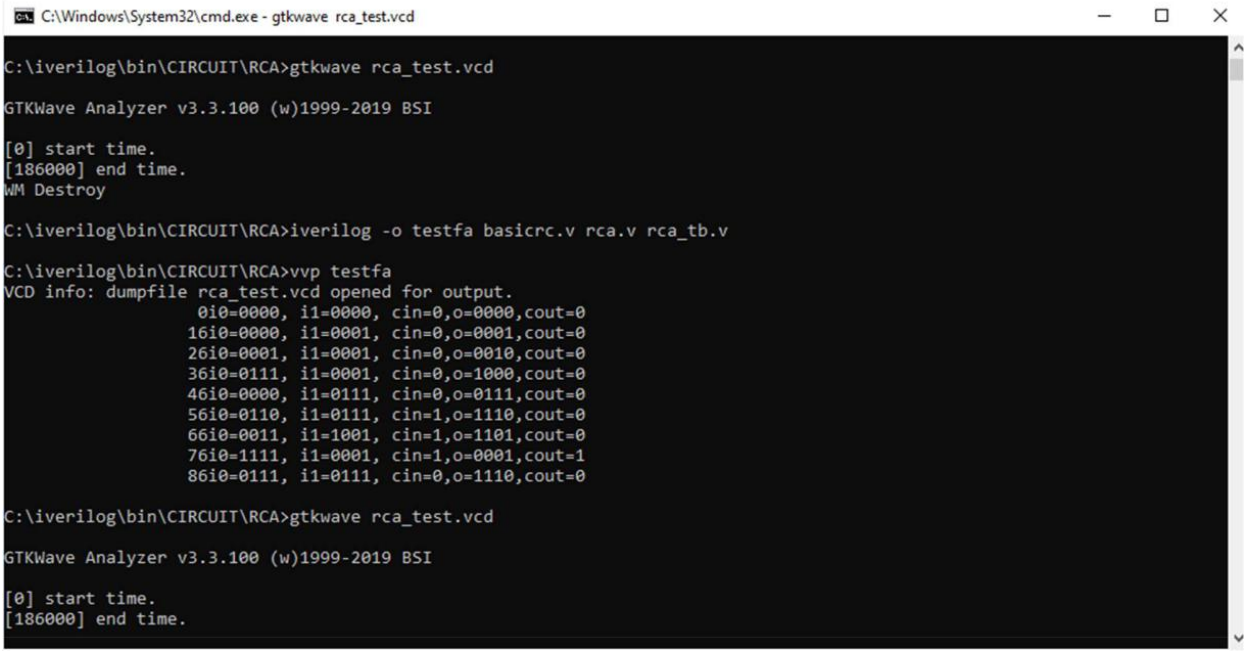
Aim:
DESIGN A FOUR RIPPLE CARRY ADDER USING FULL ADDERS

AND VERIFY THE ADDITION OF TWO FOUR BIT NUMBER

1: Screen Shot of the source code



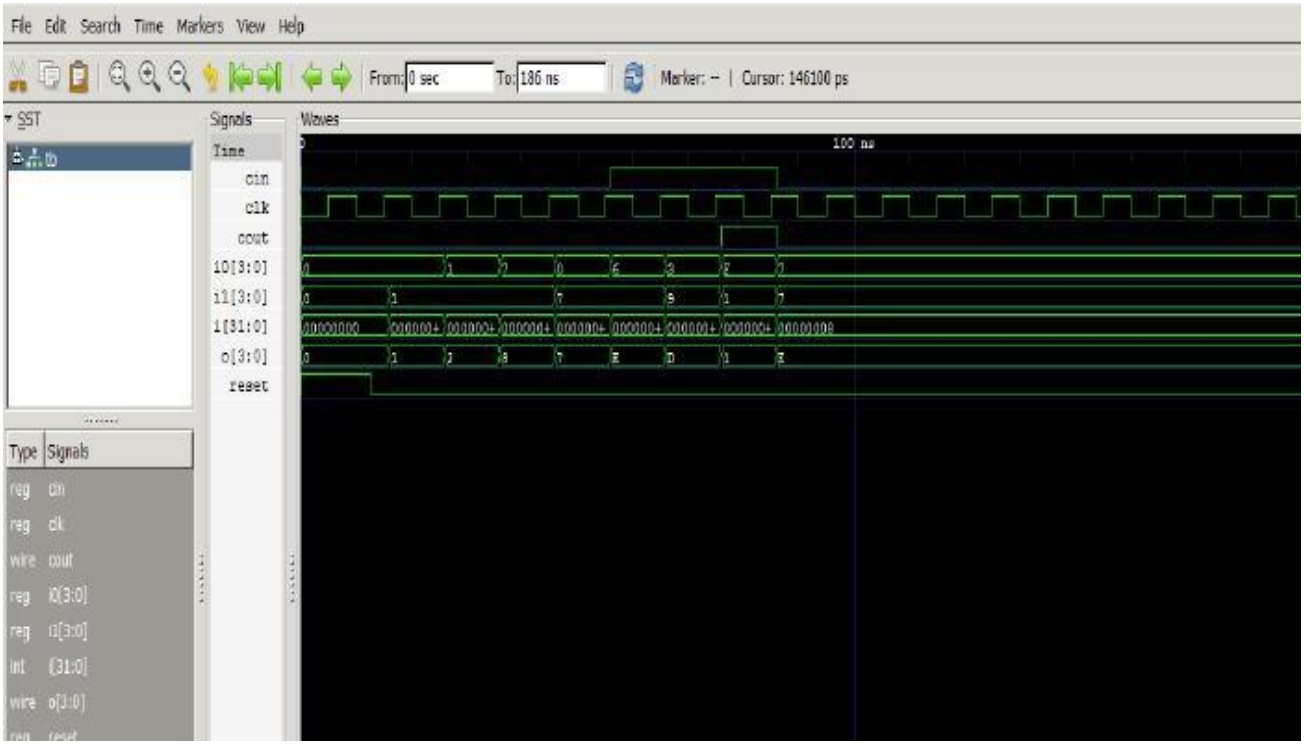
2: Screen Shot of the VVP command output



Truth Table of Ripple Carry Adder

a3	a2	a1	a0	b3	b2	b1	b0	cin						
I0[3]	I0[2]	I0[1]	I0[0]	I1[3]	I1[2]	I1[1]	I1[0]	cin	OO[3]	OO[2]	OO[1]	OO[0]	cout	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0+0=0
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0+1=1
0	0	0	1	0	0	0	1	0	0	0	1	0	0	1+1=2
0	1	1	1	0	0	0	1	0	1	0	0	0	0	7+1=8
0	0	0	0	0	1	1	1	0	0	1	1	1	0	0+7=7
0	1	1	0	0	1	1	1	0	1	1	0	1	0	6+7=E
0	0	1	1	1	0	0	1	1	1	1	0	1	0	3+9+1=D
1	1	1	1	0	0	0	1	1	0	0	0	1	1	F+1+1=1
0	1	1	1	0	1	1	1	0	1	1	1	0	0	7+7=E

3: Screen shot of the GTKWave form



Date:15/09/2020

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Week #2

Program #3

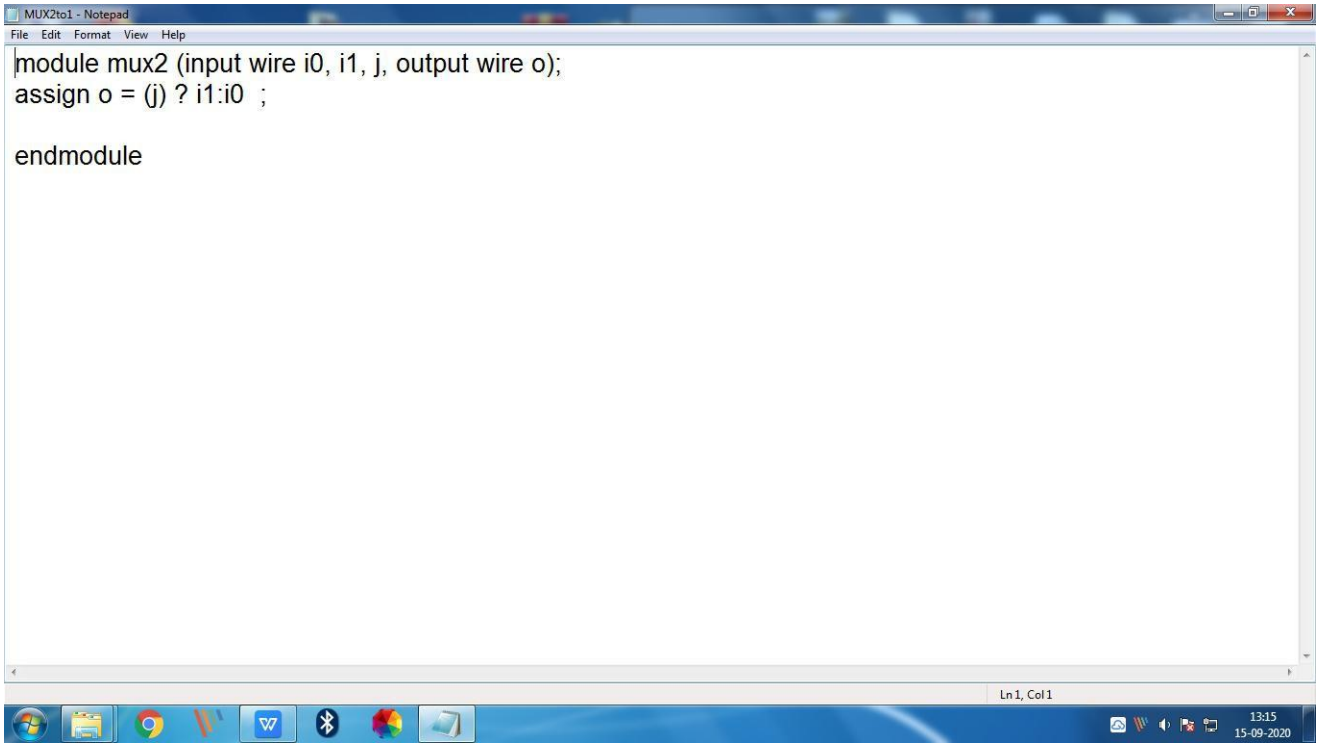
Title :

2 TO 1 MULTIPLEXER

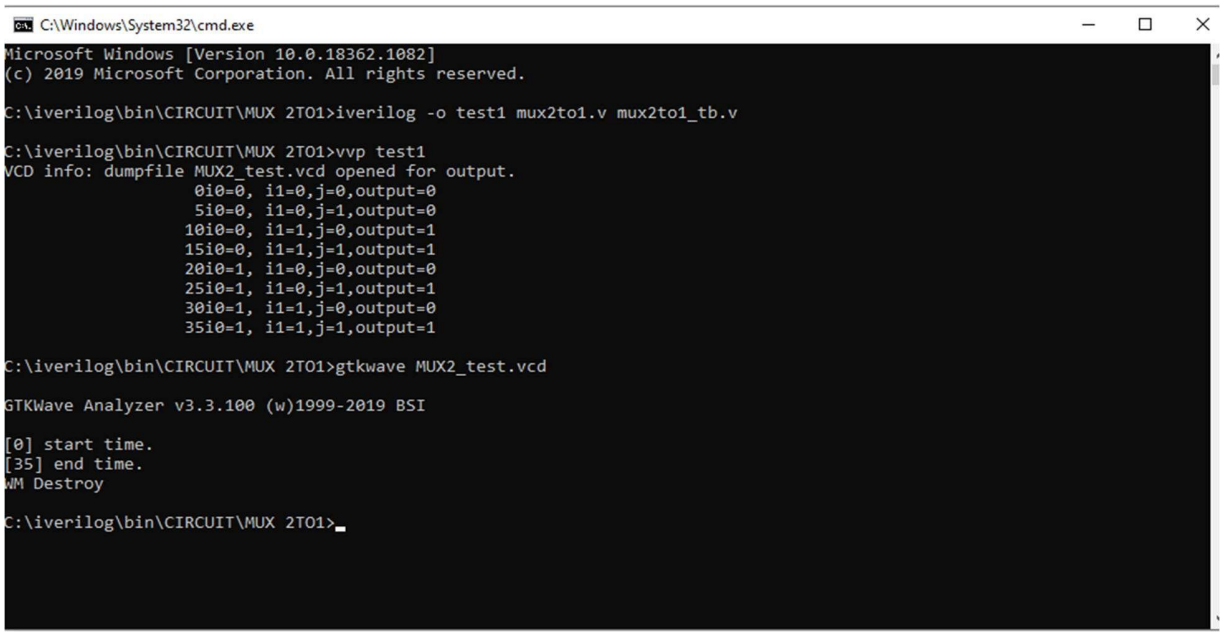
Aim:

DESIGN A 2 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE

1: Screen Shot of the source code

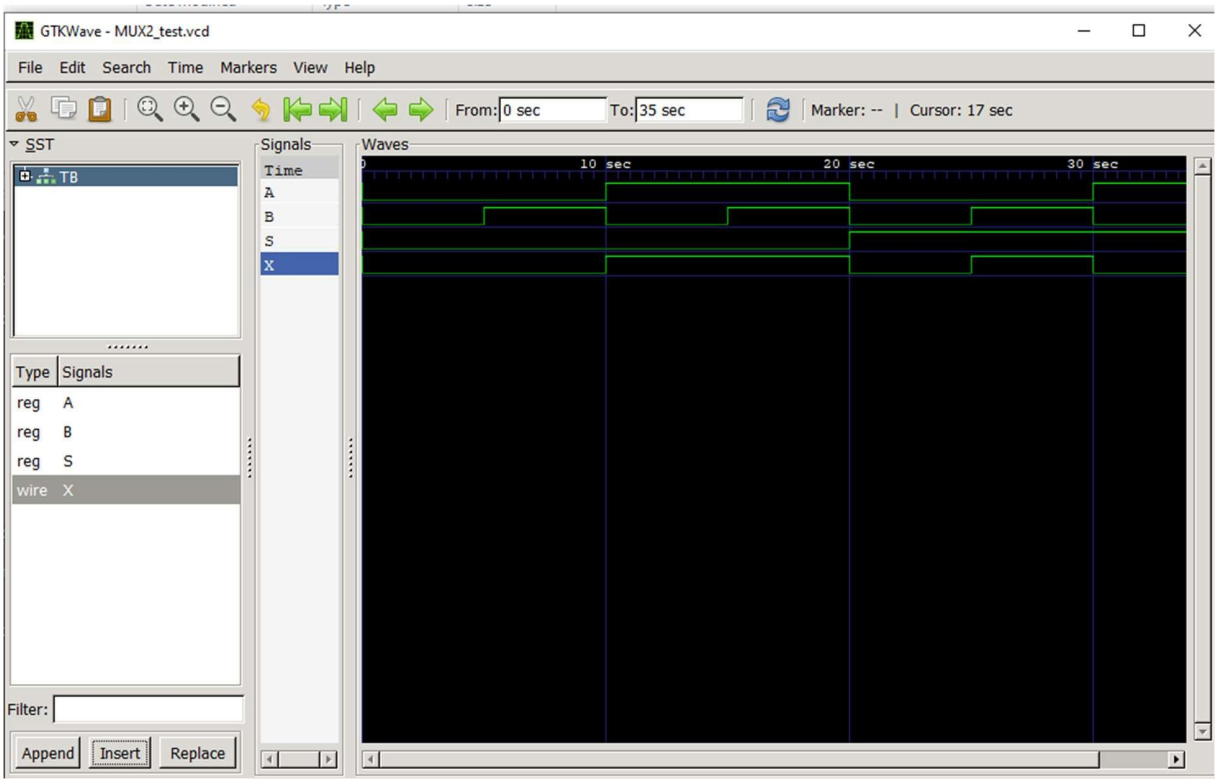


2: Screen Shot of the VVP command output



[S]j	[A]i_0	[B]i_1	[X]y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

3: Screen shot of the GTKWave form



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Week #2

Program #4

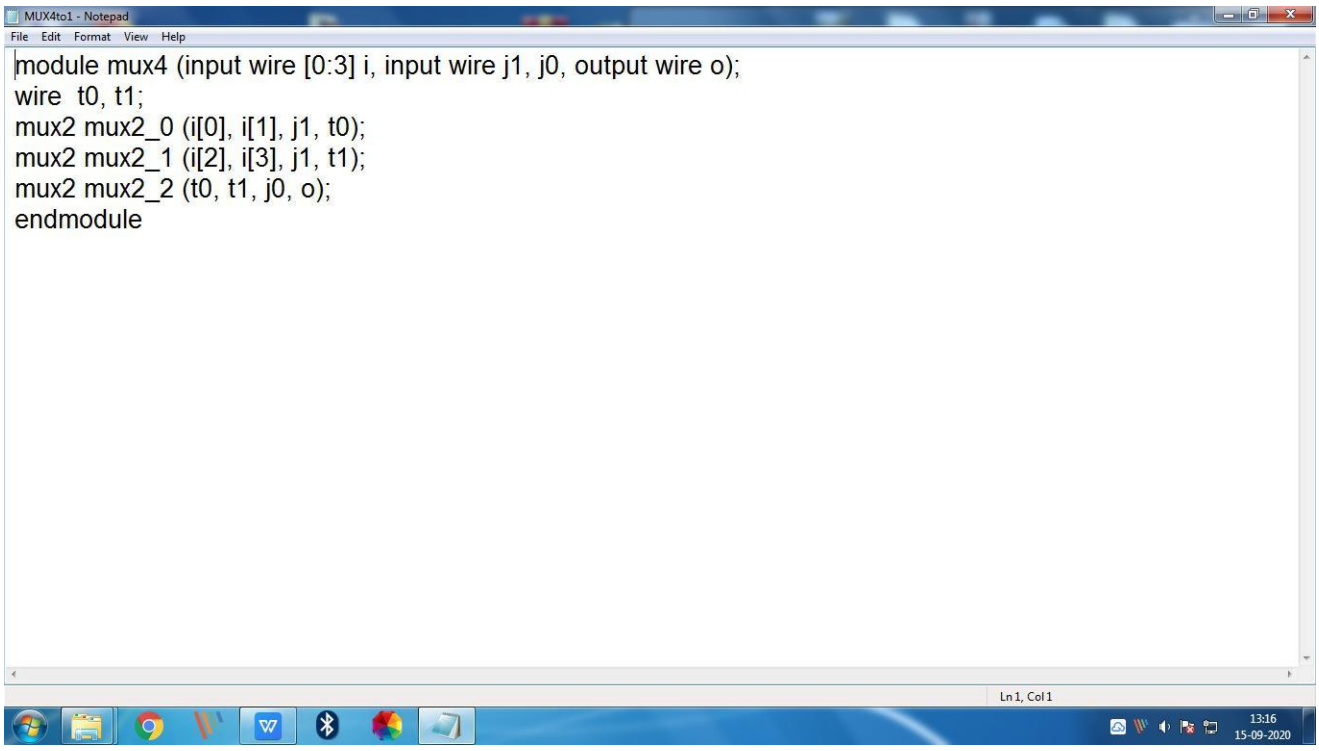
Title :

4 TO 1 MULTIPLEXER

Aim:

DESIGN A 4 TO 1 MULTIPLEXER UING 2TO 1 MULTIPLEXERS AND VERIFY ITS TRUTH TABLE

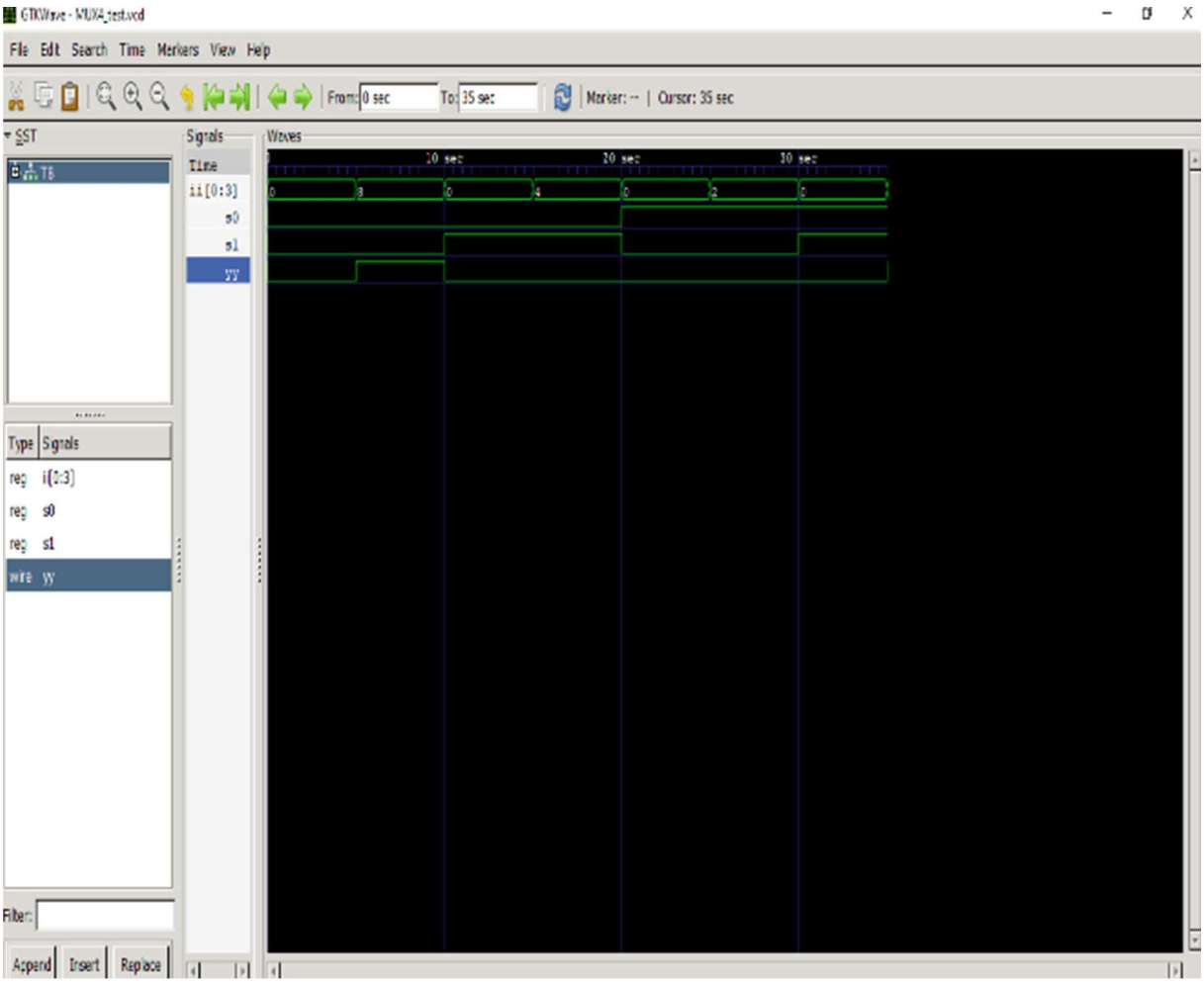
1: Screen Shot of the source code



2.Truth Table for 4:1 MUX

ii[0:3]	ii[0]	ii[1]	ii[2]	ii[3]	S_0	S_1	yy
0000	0	0	0	0	0	0	0
1000	1	0	0	0	0	0	1
0000	0	0	0	0	0	1	0
0100	0	1	0	0	0	1	0
0000	0	0	0	0	1	0	0
0010	0	0	1	0	1	0	0
0000	0	0	0	0	1	1	0
0001	0	0	0	1	1	1	1

3: Screen shot of the GTKWave form



Disclaimer:

The programs and output submitted is duly written, verified and executed my me.
I have not copied from any of my peers nor from the external resource such as internet.
If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Suhan.B.Revankar

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