

# **Digital Design and Computer Organization Laboratory**

**UE19CS206**

**3<sup>rd</sup> Semester, Academic Year 2020-21**

**Date:15—09—2020**

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**Week #2**

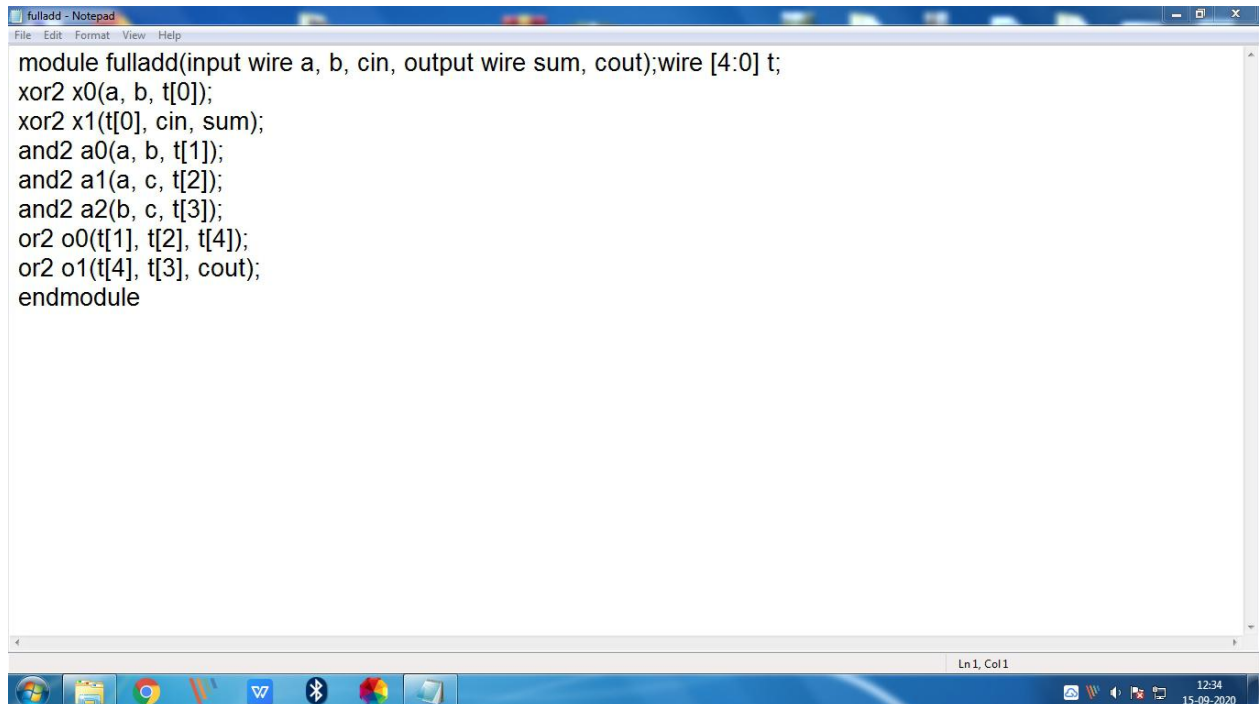
# Program #1

**Title : FULL ADDER USING BASIC GATES**

**Aim :**

**DESIGN A FULL ADDER USING BASIC GATES AND VERIFY THE FULL ADDER TRUTH TABLE**

## 1: Screen Shot of the source code

A screenshot of a Windows desktop environment. A Notepad window titled 'fulladd - Notepad' is open, displaying Verilog code for a full adder. The code defines a module 'fulladd' with inputs 'a', 'b', and 'cin', and outputs 'sum' and 'cout'. It uses a 4-bit wire 't' and implements the logic using XOR and AND gates. The Windows taskbar at the bottom shows icons for the Start menu, File Explorer, Google Chrome, Microsoft Word, and other applications. The system tray on the right indicates the time as 12:34 on 13-09-2020.

```
module fulladd(input wire a, b, cin, output wire sum, cout);wire [4:0] t;
xor2 x0(a, b, t[0]);
xor2 x1(t[0], cin, sum);
and2 a0(a, b, t[1]);
and2 a1(a, c, t[2]);
and2 a2(b, c, t[3]);
or2 o0(t[1], t[2], t[4]);
or2 o1(t[4], t[3], cout);
endmodule
```

## 2: Screen Shot of the VVP command output

```
D:\DDCO LAB PROGRAMS>iverilog -o testfa basic.v fulladd.v fulladd_tb.v

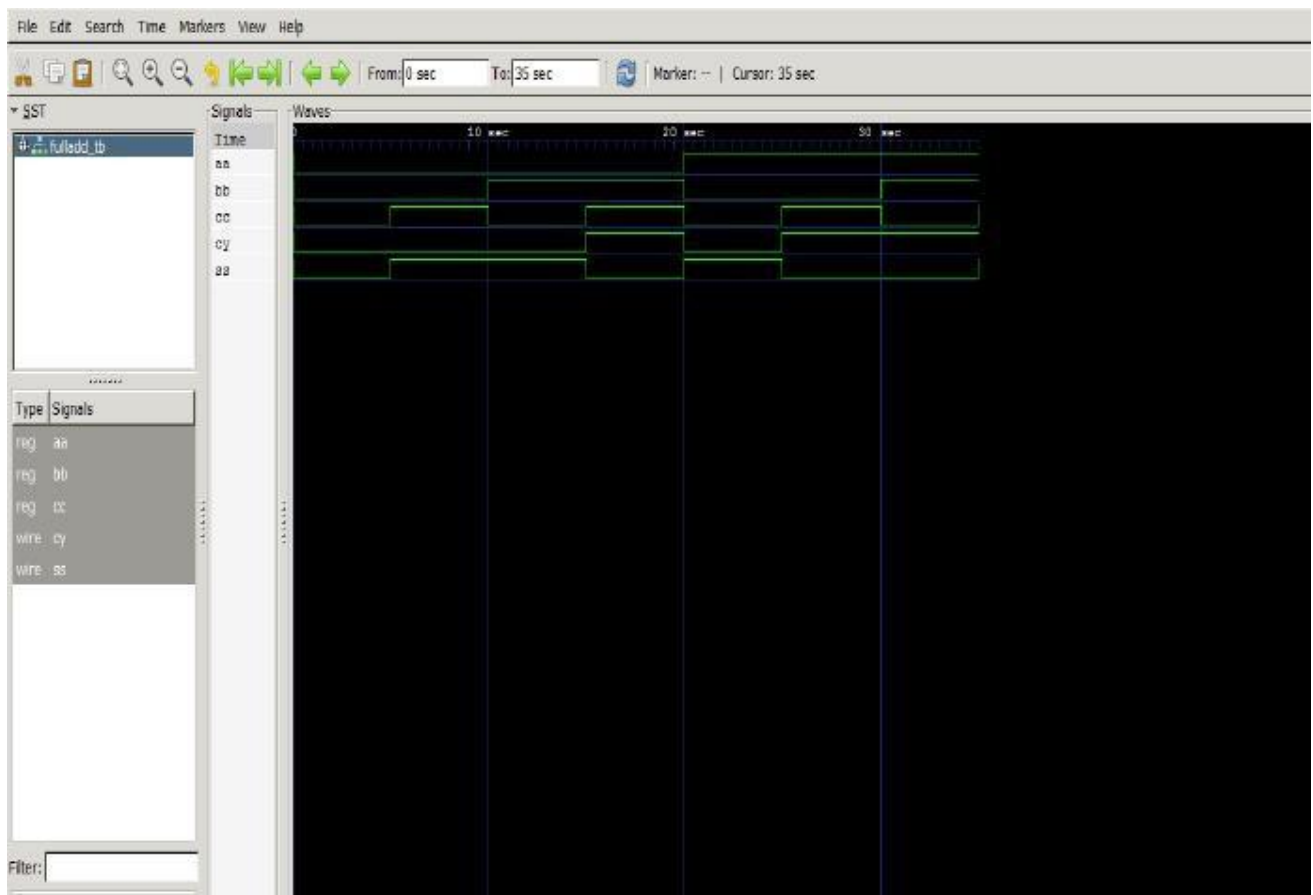
D:\DDCO LAB PROGRAMS>vvp testfa
VCD info: dumpfile fulladd_test.vcd opened for output.
      0a=0, b=0, c=0,sum=0,carry=0
      5a=0, b=0, c=1,sum=1,carry=0
     10a=0, b=1, c=0,sum=1,carry=0
     15a=0, b=1, c=1,sum=0,carry=1
     20a=1, b=0, c=0,sum=1,carry=0
     25a=1, b=0, c=1,sum=0,carry=1
     30a=1, b=1, c=0,sum=0,carry=1
     35a=1, b=1, c=1,sum=1,carry=1

D:\DDCO LAB PROGRAMS>gtkwave fulladd_test.vcd

GTKWave Analyzer v3.3.71 (w)1999-2016 BSI

[0] start time.
[35] end time.
WM Destroy
```

### 3: Screen shot of the GTKWave form



**Date:15/09/2020**

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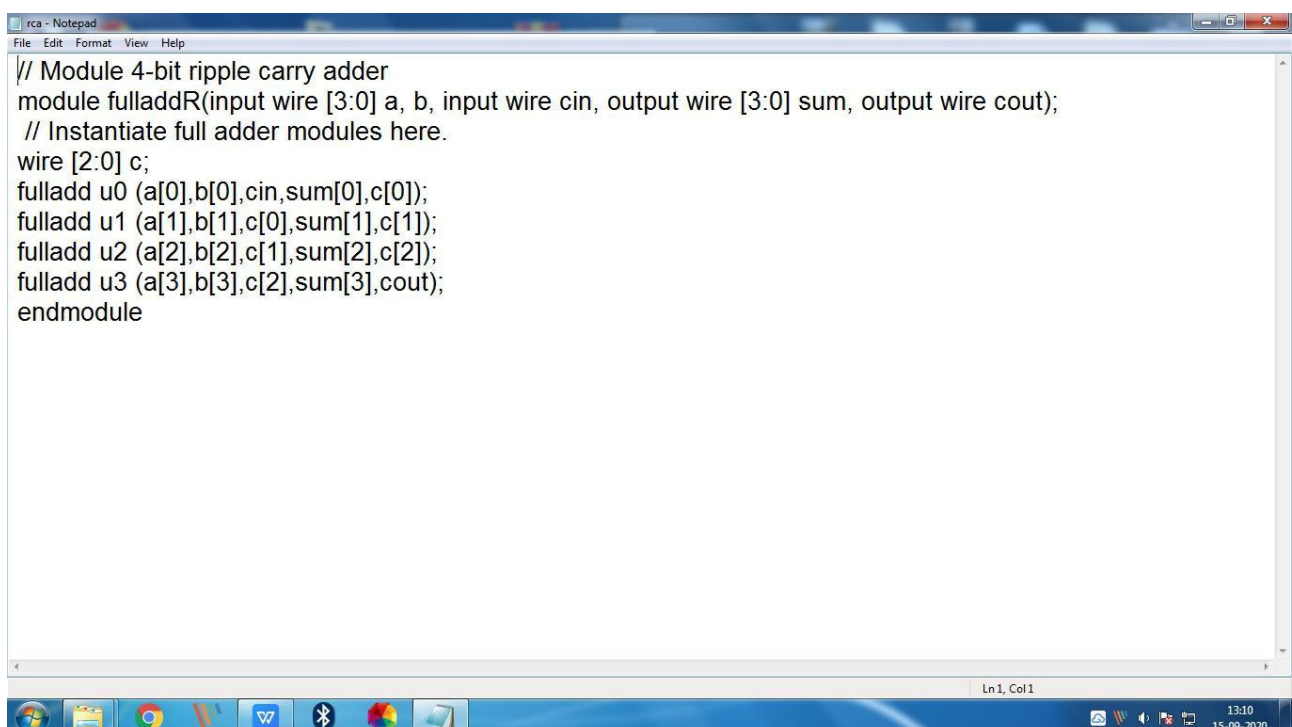
## **Week #2**

### **Program #2**

**Title :**  
**4 BIT RIPPLE CARRY ADDER**

**Aim:**  
**DESIGN A FOUR RIPPLE CARRY ADDER USING FULL ADDERS**  
**AND VERIFY THE ADDITION OF TWO FOUR BIT NUMBER**

#### **1: Screen Shot of the source code**



```
// Module 4-bit ripple carry adder
module fulladdR(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);
    // Instantiate full adder modules here.
    wire [2:0] c;
    fulladd u0 (a[0],b[0],cin,sum[0],c[0]);
    fulladd u1 (a[1],b[1],c[0],sum[1],c[1]);
    fulladd u2 (a[2],b[2],c[1],sum[2],c[2]);
    fulladd u3 (a[3],b[3],c[2],sum[3],cout);
endmodule
```

## 2: Screen Shot of the VVP command output

```

C:\Windows\System32\cmd.exe - gtkwave rca_test.vcd

C:\iverilog\bin\CIRCUIT\RCA>gtkwave rca_test.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[186000] end time.
WM Destroy

C:\iverilog\bin\CIRCUIT\RCA>iverilog -o testfa basicrc.v rca.v rca_tb.v

C:\iverilog\bin\CIRCUIT\RCA>vvp testfa
VCD info: dumpfile rca_test.vcd opened for output.
      0i0=0000, i1=0000, cin=0,o=0000,cout=0
      16i0=0000, i1=0001, cin=0,o=0001,cout=0
      26i0=0001, i1=0001, cin=0,o=0010,cout=0
      36i0=0111, i1=0001, cin=0,o=1000,cout=0
      46i0=0000, i1=0111, cin=0,o=0111,cout=0
      56i0=0110, i1=0111, cin=1,o=1110,cout=0
      66i0=0011, i1=1001, cin=1,o=1101,cout=0
      76i0=1111, i1=0001, cin=1,o=0001,cout=1
      86i0=0111, i1=0111, cin=0,o=1110,cout=0

C:\iverilog\bin\CIRCUIT\RCA>gtkwave rca_test.vcd

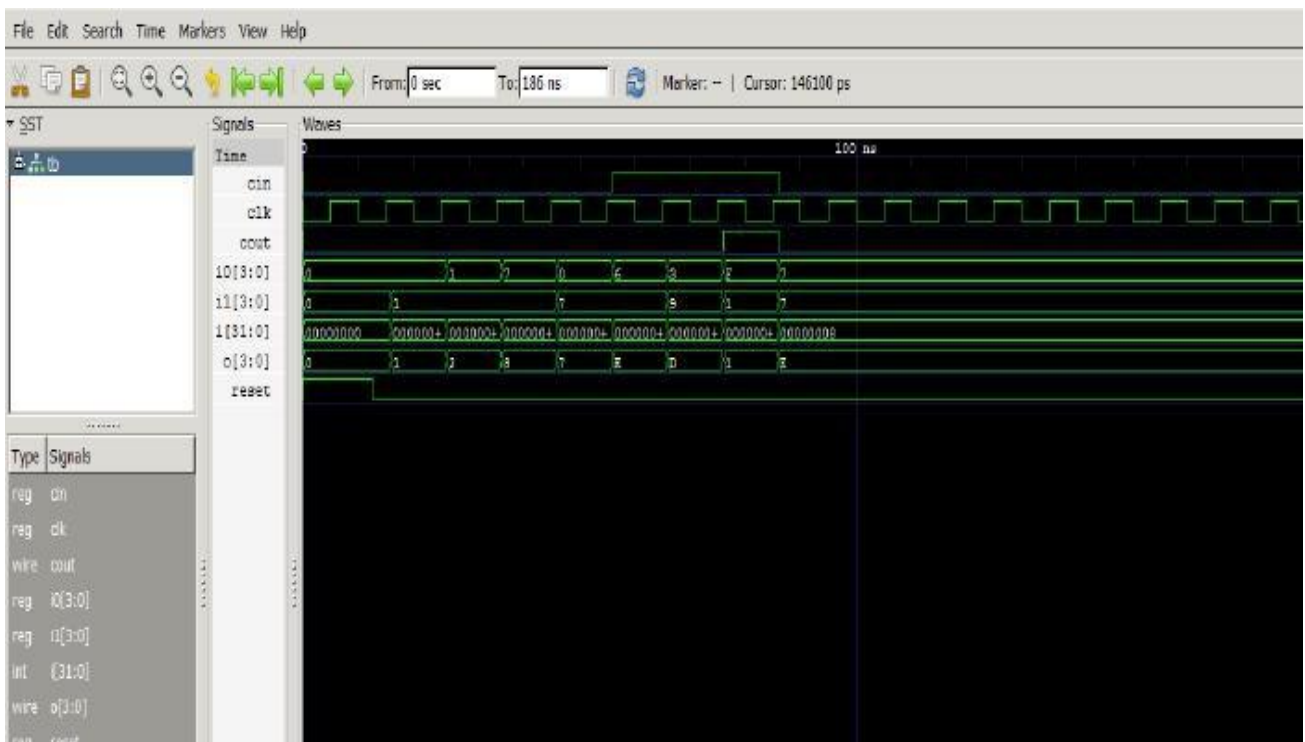
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[186000] end time.
  
```

## Truth Table of Ripple Carry Adder

a3	a2	a1	a0	b3	b2	b1	b0	cin						
IO[3]	IO[2]	IO[1]	IO[0]	I1[3]	I1[2]	I1[1]	I1[0]	cin	OO[3]	OO[2]	OO[1]	OO[0]	cout	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0+0=0
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0+1=1
0	0	0	1	0	0	0	1	0	0	0	1	0	0	1+1=2
0	1	1	1	0	0	0	1	0	1	0	0	0	0	7+1=8
0	0	0	0	0	1	1	1	0	0	1	1	1	0	0+7=7
0	1	1	0	0	1	1	1	0	1	1	0	1	0	6+7=E
0	0	1	1	1	0	0	1	1	1	1	0	1	0	3+9+1=D
1	1	1	1	0	0	0	1	1	0	0	0	1	1	F+1+1=1
0	1	1	1	0	1	1	1	0	1	1	1	0	0	7+7=E

### 3: Screen shot of the GTKWave form



**Date:15/09/2020**

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**PES2UG19CS412**

**Section**

**G**

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**Week #2**

**Program #3**

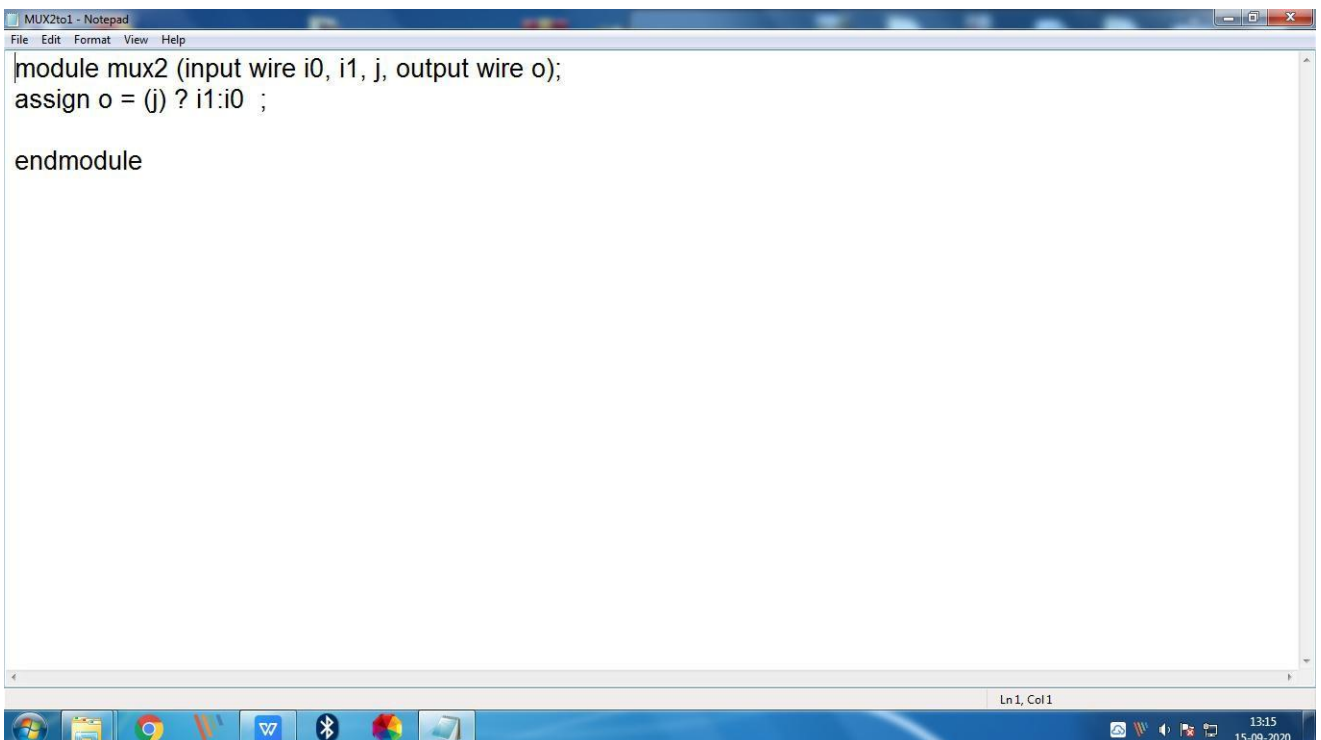
**Title :**

**2 TO 1 MULTIPLEXER**

**Aim:**

**DESIGN A 2 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE**

**1: Screen Shot of the source code**



The screenshot shows a Notepad window titled "MUX2to1 - Notepad". The text area contains the following Verilog code:

```
module mux2 (input wire i0, i1, j, output wire o);  
assign o = (j) ? i1:i0 ;  
  
endmodule
```

The status bar at the bottom of the Notepad window indicates "Ln1, Col1". The Windows taskbar is visible at the bottom of the screen, showing the Start button, taskbar icons for File Explorer, Google Chrome, and Microsoft Word, and the system tray with the date and time "13:15 15-09-2020".



## 2: Screen Shot of the VVP command output

```
C:\Windows\System32\cmd.exe
Microsoft Windows [Version 10.0.18362.1082]
(c) 2019 Microsoft Corporation. All rights reserved.

C:\iverilog\bin\CIRCUIT\MUX 2T01>iverilog -o test1 mux2to1.v mux2to1_tb.v

C:\iverilog\bin\CIRCUIT\MUX 2T01>vvp test1
VCD info: dumpfile MUX2_test.vcd opened for output.
    0i0=0, i1=0,j=0,output=0
    5i0=0, i1=0,j=1,output=0
   10i0=0, i1=1,j=0,output=1
   15i0=0, i1=1,j=1,output=1
   20i0=1, i1=0,j=0,output=0
   25i0=1, i1=0,j=1,output=1
   30i0=1, i1=1,j=0,output=0
   35i0=1, i1=1,j=1,output=1

C:\iverilog\bin\CIRCUIT\MUX 2T01>gtkwave MUX2_test.vcd

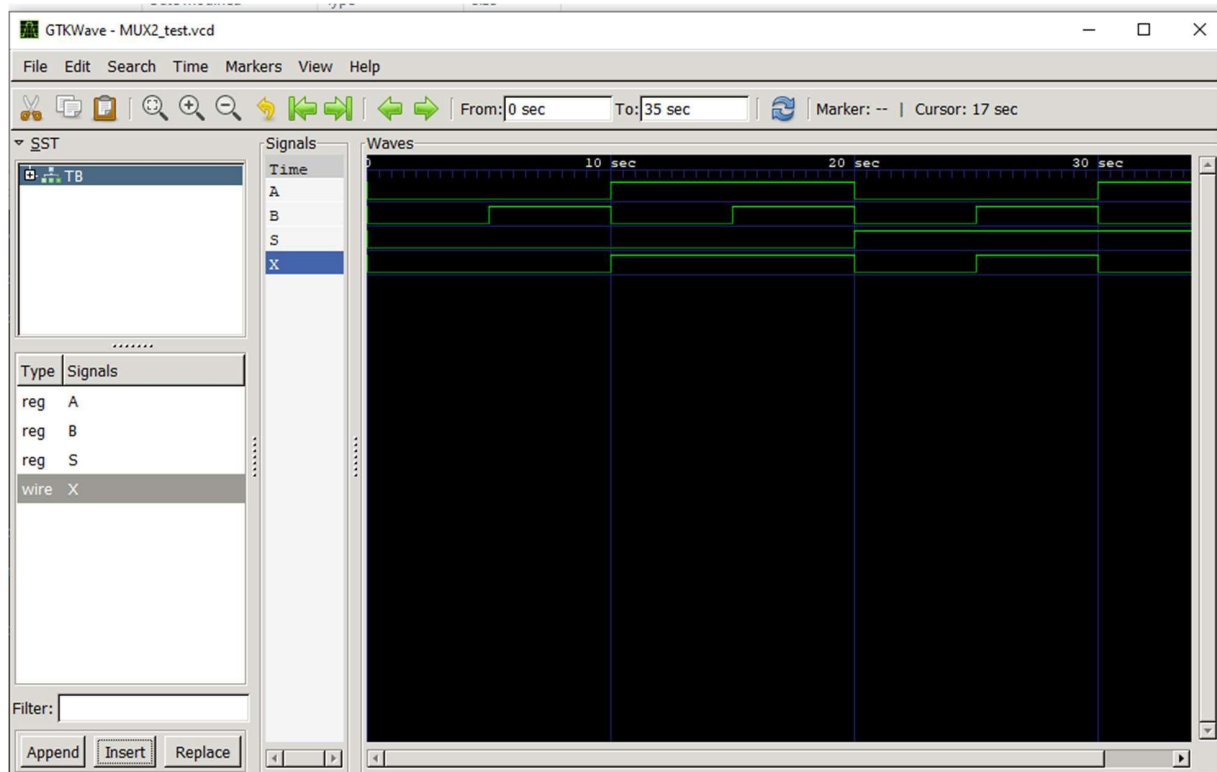
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[35] end time.
WM Destroy

C:\iverilog\bin\CIRCUIT\MUX 2T01>
```

[S]j	[A]i <sub>0</sub>	[B]i <sub>1</sub>	[X]y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

### 3: Screen shot of the GTKWave form



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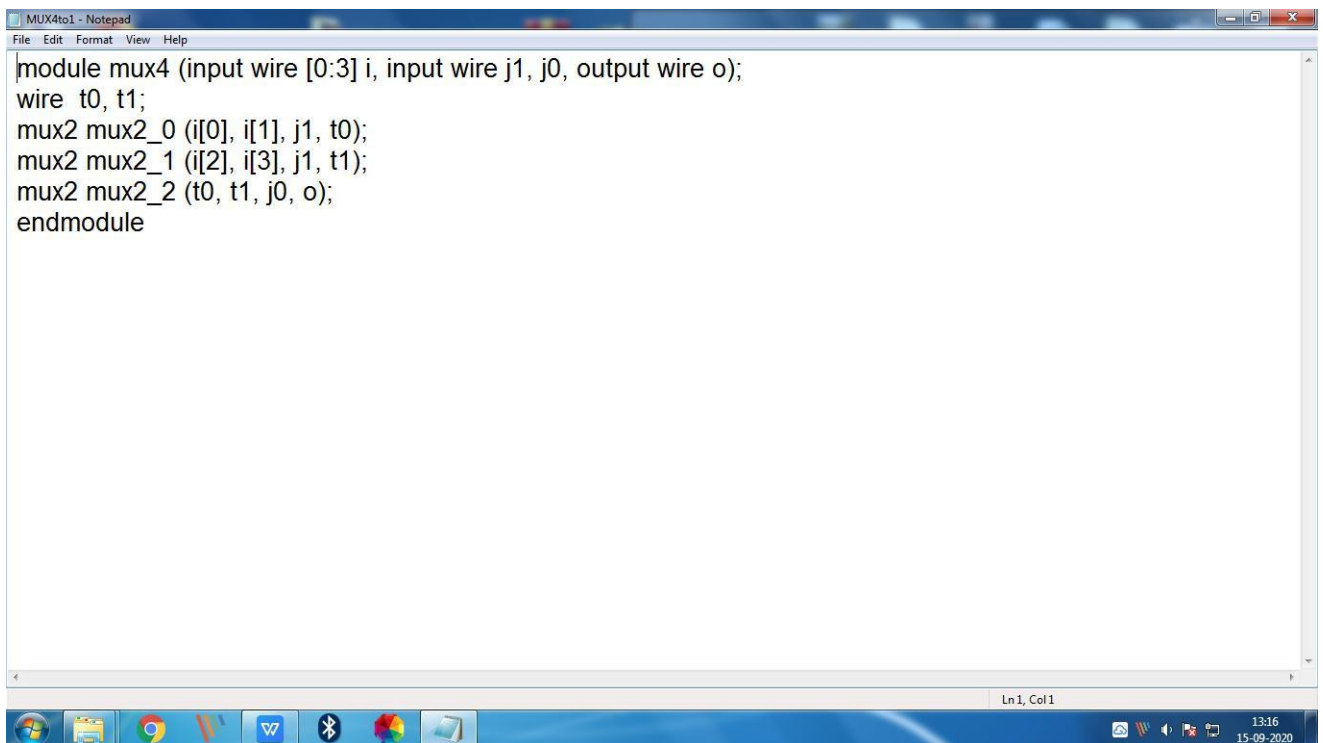
**Week #2**

**Program #4**

**Title :**  
**4 TO 1 MULTIPLEXER**

**Aim:**  
**DESIGN A 4 TO 1 MULTIPLEXER USING 2 TO 1 MULTIPLEXERS**  
**AND VERIFY ITS TRUTH TABLE**

**1: Screen Shot of the source code**



The screenshot shows a Notepad window titled "MUX4to1 - Notepad" with a menu bar (File, Edit, Format, View, Help). The text area contains the following Verilog code:

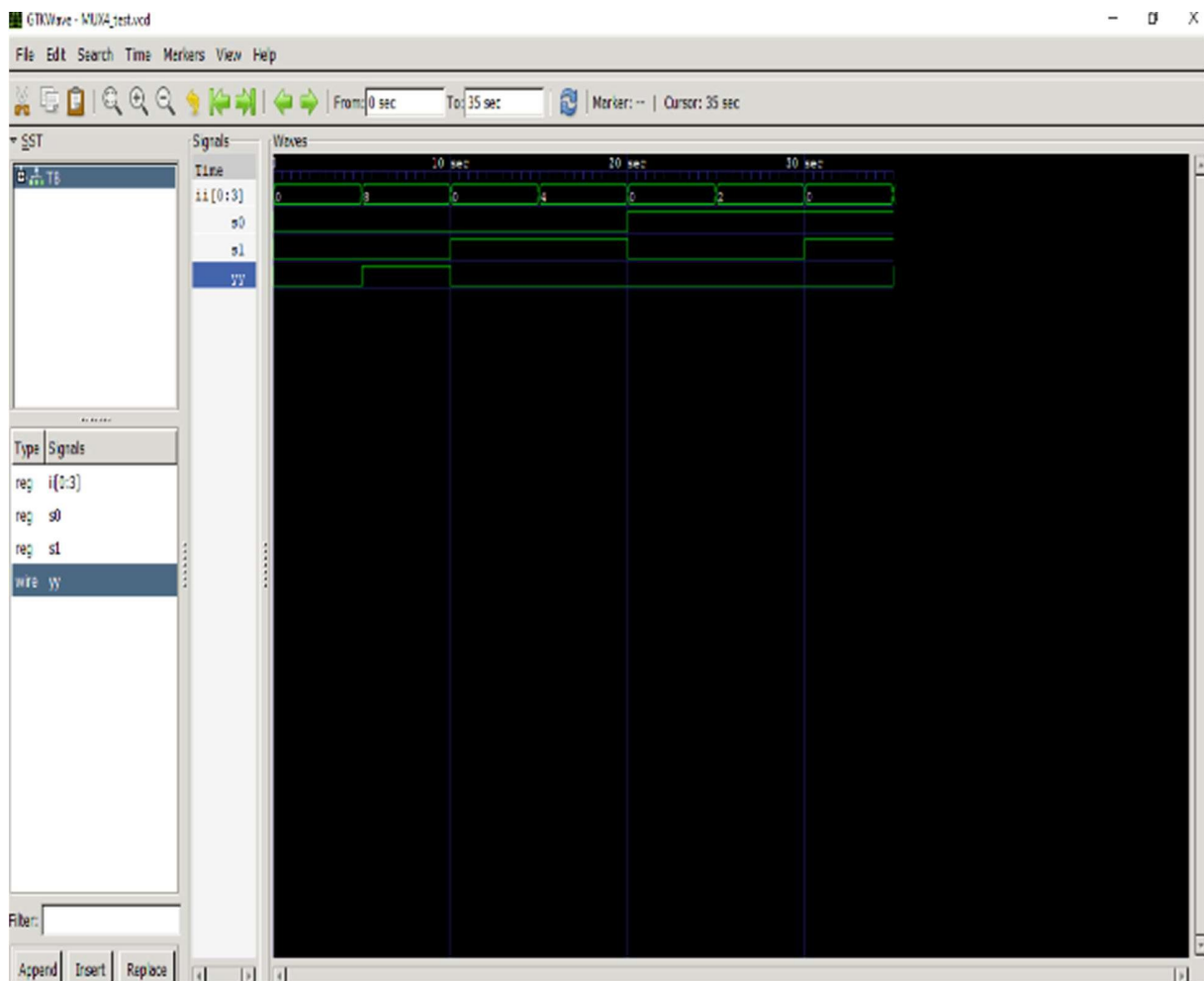
```
module mux4 (input wire [0:3] i, input wire j1, j0, output wire o);  
  wire t0, t1;  
  mux2 mux2_0 (i[0], i[1], j1, t0);  
  mux2 mux2_1 (i[2], i[3], j1, t1);  
  mux2 mux2_2 (t0, t1, j0, o);  
endmodule
```

The status bar at the bottom indicates "Ln 1, Col 1". The Windows taskbar is visible at the bottom with various icons and a system clock showing 13:16 on 15-09-2020.

## 2.Truth Table for 4:1 MUX

ii[0:3]	ii[0]	ii[1]	ii[2]	ii[3]	S <sub>0</sub>	S <sub>1</sub>	yy
0000	0	0	0	0	0	0	0
1000	1	0	0	0	0	0	1
0000	0	0	0	0	0	1	0
0100	0	1	0	0	0	1	0
0000	0	0	0	0	1	0	0
0010	0	0	1	0	1	0	0
0000	0	0	0	0	1	1	0
0001	0	0	0	1	1	1	1

### 3: Screen shot of the GTKWave form



### **Disclaimer:**

**The programs and output submitted is duly written, verified and executed by me.  
I have not copied from any of my peers nor from the external resource such as internet.  
If found plagiarized, I will abide with the disciplinary action of the University.**

**Signature: Suhan.B.Revankar**

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**Date: 15/09/2020**