

Digital Design and Computer Organization Laboratory

UE19CS206

3rd Semester, Academic Year 2020-21

Date: 20-11-2020

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Experiment Number: 8

Week #: 8


Title of the Program:

Microprocessor Control Logic – 2(Load and Jump Instructions)

Aim of the Program:

To enhance the microprocessor control logic to implement a load and a jump instruction.

Code (mproc.v)

 mproc - Notepad

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```
module nor5 (input wire [0:4] i, output wire o);
```

```
    wire t;
```

```
    or3 or3_0 (i[0],i[1],i[2],t);
```

```
    nor3 nor3_0 (t,i[3],i[4],o);
```

```
endmodule
```

```
module ir (input wire clk, reset, load, input wire [15:0] din, output wire [15:0] dout);  
    dfr1 dfr1_0 (clk, reset, load, din['h0], dout['h0]);
```

```
    dfr1 dfr1_1 (clk, reset, load, din['h1], dout['h1]);
```

```
    dfr1 dfr1_2 (clk, reset, load, din['h2], dout['h2]);
```

```
    dfr1 dfr1_3 (clk, reset, load, din['h3], dout['h3]);
```

```
    dfr1 dfr1_4 (clk, reset, load, din['h4], dout['h4]);
```

```
    dfr1 dfr1_5 (clk, reset, load, din['h5], dout['h5]);
```

```
    dfr1 dfr1_6 (clk, reset, load, din['h6], dout['h6]);
```

```
    dfr1 dfr1_7 (clk, reset, load, din['h7], dout['h7]);
```

```
    dfr1 dfr1_8 (clk, reset, load, din['h8], dout['h8]);
```

```
    dfr1 dfr1_9 (clk, reset, load, din['h9], dout['h9]);
```

```
    dfr1 dfr1_a (clk, reset, load, din['ha], dout['ha]);
```

```
    dfr1 dfr1_b (clk, reset, load, din['hb], dout['hb]);
```

```
    dfr1 dfr1_c (clk, reset, load, din['hc], dout['hc]);
```

```
    dfr1 dfr1_d (clk, reset, load, din['hd], dout['hd]);
```

```
    dfr1 dfr1_e (clk, reset, load, din['he], dout['he]);
```

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```
dfr1 dfr1_d (clk, reset, load, din['hd'], dout['hd']);
```

```
dfr1 dfr1_e (clk, reset, load, din['he'], dout['he']);
```

```
dfr1 dfr1_f (clk, reset, load, din['hf'], dout['hf']);
```

```
endmodule
```

```
module control_logic (input wire clk, reset, input wire [15:0] cur_ins, output wire [2:0] rd_addr_a, rd_addr_b, wr_addr,  
    output wire [1:0] op, output wire sel, jump, pc_inc, load_ir, wr_reg);
```

```
// Copy your assignment 3 logic here and modify.
```

```
wire s,u,w,ld_ins_,ld_ins, wr_reg1,wr_reg2;
```

```
wire fo,eo,lo, fi, ef, el;
```

```
assign rd_addr_a=cur_ins[2:0];
```

```
assign rd_addr_b=cur_ins[5:3];
```

```
assign wr_addr=cur_ins[8:6];
```

```
assign op = cur_ins[10:9];
```

```
invert i1(cur_ins[15],u);
```

```
invert i2(cur_ins[10],w);
```

```
invert i3(cur_ins[14],s);
```

```
invert i4(ld_ins,ld_ins_);
```

```
and2 a1(cur_ins[15],s,ld_ins);
```

```
nor5 n5({cur_ins[15],cur_ins[14],cur_ins[13],cur_ins[12],cur_ins[11]},alu_ins);
```

```
and3 a2(cur_ins[14],u,ef,jump);
```

```
dfr1 d1(clk,reset,1'b1,fo,eo);
```

```
and2 a3(ld_ins_,eo,ef);
```

```
and2 a4(ef,alu_ins,wr_reg1);
```

```
or2 o3(wr_reg1,wr_reg2,wr_reg);
```

```
and2 a5(eo,ld_ins,el);
```

```
and2 a6(ld_ins,el,wr_reg2);
```

```
nand2 n1(el,ld_ins,sel);
```

```
dfr1 d2(clk,reset,1'b1,el,lo);
```

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```
nor5 n5({cur_ins[15],cur_ins[14],cur_ins[13],cur_ins[12],cur_ins[11]},alu_ins);
and3 a2(cur_ins[14],u,ef,jump);
```

```
dfr1 d1(clk,reset,1'b1,fo,eo);
and2 a3(ld_ins_,eo,ef);
and2 a4(ef,alu_ins,wr_reg1);
or2 o3(wr_reg1,wr_reg2,wr_reg);
and2 a5(eo,ld_ins,el);
and2 a6(ld_ins,el,wr_reg2);
```

```
nand2 n1(el,ld_ins,sel);
```

```
dfr1 d2(clk,reset,1'b1,el,lo);
or2 o1(lo,ef,fi);
dfs1 d3(clk,reset,1'b1,fi,fo);
assign load_ir = fo;
or2 o2(load_ir,el,pc_inc);
```

```
endmodule
```

```
module mproc (input wire clk, reset, input wire [15:0] d_in, output wire [6:0] addr, output wire [15:0] d_out);
```

```
wire pc_inc, cout, cout_, sub, sel, sel_addr;
wire [2:0] rd_addr_a, rd_addr_b, wr_addr;
wire [1:0] op; wire [8:0] _addr;
```

```
wire [15:0] cur_ins, d_out_a, d_out_b;
```

```
and2 and2_0 (jump, cout, sub);
pc pc_0 (clk, reset, pc_inc, 1'b0, sub, {8'b0, cur_ins[7:0]}, {_addr, addr});
ir ir_0 (clk, reset, load_ir, d_in, cur_ins);
control_logic control_logic_0 (clk, reset, cur_ins, rd_addr_a, rd_addr_b, wr_addr, op, sel, jump, pc_inc, load_ir, wr_reg);
reg_alu reg_alu_0 (clk, reset, sel, wr_reg, op, rd_addr_a, rd_addr_b, wr_addr, d_in, d_out_a, d_out_b, cout);
assign d_out = d_out_a;
```

```
endmodule
```

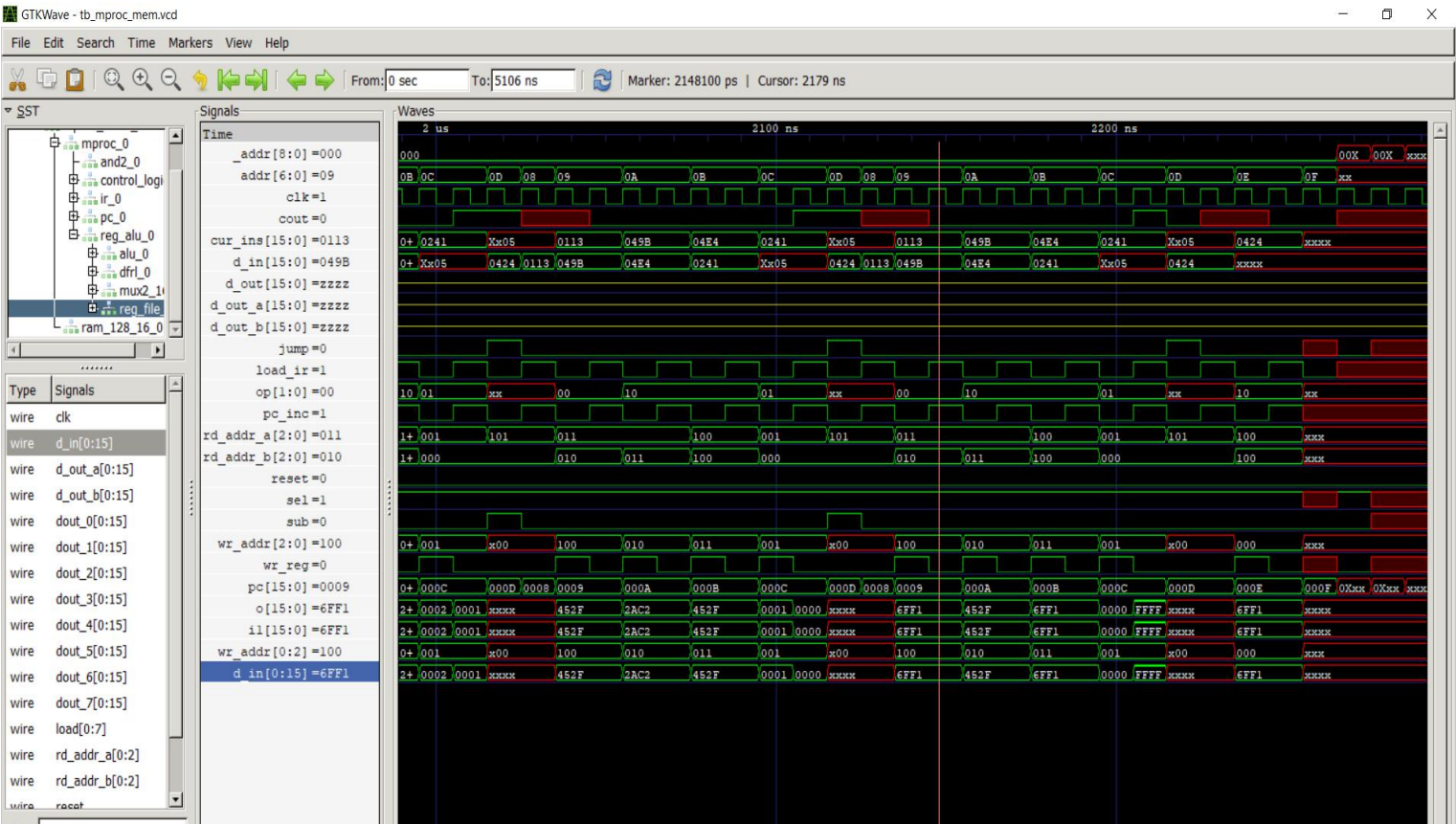
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TABLE

			In HEX				In HEX
				Fibonacci Number 11	233	89+144=233	00E9 H
Fibonacci Number 1	2	1+1 =2	0002 H	Fibonacci Number 12	377	144+233=377	0179 H
Fibonacci Number 2	3	1+2=3	0003 H	Fibonacci Number 13	610	233+377=610	0262 H
Fibonacci Number 3	5	2+3=5	0005 H	Fibonacci Number 14	987	377+610=987	03DB H
Fibonacci Number 4	8	3+5=8	0008 H	Fibonacci Number 15	1597	610+987=1597	063D H
Fibonacci Number 5	13	5+8=13	000D H	Fibonacci Number 16	2584	987+1597 =2584	0A18 H
Fibonacci Number 6	21	8+13=21	0015 H	Fibonacci Number 17	4181	1597+2584 =4181	1055 H
Fibonacci Number 7	34	13+21=34	0022 H	Fibonacci Number 18	6765	2584+4181 =6765	1A6D H
Fibonacci Number 8	55	21+34=55	0037 H	Fibonacci Number 19	10946	4181+6765 =10946	2AC2 H
Fibonacci Number 9	89	34+55=89	0059 H	Fibonacci Number 20	17711	6765+10946 =17711	452F H
Fibonacci Number 10	144	55+89=144	0090 H	Fibonacci Number 21	28657	10946+17711 =28657	6FF1 H

Output waveform

(1 screenshot showing the Fibonacci sequence)



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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