

Digital Design and Computer Organization Laboratory

UE19CS206

3rd Semester, Academic Year 2020-21

Date : 08/09/2020

Name: Suhan.B.Revankar	SRN: PES2UG19CS412	Section : G
------------------------	--------------------	-------------

Experiment number #1

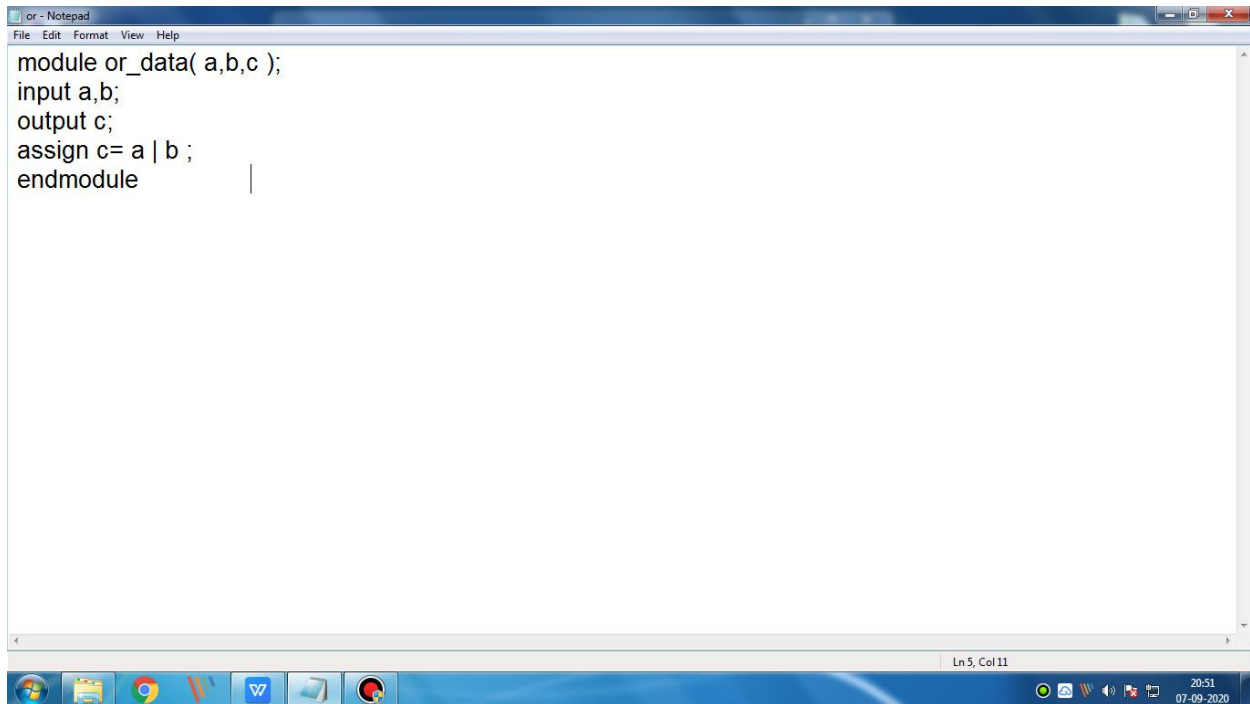
Week #1

Program #1

Title: OR gate

Aim: To write Verilog code to mimic OR gate

Program :

A screenshot of a Windows desktop environment. A Notepad window titled 'or - Notepad' is open, displaying Verilog code for an OR gate. The code is as follows:

```
module or_data( a,b,c );  
input a,b;  
output c;  
assign c= a | b ;  
endmodule
```

The cursor is positioned at the end of the 'endmodule' line. The Notepad window has a standard menu bar with 'File', 'Edit', 'Format', 'View', and 'Help'. The Windows taskbar is visible at the bottom, showing icons for the Start menu, File Explorer, Google Chrome, and other applications. The system tray on the right shows the time as 20:51 and the date as 07-09-2020.

Command Prompt Output:

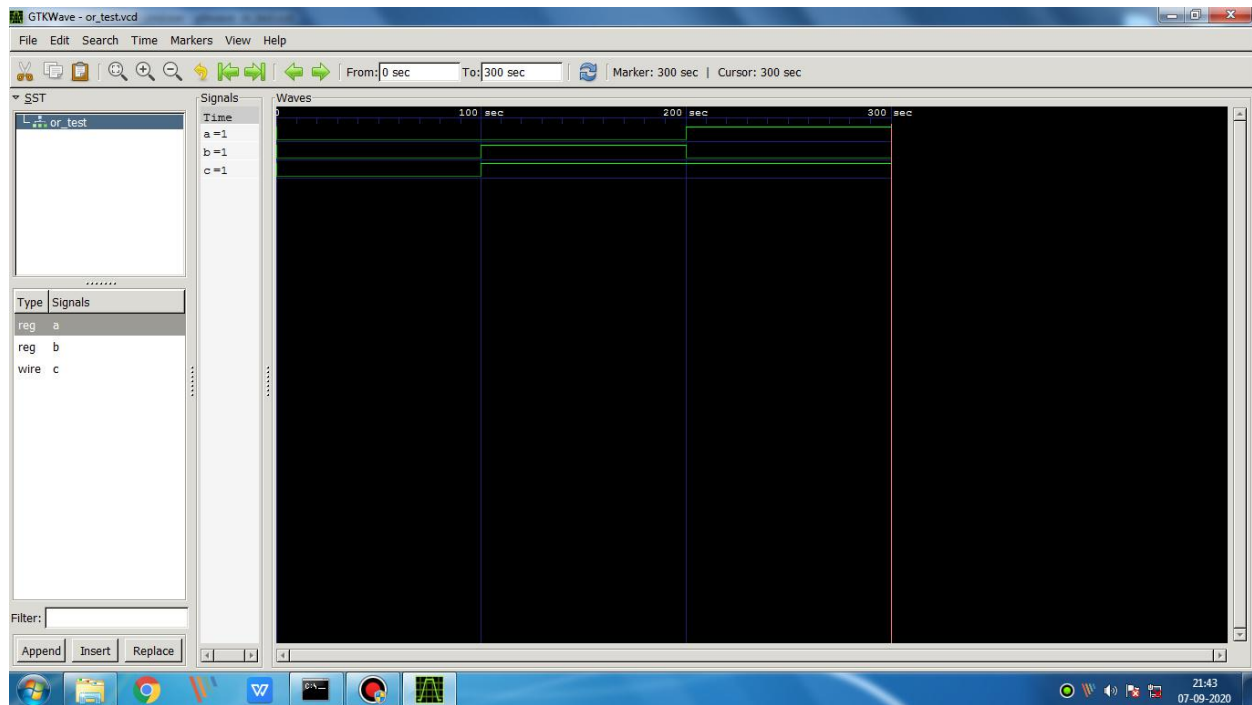
```
C:\Windows\System32\cmd.exe
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\De11\Desktop\iverilog>iverilog -o OrGate or.v or2_th.v
C:\Users\De11\Desktop\iverilog>vvp OrGate
VCD info: dumpfile or_test.vcd opened for output.
      0a=0, b=0, c=0
    100a=0, b=1, c=1
    200a=1, b=0, c=1
    300a=1, b=1, c=1
C:\Users\De11\Desktop\iverilog>gtkwave or_test.vcd
```

Truth Table :

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Wave Form :

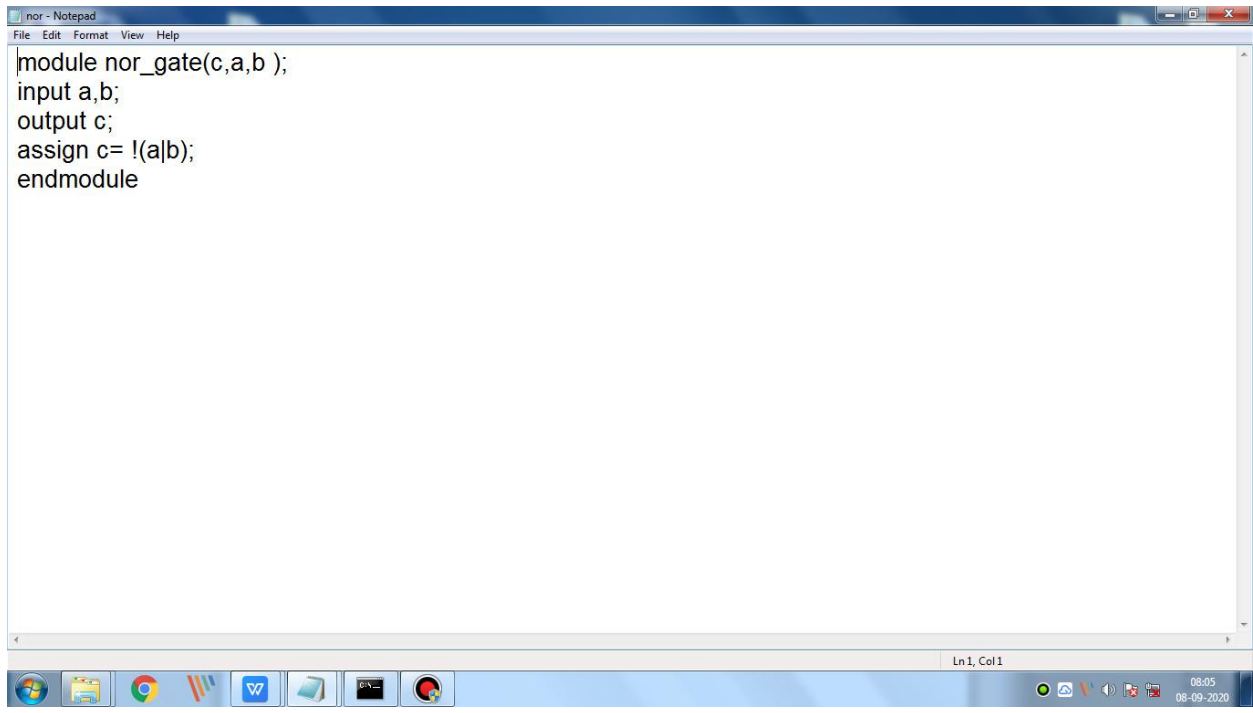


Program #2

Title: NOR gate

Aim: To write Verilog code to mimic NOR gate

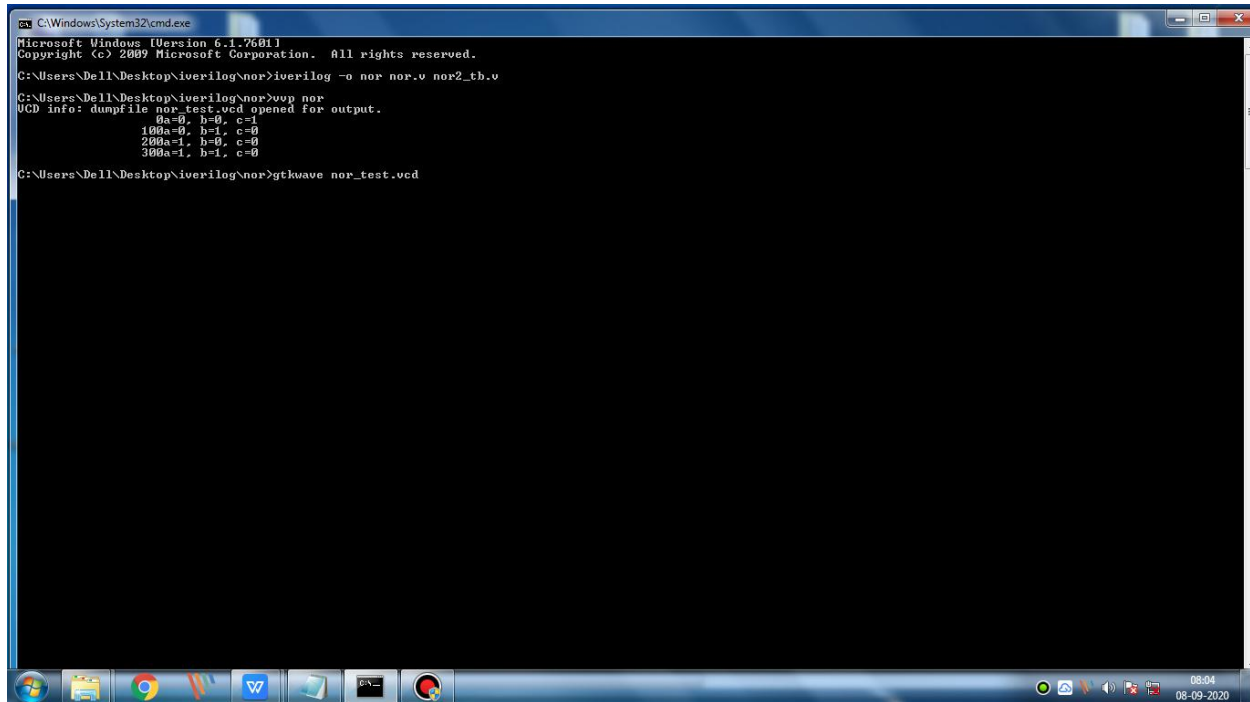
Program:

A screenshot of a Windows Notepad application window titled 'nor - Notepad'. The window contains the following Verilog code:

```
module nor_gate(c,a,b );  
input a,b;  
output c;  
assign c= !(a|b);  
endmodule
```

The code is written in a monospaced font. The window's menu bar includes 'File', 'Edit', 'Format', 'View', and 'Help'. The status bar at the bottom of the window shows 'Ln 1, Col 1'. Below the window, a portion of the Windows taskbar is visible, showing icons for the Start menu, File Explorer, Google Chrome, Microsoft Word, and a terminal window. The system clock in the bottom right corner displays '08:05' and '08-09-2020'.

CMD output:



```
C:\Windows\System32\cmd.exe
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

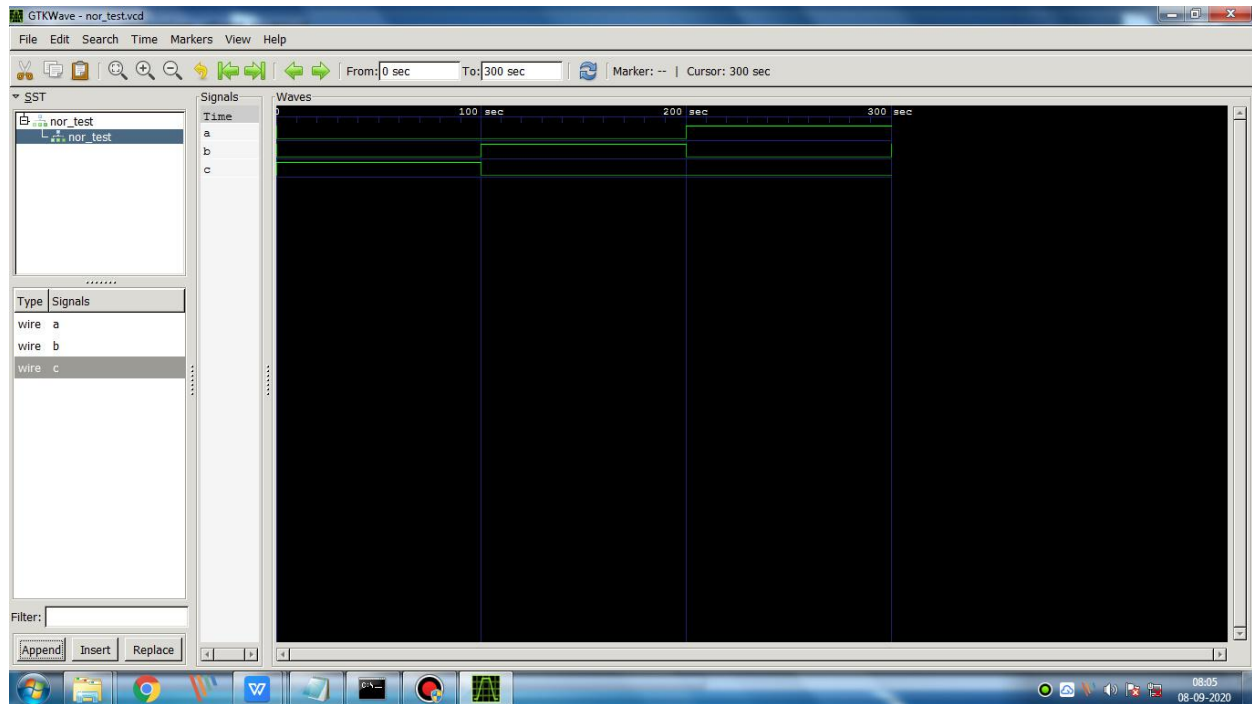
C:\Users\De11\Desktop\iverilog\nor>iverilog -o nor.nor.v nor2_tb.v
C:\Users\De11\Desktop\iverilog\nor>vvp nor
VCD info: dumpfile nor_test.vcd opened for output.
00a=0, b=0, c=1
100a=0, b=1, c=0
200a=1, b=0, c=0
300a=1, b=1, c=0

C:\Users\De11\Desktop\iverilog\nor>gtkwave nor_test.vcd
```

Truth Table:

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Wave Form:

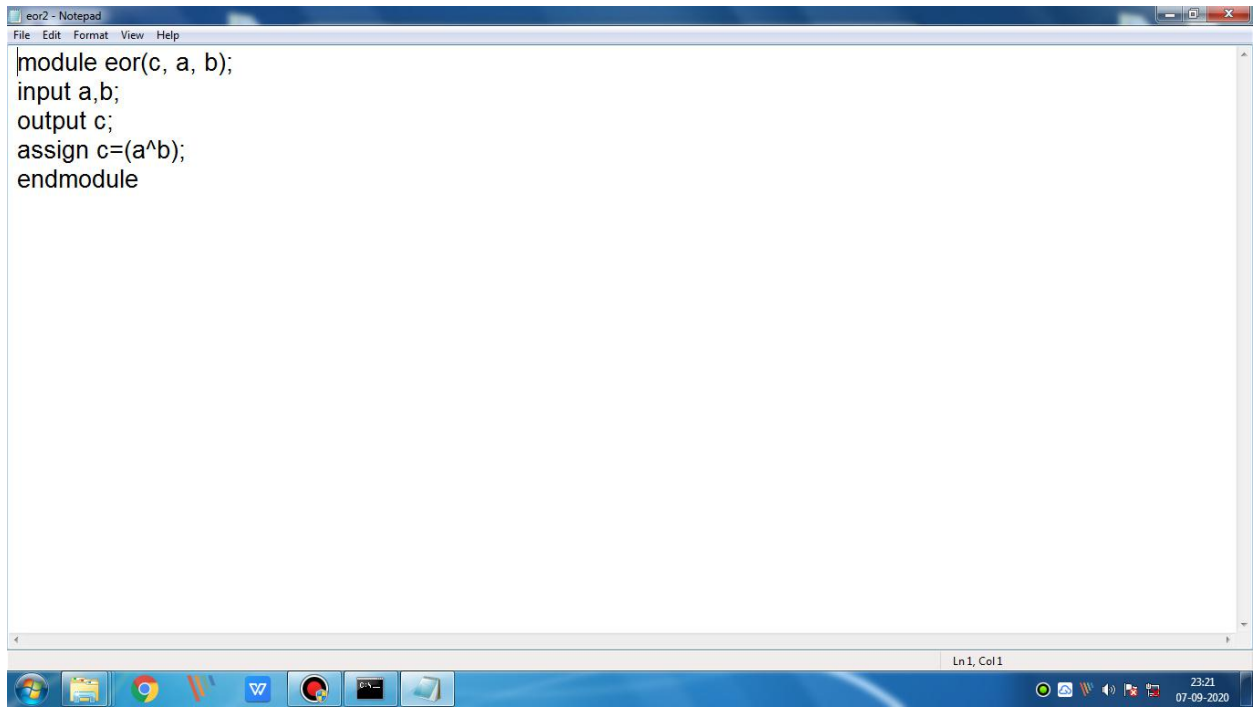


Program #3

Title: EOR gate

Aim: To write Verilog code to mimic EOR gate

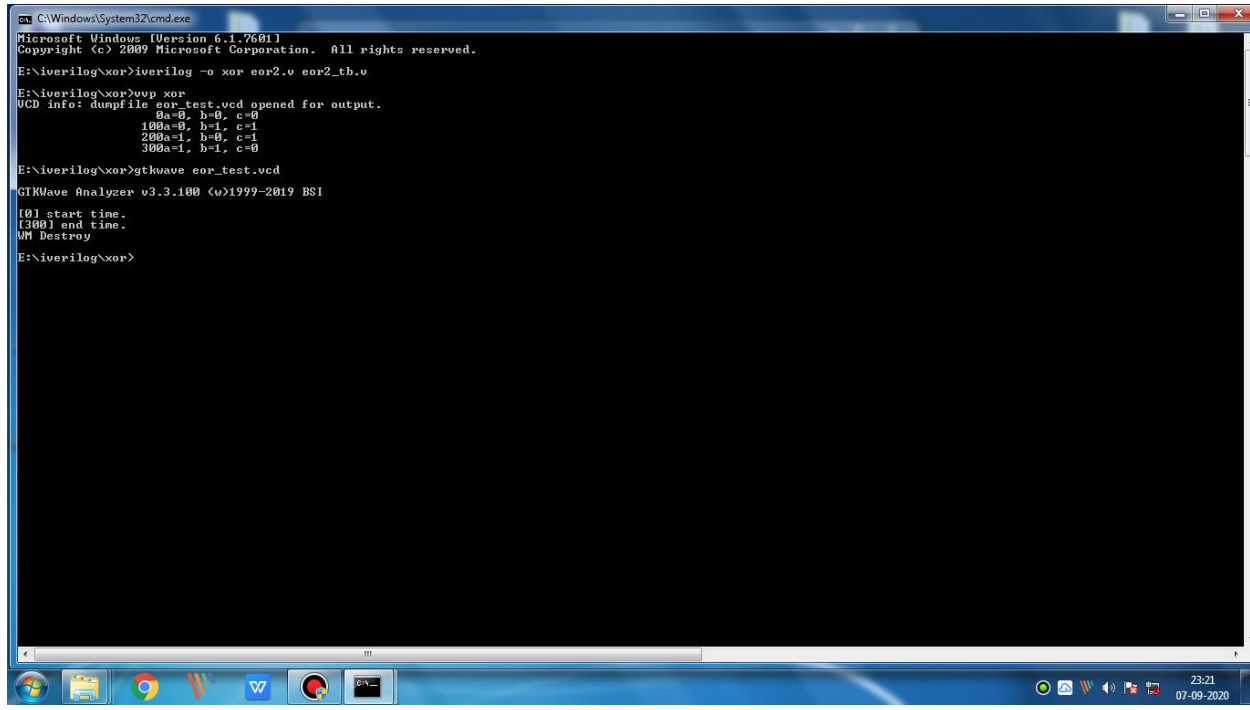
Program:

A screenshot of a Windows desktop environment. A Notepad window titled 'eor2 - Notepad' is open, displaying Verilog code for an EOR gate. The code is as follows:

```
module eor(c, a, b);  
input a,b;  
output c;  
assign c=(a^b);  
endmodule
```

The Notepad window has a standard menu bar with 'File', 'Edit', 'Format', 'View', and 'Help'. The Windows taskbar is visible at the bottom, showing icons for the Start menu, File Explorer, Google Chrome, Microsoft Word, and several other applications. The system tray on the right shows the date and time as '23:21 07-09-2020'.

CMD output:



```
C:\Windows\System32\cmd.exe
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

E:\iverilog\xor>iverilog -o xor_eor2.v eor2_th.v

E:\iverilog\xor>vvp xor
VCD info: dumpfile xor_test.vcd opened for output.
      0a=0, b=0, c=0
     100a=0, b=1, c=1
     200a=1, b=0, c=1
     300a=1, b=1, c=0

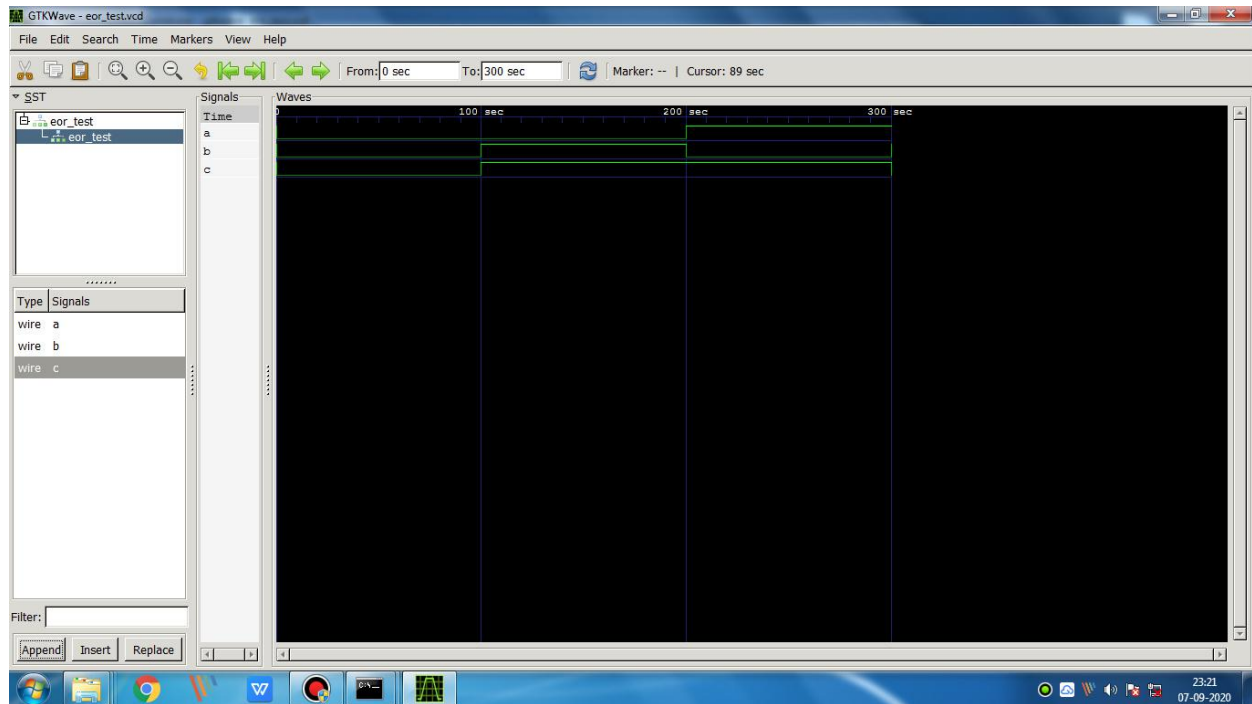
E:\iverilog\xor>gtkwave xor_test.vcd
GTKWave Analyzer v3.3.100 (c)1999-2019 BSI

[0] start time.
[300] end time.
VM Destroy
E:\iverilog\xor>
```

Truth Table:

2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Wave Form:

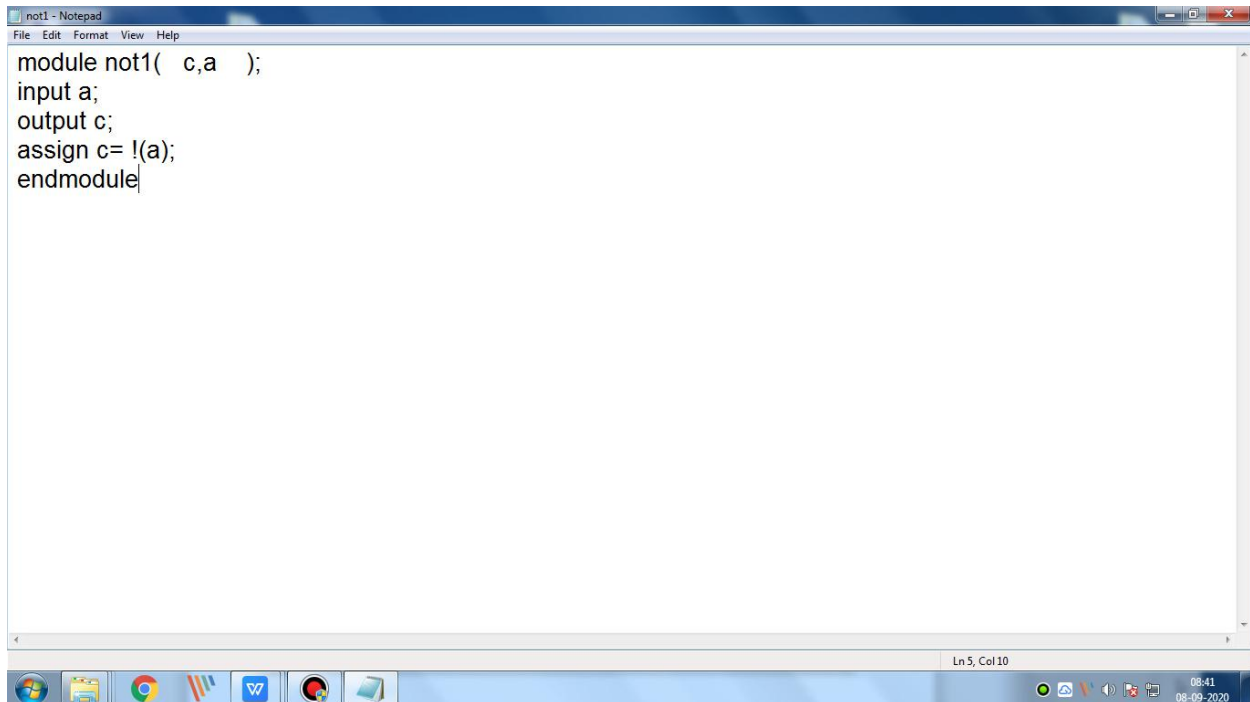


Program #4

Title: NOT gate

Aim: To write Verilog code to mimic NOT gate

Program:

A screenshot of a Windows desktop environment. A Notepad window titled 'not1 - Notepad' is open, displaying Verilog code for a NOT gate. The code is as follows:

```
module not1( c,a );  
input a;  
output c;  
assign c= !(a);  
endmodule
```

The Notepad window has a menu bar with 'File', 'Edit', 'Format', 'View', and 'Help'. The status bar at the bottom of the window indicates 'Ln 5, Col 10'. The Windows taskbar is visible at the bottom, showing icons for the Start menu, File Explorer, Google Chrome, Microsoft Word, and other applications. The system clock in the bottom right corner shows '08:41' and '08-09-2020'.

CMD output:

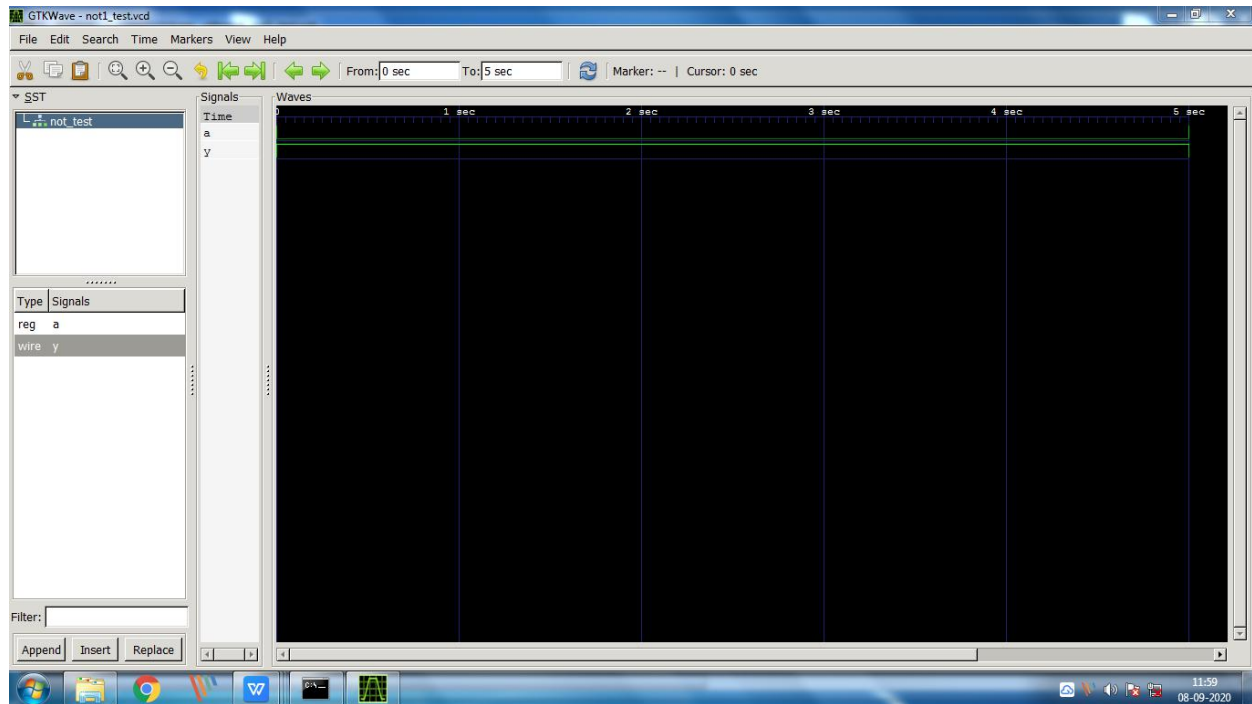
```
C:\Windows\System32\cmd.exe - gtkwave not1_test.vcd
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\DeLL\Desktop\not>iverilog -o not not1.v not1_tb.v
C:\Users\DeLL\Desktop\not>vvp not
VCD info: dumpfile not1_test.vcd opened for output.
          0a=0, y=1
          5a=1, y=0
C:\Users\DeLL\Desktop\not>gtkwave not1_test.vcd
GTKWave Analyzer v3.3.100 (c)1999-2019 BSI
[0] start time.
[5] end time.
```

Truth Table:

NOT gate	
A	\bar{A}
0	1
1	0

Wave form:

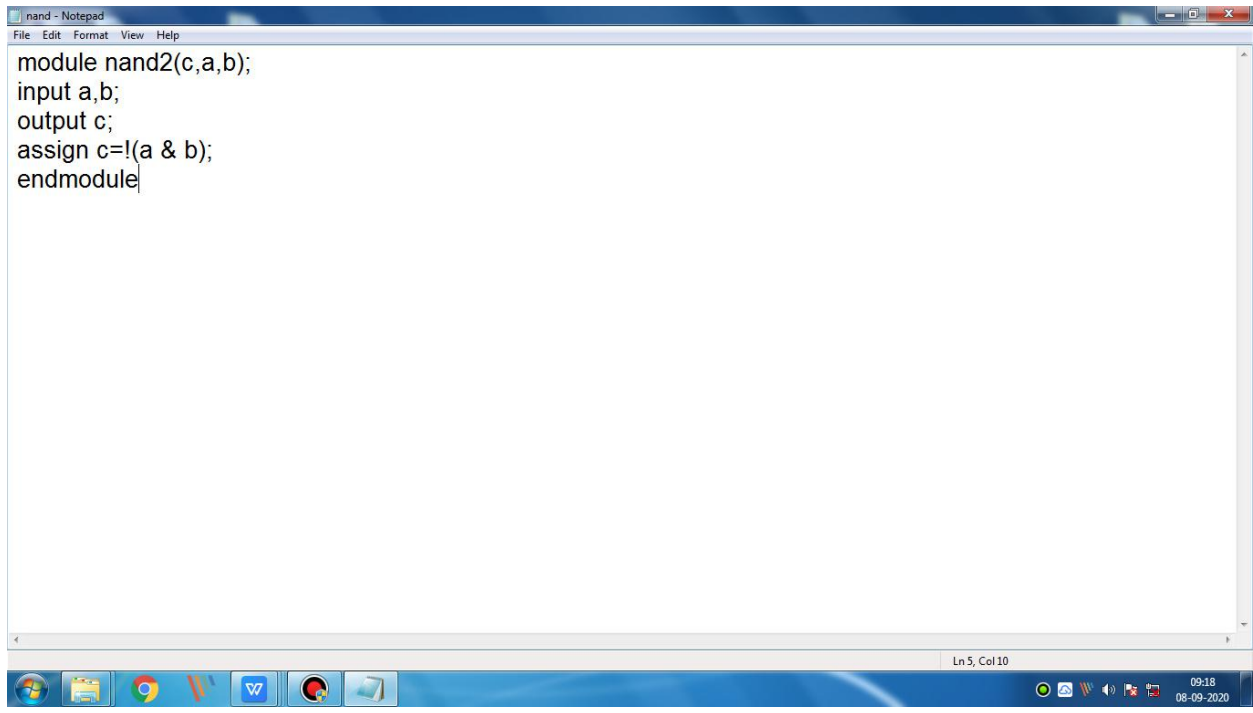


Program #5

Title: NAND gate

Aim: To write a Verilog code to mimic NAND gate

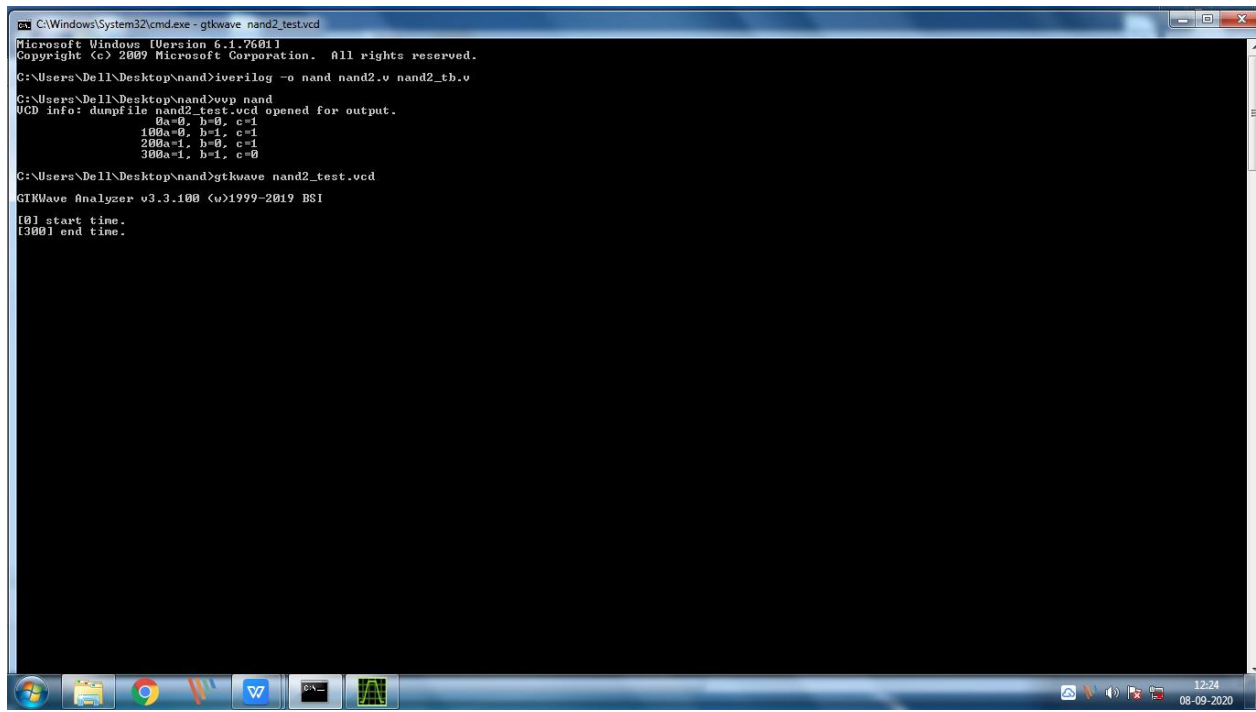
Program:

A screenshot of a Windows desktop environment. A Notepad window titled 'nand - Notepad' is open, displaying Verilog code for a 2-input NAND gate. The code is as follows:

```
module nand2(c,a,b);  
input a,b;  
output c;  
assign c=! (a & b);  
endmodule
```

The Notepad window has a menu bar with 'File', 'Edit', 'Format', 'View', and 'Help'. The status bar at the bottom of the window shows 'Ln 5, Col 10'. The Windows taskbar is visible at the bottom of the screen, showing icons for the Start menu, File Explorer, Google Chrome, Microsoft Word, and a terminal. The system tray on the right shows the date and time as '09:18 08-09-2020'.

CMD output:



```
C:\Windows\System32\cmd.exe - gtkwave nand2_test.vcd
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\De11\Desktop\nand>iverilog -o nand nand2.v nand2_tb.v
C:\Users\De11\Desktop\nand>vvp nand
VCD info: dumpfile nand2_test.vcd opened for output.
          0a=0, b=0, c=1
        100a=0, b=1, c=1
        200a=1, b=0, c=1
        300a=1, b=1, c=0

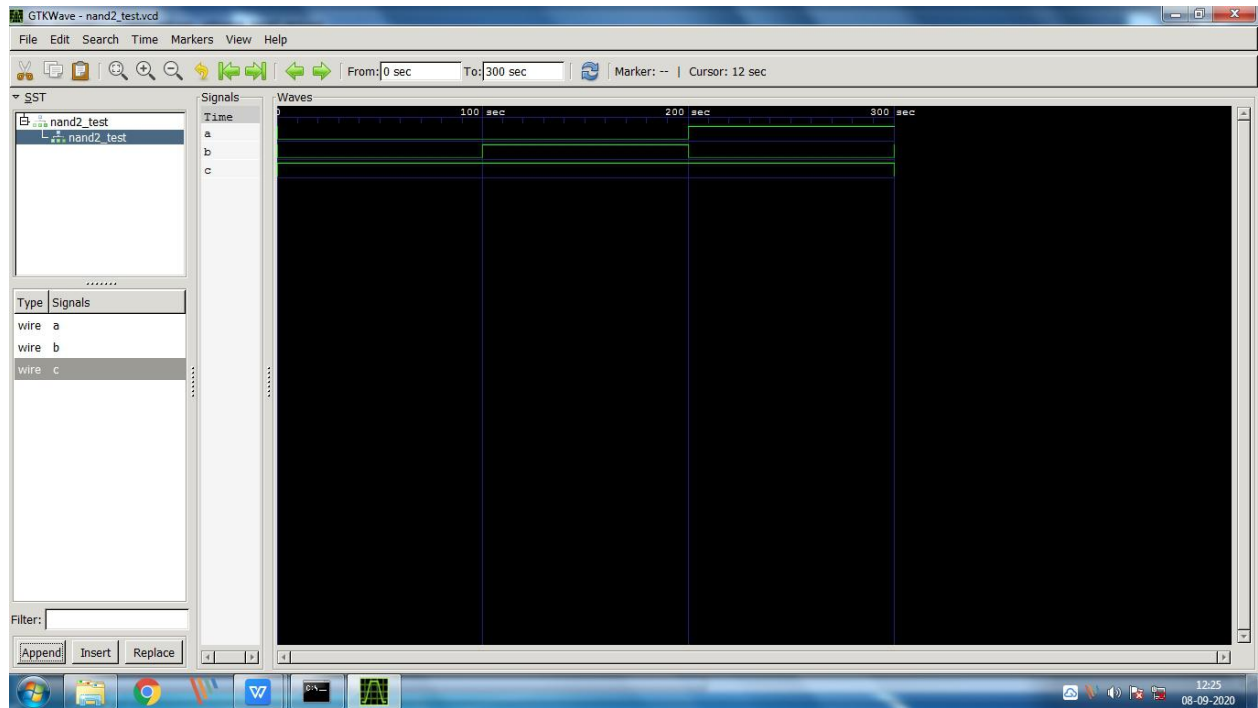
C:\Users\De11\Desktop\nand>gtkwave nand2_test.vcd
GTKWave Analyzer v3.3.100 (c)1999-2019 BS1

[0] start time.
[300] end time.
```

Truth Table:

2 Input NAND gate		
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Wave Form :

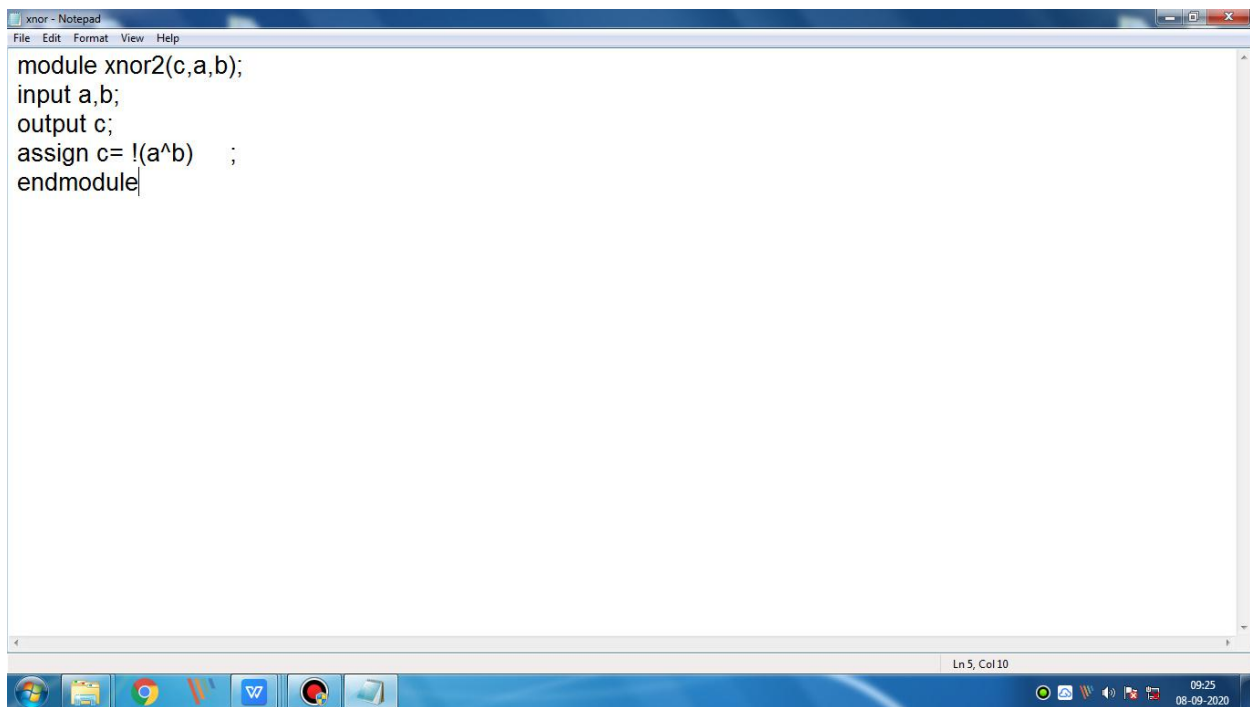


Program #7

Title: XNOR Gate

Aim: To write a Verilog code to mimic XNOR gate

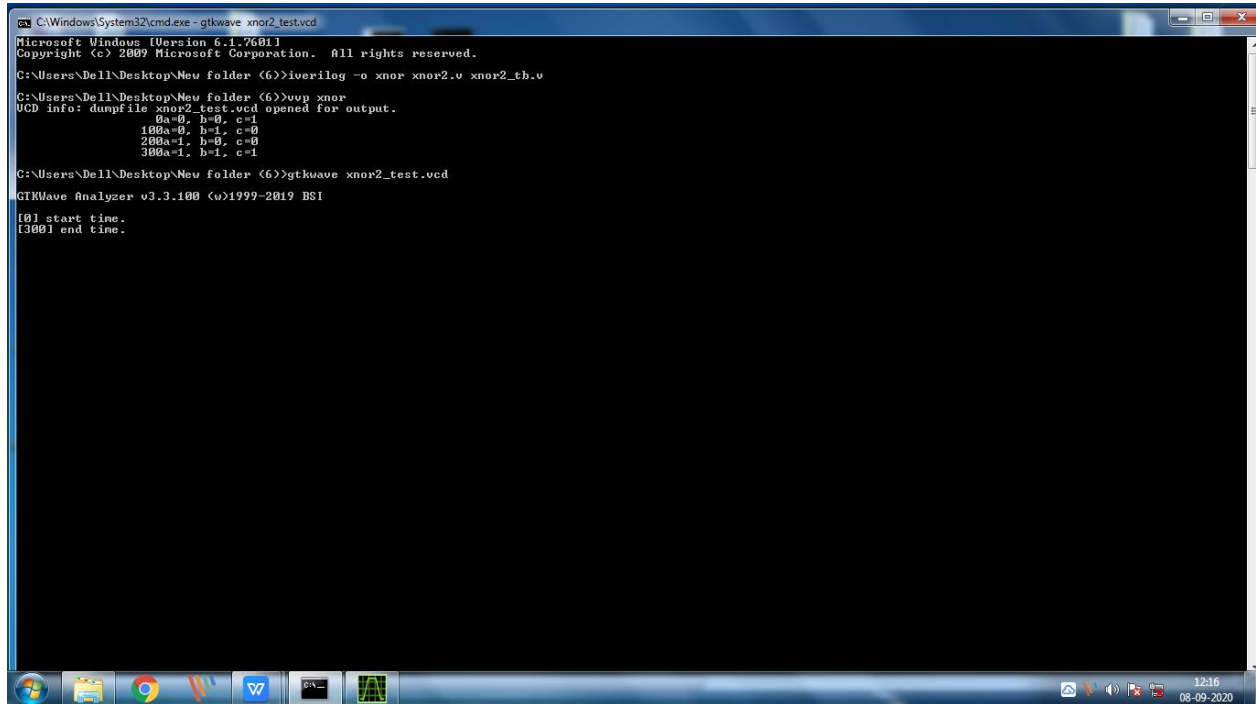
Program:

A screenshot of a Windows Notepad application window titled 'xnor - Notepad'. The window contains Verilog code for an XNOR gate. The code is as follows:

```
module xnor2(c,a,b);  
input a,b;  
output c;  
assign c=!(a^b) ;  
endmodule
```

The status bar at the bottom of the Notepad window indicates 'Ln 5, Col 10'. The Windows taskbar is visible at the bottom of the screen, showing various application icons and the system clock displaying '09:25 08-09-2020'.

CMD output:



```
C:\Windows\System32\cmd.exe - gtkwave xnor2_test.vcd
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\Dell\Desktop\New folder (6)>iverilog -o xnor xnor2.v xnor2_tb.v

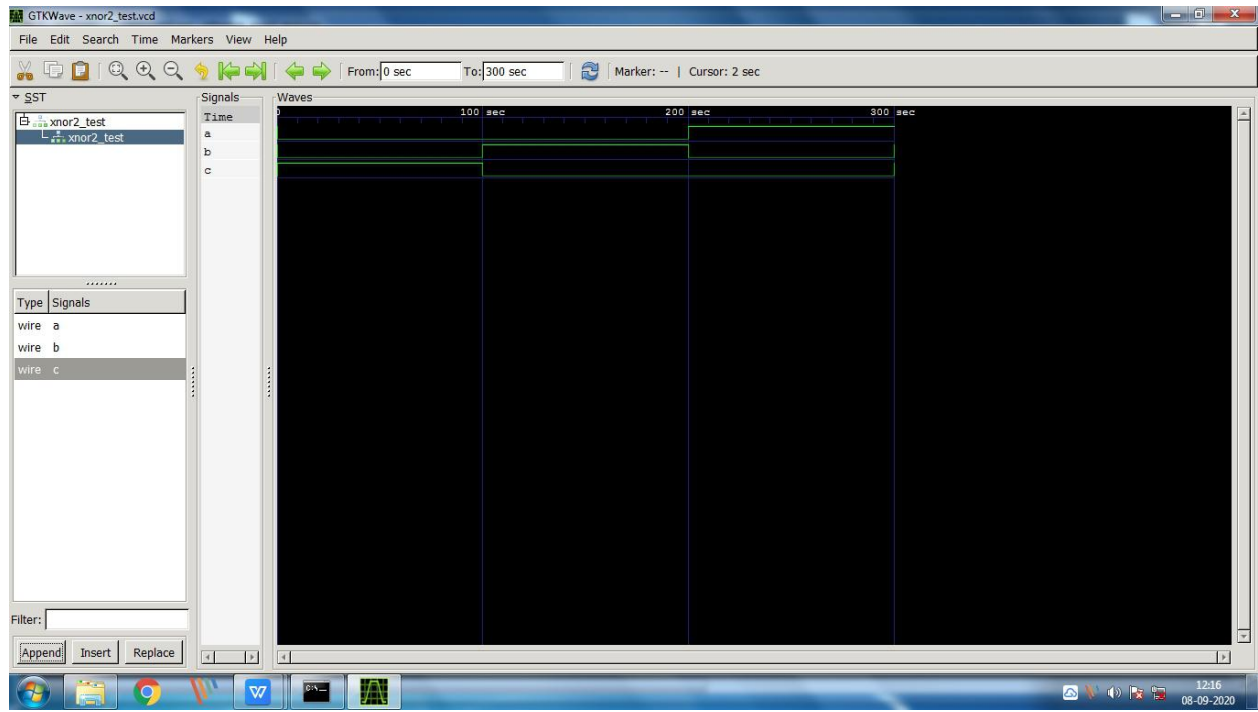
C:\Users\Dell\Desktop\New folder (6)>vvp xnor
VCD info: dumpfile xnor2_test.vcd opened for output.
      0a=0, b=0, c=1
     100a=0, b=1, c=0
     200a=1, b=0, c=0
     300a=1, b=1, c=1

C:\Users\Dell\Desktop\New folder (6)>gtkwave xnor2_test.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[300] end time.
```

Truth Table:

Inputs		Outputs
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

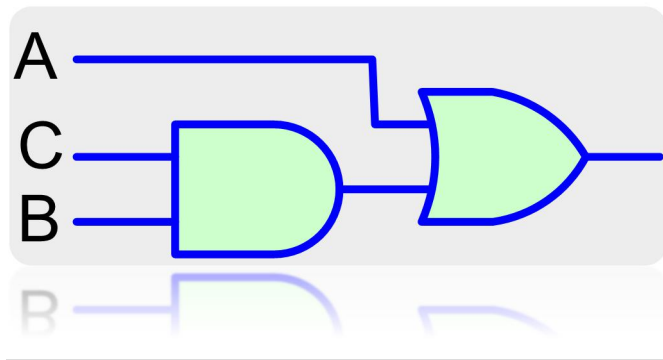
Wave Form:



Program #8

Title: Circuit 1

Aim: To achieve the below shown circuit



Program:

```
simple_circuit - Notepad
File Edit Format View Help
module simple_circuit(A,B,C,Y);
input A,B,C;
output Y;
wire w1;
assign w1 = C&B;
assign Y= A|w1 ;
endmodule
Ln1, Col1
08:53
08-09-2020
```

CMD output:

```
C:\Windows\System32\cmd.exe - gtwave circuit1.vcd
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

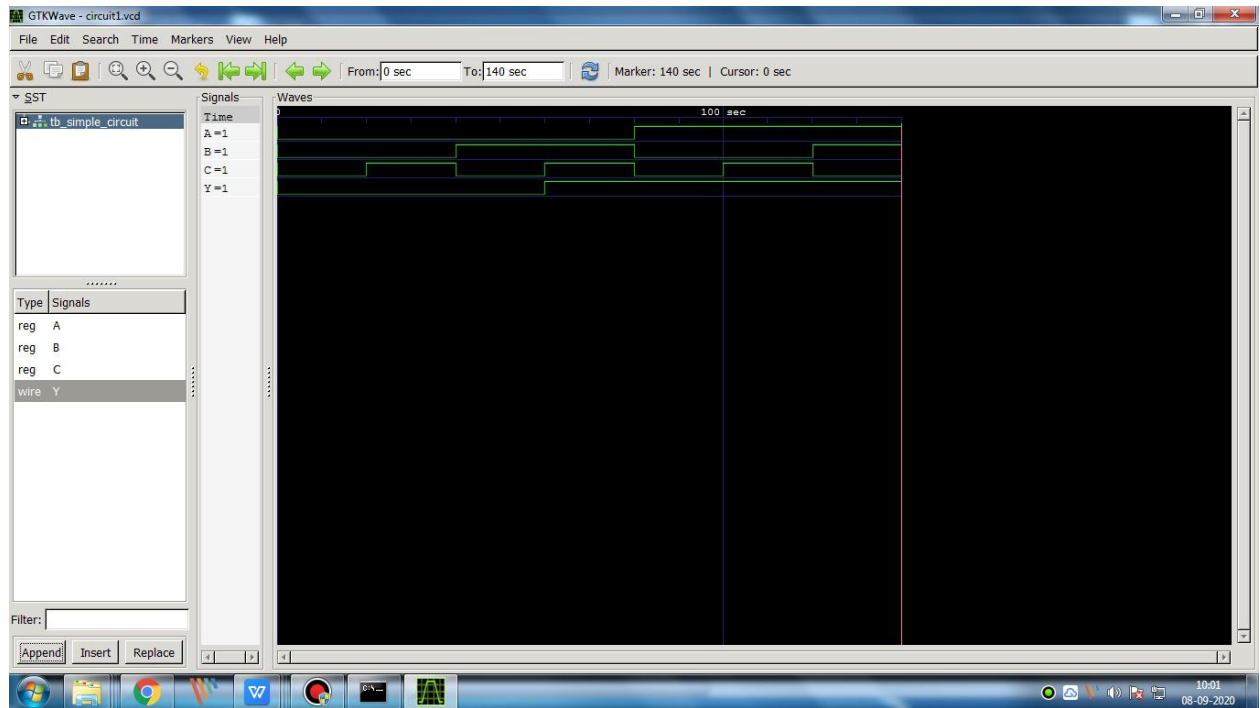
C:\Users\Dell\Desktop\New folder <3>>iverilog -o circuit1 circuit1.v circuit1.tb.v
C:\Users\Dell\Desktop\New folder <3>>vvp circuit1
VCD info: dumpfile circuit1.vcd opened for output.
      0ns-0, B=0, C=0,V=0
     200ns-0, B=0, C=1,V=0
     400ns-0, B=1, C=0,V=0
     600ns-0, B=1, C=1,V=1
     800ns-1, B=0, C=0,V=1
    1000ns-1, B=0, C=1,V=1
    1200ns-1, B=1, C=0,V=1
    1400ns-1, B=1, C=1,V=1

C:\Users\Dell\Desktop\New folder <3>>gtkwave circuit1.vcd
GTKWave Analyzer v3.3.100 (w)1999-2019 BSI
[0] start time.
[140] end time.
```

Truth Table:

A	B	Y
0	0	0
0	1	0
0	0	0
0	1	1
1	0	1
1	1	1
1	0	1
1	1	1

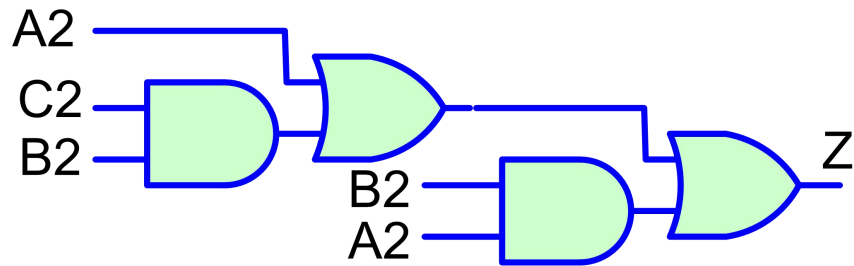
Wave Form:



Program #9

Title: Circuit 2

Aim: To achieve the below shown circuit



Program:

```
module simple_circuit( A2,B2,C2,Y );
output Y;
input A2,B2,C2;
wire w1,w2,w3;
assign w1= ( C2 & B2 );
assign w2= ( A2 | w1 );
assign w3= ( B2 & A2 );
assign Y= ( w3 | w2 );
endmodule
```

CMD output:

```
C:\Windows\System32\cmd.exe - gtwave circuit2.vcd
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\Users\De11\Desktop\circuit 2>iverilog -o circuit2 circuit2.v circuit2_th.v

C:\Users\De11\Desktop\circuit 2>vvp circuit2
VCD info: dumpfile circuit2.vcd opened for output.
      0002=0, B2=0, C2=0.V=0
      2002=0, B2=0, C2=1.V=0
      4002=0, B2=1, C2=0.V=0
      6002=0, B2=1, C2=1.V=1
      8002=1, B2=0, C2=0.V=1
      10002=1, B2=0, C2=1.V=1
      12002=1, B2=1, C2=0.V=1
      14002=1, B2=1, C2=1.V=1

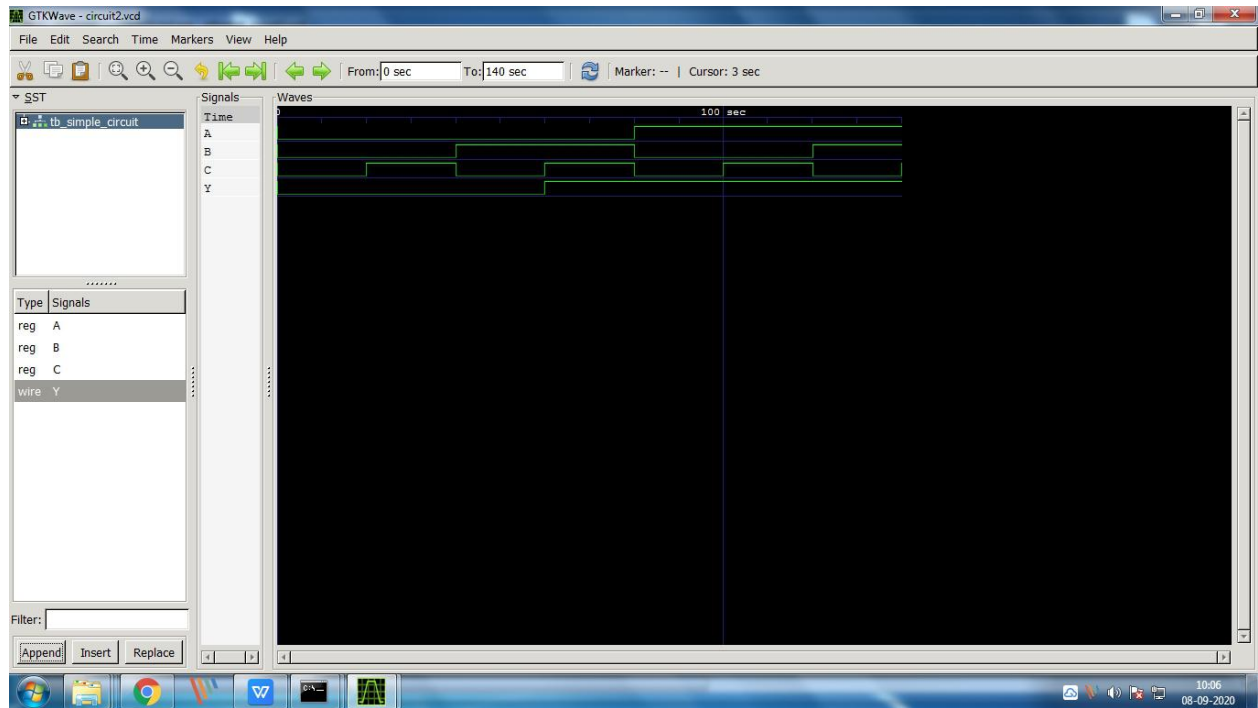
C:\Users\De11\Desktop\circuit 2>gtwawe circuit2.vcd
GTKWave Analyzer v3.3.100 (v)1999-2019 BSI

[0] start time.
[140] end time.
```

Truth Table:

A	B	Y
0	0	0
0	1	0
0	0	0
0	1	1
1	0	1
1	1	1
1	0	1
1	1	1

Wave Form:



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: suhan.b.revankar

Name: Suhan.B.Revankar

SRN: PES2UG19CS412

Section: G

Date: 08/09/2020