Digital Design and Computer Organization Laboratory

UE19CS206

3rd Semester, Academic Year 2020-21

Date : 08/09/2020

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Experiment number #1

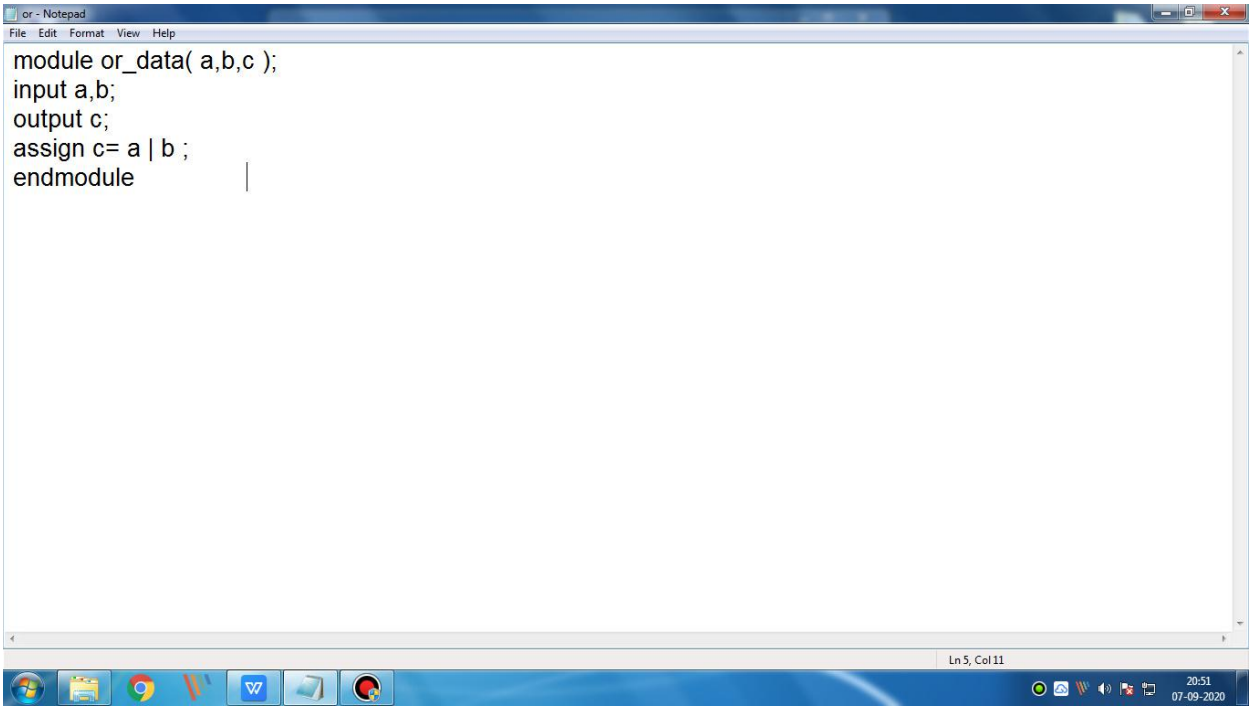
Week #1

Program #1

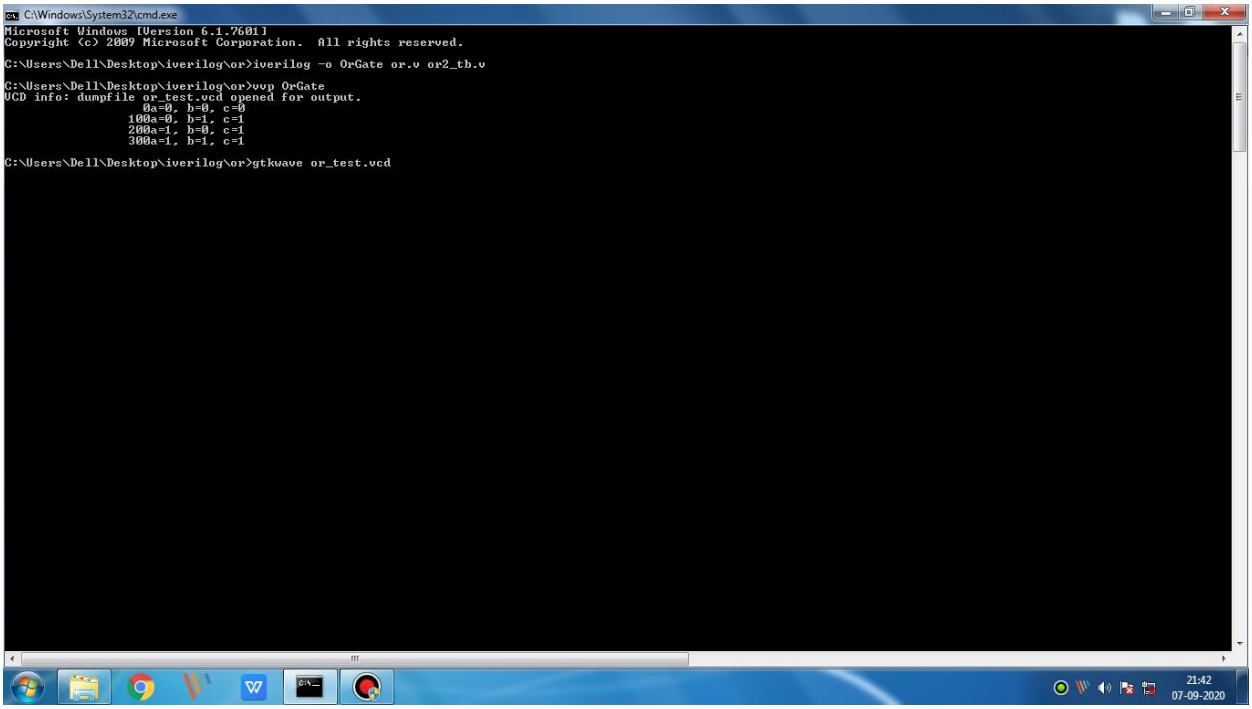
Title: OR gate

Aim: To write Verilog code to mimic OR gate

Program :



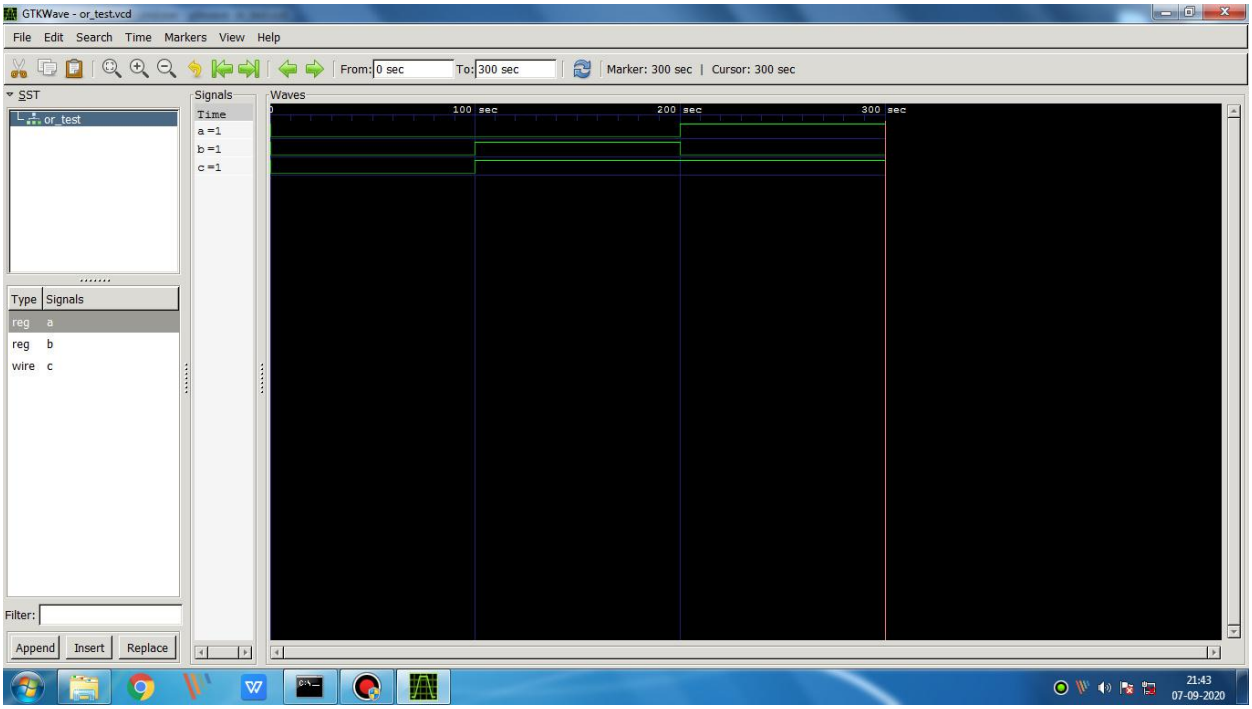
Command Prompt Output:



Truth Table :

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Wave Form :

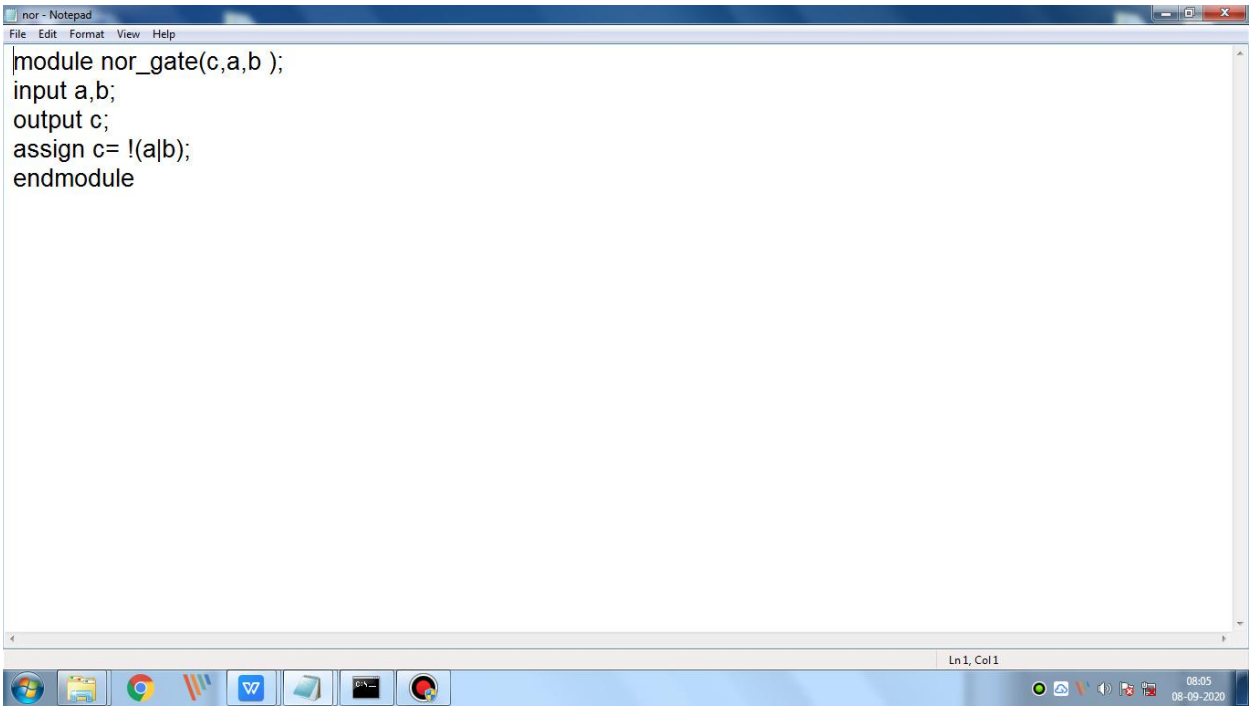

GTKWave - or_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 sec
Marker: 300 sec | Cursor: 300 sec
SST
or_test
Signals
Time
a =1
b =1
c =1
Waves
100 sec
200 sec
300 sec
Type Signals
reg a
reg b
wire c
Filter:
Append
Insert
Replace
21:43
07-09-2020

Program #2

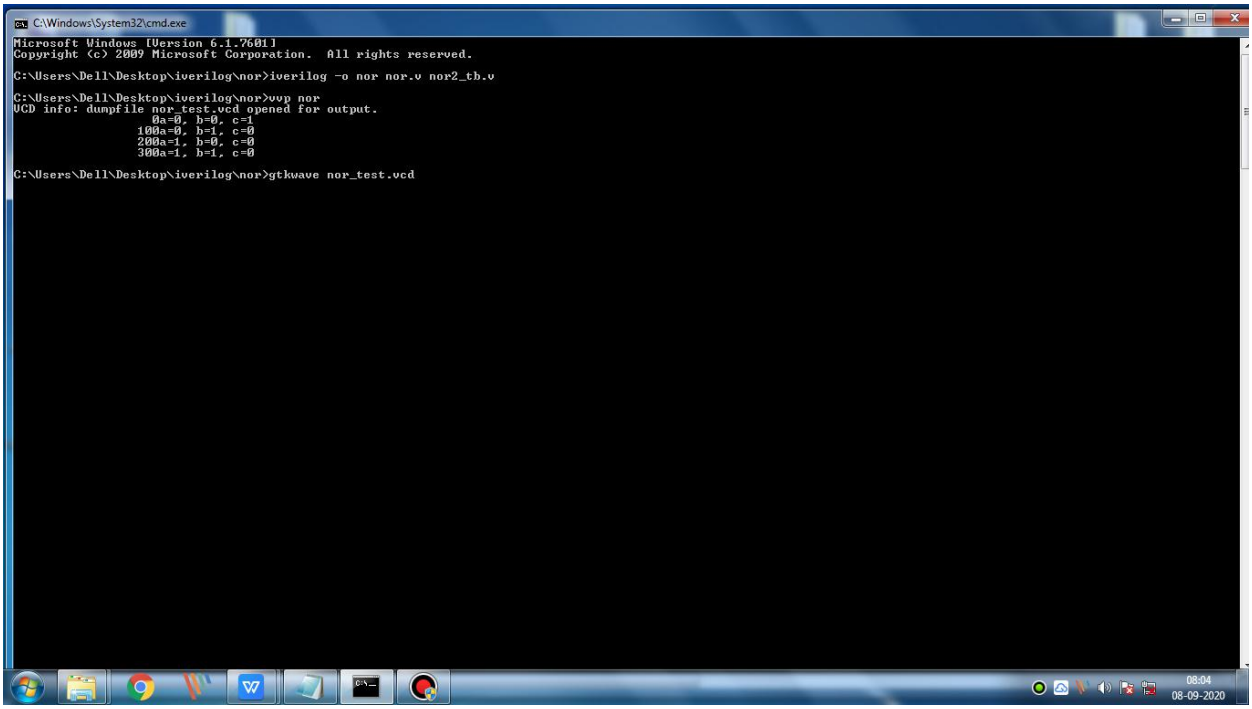
Title: NOR gate

Aim: To write Verilog code to mimic NOR gate

Program:



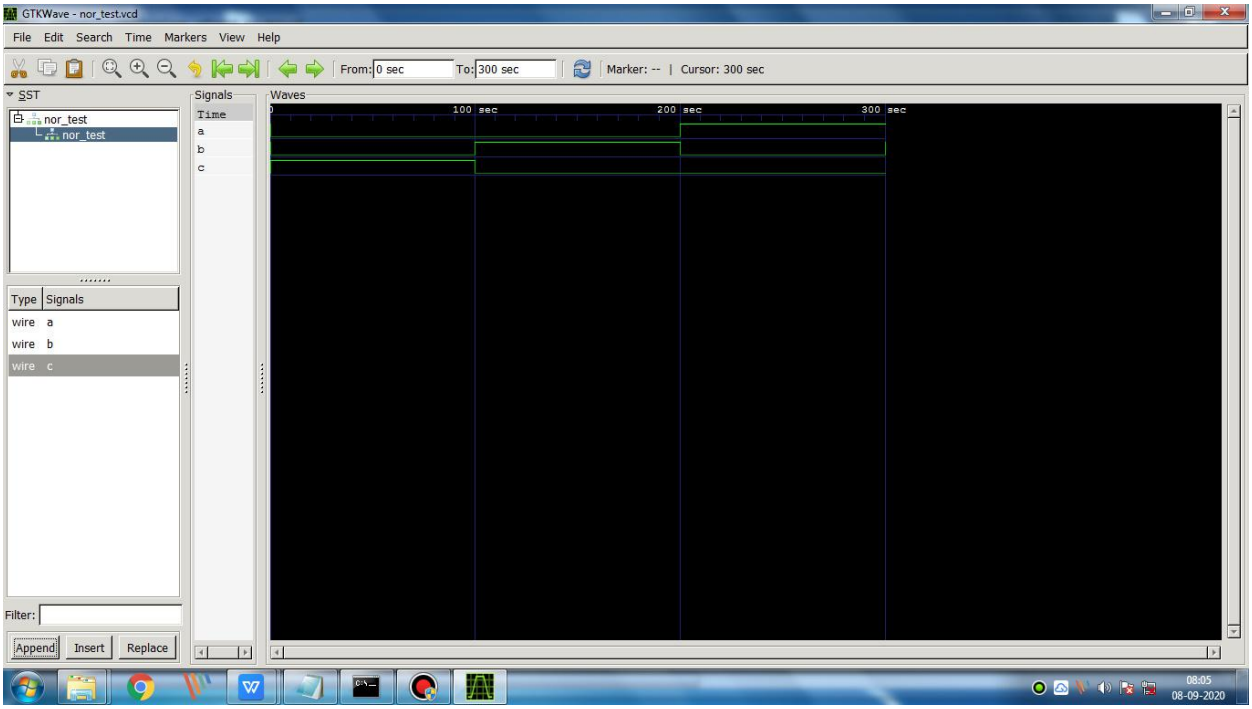
CMD output:



Truth Table:

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Wave Form:

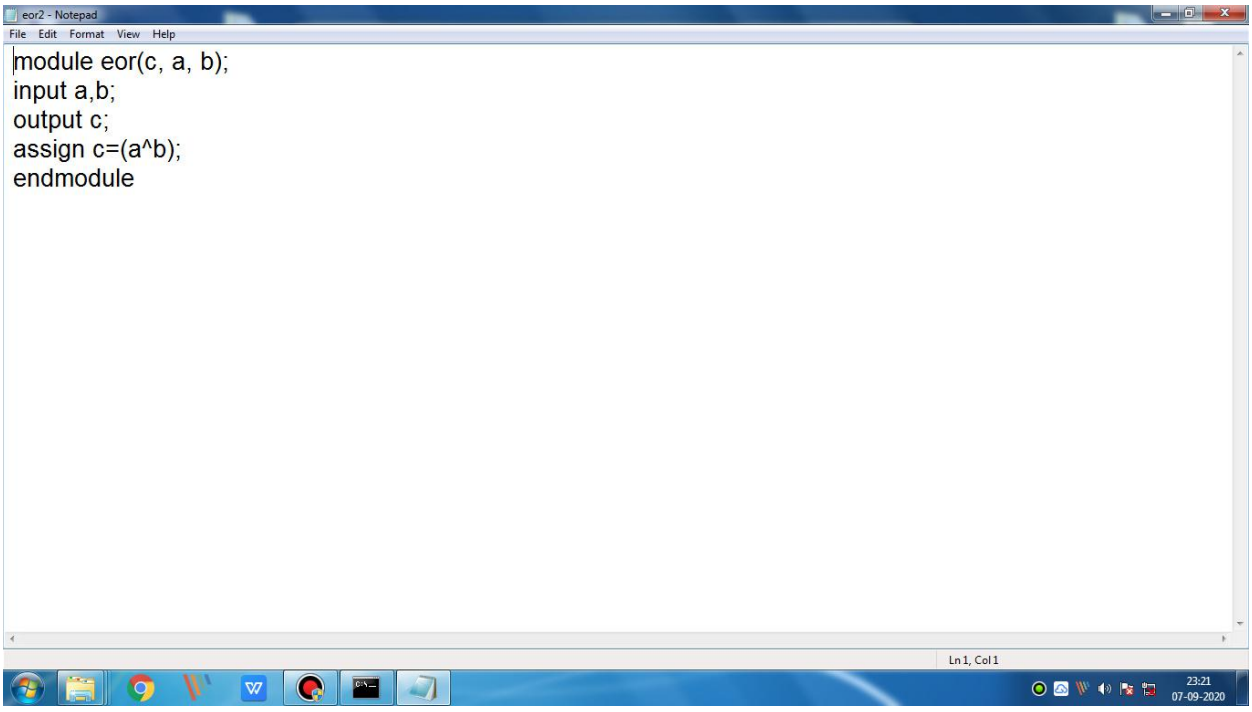

GTKWave - nor_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 sec
Marker: --
Cursor: 300 sec
SST
nor_test
nor_test
Type Signals
wire a
wire b
wire c
Filter:
Append
Insert
Replace
Signals
Time
a
b
c
Waves
100 sec
200 sec
300 sec
08:05
08-09-2020

Program #3

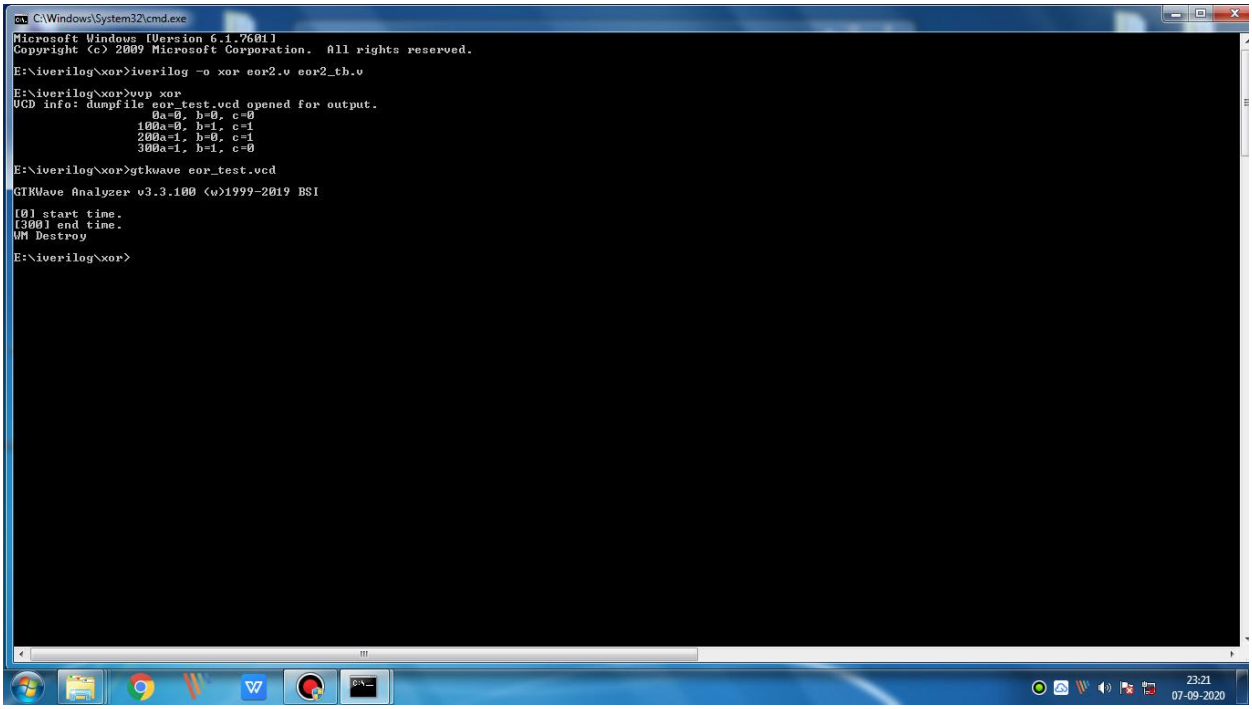
Title: EOR gate

Aim: To write Verilog code to mimic EOR gate

Program:



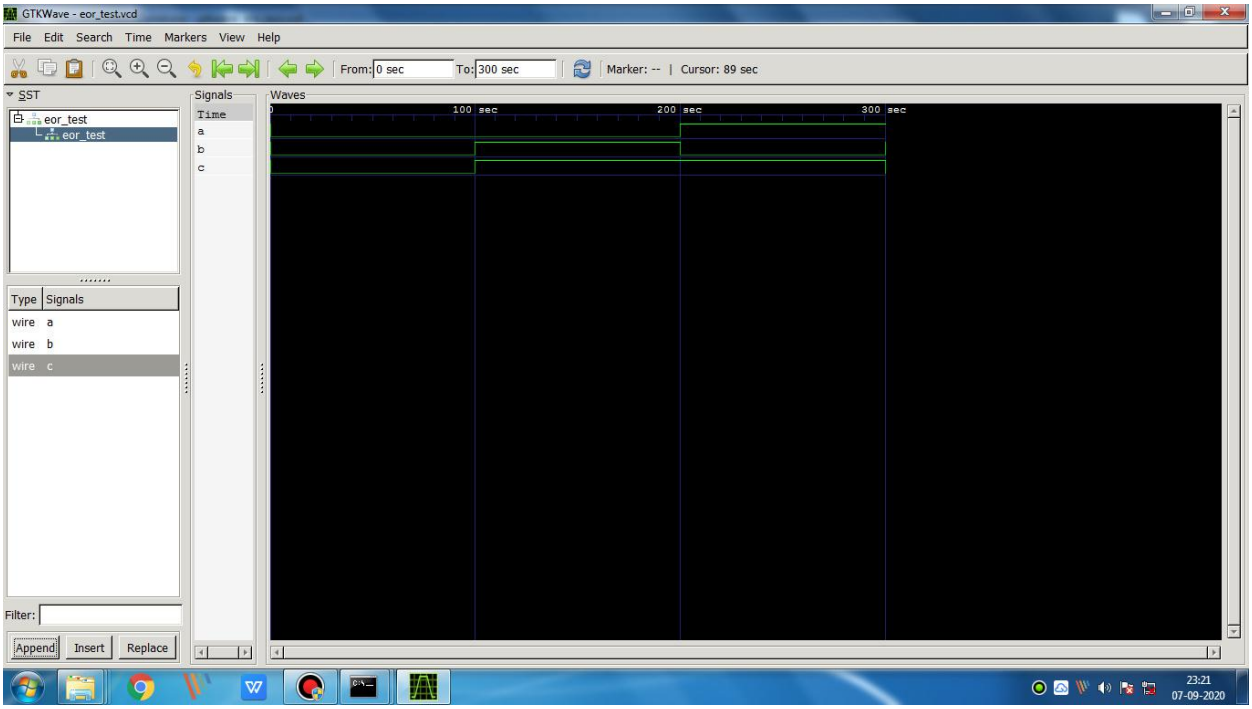
CMD output:



Truth Table:

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Wave Form:

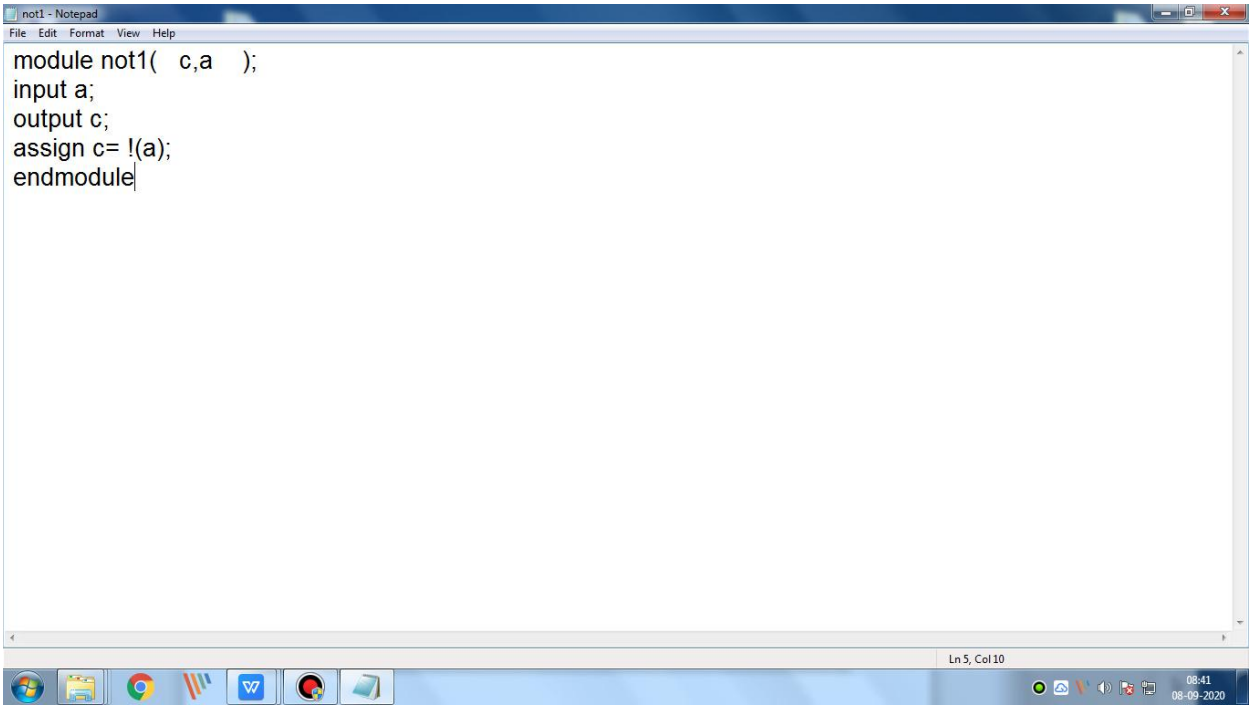

GTKWave - eor_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 sec
Marker: --
Cursor: 89 sec
SST
eor_test
eor_test
Signals
Time
a
b
c
Waves
100 sec
200 sec
300 sec
Type Signals
wire a
wire b
wire c
Filter:
Append
Insert
Replace
23:21
07-09-2020

Program #4

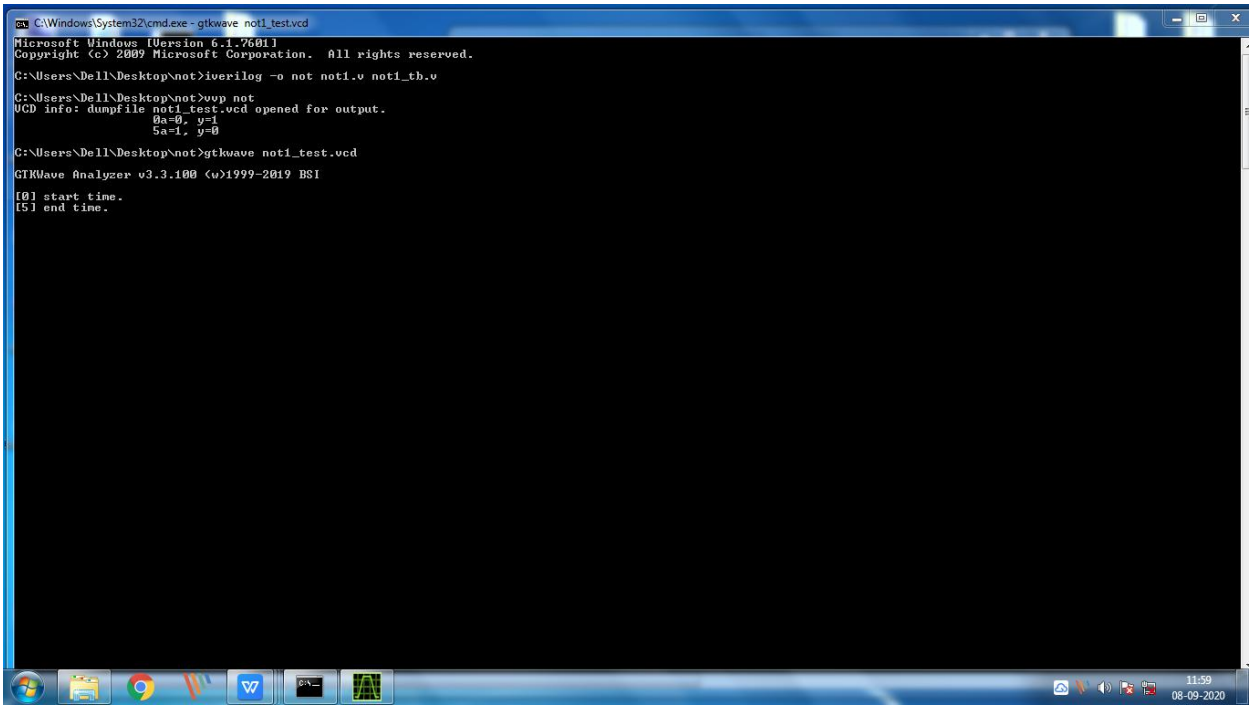
Title: NOT gate

Aim: To write Verilog code to mimic NOT gate

Program:



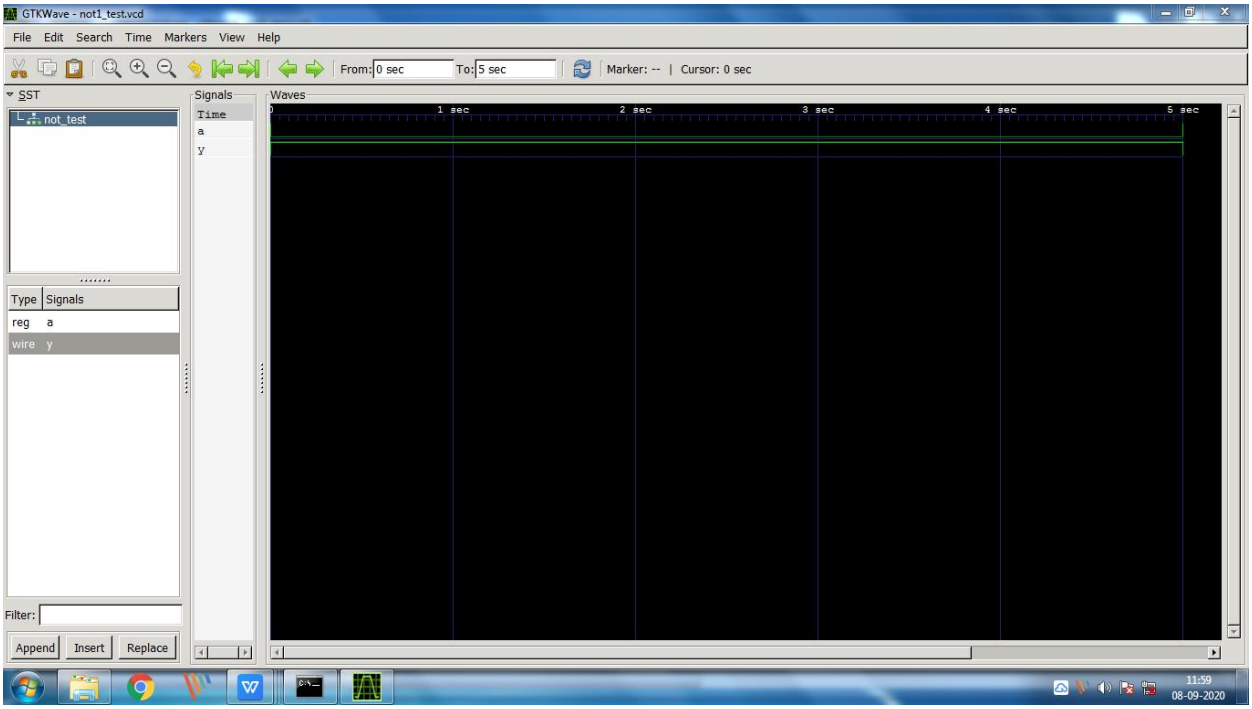
CMD output:



Truth Table:

NOT gate	
A	$\overline{A}$
0	1
1	0

Wave form:

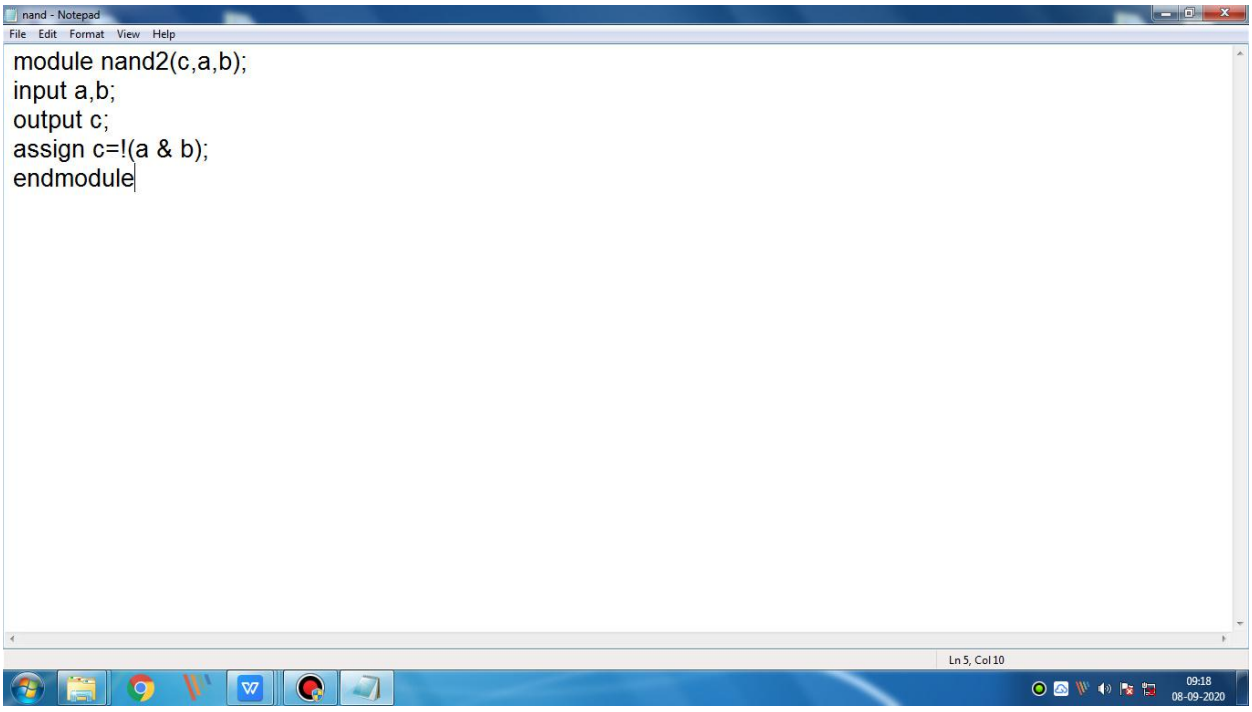

GTKWave - not1_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 5 sec
Marker: --
Cursor: 0 sec
SST
not_test
Signals
Time
a
y
Waves
1 sec
2 sec
3 sec
4 sec
5 sec
Type Signals
reg a
wire y
Filter:
Append
Insert
Replace
11:59
08-09-2020

Program #5

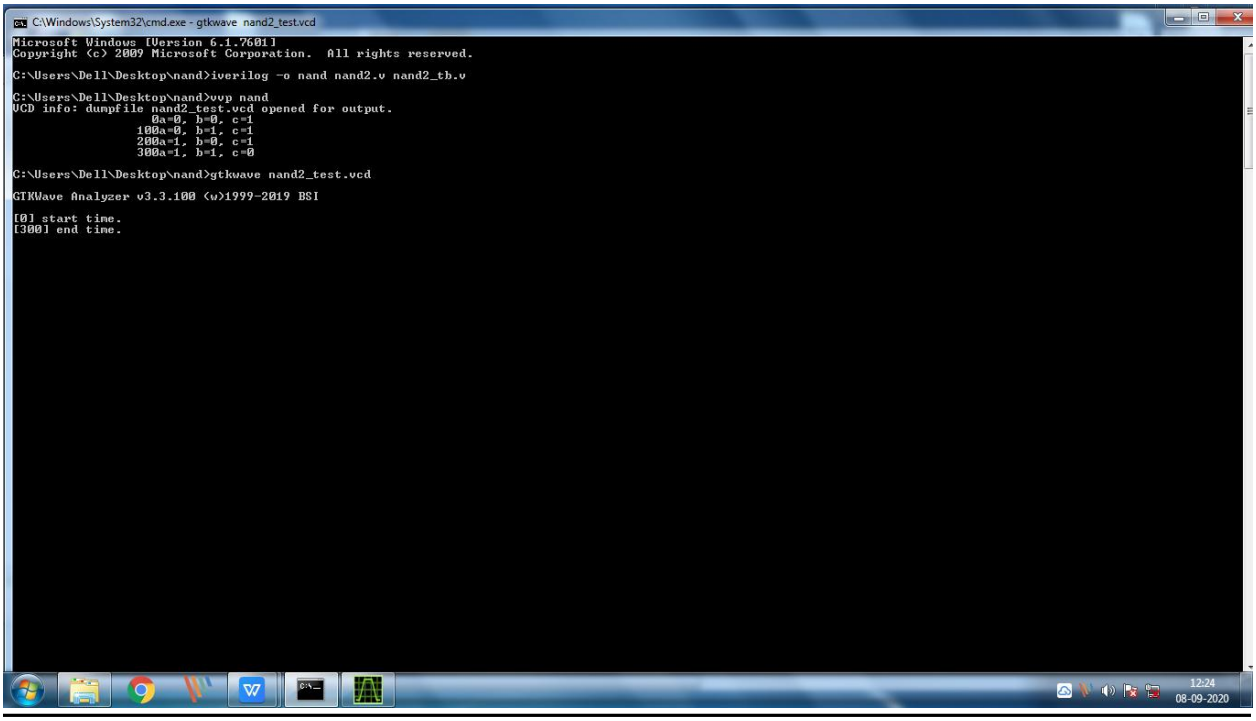
Title: NAND gate

Aim: To write a Verilog code to mimic NAND gate

Program:



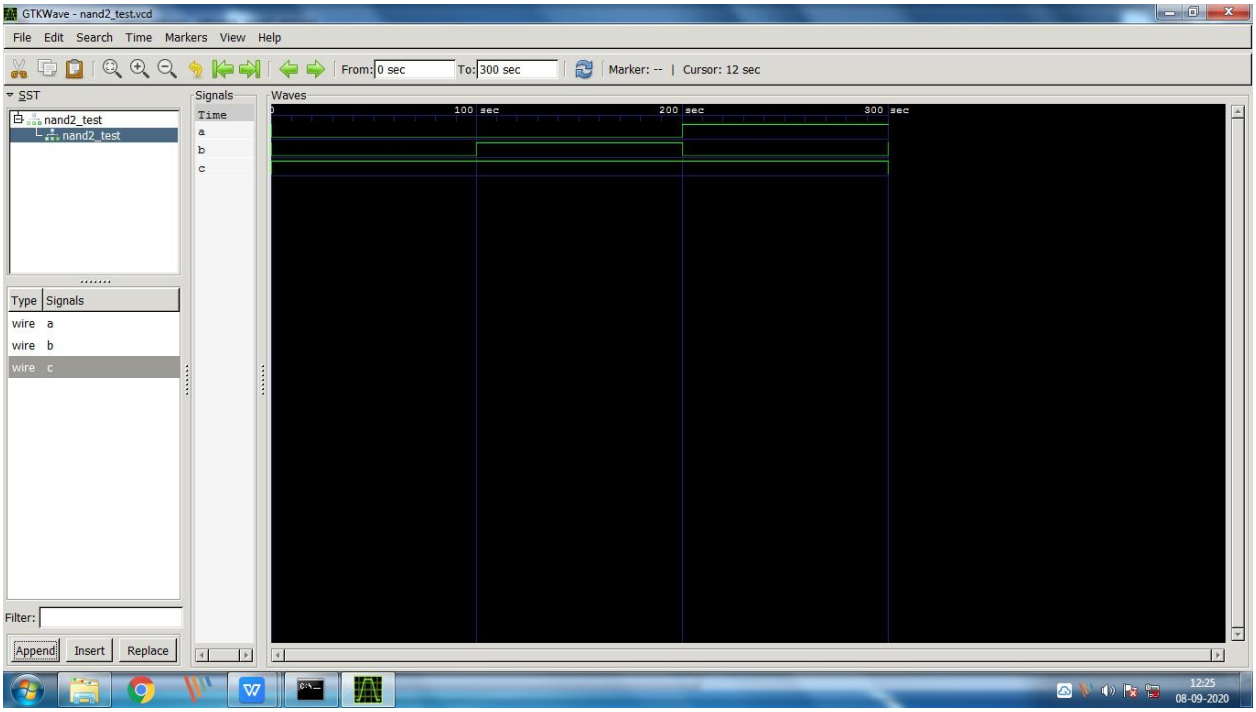
CMD output:



Truth Table:

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

Wave Form :

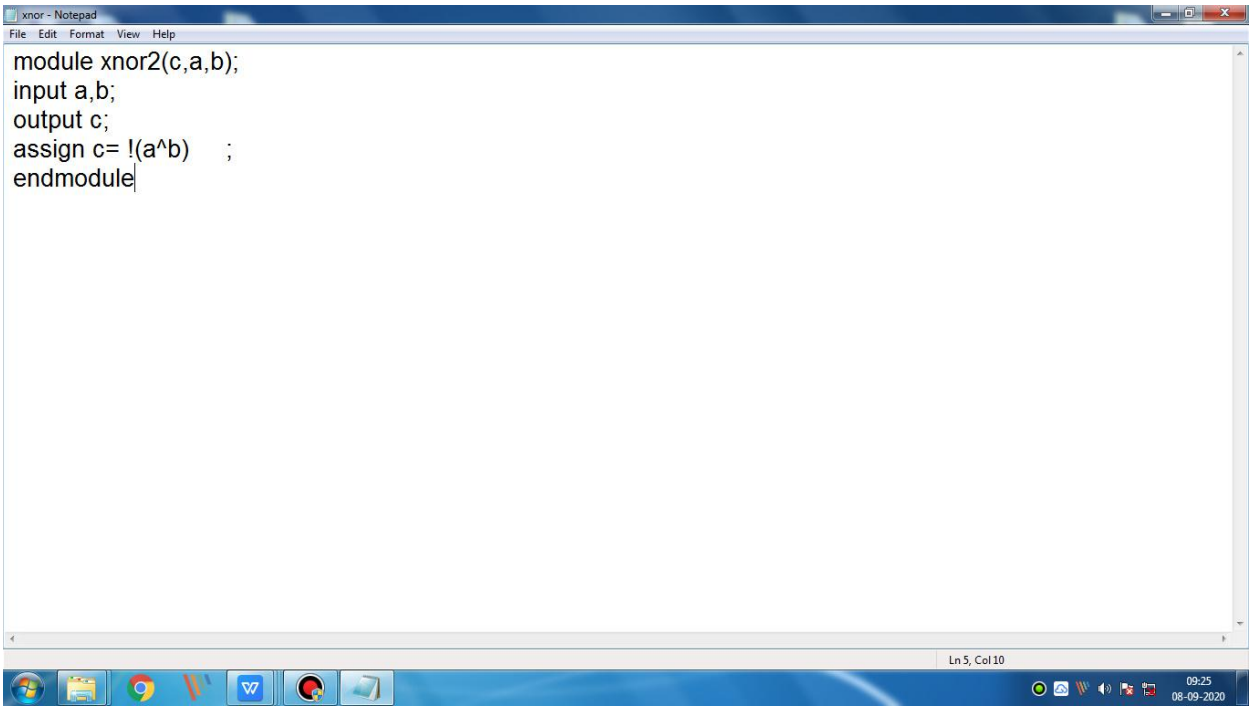

GTKWave - nand2_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 sec
Marker: --
Cursor: 12 sec
SST
nand2_test
nand2_test
Signals
Time
a
b
c
Waves
100 sec
200 sec
300 sec
Type Signals
wire a
wire b
wire c
Filter:
Append
Insert
Replace
12:25
08-09-2020

Program #7

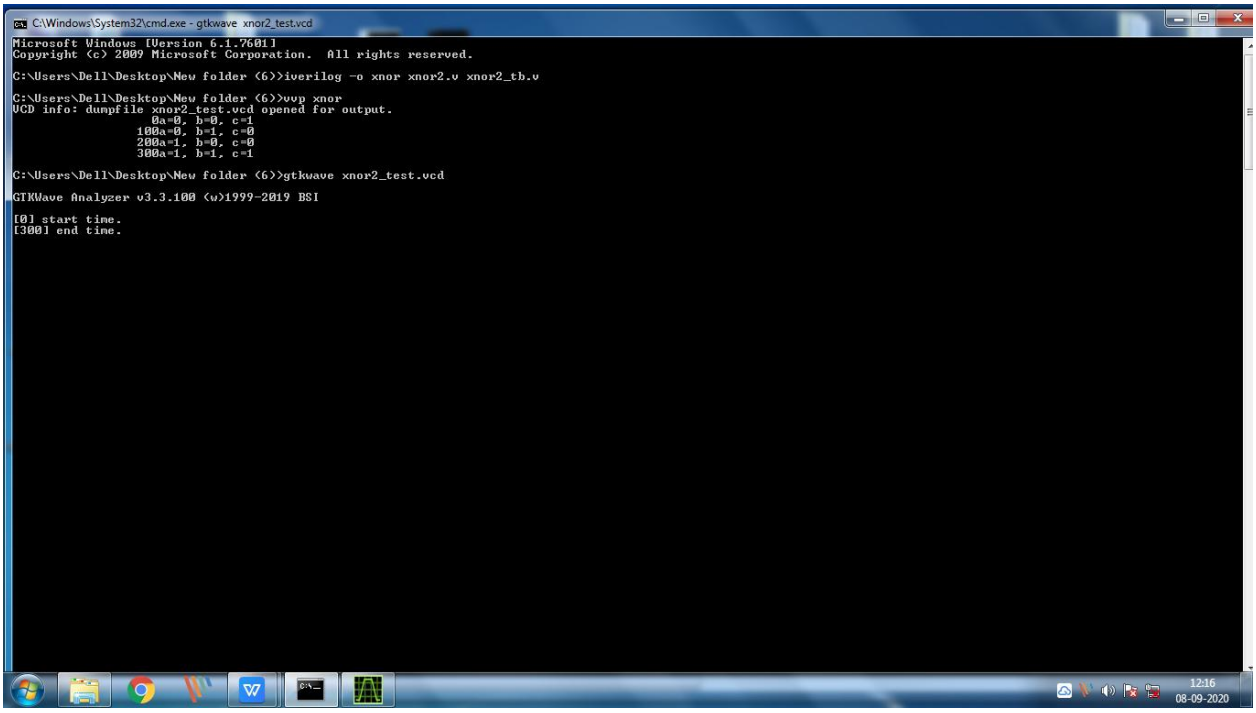
Title: XNOR Gate

Aim: To write a Verilog code to mimic XNOR gate

Program:



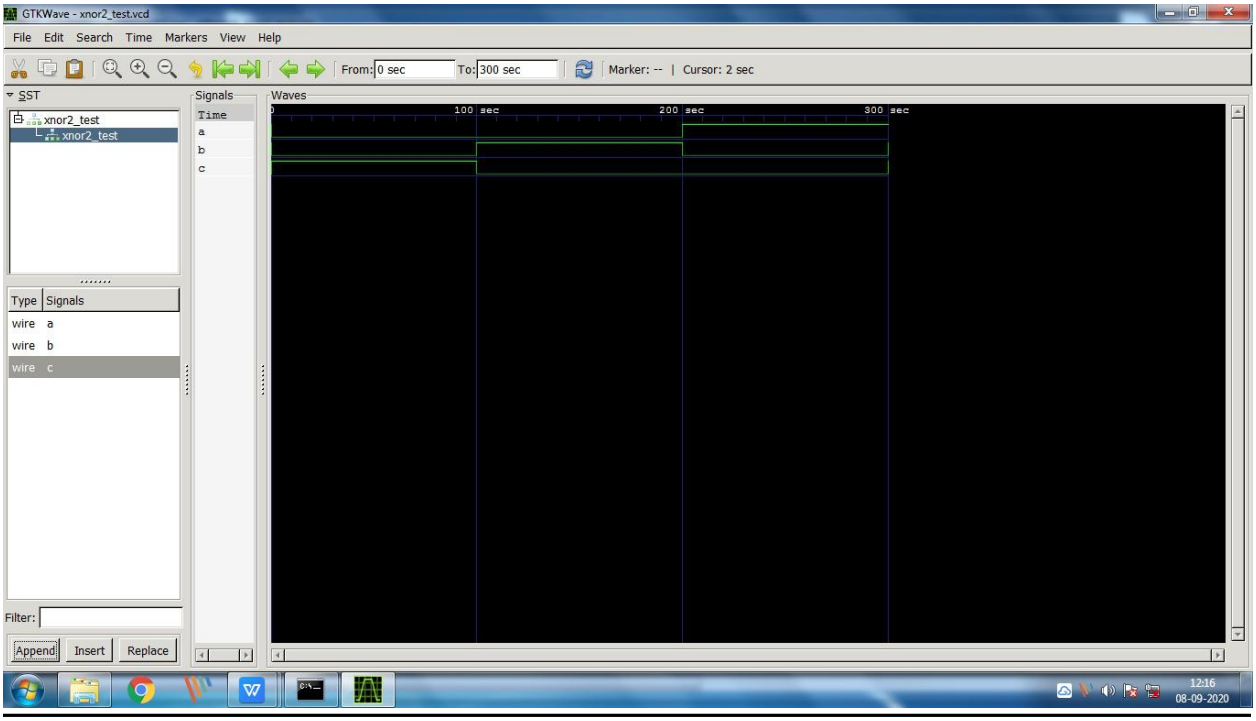
CMD output:



Truth Table:

Inputs		Outputs
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

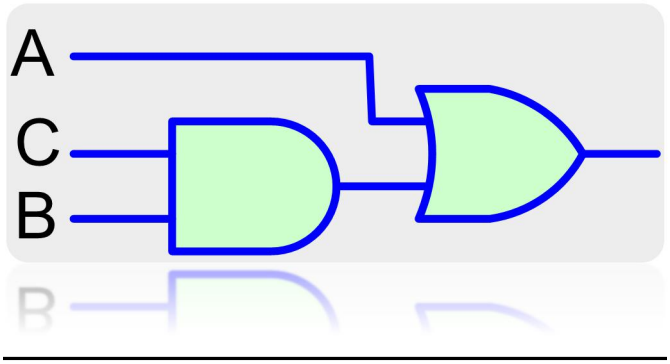
Wave Form:


GTKWave - xnor2_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 300 sec
Marker: --
Cursor: 2 sec
SST
xnor2_test
xnor2_test
Type Signals
wire a
wire b
wire c
Filter:
Append
Insert
Replace
Signals
Time
a
b
c
Waves
100 sec
200 sec
300 sec
12:16
08-09-2020

Program #8

Title: Circuit 1

Aim: To achieve the below shown circuit



Program:

simple_circuit - Notepad

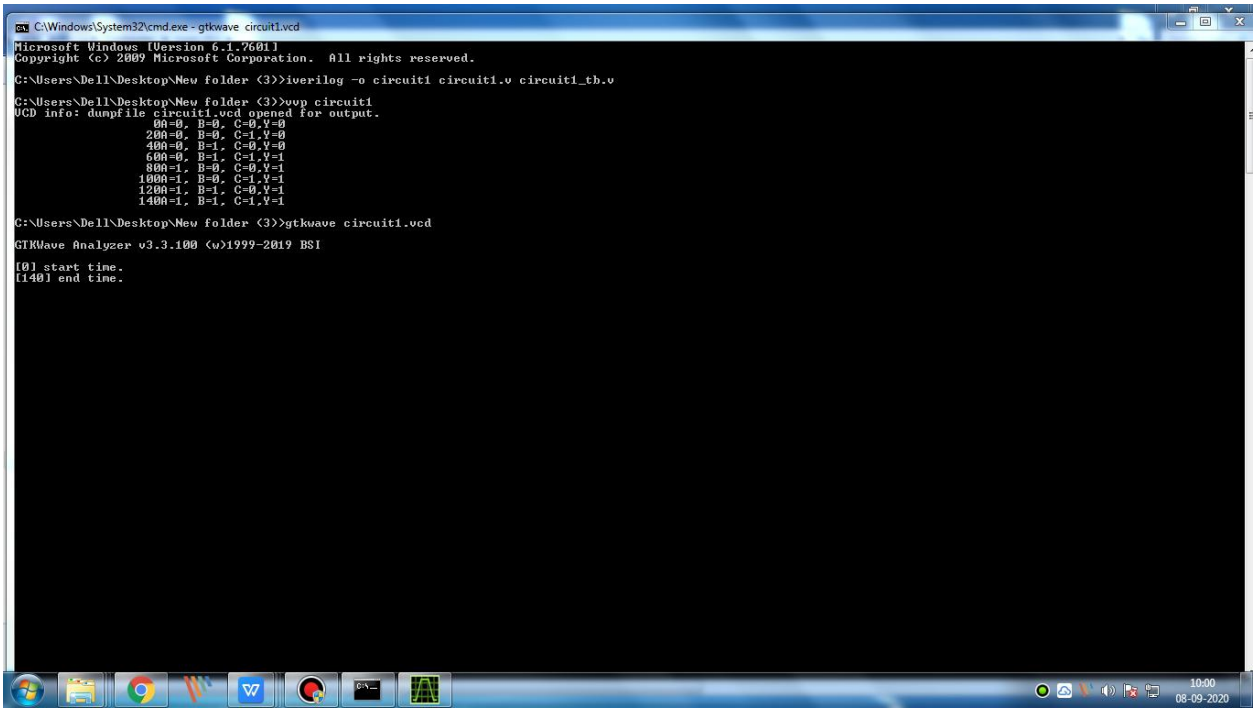
File Edit Format View Help

```
module simple_circuit(A,B,C,Y);
input A,B,C;
output Y;
wire w1;
assign w1 = C&B;
assign Y=  A|w1    ;
endmodule
```

Ln 1, Col 1

08:53
08-09-2020

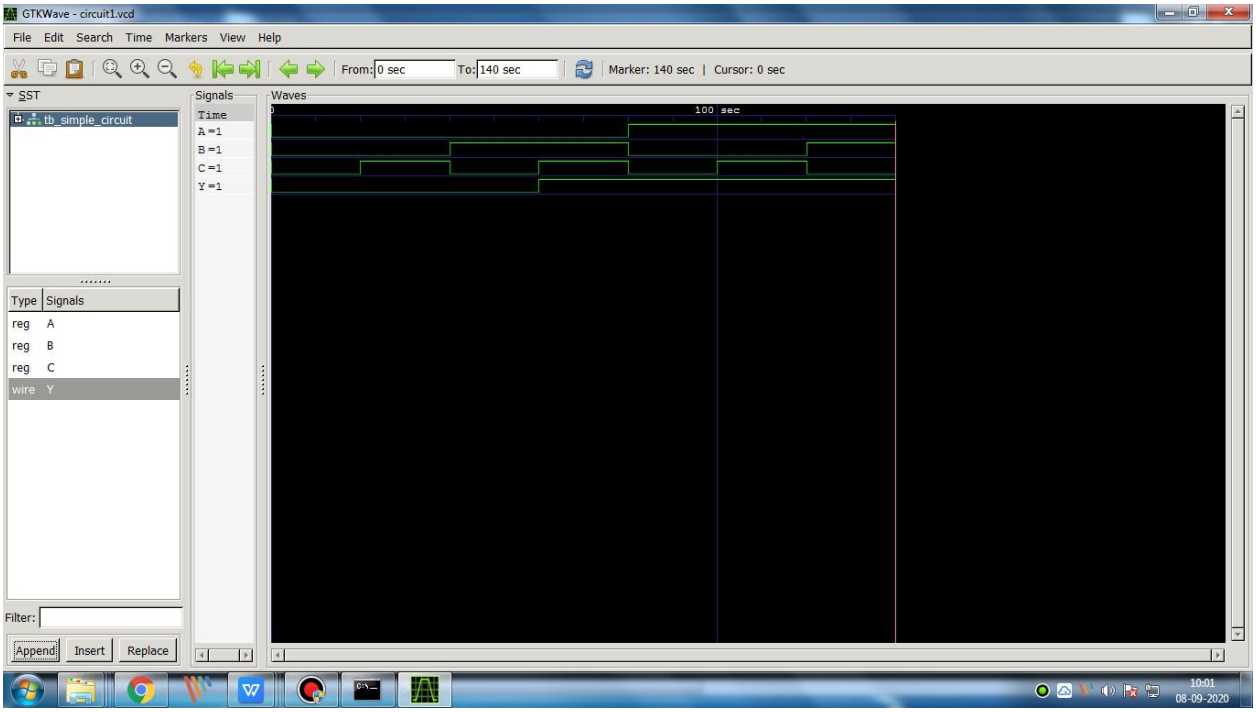
CMD output:



Truth Table:

A	B	Y
0	0	0
0	1	0
0	0	0
0	1	1
1	0	1
1	1	1
1	0	1
1	1	1

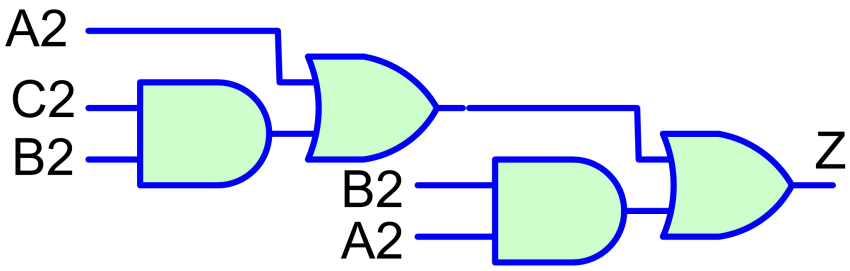
Wave Form:


GTKWave - circuit1.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 140 sec
Marker: 140 sec | Cursor: 0 sec
SST
tb_simple_circuit
Type Signals
reg A
reg B
reg C
wire Y
Filter:
Append
Insert
Replace
Signals
Time
A =1
B =1
C =1
Y =1
Waves
100 sec
10:01
08-09-2020

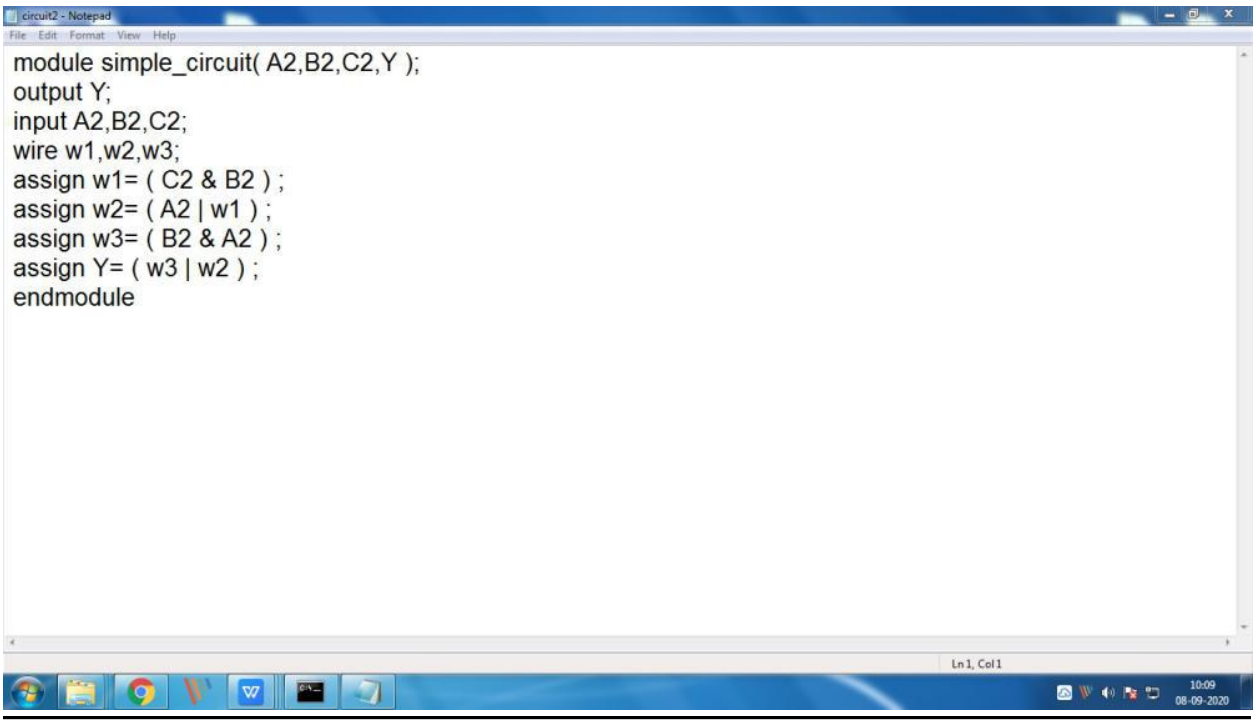
Program #9

Title: Circuit 2

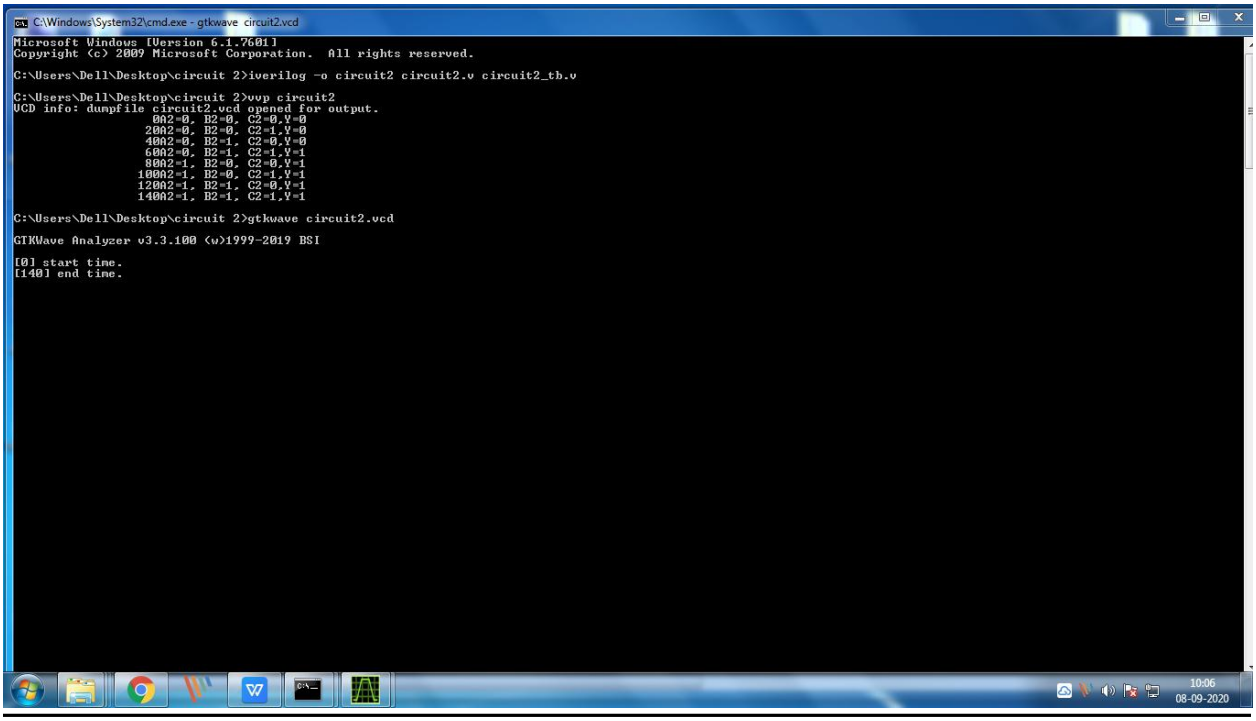
Aim: To achieve the below shown circuit



Program:



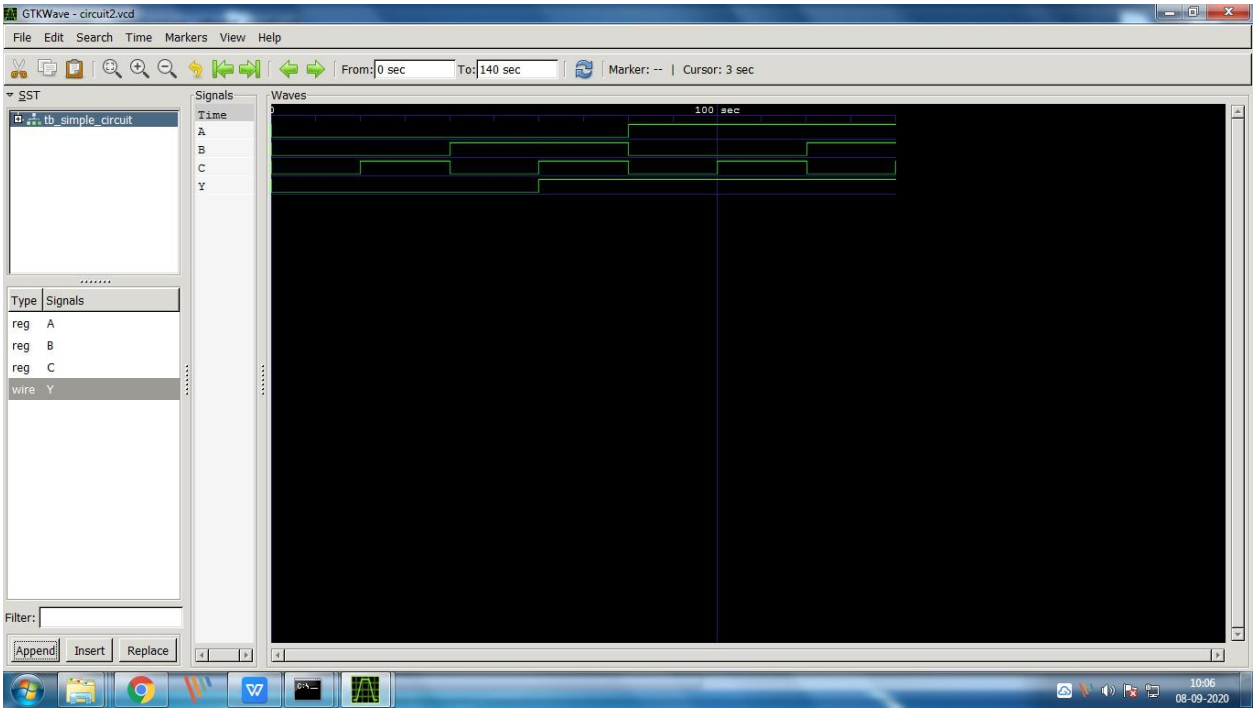
CMD output:



Truth Table:

A	B	Y
0	0	0
0	1	0
0	0	0
0	1	1
1	0	1
1	1	1
1	0	1
1	1	1

Wave Form:


GTKWave - circuit2.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 140 sec
Marker: --
Cursor: 3 sec
SST
tb_simple_circuit
Type Signals
reg A
reg B
reg C
wire Y
Filter:
Append
Insert
Replace
Signals
Time
A
B
C
Y
Waves
100 sec
10:06
08-09-2020

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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Section: G
Date: 08/09/2020