Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/4/2021

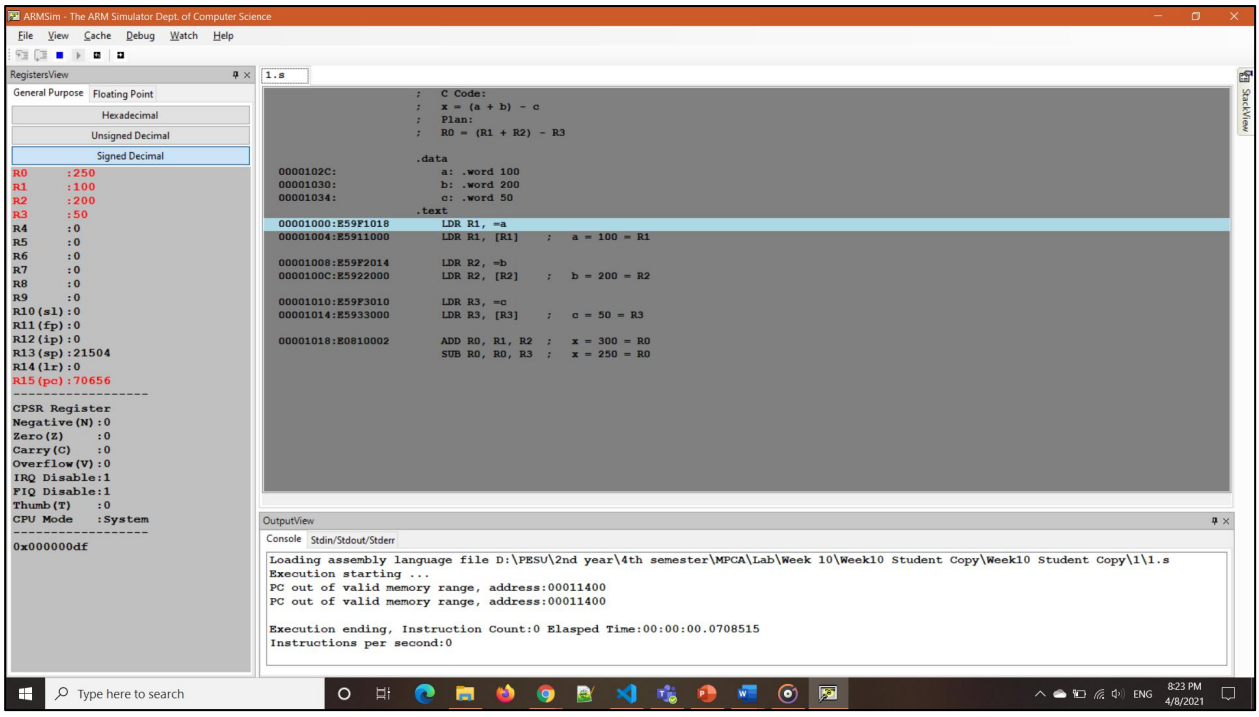
Name: Suhan B Revankar	SRN: PES2UG19CS412	Section G

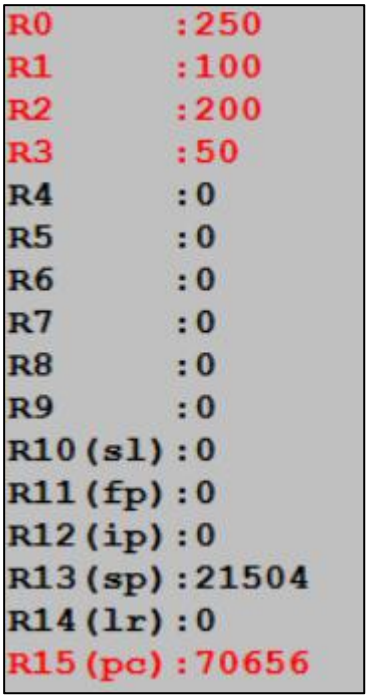
Week#____10____ Program Number: ____1____

Given a C- Code convert it in its equivalent ARM Code.
These programs need to be executed on ARMSIM Simulator

1) x = (a + b) - c;

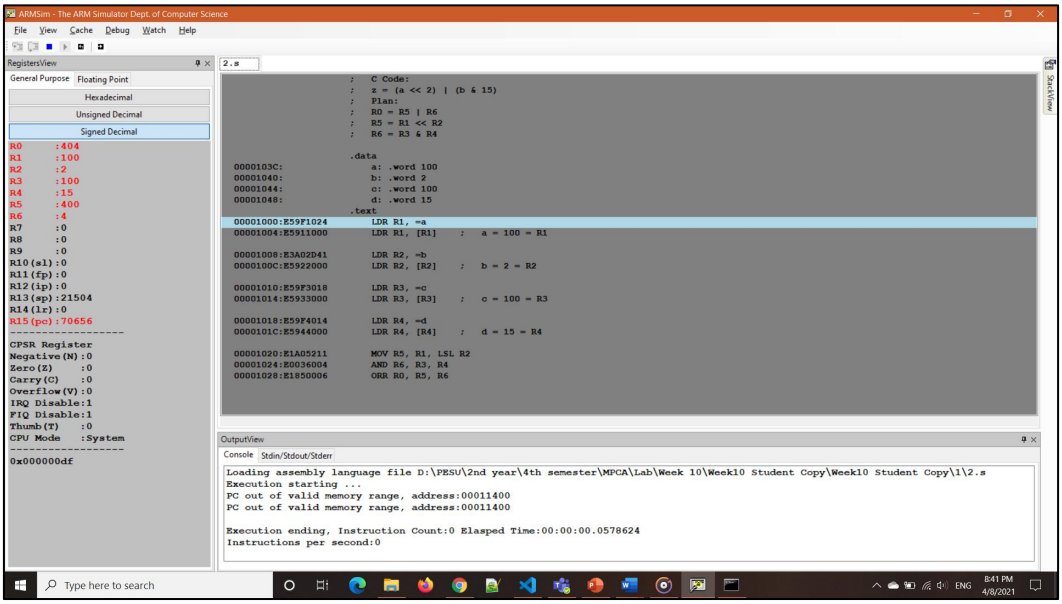
```
1   ;   C Code:
2   ;   x = (a + b) - c
3   ;   Plan:
4   ;   R0 = (R1 + R2) - R3
5
6   .data
7       a: .word 100
8       b: .word 200
9       c: .word 50
10  .text
11      LDR R1, =a
12      LDR R1, [R1]    ;   a = 100 = R1
13
14      LDR R2, =b
15      LDR R2, [R2]    ;   b = 200 = R2
16
17      LDR R3, =c
18      LDR R3, [R3]    ;   c = 50 = R3
19
20      ADD R0, R1, R2  ;   x = 300 = R0
21      SUB R0, R0, R3  ;   x = 250 = R0
```




R0 :250
R1 :100
R2 :200
R3 :50
R4 :0
R5 :0
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):70656

2) z = (a << 2) | (b & 15);

```
1   ;   C Code:
2   ;   z = (a << 2) | (b & 15)
3   ;   Plan:
4   ;   R0 = R5 | R6
5   ;   R5 = R1 << R2
6   ;   R6 = R3 & R4
7
8   .data
9       a: .word 100
10      b: .word 2
11      c: .word 100
12      d: .word 15
13  .text
14      LDR R1, =a
15      LDR R1, [R1]    ;   a = 100 = R1
16
17      LDR R2, =b
18      LDR R2, [R2]    ;   b = 2 = R2
19
20      LDR R3, =c
21      LDR R3, [R3]    ;   c = 100 = R3
22
23      LDR R4, =d
24      LDR R4, [R4]    ;   d = 15 = R4
25
26      MOV R5, R1, LSL R2
27      AND R6, R3, R4
28      ORR R0, R5, R6
```



```
R0      :404
R1      :100
R2      :2
R3      :100
R4      :15
R5      :400
R6      :4
R7      :0
R8      :0
R9      :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):70656
------------------
```

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/4/2021

Name: Suhan B Revankar	SRN: PES2UG19CS412	Section G

Week#____10____ Program Number: ____2____

1) Consider the following instructions. Execute these instructions using simulator of 5 stage pipeline of MIPS architecture.

```
ADD R0, R1, R2
SUB R3, R0, R4.
```

Observe the following and note down the results.

a) Check whether there is data dependency for the second instruction?

Potential Hazards:

```
RAW: Instructions 0 and 1.  Register F1.
```

Dependency lies in F1 (R0).

b) If yes, then, how many stall states have been introduced?

Two stalls

		CPU Cycles									
Instruction		1	2	3	4	5	6	7	8	9	10
0	fp_add (F1, F2, F2)	IF	ID	+|- (f)	MEM	WB					
1	fp_sub (F4, F1, F5)		IF	ID	S	S	+|- (f)	MEM	WB		

Step Execute All Instructions

c) If data forwarding is applied how many stall states have been reduced?

Two stalls

		CPU Cycles									
Instruction		1	2	3	4	5	6	7	8	9	10
0	fp_add (F1, F2, F2)	IF	ID	+|- (f)	MEM	WB					
1	fp_sub (F4, F1, F5)		IF	ID	+|- (f)	MEM	WB				

Step Execute All Instructions

Potential Hazards:

```
No Hazards Found.
```

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/4/2021

Name: Suhan B Revankar	SRN: PES2UG19CS412	Section G

Week#____10____ Program Number: ____3____

Consider the following code segment in C.

```
A = B + E;
C = A + F;
```

a) Write the code using MIPS 5 STAGE pipeline architecture.

```
ADD R0, R1, R2 ; R0 = A, R1 = B, R2 = E
ADD R3, R0, R4 ; R3 = C, R0 = A, R4 = F
```

b) Find the hazards.

		CPU Cycles									
	Instruction	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
0	fp_add (F1, F2, F3)	IF	ID	+|- (f)	MEM	WB					
1	fp_add (F4, F1, F5)		IF	ID	S	S	+|- (f)	MEM	WB		

Step | Execute All Instructions

Potential Hazards:

```
RAW: Instructions 0 and 1.  Register F1.
```

c) Reorder the instructions to avoid pipeline stalls.

$$C = A + F$$
$$A = B + E$$

```
ADD R3, R0, R4 ;   R3 = C, R0 = A, R4 = F
ADD R0, R1, R2 ;   R0 = A, R1 = B, R2 = E
```

		CPU Cycles									
	Instruction	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
0	fp_add (F4, F1, F5)	IF	ID	+|- (f)	MEM	WB					
1	fp_add (F1, F2, F3)		IF	ID	+|- (f)	MEM	WB				

Step | Execute All Instructions

Potential Hazards:

```
No Hazards Found.
```

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/4/2021

Name: Suhan B Revankar	SRN: PES2UG19CS412	Section G

Week#____10____ Program Number: ___4___

Using MIPS 5 stage pipeline architecture, execute the following instructions and avoid stall states if any.

```
LW  $10, 20($1)
SUB $11, $2, $3
ADD $12, $3, $4
LW  $13, 24($1)
ADD $14, $5, $6
```

a)

		CPU Cycles														
	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	fp_ld (F11, Offset, R2)	IF	ID	EX	MEM	WB										
1	fp_sub (F12, F3, F4)		IF	ID	+|- (f)	MEM	WB									
2	fp_add (F13, F4, F5)			IF	ID	+|- (f)	MEM	WB								
3	fp_ld (F14, Offset, R2)				IF	ID	EX	MEM	WB							
4	fp_add (F15, F6, F7)					IF	ID	+|- (f)	MEM	WB						

Step Execute All Instructions

Potential Hazards:

No Hazards Found.

b)

		CPU Cycles														
	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	fp_ld (F11, Offset, R2)	IF	ID	EX	MEM	WB										
1	fp_sub (F12, F3, F4)		IF	ID	+|- (f)	MEM	WB									
2	fp_add (F13, F4, F5)			IF	ID	+|- (f)	MEM	WB								
3	fp_ld (F14, Offset, R2)				IF	ID	EX	MEM	WB							
4	fp_add (F15, F6, F7)					IF	ID	+|- (f)	MEM	WB						

Step Execute All Instructions

Potential Hazards:

No Hazards Found.

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/4/2021

Name: Suhan B Revankar	SRN: PES2UG19CS412	Section G

Week#____10____ Program Number: ___5___

This exercise is to understand the relationship between delay slots, control hazards and branch execution in a 5 stage MIPS pipelined processor.

```
Label 1:    LW  $1, 40($6)
            BEQ $2, $3, Label2: branch taken
            ADD $1, $6, $4

Label 2:    BEQ $1, $2, Label1: branch not taken
            SW  $2, 20($4)
            ADD $1, $1, $4
```

Assume full data forwarding and predict- taken branch prediction.

Note the observations.

There are no hazards.

		CPU														
	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	fp_ld (F2, Offset, R7)	IF	ID	EX	MEM	WB										
1	br_taken (Offset, R3)		IF	ID												
2	fp_add (F2, F7, F5)			IF												
3	br_untaken (Offset, R2)				IF	ID										
4	fp_sd (F3, Offset, R5)					IF	ID	EX	MEM	WB						
5	fp_add (F2, F2, F5)						IF	ID	+|- (f)	MEM	WB					

Step | Execute All Instructions

Potential Hazards:

```
No Hazards Found.
```

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name: Suhan B Revankar

SRN: PES2UG19CS412

Section: G

Date: 11/4/2021