

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:05—03—2021

Name: SUHAN B REVANKAR	SRN: PES2UG19CS412	Section G
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Week#____6_____

Program Number:____1

1. Write an ALP to blink LEDs. First, the right LED is switched on and the left LED is switched off. After 1 second, the right LED is switched off and the left LED is switched on and the program continue to blink both the LEDs.

I. ARM Assembly Code (1).

```

.text
mov r8,#6400
left:
    mov r0,#0x01
    swi 0x201
    sub r0,r0,#1
    cmp r8,#0
    bne leftmov r8,#6400
right:
    mov r0,#0x02
    swi 0x201
    sub r0,r0,#1
    cmp r8,#0
    bne right
mov r8,#6400
both:
    mov r0,#0x03
    swi 0x201
    sub r0,r0,#1
    cmp r8,#0
    bne both
swi 0x011
.end

```

II. Output Screen Shot

The screenshot displays the ARMSim - The ARM Simulator interface. The main window is divided into several panes:

- RegistersView:** Shows the state of 16 registers (R0-R15) and the CPSR register. R0-R15 are all 0x00000000, except for R8 which is 0x00019000. CPSR register shows Negative (N): 0, Zero (Z): 0, Carry (C): 1, Overflow (V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb (T): 0, and CPU Mode: System.
- PluginUIView:** Displays a graphical representation of the ARM processor core, including a 4x4 grid of blue squares and a green square.
- MemoryView:** Shows memory addresses and their corresponding values. The first 16 addresses (0x00000000 to 0x0000000F) are all 0x00000000.
- OutputView:** Displays the execution log, showing the loading of the assembly file and the start of execution.

The assembly code being executed is shown in the center pane, matching the code provided in the first image. The execution log in the OutputView shows the following steps:

```

Loading assembly language file C:\Users\dell\Desktop\MPCA LAB_WEEK6_PES2UG19CS412\WEEK6_1_PES2UG19CS412.s
Execution starting ...

```

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Week#____6_____

Program Number:____2

**Write an ALP to display 0-9, A-F (up and down count)
on an 8 segment display**

I. ARM Assembly Code (1).

```
.data
zero: .byte 0b11101101
one: .byte 0b01100000
two: .byte 0b11001110
three: .byte 0b11101010
four: .byte 0b01100011
five: .byte 0b10101011
six: .byte 0b10101111
seven: .byte 0b11100000
eight: .byte 0b11101111
nine: .byte 0b11101011
A: .byte 0b11100111
B: .byte 0b11101111
C: .byte 0b10001101
D: .byte 0b11101101
E: .byte 0b10001111
F: .byte 0b10000111
```

```
.text
```

```
MOV R0,#0
```

```
always:
```

```
SWI 0x202
CMP R0,#1
BEQ forward
CMP R0,#2
BEQ backward
B always
```

```
forward:
```

```
MOV R3,#16
MOV R2,#1
LDR R1,=zero
loop1:
LDRB R0,[R1]
SWI 0x200
BL delay
ADD R1,R1,R2
SUB R3,R3,#1
CMP R3,#0
BNE loop1
B always
```

```
backward:
```

```
MOV R3,#16
MOV R2,#-1
LDR R1,=F
loop2:
LDRB R0,[R1]
SWI 0x200
BL delay
ADD R1,R1,R2
SUB R3,R3,#1
CMP R3,#0
BNE loop2
B always
```

```
delay:
```

```
MOV R4,#64000
delaycount:
SUB R4,R4,#1
CMP R4,#0
BGE delaycount
MOV PC,LR
```

II. Output Screen Shot

The screenshot displays the ARMSim - The ARM Simulator interface. The main window is divided into several panes:

- RegistersView:** Shows the state of 16 registers (R0-R15) and CPSR. All registers are at 0x00000000 except R13 (SP) at 0x00054000 and R15 (PC) at 0x00010000. CPSR flags are: Negative (N): 0, Zero (Z): 0, Carry (C): 0, Overflow (V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb (T): 0, CPU Mode: System.
- PluginUIView:** Displays a graphical representation of the processor core with a grid of 16 blue squares (0.0 to 3.3) and a green square (3.4). Below the grid is a text area showing assembly code for WEEK6_2_PES2UG19CS412.s, including instructions like MOV R0, #0, SWI 0x202, and CMP R0, #1.
- MemoryView3:** Shows memory addresses from 0x00000000 to 0x0000001F, with values mostly represented by '??'.
- OutputView:** Shows the console output, displaying the message: "Loading assembly language file C:\Users\dell\Desktop\MPCA LAB_WEEK6_PES2UG19CS412\WEEK6_2_PES2UG19CS412.s".

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Week#____6_____

Program Number:____3

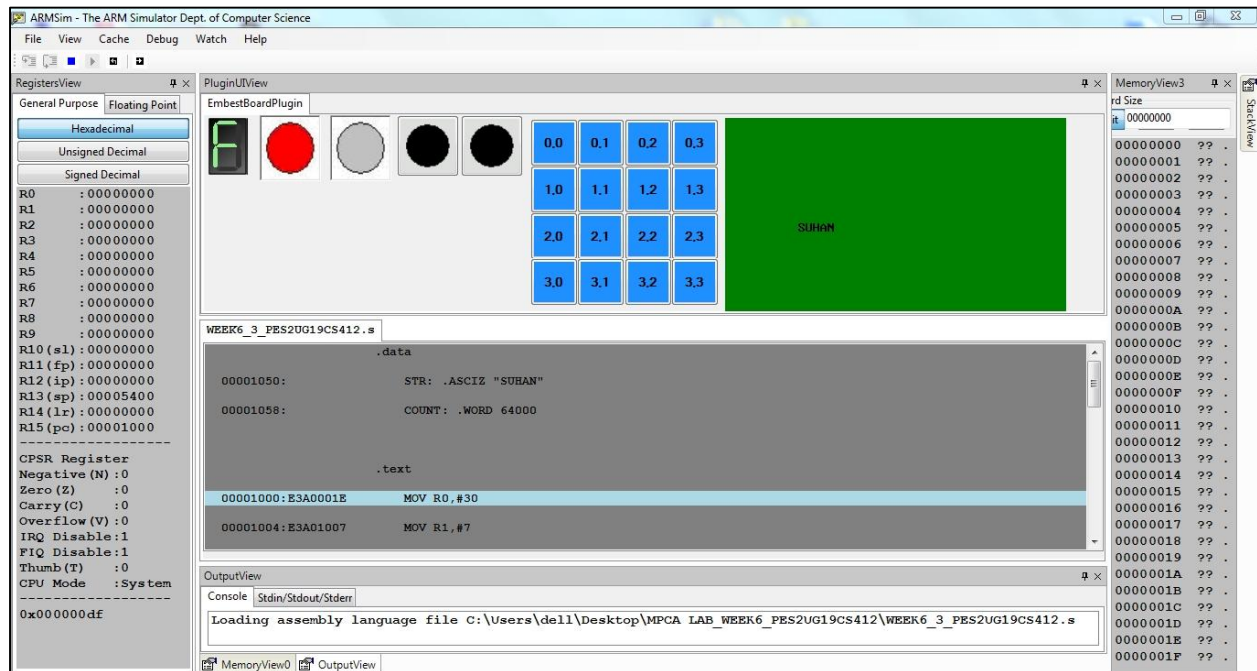
**Write an ALP to move a string from Right to Left on LCD
(40 columns by 15 rows).**

I. ARM Assembly Code

```
.data
STR: .ASCIZ "SUHAN"
COUNT: .WORD 64000
```

```
.text
MOV R0,#30
MOV R1,#7
MOV R7,#0
LDR R8,=COUNT
LDR R8,[R8]
LDR R2,=STR
loop:
    SWI 0x204
    BL delay
    CMP R0,#0
    SUBNE R0,R0,#1
    SWIEQ 0x011
    B loop
delay:
    CMP R7,R8
    ADDNE R7,R7,#1
    BNE delay
    SWI 0x206
    MOV R7,#0
    MOV PC,LR
```

II. Output Screen Shot



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: SUHAN

B REVANKAR

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Section: G

Date: 05—03—2021