Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:27—01—2021

Name: SUHAN B REVANKAR	SRN: PES2UG19CS412	Section G

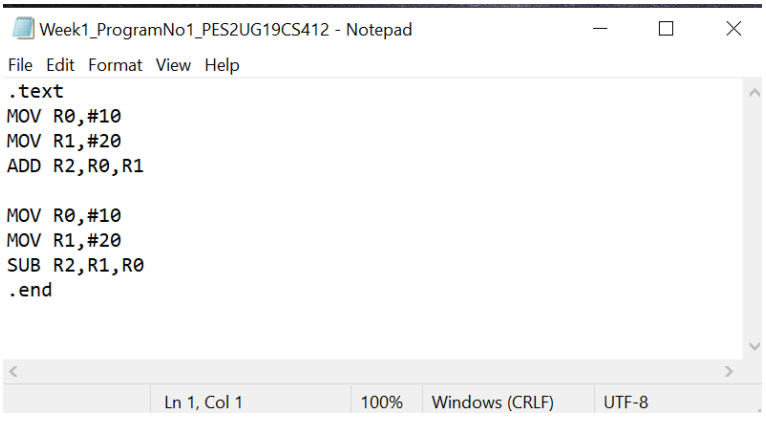
Week#____1_____ Program Number: ____1___

Title of the Program

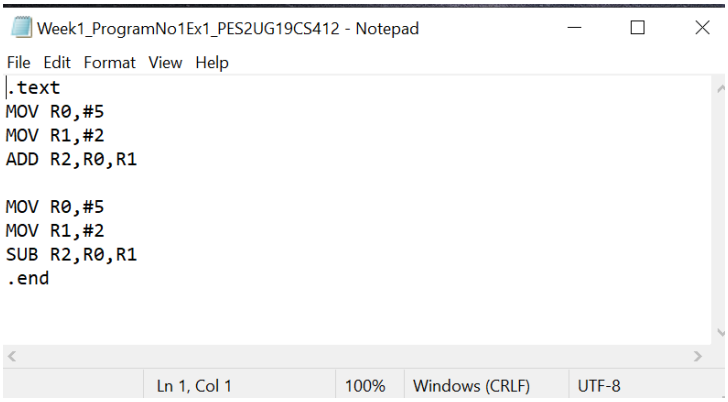
Write an ALP using ARM instruction set to add and subtract two 32 bit numbers .Both numbers are in registers.

I. ARM Assembly Code for each program

Test case used in class



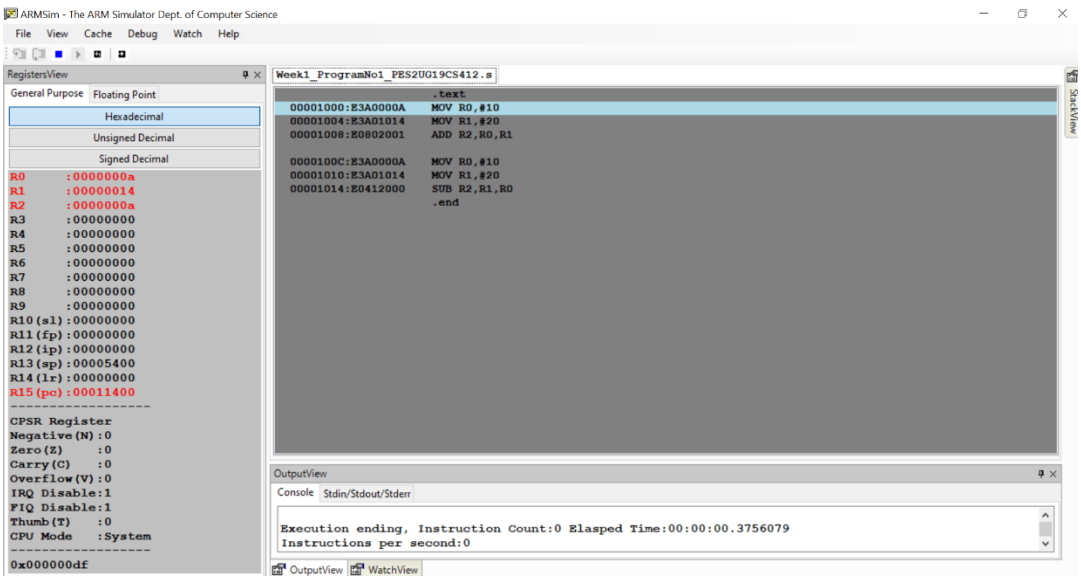
Own example



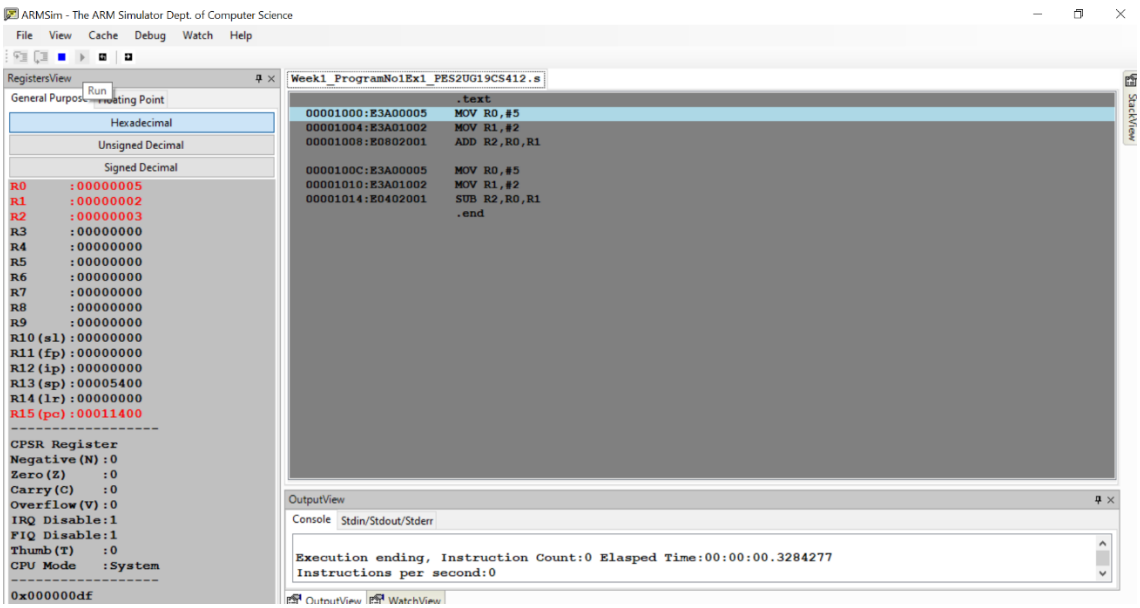
II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)

Output of test case



Output of own example



III. Output table for each program

TESTCASE R0=10=Hex 0A R1=20=Hex 14 After addition R2=30=Hex 1E After subtraction R2=10=Hex 0A			
R0	R1	Arithmetic operation	RESULTS
0x0A	0x14	ADD	R2=0x1E
0x0A	0x14	SUB	R2=0x0A

Own example

Own example R0=5=Hex05 R1=2==Hex02 After addition R2=7=Hex07 After subtraction R2=3=Hex03			
R0	R1	Arithmetic operation	Results
0x05	0x02	ADD	R2=0x07
0x05	0x02	SUB	R2=0x03

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Name: SUHAN B REVANKAR	SRN: PES2UG19CS412	Section G

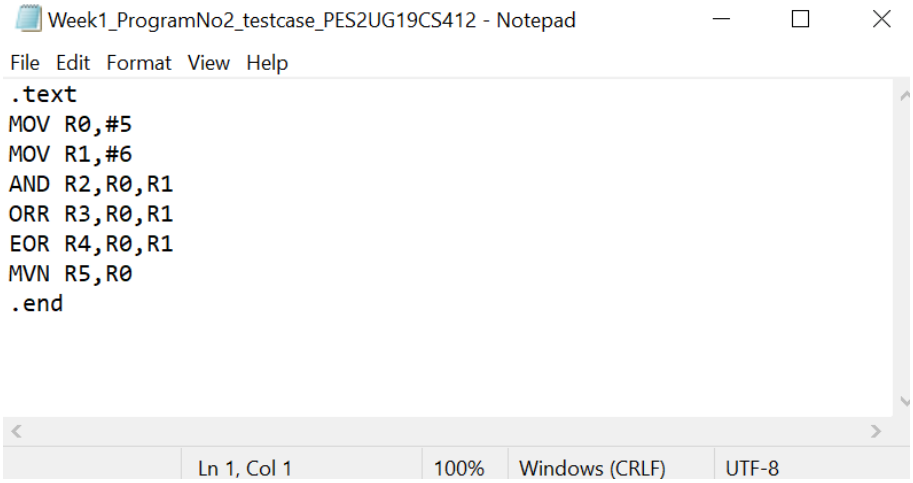
Week#____1_____ Program Number: ____2___

Title of the Program

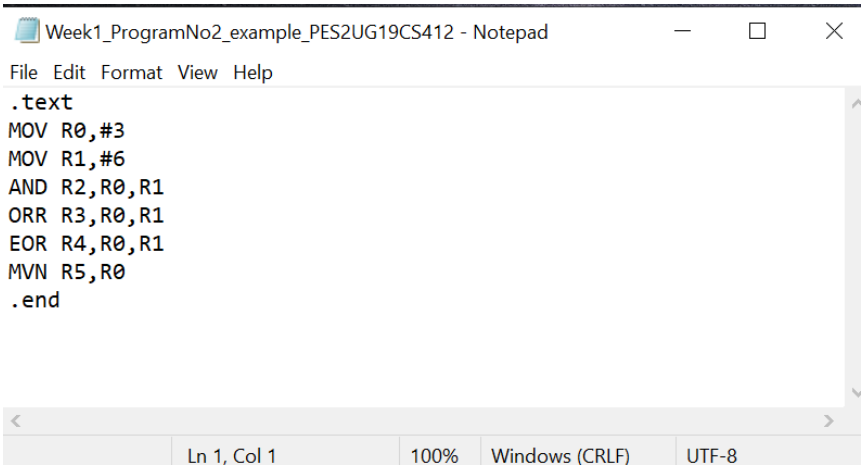
Write an ALP to demonstrate logical operations. All operands are in registers.

I. ARM Assembly Code for each program

Test case used in class



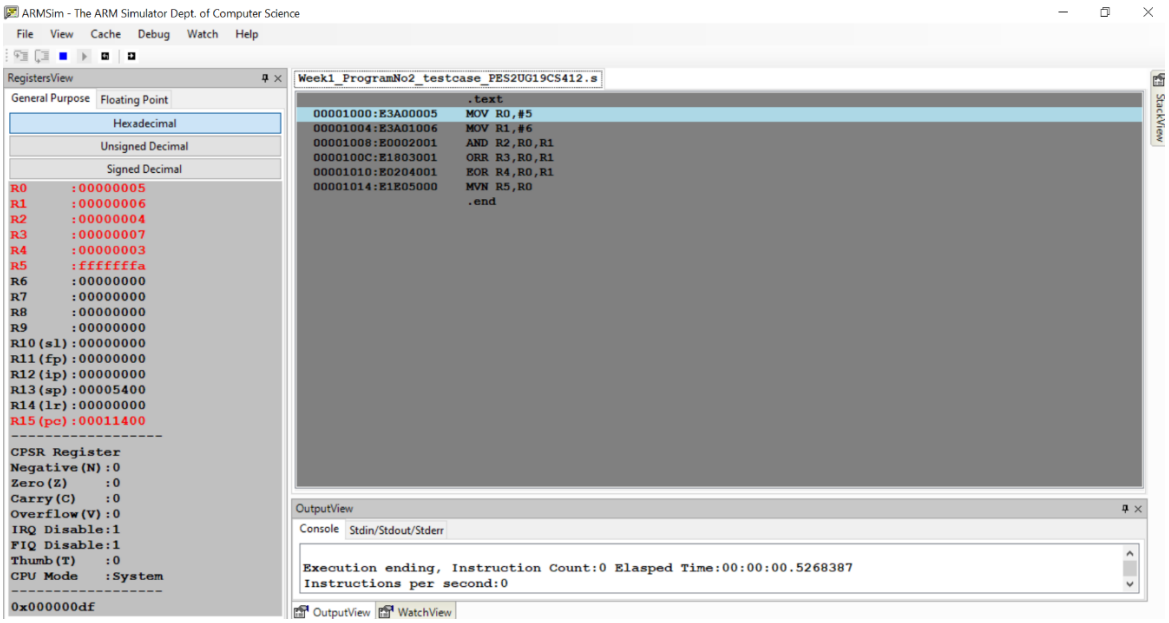
Own example



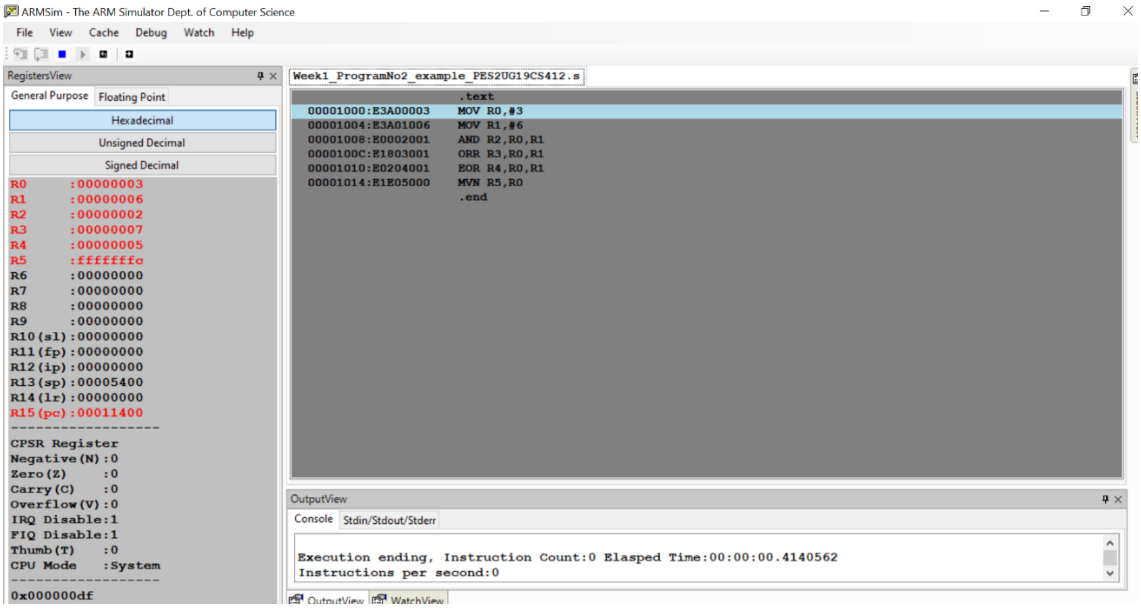
II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)

Output of testcase used in the class



Output of own example



III. Output table for each program

TESTCASE

R0	R1	Logic operation		Results
0x05	0x06	ADD	ADD	R2=0x04
0x05	0x06	OR	OR	R3=0x07
0x05	0x06	EX-OR	EX-OR	R4=0x03
0x05		NOT	MVN	R5=0xfffffffa

Own example

R0	R1	Logic operations		Results
0x03	0x06	AND	AND	R2=0x02
0x03	0x06	OR	OR	R3=0x07
0x03	0x06	EX-OR	EX-OR	R4=0x05
0x03		NOT	MNV	R5=fffffffc

Date:27—01--2021

Name: SUHAN B REVANKAR	SRN: PES2UG19CS412	Section G

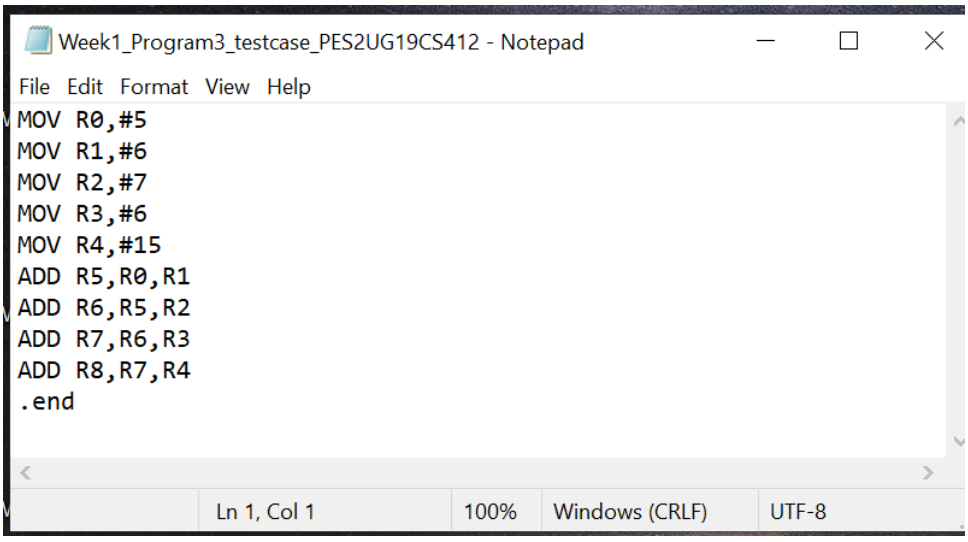
Week#____1_____ Program Number: ____3___

Title of the Program

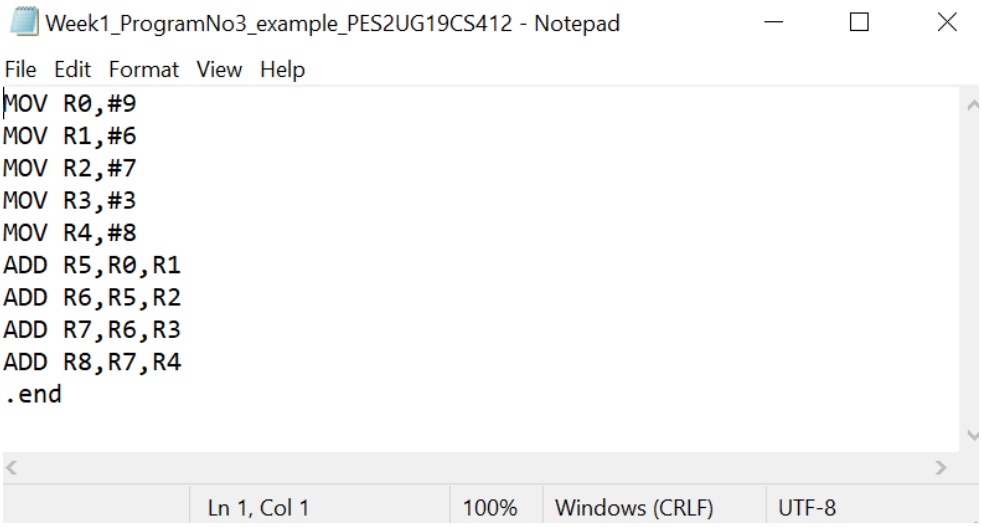
Write an ALP to add 5 numbers where values are present in registers.

I. ARM Assembly Code for each program

Testcase used in class

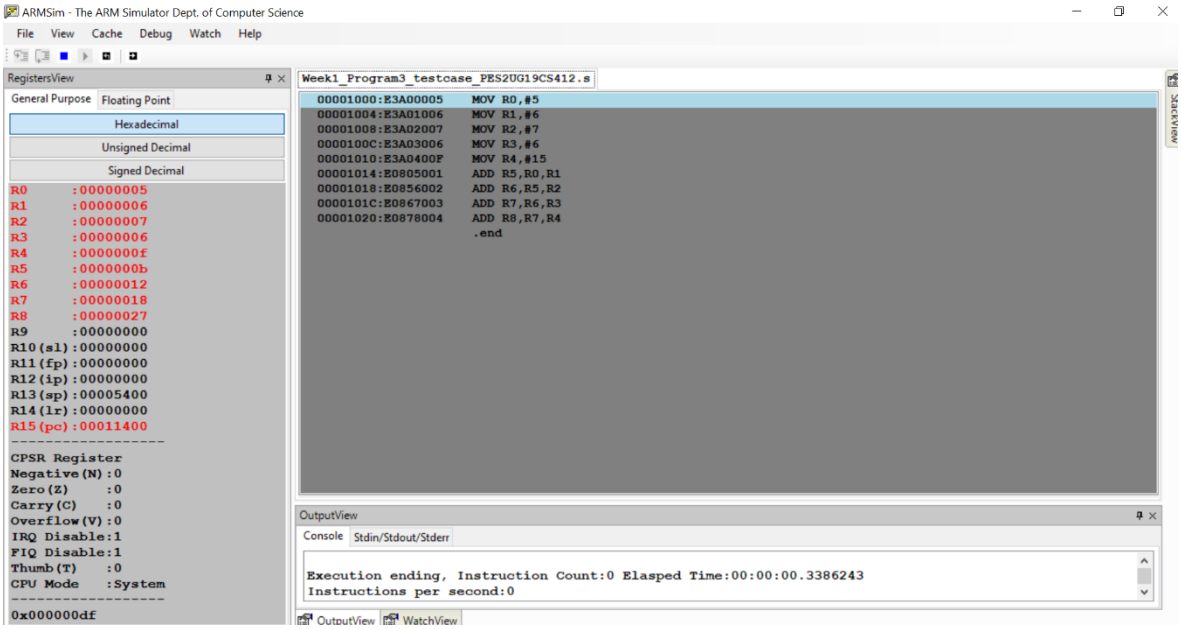


Own example

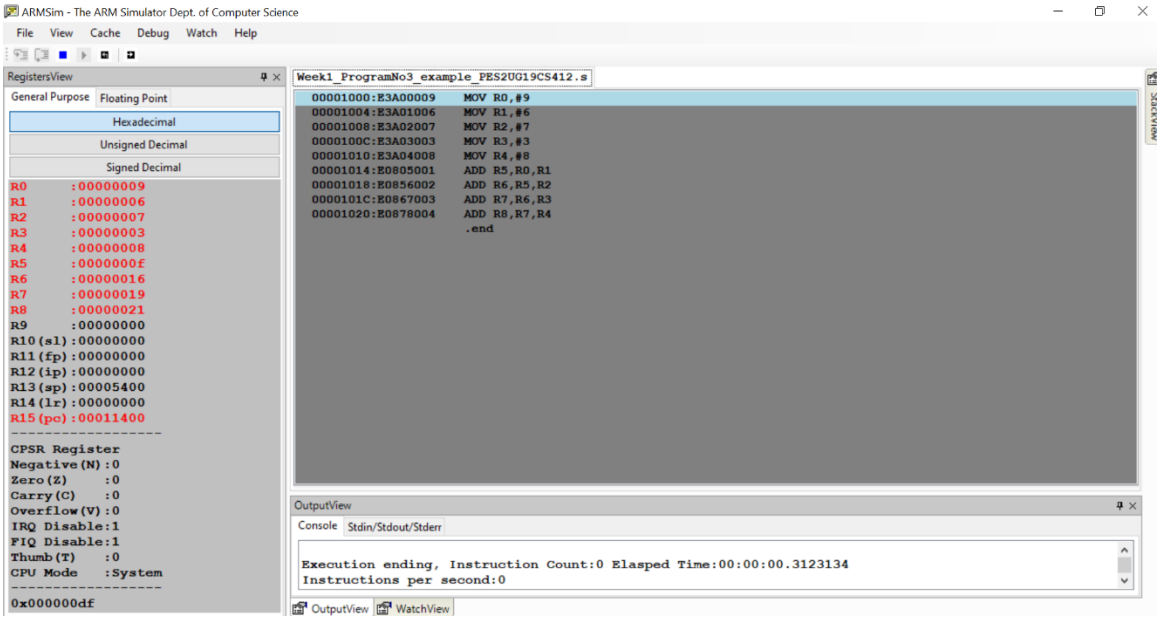


II. Output Screen Shot (Register Window, Output window)
The output should be verified with 2 test cases (one example shown in class, one example of own choice)

Output of testcase



Output of own example



III. Output table for each program

TESTCASE

R0		0x05
R1		0x06
R2		0x07
R3		0x06
R4		0x15
R5	R0+R1	0x0b
R6	R5+R2	0x12
R7	R6+R3	0x18
R8	R7+R4	0x27

Own example

R0		0x09
R1		0x06
R2		0x07
R3		0x03
R4		0x08
R5	R0+R1	0x0f
R6	R5+R2	0x16
R7	R6+R3	0x19
R8	R7+R4	0x21

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4th Semester, Academic Year 2020-21

Date:27—01—2021

Name: SUHAN B REVANKAR	SRN: PES2UG19CS412	Section G

Week#____1_____ Program Number: ____4___

Title of the Program

Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

I. ARM Assembly Code for each program

Week1_ProgramNo4_PES2UG19CS412 - Notepad

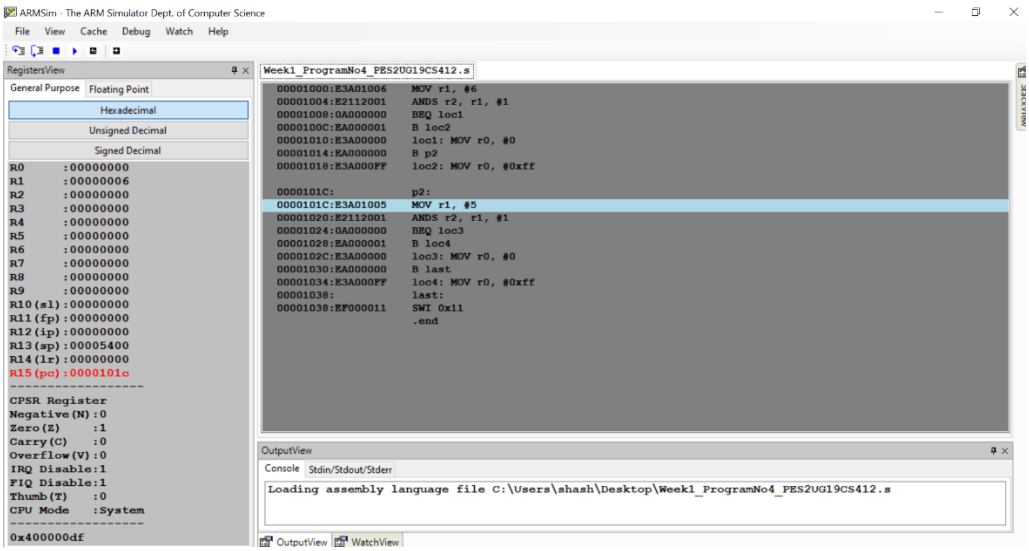
File Edit Format View Help

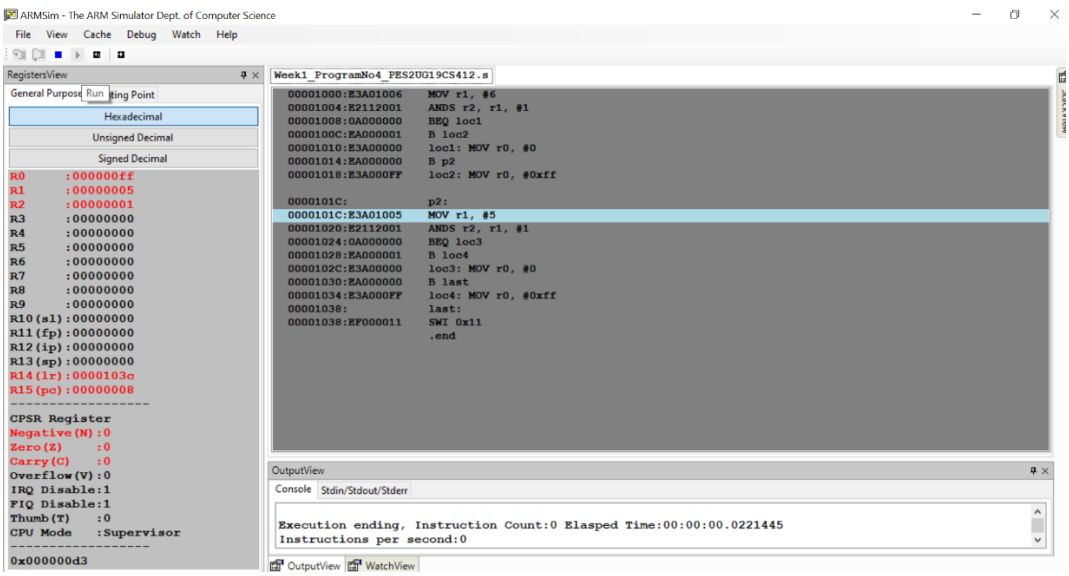
```
MOV r1, #6
ANDS r2, r1, #1
BEQ loc1
B loc2
loc1: MOV r0, #0
B p2
loc2: MOV r0, #0xff

p2:
MOV r1, #5
ANDS r2, r1, #1
BEQ loc3
B loc4
loc3: MOV r0, #0
B last
loc4: MOV r0, #0xff
last:
SWI 0x11
.end
```

II. Output Screen Shot (Register Window, Output window)

The output should be verified with 2 test cases (one example shown in class, one example of own choice)





III. Output table for each program

CASE1	R1		0x06
	R2	After AND operation	0x00
	R0	(EVEN)	0x00
CASE2	R1		0x05
	R2	After AND operation	0x01
	R0	(ODD)	0xff

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.

- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: suhanb
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SRN: PES2UG19CS412
Section: G
Date: 27—01—2021