Assignment 9 (GATE, EC2017,45)

Suhani Kalra

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0.1 QUESTION

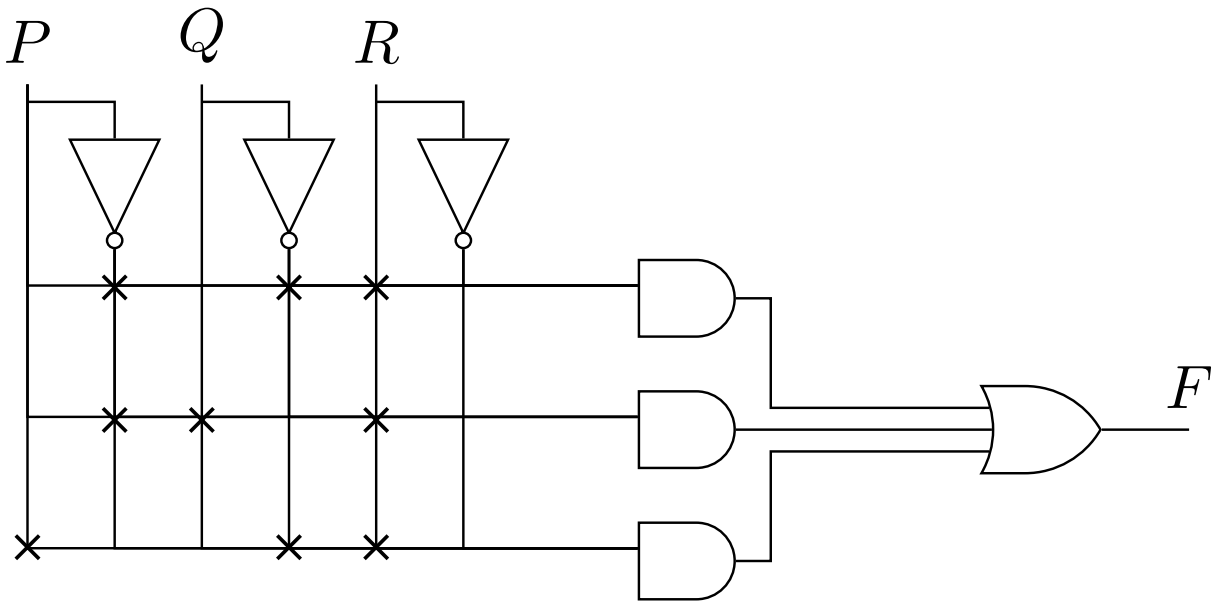


Figure 1: GATE, EC2017,45

A programmable logic array (PLA) is shown in the figure.The Boolean function F implemented is

1. P'Q'R+PQ'R+P'QR
2. (P'+Q'+R)(P'+Q+R)(P+Q'+R')
3. P'QR+PQ'R+PQR
4. (P+Q'+R)(P'+Q+R)(P+Q'+R')

0.2 SOLUTION

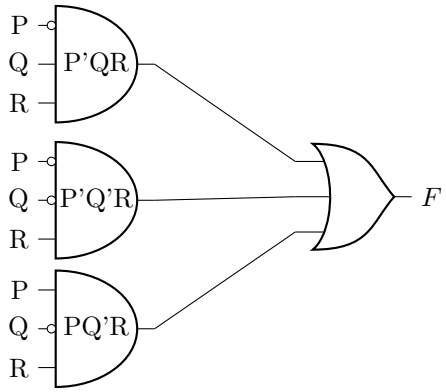
For the question 45 of GATE EC 2017 exam(Figure 1, Section 0.1),
we had to deduce the expression for the final Output F, given in Figure 1 (section0.1) for this, we can say that, Figure 1 could be reduced to the following equation

$$F = P'Q'R + PQ'R + P'QR \tag{1}$$

The following report aims at providing a detailed derivation of the equation1 using,Truth Table and Logical Circuit Diagram.

0.3 CIRCUIT DIAGRAM

The given question (figure 1, section 0.1) can also be represented by the following circuit diagram. This circuit diagram helps us to deduce the above mentioned equation1 (section0.2).



P	Q	R	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

0.4 TRUTH TABLE

TRUTH TABLE- The given question (figure 1, section 0.1) can also be represented by the eforementioned Truth Table. This Truth table helps us to deduce the above mentioned equation1 (section0.2).