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Ans 1: (a) Hit ratio $= 2/9 = 0.22$

(b)

Index	V	Tag	Data
000	N		
001	Y	00	Mem[00001]
010	Y	01	Mem[01010]
011	Y	10	Mem[10011]
100	Y	10	Mem[10100]
101	Y	01	Mem[01101]
110	Y	01	Mem[01110]
111	N		

Ans 2 (a) Disk Access Time

$= $ seek time + rotational delay + transfer time + controller overhead

$= 12 + (0.5 * 60 * 10^3/3600) + (512/(3.5 * 2^{20})) * 1000 + 5.5$

$= \underline{25.97 \text{ ms}}$

(b) transfer time gets changed to $(8 * 1024/(3.5 * 2^{20})) * 1000$

Disk Access Time $= 12 + (0.5 * 60 * 10^3/3600) + (8 * 1024/(3.5 \times 2^{20})) * 1000 + 5.5$

$= \underline{28.07 \text{ ms}}$

Ans 3

(i) 6 page faults (ii) 5 page faults

(iii) It is unexpected as MFU is coming more effective than LRU which is used more generally as most frequent page is expected to occur more frequently but we are replacing it.

Ans 4 This is done to effectively reduce cache miss penalty as the first level cache minimizes the hit time whereas second level cache minimizes the miss rate. As a result, first level cache is usually small with low associativity and second level cache is usually large with large blocks & a higher associativity.

Ans 5 Max allowable time = Time for one cycle − TLB lookup time

$= 0.4 - 0.12$

$= \underline{0.28 \text{ ns}}$

Ans 6 (i) As page table is indexed by the virtual page numbers, it uses $54 - 14 = 40$ bits. Number of entries $= 2^{40}$.

Each PTE has 4 bytes.

∴ Total size of the page table $= \underline{2^{42} \text{ bytes}} \approx$ 4 terabytes.

(~~Assuming~~ (~~virtual page offset~~ $\log_2(16 * 2^{10}) = 14$)

(ii) Each page table has 4 bytes (32 bits) and page size is 16K bytes (as we need $\log_2(16 * 2^{10} * 2^3)$, ie, 17 bits to hold the page offset.

(b) we need $32 - 8$ (used for protection) $= 24$ bits for page nos.

The largest physical memory size is $2^{(17+24)}/2^{(3)}$ bytes

$= \underline{2^{38} \text{ bytes} = 256 \text{GB}}$.