CS31007: Computer Organization and Architecture

Solution for Class Test-4 (on 7th November 2020)

1. (a) [2 marks] Hit ratio = 2/9 = 0.22.
   Note: cache hit occurs for the 2nd and 3rd accesses (full credit would be given even if you only mention the hit ratio.)
   (b) [6 marks]

Index	V	Tag	Data
000	N	X	X
001	Y	00	Mem[00001]
010	Y	01	Mem[01010]
011	Y	10	Mem[10011]
100	Y	10	Mem[10100]
101	Y	01	Mem[01101]
110	Y	01	Mem[01110]
111	N	X	X

2. (i) [4 marks] Time to read a single sector = 25.97 ms.
   (ii) [1 mark] Only the transfer time gets changed. The average time to read 8 KB in 16 consecutive sectors in the same cylinder = 28.07 ms.

3. (i) [3 marks] No. of page faults for LRU scheme: 6
   Hit/miss sequence: M M M M H H M (evicts 1) M
   (ii) [3 marks] No. of page faults for MFU scheme: 5
   Hit/miss sequence: M M M M H H M (evicts 4) H
   (iii) [1 mark] The result is somewhat surprising because LRU usually is a very effective and logically intuitive scheme, but here MFU outperforms LRU.

4. [2 marks] Given extremely high microprocessor clock frequencies prevalent currently, as cache memory becomes larger, it becomes progressively difficult to implement the circuitry capable to searching a cache and returning the searched value (in case of a cache hit) within one clock cycle. Hence, it is a pragmatic choice to design multi-levelled cache memory, so that if a cache miss occurs, there is still the possibility of finding the searched value in the higher-level cache, while incurring minimal 1st-level cache miss penalty.

5. [2 marks] Maximum allowable time = Clock time period – time to lookup TLB
   = 1/(2.5 GHz) – 0.12 ns = (0.40 - 0.12) ns = 0.28 ns
   Note: full credit for correct numerical answer without any explanation.

6. (i) [2 marks] Page offset requires 14 bits.
   Size of page table: No. of page table entries * PTE size = $2^{40} * 2^2 = 2^{42}$ bytes.

(ii) [4 marks] No. of bits required for page number: 24. Each page: 2^{14} bytes. Largest physical memory size = $2^{(24 + 14)}/2^{10}$ kB = 2^{28} kB.