# CS31007: Computer Organization and Architecture

## Solution for Class Test-2 (on 3rd October 2020)

1. [5 marks] 27 clock cycles (@2.5 GHz frequency, i.e. 0.4 ns per clock cycle) => 10.8 ns

2. [5 marks] 3 lw/sw instructions => 12 bytes transferred

3. [5 marks] The content of register $t1 is 1 (0x00000001).

Note that addu and sll operate in unsigned mode, while addi treats the two operands as signed quantities.

4. [5 marks]
```
lui $t1, 1
ori  $t1, $t1, 9464
```

5. [4 marks] $t2 contains the absolute value of the number contained in $t1.

6. [6 marks]
```
/* The following function returns x+1 */
int function_increment (int x)
{
    if (x == 0) return 1;
    else if (x % 2 == 1) return (2 * function_increment(x/2));
    else return (x+1);
}
```