Indian Institute of Technology Kharagpur

Department of Computer Science and Engineering

Class Test-4, Autumn 2020-21

Computer Organization and Architecture (CS31007)

Students: 118 **Date**: 07-November-2020

Full marks: 30 **Time**: 75 minutes

Credit: 20%

INSTRUCTIONS: This is an OPEN-BOOK, OPEN-NOTES test. The questions are such that they require either numerical answers or very short answers (in one/two sentences or a few lines of code). Please write ONLY THE ANSWERS on a sheet of paper, scan it (or take a photo), and submit the image of the solution sheet on Moodle. DO NOT FORGET TO WRITE YOUR NAME AND ROLL NUMBER AT THE TOP OF YOUR ANSWER SHEET. You may use calculators if required. ANSWER ALL QUESTIONS.

1. A processor has an 32 byte main memory (DRAM) module, a word size of 1 byte, and a direct-mapped cache capable of holding 8 words. Table-1 given below shows the initial state of the cache. (a) Calculate the *hit*

Table 1: Initial State of Cache

Index	V	Tag	Data
000	N		
001	Y	00	Mem[00001]
010	N		
011	Y	11	Mem[11011]
100	Y	10	Mem[10100]
101	Y	01	Mem[01101]
110	Y	00	Mem[00110]
111	N		

ratio, and (b) show the final contents of the cache for the following memory address access sequence:

10011 00001 00110 01010 01110 11001 00001 11100 10100

[**2 + 6 = 8**]

2. Suppose we have a magnetic disk with the following parameters: average seek time: 12 ms; rotation rate: 3600 RPM; transfer rate: 3.5 MB/second (with 1 MB $\equiv 2^{20}$ bytes); number of sectors per track: 64; sector size: 512 bytes; controller overhead: 5.5 ms. Calculate: (i) the average time to read a single sector, and, (ii) the average time to read 8 KB in 16 consecutive sectors in the same cylinder. [**4 + 1 = 5**]

3. Consider a main memory (DRAM module) that is capable of holding only 4 pages, each of size 1 MB. Suppose the virtual pages are numbered as 1, 2, 3, ... etc. Consider the following access sequence of virtual page numbers:

1 2 3 4 4 4 5 1

Consider two different page replacement policies: *Least Recently Used* (**LRU**) and *Most Frequently Used* (**MFU**). The MFU scheme (somewhat surprisingly) preferentially evicts the page from main memory that has been accessed the most number of times. Calculate: (i) the number of page faults for the LRU scheme; (ii) the number of page faults for the MFU scheme, and, (iii) comment whether you find the result unexpected. [**3 + 3 + 1 = 7**]

4. (Answer in maximum two sentences) What is the reason for using a combination of first and second-level caches rather than using the same chip area for a larger first-level cache? [**2**]

5. Consider a microprocessor that uses a TLB indexed by virtual page number, and a direct-mapped cache which is tagged by physical address. The microprocessor clock frequency is 2.5 GHz. A single TLB lookup takes 0.12 ns. Calculate the maximum allowable time for a cache hit in this microprocessor. [**2**]

6. The memory architecture of a machine $\mathcal{M}$ is summarized as follows: virtual address: 54 bits, page size: 16 KB, each page table entry is of size: 4 bytes. (i) Calculate the size of the page table (in bytes); (ii) for the above machine $\mathcal{M}$, assume that for each page table entry, 8 bits are reserved for various operating system functionalities (protection, replacement, valid, modified, hit/miss, etc.). Derive the largest physical memory size (in bytes) allowed for this machine. Make sure you consider all the fields required by the translation algorithm. [$\mathbf{2 + 4 = 6}$]