Indian Institute of Technology Kharagpur

Computer Science and Engineering

CS 31007 COMPUTER ORGANIZATION AND ARCHITECTURE Autumn 2020

Date: 17.11.2020 **Maximum points = 25** Credit: 20%

Online Test-05 (Solutions) **Time:** 10:15 AM - 11:30 AM

Instructions:

This is an OPEN-BOOK, OPEN-NOTES, MCQ/Short-Answer type test. For an **MCQ-type** question, please choose answers from the given choices or select TRUE/FALSE. Unless otherwise stated, each correct answer will fetch 4 points, incorrect answer will contribute 0 point, and no answer leads to 1 point. Answer *all* questions. This question paper has *five* pages.

Submission of answers: Please create a file including **your name, roll-number**, and your **answers**, and submit it to the CSE Moodle Page by **11:45 AM, 17 November 2020.**

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1. (4 points): Short-Answer type

A single-cycle data path implementation of a *non-pipelined* MIPS processor is shown in Figure 1. **Fill out** the following table with appropriate values {0, 1, *x* (don't care)} that are required to assert the control signals for executing the MIPS instruction: *addi* $t1, $t2, 200.

RegDst	Branch	Mem Read	Memto Reg	Mem Write	ALU Src	Reg Write	ALU Op1	ALU Op0	Function Field Instruct. bits [5-0]					
0	0	0	0	0	1	1	0	0	*x*	*x*	*x*	*x*	*x*	*x*

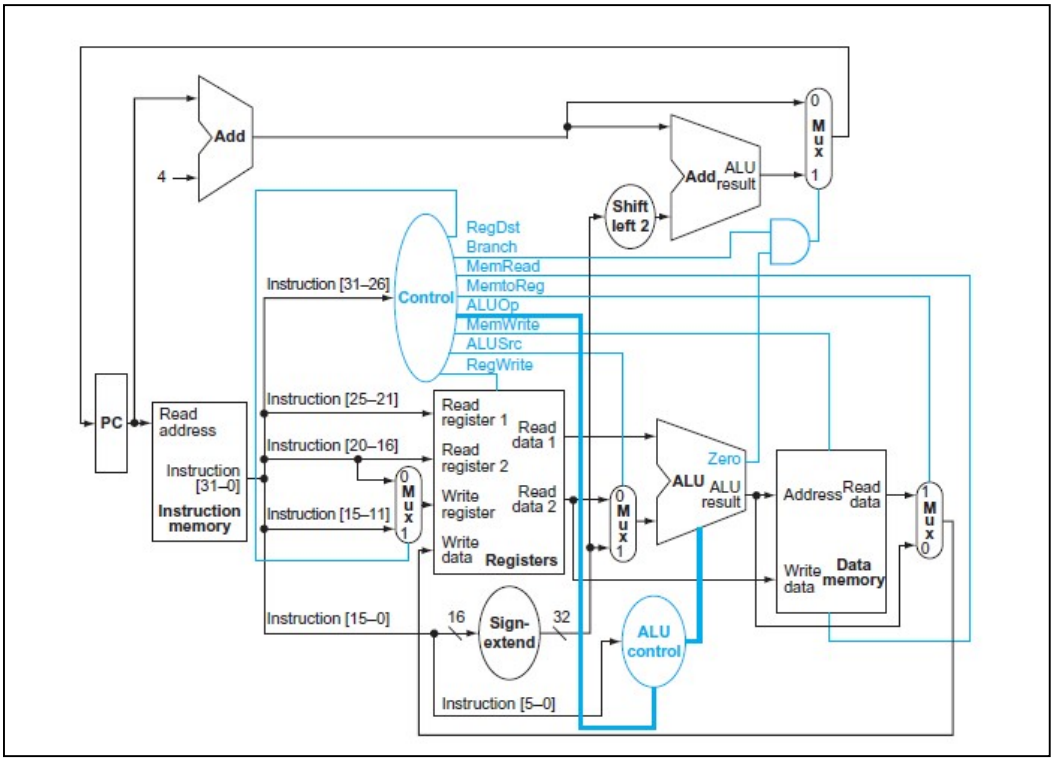

Figure 1: Single-cycle implementation of a MIPS Processor

2. (4 points): MCQ
In a single-cycle data path implementation of a *non-pipelined* MIPS processor as shown in Figure 1 above, operation times for the major functional units are given as follows:

> Instruction and Data Memory Units: 2 *n*s each; Register File Read/Write: 1 *ns* each; ALU: 3 *ns*; Adder for PC+4: 2 *ns*; Adder for branch-address computation: 2 *ns*; MUX block: 1 *ns* each; Sign-Extend and Shift-Left: 1 *ns* each; other units: negligible.

Assume that the machine implements only a small subset (*lw, sw, add, addi, beq*) of instructions. The value of the clock-cycle-time (CCT) should be at least (choose the closest one):

A. 10 *ns*; B. 11 *ns*; C. 12 *ns*; D. 13 *ns*. E. none of these

3. (4 points): MCQ
In the MIPS single-cycle architecture shown in Figure 2 below, suppose one wire of the data path marked with red cross-mark (output bus of the sign-extension module) has become faulty (say, always the wire is fixed at logic 0 regardless of the actual signal arriving on it). Assume that the machine implements only a small subset (*lw, sw, add, addi, beq*) of instructions. Which of the following statement(s) is(are) true?

A. The execution of some *lw* and *sw* instructions might be affected but other instructions will be fine.
B. The execution of some *lw*, *sw* and *beq* instructions might be affected but other instructions will be fine.
C. The execution of some *sw* instructions, some *addi* instructions, and all *beq* instructions will be affected.
D. The execution of all *add* instructions and all branch instructions of type *beq* $t1, $t2, Target, where ($t1) ≠ ($t2) will remain unaffected.
E. None of the above (Only D is true)

4. (4 points): MCQ
Consider a pipelined implementation of MIPS processor as shown in Figure 3, where each of the stages takes the same amount of time (i.e., 1 clock cycle). Given a program *P*, assume that all machine instructions in *P* can be executed without any pipeline stall, except *beq* instructions. In *P*, the frequency of branch instructions is 30% and out of those, 60% are not taken. The pipeline controller works on statically predicting that branch is always "*not taken*". Assume pipeline overhead due to inter-stage latches is negligible. The maximum speed-up achievable by this pipelined machine over non-pipelined single-cycle implementation when the number of instructions in *P* is large, is closest to (choose one):

A. 2.63; B. 3.67; C. 4.03; D. 4.32; E. None of these

5. (4 points): MCQ
Consider the following sequence of actual outcomes in a program for a branch instruction that is iteratively executed 11 times. “T” means ‘the branch is taken’, whereas “N” means ‘the branch is not taken’. Assume that this is the only branch instruction in the program.

Actual branch outcomes are: T T T N T N T T T N T

The pipeline controller uses a dynamic branch predictor based on **2-bit branch history.** Assume that the predictor state is initialized to ‘N’. The number of mispredictions is (choose one):

A. 3; B. 5; C. 7; D. 8; E. None of these

6. (5 points) MCQ [There are five TRUE/FALSE type questions below; each correct answer will fetch 1 point, each wrong answer/no answer will be given 0 point but “all no-answer” will fetch 1 point).

Consider the execution of the following code *P* in a 5-stage MIPS pipelined machine, where registers are updated in the first-half of a clock cycle and they are read in the second half of a clock cycle. Assume that the first stage (IF: Instruction Fetch) of the first instruction (I0) is being executed during clock cycle #1.

- I0: *add* $r4, $r1, $r0
- I1: *sub* $r9, $r3, $r4
- I2: *add* $r4, $r5, $r6
- I3: *lw* $r2, 100($r3)
- I4: *lw* $r2, 0($r2)
- I6: *and* $r3, $r4, $r1

For each of the following statements, state whether it is TRUE or FALSE:

(a) There are three instances of data-hazards in *P*; FALSE
(b) Using additional resources such as hazard detector and forwarding hardware (EX → EX, and Mem → EX) all data-hazards in *P* can be eliminated without using stalls; FALSE
(c) There is no control hazard in the above code snippet *P*; TRUE
(d) Using additional resources such as hazard detector, forwarding hardware, and code reshuffling, the execution of code *P* can be completed in 10 cycles. TRUE
(e) The clock-cycle time for this architecture is determined by the total delay of five stages. FALSE

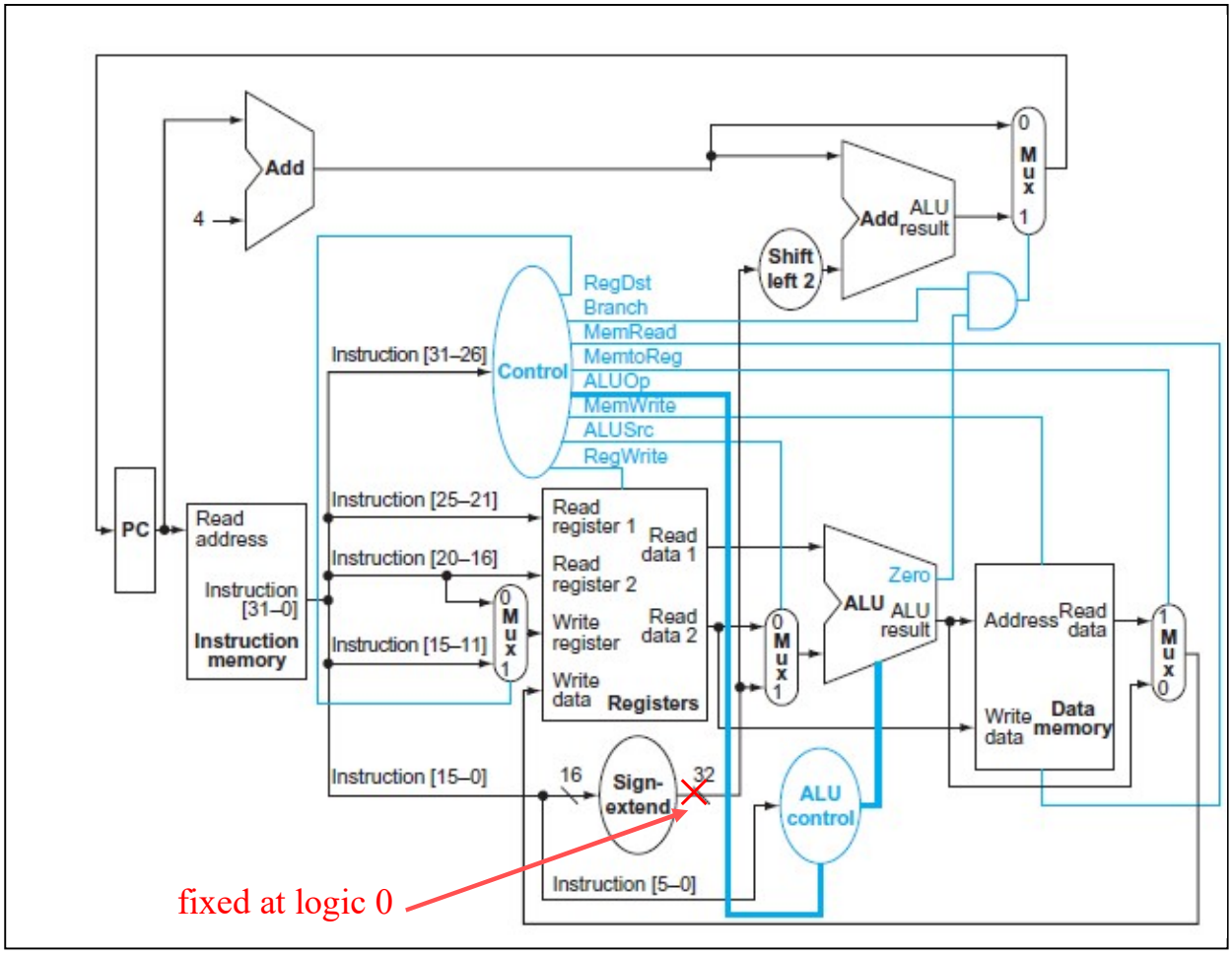

Figure 2: Fault in a single-cycle MIPS Processor

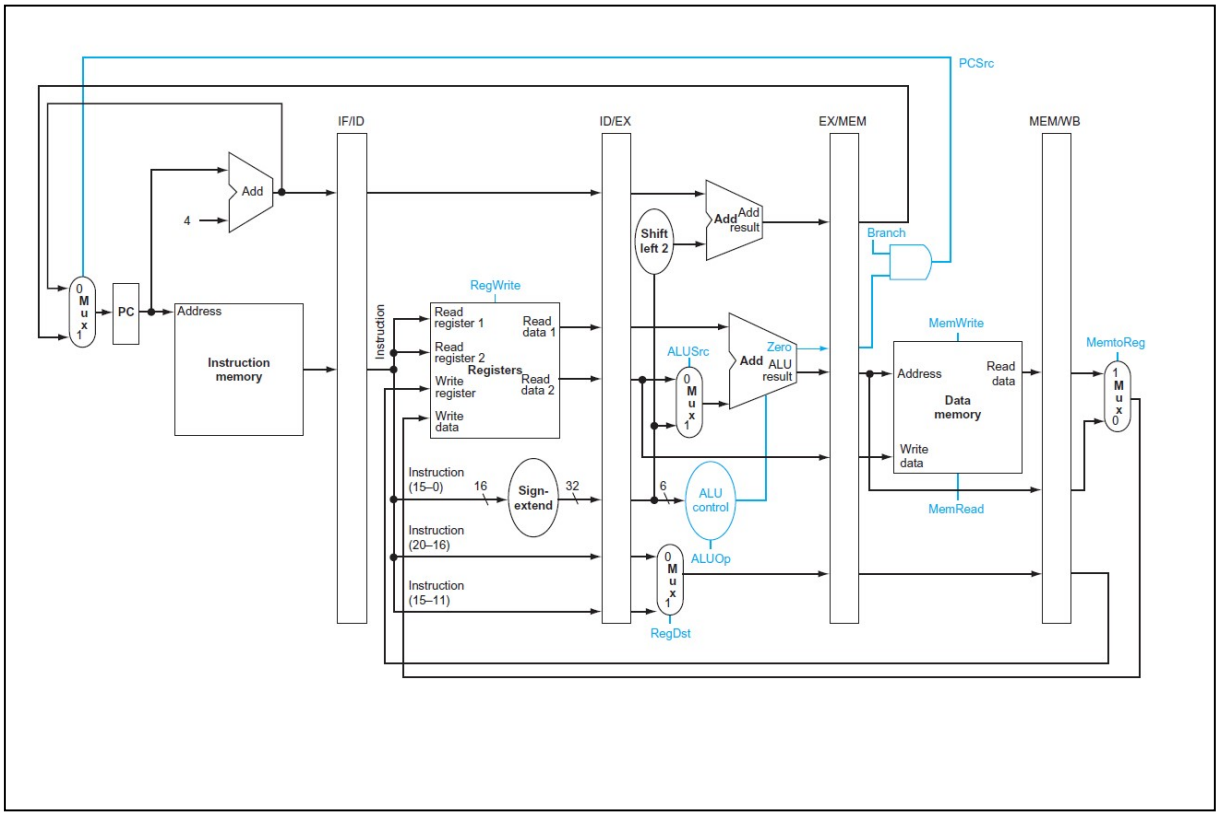

Figure 3: Five-stage pipelined implementation of a MIPS Processor