

- 1) (a) 80% of the process will be speed up by multi-core processor.

$$\text{Maximum Speed up} = \frac{T_e}{T_e(0.2 + \frac{0.8}{80})}$$

$$= \frac{T_e}{0.2T_e}$$

$$= \boxed{4.761}$$

- (b) Maximal speed up = $0.2 + (0.8) \times 80$
(Gustafson - bassis law)

$$= \boxed{64.2}$$

Reason: Amdahl's law is ~~based~~ based on assumption of a fixed problem size, i.e. workload does not change when performance is increased. Gustafson's law says size of problem changes to best exploit the competing power available. Therefore the formula and hence values of maximum speed up is different.

2) Loop will be executed only once.

$$\begin{aligned} \text{Total clock cycles} &= 5 + 3 + 3 + 3 + 3 + 3 + 3 \\ &\quad + 2 + 4 \\ &= 29 \text{ clock cycles.} \end{aligned}$$

$$\text{Time for 1 clock cycle} = \frac{1}{3.5} \text{ ns.}$$

$$\text{Total time} = \frac{29}{3.5} = \boxed{8.28 \text{ ns}}$$

3)

(a) C statement

`int f = (x == 0) ? z : y;`

(b)

~~beq \$t1, \$zero, L2~~

~~L1: add \$t4, \$t2, \$zero~~

~~L2: add \$t4, \$t3, \$zero~~

~~add \$t0, \$t4, \$zero~~

beq \$t1, \$zero, L1

move \$t0, \$t2

exit

L1: move \$t0, \$t3

exit: - - -

4) Ans: (d) More instruction count, less CPI, higher
die yield, better performance

5)

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move    $t2, $t1
bge     $t1, $zero, Exit
not      $t2, $t2
addi    $t2, $t2, 1


```

```


sra     $t2, $t1, 31
xor     $t2, $t1, $t2


```

```

sra     $t3, $t1, 31
xor     $t2, $t3, $t1
sub     $t2, $t2, $t3

```

\$t3 = -1 if $N < 0$
else 0.

6) (a) Program computes GCD of 2
no numbers stored in registers
\$a0 and \$a1.

(b) Output:

The value is: 3

7) The number 0x1234 in its binary representation has its MSB as 1. That means sign bit is 1. So during sign extension it will have all 1's in top 16 MSB's before adding. Instead for ~~correct~~ correct answer they should be 0. Final value stored in \$t0 =

0x1234

Instead of adding we should have written 0x1234

8) `lui $t1, 1`
`ori $t1, $t1, 5698`

9) Out of the 4 inputs at least 1 should be 1, others can be anything.

Full adder ~~(at least 1 bit)~~ ;
 both 0 for 1 case
 at least 1 bit 1 for 7 cases.

NOR
 0 for 3 cases
 1 for 1 case

NAND
 0 for 1 case
 1 for 7 cases.

Output will be 0 if all input bits are 0 else 1.

Cases when output will be 0.

$$= 3 \times 1 \times 1 = 3$$

Cases when it will be 1

$$= 256 - 3$$

$$= \boxed{253}$$

10)

toupper :

la \$t0, \$a0

loop :

lb \$t0, (\$a0)

beqz \$t0, exit

blt \$t0, 'a', no_change

bgt \$t0, 'z', no_change

addiu \$t0, \$t0, -32

sb \$t0, (\$a0)

no_change:

addiu \$a0, \$a0, 1

j loop

exit :

la \$a0, \$t0

jr \$ra.