

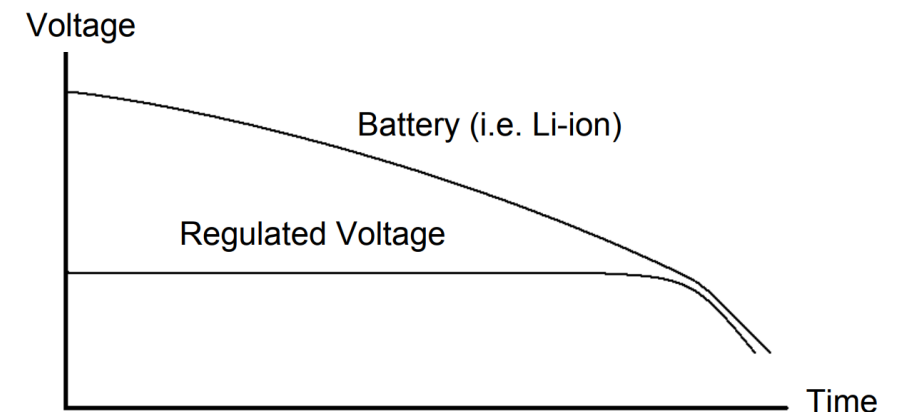
LOW DROPOUT VOLTAGE REGULATOR [LDO]

MENTOR- Dr. Sujata S Kotabagi

Power management

Why do we need power management?

- > Batteries discharge “almost” linearly with time. – To optimize the charging of batteries to be safe and extend their life. –
- > Circuits with reduced power supply that are time dependent.
- > To optimize the charging of batteries to be safe and extend their life.
- > Circuits with reduced power supply that are time dependent operate poorly. Optimal circuit performance can not be obtained
- > Mobile applications impose saving power as much as possible. Thus, the sleep-mode and full-power mode must be carefully controlled
- > Objective of a power converter is to provide a regulated output voltage



- The LDO act as a variable resistor that is placed between input power source and the load in order to drop and control the voltage applied to the load.

Compared to DC-DC switching regulators, LDOs are: –

- Of continuous operation
- Easier to use
- Cheaper solution
- But of Lower efficiency

LDO-Low dropout regulator

- An important building block in power management is the low drop-out (LDO) linear regulator which often follows a DC-DC switching converter, as shown in Fig. 1. It is used to regulate the supplies ripples to provide a clean voltage source for the noise-sensitive analog/RF blocks

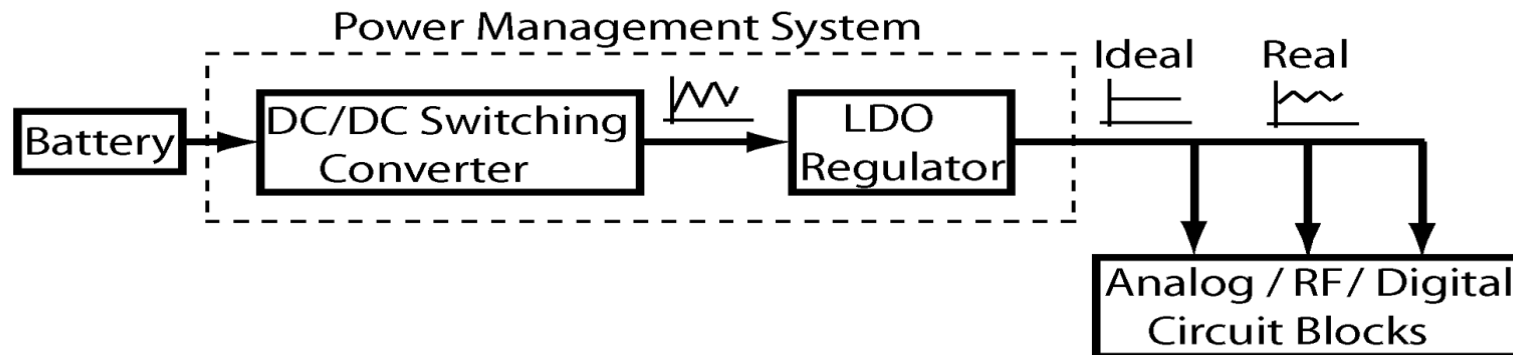
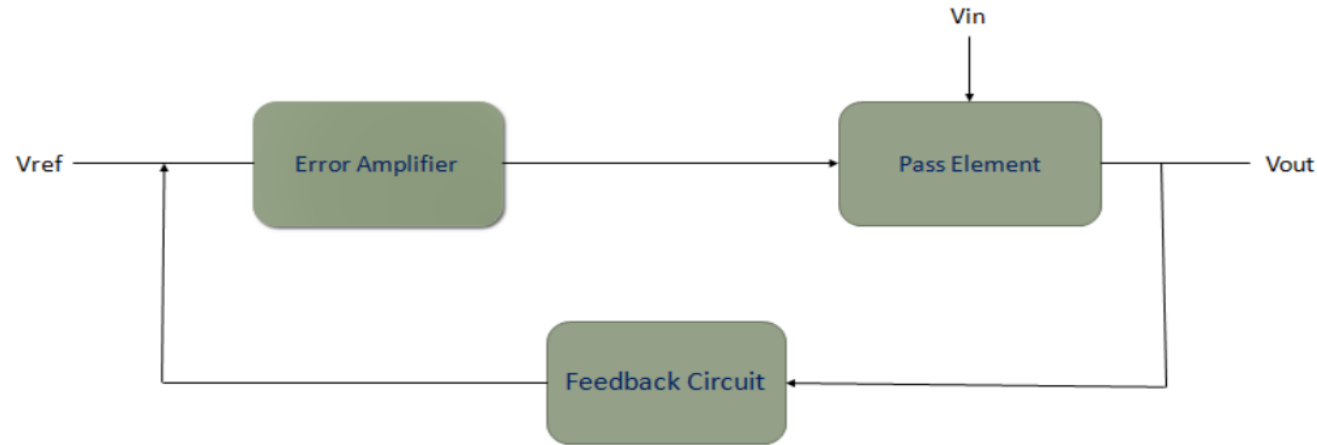


Fig. 1. Block diagram of typical power management system.

Block diagram of LDO



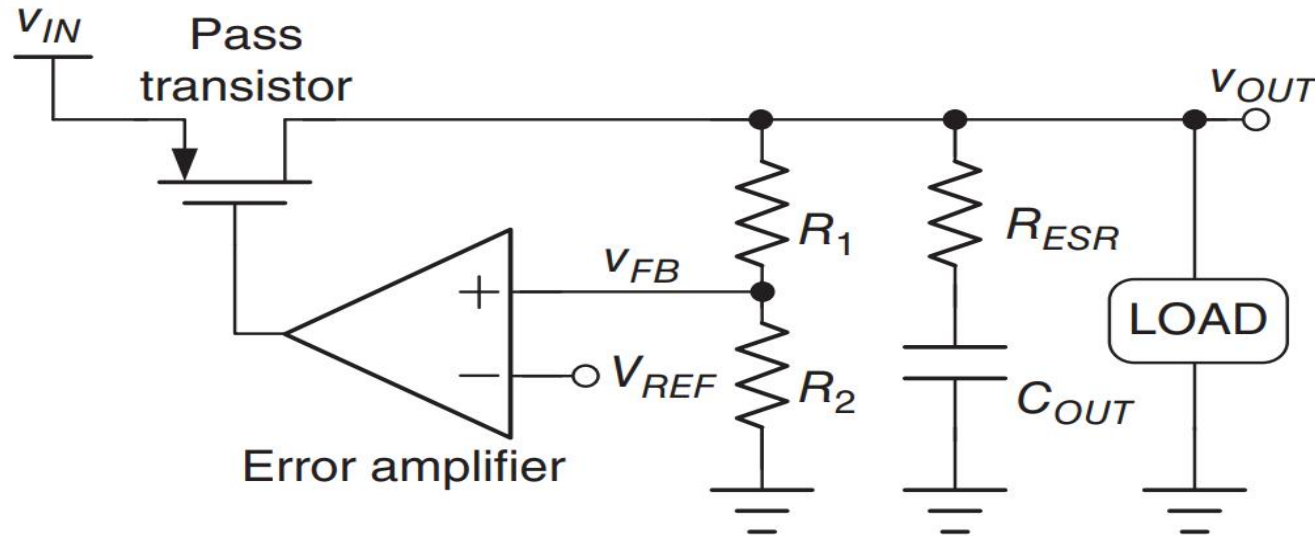
The feedback circuit is capable of scaling down the output voltage so that the error amplifier may compare it to the reference value.

The fundamental criterion for the error amplifier's design is that it draw as little current as feasible. Since the pass transistor's gate capacitance is significant, the amplifier's output resistance must be as low as reasonable.

The feedback circuit scaled-down output voltage is one input of the error amplifier, while the reference voltage is the other.

The error amplifier then modifies the resistance of the pass element based on the correlation. Reference voltage serves as the beginning point for every regulator since it establishes the operating point of the error amplifier. A band-gap type voltage reference is typically employed since it allows for operation at low supply voltages.

Structure of basic LDO architecture



Pass transistor

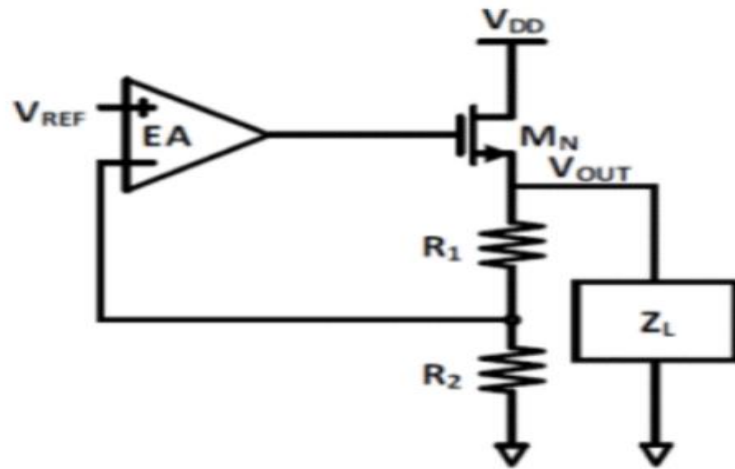
> load current will determine its size and thus layout

- Error amplifier

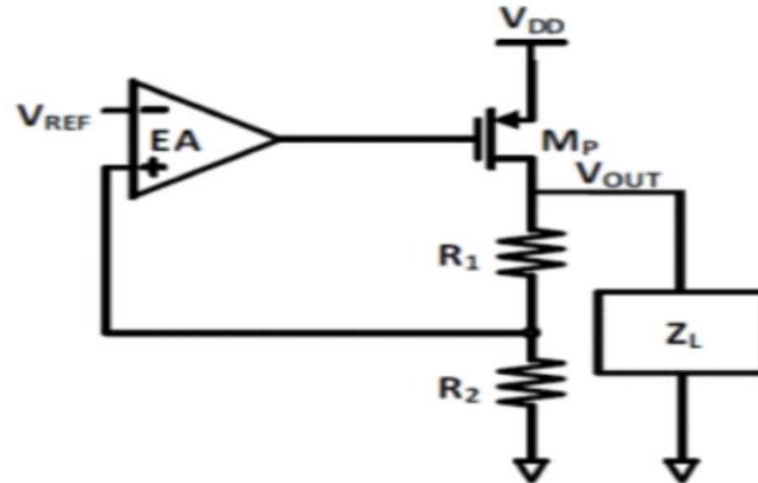
- The accuracy required by the LDO, determines the magnitude of the open loop gain.
- Single pole architectures are recommended for better and easier stability.
- The amp transient requirement is dependent on the stability i.e. gain and phase margins. There is a trade-off in making the PM high and speed of amp. This is also true for the Gain.
- Should have high PSRR

Types of LDO.

- > i) N channel MOSFET LDO.
- > ii) P channel MOSFET LDO.



N channel LDO

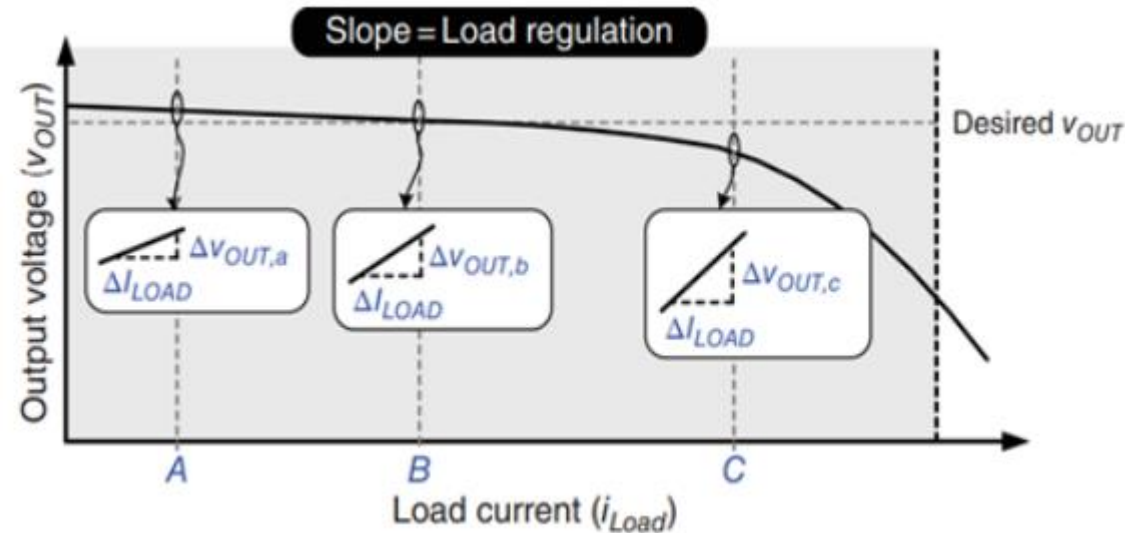


P channel LDO

Performance parameters:-

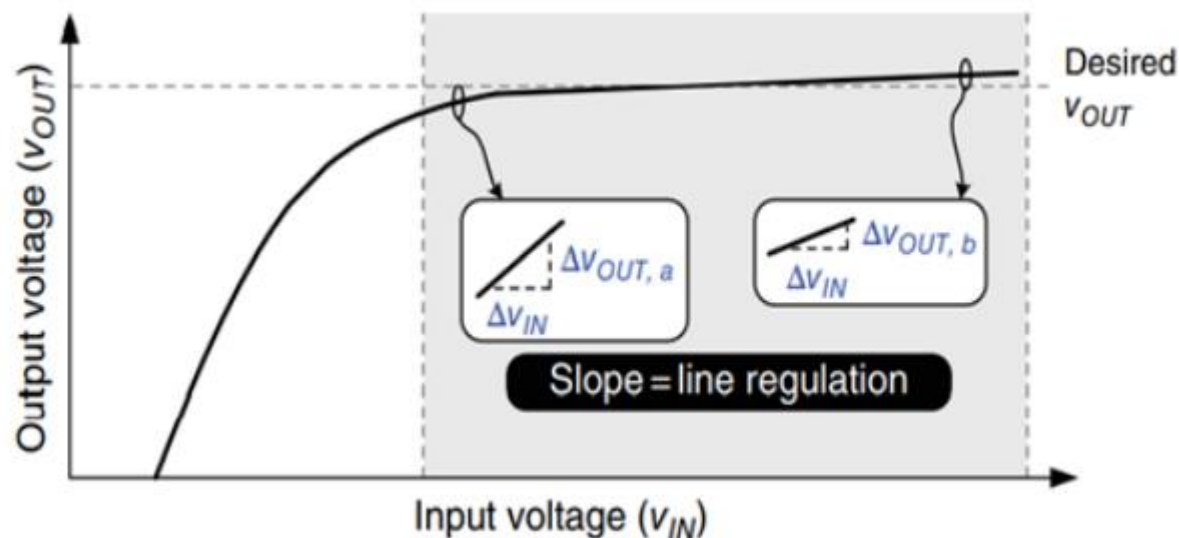
- **Load regulation**:-change in output voltage with respect to change in load current.

$$\text{Load regulation} = \frac{\Delta v_{out}}{\Delta I_{out}}$$



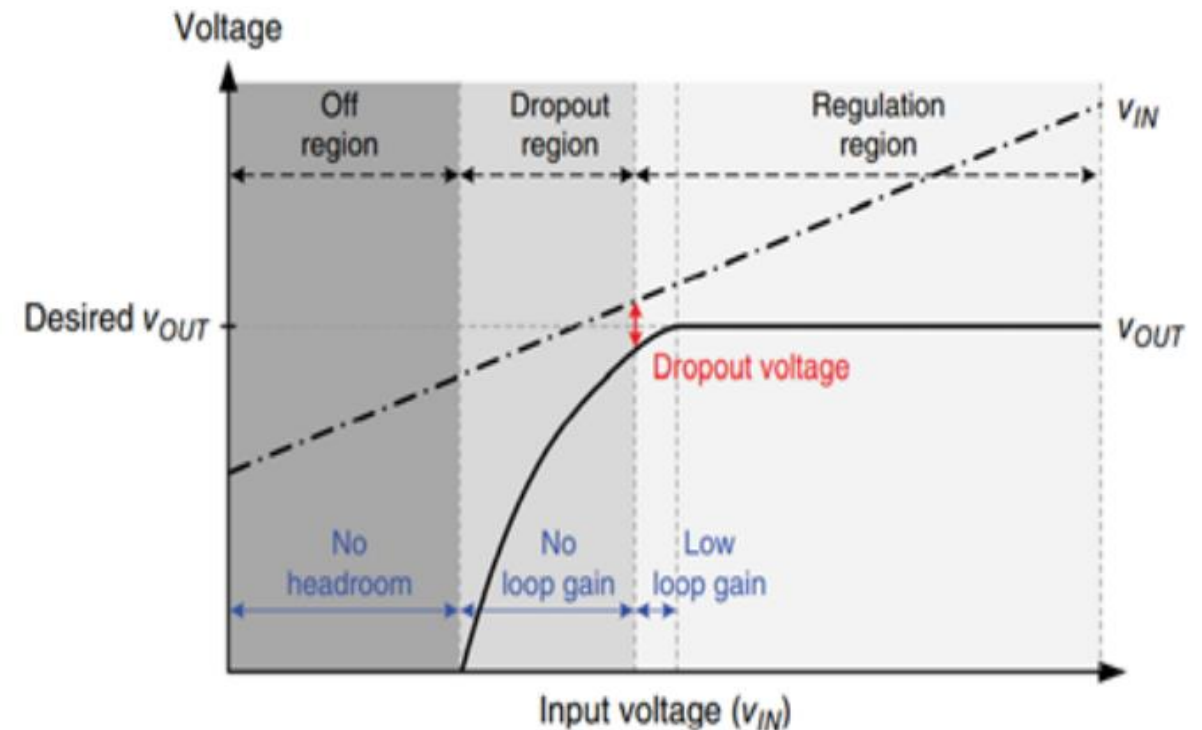
2.Line regulation:-change in output voltage with respect to change in input voltage.

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$



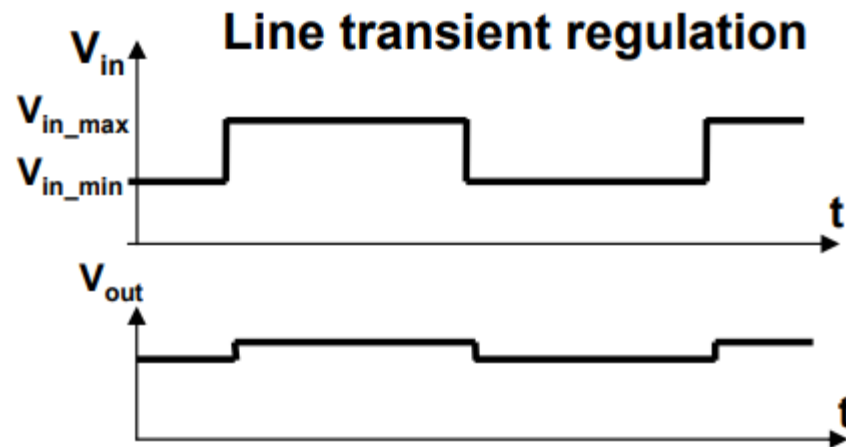
3. Dropout voltage (V_{do}):

- This is the difference between the minimum voltage the input DC supply can attain and the regulated output voltage.



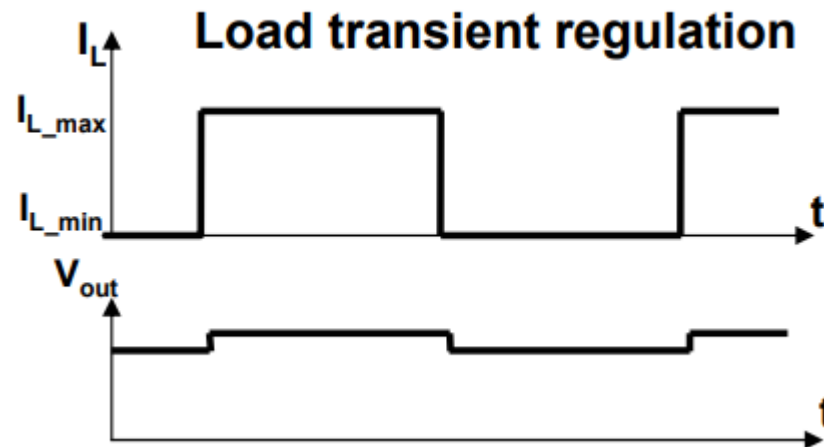
Line regulation:

- This is the variation in output voltage as supply voltage is varied from min. to max.
- Line regulation is a steady state parameter. increase in loop gain improves line regulation



LOAD REGULATION

- Load regulation: This is the variation in output voltage as current moves from min. to max . It defines the output resistance of ldo
- Ideally line regulation is zero



Efficiency

- It is the ratio of output power P_{out} to the ratio of input P_{in} .

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} * I_{load}}{V_{in} * I_{in}}$$

$$\eta = \frac{V_{out} * I_{load}}{V_{in} * (I_{load} + I_q)}$$

$$\eta = \eta_v * \eta_i$$

Power supply rejection ratio

- Power Supply Rejection Ratio or Power Supply Ripple Rejection (PSRR) is a measure of a circuit's power supply's rejection expressed as a log ratio of output noise to input noise.
- PSRR provides a measure of how well a circuit rejects ripple, of various frequencies, injected at its input. In the case of LDOs, PSRR is a measure of the regulated output voltage ripple compared to the input voltage ripple over a wide frequency range (10Hz to 1MHz is common) and is expressed in decibels (dB).
- The PSRR is very critical parameter in many audio and RF applications.

$$\text{PSRR} = \frac{\Delta V_{\text{IN}}^2}{\Delta V_{\text{OUT}}^2} = 10 \log \left(\frac{\Delta V_{\text{IN}}^2}{\Delta V_{\text{OUT}}^2} \right) \text{ dB}$$

BASIC LDO

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Virtuoso® Analog Design Environment L Editing: 01FE20BEC135 SEVEN_PACK1 schematic

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ADE L Search

AC DC Trans

Navigator

Instances
SEVEN_PACK1

Search

Name

- I2 (idc)
- M0 (P_18_MM)
- M1 (P_18_MM)
- M2 (N_18_MM)
- M3 (N_18_MM)
- M4 (N_18_MM)
- M5 (N_18_MM)
- M6 (P_18_MM)
- M7 (N_18_MM)
- M8 (P_18_MM)
- PIN0 (opin)
- R0 (res)
- R1 (res)

Property Editor

mouse L: schSingle SelectPt()

M: sevNetlistAndRun('sevSession2')

R: schHiMouse PopUp()

1(2)

Cmd: Sel: 0 Status: Ready T=27 C Simulator: spectre

Implemented LDO

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Virtuoso® Schematic Editor L Editing: 01FE20BEC135 LDO2 schematic

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Basic Search

Navigator

Instances
LDO2

Search

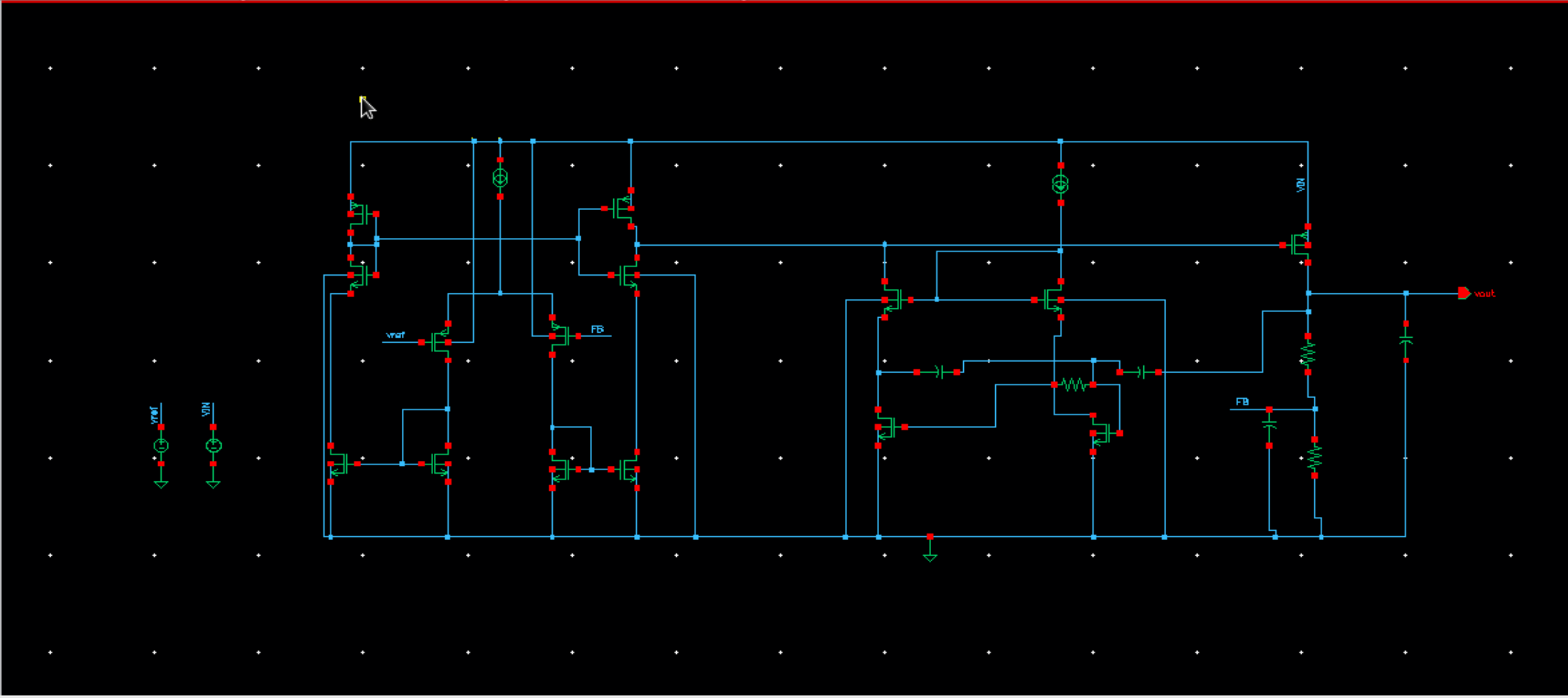
Name

- LDO2
 - C0 (cap)
 - C1 (cap)
 - C2 (cap)
 - C3 (cap)
 - I0 (idc)
 - I1 (idc)
 - M0 (P_18_MM)
 - M1 (N_18_MM)
 - M2 (P_18_MM)
 - M4 (P_18_MM)
 - M5 (P_18_MM)
 - M6 (N_18_MM)
 - M7 (N_18_MM)

Property Editor

mouse L: schSingleSelectPt() M: schZoomFit(1.0 0.9) R: schHiMousePopUp()

6(11) Cmd: Sel: 0



Changes from that IEEE paper with our LDO

Parameters	Paper LDO	Our LDO
Technology	350nm	180nm
Gain	50db	42db
Bandwidth	18KHz	10MHz
Phase	>45	54

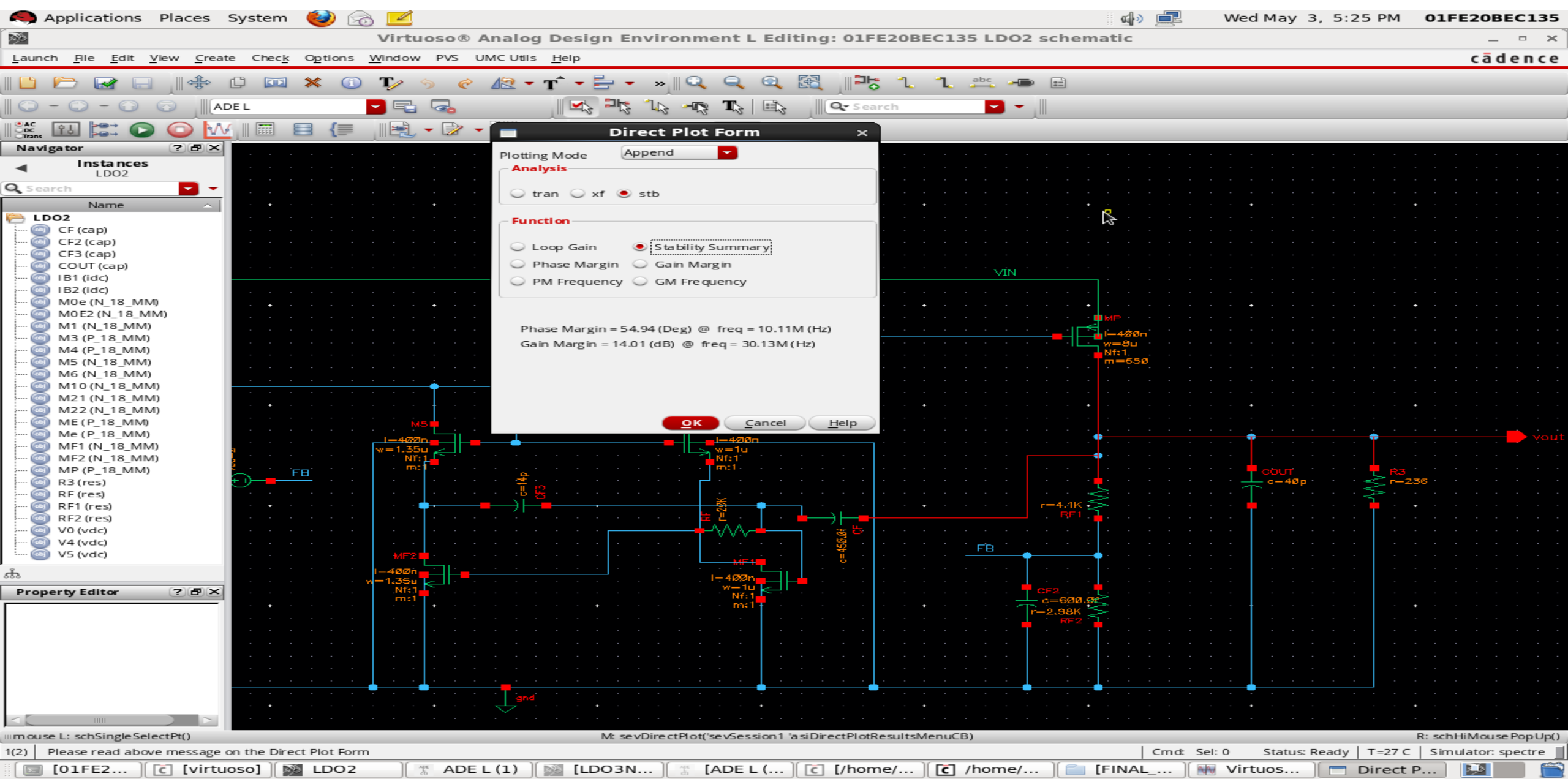
Gain and Phase



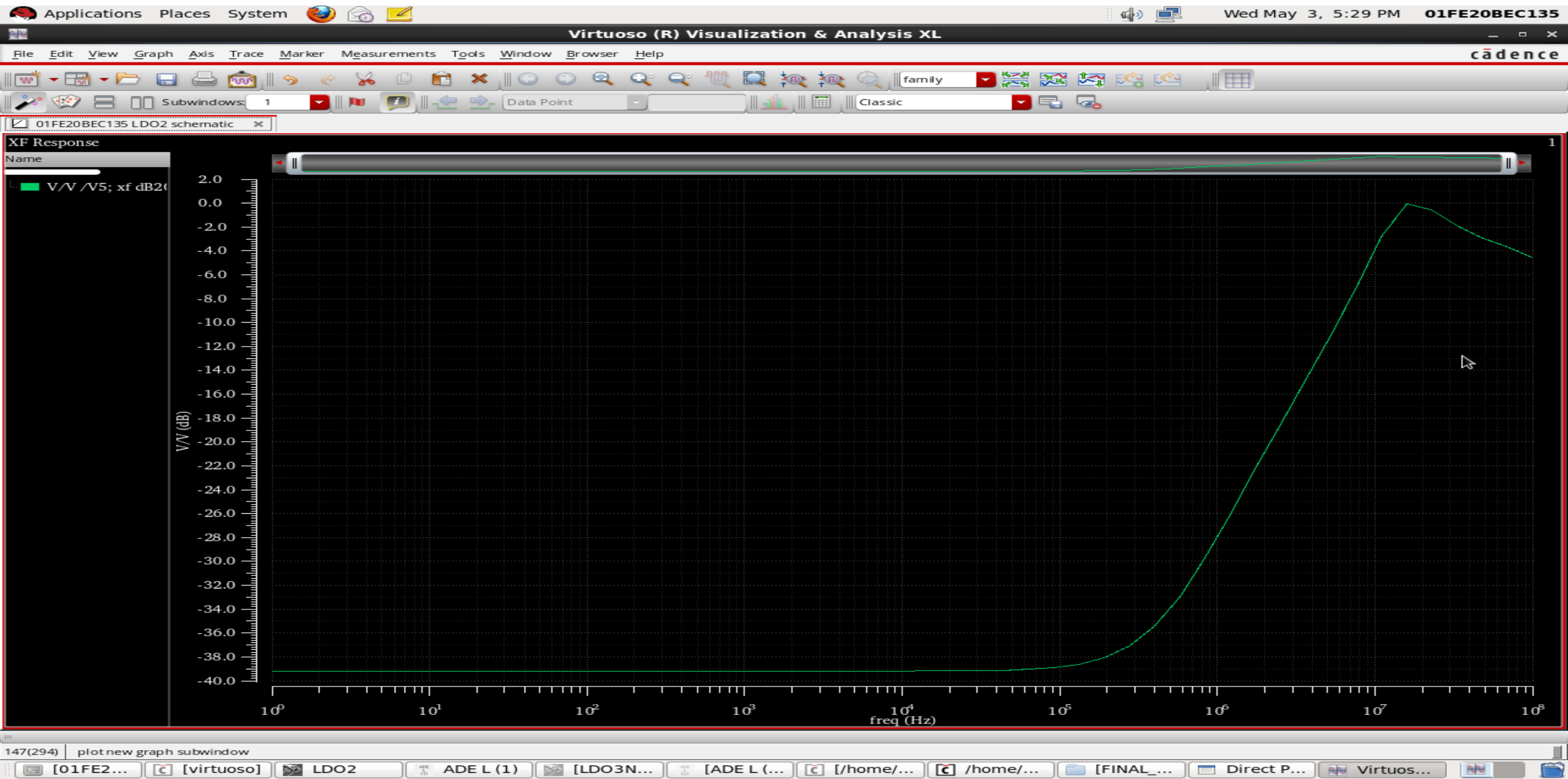
Basic Transient



Stability summary



Psrr



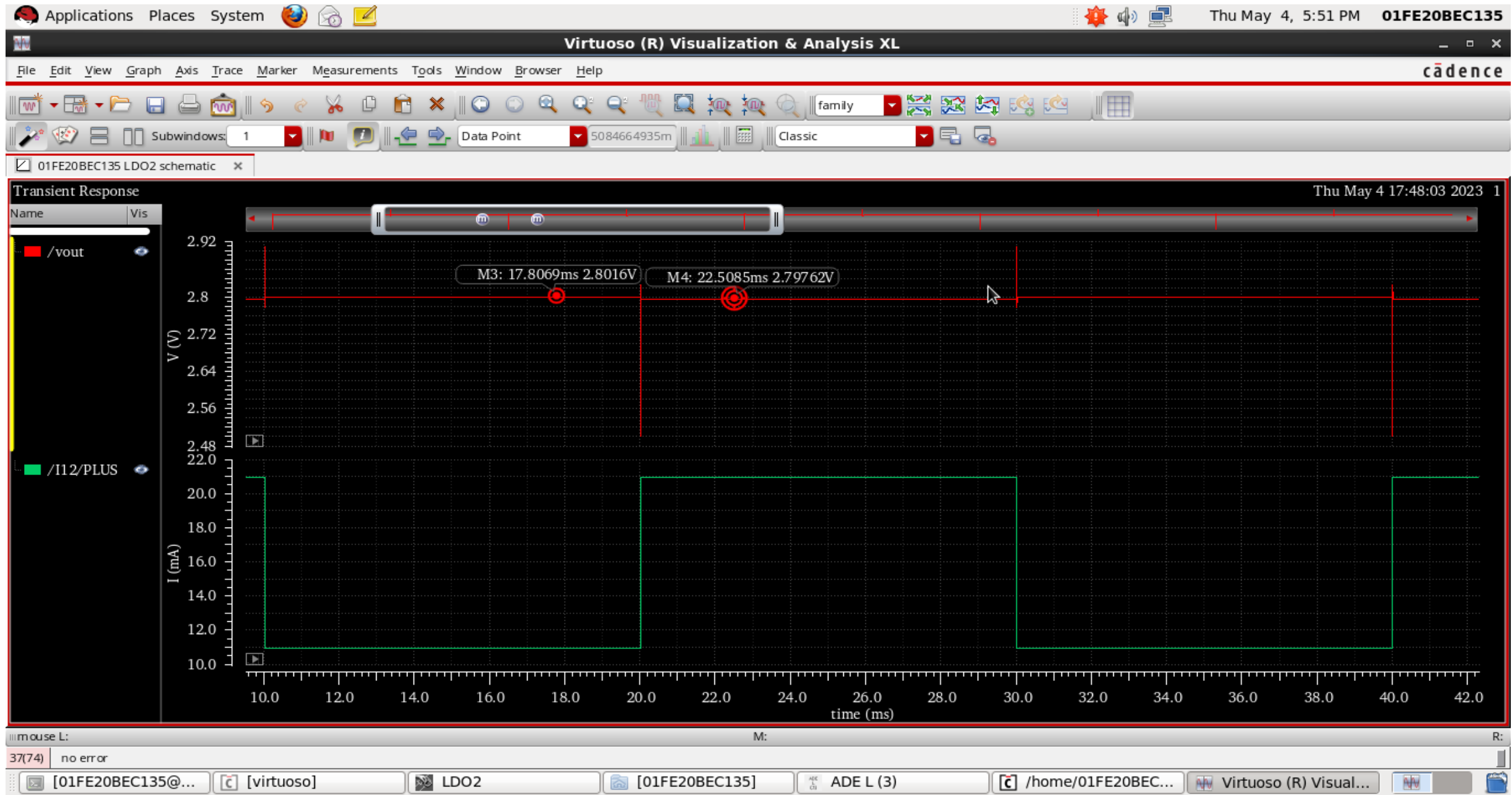
Variation at 0us



Line transient



Load transient



Calculations

Line transient

$$\begin{aligned}\text{Line Transient} &= \frac{\Delta V_{out}}{\Delta V_{in}} \\ &= \frac{2.80132 - 2.799}{3.1 - 2.9} \\ &= 11.6 \text{ mV/V}\end{aligned}$$

For every 1v variation in input,
varies Vout by 11.6mV

Load transient

$$\begin{aligned}\text{Load Transient} &= \frac{\Delta V_{out}}{\Delta I_{out}} \\ &= \frac{2.8014 - 2.7977}{(21 - 11)10^{-3}} \\ &= 37 * 10^{-5} \text{ V/mA}\end{aligned}$$

For every 1mA variation in Iout,
varies Vout by 3.7uV

Calculations(1M)

Line transient

$$\begin{aligned}\text{Line Transient} &= \frac{\Delta V_{out}}{\Delta V_{in}} \\ &= \frac{2.8052 - 2.8031}{3.1 - 2.9} \\ &= 10.5 \text{ mV/V}\end{aligned}$$

For every 1v variation in input,
varies Vout by 11.6mV

Load transient

$$\begin{aligned}\text{Load Transient} &= \frac{\Delta V_{out}}{\Delta I_{out}} \\ &= \frac{2.8078 - 2.8047}{(22 - 12)10^{-3}} \\ &= 31 * 10^{-5} \text{ V/mA}\end{aligned}$$

For every 1mA variation in Iout,
varies Vout by 3.7uV

Specification

Parameters	Values
Input voltage	3V
reference voltage	1.24V
regulated output	2.8V
Dropout	0.2V
load current	21mA
load capacitance	90p
line regulation	11.6mV/V
load regulation	0.00037V/mA
Gain	42db
Phase	54
Bandwidth	10MHz

Application in which our LDO can be used

- Low-power microcontrollers
- Battery-powered devices
- Audio and video equipment
- Communications equipment

Above Applications are for the LDO with low Gain and High Bandwidth.

As we have high Bandwidth which means that it will respond more quickly to changes in the input voltage. This could result in better transient response and stability.

THANK YOU