KLE Technological University

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School

of

Electronics and Communication Engineering

Senior Design Project Report

on

LAYOUT OF LOW DROPOUT VOLTAGE FOR PMIC

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Under the Guidance of

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SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled **" Layout of LOW DROPOUT VOLTAGE FOR PMIC"** is a bonafide work carried out by the student team of **"Sakshi Desai: 01FE20BEC125, Anusha Bagali:01FE20BEC132,Pallavi Myageri:01FE20BEC135, Suhas: 01FE20BEC175**. The project report has been approved as it satisfies the requirements with respect to the Senior Design Project project work prescribed by the university curriculum for BE (VII semester) in School of Electronics and Communication Engineering of KLE technological University for the academic year 2023-2024.

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1.

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We would like to thank our institute, KLE Technological University, Hubballi, for supplying us with all of the materials we needed to complete our project,"Layout of Low Dropout voltage for PMIC"We are grateful to our mentor, Dr. Sujata S Kotabagi and Mrs.Jency Cletus for entrusting us with this project, as well as Dr. Suneeta V. Budihal, Head of the School of Electronics and Communication, for guiding us in the right direction with this industrial-scale project. We would like to thank our guide for supporting us in completing our project successfully and for his ongoing encouragement. We would like to offer our heartfelt appreciation to the Prakalp team for their suggestions and help. We'd also want to thank our seniors for their continuous support in guaranteeing the successs of our initiative. Finally, we'd want to offer our appreciation to those who have indirectly helped us achieve the joy of project completion.

-Suhas,Anusha,Sakshi,Pallavi

ABSTRACT

The report presents an Layout of external capacitorless Low-dropout (LDO) regulator design as an alternative to the current bulky external capacitor LDO voltage regulators. Greater power system integration for system-on-chip (SoC) applications is made possible by eliminating the massive external capacitor commonly employed in standard LDOs. The output load can be as high as 40 pF, yet a compensation technique is provided that offers both a quick transient response and full range alternating current (ac) stability from 0- to 21-mA load current.The proposed design is implemented in UMC 0.18µm CMOS technology and was used to create the 2.8-V capacitorless LDO voltage regulator, which has a 3 V power supply with a 200 mV dropout voltage.According to experimental result, the suggested capacitorless LDO architecture resolves the typical load transient and ac stability problems that were present in earlier models.The Line and load regulation is 11.6(mV/V),37(mV/A) respectively.

The layout's total area is about 11.95sq.mm. The complete system is modelled and simulated in UMC 180nm technology on Cadence Virtuoso platform.

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Chapter 1

Introduction

An irregular input voltage is converted by a linear voltage regulator into a steady, low-noise DC output value. For linear voltage regulators to work properly, there must be a large voltage drop between the input and the output. This is ineffective and needs a high-voltage input power source. A linear voltage regulator with low dropout (LDO) performs effectively even when the output voltage is extremely close to the input value, increasing power efficiency. Reducing the incoming supply voltage to the lower voltage needed by the load is the first of the LDO's main tasks. The provision of a very low-noise voltage source, notwithstanding noise from the incoming power supply or load transients, is a second responsibility. Since noise isolation and emissions are important system components.

Low dropout (LDO) voltage regulators are designed to maintain an output voltage even when the input voltage varies. It is a sort of linear regulator used to control the voltage of a circuit. Even when the input voltage changes, it is designed to keep the output voltage within a particular range. LDOs are widely employed in power supply, battery chargers, and other sensitive electronic circuits. They are also utilised in automotive and aviation applications because they can maintain a consistent output voltage despite a broad variety of input voltages.

INDUSTRY is promoting entire system-on-chip (SoC) design solutions that incorporate power management. The research of power management strategies has risen dramatically in recent years, coinciding with a significant growth in the usage of portable, handheld battery-powered gadgets. Power management is to increase the device's power efficiency, resulting in longer battery life and running time. A power management system is made up of many subsystems such as linear regulators, switching regulators, and control logic [1]. To optimise the device's power usage, the control logic modifies the properties of each subsystem, such as turning the outputs on and off and modifying the output voltage levels.

This study focuses on voltage regulators with low dropout (LDO). LDO regulators are an important component of a power management system because they offer constant voltage supply rails. They are classified as linear voltage regulators with increased power efficiency. By replacing the common-drain pass element with a common-source pass element, the minimum needed voltage drop across the control device is reduced . Because LDO regulators have less voltage headroom in the pass element, they dissipate less power, making them more appropriate for low-voltage, on-chip power management solutions.

For stability, the typical LDO voltage regulator requires a somewhat high output capacitor in the single microfarad range. Due to the inability of existing design approaches to realise large microfarad capacitors, each LDO regulator requires an extra pin for a board-mounted output capacitor. To address this issue, presented a capacitorless LDO; however, this topology is unstable at low currents, rendering it unsuitable for real-world applications. The goal of this research is to eliminate the big external capacitor while ensuring stability under all operating situations. By removing the massive off-chip output capacitor, the board real estate and total cost of the design are reduced, and the design is now appropriate for SoC designs. The removal of the external capacitor necessitates the development of a sound compensation strategy for both transient responsiveness and alternating current (ac) stability.

A compensated 2.8-V, 50-mA capacitorless LDO regulator with a power supply of 3 V was constructed in a TSMC 0.35- m CMOS process using the MOSIS educational service, and the experimental results are reported.

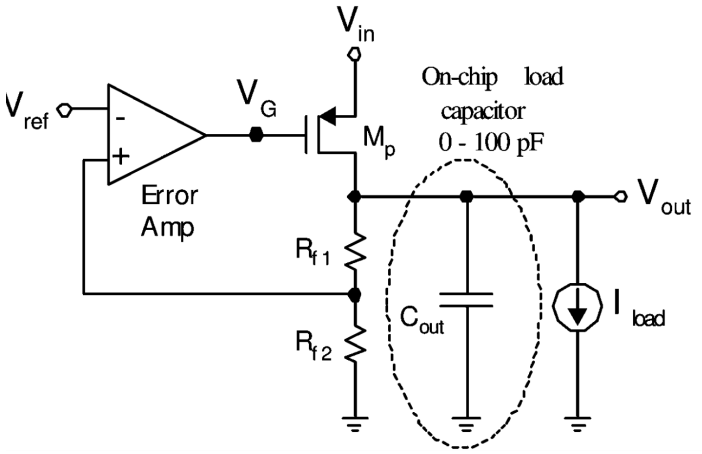


Figure 1.1: LDO voltage regulator without external capacitors

1.1 Motivation

A voltage regulator is probably required in more than 90 percent of products, making it one of the most widely used electrical components. A voltage regulator is essential unless everything can be powered directly from the battery or an external AC/DC adaptor. The objective of a voltage regulator is to keep the voltage in a circuit close to a preset level. Voltage regulators 7 are one of the most common electronic components because a power source frequently produces raw current that might otherwise kill one of the circuit's components

1.2 Objectives

LDO regulators are used to reduce the output voltage of a main supply or a battery With line and load variations, the output voltage is optimally steady, immune to changes in ambient temperature, and stable over time.:

1) Voltage regulator should be stable, noise free, constant, accurate.

2) Independent of load voltage.

3) It should have fast response.

4)Ultra low power consuming / low voltage drop across device.

5)Control signal should be continues in time.

6)Current flow should be continues in time.

1.3 Why Ldo?

Voltage regulators are divided into two major different types Switching regulator and linear regulator where LDO falls under Linear regulator. LD0 is a device which can bear a drop of very less voltage drop so shown in the figure below for instance consider that the input of the regulator is 2.5V and the required output is 1.8V and in the total regulator subsystem we consists of two regulators switching and linear the first block is switching regulator which can bare a large voltage drop compared to linear regulator so here the input is 3.6V is given to switching regulator here it drops the maximum voltage nearly it drops 1.6V i.e the output of the switching regulator is 2V and then this output voltage of switching regulator is fed to the linear regulator which provides the drop of 0.2V and then the output of the regulator is 1.8V, it is required at the beginning. Two things that we need to observe here is how ripples present in the inputs goes on to be a straight line there was a huge ripples at the input once it moves on to the switching regulator then its ripples were comparatively less as input and finally once it is fed towards the LDO then the ripples were totally eliminated and the output will be straight line

1.4 Uncompensated LDO

When the external capacitor is lowered by many orders of magnitude, most typical LDO performances suffer considerably. The lack of a big external output capacitor creates a number of design issues in terms of ac stability and load transient response. Traditional LDO regulators employ a large external capacitor to generate the dominant pole and offer an instantaneous charge source during rapid load transients . To compensate for the lack of a large external capacitor, a capacitorless LDO requires an internal rapid transient route. The basic capacitorless LDO regulator illustrated in Fig. 1 is explored in the fig 1.2 and fig 1.3

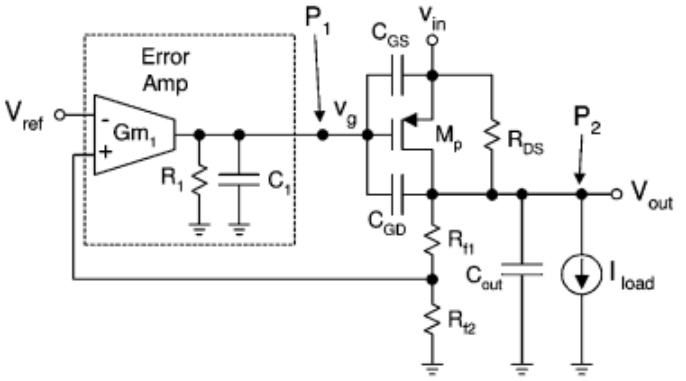


Figure 1.2: Equivalent circuit of LDO voltage regulator

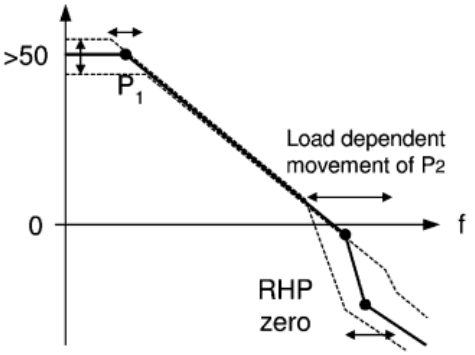


Figure 1.3: pole locations for uncompensated capacitorless LDO voltage regulator

1.5 Literatire survey

1. Full On-Chip CMOS Low-Dropout Voltage Regulator Robert J. Milliken, Jose Silva-Martínez, Senior Member, IEEE, and Edgar Sánchez-Sinencio, Fellow, IEEE

This paper provides the development of intricate equipment that requires high precision supply voltages, such as portable, battery-operated gadgets, has driven the growth of the low dropout regulator (LDO), due to its numerous advantages. Greater power system integration for system on-chip applications is made possible by the elimination of the external capacitor. The regulator that offers a quick transient response and a low quiescent current is shown in this paper.

2. A Capacitor-Free CMOS Low-Dropout Regulator With Damping-Factor-Control Frequency Compensation

For system-on-chip applications, a 1.5-V 100-mA capacitor-free CMOS low-dropout regulator (LDO) is introduced to save board space and eliminate extra pins. Using the improved LDO structure's damping-factorcontrol frequency correction, Even in capacitor-free operation, the proposed LDO offers great stability and quick line and load transient responses.

3. CMOS 0.35 µm Low-Dropout Voltage Regulator using Differentiator Technique 1Shailika Sharma, 2Himani Mittal, 1.2Electronics Communication Department, 1,2JSS Academy of Technical Education,Gr. Noida, India

This paper is a review paper to full on chip CMOS Low dropout voltage regulator. The 2.8-V LDO Voltage regulator (SoC) with a 200mV dropout in 0.35 µm CMOS technology with a load current of 50mA in the presence of 100 pF load on chip. A better transient analysis and fast turn on response is obtained. This architecture is composed by having a compensation scheme to provide better stability.

4. A low noise, high PSR low-dropout regulator for low-cost portable electronics Karim EL KHADIRI and Hassan Qjidaa Université Sidi Mohamed Ben Abdellah Faculté des sciences

A low noise, high PSRR low was presented in this paper. Results demonstrate that the proposed LDO's low noise, low quiescent current, ultra-low noise, high PSRR, and low dropout linear r require no substantial off-chip capacitor, making it appropriate for portable devices.

1.6 Problem statement

To design an Layout of LDO for PMIC applications, which provides constant output of 2.8V and a load current of 21uA to drive RF circuits for the input voltage range from 3V.

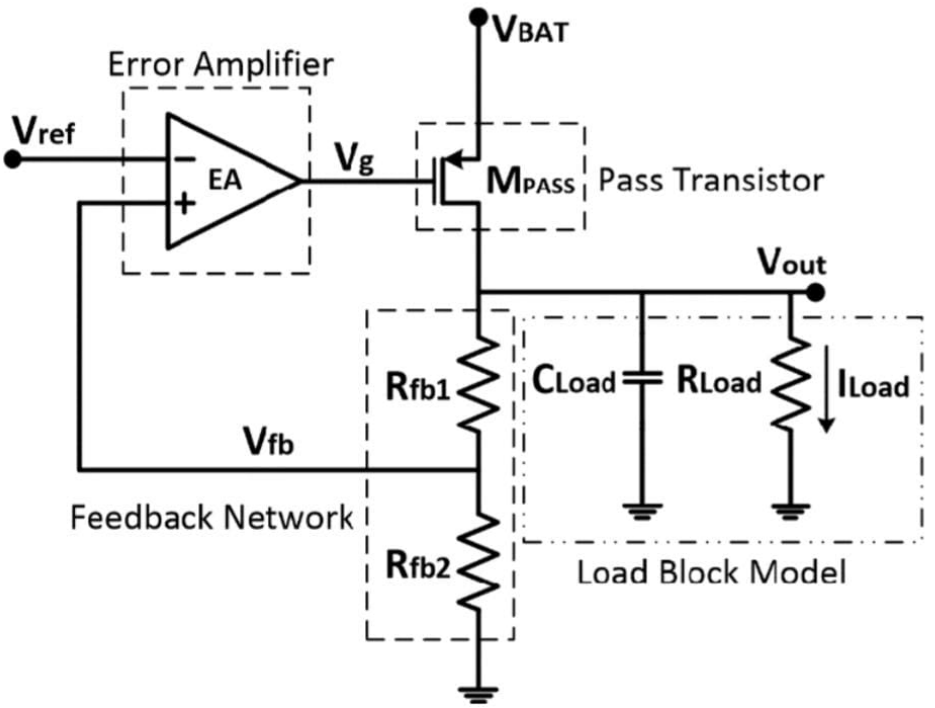
1.7 Project Planning

First we started with testing the LDO in ideal conditions by using vcvs (ideal op-amp) in cadence.We got the expected results, then we get in to the original design. We designed an 7 pack op-amp for error amplifier and studied various paper related to design of LDO in order to understand the architecture which are being used. Out of those research papers we selected the one which had better architecture and control system analysis and matched our specifications.

Chapter 2

System design

2.1 Functional Block Diagram



2.2 Working of LDO

The reference voltage source, pass element, and error amplifier are the key components of the LDO. The pass element can be either a P-channel or an N-channel FET. As a result, it begins by passing the input voltage to the pass element (N-channel transistor).

The transistor then operates in a linear zone to lower the input voltage. This operation is repeated until the input voltage equals the desired output voltage. The error amplifier detects the resultant output voltage at this stage. The output and reference voltage are then compared by the error amplifier.

In addition, the error amplifier will change the gate of the FET to the proper working position. As a result, it aids in ensuring that the output voltage is precise. As a result, when the input voltage varies, the error amplifier adjusts the FET to maintain a constant output voltage.

When the operational circumstances are stable, what happens? The LDO will then function as a basic resistor. You may also use the Enable pin to switch on or off the regulator. When the LDO is not in use, this function helps users avoid using the battery.

2.3 Types of LDO

Their are two main architectural types of LDO

1.NMOS LDO

A voltage regulator circuit known as an NMOS LDO (Low Dropout Regulator) uses a single NMOS transistor as the primary control element. Even when the input voltage is close to the required output value, LDO regulators are frequently employed in electronic devices to give a stable and regulated output voltage from a higher input voltage source.

The NMOS transistor serves as a variable resistor to control the output voltage in the NMOS LDO. An NMOS transistor linked in series between the input and output terminals, together with a feedback loop, forms the foundation of an NMOS LDO.

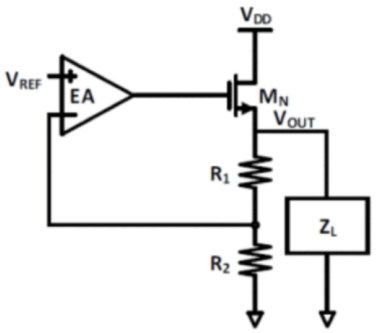


Figure 2.1: NMOS LDO

2.PMOS LDO

A voltage regulator circuit that employs a P-MOS transistor as the pass element is the P-MOS LDO (low-dropout) regulator. Even when there is a substantial voltage differential between the input and output.

2cmP-MOS LDO regulators often have lower dropout voltage than N-MOS (N-channel metal-oxide-semiconductor) LDO regulators, which is the minimal voltage difference needed between the input and output for the regulator to function properly. When a low dropout voltage is required for proper functioning and the input voltage is close to the desired output voltage, P-MOS LDOs are frequently employed.

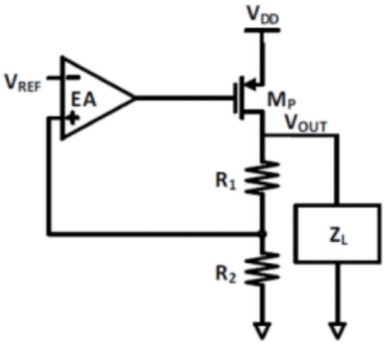


Figure 2.2: PMOS LDO

2.4 Proposed LDO topology

Proposed LDO topology including a differentiator for fast transient path

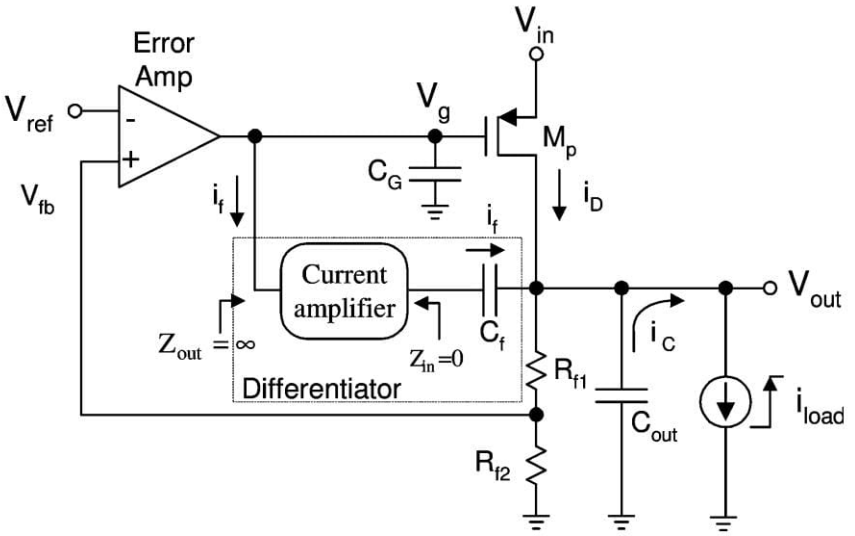


Figure 2.3: Proposed LDO

2.5 Transient Response Compensation

The relatively tiny and load-dependent on-chip output capacitor cannot be employed to form the dominant pole in an off-chip capacitorless LDO voltage regulator because the output pole must dwell at high frequency. As a result, the dominant pole must be located within the error amplifier control loop, and the transient control signal must pass via an internal dominant pole before or at the gate of the pass transistor.The most significant piece is the pass transistor, which delivers current to the load impedance and so generates

the required output voltage. The error amplifier's transistor gate capacitance and output resistance serve as a current to voltage converter and hence have an analogous propagation delay. The propagation delay increases as the gate capacitance increases. The effective input gate capacitance of a pass transistor is exceptionally high. As a result, a circuit that enhances the speed of charging the gate of the pass transistor is required.

The backbone of the architecture is an auxiliary fast loop (differentiator), which provides both a quick transient detector path as well as internal ac compensation. A unity gain current buffer monitors changes in output voltage as a current. The current is subsequently fed into the pass transistor gate capacitance through the coupling network. The compensating circuitry separates the poles in the same way as the normal Miller compensating method does while also increasing loop speed.

2.6 Final design

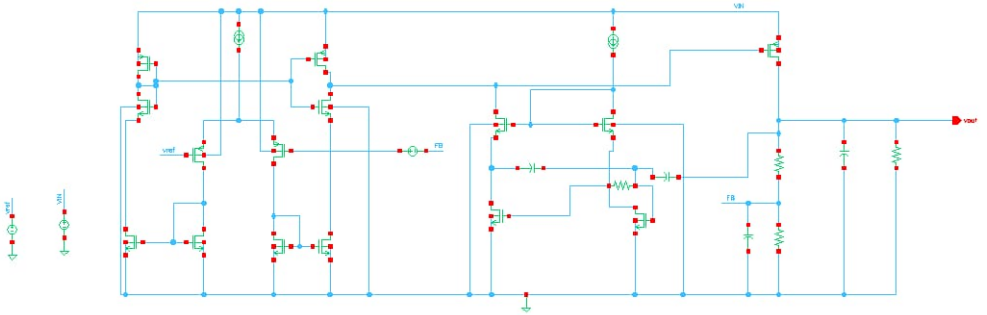


Figure 2.4: The proposed LDO's architecture's transistor level implementation

Chapter 3

Implementation details

3.1 Performance Parameters

1.Efficiency

2.Dropout Voltage

3.Line Regulation

4.Load Regulation

5.Power Supply Rejection Ration (PSRR)

3.1.1 Efficiency:

Efficiency is defined as a ratio of output power to the ratio of input power

$$Efficiency(\eta) = \frac{Pout}{Pin} (3.1)$$

3.1.2 Dropout voltage

The dropout voltage is the minimum voltage required across the regulator to maintain regulation.The input voltage minus the output voltage drop across the pass element equals to the output voltage

Vin ¡Vout+$V_{dropout}$

$V_{dropout} = I_o * R_{on}$

Where $I_o = load\ current$

$R_{on} = equivalent\ resistance\ of\ power\ transistor$

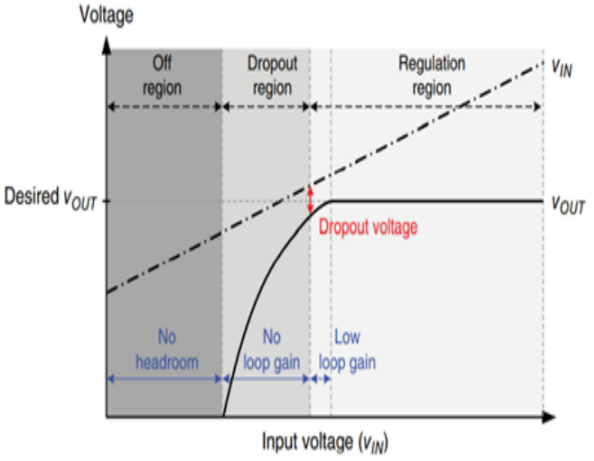


Figure 3.1: Dropout

3.1.3 Line Regulation:

Line regulation is a ability of the power supply to keep the output current constant while maintaining a steady output voltage despite changes in the input voltage Line regulation is calculated as follows:

$$Line\ Regulation = \frac{Change\ in\ output\ voltage(\Delta Vout)}{Change\ in\ input\ voltage(\Delta Vin)} (3.2)$$

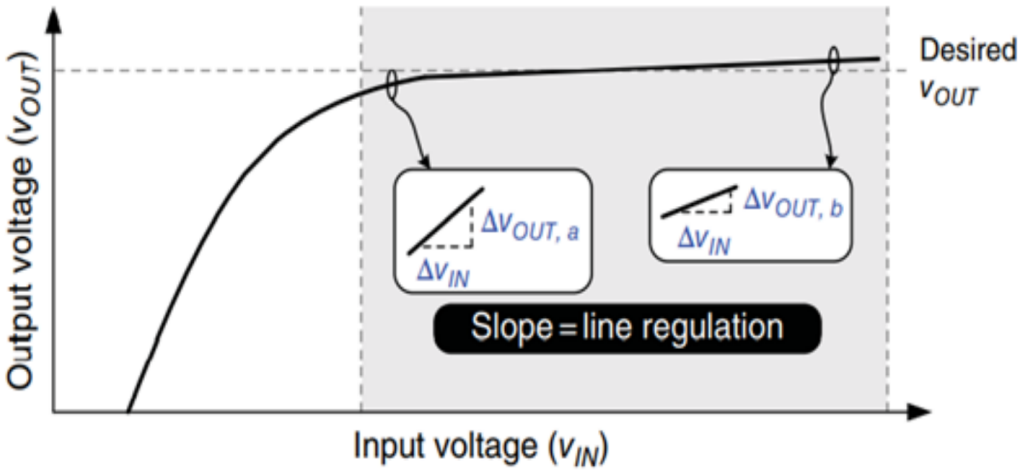


Figure 3.2: Line Regulation

3.1.4 Load Regulation:

The variation in output voltage caused by change in loading current

$$Load\ Regulation = \frac{Change\ in\ output\ voltage(\Delta Vout)}{Change\ in\ output\ current(\Delta I_{OUT})} (3.3)$$

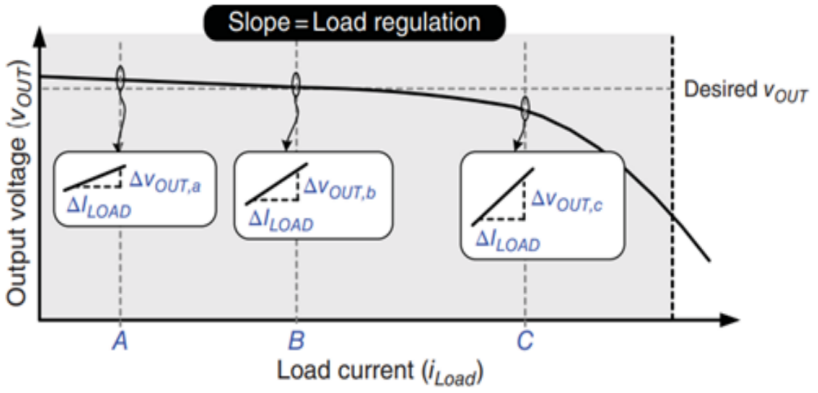


Figure 3.3: Load Regulation

3.1.5 Power Supply Rejection Ratio (PSRR):

!ower supply rejection ration(PSRR)is a term used to describe an electronic circuit's ability to supress any power supply variations in its output signal.It is sometimes referred toas supply-voltage rejection ratio.The formula is as follows:

$$PSRR = 20\ log \frac{\Delta Vout(ac)}{\Delta Vinp(ac)dB} (3.4)$$

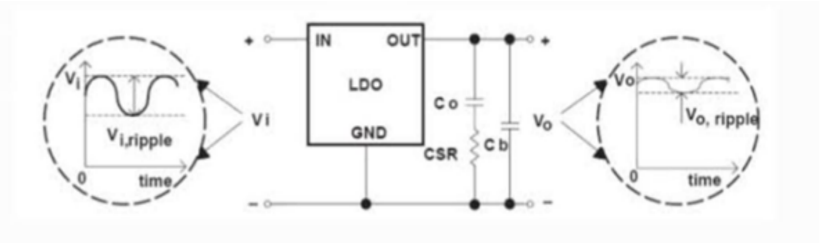


Figure 3.4: Power supply rejection ratio

3.2 Specification

Technology	CMOS 0.35µm	CMOS 0.18µm
Pass Element	Common Source	Common Source
$I_{max}(mA)$	50	21
V_{OUT}	2.8v	2.8v
$V_{DROP}(mV)$	200	200
$C_{out}(pF)$	0-100	0-40
Bandwidth	220KHz	10MHz
Loop gain(dB)	50	42
Phase Margin(°)	45	54
Line Regulation(mV/v)	10	11.6
Load Regulation(µV/mA)	26	37
PSSR (db)	31	1

Chapter 4

Results and discussions

4.1 Result Analysis

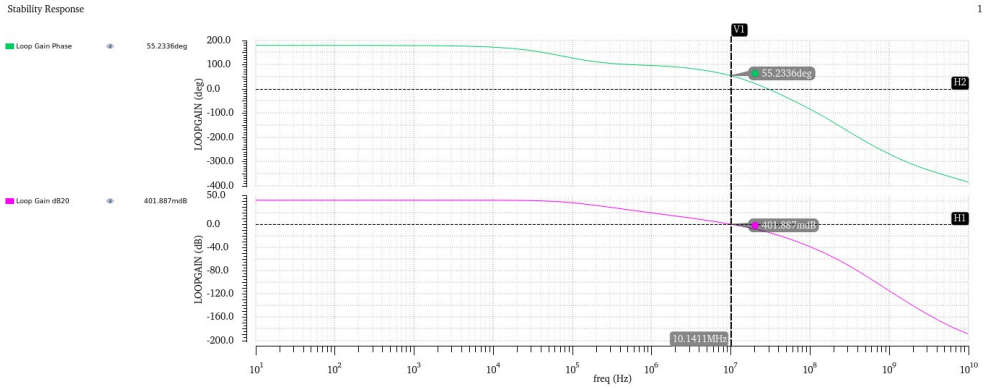


Figure 4.1: GAIN AND PHASE MARGIN

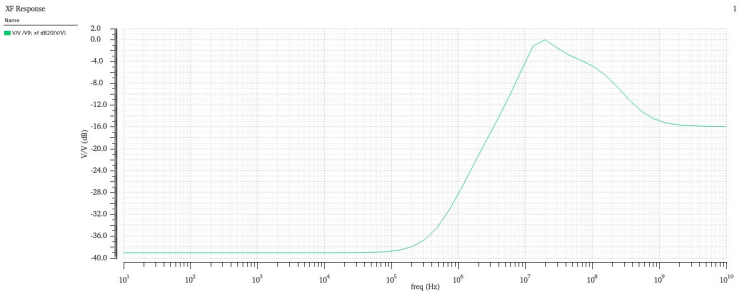


Figure 4.2: PSRR

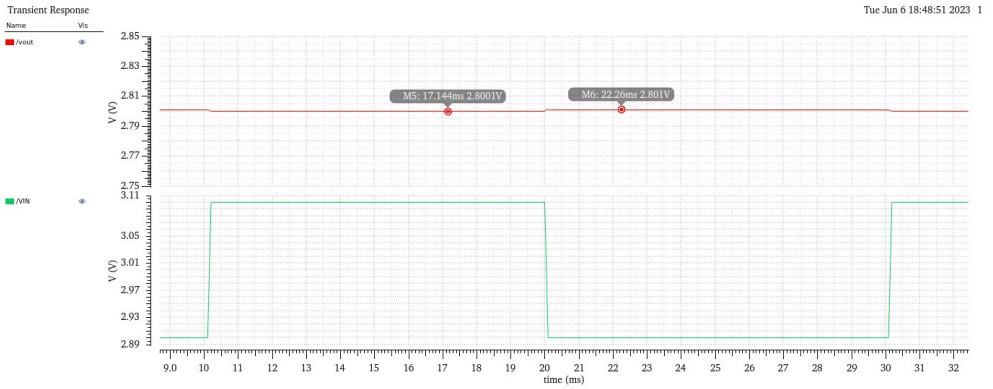


Figure 4.3: LINE REGULATION

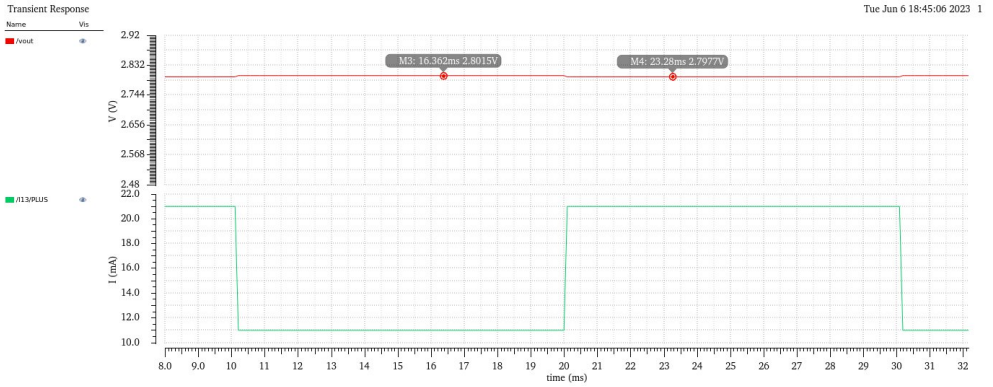


Figure 4.4: LOAD REGULATION

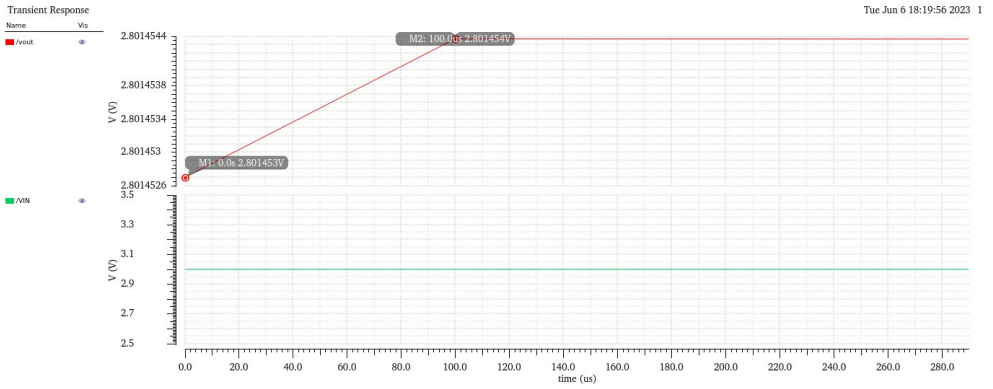


Figure 4.5: TRANSIENT RESPONSE

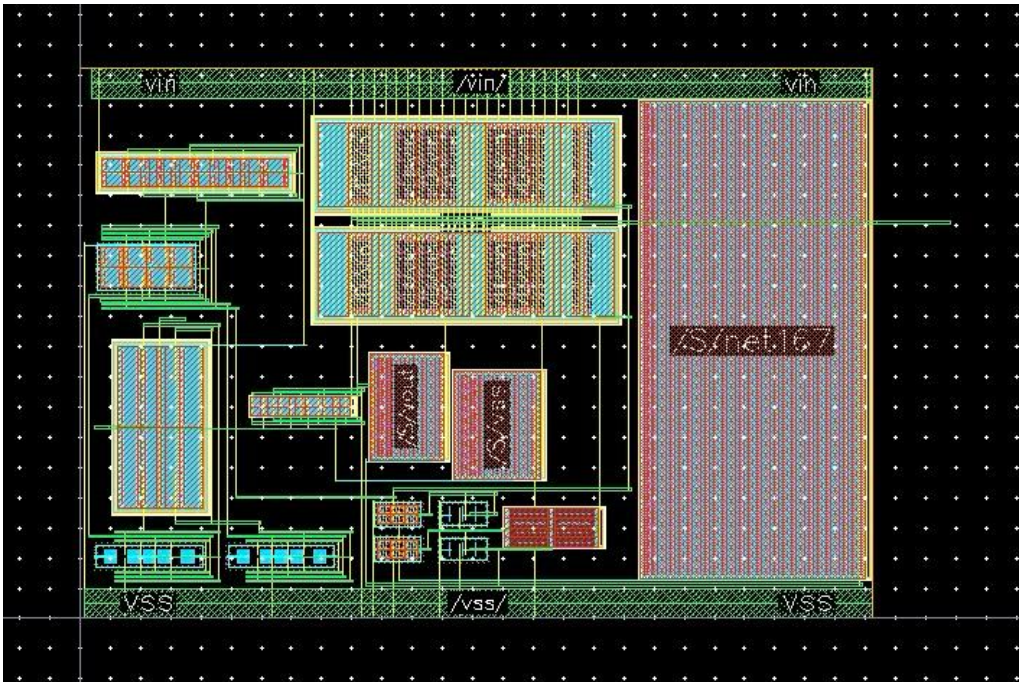


Figure 4.6: Layout of Low Dropout Regulator

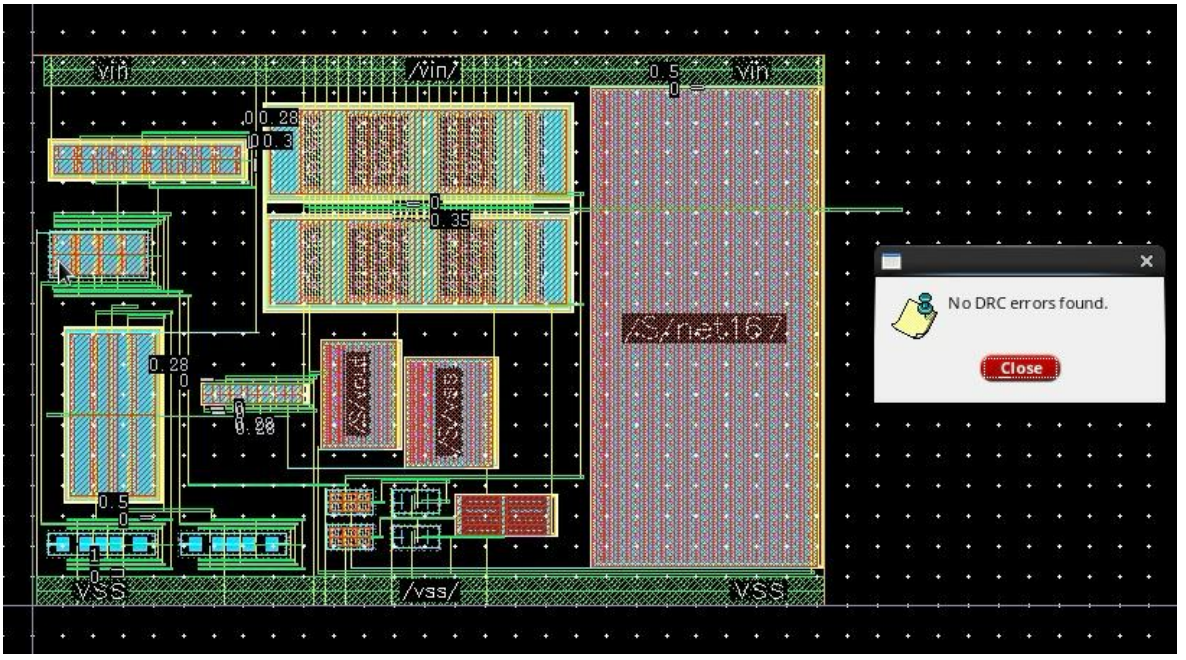


Figure 4.7: DRC clear Layout of Low Dropout Regulator

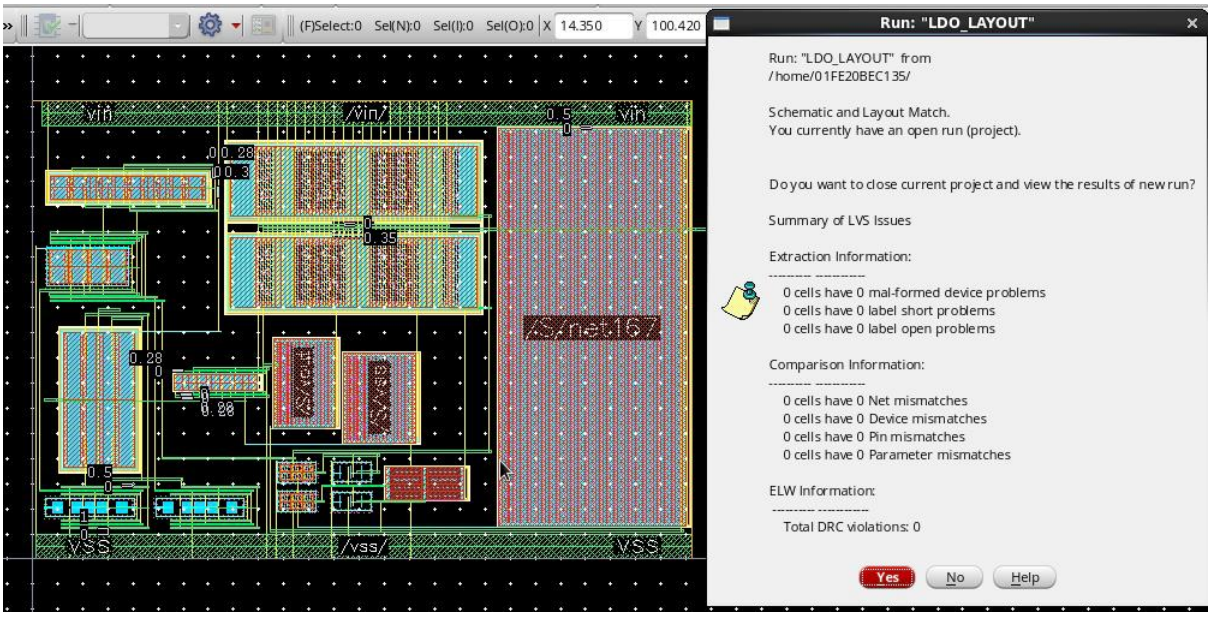


Figure 4.8: LVS clear Layout of Low Dropout Regulator

Chapter 5

Conclusions and future scope

5.1 Conclusion

The experimental findings demonstrate that the proposed LDO voltage regulator performs better in terms of transient response and ac stability than existing external capacitorless LDO regulators. The internal compensating capacitors are as small as 7 pF while the load capacitor can be as large as 40 pF in the worst case possible. As long as the load capacitance value stays within the specified bounds imposed by the positioning of the second pole, stability is unaffected by it. The recommended regulator uses less energy and also has a rapid settling period and low dropout voltage. The reduced board area, pin count, and cost of the proposed off-chip capacitorless full CMOS LDO regulator would be advantageous for SoC designs.

5.2 Future scope

IoT devices, wearable electronics, mobile devices, automotive electronics, renewable energy systems, industrial automation, medical devices, and aerospace/defense are just a few of the many applications that LDO regulators will be used for in the future. The demand for effective voltage regulation and power management solutions offered by LDO regulators will increase as technology develops and power requirements rise.

5.3 Application

LDO is a significant part of appliances falling in the categories of

1] Energy harvested power management IC.

2] Consumer Electronics

3] Automotive Systems

4] Industrial Automation

5] Telecommunications

6] Medical devices

7] Aerospace and defense

Chapter 6

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