DS 221 Quiz

Points: -/10

1. Assume a floating-point normalized representation similar to IEEE 754 representation. This representation has 1 bit for sign, 4 bits for exponent with bias 8 and 3 bits for mantissa. Compute the largest positive floating point number that can be represented with this format. *

   (01110111) base 2 = (120) base 10

2. In the IEEE 754 format with 32 bits, show the binary representation for -2178.375 *

   1100 0101 0000 1000 0010 0110 0000 0000 (32 bits)

3. Consider a 8-way set associative cache of size 64k bytes, block size of 32 bytes, and memory address of 32 bits. Find the total number of index bits required. *

8

4. Consider a 16-way set associative cache of size 256K bytes, block size of 32 bytes, and memory address of 64 bits. Find the number of tag bits required. * 📖

50

5. 1.   Consider a matrix-matrix multiplication program written in C in which the matrices are of type double, where the size of a double is considered to be 8 bytes. The program multiplies a 4x4 matrix A with a 4x4 matrix B to produce a 4x4 matrix C. Matrices A, B and C are stored in memory one after the other, and matrix A starts at address 0. Let the size of a block be 32 bytes and the size of memory address be 16 bits. Consider a 2-way set associative cache of size 256 bytes. Find the total number of cache misses for the **kij variant** of matrix-matrix multiplication for the entire program. * 📖

128 misses

6. For the same matrix-matrix multiplication and the same configuration of memory addresses, cache configuration and other parameters in the above question, imagine that memory addresses are split into (index, tag, offset) instead of the (tag, index, offset) organization we have seen in the class. Find the cache hit ratio. Explain your answer. * 📖

The cache hit ratio will be 25%. In such a case, all elements of all three arrays will map to the exact sa