
STM32
CubeMX

1. Description

1.1. Project

Project Name	EMU150_333
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	11/05/2020

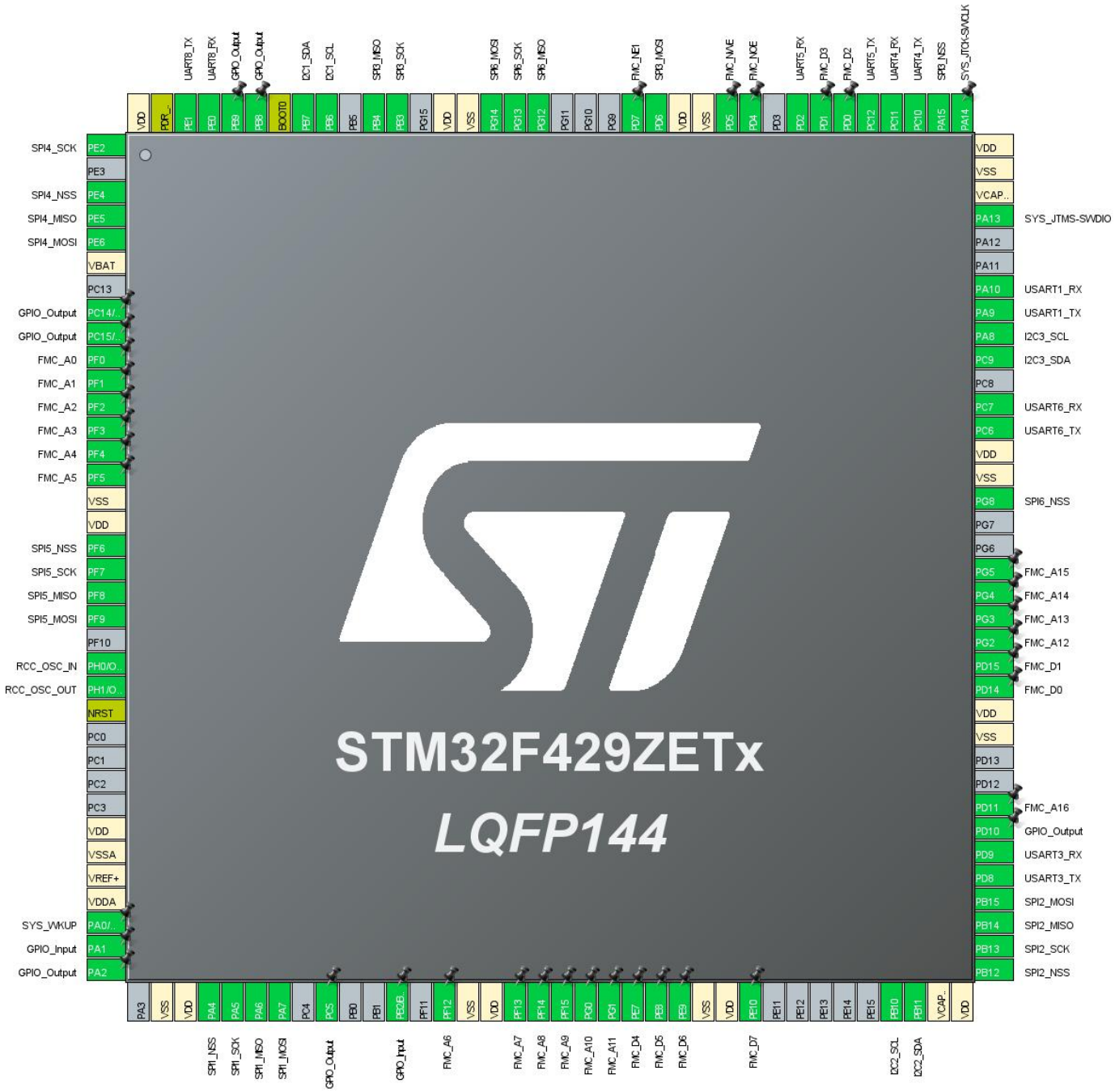
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZETx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

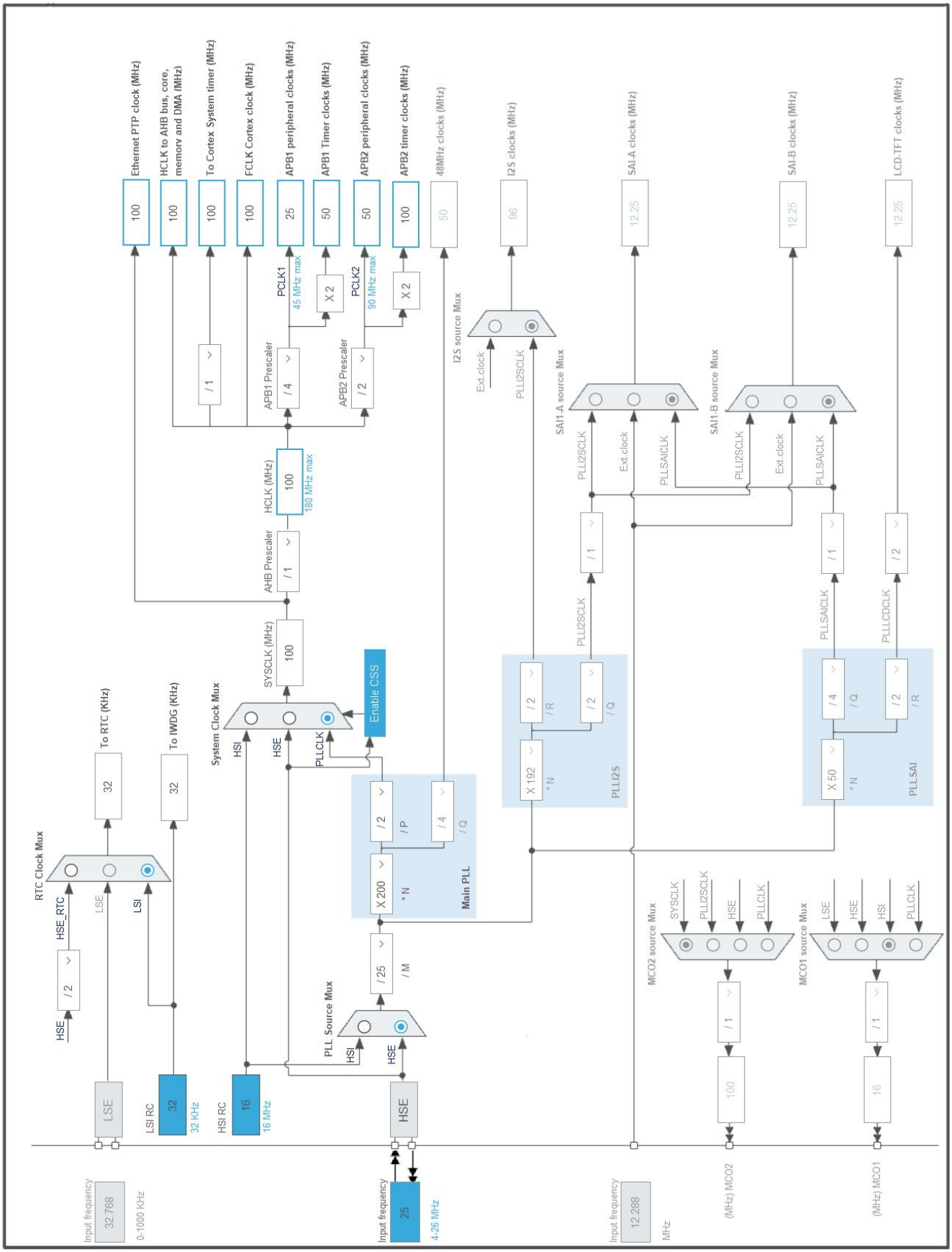
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
3	PE4	I/O	SPI4_NSS	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
8	PC14/OSC32_IN *	I/O	GPIO_Output	
9	PC15/OSC32_OUT *	I/O	GPIO_Output	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	SPI5_NSS	
19	PF7	I/O	SPI5_SCK	
20	PF8	I/O	SPI5_MISO	
21	PF9	I/O	SPI5_MOSI	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	SYS_WKUP	
35	PA1 *	I/O	GPIO_Input	
36	PA2 *	I/O	GPIO_Output	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI1_NSS	
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
45	PC5 *	I/O	GPIO_Output	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	PB2/BOOT1 *	I/O	GPIO_Input	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
69	PB10	I/O	I2C2_SCL	
70	PB11	I/O	I2C2_SDA	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	SPI2_NSS	
74	PB13	I/O	SPI2_SCK	
75	PB14	I/O	SPI2_MISO	
76	PB15	I/O	SPI2_MOSI	
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
79	PD10 *	I/O	GPIO_Output	
80	PD11	I/O	FMC_A16	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
88	PG3	I/O	FMC_A13	
89	PG4	I/O	FMC_A14	
90	PG5	I/O	FMC_A15	
93	PG8	I/O	SPI6_NSS	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	USART6_TX	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
97	PC7	I/O	USART6_RX	
99	PC9	I/O	I2C3_SDA	
100	PA8	I/O	I2C3_SCL	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15	I/O	SPI3_NSS	
111	PC10	I/O	UART4_TX	
112	PC11	I/O	UART4_RX	
113	PC12	I/O	UART5_TX	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2	I/O	UART5_RX	
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	SPI3_MOSI	
123	PD7	I/O	FMC_NE1	
127	PG12	I/O	SPI6_MISO	
128	PG13	I/O	SPI6_SCK	
129	PG14	I/O	SPI6_MOSI	
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SPI3_SCK	
134	PB4	I/O	SPI3_MISO	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	
140	PB9 *	I/O	GPIO_Output	
141	PE0	I/O	UART8_RX	
142	PE1	I/O	UART8_TX	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	EMU150_333
Project Folder	C:\Users\jinho\STM32CubeIDE\workspace_1.4.0\EMU150_333
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_FMC_Init	FMC
4	MX_IWDG_Init	IWDG
5	MX_RTC_Init	RTC
6	MX_SPI1_Init	SPI1
7	MX_SPI2_Init	SPI2
8	MX_SPI3_Init	SPI3
9	MX_SPI4_Init	SPI4
10	MX_SPI5_Init	SPI5
11	MX_SPI6_Init	SPI6

Rank	Function Name	IP Instance Name
12	MX_UART5_Init	UART5
13	MX_UART8_Init	UART8
14	MX_USART1_UART_Init	USART1
15	MX_USART3_UART_Init	USART3
16	MX_USART6_UART_Init	USART6
17	MX_WWDG_Init	WWDG
18	MX_I2C1_Init	I2C1
19	MX_I2C2_Init	I2C2
20	MX_I2C3_Init	I2C3
21	MX_TIM6_Init	TIM6
22	MX_TIM7_Init	TIM7
23	MX_UART4_Init	UART4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZETx
Datasheet	DS9405_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

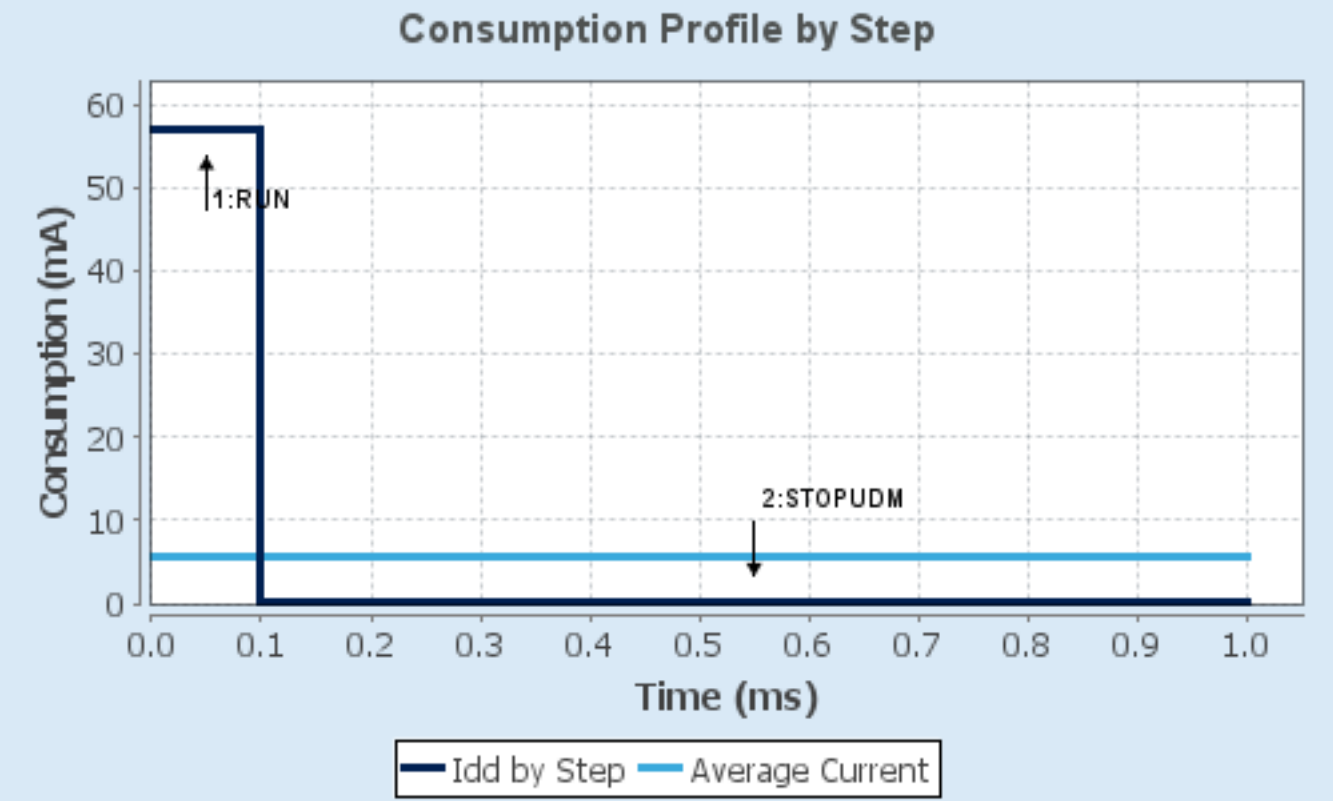
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	57 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	97.48	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
60
50
40
30
20
10
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: PSRAM

Address: 17 bits

Data: 8 bits

7.1.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	PSRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**0 ***
Data setup time in HCLK clock cycles	**1 ***
Bus turn around time in HCLK clock cycles	**2 ***

7.2. GPIO

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

General Call address detection	Disabled

7.4. I2C2

I2C: I2C

7.4.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.5. I2C3

I2C: I2C

7.5.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.6. IWDG

mode: Activated

7.6.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

7.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

7.8. RTC

mode: Activate Clock Source

7.8.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.9. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.10. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**12.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.11. SPI3

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**12.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.12. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.13. SPI5

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.14. SPI6

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.14.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

7.15. SYS

Debug: Serial Wire

mode: System Wake-Up

Timebase Source: TIM1

7.16. TIM6

mode: Activated

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.17. TIM7

mode: Activated

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.18. UART4

Mode: Multiprocessor Communication

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.19. UART5

Mode: Multiprocessor Communication

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.20. UART8

Mode: Multiprocessor Communication

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

Wake-Up Method	Idle Line

7.21. USART1

Mode: Multiprocessor Communication

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.22. USART3

Mode: Multiprocessor Communication

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.23. USART6

Mode: Multiprocessor Communication

7.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Wake-Up Method	Idle Line

7.24. WWDG

mode: Activated

7.24.1. Parameter Settings:

Watchdog Clocking:

WWDG counter clock prescaler	1
WWDG window value	64
WWDG free-running downcounter value	64

Watchdog Interrupt:

Early wakeup interrupt	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SPI2	PB12	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SPI3	PA15	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PD6	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI5	PF6	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI6	PG8	SPI6_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA0/WKUP	SYS_WKUP	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC14/OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC15/OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2/BOOT1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART3 global interrupt	true	0	0
UART5 global interrupt	true	0	0
USART6 global interrupt	true	0	0
UART8 global interrupt	true	0	0
Window watchdog interrupt	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI2 global interrupt	unused		
SPI3 global interrupt	unused		
UART4 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
TIM7 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
SPI5 global interrupt	unused		
SPI6 global interrupt	unused		

8.3.2. NVIC Code generation

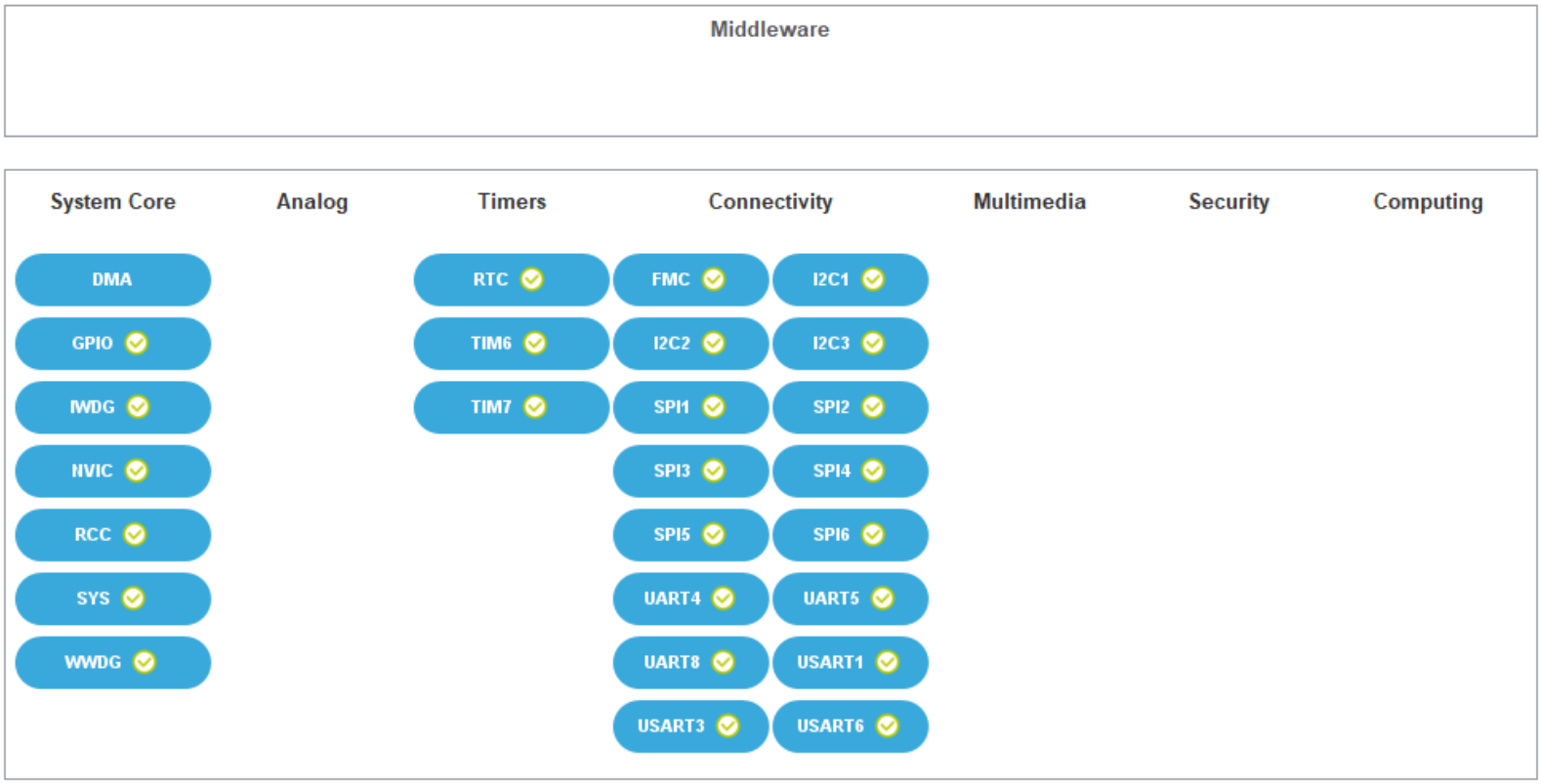
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
TIM1 update interrupt and TIM10 global interrupt	true	true	true
SPI1 global interrupt	true	true	true
USART1 global interrupt	true	true	true
USART3 global interrupt	true	true	true
UART5 global interrupt	true	true	true
USART6 global interrupt	true	true	true
UART8 global interrupt	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00071990.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00068628.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf

Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00161778.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00172465.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf