Tileboard update

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Tileboard update, 112020

Introduction and Summary

- Introduction to loopback design and problem for QSH loopback design discussed on 110420
- The issue of pin assignment for QSH detailed at the end of 110420 (P-N polarity issue)
- FPGA pins assigned without considering P/N polarity, given it's differential signal
- No success, realizing a potential issue in creation of HDL wrapper from BD.
- Decided not to touch BD and HDL wrapper, but change **only XDC (Pin assignment) constraint file**
- 4 to 5 pins out of 9 pins showing success (no error rate)

Structure of Presentation

- 1 Problem in BD edition and HDL wrapper
- 2 Strategy of only editing XDC file
- 3 QTH variation and terminal output understanding
- 4 QSH XDC assignment
- 5 result and interpretation

Problem in BD edition and HDL wrapper

- 1 **Problem in BD edition and HDL wrapper**
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Problem in BD edition and HDL wrapper

- Post-synthesis and Pre-Implementation step : I/O bank window preventing P-connected I/O port getting assigned to Negative differential leg and vice versa.
- Just assign P to P leg, and N to N leg given it's a differential signal. For instance,
  - QSH) F2 (HGCROC1_TRIG_IN_P2) - A8 (HGCROC1_TRIG_IN_N3)
    becomes
  - QSH) F2 (HGCROC1_TRIG_IN_P2) - A9 (HGCROC1_TRIG_IN_N3)
- Terminal output in next slide
- Result: still giving very erroneous number

Problem in BD edition and HDL wrapper - 2

- Screenshot of terminal output
- We see no improvement.

```
[HGCAL_dev@localhost ~]$ python ber_scan.py
0,1337573721,1281714087
0,192429899,2426857909
0,122247,2619165561
0,2197000031,422287777
0,2529057531,90230277
0,1037659592,1581628216
0,2619287745,63
0,2619287808,0
0,1901073711,718214097
10,1185319967,1377778657
10,169454804,2393643820
10,132832,2562965792
10,2149461319,413637305
10,2469631550,93467074
10,1063429067,1499669557
10,2563098618,6
10,2563098624,0
10,1984496973,578601651
20,1059347048,1503709080
20,174473426,2388582702
20,141157,2562914971
20,2158870025,404186103
20,2467040603,96015525
20,1132385473,1430670655
20,2563056119,9
20,2563056125,3
```

Problem in BD edition and HDL wrapper - 3

- To track down the source of the error, a simple QTH exercise done
- QTH BD's I/O for for bytegenerator 0 got reversed, and HDL created, and bitstream generated

Table	Output	Input
Name	HGCROC1-TRIG-IN-P(N)2	HGCROC1-TRIG-OUT-P(N)3
Name	HGCROC1-TRIG-OUT-P(N)3	HGCROC1-TRIG-IN-P(N)2

Table: QTH BD's reversed I/O table

- I get no error as expected, suggests simple BD edit works
- But QTH to QSH involves, I/O reversal, Polarity reversal, byte-generator (0-8) position mixing and so on...

Problem in BD edition and HDL wrapper - 4

- Current Workflow
  - To create new code, I/O ports are connected/dis-connected in BD
  - The BD is translated into Verilog code via HDL-wrapper
  - Verilog code gets synthesized (compiled)
  - Process above, especially HDL wrapper are executed in very deep-end level, out of my FPGA skill
  - Could bring unknown bugs in total transformation from QTH BD to QSH BD
- How can we get around the issue..?
- **Just leave the BD, and Verilog code**
- **And edit the XDC file's pin assignment to correspond QTH I/O port in FPGA to QSH I/O port in FPGA**

Strategy of only editing XDC file

- 1 Problem in BD edition and HDL wrapper
- 2 **Strategy of only editing XDC file**
- 3 QTH variation and terminal output understanding
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Strategy of only editing XDC file

- BD and Verilog code stays same as QTH
- Everything upto **Synthesis** is identical
- Just adjust XDC pinout file
- If you have

	Output [pin]	Input [pin]
QTH	fast-clk-p(n) [D7,D6]	HGCROC2-TRIG-OUT-P(N)3 [E5,D5]
QSH	fast-clk-p(n) [D7,D6]	fast-sig-p(n) [C9,B9]

Table: QTH,QSH XDC info

- In QTH XDC,
  PACKAGE_PIN E5 [get_ports HGCROC2_TRIG_OUT_P3]
  PACKAGE_PIN D5 [get_ports HGCROC2_TRIG_OUT_N3]

Strategy of only editing XDC file

- If you have

	Output [pin]	Input [pin]
QTH	fast-clk-p(n) [D7,D6]	HGCROC2-TRIG-OUT-P(N)3 [E5,D5]
QSH	fast-clk-p(n) [D7,D6]	fast-sig-p(n) [C9,B9]

Table: QTH,QSH XDC info

- In QSH XDC,
  PACKAGE_PIN C9 [get_ports **HGCROC2_TRIG_OUT_P3**]
  PACKAGE_PIN D5 [get_ports **HGCROC2_TRIG_OUT_N3**]
- In this way, BD can stay same but make the bitstream for QSH instead of QTH.

QTH variation and understanding

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QTH variation and understanding - 1

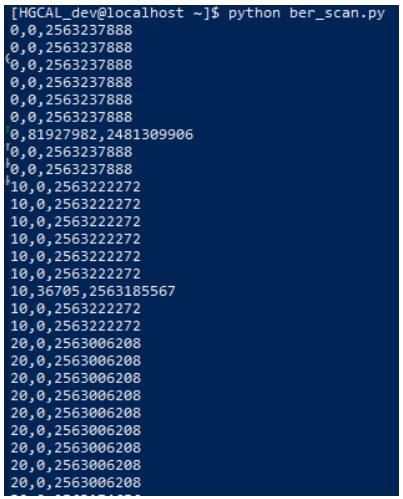
- Now, we can start creating QSH's XDC file.
- Before that, I tried various experiment in QTH, to better understand the terminal output info
  - 1 **QTHInverted**
  - 2 **QTHhalfInverted**
  - 3 **QTHwrongAssign**
- Each of items above taught me some useful information.
- Place of inversion discovered in Link : loopback-top.v at L76

QTH variation and understanding - 2

- After discovery of place of inversion, inverting differential signals in All bytegenerators tried

	0	1	2	3	4	5	6	7	8
Inv	Y	Y	Y	Y	Y	Y	Y	Y	Y

Table: Inversion table



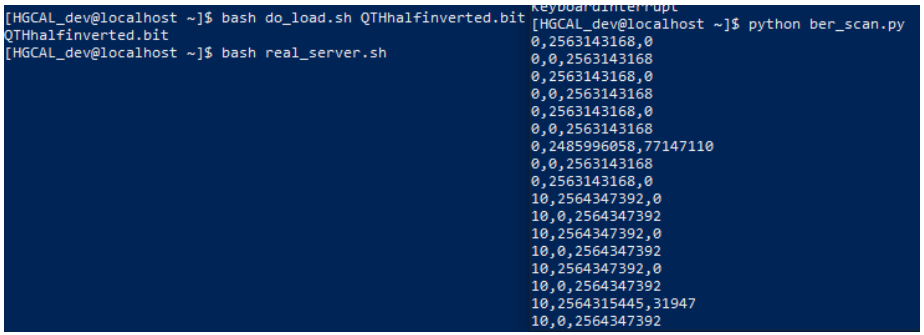
- When signals are inverted, the terminal reads the error rate received (0) in the second column and the data went out (2E10) in the third column

QTH variation and understanding - 3

- Inverting only odd number bytegenerators tried.

Inv	0 N	1 Y	2 N	3 Y	4 N	5 Y	6 N	7 Y	8 N

Table: Inversion table



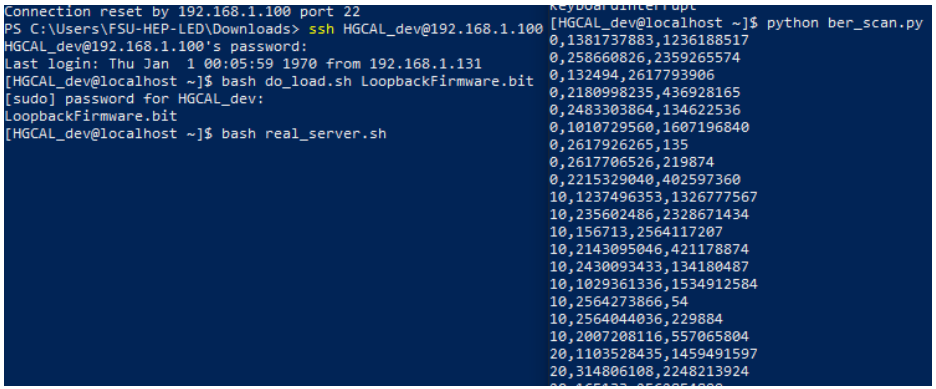
- Each row in time slot means each bytegenerator
- Used to think each row in time slot meant error rate for sub-time interval.

QTH variation and understanding - 4

- Assigning pins to pins that are not connected via loopback

	0	1	2	3	4	5	6	7	8
Loop	N	N	N	N	N	N	N	N	N

Table: Inversion table



- Not getting "0" value for either column

QTH variation and understanding - 5

- Although looking trivial, it gave principles that
  - 1 When signal is inverted, second and third columns are inverted
  - 2 Each row means bytegenerator number
  - 3 When no loop formed, both columns read non-zero value

QSH XDC assignment

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QSH XDC assignment - 1

- To write down QSH XDC file, start with the easiest bytegenerator

QTH/QSH Output	QTH Input	QSH Input
HGCROC1-TRIG-IN-P(N)2 [F2,E2]	HGCROC1-TRIG-OUT-P(N)3 [A9,A8]	HGCROC1-TRIG-OUT-N(P)3 [A8,A9]

Table: bytegenerator0

- PACKAGE_PIN [get_ports A9 HGCROC1_TRIG_OUT_P3]
- PACKAGE_PIN [get_ports A8 HGCROC1_TRIG_OUT_N3]
- Inversion from A8,A9 design, Inverting those legs - No Inversion

QSH XDC assignment - 2

- bytegenerator1

QTH/QSH Output	QTH Input	QSH Input
HGCROC1-TRIG-IN-P(N)1 [G6,F6]	HGCROC2-TRIG-OUT-P(N)0 [A7,A6]	HGCROC1-TRIG-in-N(P)0 [E8,F8]

Table: bytegenerator1

- PACKAGE_PIN [get_ports F8 HGCROC2_TRIG_OUT_P0]
- PACKAGE_PIN [get_ports E8 HGCROC2_TRIG_OUT_N0]
- Inversion from E8,F8 design, Inverting those legs - No Inversion

QSH XDC assignment - 3

- bytegenerator2

QSH Output	QTH Output	QTH/QSH Input
HGCROC2-TRIG-OUT-N(P)0 [A6,A7]	HGCROC1-TRIG-OUT-P(N)0 [F8,E8]	HGCROC2-TRIG-out-P(N)1 [B4,A4]

Table: bytegenerator2

- PACKAGE_PIN [get_ports A7 HGCROC1_TRIG_OUT_P0]
- PACKAGE_PIN [get_ports A6 HGCROC1_TRIG_OUT_N0]
- Inverting Output legs - Inversion

QSH XDC assignment - 4

- bytegenerator3

QTH/QSH Output	QTH Input	QSH Input
fc-sig-in-p(n) [C9,B9]	HGCROC2-TRIG-OUT-P(N)2 [E1,D1]	fc-clk-in-n(p) [D6,D7]

Table: bytegenerator3

- PACKAGE_PIN [get_ports D7 HGCROC2_TRIG_OUT_P2]
- PACKAGE_PIN [get_ports D6 HGCROC2_TRIG_OUT_N2]
- Inversion from D7,D6 design, Inverting those legs - No Inversion
- And the same pattern for all other bytegenerators..

Result and interpretation

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Result and interpretation - 1

We see successful connection for bytegenerator 0,3,5,6 (inverted)

```
[HGCAL_dev@localhost ~]$ python ber_scan.py
0,2618980864,0
0,2388256709,230724155
0,1024982908,1593997956
0,2618980864,0
0,1481080272,1137900592
0,2618980864,0
0,3,2618980861
0,2076700364,542280500
0,1476282404,1142698460
10,2564436736,0
10,1856745667,707691069
10,950492067,1613944669
10,2564436736,0
10,1318877668,1245559068
10,2564436736,0
10,0,2564436736
10,2041804883,522631853
10,1502149069,1062287667
20,2563008512,0
20,1417696411,1145312101
20,919710335,1643298177
20,2563008512,0
20,1186319309,1376689203
20,2563008512,0
20,0,2563008512
```

Byte0

Byte3

Byte5

Byte6(Inv)

Result and interpretation - 2

- **We see correct connection made for 4 different loops**
- **It makes sense to see connection for 0,5. Those connections are the easiest edit of all byte-generators (Keeping all pin assignment same as QTH, but adding 1 more sign of inversion)**
- It was byte6 where the inversion was opposite
- All the other ports are not inversion issue, but data not forming a loopback

Result and interpretation - 3

- List of causes for the error loopback
  - Code gives incorrect pin assignment for those bytegenerators
  - The Cable is truly not forming a loop for those bytegenerators (Cable inside disconncted, short-circuited, etc...)
  - QSH loopback design incorrect

Result and interpretation - 4

- Proposal for solution
  - If the pin assignment was incorrect for either coding issue or QSH design, I can try pin assignment on different FPGA legs and see if it improves any
  - If the WB-cable loopback that we created has an issue, we can create new set of them and see if it improves any.

Summary

- No touch on BD,and V source code. Only fix XDC to change from QTH to QSH (section 1-2)
- QTH variation producing useful information about nature of terminal output (section 3)
- **Newly designed QSH loopback giving about 50% success rate (Section 4-5)**
- **Source of error could be still code issue, or indication of Hardware connection error in WB-QSH Loopback that Kurt and I made in the summer.**

Back-Up