Tileboard update

S. Kim[1]

[1]Department of Physics
Florida State University

Tileboard update, 110220

Introduction

- 1 Tileboard(TB), planned to be inserted into HGCAL, connected to Mezzanine board (Wingboard,WB) via cable
- 2 Cable performance to be tested in the tileboard tester produced by the University of Minnesota (UMinn).
- 3 Loopback executable demonstrating good behavior in Tileboard-QTH connection
- 4 Tileboard-cable-QTH connection impossible due to QTH's sex
- 5 Tileboard-cable-QSH connection possible
- 6 For QSH connection, new Loopback executable for QSH to be programmed in VIVADO

Structure of overall Connection

FPGA Leg (Processor of TB)- Tileboard - Cable - WB - QSH connection
The presentation displays each connection's details with citation of relevant source.

- 1 FPGA pin name - FPGA Leg
- 2 FPGA Leg - Tileboard
- 3 Tileboard - Cable
- 4 Cable - QSH

FPGA pin name - FPGA Leg

- This step has nothing to do with Tileboard.
- The assignments are made purely by Xilinx, producer of FPGA.
- However, this info is essential for synthesis (compilation) of our QSH loopback bitstream (executable).
- FPGA : MPSoC UltraScale+ xczu2cgsfvc784
- Link : `https://www.xilinx.com/support/packagefiles/zuppackages/xczu2cgsfvc784pkg.txt`

FPGA pin name - FPGA Leg Assignment Table

- Example of relevant pins in the table

Table: Caption

FPGA pin name - FPGA Leg Assignment Table

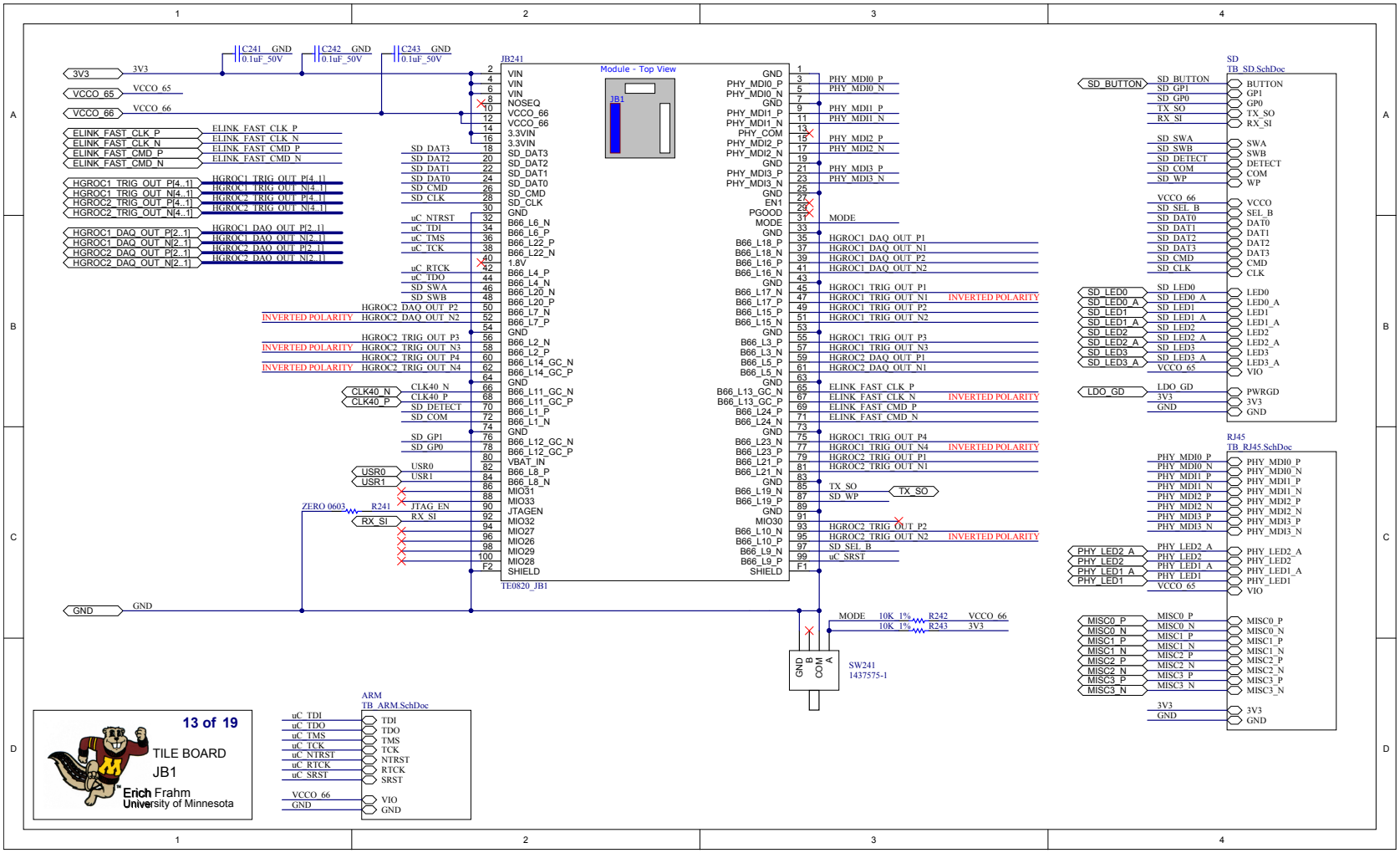
- Example of relevant pins in the table

Pin name	Pin Leg
B9	IO_L24N_T3U_N11_66
C9	IO_L24P_T3U_N10_66
A8	IO_L23N_T3U_N9_66
A9	IO_L23P_T3U_N8_66
A6	IO_L21N_T3L_N5_AD8N_66
A7	IO_L21P_T3L_N4_AD8P_66
B6	IO_L20N_T3L_N3_AD1N_66
C6	IO_L20P_T3L_N2_AD1P_66

FPGA Leg - Tileboard

- FPGA legs connected to different components of the Tileboard (LEDs, SD card, GBTSCA...)
- The Leg - Tileboard components connection, designed and fabricated by the UMinn
- Schematic pdf showing Leg - Tileboard assignment
- The legs are notated as B-L-P structure where
  - B : Leg's location in FPGA I/O bank
  - L : Leg number within the bank
  - P : Differential polarity P/N

Tileboard Schematic for I/O B66



Tileboard table for I/O B66

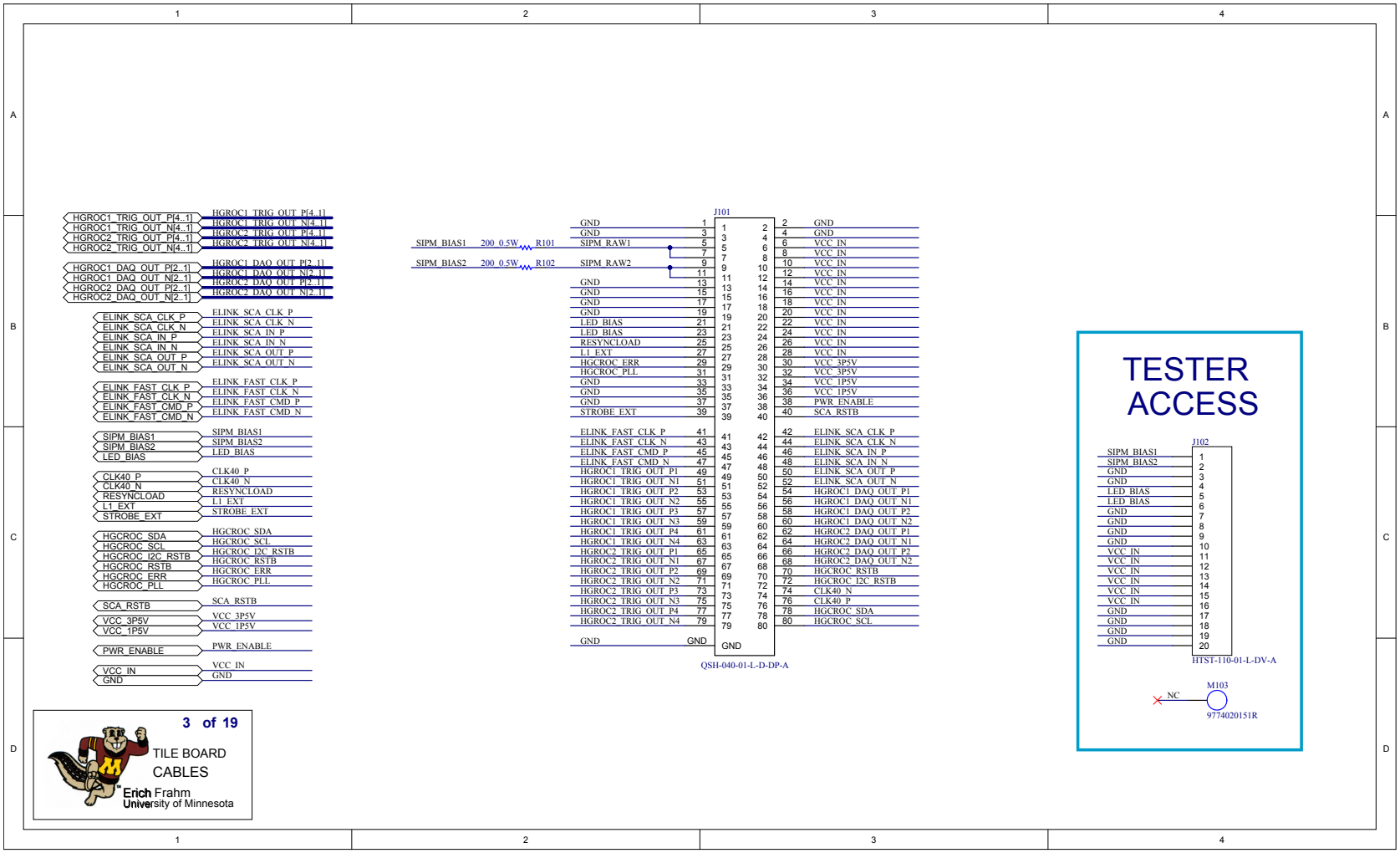
- Following B-L-P pattern and the schematic information, we can complete the table below

Pin name	Pin Leg	Tileboard
B9	IO_L24N_T3U_N11_66	ELINK FAST CMD N
C9	IO_L24P_T3U_N10_66	ELINK FAST CMD P
A8	IO_L23N_T3U_N9_66	HGROC1 TRIG OUT P4
A9	IO_L23P_T3U_N8_66	HGROC1 TRIG OUT N4
A6	IO_L21N_T3L_N5_AD8N_66	HGROC2 TRIG OUT N2
A7	IO_L21P_T3L_N4_AD8P_66	HGROC2 TRIG OUT P2
B6	IO_L20N_T3L_N3_AD1N_66	SD SWA
C6	IO_L20P_T3L_N2_AD1P_66	SD SWB

Tileboard - Cable

- HGROC and ELINK assignment in Tileboard connected to the cable connector (J101)
- Via the cable connector, HGROC and ELINK assignment in Tileboard transfers data to outside of the Tileboard.

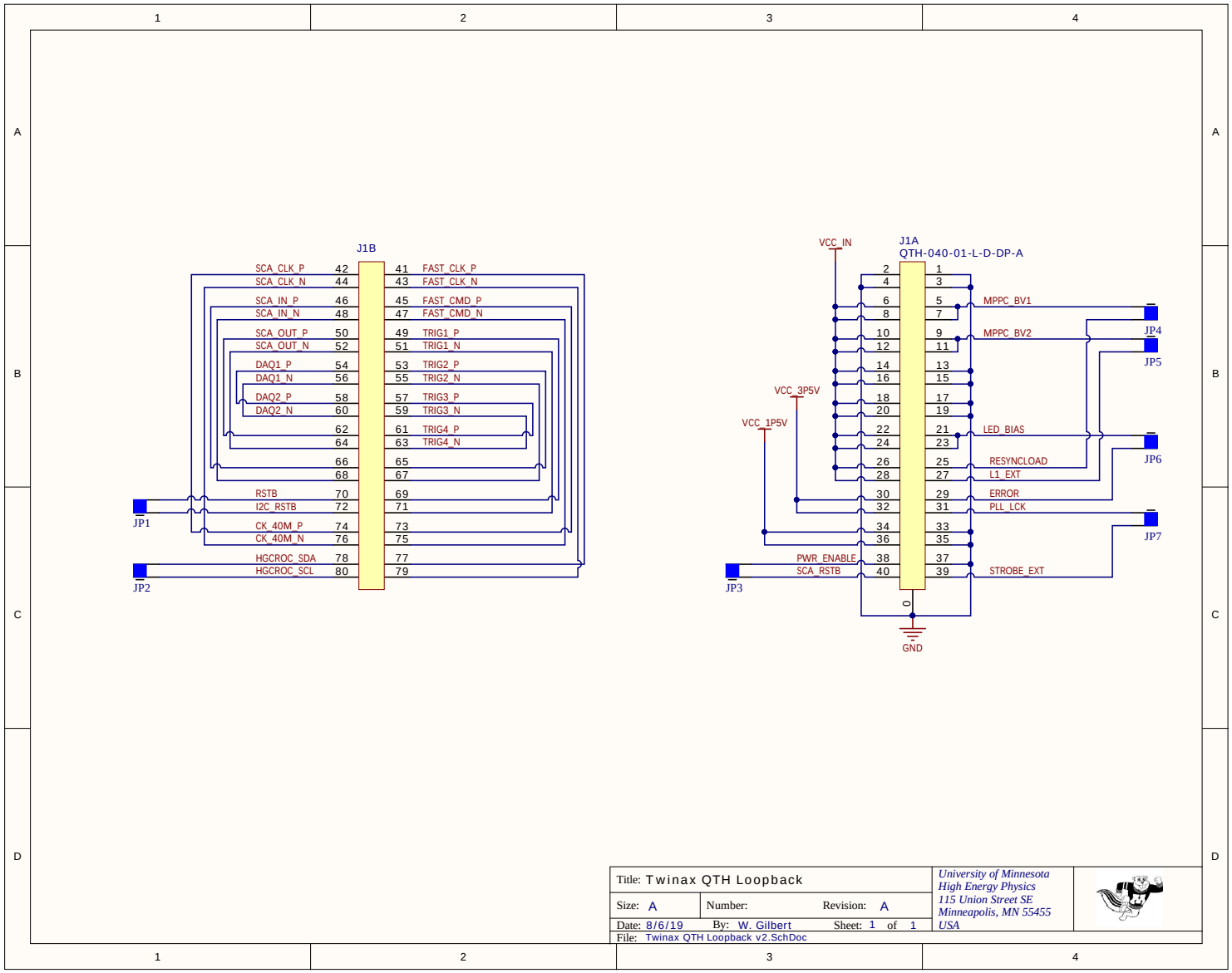
Tileboard - Cable Schematic



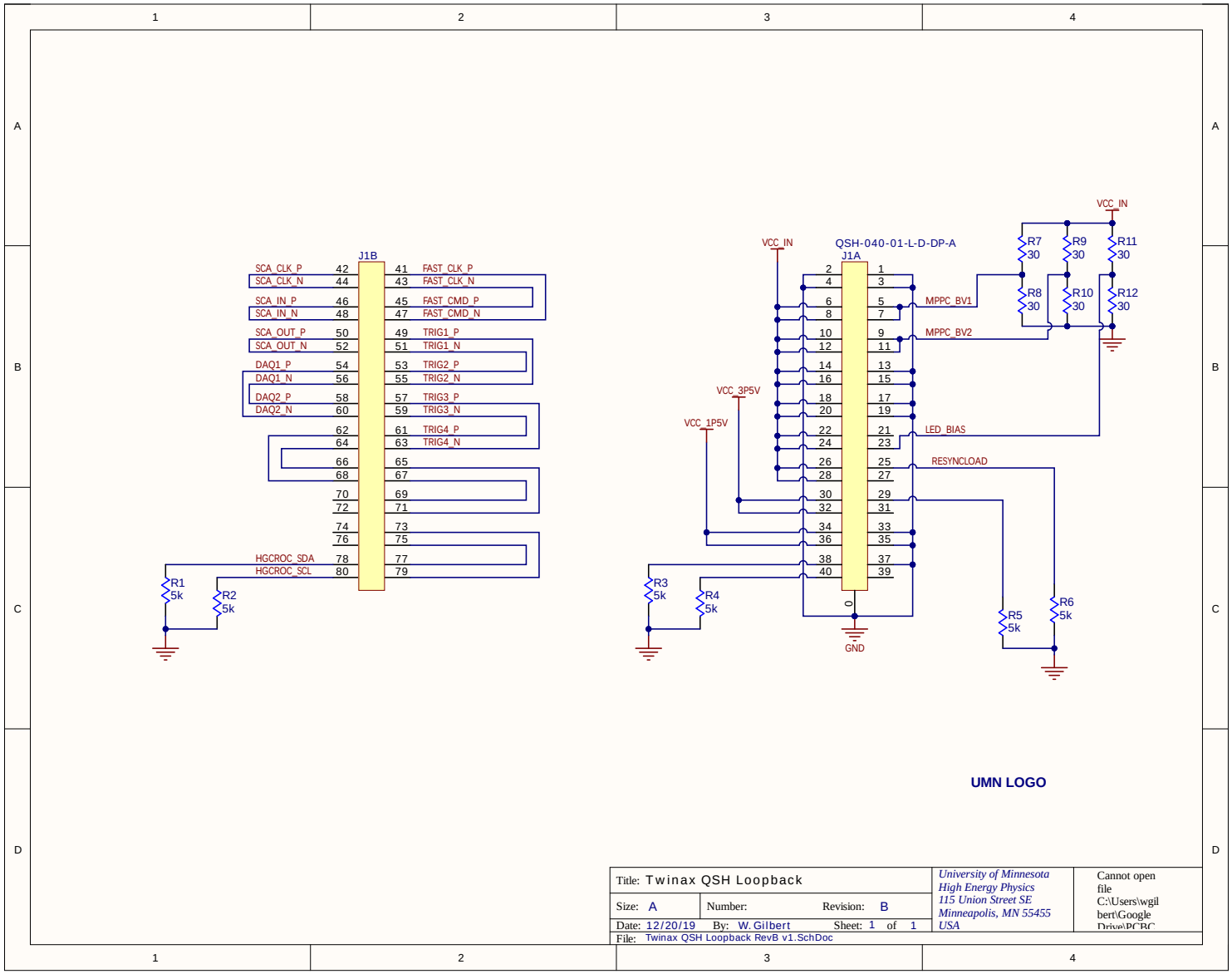
Cable - QTH/QSH Loopback

- One side of the cable - Tileboard's HGROC and ELINK outputs into J101 cable connector, and into the cable
- Opposite side of the cable connector - it's connected to the QTH/QSH Loopback.
- It makes loop connection among cable I/Os

Cable - QTH Loopback Schematic



Cable - QSH Loopback Schematic



Summary

- Details of each connection are all publicated in the above slides
- Based on the QTH and QSH loopback connection, we can generate Output-to-Input table for QTH/QSH as below.

Full Connection Table for QTH

Pin	Leg	Tileboard	Cable O	Cable I	Tileboard	Leg	Pin
B9	IO-L24N-66	ELINK FAST CMD N	47	75	HGROC2 TRIG OUT N3	IO-L2P-66	E1
C9	IO-L24P-66	ELINK FAST CMD P	45	73	HGROC2 TRIG OUT P3	IO-L2N-66	D1
D9	IO-L18N-66	HGROC1 DAQ OUT N1	56	60	HGROC1 DAQ OUT N2	IO-L16N-66	F7
E9	IO-L18P-66	HGROC1 DAQ OUT P1	54	58	HGROC1 DAQ OUT P2	IO-L16P-66	G8
E8	IO-L17N-66	HGROC1 TRIG OUT P1	49	65	HGROC2 TRIG OUT P1	IO-L21P-66	A7
F8	IO-L17P-66	HGROC1 TRIG OUT N1	51	67	HGROC2 TRIG OUT N1	IO-L21N-66	A6
F6	IO-L15N-66	HGROC1 TRIG OUT N2	55	71	HGROC2 TRIG OUT N2	IO-L10N-66	A4
G6	IO-L15P-66	HGROC1 TRIG OUT P2	53	69	HGROC2 TRIG OUT P2	IO-L10P-66	B4

Full Connection Table for QTH - 2

D6	IO-L13N-66	ELINK FAST CLK P	41	77	HGROC2 TRIG OUT P4	IO-L14N-66	D5
D7	IO-L13P-66	ELINK FAST CLK N	43	79	HGROC2 TRIG OUT N4	IO-L14P-66	E5
E2	IO-L3N-66	HGROC1 TRIG OUT N3	59	63	HGROC1 TRIG OUT N4	IO-L23P-66	A9
F2	IO-L3P-66	HGROC1 TRIG OUT P3	57	61	HGROC1 TRIG OUT P4	IO-L23N-66	A8
AD9	IO-L1N-64	SCA-MOSI-N	48	68	HGROC2 DAQ OUT N2	IO-L7P-66	C1
AC9	IO-L1P-64	SCA-MOSI-P	46	66	HGROC2 DAQ OUT P2	IO-L7N-66	B1
AF6	IO-L11N-64	SCA-CLK-N	44	76	CLK40_N	IO-L11N-66	C4
AF7	IO-L11P-64	SCA-CLK-P	42	74	CLK40_P	IO-L11P-66	D4
AE8	IO-L2N-64	SCA-MISO-N	52	64	HGROC2 DAQ OUT N1	IO-L5N-66	E3
AE9	IO-L2P-64	SCA-MISO-P	50	62	HGROC2 DAQ OUT P1	IO-L5P-66	E4

Full Connection Table for QSH

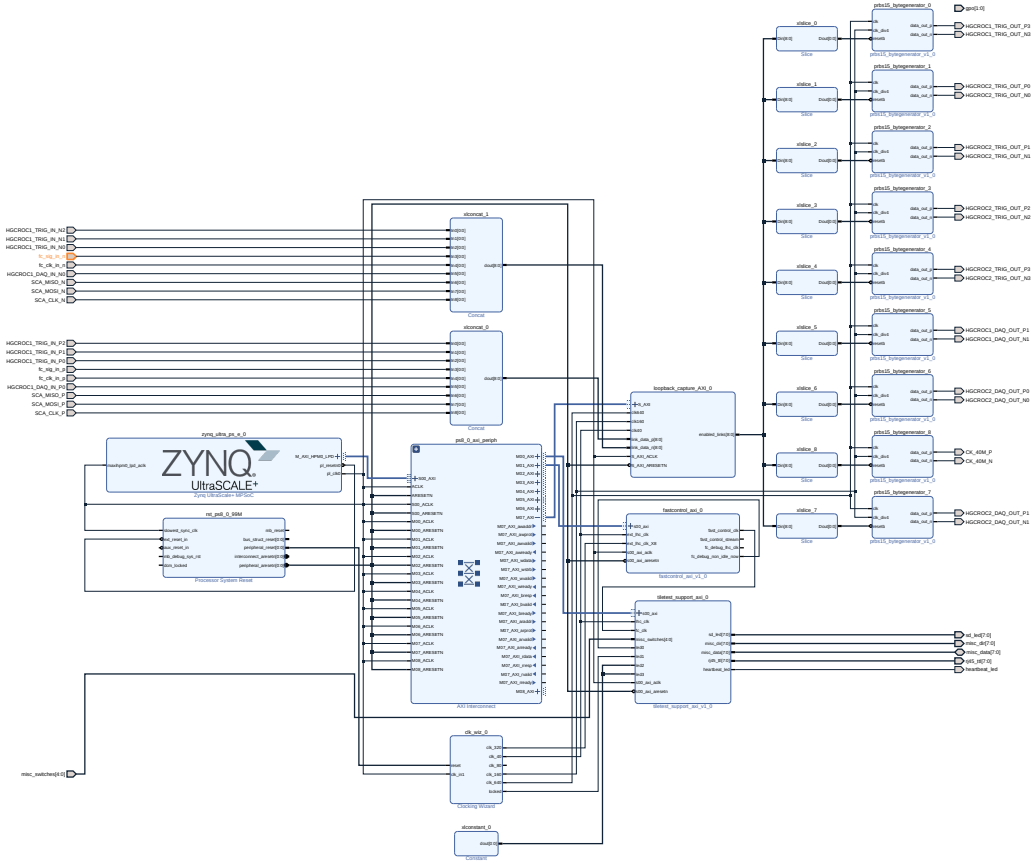
Pin	Leg	Tileboard	Cable O	Cable I	Tileboard	Leg	Pin
B9	IO-L24N-66	ELINK FAST CMD N	47	41	ELINK FAST CLK P	IO-L13N-66	D6
C9	IO-L24P-66	ELINK FAST CMD P	45	43	ELINK FAST CLK N	IO-L13P-66	D7
D9	IO-L18N-66	HGROC1 DAQ OUT N1	56	58	HGROC1 DAQ OUT P2	IO-L16P-66	G8
E9	IO-L18P-66	HGROC1 DAQ OUT P1	54	60	HGROC1 DAQ OUT N2	IO-L16N-66	F7
E8	IO-L17N-66	HGROC1 TRIG OUT P1	49	55	HGROC1 TRIG OUT N2	IO-L15N-66	F6
F8	IO-L17P-66	HGROC1 TRIG OUT N1	51	53	HGROC1 TRIG OUT P2	IO-L15P-66	G6
E2	IO-L3N-66	HGROC1 TRIG OUT N3	59	61	HGROC1 TRIG OUT P4	IO-L23N-66	A8
F2	IO-L3P-66	HGROC1 TRIG OUT P3	57	63	HGROC1 TRIG OUT N4	IO-L23P-66	A9

Full Connection Table for QSH - 2

A7	IO-L21P-66	HGROC2 TRIG OUT P1	65	71	HGROC2 TRIG OUT N2	IO-L10N-66	A4
A6	IO-L21N-66	HGROC2 TRIG OUT N1	67	69	HGROC2 TRIG OUT P2	IO-L10P-66	B4
E1	IO-L2P-66	HGROC2 TRIG OUT N3	75	77	HGROC2 TRIG OUT P4	IO-L14N-66	D5
D1	IO-L2N-66	HGROC2 TRIG OUT P3	73	79	HGROC2 TRIG OUT N4	IO-L14P-66	E5
E4	IO-L5P-66	HGROC2 DAQ OUT P1	62	68	HGROC2 DAQ OUT N2	IO-L7P-66	C1
E3	IO-L5N-66	HGROC2 DAQ OUT N1	64	66	HGROC2 DAQ OUT P2	IO-L7N-66	B1
AF6	IO-L11N-64	SCA-CLK-N	44	42	SCA-CLK-P	IO-L11P-64	AF7
C4	IO-L11N-66	CLK40_N	76	74	CLK40_P	IO-L11P-66	D4
AE8	IO-L2N-64	SCA-MISO-N	52	50	SCA-MISO-P	IO-L2P-64	AE9
AD9	IO-L1N-64	SCA-MOSI-N	48	46	SCA-MOSI-P	IO-L1P-64	AC9

Block Diagram for QTH

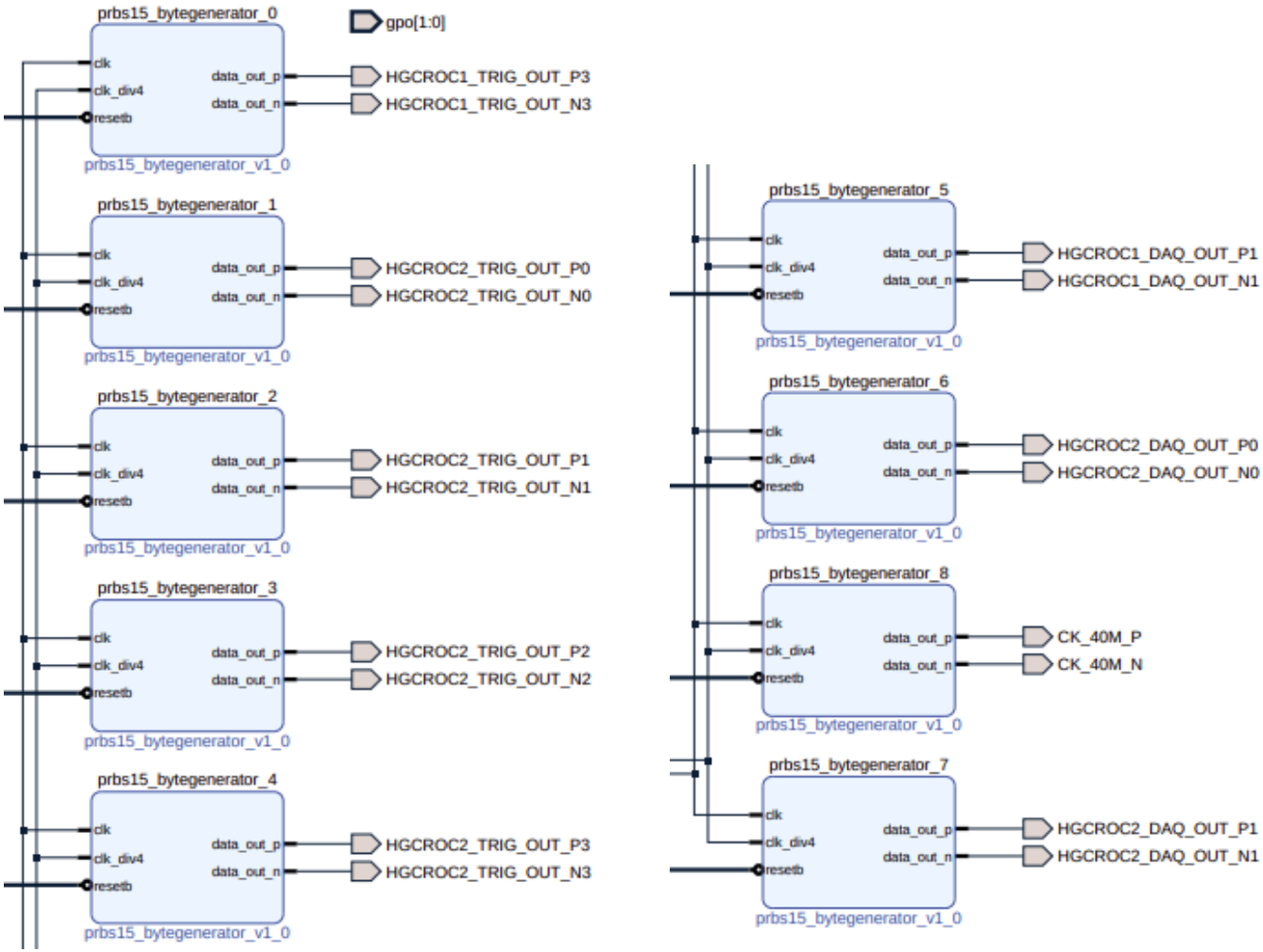
The Block Diagram for QTH Loopback is below.



Block Diagram for QTH - Zoom1

Zoomed in

Block Diagram for QTH - Zoom2

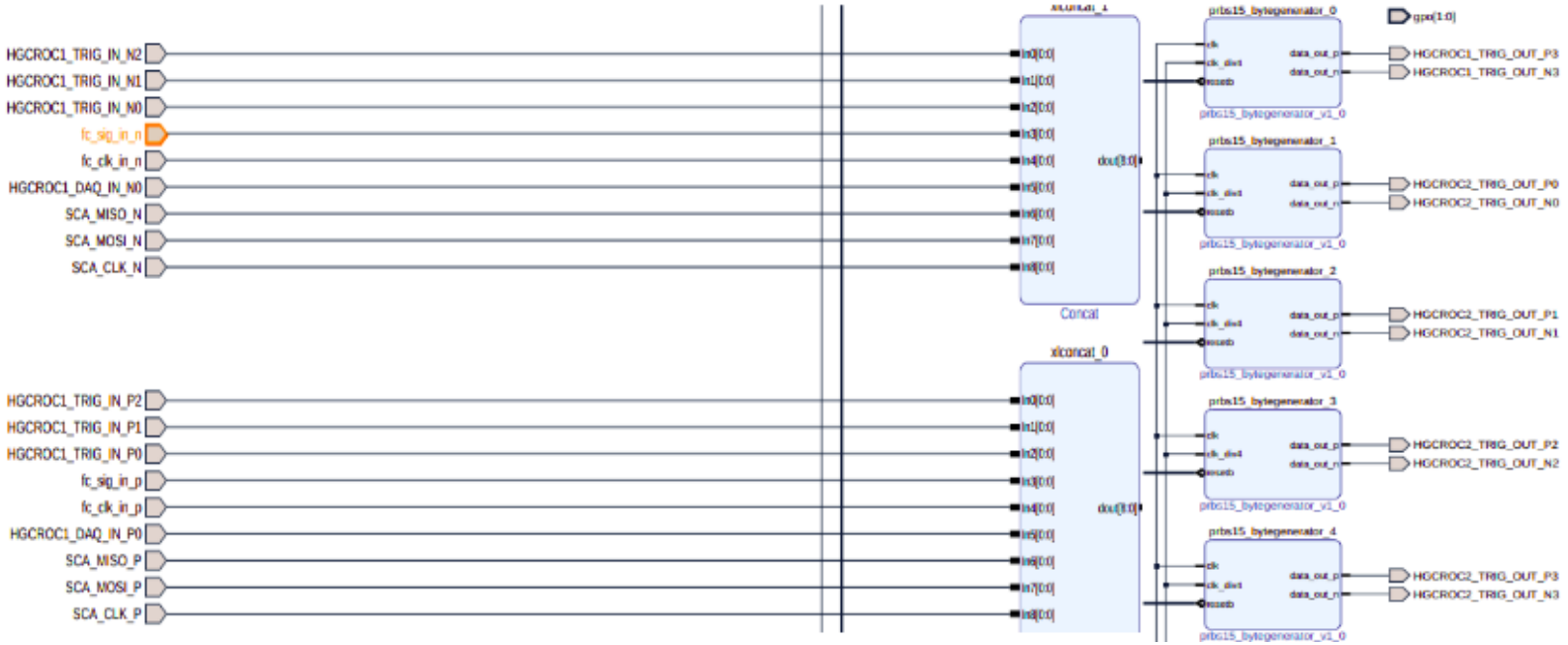


Block Diagram's Mechanism

Based on comparison of the QTH table and the QTH Block Design (BD), **Loopback connection is made in**

- In[n] of xlconcat 0 - prbs15_bytegenerator_n's data_out_p : Loopback for positive differential pair
- In[n] of xlconcat 1 - prbs15_bytegenerator_n's data_out_n : Loopback for negative differential pair
- ex)HGCROC1_TRIG_IN_P2 (In[0] of xlconcat 0) - HGCROC1_TRIG_IN_P3
  (data_out_p of prbs15_bytegenerator_0)

Block Diagram for QTH - Combined



QSH design

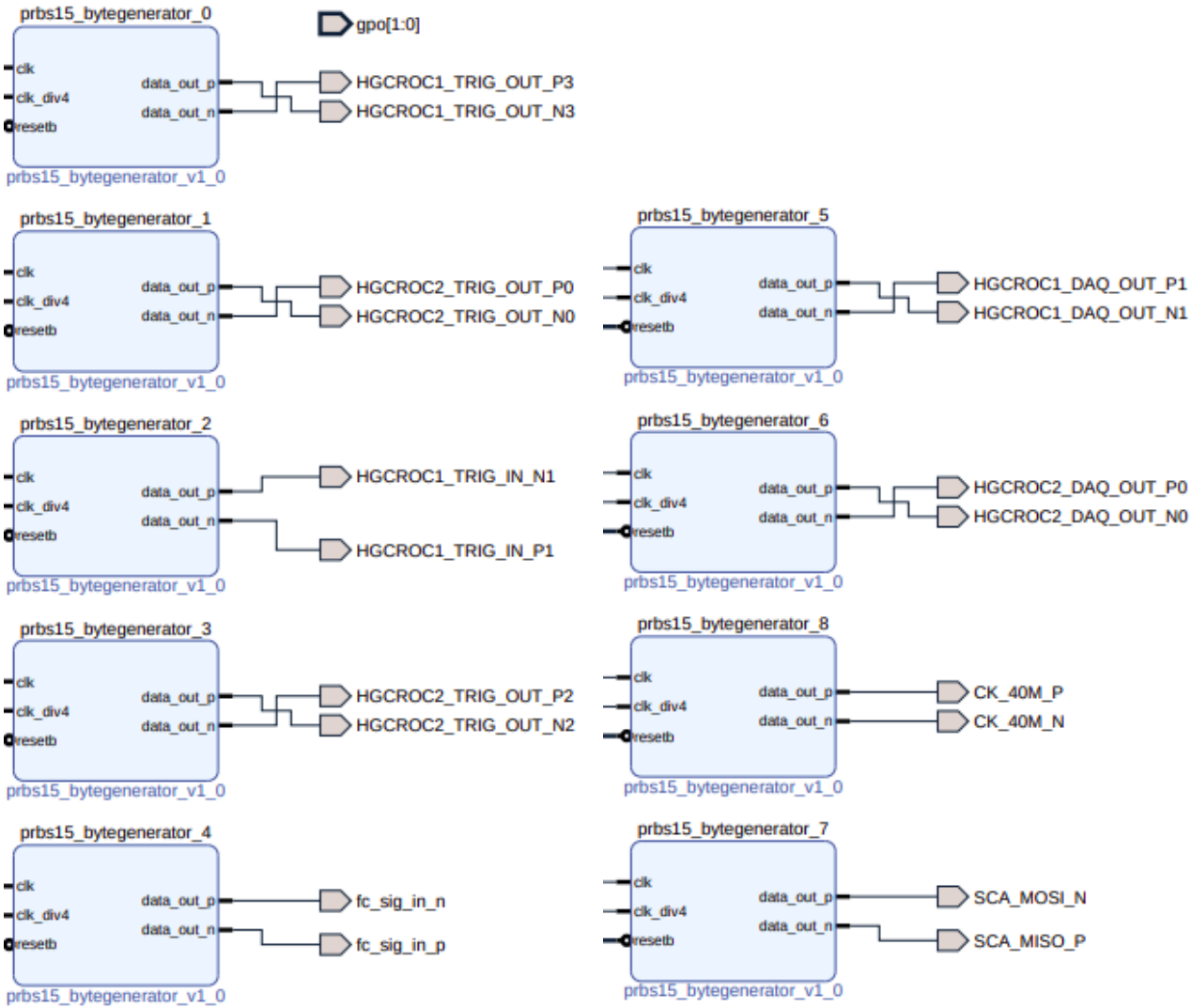
Based on the same principle, one can design QSH by editing the I/O ports connected to In[n] of xlconcat
and data_out of prbs15_bytegenerator

- QTH) HGCROC1_TRIG_IN_P2 (In[0] of xlconcat 0) - HGCROC1_TRIG_IN_N3 (data_out_p of prbs15_bytegenerator_0) **becomes**
- QSH) HGCROC1_TRIG_IN_P2 (In[0] of xlconcat 0) - HGCROC1_TRIG_IN_N3 (data_out_p of prbs15_bytegenerator_0)

Block Diagram for QSH - Zoom1

The Block Diagram for QSH Loopback is below.

Block Diagram for QSH - Zoom2

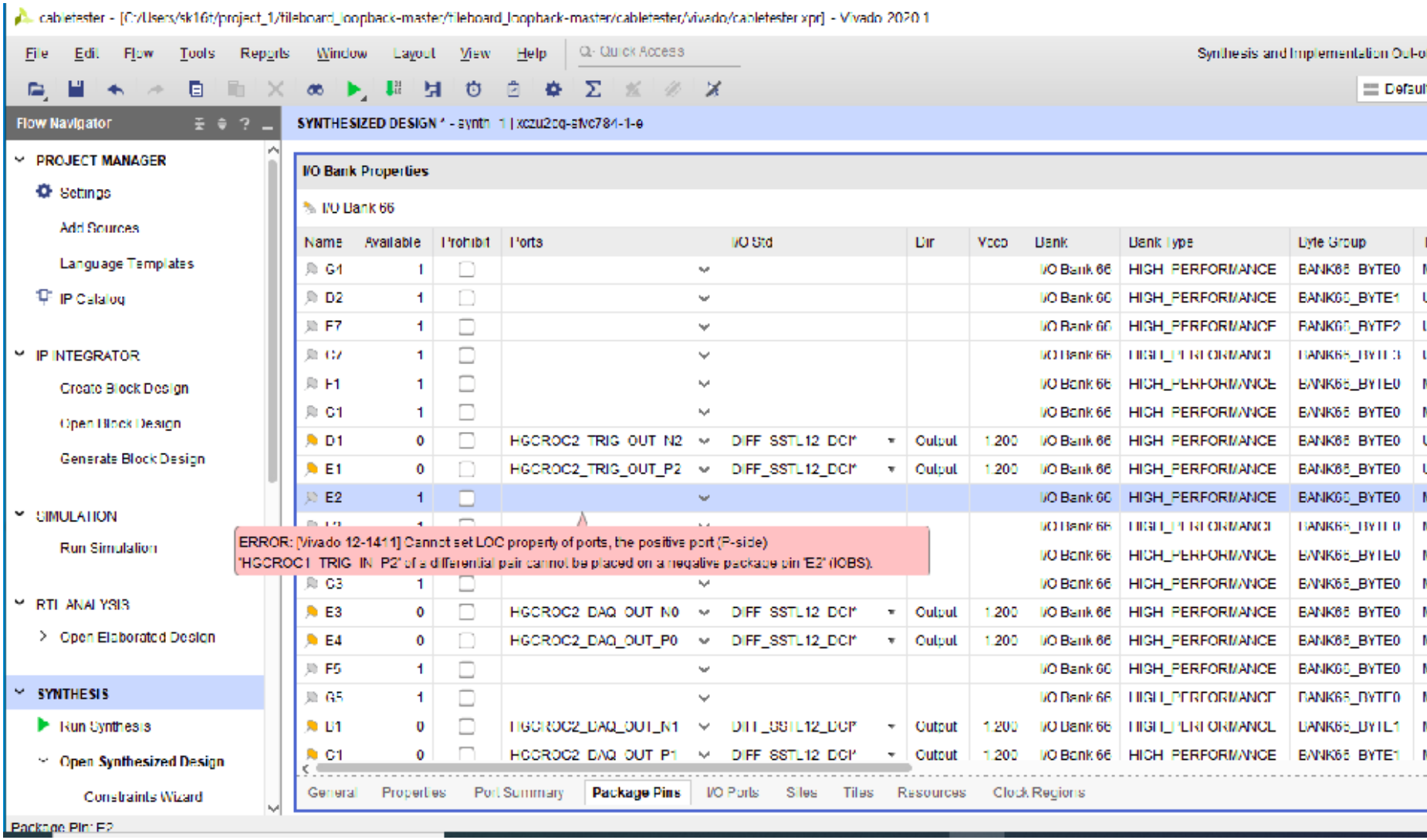


QSH Synthesis

Synthesis (Compilation) of the BD completed successfully

- Synthesis (Compilation) of the BD completed successfully
- This is expected as the P,N polarity is not yet implemented in the FPGA level. P,N are nothing but just name for I/O pins in synthesis level.
- Implementation assigns FPGA pins to I/O ports of the synthesis code. In the process, it also checks its validity
- Implementation step allow I/O_N polarity to be only assigned to positive differential leg due to its connection to data_out_p.
- However, correct assignment based on the design of FPGA pin - Tileboard is that they have to be assigned to negative differential pair.

Example of such case



Solution

Inverting the signal (changing the differential polarity) suggested as general solution

- Kurt suggests it would not be such naive and needs to have change in IP used in BD.
- Tried inserting NOT function into OBUFDS while assigning the opposite differential leg in the implementation - Not working completely
- I need to find some solutions

Back-Up