Tileboard update

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Tileboard update, 113020

Introduction and Summary

- 112020 presentation : 0,3,5,6 loopbacks working in the TB
- Investigation of GBTSCA, WB schematics, and DMM continuity test to explain errors for 1,2,4,7,8 loopbacks
- 2,4,6 were not supposed to work due to grounding of output signals in the EB
- 7,8 were not supposed to work since the Cable Connector (J101) receives signal from GBTSCA.
- **Things that were supposed to work, and things not supposed to work do not work** (except 1,6).

Structure of Presentation

- 0 Review of 112020 result
- 1 Complete QSH XDC assignment
- 2 Review of the GBTSCA schematics
- 3 Review of the WB schematics
- 4 Conclusion

Result and interpretation - 1

Before jumping into item1, this is review of where I left off on 112020.

We see successful connection for bytegenerator 0,3,5,6 (inverted)

```
[HGCAL_dev@localhost ~]$ python ber_scan.py
0,2618980864,0
0,2388256709,230724155
0,1024982908,1593997956
0,2618980864,0
0,1481080272,1137900592
0,2618980864,0
0,3,2618980861
0,2076700364,542280500
0,1476282404,1142698460
10,2564436736,0
10,1856745667,707691069
10,950492067,1613944669
10,2564436736,0
10,1318877668,1245559068
10,2564436736,0
10,0,2564436736
10,2041804883,522631853
10,1502149069,1062287667
20,2563008512,0
20,1417696411,1145312101
20,919710335,1643298177
20,2563008512,0
20,1186319309,1376689203
20,2563008512,0
20,0,2563008512
```

Byte0

Byte3

Byte5

Byte6(Inv)

Result and interpretation - 2

- **We see correct connection made for 4 different loops**
- **It makes sense to see connection for 0,5. Those connections are the easiest edit of all byte-generators (Keeping all pin assignment same as QTH, but adding 1 more sign of inversion)**
- It was byte6 where the inversion was opposite
- All the other ports are not inversion issue, but data not forming a loopback

QSH XDC assignment - 1

- **GBTSCA and WB's sections later in the presentation need these technical details as referral to explain why 2,4,6,7,8 should get non-zero error.**
- To write down QSH XDC file, start with the easiest bytegenerator

QTH/QSH Output	QTH Input	QSH Input
HGCROC1-TRIG-IN-P(N)2 [F2,E2]	HGCROC1-TRIG-OUT-P(N)3 [A9,A8]	HGCROC1-TRIG-OUT-N(P)3 [A8,A9]

Table: bytegenerator0

- PACKAGE_PIN [get_ports A9 HGCROC1_TRIG_OUT_P3]
- PACKAGE_PIN [get_ports A8 HGCROC1_TRIG_OUT_N3]
- Inversion from A8,A9 design, Inverting those legs - No Inversion

QSH XDC assignment - 2

- bytegenerator1

QTH/QSH Output	QTH Input	QSH Input
HGCROC1-TRIG-IN-P(N)1 [G6,F6]	HGCROC2-TRIG-OUT-P(N)0 [A7,A6]	HGCROC1-TRIG-in-N(P)0 [E8,F8]

Table: bytegenerator1

- PACKAGE_PIN [get_ports F8 HGCROC2_TRIG_OUT_P0]
- PACKAGE_PIN [get_ports E8 HGCROC2_TRIG_OUT_N0]
- Inversion from E8,F8 design, Inverting those legs - No Inversion

QSH XDC assignment - 3

- bytegenerator2

QSH Output	QTH Output	QTH/QSH Input
HGCROC2-TRIG-OUT-N(P)0 [A6,A7]	HGCROC1-TRIG-OUT-P(N)0 [F8,E8]	HGCROC2-TRIG-out-P(N)1 [B4,A4]

Table: bytegenerator2

- PACKAGE_PIN [get_ports A7 HGCROC1_TRIG_OUT_P0]
- PACKAGE_PIN [get_ports A6 HGCROC1_TRIG_OUT_N0]
- Inverting Output legs - Inversion

QSH XDC assignment - 4

- bytegenerator3

QTH/QSH Output	QTH Input	QSH Input
fc-sig-in-p(n) [C9,B9]	HGCROC2-TRIG-OUT-P(N)2 [E1,D1]	fc-clk-in-n(p) [D6,D7]

Table: bytegenerator3

- PACKAGE_PIN [get_ports D7 HGCROC2_TRIG_OUT_P2]
- PACKAGE_PIN [get_ports D6 HGCROC2_TRIG_OUT_N2]
- Inversion from D7,D6 design, Inverting those legs - No Inversion

QSH XDC assignment - 5

- bytegenerator4

QSH Output HGCROC2-TRIG-OUT-N(P)2 [D1,E1]	QTH Output fc-clk-in-p(n) [D7,D6]	QTH/QSH Input HGCROC2-TRIG-out-P(N)3 [E5,D5]

Table: bytegenerator4

- PACKAGE_PIN [get_ports E1 fc-clk-in-p]
- PACKAGE_PIN [get_ports D1 fc-clk-in-n]
- Inverting Output legs, Inversion from D1,E1 design, Inversion from E5,D5 design - Inversion

- bytegenerator5

QTH/QSH Output HGCROC1-DAQ-IN-P(N)0 [E9,D9]	QTH Input HGCROC1-DAQ-OUT-P(N)1 [G8,F7]	QSH Input HGCROC1-DAQ-OUT-N(P)1 [F7,G8]

Table: bytegenerator5

- PACKAGE_PIN [get_ports G8 HGCROC1_DAQ_OUT_P1]
- PACKAGE_PIN [get_ports F7 HGCROC1_DA1_OUT_N1]
- Inverting G8,F7 legs - Inversion

QSH XDC assignment - 7

- bytegenerator6

QSH Output	QTH Output	QTH/QSH Input
HGCROC2-DAQ-OUT-N(P)1 [B1,C1]	SCA-MISO-p(n) [AE9,AE8]	HGCROC2-DAQ-OUT-P(N)0 [E4,E3]

Table: bytegenerator6

- PACKAGE_PIN [get_ports C1 SCA-MISO-p]
- PACKAGE_PIN [get_ports B1 SCA-MISO-n]
- Inversion from B1,C1 design, Inverting those legs - No Inversion

QSH XDC assignment - 8

- bytegenerator7

QSH Output	QTH Output	QTH Input	QSH Input
SCA-MOSI-p,SCA-MISO-n [AC9,AE8]	SCA-MOSI-p(n) [AC9,AD9]	HGCROC2-DAQ-OUT-P(N)1 [C1,B1]	SCA-MOSI-n,SCA-MISO-p [AD9,AE9]

Table: bytegenerator7

- PACKAGE_PIN [get_ports AE8 SCA-MOSI-n]
- PACKAGE_PIN [get_ports AE9 HGCROC2_DAQ_OUT_P1]
- PACKAGE_PIN [get_ports AD9 HGCROC2_DAQ_OUT_N1]

- bytegenerator8

QSH Output	QTH Output	QTH Input	QSH Input
SCA-CLK-p,CK-40M-n [AF7,C4]	SCA-CLK-p(n) [AF7,AF6]	CK-40M-p(n) [D4,C4]	SCA-CLK-n,CK-40M-p [AF6,D4]

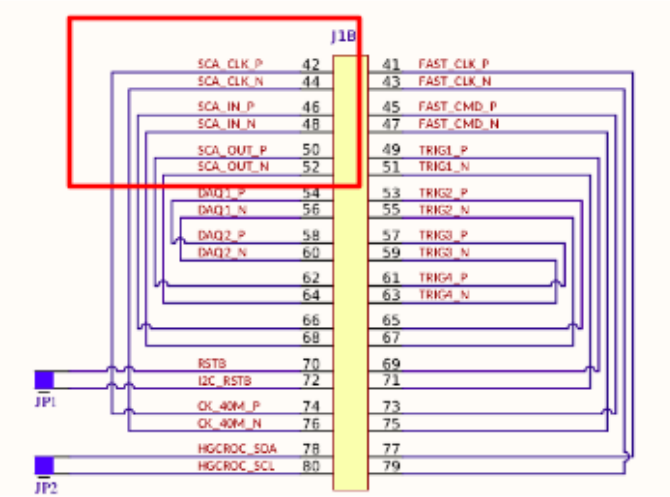
Table: bytegenerator8

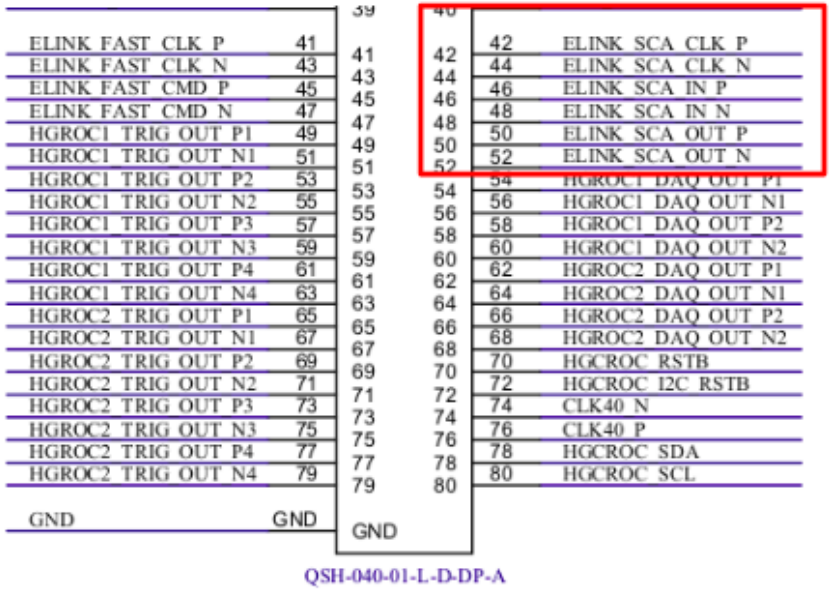
- PACKAGE_PIN [get_ports C4 SCA-CLK-n]
- PACKAGE_PIN [get_ports AF6 CK-40M-p]
- PACKAGE_PIN [get_ports D4 SCA-CLK-n]

Review of the GBTSCA schematics - 1

Left schematic is from QTH loopback, the right is from UMinn schematics

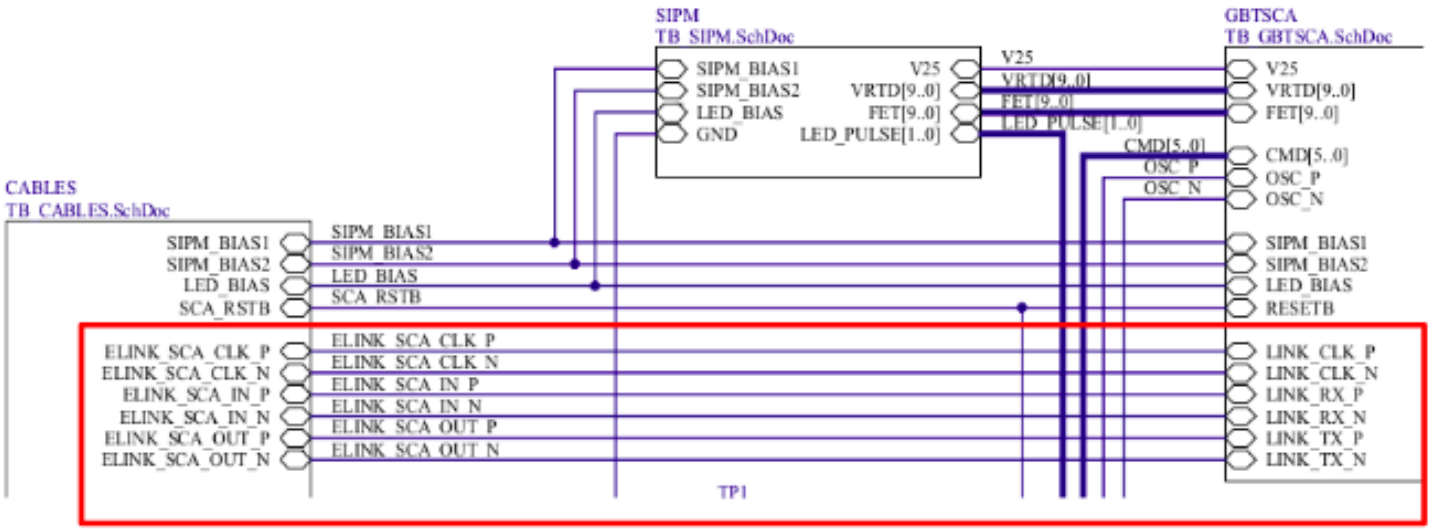
Red box highlights the corresponding pins in 2 different schematics.





Review of the GBTSCA schematics - 2

In the same UMinn schematics p.2, It shows signals for the cable comes from **GBTSCA, not FPGA.**



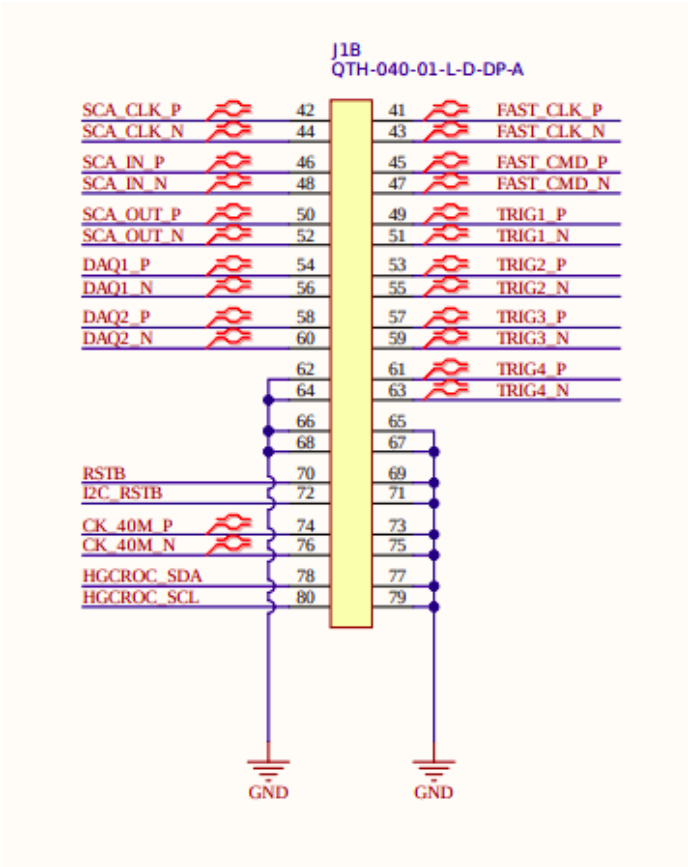
Review of the GBTSCA schematics - 3

These I/O ports are **SCA-MISO,MOSI,CLK-p/n** of our Loopbacks.
For QSH Loopback, they compose **Loopback 7,8.**
Since they need signal from GBTSCA, which we do not have, it makes sense that we are getting **non-zero error values for 7,8**.

Review of the WB schematics - 1

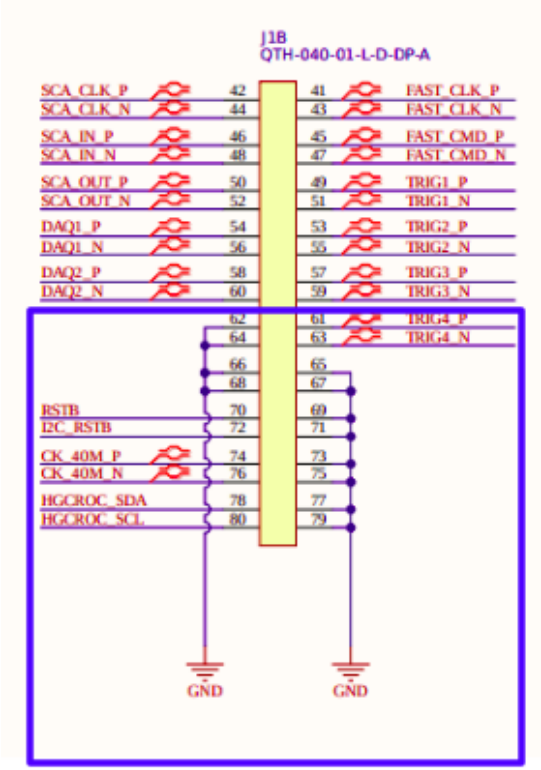
In FPGA Leg (Processor of TB)- Tileboard - Cable - WB - QSH connection, WB-QSH connection explains error rate for 2,4,6 loopbacks

Below is the diagram of **Cable inside the WB** (not the cable loopback on TB).



Review of the WB schematics - 2

After receiving the output signal from the FPGA via TB, **the WB grounds the signals for HGCROC2 I/O pins** before looping over through the cables.
In QSH, **Loopback 2,4,6** have HGCROC2-TRIG/DAQ-p/n I/O pins.



It explains **non-zero error rate for 2,4,6**.

- 1 Complete QSH XDC assignment
- 2 Review of the GBTSCA schematics
- 3 Review of the WB schematics
- 4 **Conclusion**

Conclusion - 1

- My loopback has non-zero error rate for 1,2,4,7,8 (section 0)
- **GBTSCA's signal** explains error rate for Loopback 7,8 (section 2)
- **WB's grounding** explains error rate for Loopback 2,4,6 (section 3)
- The only mismatch is loopback 1 and 6, which I switched their pin assignment in the constraint file
- Thus, I claim the FPGA bitstream for QSH finally gets correct error rate (0 for complete loop, non-zero for disconnected loop) QSH loopback design.

Back-Up