

A

A

B

B

C

C

D

D

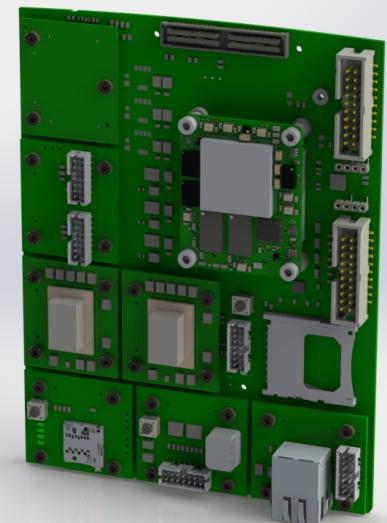
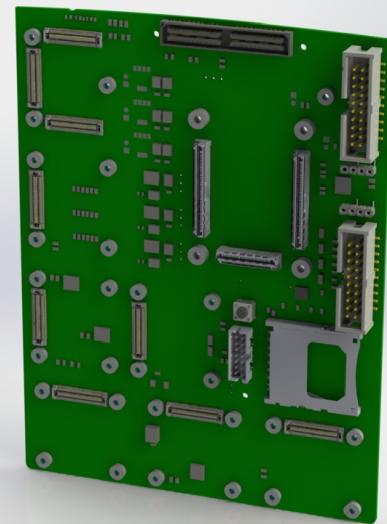


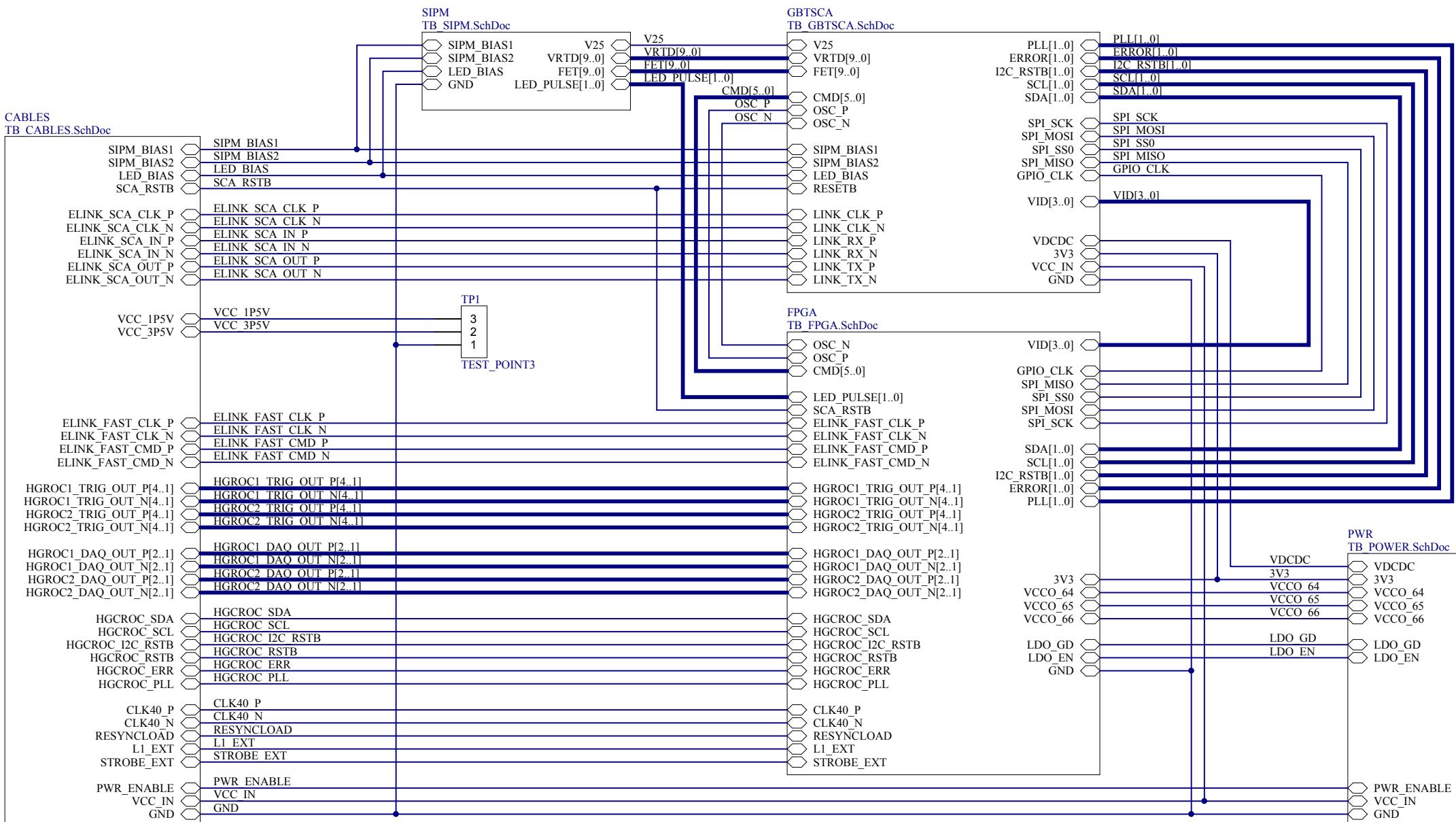
1 of 19

TILE BOARD  
INTROErich Frahm  
University of Minnesota

# UMN.edu TILE BOARD EMULATOR

## V0.1 - JAN. 2019





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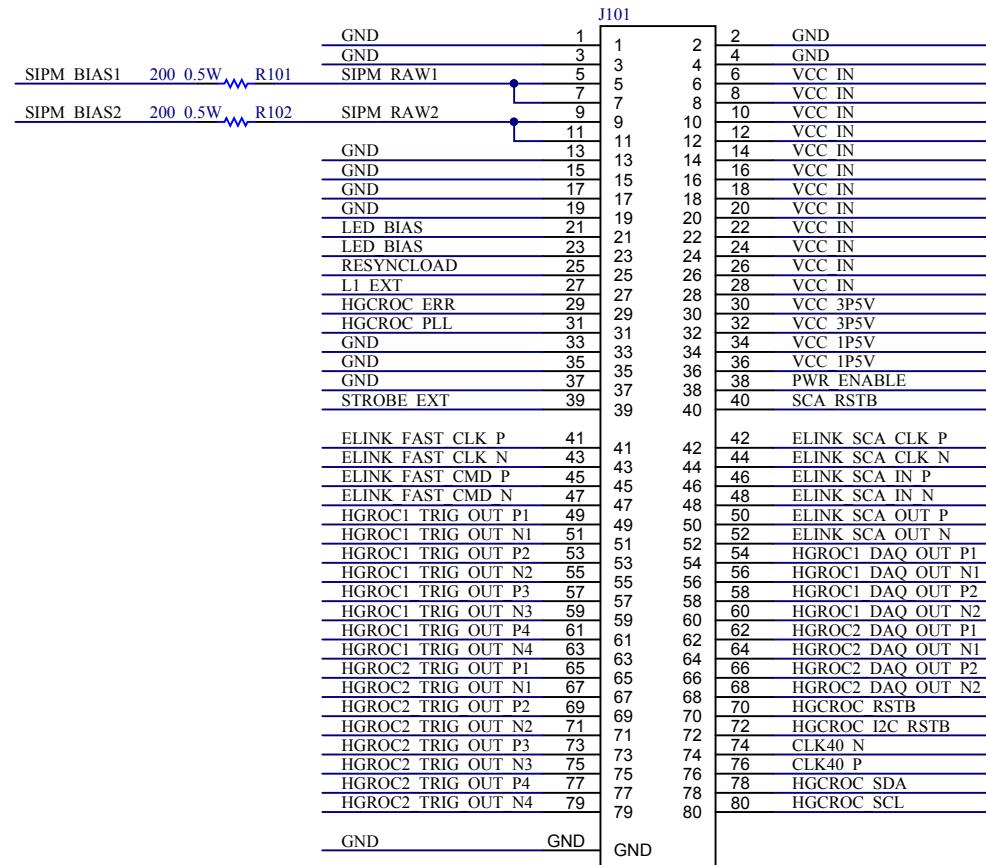
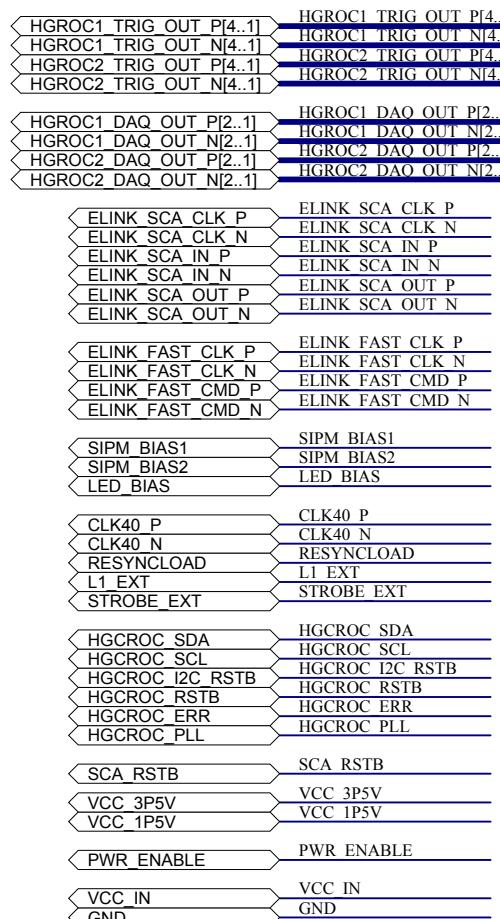


FIDUCIAL

FIDUCIAL

FIDUCIAL

GOLDY

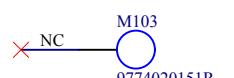


## TESTER ACCESS

**J102**

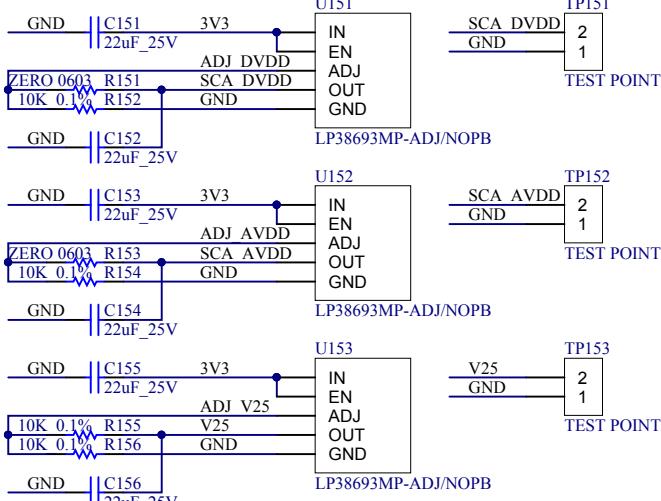
SIPM_BIAS1	1
SIPM_BIAS2	2
GND	3
GND	4
LED_BIAS	5
LED_BIAS	6
GND	7
GND	8
GND	9
VCC_IN	10
VCC_IN	11
VCC_IN	12
VCC_IN	13
VCC_IN	14
VCC_IN	15
GND	16
GND	17
GND	18
GND	19
GND	20

HTST-110-01-L-DV-A

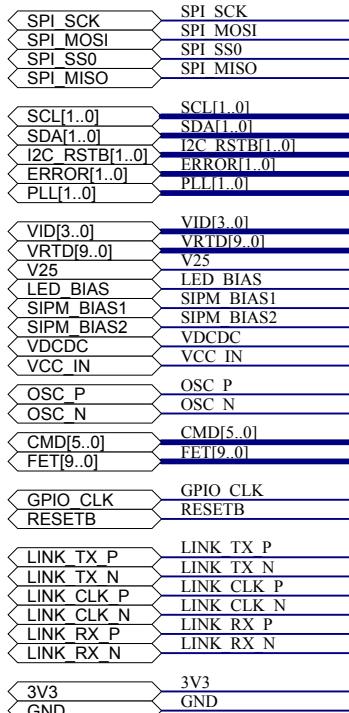


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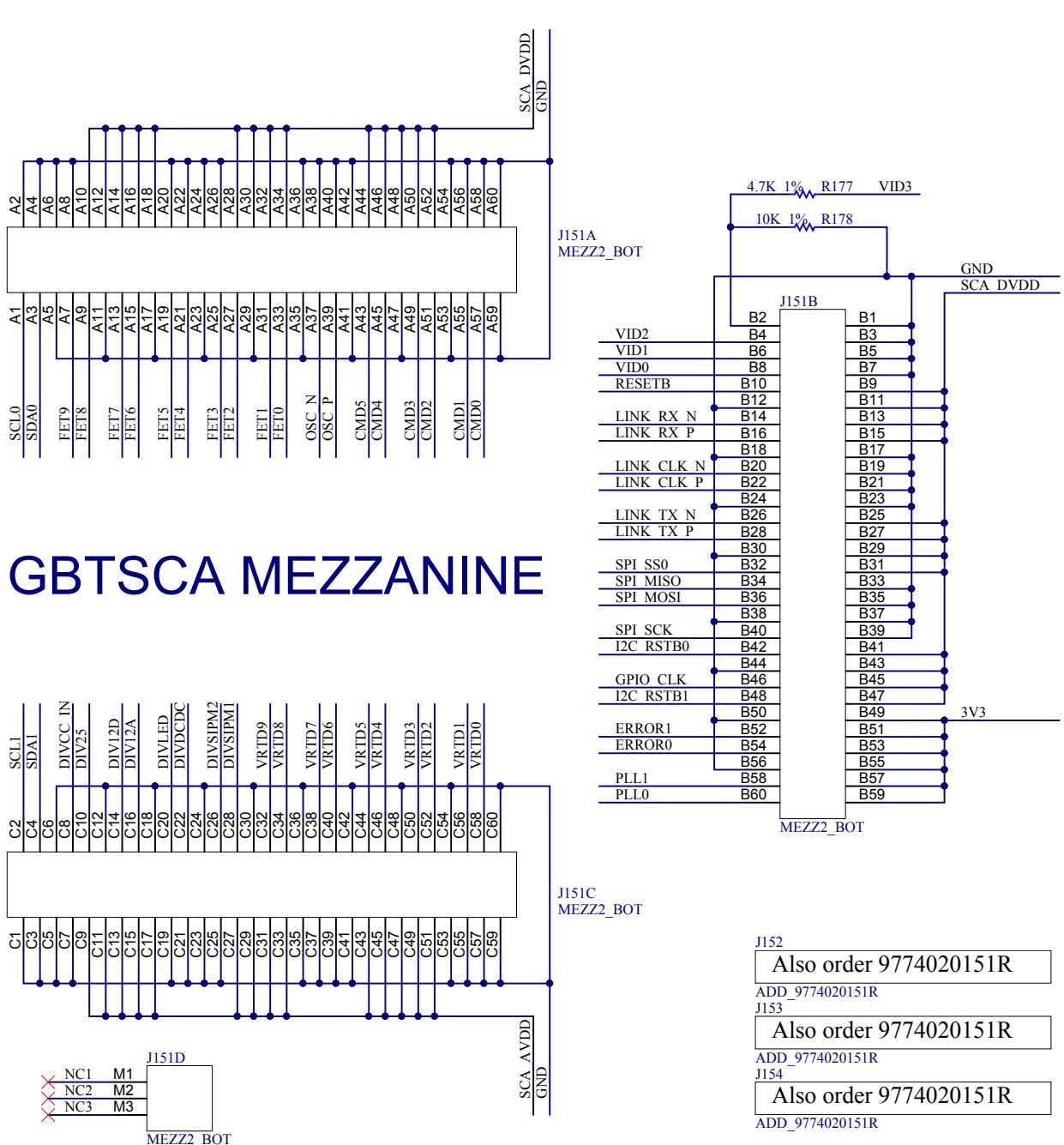
R1	R2	VOUT
10K	10K	2.5
2K	10K	1.5
0	10K	1.25



BLANK MEZZ

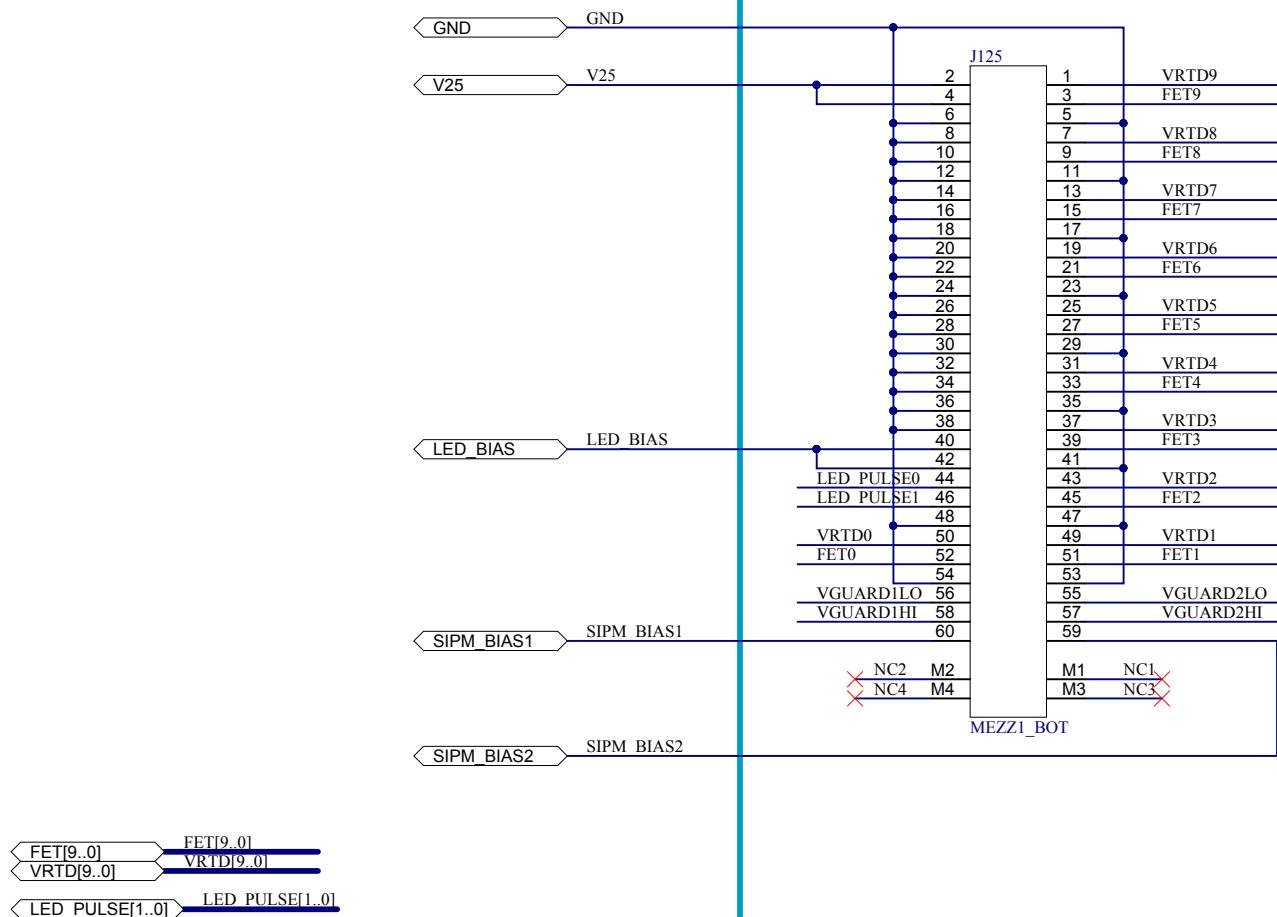
```
=====  
CMD0 = LINK_TX_P  
CMD1 = LINK_TX_N  
CMD2 = LINK_CLK_P  
CMD3 = LINK_CLK_N  
CMD4 = LINK_RX_P  
CMD5 = LINK_RX_N  
OSC_P = 160MHZ_P  
OSC_N = 160MHZ_N
```

SCL0	4.7K	1%	R173	SCA	DVDD
SDA0	4.7K	1%	R174		
SCL1	4.7K	1%	R175		
SDA1	4.7K	1%	R176		



# GBTSCA MEZZANINE

# SIPM MEZZANINE



J121  
Also order 9774020151R  
ADD\_9774020151R

J122  
Also order 9774020151R  
ADD\_9774020151R

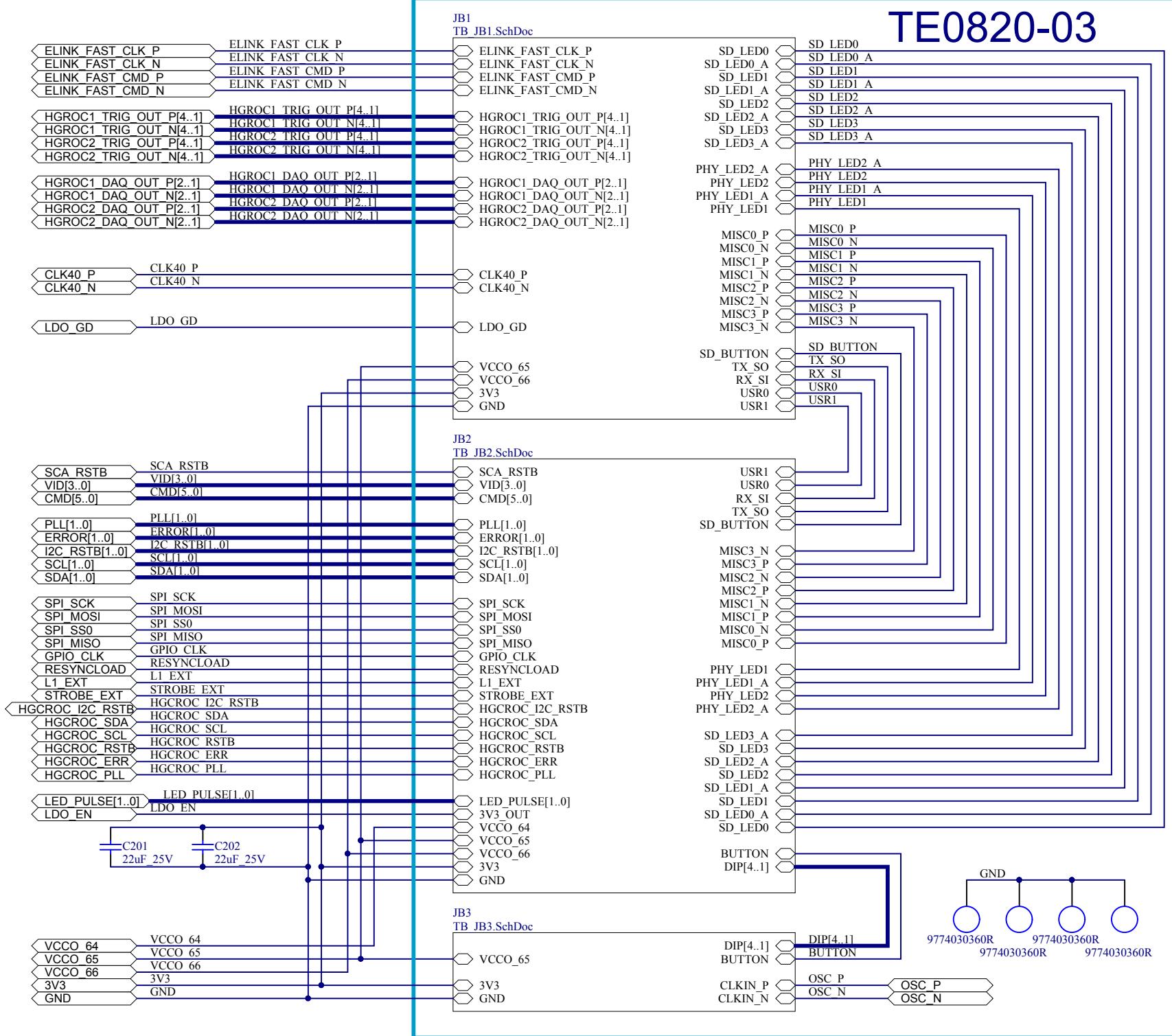
J123  
Also order 9774020151R  
ADD\_9774020151R

J124  
Also order 9774020151R  
ADD\_9774020151R

SIPM_BIAS1	100K 1%	R121	VGUARD1HI	100K 1%	R122	VGUARD1LO	100K 1%	R125	GND
SIPM_BIAS2	100K 1%	R123	VGUARD2HI	100K 1%	R124	VGUARD2LO	100K 1%	R126	GND



# TE0820-03



A

A

B

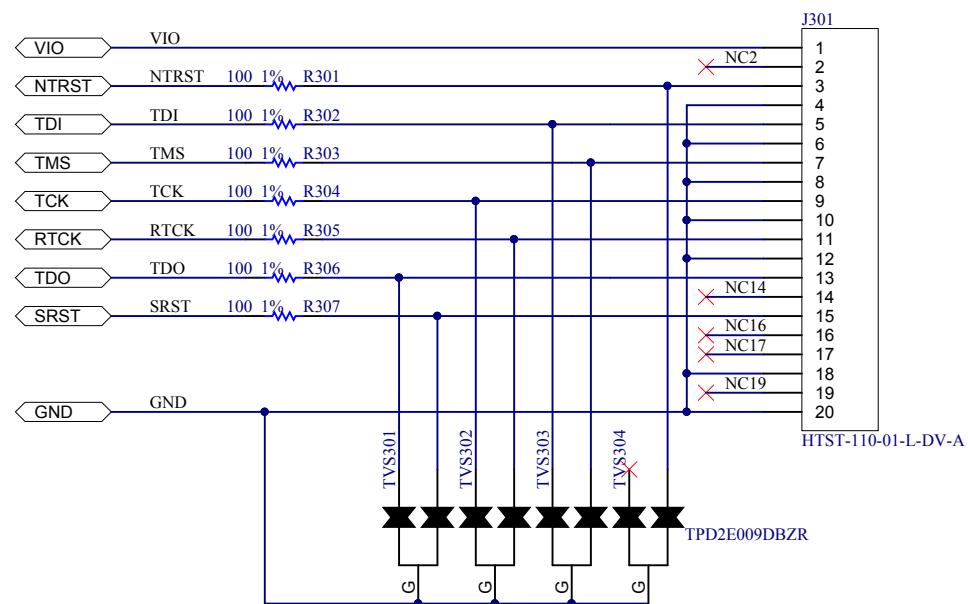
B

C

C

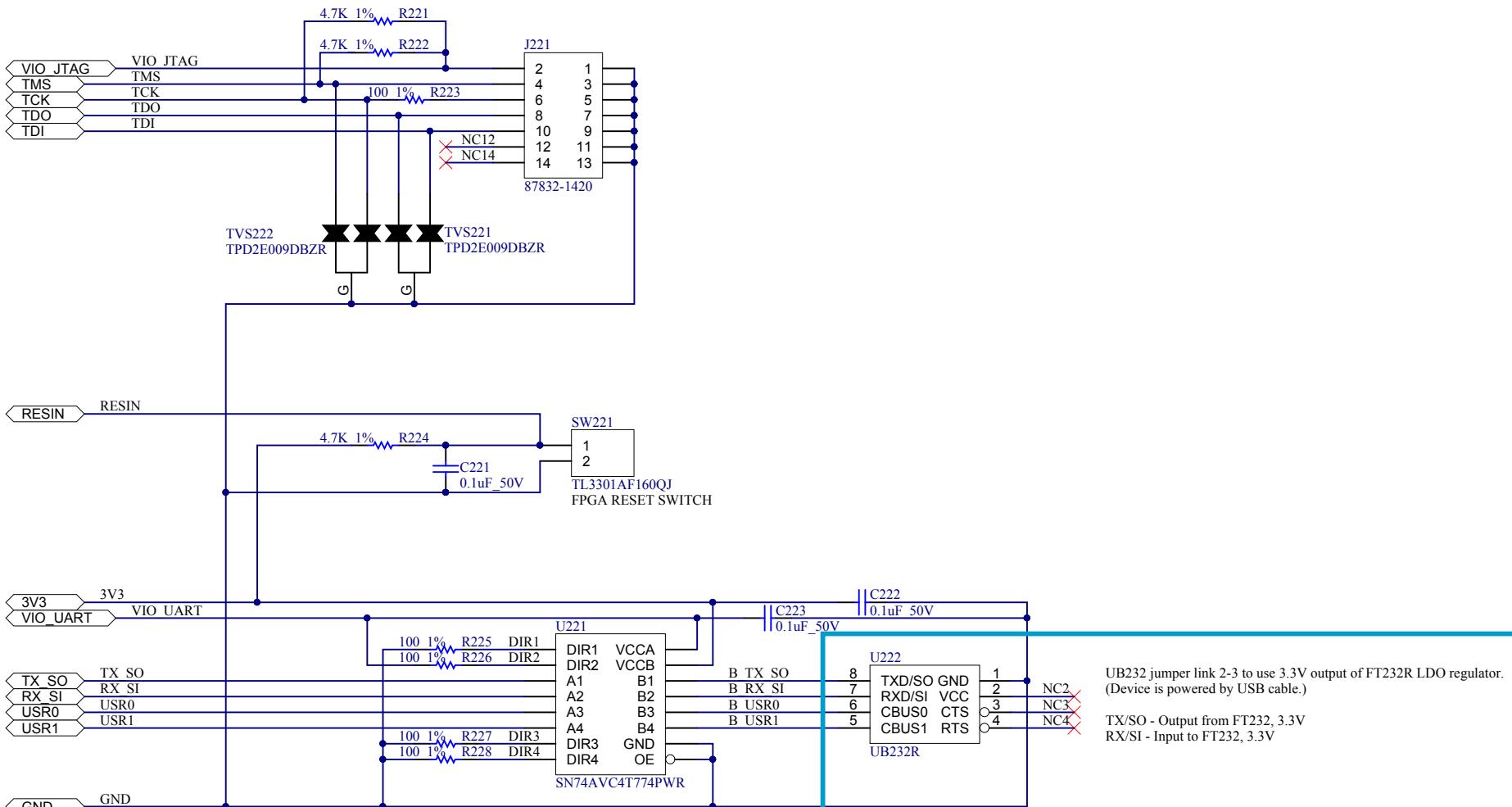
D

D

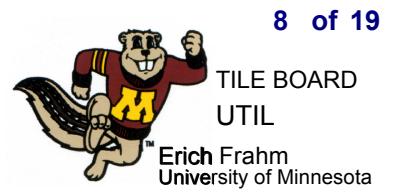


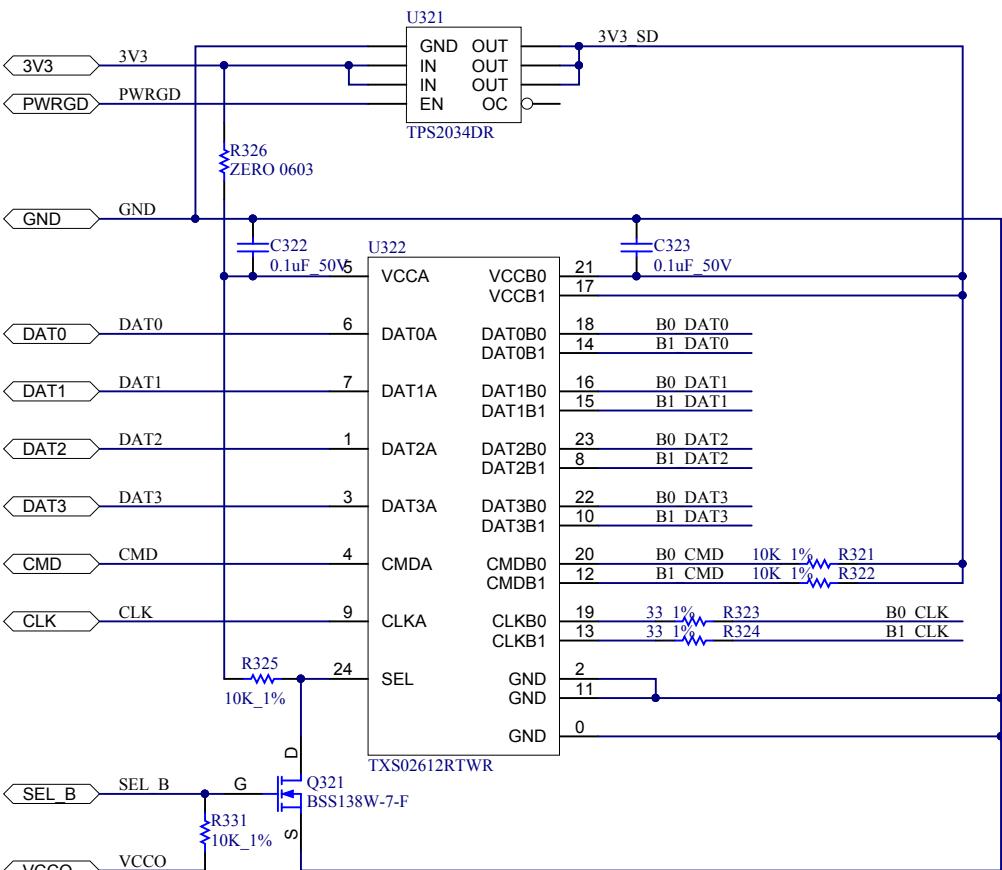
7 of 19



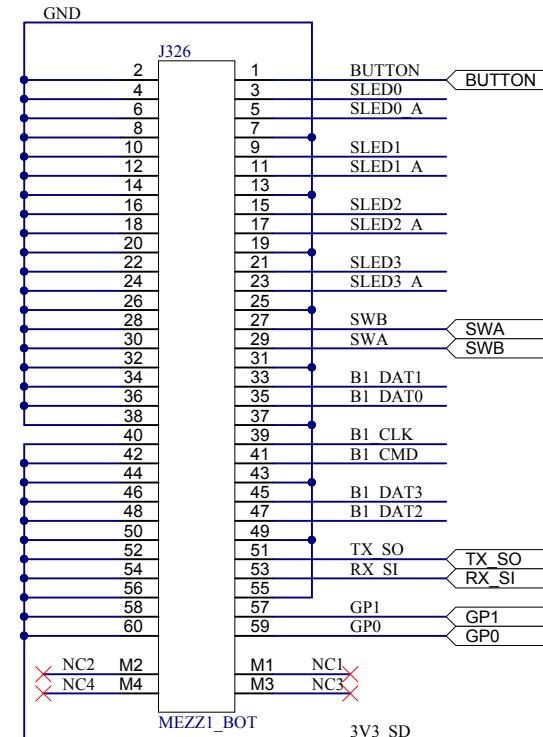


## UART TO USB MEZZANINE

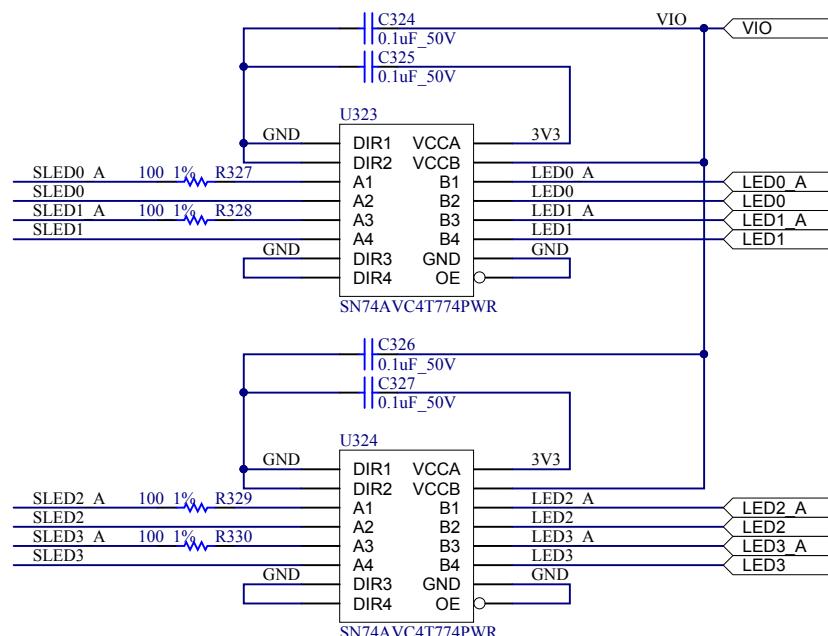




# SD MEZZANINE

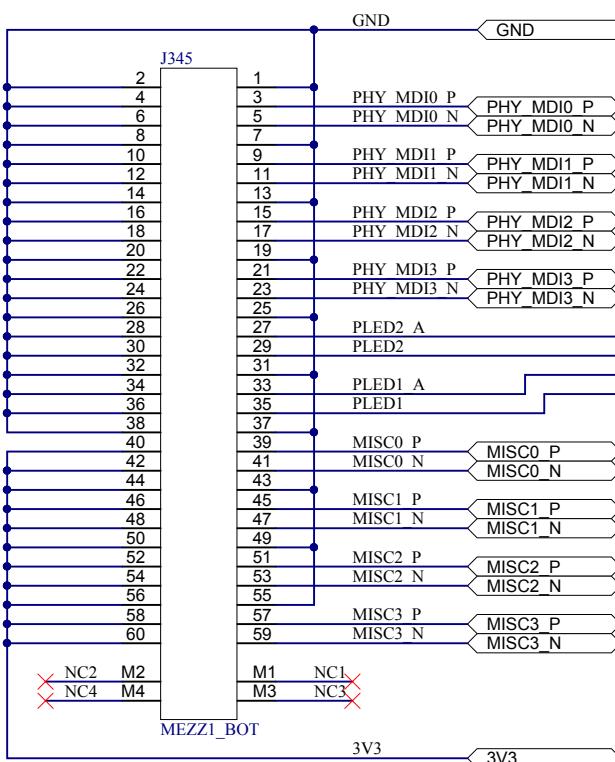


**J321** Also order 9774020151R  
ADD\_9774020151R  
**J322** Also order 9774020151R  
ADD\_9774020151R  
**J323** Also order 9774020151R  
ADD\_9774020151R  
**J325** Also order 9774020151R  
ADD\_9774020151R



A

## RJ45 MEZZANINE

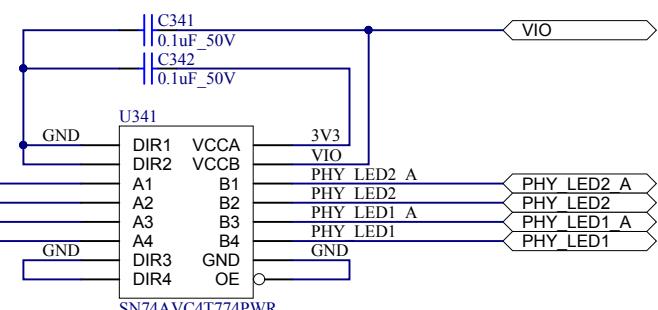


J341  
Also order 9774020151R  
ADD\_9774020151R

J342  
Also order 9774020151R  
ADD\_9774020151R

J343  
Also order 9774020151R  
ADD\_9774020151R

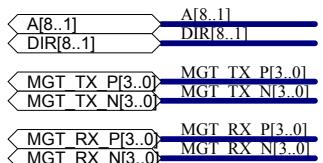
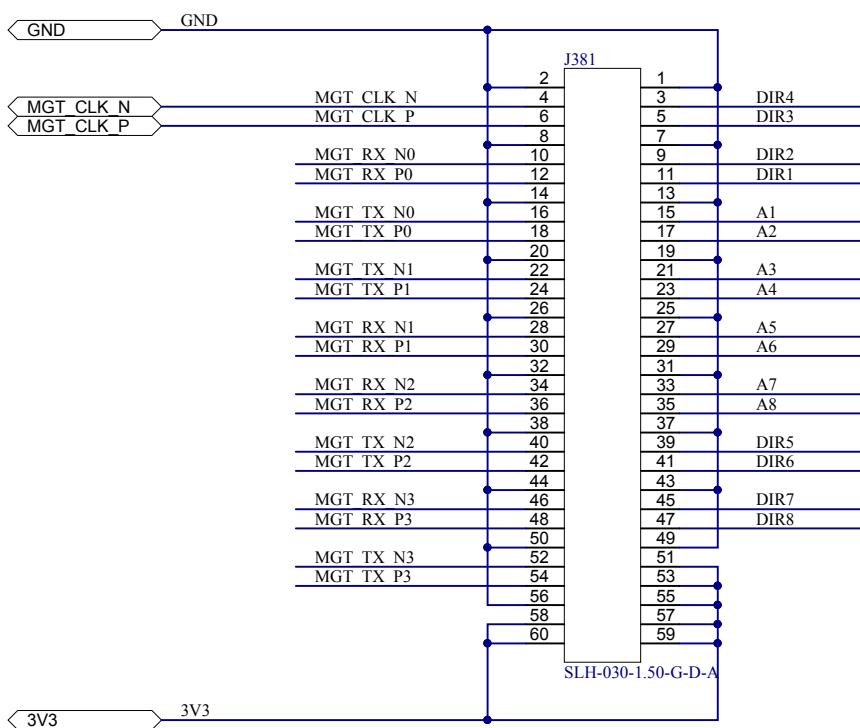
J344  
Also order 9774020151R  
ADD\_9774020151R



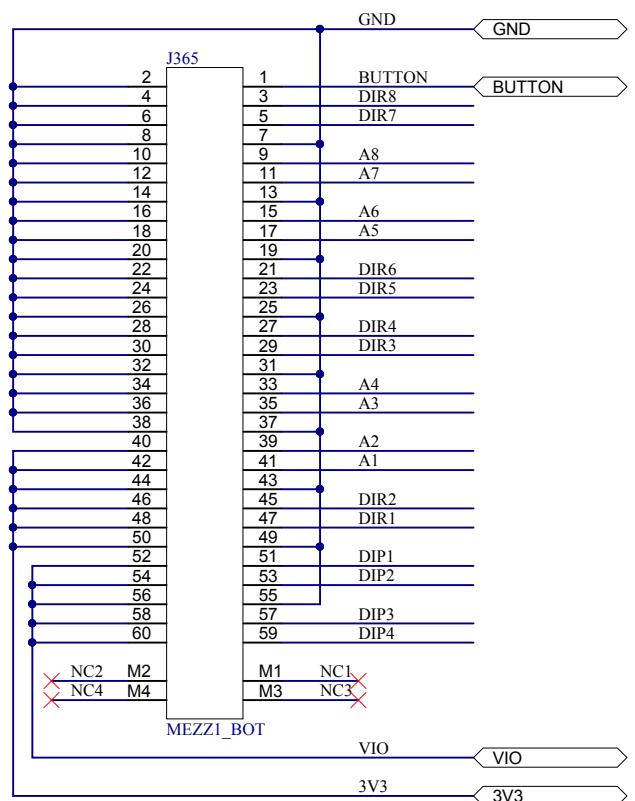
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# MGT MEZZANINE - DO NOT POPULATE



# MISC MEZZANINE



A[8..1]  
DIR[8..1]  
DIP[4..1]

J361

Also order 9774020151R

ADD\_9774020151R

J362

Also order 9774020151R

ADD\_9774020151R

J363

Also order 9774020151R

ADD\_9774020151R

J364

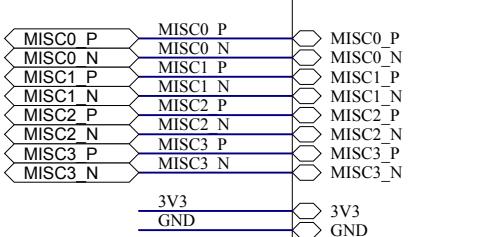
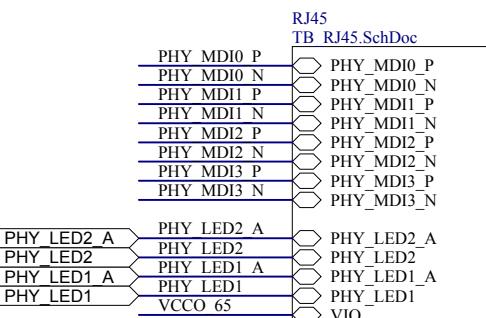
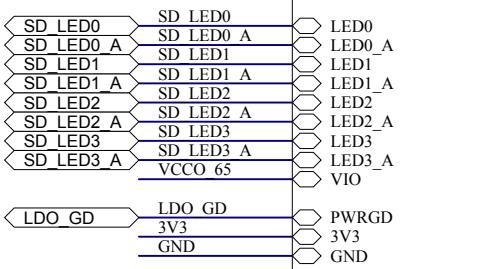
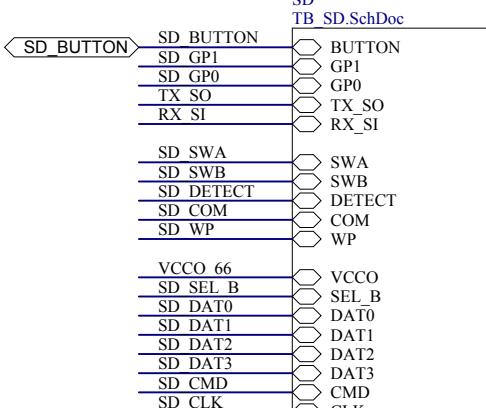
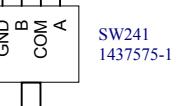
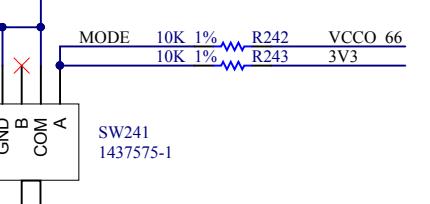
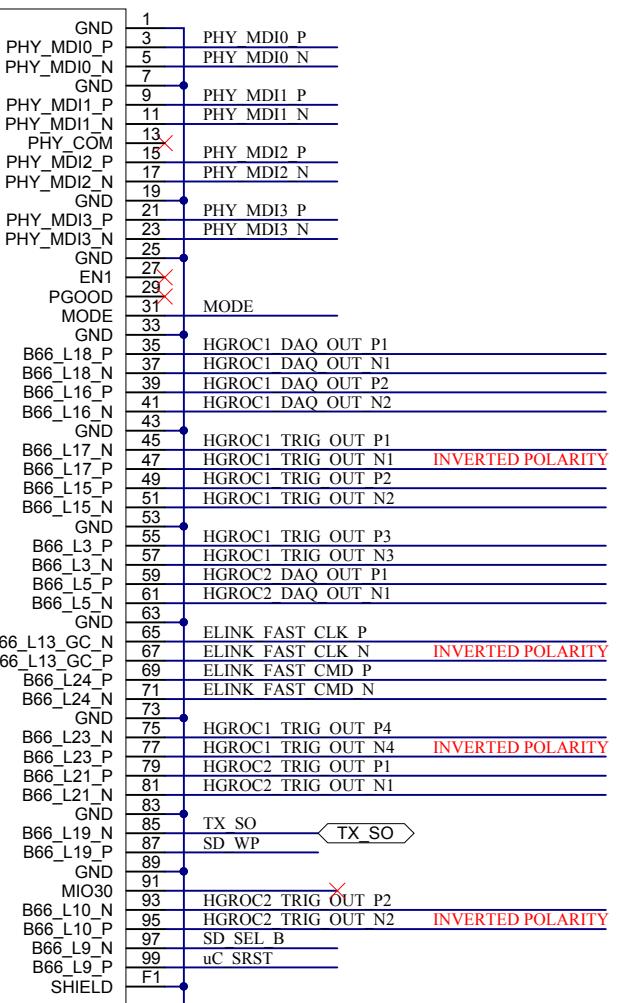
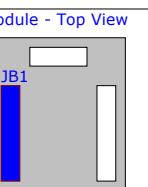
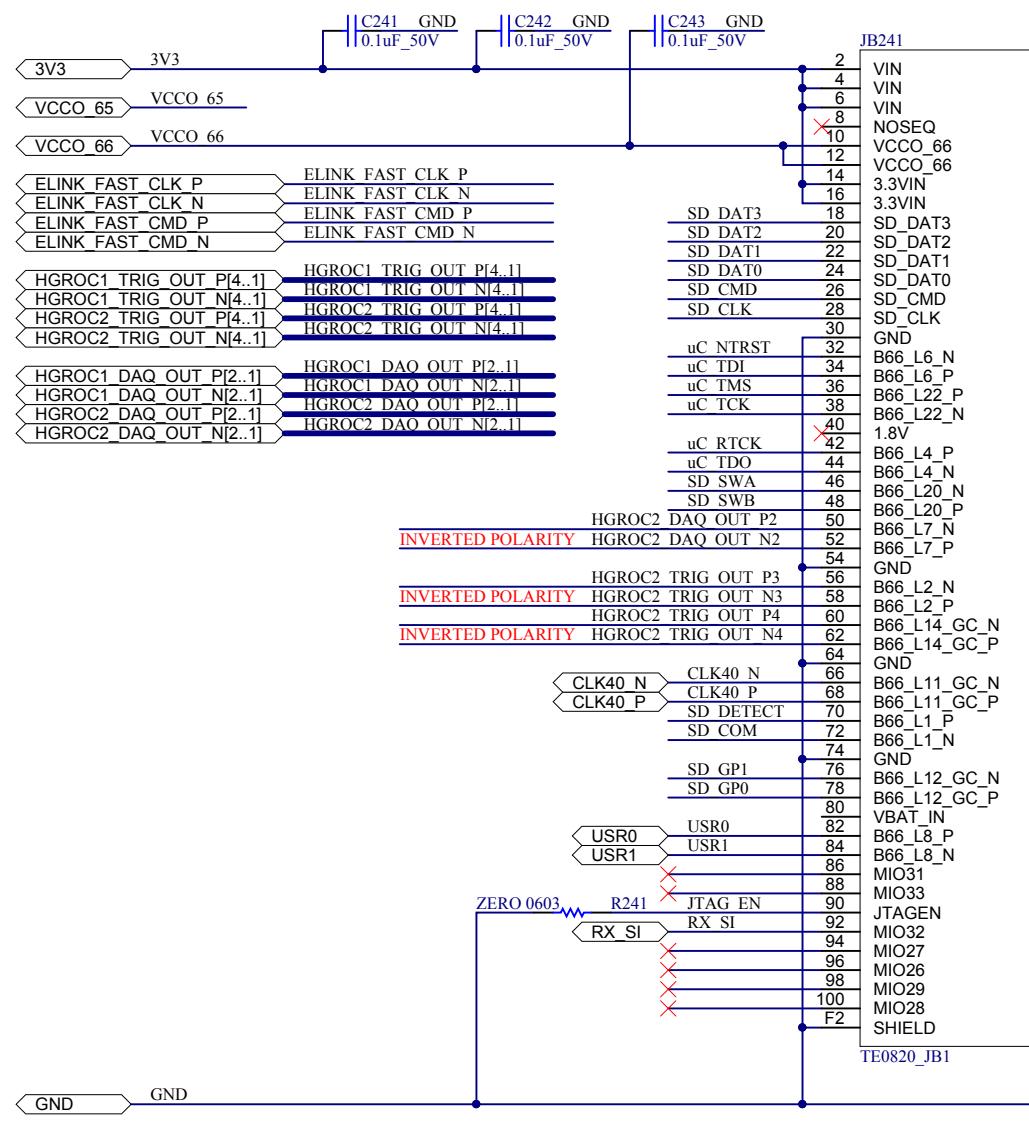
Also order 9774020151R

ADD\_9774020151R

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A

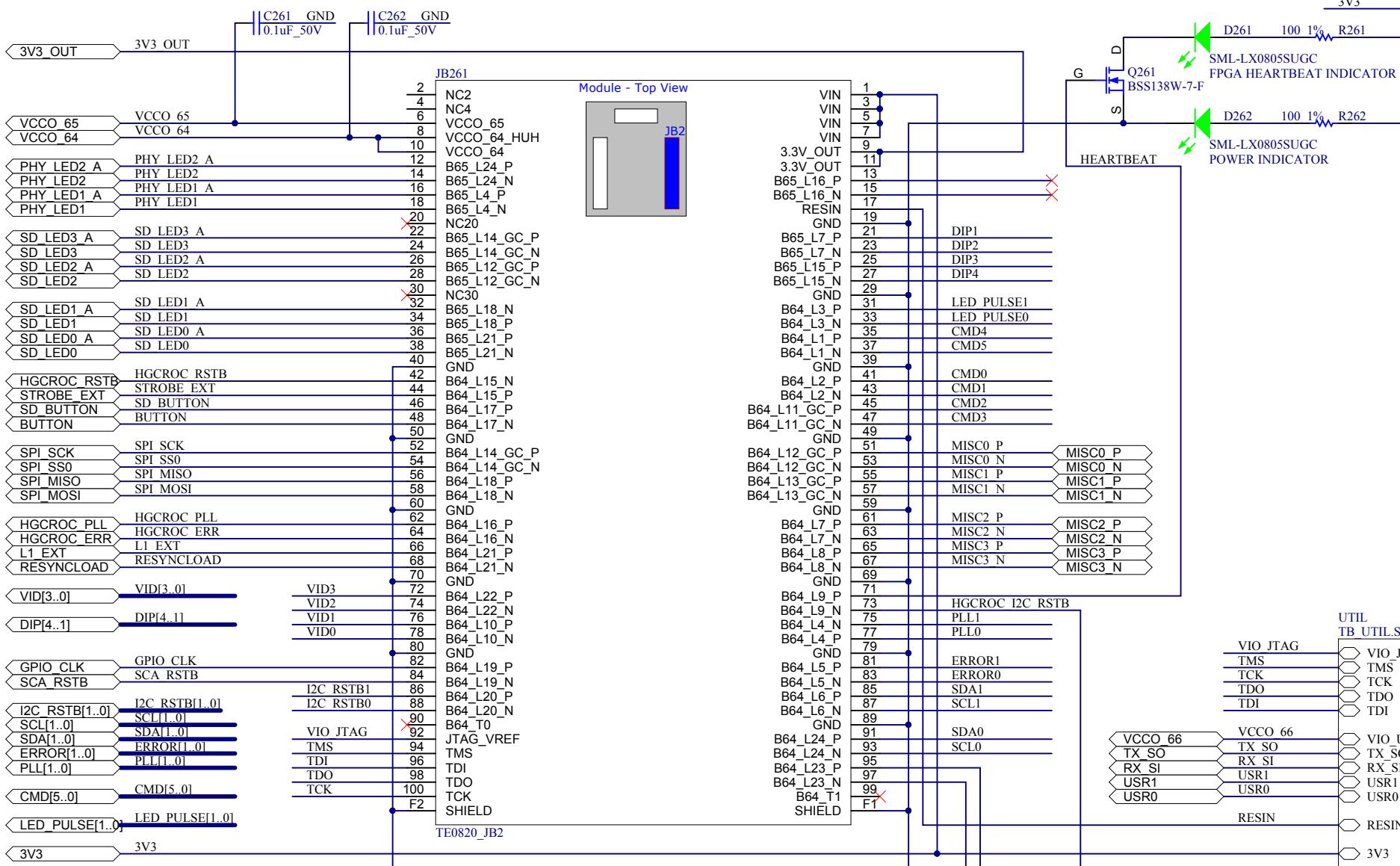


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**TILE BOARD  
JB1**  
Erich Frahm  
University of Minnesota

ARM  
TB\_ARM.SchDoc

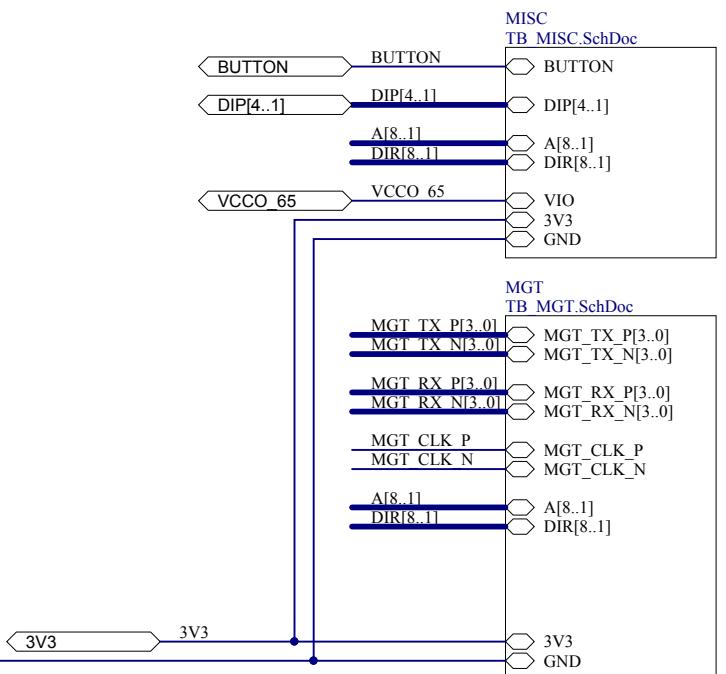
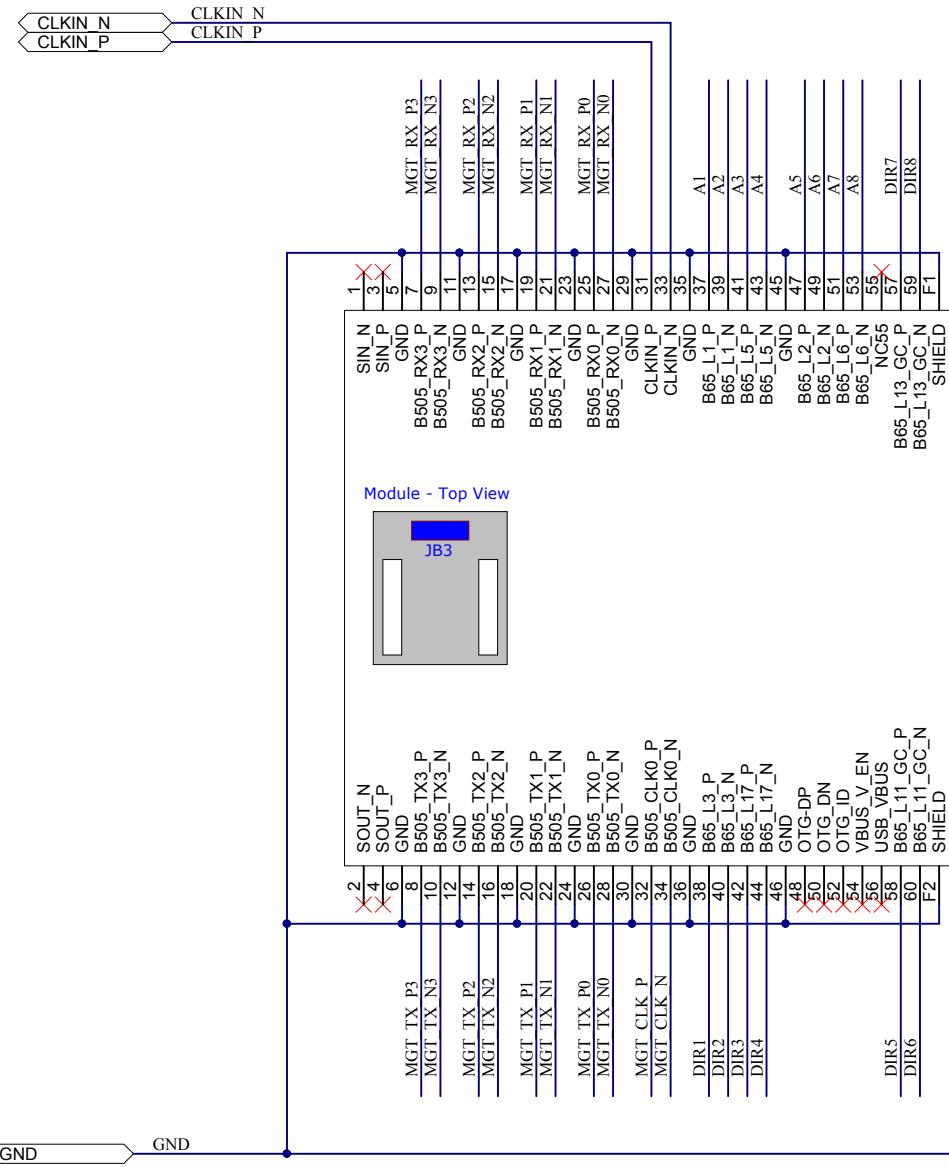
uC_TDI	TDI
uC_TDO	TDO
uC_TMS	TMS
uC_TCK	TCK
uC_NTRST	NTRST
uC_RTCK	RTCK
uC_SRST	SRST
VCCO_66	VIO
GND	GND



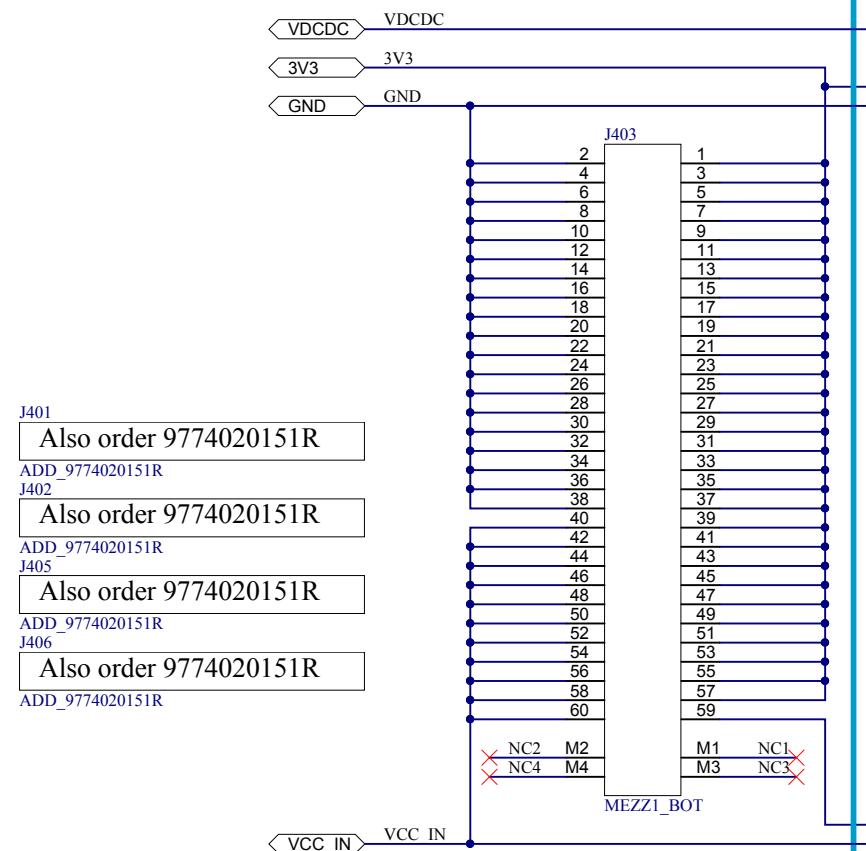
**BLANK\_MEZZ**

=====

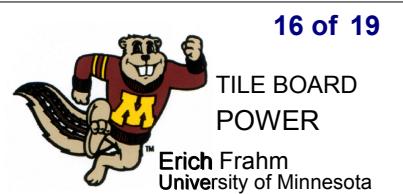
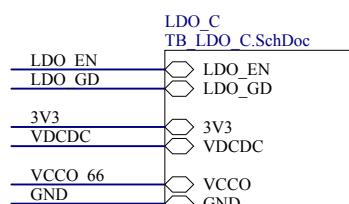
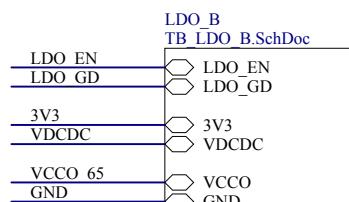
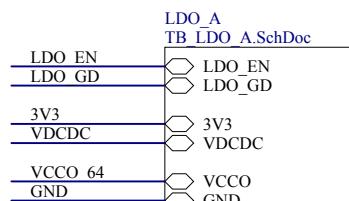
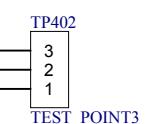
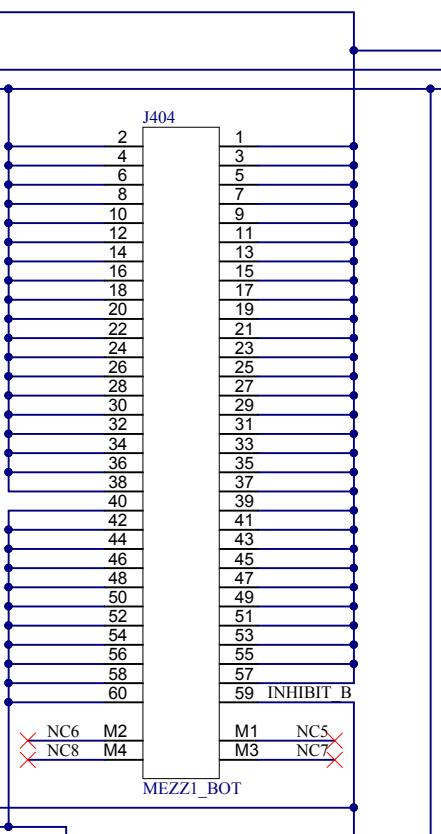
CMD0 = LINK\_TX\_P  
CMD1 = LINK\_TX\_N  
CMD2 = LINK\_CLK\_P  
CMD3 = LINK\_CLK\_N  
CMD4 = LINK\_RX\_P  
CMD5 = LINK\_RX\_N  
OSC\_P = 160MHZ\_P  
OSC\_N = 160MHZ\_N



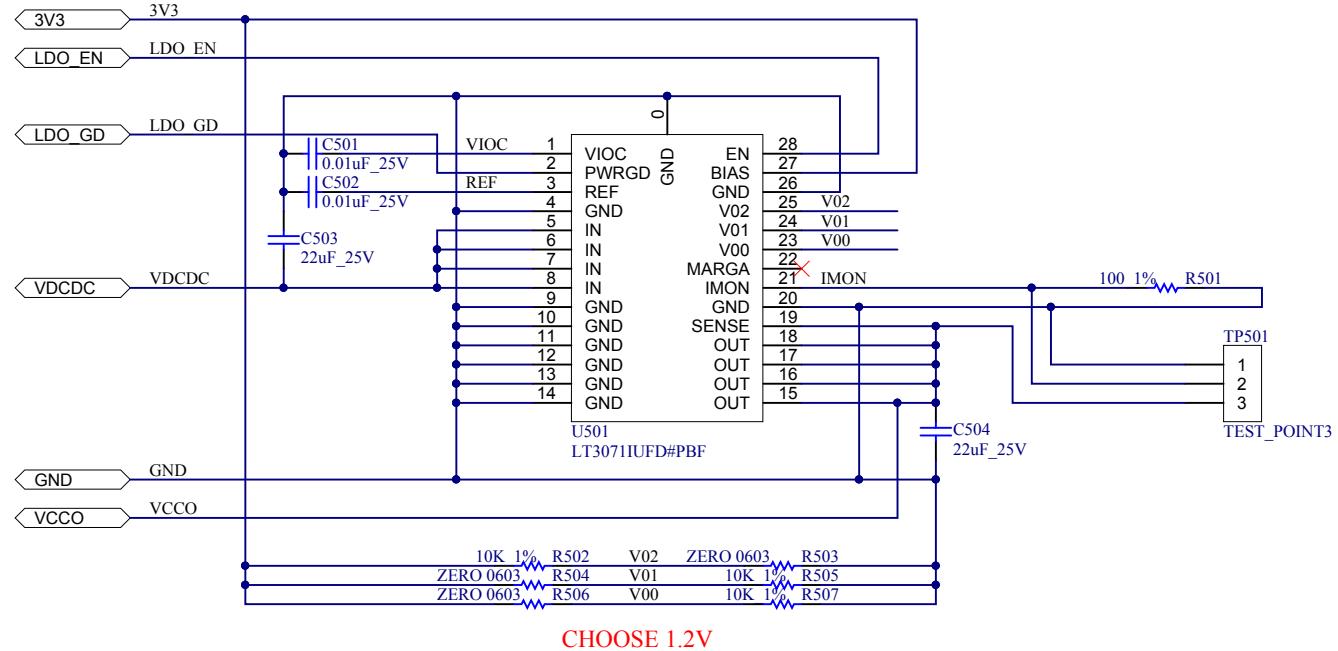
# DCDC MEZZANINE



# DCDC MEZZANINE



A



B

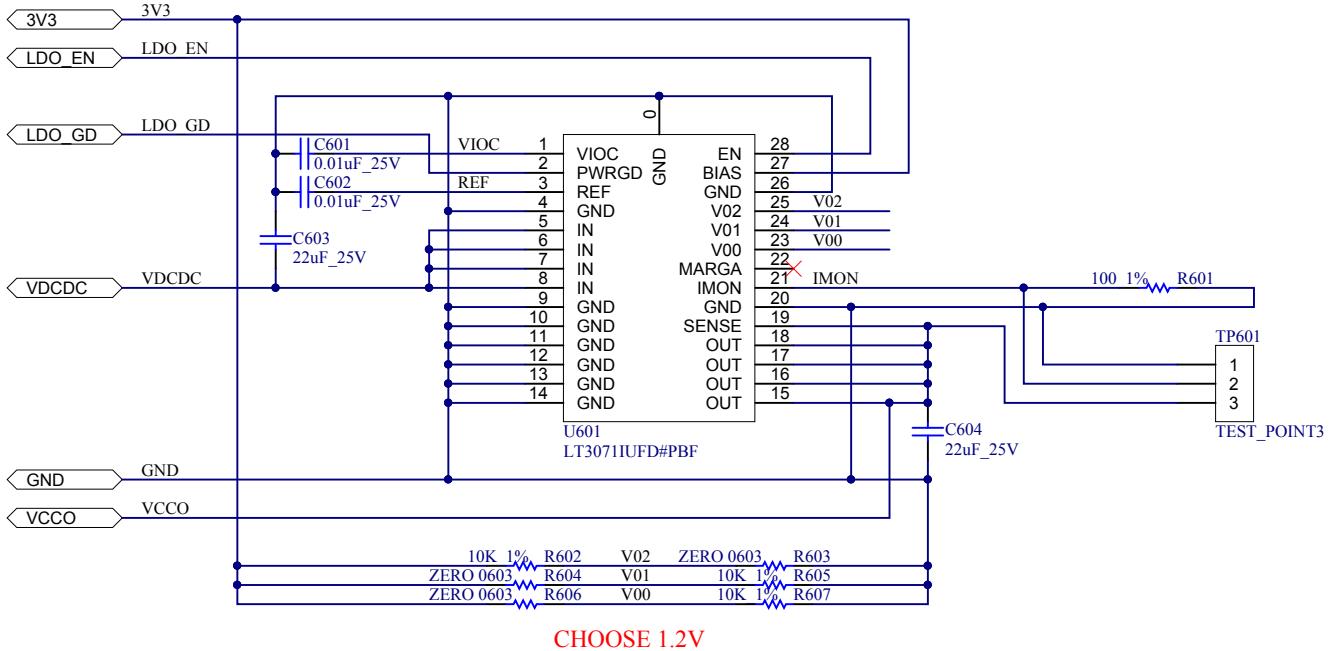
**Table 1:  $V_{O2}$  to  $V_{O0}$  Settings vs Output Voltage**

$V_{O2}$	$V_{O1}$	$V_{O0}$	$V_{OUT(NOM)}$	$V_{O2}$	$V_{O1}$	$V_{O0}$	$V_{OUT(NOM)}$
0	0	0	0.80V	Z	0	1	1.35V
0	0	Z	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	Z	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High

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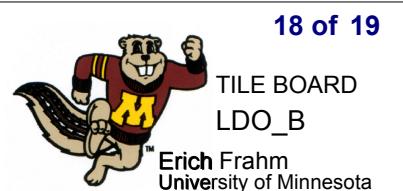




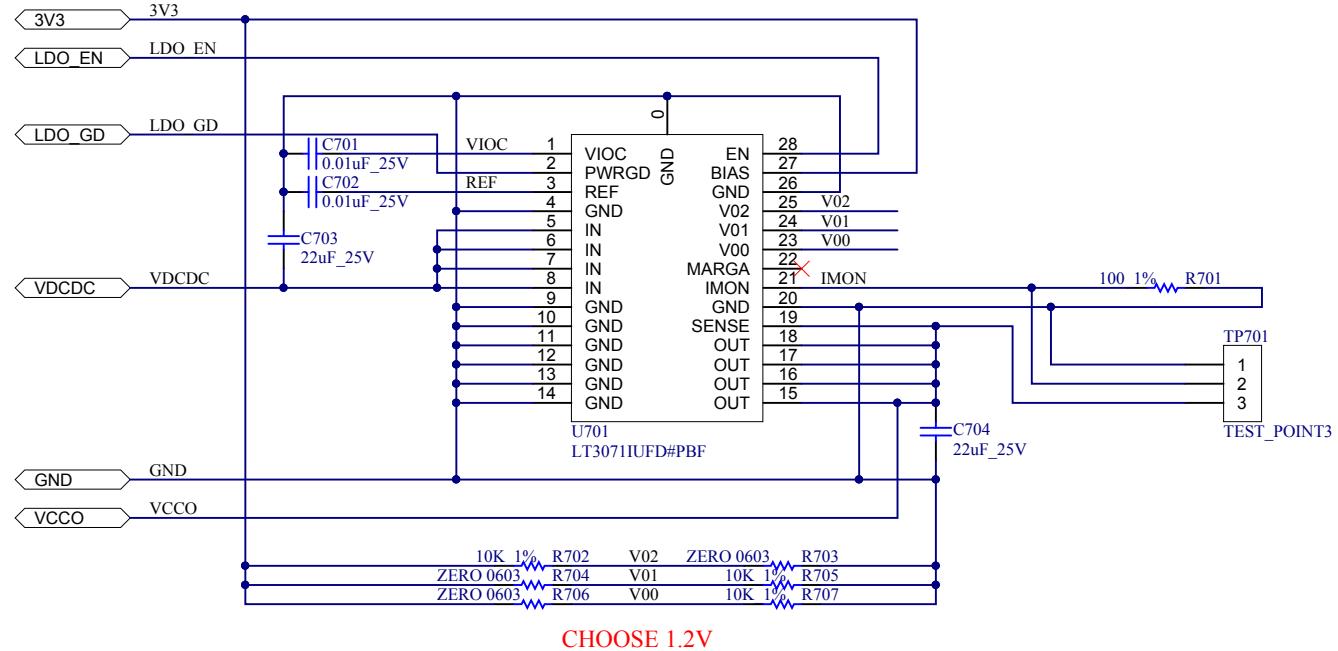
**Table 1: V<sub>O2</sub> to V<sub>O0</sub> Settings vs Output Voltage**

<b>V<sub>02</sub></b>	<b>V<sub>01</sub></b>	<b>V<sub>00</sub></b>	<b>V<sub>OUT(NOM)</sub></b>	<b>V<sub>02</sub></b>	<b>V<sub>01</sub></b>	<b>V<sub>00</sub></b>	<b>V<sub>OUT(NOM)</sub></b>
0	0	0	0.80V	Z	0	1	1.35V
0	0	Z	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	Z	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High



A

**Table 1: V<sub>O2</sub> to V<sub>OO</sub> Settings vs Output Voltage**

V <sub>O2</sub>	V <sub>O1</sub>	V <sub>OO</sub>	V <sub>OUT(NOM)</sub>	V <sub>O2</sub>	V <sub>O1</sub>	V <sub>OO</sub>	V <sub>OUT(NOM)</sub>
0	0	0	0.80V	Z	0	1	1.35V
0	0	Z	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	Z	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High

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