ECE385

Fall 2021

Experiment 1

Introductory Experiment

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1 Introduction

In this lab, we use NAND gates to build two versions of a 2 to 1 multiplexer using Quartus Prime. The purpose of this Lab is to have a better understanding of the static hazard (also called "Glitch") and implement a possible solution to avoid the static hazard.

2 Documentation

K-map To implement a 2 to 1 multiplexer, we can first create a K-map.

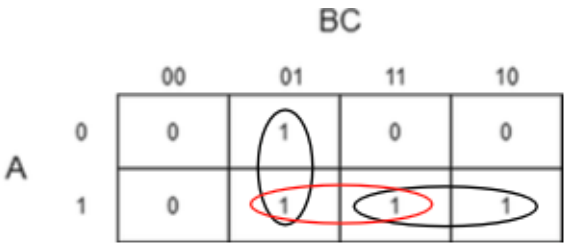

Figure 1: K-map for a 2 to 1 Multiplexer

Boolean equation By drawing the black circle, we can get the SOP Boolean equation quickly:

$$Z = BA + B^{'}C$$

However, delay may arise due to the additional NOT gate which is used to flip $inputB$, and this may cause static-1 hazard. To eliminate this, we can cover all adjacent min-terms in K-map. In this example, I choose to add a new red circle in my K-map to derive a new Boolean function:

$$Z = BA + B^{'}C + AC$$

A Logic Diagrams With Boolean function, we can start to build our 2 to 1 multiplexer using 7400 NAND gates. First we build the circuit with the original design that may have static hazard.

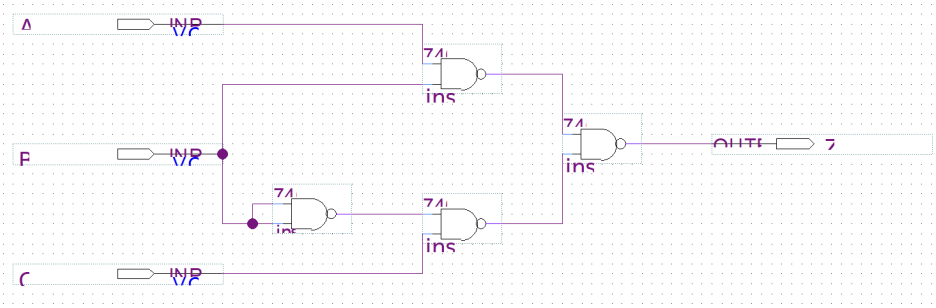

Figure 2: Circuit in Part A

Then, we can also build a new circuit with additional element which can help eliminate static hazard.

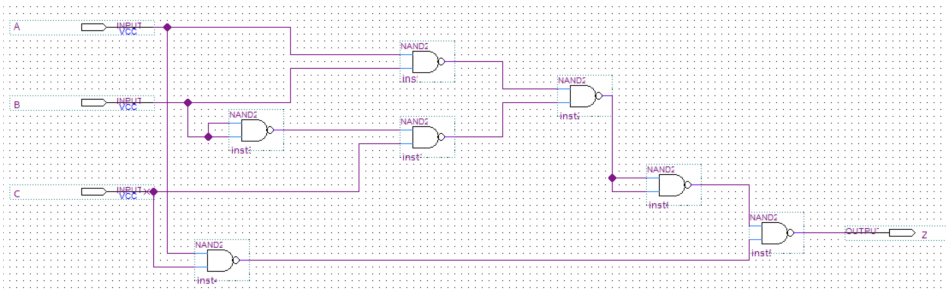

Figure 3: Circuit in Part B

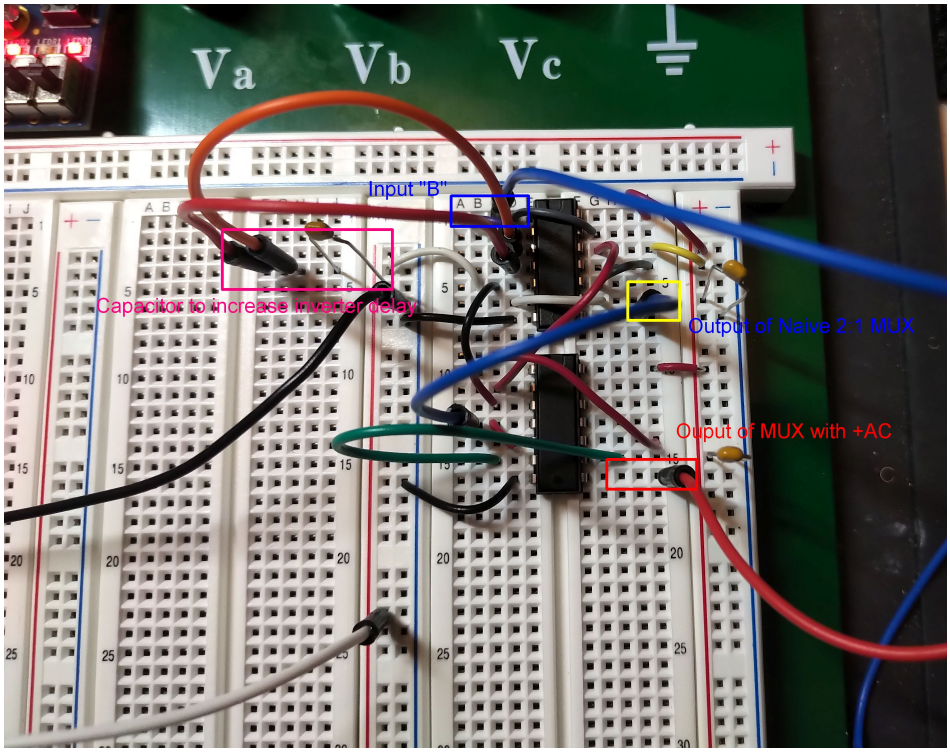

Figure 4: The layout of the circuit

3 Results in Lab

Truth table We can get a truth table through testing the circuit of part A by applying all possible input combinations using the three switches.
We use a 1 Mhz, 0 to 5 volt sqare wave to replace the input B. Then display input B on one channel of the scope and the circuit output on the other channel. The picture shows that the output is not always high as there is a period the wave drops.

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 1: Truth table for part A

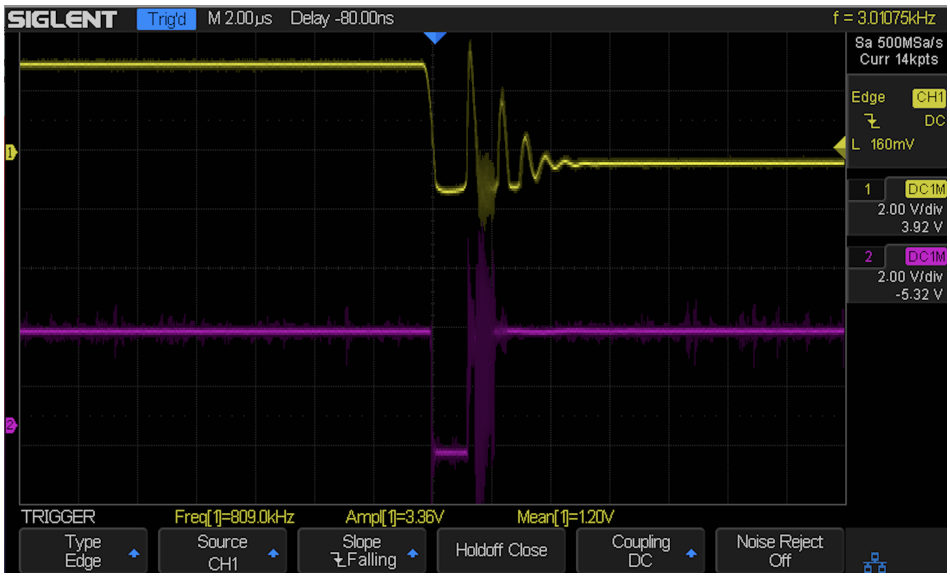

Figure 5: Result of original circuit with delay module

Then, we also test the circuit of part B by applying all possible input combinations using the three switches.

A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 2: Truth table for part A

Similarly, we apply the same experiment to our modified circuit. we can see that the output is almost always high and the static hazard is eliminated.

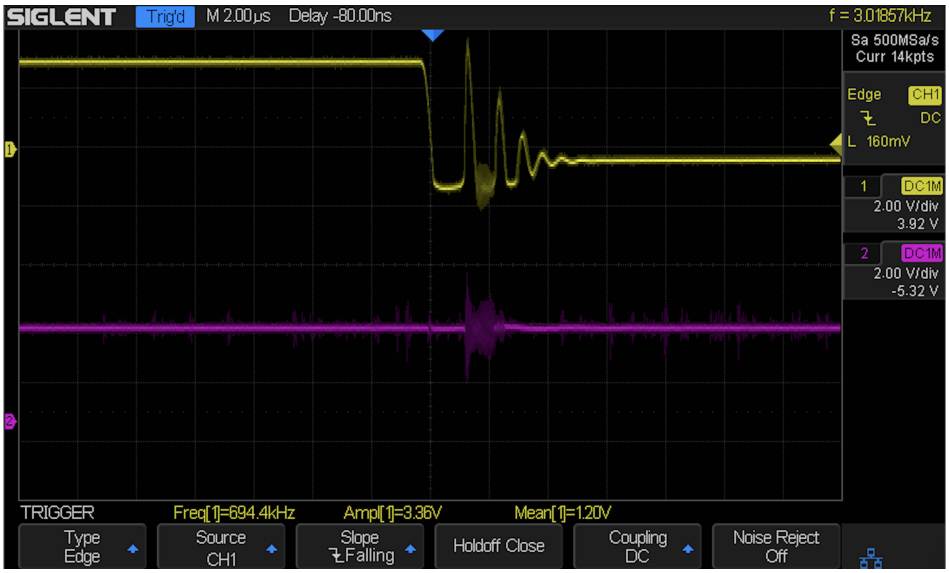

Figure 6: Result of modified circuit

4 Answer to the pre-lab question

4.1 Why does the hazard appear when you chain an odd number of inverters togerter?

Because the delay of one inverter is too small to notice, chaining many inverters will enlarge this phenomenon.

5 Answer to the lab question

5.1 Test the circuit in part B of the pre-lab. Complete a truth table of the output. Does it respond like the circuit of part A?

From above document, we can see that the truth table of the circuit in part B is the same as in part A.

5.2 Describe and save the output and explain any differences between it and the results obtained in part 2.

The outputs on the oscilloscope show that there is no glitch in circuit of part B, as the additional component logic AC cover the delay and eliminate the static 1 hazard.

5.3 For the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?

We are more likely to observe a glitch at the falling edge of the input B. Because in the rising edge, the logic transition before the last NAND gate is 10-¿00-¿01, and the output will always be 1. But for the falling edge, the logic transition before the last NAND gate is 01-¿11-¿10, and the output will goes to 0 in the middle.

6 Answer to the post lab question

6.1 Complete the timing diagram below for the circuit of part A.

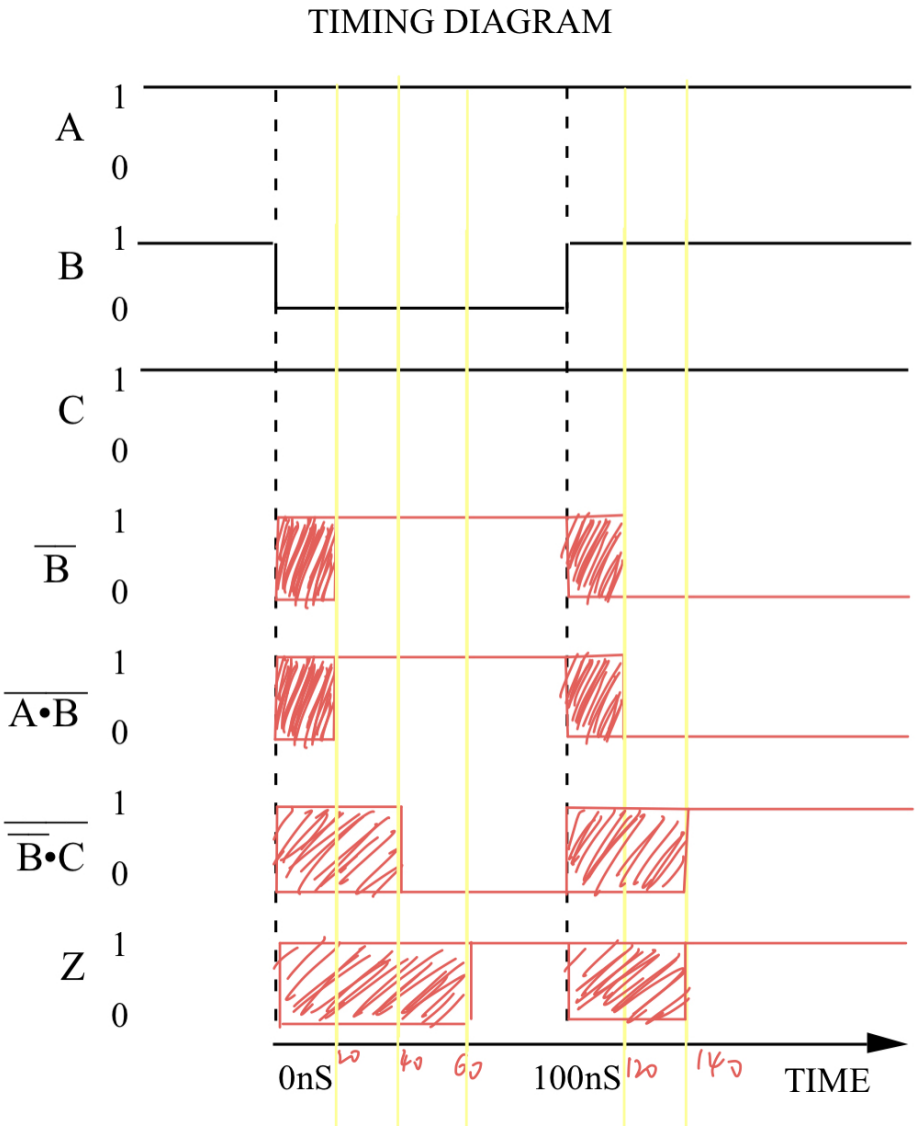

Figure 7: Timing Diagram

6.2 How long does it take the output Z to stabilize on the falling edge of B (in ns)? How long does it take on the rising edge (in ns)? Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.

It takes 60ns for output Z to stabilize on the falling edge of B
It takes 60ns for output Z to stabilize on the rising edge of B
Yes, there are potential glitches on Z. During the time between 40 to 60 ns, $\overline{AB}$ is 1 while $\overline{\overline{B}C}$ can be 1, which makes C to be 0. During the time between 120 to 140 ns, $\overline{AB}$ is 0 while $\overline{\overline{B}C}$ can be 0, which makes C to be 0.

7 Answer to the GG

7.1 What is the advantage of a larger noise immunity?

A large noise immunity will increase the stability of a circuit because the output will not be changed easily as the input voltage has some fluctuations.

7.2 Why is the last inverter observed rather than simply the first?

Because using more inverters can rules out occasional situations. By connecting inverters in series, if one of them has a flip between low and high, the output will sense it.

7.3 How would you calculate the noise immunity for the inverter?

If the ideal inverter always has the input signal in the middle of the nominal range, namely 0.35 V for logic "0" and 3.5 V for logic "1", the noise immunity for logic "0" will be 1.15 - 0.35 = 0.8 V, and the noise immunity for logic "1" will be 3.5 - 1.35 = 2.15 V. The overall noise immunity of the gate is the smallest of the ranges X and Y. In this case, $0.8 < 2.15$, so 0.8 V is the noise immunity for this gate. However, for an real world inverter, we should consider all the possible input within the nominal range. For logic "0", the maximun normal input is 0.7 V and it can tolerate up to 1.15 V, so the noise immunity for logic "0" will be 1.15 - 0.7 = 0.45 V. Similiarly, the noise immunity for logic "1" will be 2 - 1.35 = 0.65 V. The overall noise immunity of the gate is the smallest of the ranges X and Y. In this case, $0.45 < 0.65$, so 0.45 V is the noise immunity for this gate.

7.4 If we have two or more LEDs to monitor several signals, why is it a bad practice to share resistors?

Because if LEDs are connected in parallel.The current is divided into several small ones as the total current remains the same. Each unit may be too small to make the LED light.

8 Conclusion

This lab is about static hazard. Sometimes static hazard may happen as there are delays in some path of the circuit, which may influence the output. To eliminate static hazard, we can add additional terms to cover all adjacent min-terms in the K-map. Generally, nothing unexpected happened in this lab.