AN70707

EZ-USB® FX3 Hardware Design Guidelines

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Associated Part Family: CYUSB3014
Software Version: N/A
Associated Application Notes: None

Abstract

AN70707 discusses recommended practices for EZ-USB® FX3 hardware design and the critical items that a developer must consider. The Cypress EZ-USB FX3 is the next generation USB 3.0 peripheral controller. With its highly integrated and flexible features, developers can add USB 3.0 functionality to any system.

Introduction

The Cypress EZ-USB FX3 has an integrated USB 3.0 and USB 2.0 physical layer (PHY), and a fully configurable, parallel, general programmable interface called GPIF II, which can connect to an external processor, ASIC, or FPGA. EZ-USB FX3 enables data transfers up to 320 MBps from GPIF II to the USB interface.

To successfully add this high throughput pipe to a system, a developer must take care when designing the system. You should apply techniques for high-speed to systems that use the EZ-USB FX3 device. Because of the packaging and high performance characteristics of the EZ-USB FX3 device, you should follow the guidelines for trace width, stack up, and other layout considerations to make sure the system will perform as expected.

Booting

EZ-USB FX3 can be either the main processor in a system or a co-processor. The booting option you use depends on the specific system implementation. PMODE[2:0] configures the boot option and can be connected directly to the main processor or hardwired on the board depending on the booting option that will be used. The following table shows the levels of the PMODE[2:0] signals required for the different booting options.

PMODE[2:0]	Boot from
F00	Sync ADMUX (16-bit)
F01	Async ADMUX (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I^2C, on failure, USB boot is enabled
1FF	I^2C only
0F1	SPI, on failure, USB boot is enabled

If an external EEPROM is used on the I^2C bus, 1 KΩ pull-up resistors should be placed on the SCL and SDA lines for up to 1 MHz EEPROM communication.

Clocking

You can use either a crystal or an external clock as the clocking source for EZ-USB FX3. Crystal supports only 19.2 MHz, while an external clock can support 19.2 MHz, 26 MHz, 38.4 MHz, and 52 MHz.

Based on the clocking option that is used, the FSLC[2:0] lines can be tied to power or ground .The following table shows the values of FSLC[2:0] for the different clocking options.

CVDDQ supply is the supply associated with the clock input. It should be set to the same voltage level as the external clock input.

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/clock frequency
0	0	0	19.2 MHz crystal
1	0	0	19.2 MHz input clock
1	0	1	26 MHz input clock
1	1	0	38.4 MHz input clock
1	1	1	52 MHz input clock

If only external clock input is used, the XTALIN and XTALOUT pins can be left unconnected. If only crystal clocking is used, the CLKIN pin can be left unconnected.

A 32.768 KHz clock input can be used for watchdog timer operation during suspend mode. This may be optionally supplied by an external source.

Device Supply Decoupling

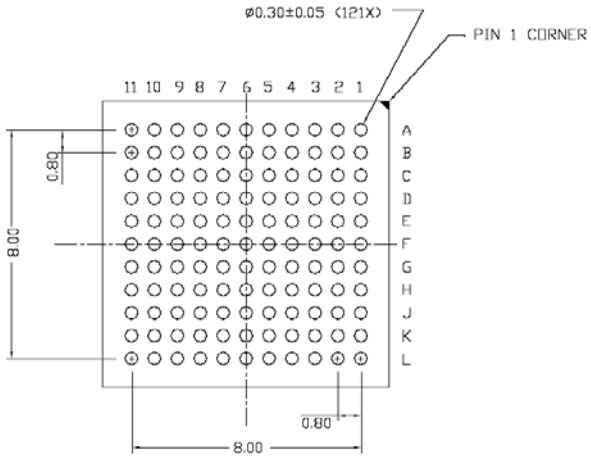
Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB bus, which results in higher CRC error rate and more retries. Decoupling capacitors should be ceramic type of a stable dielectric. It is important to have the decoupling caps as close to the power pins as possible and short trace runs for the power and ground connections on the EZ-USB FX3 device to solid power and ground planes.

The specific recommendation for the ceramic capacitor nearest to each EZ-USB FX3 power pin is given in the following table.

Cap Value	Number of caps	Pin Name
0.1 uF, 0.01 uF	4 of each	VDD
0.1 uF, 2.2 uF	1 of each	AVDD
0.1 uF, 2.2 uF	1 of each	U3TXVDDQ
0.1 uF, 2.2 uF	1 of each	U3RXVDDQ
0.1 uF, 0.01 uF	1 of each	CVDDQ
0.1 uF, 0.01 uF	1 of each per supply	VIO1-5

PCB Footprint

EZ-USB FX3 is packaged on a 10 x 10 mm, 0.8 mm pitch ball grid array (BGA). The recommended pad size is 0.241 mm (9.5 mil). Pitch is 0.8 mm and package is 10 x 10 mm.



EMI and ESD Considerations

You must consider EMI and ESD on a case-by-case basis relative to the product enclosure, deployment environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI, but only gives general EMI and ESD considerations.

EZ-USB FX3 has built-in ESD protection on the D+, D- and GND pins on the USB interface. The ESD protection levels given on these ports are:

- ±2.2 kV human body model (HBM) based on ±6 kV Contact Discharge and ±8 kV Air Gap Discharge based on IEC61000-4-2 level 3A
- ±8 kV Contact Discharge and ±15 kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device will continue to function after ESD events up to the levels stated.

The SSRX+, SSRX-, SSTX+, SSTX- pins have only up to ±2.2 kV Human Body Model (HBM) internal ESD protection. You can include additional protection to these pins by using high performance, low capacitance external ESD devices. To prevent an effect on the performance of this bus, the added capacitance should not exceed 0.4 pF.

In terms of EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, these emissions must be minimized. You can use several techniques to lower EM emissions:

- Consider putting the power and ground planes as the outside layers with signal layers underneath.
- Always have solid copper fills beneath integrated circuits and clocks.
- Ensure an adequate ground return path for all signals.
- Minimize the trace length of high speed, high current traces.

Electrical Design Consideration

USB 3.0 protocol enhances USB speed up to 5 Gbps. By including SuperSpeed lines along with High Speed lines, it is backward compatible with the USB 2.0 specification. Both buses require a greater level of attention to electrical design. Careful attention to component selection, supply decoupling, signal line impedance, and noise are required when designing for SuperSpeed USB. These physical issues are mostly affected by the PCB design.

USB 3.0 SuperSpeed Design Guidelines

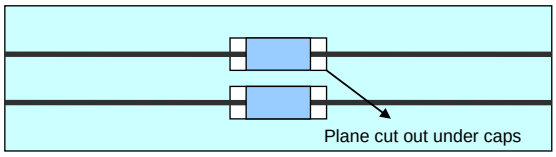
EZ-USB FX3 has SuperSpeed USB lines and High Speed USB lines. Use the following best practices when designing with these busses:

For detailed High Speed routing guidelines, see *AN1168 - High-Speed USB PCB Layout Recommendations*.

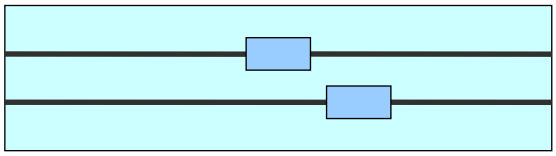
- Minimize USB lines as much as possible. These should be routed first to make sure certain recommendations on this list are achievable.

Long traces affect the transmitter quality and introduce intersymbol interference (ISI) on the receive side.

- The polarity can be swapped on the USB 3.0 differential pairs. Given that the USB connector pin-out is defined, this is a mechanism to ensure that these traces do not cross each other. Polarity detection is done automatically by the USB 3.0 PHY during link training and does not require any additional changes to device Firmware.
- Tie the R_USB2 pin to ground through a 1% 6.04 KΩ precision resistor. R_USB3 pin should be tied to ground through a 1% 200 Ω precision resistor.
- USB 3.0 traces require additional AC coupling capacitors (0.1 uF) placed on the SS_TX lines. Place these capacitors symmetrically and close to the FX3 device.
- Two immediate planes underneath these AC coupling capacitors should have a cut out in the shape of these capacitors to avoid extra capacitance on the lines because of the capacitor pads.

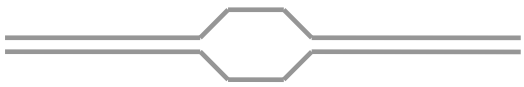


Recommended



Not recommended

- USB signal line impedance should be 90 Ω differential (±7%).
- Keep trace spacing between differential pairs constant to avoid impedance mismatches.

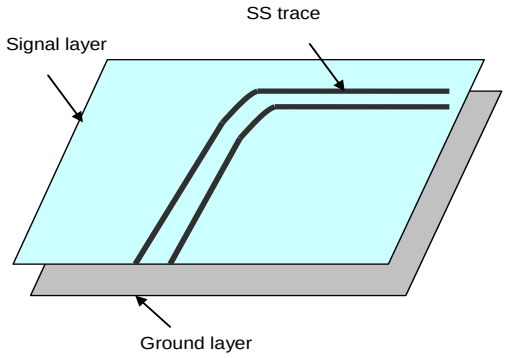


Not recommended

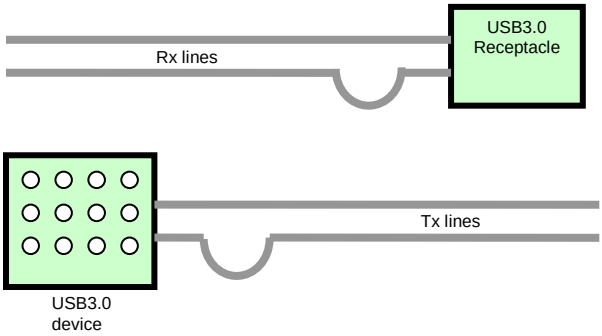
Not recommended

Recommended

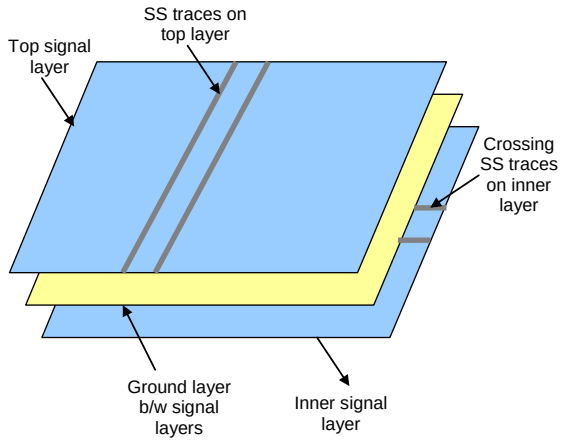
- All SS signal lines should be routed entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the SS signals increases loop inductance, introduces impedance mismatches and increases electrical emissions.



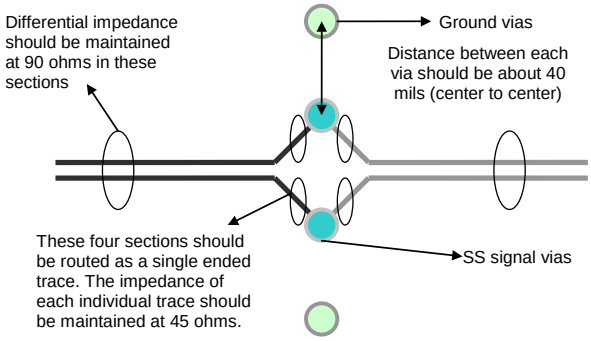
- Differential SS pair trace lengths should be matched within 0.12 mm (5 mils). The HS D+ and D– signal trace lengths should be matched within 1.25 mm (50 mils). Adjustment for HS signals should be made near the USB receptacle, if necessary. Adjustments for SS Rx signals should be made near the USB receptacle, while adjustments for SS Tx signals should be made near the device, if necessary.



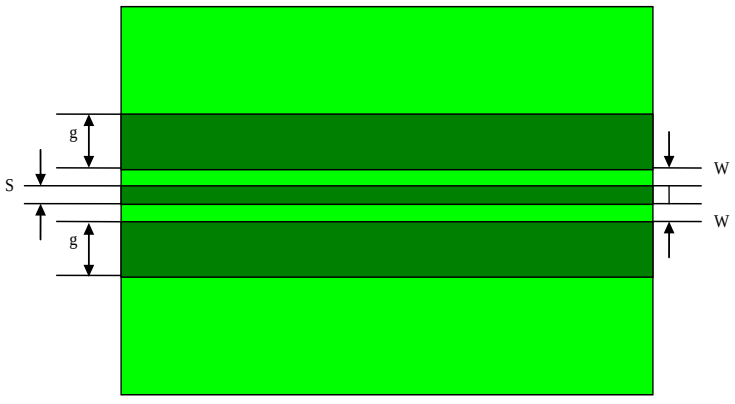
- The number of layers on the PCB should at least be four. To maintain 90 Ω differential impedance, use a solid reference power plane.
- Any time two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers.



- If signal routing has to be changed to another layer, continuous grounding has to be maintained to ensure uniform impedance throughout. The distance between the signal and ground vias should be at least 40 mils.



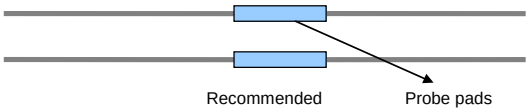
- Maintain constant trace width in differential pairs to avoid impedance mismatches.

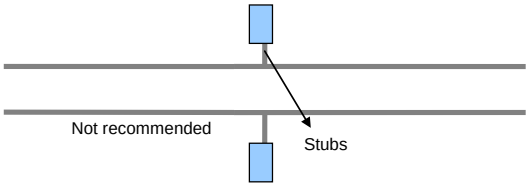


The following table defines the recommended parameters in the previous diagram.

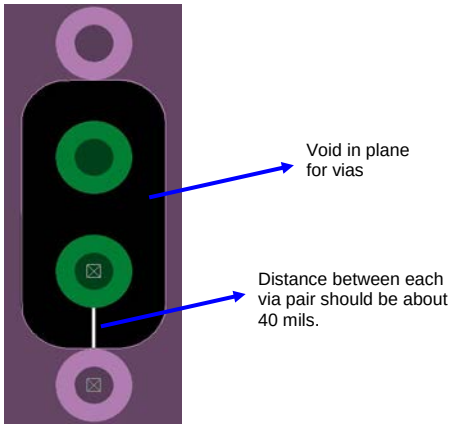
S	Intra pair spacing	8 mils
W	Trace width	11 mils
g	Minimum gap b/w trace and other planes	8 mils

- Avoid stubs on all USB lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub.

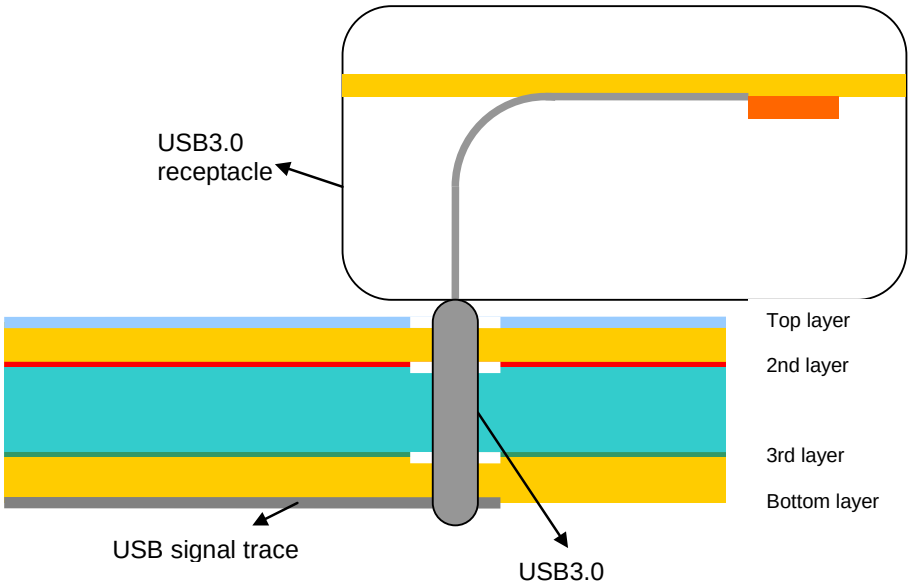




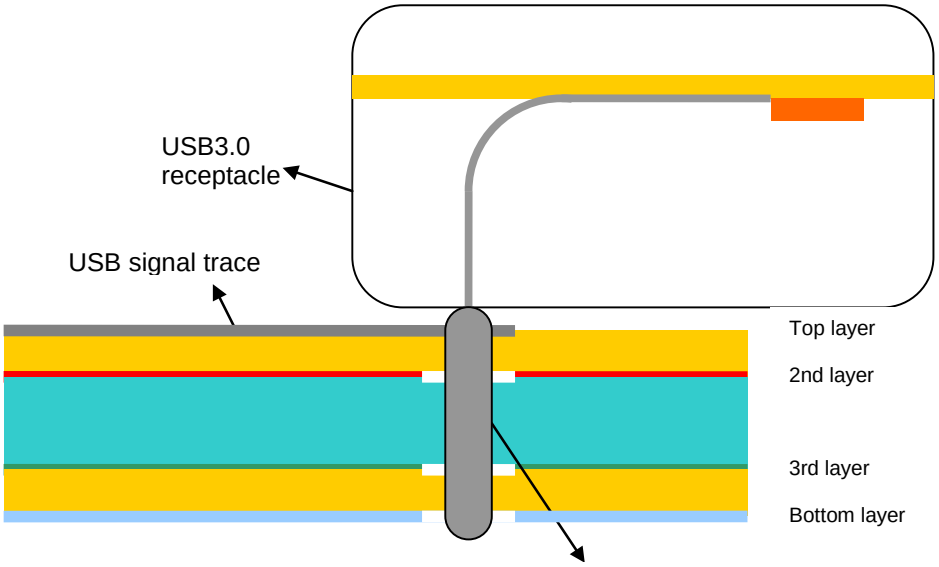
- Void for vias on the SS signal lines should be common for the differential pair. Having a common void, as shown in the following figure, maintains better impedance matching in comparison to separate vias.



- It is highly recommended that, when using a Type B receptacle (through hole receptacle), the USB signal lines be connected to the receptacle pins on the opposite layer of where the receptacle is placed. For example, if the Type B receptacle is placed on the top layer, the signal lines should connect to the receptacle pins on the bottom layer. This will prevent the unnecessary stubs due to the USB receptacle pins, as shown in the following figure.

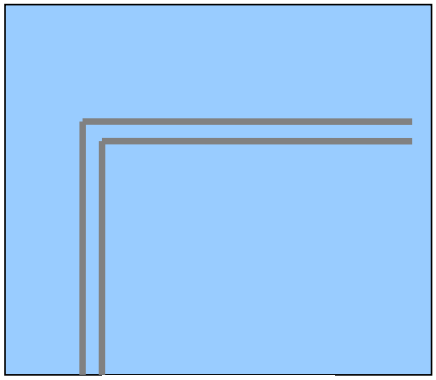


PCB cross-section view: The USB3.0 receptacle through hole pin acts as a part of the signal trace, thus eliminating the possibility of a stub on the signal line.

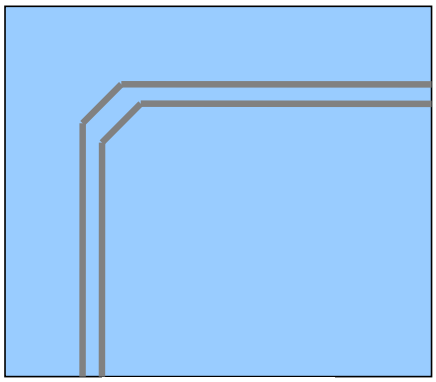


PCB cross section view: The USB3.0 receptacle through hole pin acts a stub to the USB signal trace

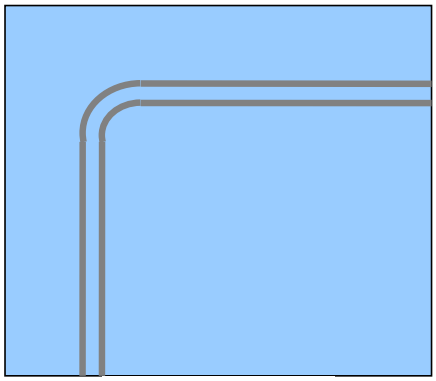
- Connect the “shield” pins on the USB 3.0 receptacle to ground through an inductor for AC isolation.
- On the USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45 degrees or rounded (curved) bends if necessary.



Not recommended

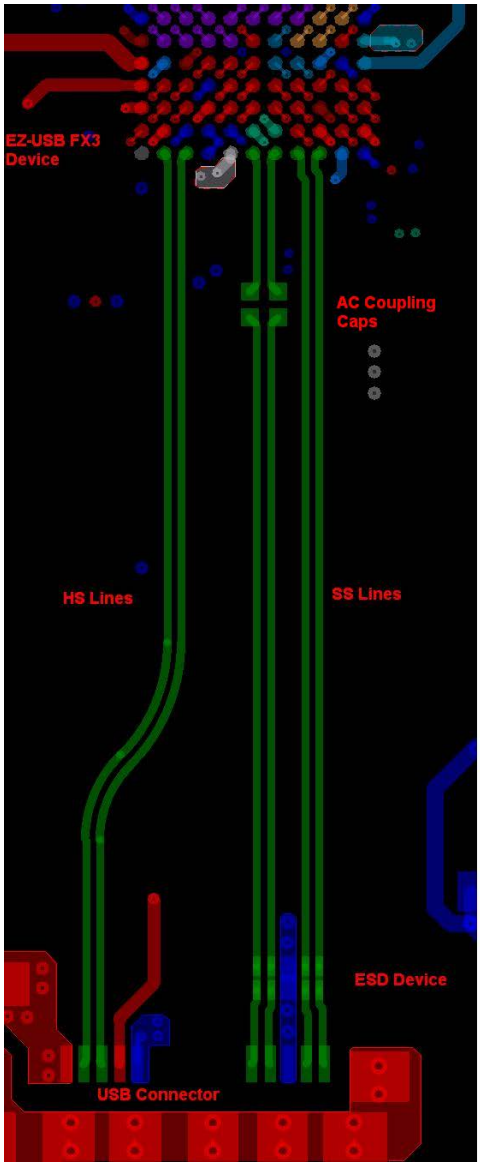


Recommended



Recommended

- To avoid cross talk, do not place the differential pairs close to other differential pairs, clock signals, or any other high-speed signals.
- The following image shows an example of routing the USB signals from the FX3 device to the USB 3.0 Micro B receptacle. Each differential pair should be kept uniform throughout the trace. Place AC coupling caps as close to the device as possible. ESD devices should be placed as close to the receptacle as possible.



Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3312933	HFO	07/14/2011	New application note.
*A	3381402	MRKA	09/23/2011	Updated trace adjustment diagram. Updated via void diagram. Updated AC coupling capacitors diagram.

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