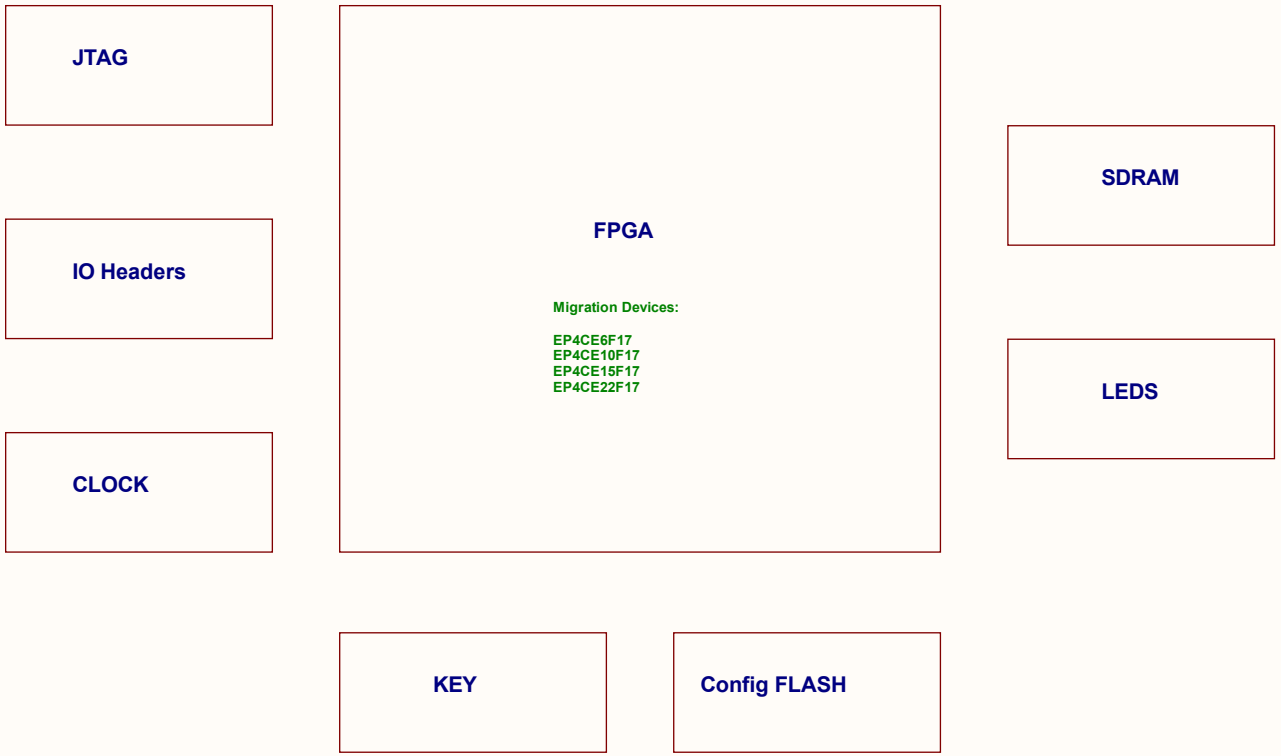
SCHEMATIC PAGE DESCRIPTION :

BLOCK DIAGRAM



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Title: ALTERA Cyclone IV FPGA C406		
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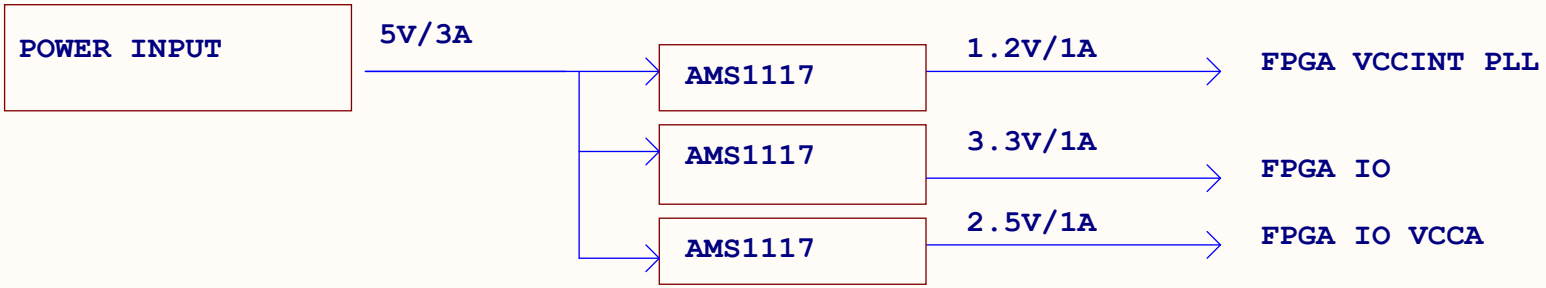
POWER CONSUMPTION

COMPONENTS	VOTAGE&CURRENT						
	1.2V	2.5V	3.3V				
FPGA	TBD	TBD	TBD				

POWER DISTRIBUTION



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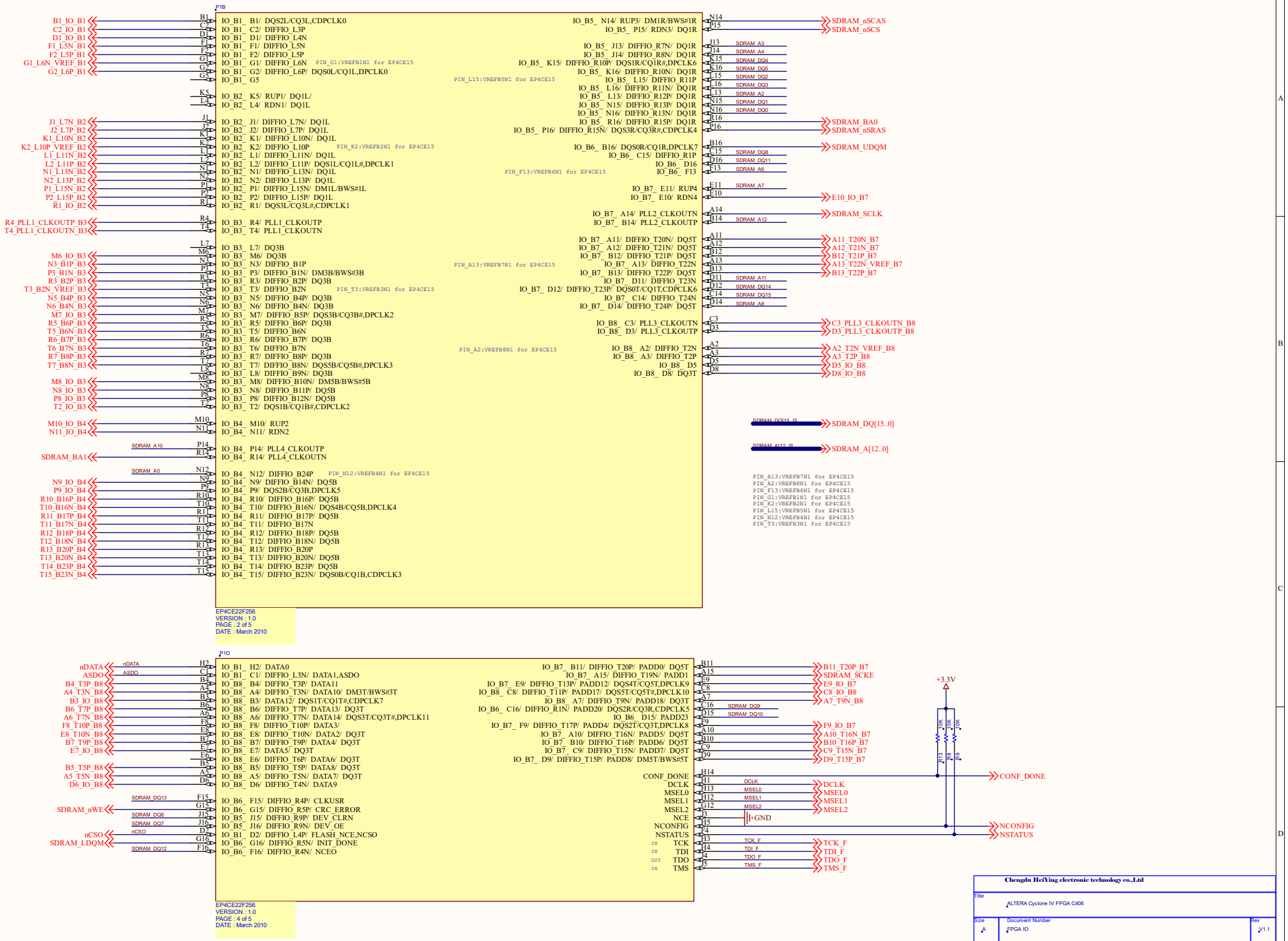
P1B
B1_IO_B1
C2_IO_B1
D1_IO_B1
F1_L5N_B1
F2_L5P_B1
G1_L6N_VREF_B1
G2_L6P_B1
IO_B1_ B1/ DQS2L/CQ3L,CDPCLK0
IO_B1_ C2/ DIFFIO_L3P
IO_B1_ D1/ DIFFIO_L4N
IO_B1_ F1/ DIFFIO_L5N
IO_B1_ F2/ DIFFIO_L5P
IO_B1_ G1/ DIFFIO_L6N PIN_G1:VREFB1N1 for EP4CE15
IO_B1_ G2/ DIFFIO_L6P/ DQS0L/CQ1L,DPCLK0
IO_B1_ G5
J1_L7N_B2
J2_L7P_B2
K1_L10N_B2
K2_L10P_VREF_B2
L1_L11N_B2
L2_L11P_B2
N1_L13N_B2
N2_L13P_B2
P1_L15N_B2
P2_L15P_B2
R1_IO_B2
IO_B2_ K5/ RUP1/ DQ1L/
IO_B2_ L4/ RDN1/ DQ1L
IO_B2_ J1/ DIFFIO_L7N/ DQ1L
IO_B2_ J2/ DIFFIO_L7P/ DQ1L
IO_B2_ K1/ DIFFIO_L10N/ DQ1L
IO_B2_ K2/ DIFFIO_L10P PIN_K2:VREFB2N1 for EP4CE15
IO_B2_ L1/ DIFFIO_L11N/ DQ1L
IO_B2_ L2/ DIFFIO_L11P/ DQS1L/CQ1L#,DPCLK1
IO_B2_ N1/ DIFFIO_L13N/ DQ1L
IO_B2_ N2/ DIFFIO_L13P/ DQ1L
IO_B2_ P1/ DIFFIO_L15N/ DM1L/BWS#1L
IO_B2_ P2/ DIFFIO_L15P/ DQ1L
IO_B2_ R1/ DQS3L/CQ3L#,CDPCLK1
R4_PLL1_CLKOUTP_B3
T4_PLL1_CLKOUTN_B3
IO_B3_ R4/ PLL1_CLKOUTP
IO_B3_ T4/ PLL1_CLKOUTN
M6_IO_B3
N3_B1P_B3
P3_B1N_B3
R3_B2P_B3
T3_B2N_VREF_B3
N5_B4P_B3
N6_B4N_B3
M7_IO_B3
R5_B6P_B3
T5_B6N_B3
R6_B7P_B3
T6_B7N_B3
R7_B8P_B3
T7_B8N_B3
M8_IO_B3
N8_IO_B3
P8_IO_B3
T2_IO_B3
IO_B3_ L7/ DQ3B
IO_B3_ M6/ DQ3B
IO_B3_ N3/ DIFFIO_B1P
IO_B3_ P3/ DIFFIO_B1N/ DM3B/BWS#3B
IO_B3_ R3/ DIFFIO_B2P/ DQ3B
IO_B3_ T3/ DIFFIO_B2N PIN_T3:VREFB3N1 for EP4CE15
IO_B3_ N5/ DIFFIO_B4P/ DQ3B
IO_B3_ N6/ DIFFIO_B4N/ DQ3B
IO_B3_ M7/ DIFFIO_B5P/ DQS3B/CQ3B#,DPCLK2
IO_B3_ R5/ DIFFIO_B6P/ DQ3B
IO_B3_ T5/ DIFFIO_B6N
IO_B3_ R6/ DIFFIO_B7P/ DQ3B
IO_B3_ T6/ DIFFIO_B7N
IO_B3_ R7/ DIFFIO_B8P/ DQ3B
IO_B3_ T7/ DIFFIO_B8N/ DQS5B/CQ5B#,DPCLK3
IO_B3_ L8/ DIFFIO_B9N/ DQ3B
IO_B3_ M8/ DIFFIO_B10N/ DM5B/BWS#5B
IO_B3_ N8/ DIFFIO_B11P/ DQ5B
IO_B3_ P8/ DIFFIO_B12N/ DQ5B
IO_B3_ T2/ DQS1B/CQ1B#,CDPCLK2
M10_IO_B4
N11_IO_B4
IO_B4_ M10/ RUP2
IO_B4_ N11/ RDN2
SDRAM_A10
SDRAM_BA1
IO_B4_ P14/ PLL4_CLKOUTP
IO_B4_ R14/ PLL4_CLKOUTN
SDRAM_A0
N9_IO_B4
P9_IO_B4
R10_B16P_B4
T10_B16N_B4
R11_B17P_B4
T11_B17N_B4
R12_B18P_B4
T12_B18N_B4
R13_B20P_B4
T13_B20N_B4
T14_B23P_B4
T15_B23N_B4
IO_B4_ N12/ DIFFIO_B2P PIN_N12:VREFB4N1 for EP4CE15
IO_B4_ N9/ DIFFIO_B14N/ DQ5B
IO_B4_ P9/ DQS2B/CQ3B,DPCLK5
IO_B4_ R10/ DIFFIO_B16P/ DQ5B
IO_B4_ T10/ DIFFIO_B16N/ DQS4B/CQ5B,DPCLK4
IO_B4_ R11/ DIFFIO_B17P/ DQ5B
IO_B4_ T11/ DIFFIO_B17N
IO_B4_ R12/ DIFFIO_B18P/ DQ5B
IO_B4_ T12/ DIFFIO_B18N/ DQ5B
IO_B4_ R13/ DIFFIO_B20P
IO_B4_ T13/ DIFFIO_B20N/ DQ5B
IO_B4_ T14/ DIFFIO_B23P/ DQ5B
IO_B4_ T15/ DIFFIO_B23N/ DQS0B/CQ1B,CDPCLK3
IO_B5_ N14/ RUP3/ DM1R/BWS#1R
IO_B5_ P15/ RDN3/ DQ1R
IO_B5_ J13/ DIFFIO_R7N/ DQ1R
IO_B5_ J14/ DIFFIO_R8N/ DQ1R
IO_B5_ K15/ DIFFIO_R10P/ DQS1R/CQ1R#,DPCLK6
IO_B5_ K16/ DIFFIO_R10N/ DQ1R
PIN_L15:VREFB5N1 for EP4CE15
IO_B5_ L15/ DIFFIO_R11P/ DQ1R
IO_B5_ L16/ DIFFIO_R11N/ DQ1R
IO_B5_ L13/ DIFFIO_R12P/ DQ1R
IO_B5_ N15/ DIFFIO_R13P/ DQ1R
IO_B5_ N16/ DIFFIO_R13N/ DQ1R
IO_B5_ R16/ DIFFIO_R15P/ DQ1R
IO_B5_ P16/ DIFFIO_R15N/ DQS3R/CQ3R#,CDPCLK4
IO_B6_ B16/ DQS0R/CQ1R,DPCLK7
IO_B6_ C15/ DIFFIO_R1P
PIN_F13:VREFB6N1 for EP4CE15
IO_B6_ D16
IO_B6_ F13
IO_B7_ E11/ RUP4
IO_B7_ E10/ RDN4
IO_B7_ A14/ PLL2_CLKOUTN
IO_B7_ B14/ PLL2_CLKOUTP
IO_B7_ A11/ DIFFIO_T20N/ DQ5T
IO_B7_ A12/ DIFFIO_T21N/ DQ5T
IO_B7_ B12/ DIFFIO_T21P/ DQ5T
PIN_A13:VREFB7N1 for EP4CE15
IO_B7_ A13/ DIFFIO_T22N
IO_B7_ B13/ DIFFIO_T22P/ DQ5T
IO_B7_ D11/ DIFFIO_T23N
IO_B7_ D12/ DIFFIO_T23P/ DQS0T/CQ1T,CDPCLK6
IO_B7_ C14/ DIFFIO_T24N
IO_B7_ D14/ DIFFIO_T24P/ DQ5T
IO_B8_ C3/ PLL3_CLKOUTN
IO_B8_ D3/ PLL3_CLKOUTP
PIN_A2:VREFB8N1 for EP4CE15
IO_B8_ A2/ DIFFIO_T2N
IO_B8_ A3/ DIFFIO_T2P
IO_B8_ D5
IO_B8_ D8/ DQ3T
SDRAM_nSCAS
SDRAM_nSCS
SDRAM_A3
SDRAM_A4
SDRAM_DQ4
SDRAM_DQ5
SDRAM_DQ2
SDRAM_DQ3
SDRAM_A2
SDRAM_DQ1
SDRAM_DQ0
SDRAM_BA0
SDRAM_nSRAS
SDRAM_UDQM
SDRAM_DQ8
SDRAM_DQ11
SDRAM_A6
SDRAM_A7
E10_IO_B7
SDRAM_SCLK
SDRAM_A12
A11_T20N_B7
A12_T21N_B7
B12_T21P_B7
A13_T22N_VREF_B7
B13_T22P_B7
SDRAM_A11
SDRAM_DQ14
SDRAM_DQ15
SDRAM_A8
C3_PLL3_CLKOUTN_B8
D3_PLL3_CLKOUTP_B8
A2_T2N_VREF_B8
A3_T2P_B8
D5_IO_B8
D8_IO_B8
SDRAM_DQ[15..0]
SDRAM_A[12..0]
PIN_A13:VREFB7N1 for EP4CE15
PIN_A2:VREFB8N1 for EP4CE15
PIN_F13:VREFB6N1 for EP4CE15
PIN_G1:VREFB1N1 for EP4CE15
PIN_K2:VREFB2N1 for EP4CE15
PIN_L15:VREFB5N1 for EP4CE15
PIN_N12:VREFB4N1 for EP4CE15
PIN_T3:VREFB3N1 for EP4CE15
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P1D
nDATA
ASDO
B4_T3P_B8
A4_T3N_B8
B3_IO_B8
B6_T7P_B8
A6_T7N_B8
F8_T10P_B8
E8_T10N_B8
B7_T9P_B8
E7_IO_B8
B5_T5P_B8
A5_T5N_B8
D6_IO_B8
SDRAM_nWE
nCSO
SDRAM_LDQM
IO_B1_ H2/ DATA0
IO_B1_ C1/ DIFFIO_L3N/ DATA1,ASDO
IO_B8_ B4/ DIFFIO_T3P/ DATA11
IO_B8_ A4/ DIFFIO_T3N/ DATA10/ DM3T/BWS#3T
IO_B8_ B3/ DATA12/ DQS1T/CQ1T#,CDPCLK7
IO_B8_ B6/ DIFFIO_T7P/ DATA13/ DQ3T
IO_B8_ A6/ DIFFIO_T7N/ DATA14/ DQS3T/CQ3T#,DPCLK11
IO_B8_ F8/ DIFFIO_T10P/ DATA3/
IO_B8_ E8/ DIFFIO_T10N/ DATA2/ DQ3T
IO_B8_ B7/ DIFFIO_T9P/ DATA4/ DQ3T
IO_B8_ E7/ DATA5/ DQ3T
IO_B8_ E6/ DIFFIO_T6P/ DATA6/ DQ3T
IO_B8_ B5/ DIFFIO_T5P/ DATA8/ DQ3T
IO_B8_ A5/ DIFFIO_T5N/ DATA7/ DQ3T
IO_B8_ D6/ DIFFIO_T4N/ DATA9
IO_B6_ F15/ DIFFIO_R4P/ CLKUSR
IO_B6_ G15/ DIFFIO_R5P/ CRC_ERROR
IO_B5_ J15/ DIFFIO_R9P/ DEV_CLRN
IO_B5_ J16/ DIFFIO_R9N/ DEV_OE
IO_B1_ D2/ DIFFIO_L4P/ FLASH_NCE,NCSO
IO_B6_ G16/ DIFFIO_R5N/ INIT_DONE
IO_B6_ F16/ DIFFIO_R4N/ NCEO
IO_B7_ B11/ DIFFIO_T20P/ PADD0/ DQ5T
IO_B7_ A15/ DIFFIO_T19N/ PADD1
IO_B7_ E9/ DIFFIO_T13P/ PADD12/ DQS4T/CQ5T,DPCLK9
IO_B8_ C8/ DIFFIO_T11P/ PADD17/ DQS5T/CQ5T#,DPCLK10
IO_B8_ A7/ DIFFIO_T9N/ PADD18/ DQ3T
IO_B6_ C16/ DIFFIO_R1N/ PADD20/ DQS2R/CQ3R,CDPCLK5
IO_B6_ D15/ PADD23
IO_B7_ F9/ DIFFIO_T17P/ PADD4/ DQS2T/CQ3T,DPCLK8
IO_B7_ A10/ DIFFIO_T16N/ PADD5/ DQ5T
IO_B7_ B10/ DIFFIO_T16P/ PADD6/ DQ5T
IO_B7_ C9/ DIFFIO_T15N/ PADD7/ DQ5T
IO_B7_ D9/ DIFFIO_T15P/ PADD8/ DM5T/BWS#5T
CONF_DONE
DCLK
MSEL0
MSEL1
MSEL2
NCE
NCONFIG
NSTATUS
TCK
TDI
TDO
TMS
B11_T20P_B7
SDRAM_SCKE
E9_IO_B7
C8_IO_B8
A7_T9N_B8
SDRAM_DQ9
SDRAM_DQ10
F9_IO_B7
A10_T16N_B7
B10_T16P_B7
C9_T15N_B7
D9_T15P_B7
CONF_DONE
DCLK
MSEL0
MSEL1
MSEL2
GND
NCONFIG
NSTATUS
TCK_F
TDI_F
TDO_F
TMS_F
+3.3V
10K
R13
R8
R9
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A
Document Number
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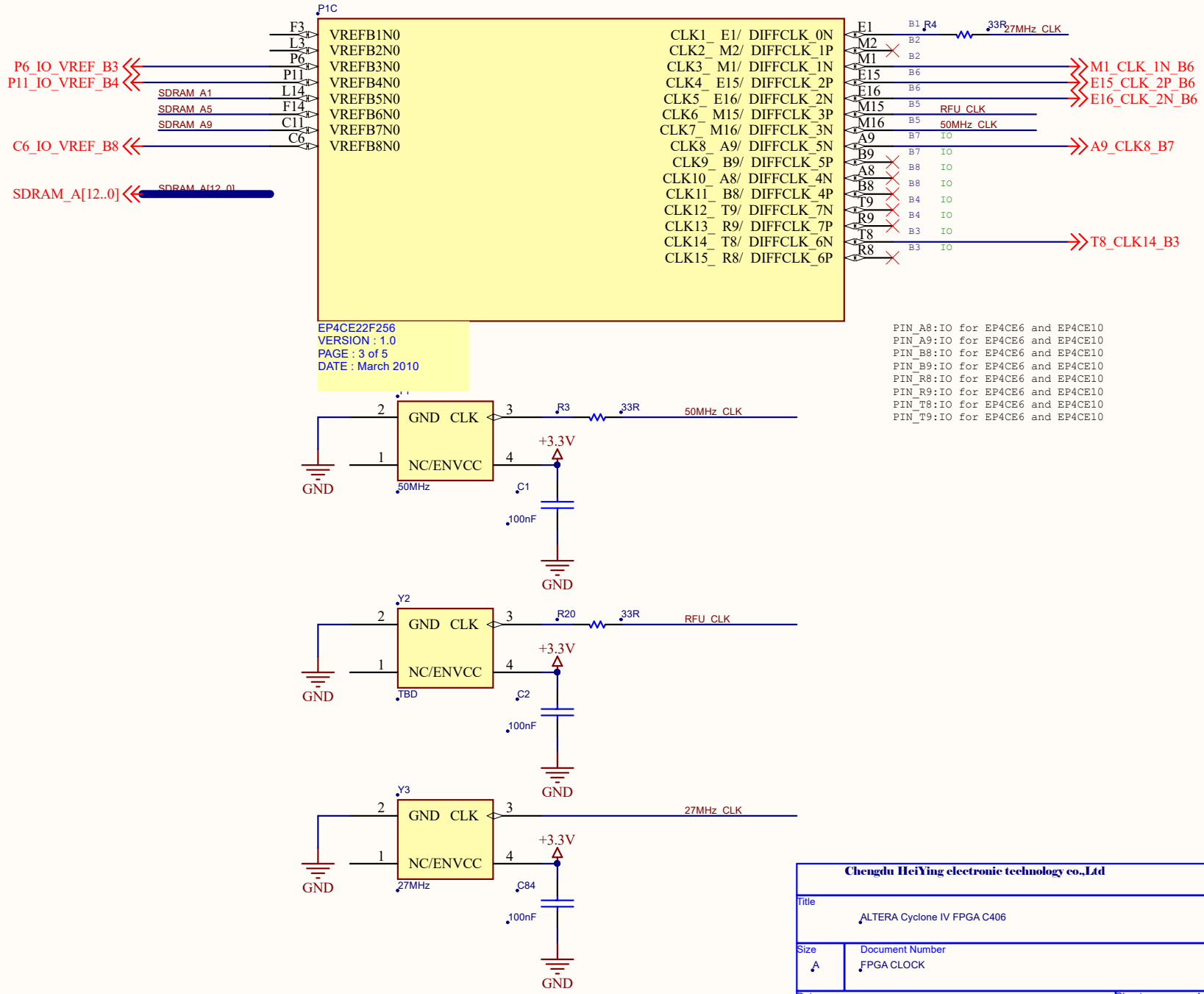
P1C
F3 VREFB1N0
L3 VREFB2N0
P6 VREFB3N0
P11 VREFB4N0
L14 VREFB5N0
F14 VREFB6N0
C11 VREFB7N0
C6 VREFB8N0
P6_IO_VREF_B3
P11_IO_VREF_B4
C6_IO_VREF_B8
SDRAM_A1
SDRAM_A5
SDRAM_A9
SDRAM_A[12..0]
CLK1_ E1/ DIFFCLK_0N
CLK2_ M2/ DIFFCLK_1P
CLK3_ M1/ DIFFCLK_1N
CLK4_ E15/ DIFFCLK_2P
CLK5_ E16/ DIFFCLK_2N
CLK6_ M15/ DIFFCLK_3P
CLK7_ M16/ DIFFCLK_3N
CLK8_ A9/ DIFFCLK_5N
CLK9_ B9/ DIFFCLK_5P
CLK10_ A8/ DIFFCLK_4N
CLK11_ B8/ DIFFCLK_4P
CLK12_ T9/ DIFFCLK_7N
CLK13_ R9/ DIFFCLK_7P
CLK14_ T8/ DIFFCLK_6N
CLK15_ R8/ DIFFCLK_6P
E1 R4 33R 27MHz_CLK
M1_CLK_1N_B6
E15_CLK_2P_B6
E16_CLK_2N_B6
RFU_CLK
50MHz_CLK
A9_CLK8_B7
T8_CLK14_B3
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PIN_A8:IO for EP4CE6 and EP4CE10
PIN_A9:IO for EP4CE6 and EP4CE10
PIN_B8:IO for EP4CE6 and EP4CE10
PIN_B9:IO for EP4CE6 and EP4CE10
PIN_R8:IO for EP4CE6 and EP4CE10
PIN_R9:IO for EP4CE6 and EP4CE10
PIN_T8:IO for EP4CE6 and EP4CE10
PIN_T9:IO for EP4CE6 and EP4CE10
GND CLK
NC/ENVCC
50MHz
R3 33R 50MHz_CLK
+3.3V
C1 100nF
Y2
TBD
R20 33R RFU_CLK
C2 100nF
Y3
27MHz
27MHz_CLK
C84 100nF
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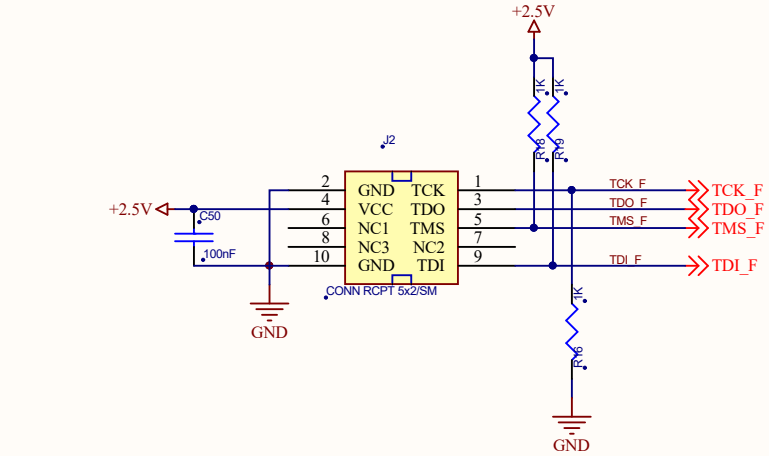

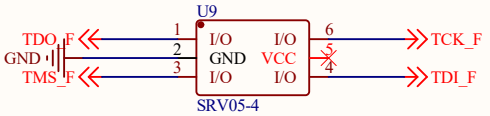

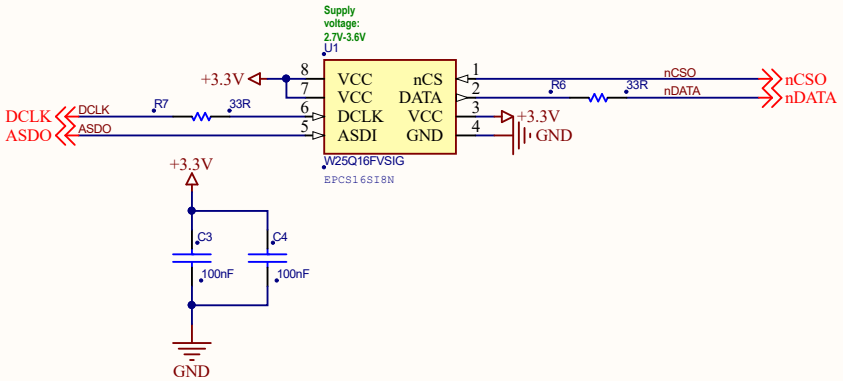

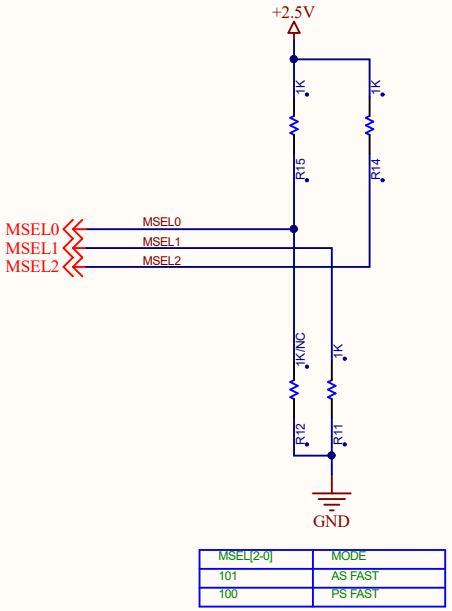

MSEL[2-0]	MODE
101	AS FAST
100	PS FAST

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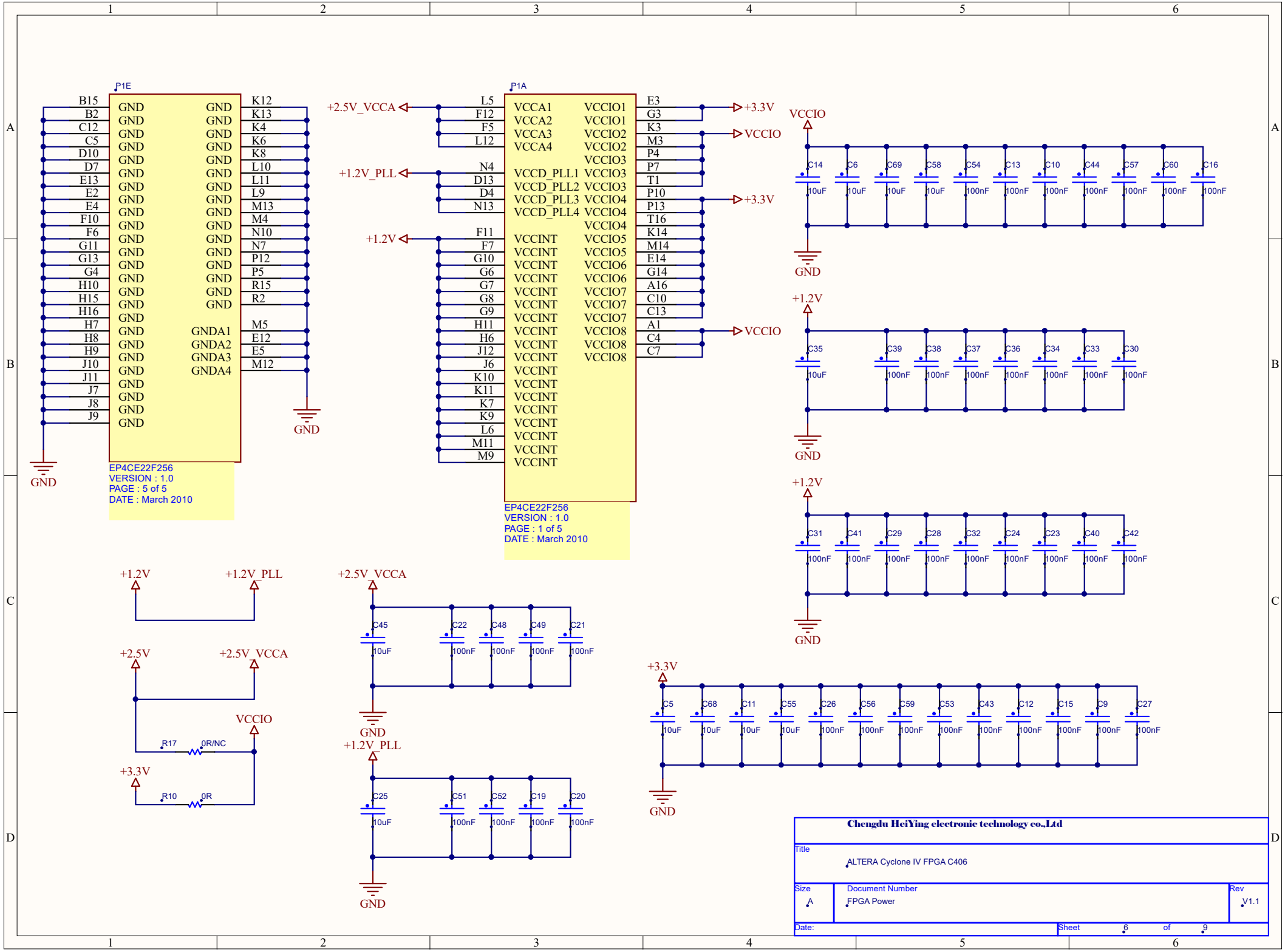
P1E
B15 B2 C12 C5 D10 D7 E13 E2 E4 F10 F6 G11 G13 G4 H10 H15 H16 H7 H8 H9 J10 J11 J7 J8 J9
GND
K12 K13 K4 K6 K8 L10 L11 L9 M13 M4 N10 N7 P12 P5 R15 R2
GNDA1 GNDA2 GNDA3 GNDA4
M5 E12 E5 M12
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P1A
+2.5V_VCCA
L5 F12 F5 L12
VCCA1 VCCA2 VCCA3 VCCA4
+1.2V_PLL
N4 D13 D4 N13
VCCD_PLL1 VCCD_PLL2 VCCD_PLL3 VCCD_PLL4
+1.2V
F11 F7 G10 G6 G7 G8 G9 H11 H6 J12 J6 K10 K11 K7 K9 L6 M11 M9
VCCINT
E3 G3 K3 M3 P4 P7 T1 P10 P13 T16 K14 M14 E14 G14 A16 C10 C13 A1 C4 C7
VCCIO1 VCCIO1 VCCIO2 VCCIO2 VCCIO3 VCCIO3 VCCIO3 VCCIO4 VCCIO4 VCCIO4 VCCIO5 VCCIO5 VCCIO6 VCCIO6 VCCIO7 VCCIO7 VCCIO7 VCCIO8 VCCIO8 VCCIO8
+3.3V
VCCIO
+3.3V
VCCIO
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VCCIO
C14 C6 C69 C58 C54 C13 C10 C44 C57 C60 C16
10uF 10uF 10uF 10uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF
GND
+1.2V
C35 C39 C38 C37 C36 C34 C33 C30
10uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF
GND
+1.2V
C31 C41 C29 C28 C32 C24 C23 C40 C42
100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF
GND
+1.2V
+1.2V_PLL
+2.5V
+2.5V_VCCA
VCCIO
R17 0R/NC
+3.3V
R10 0R
+2.5V_VCCA
C45 C22 C48 C49 C21
10uF 100nF 100nF 100nF 100nF
GND
+1.2V_PLL
C25 C51 C52 C19 C20
10uF 100nF 100nF 100nF 100nF
GND
+3.3V
C5 C68 C11 C55 C26 C56 C59 C53 C43 C12 C15 C9 C27
10uF 10uF 10uF 10uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF
GND
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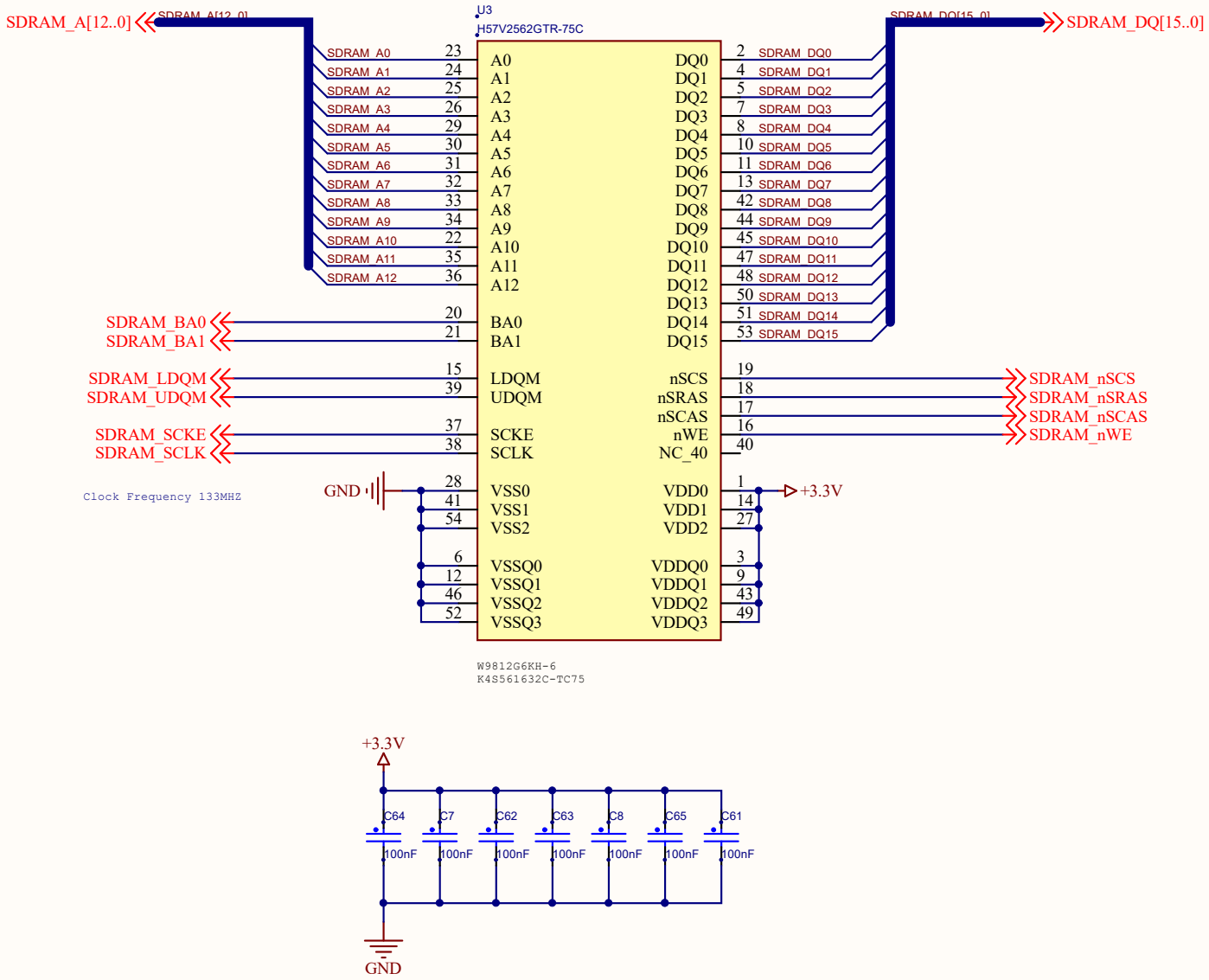

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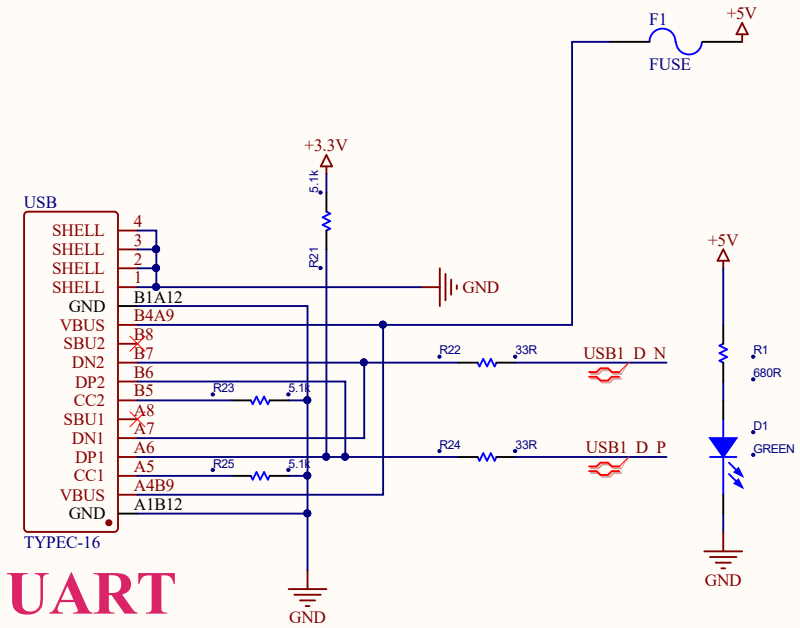

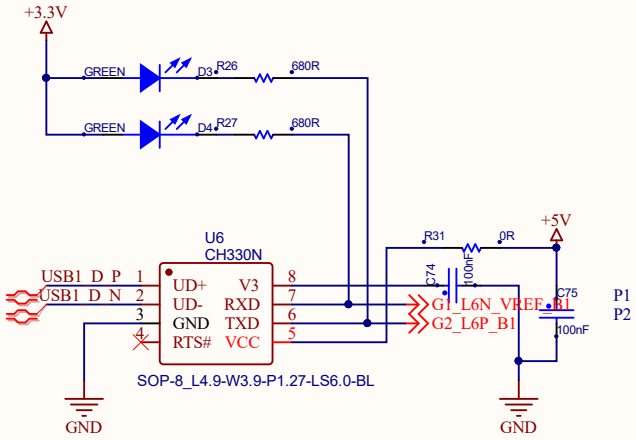

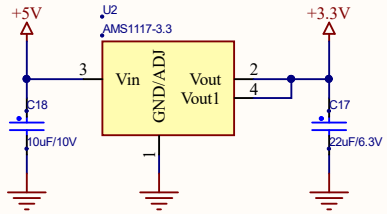

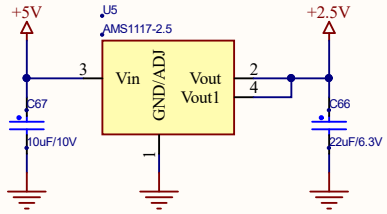

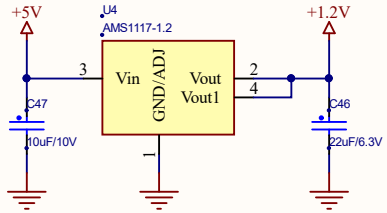

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Title: ALTERA Cyclone IV FPGA C406		
Size: A	Document Number: System Power	Rev: V1.1
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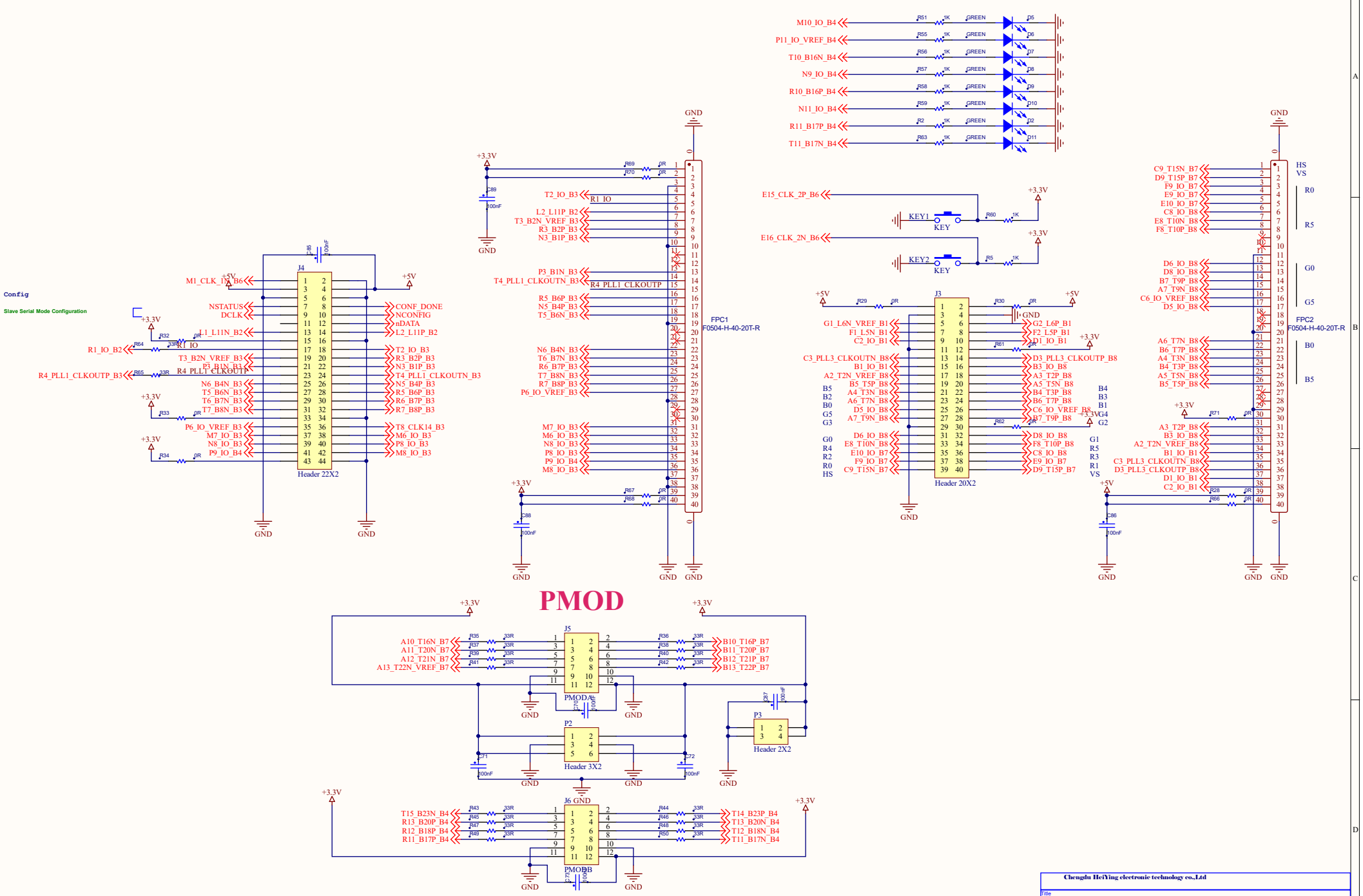
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Slave Serial Mode Configuration
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F0504-H-40-20T-R
FPC2
F0504-H-40-20T-R
J3
Header 20X2
KEY1
KEY2
KEY
PMOD
J5
PMODA
P2
Header 3X2
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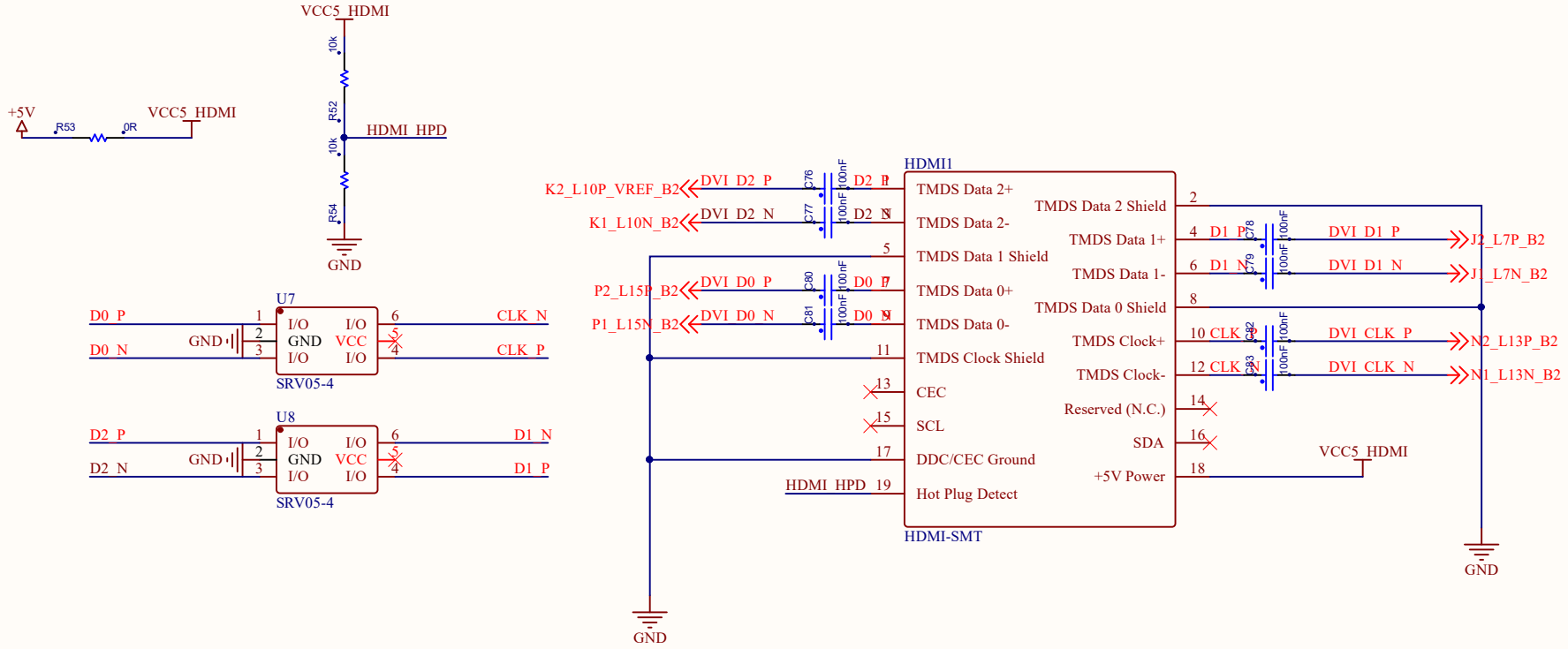
J6
PMODB
Chengdu HeiYing electronic technology co.,Ltd
ALTERA Cyclone IV FPGA C406
Connectors
V1.1



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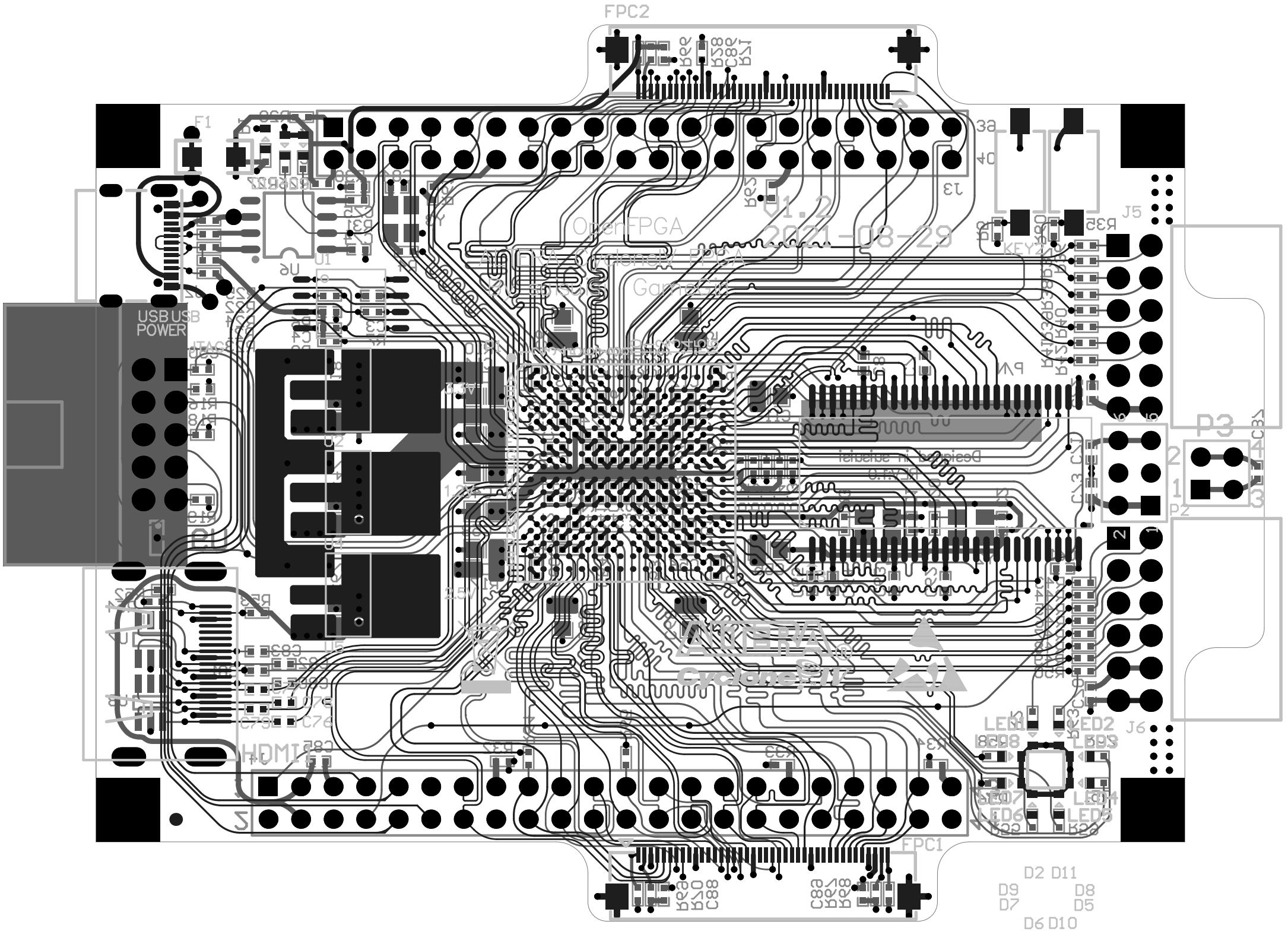
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FPC1
USB USB
POWER
HDMI
P3
P2
J5
J6
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
OpenFPGA
V1.2
2021-08-29
ALTERA
Cyclone® IV


Board S