1. Description

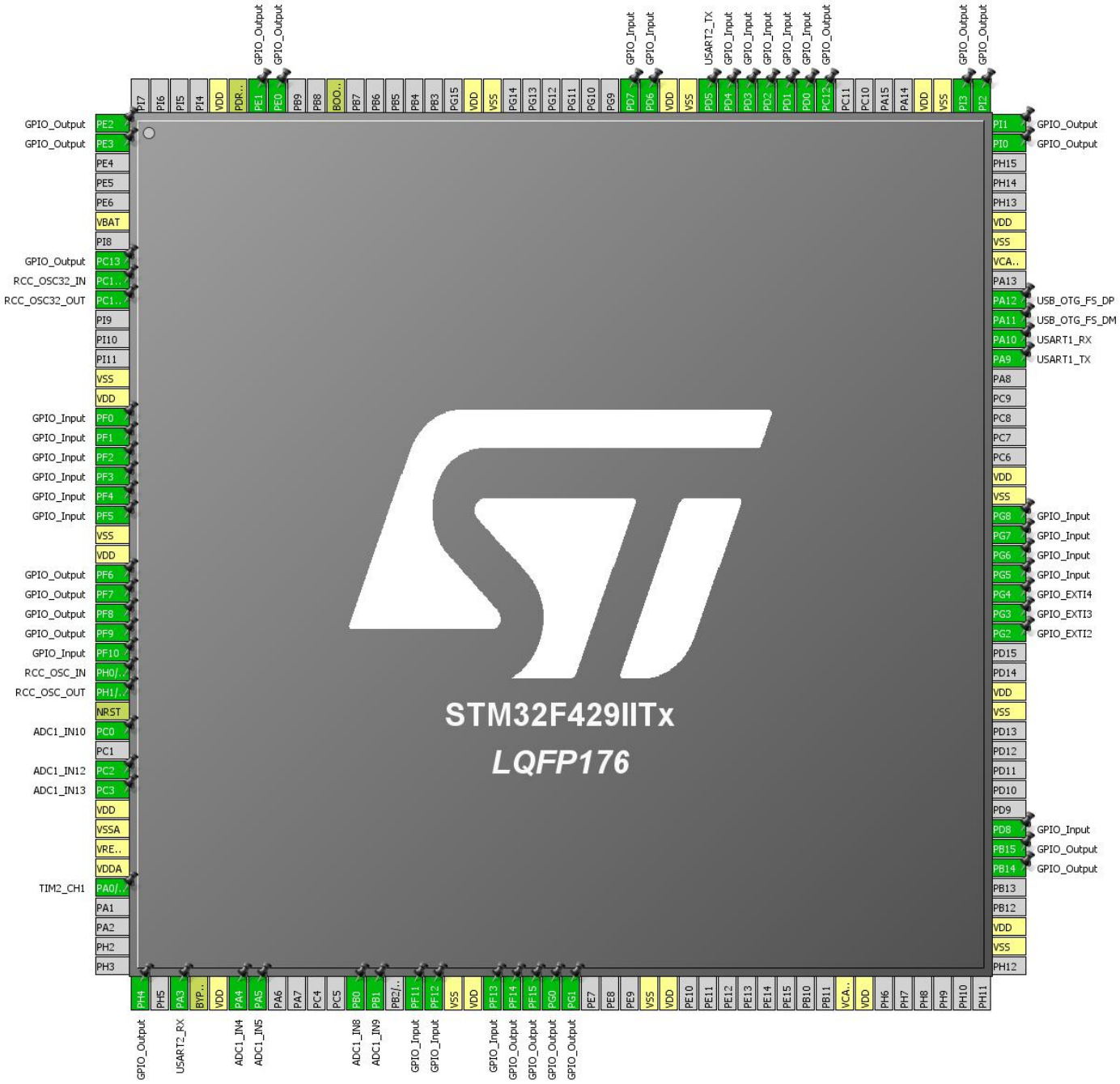
1.1. Project

Project Name	Tray_Loader
Board Name	custom
Generated with:	STM32CubeMX 4.26.1
Date	04/01/2021

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429IITx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

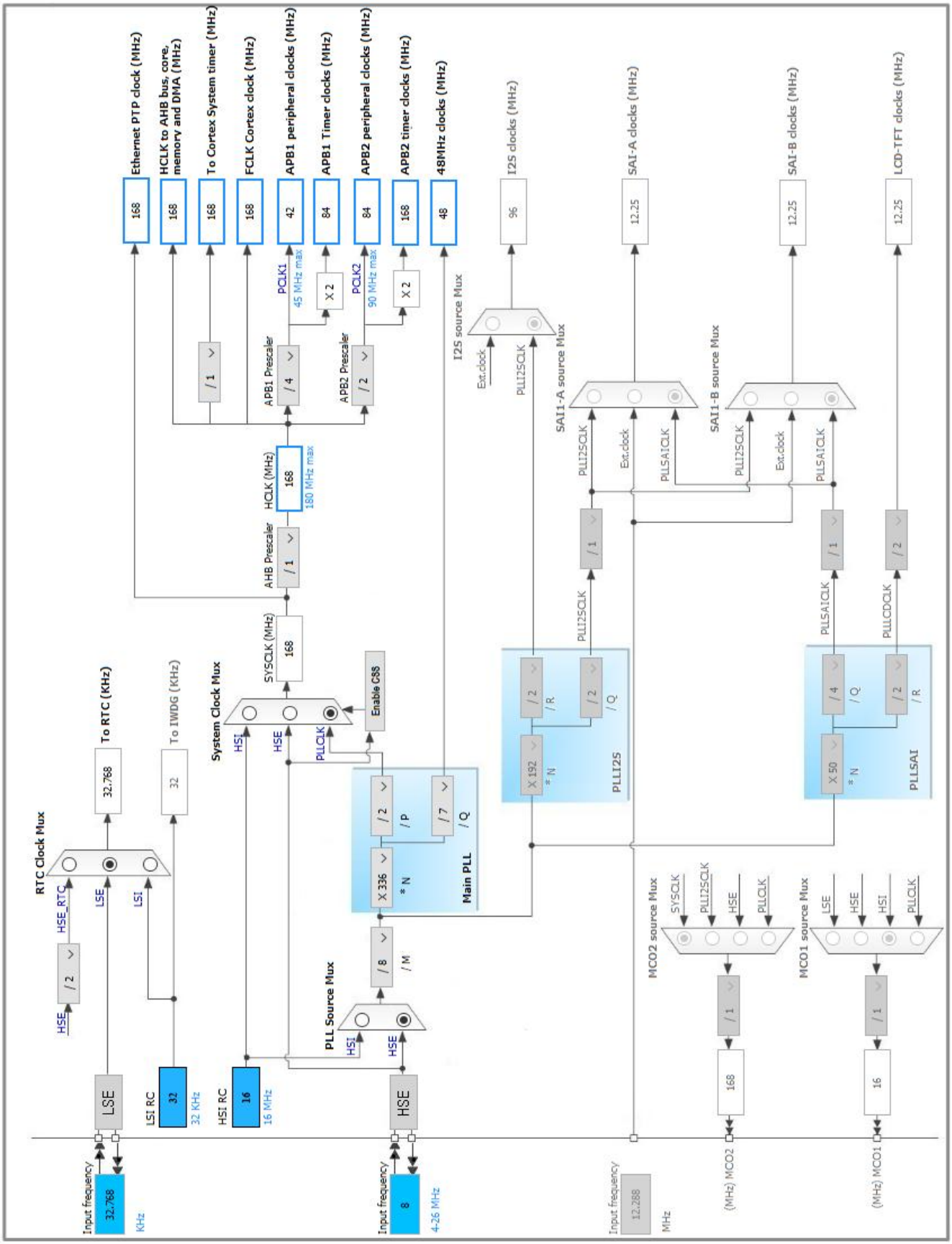
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
6	VBAT	Power		
8	PC13 *	I/O	GPIO_Output	
9	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
10	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
14	VSS	Power		
15	VDD	Power		
16	PF0 *	I/O	GPIO_Input	
17	PF1 *	I/O	GPIO_Input	
18	PF2 *	I/O	GPIO_Input	
19	PF3 *	I/O	GPIO_Input	
20	PF4 *	I/O	GPIO_Input	
21	PF5 *	I/O	GPIO_Input	
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Output	
25	PF7 *	I/O	GPIO_Output	
26	PF8 *	I/O	GPIO_Output	
27	PF9 *	I/O	GPIO_Output	
28	PF10 *	I/O	GPIO_Input	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	ADC1_IN10	
34	PC2	I/O	ADC1_IN12	
35	PC3	I/O	ADC1_IN13	
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
40	PA0/WKUP	I/O	TIM2_CH1	
45	PH4 *	I/O	GPIO_Output	
47	PA3	I/O	USART2_RX	
48	BYPASS_REG	Reset		
49	VDD	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
50	PA4	I/O	ADC1_IN4	
51	PA5	I/O	ADC1_IN5	
56	PB0	I/O	ADC1_IN8	
57	PB1	I/O	ADC1_IN9	
59	PF11 *	I/O	GPIO_Input	
60	PF12 *	I/O	GPIO_Input	
61	VSS	Power		
62	VDD	Power		
63	PF13 *	I/O	GPIO_Input	
64	PF14 *	I/O	GPIO_Output	
65	PF15 *	I/O	GPIO_Output	
66	PG0 *	I/O	GPIO_Output	
67	PG1 *	I/O	GPIO_Output	
71	VSS	Power		
72	VDD	Power		
81	VCAP_1	Power		
82	VDD	Power		
90	VSS	Power		
91	VDD	Power		
94	PB14 *	I/O	GPIO_Output	
95	PB15 *	I/O	GPIO_Output	
96	PD8 *	I/O	GPIO_Input	
102	VSS	Power		
103	VDD	Power		
106	PG2	I/O	GPIO_EXTI2	
107	PG3	I/O	GPIO_EXTI3	
108	PG4	I/O	GPIO_EXTI4	
109	PG5 *	I/O	GPIO_Input	
110	PG6 *	I/O	GPIO_Input	
111	PG7 *	I/O	GPIO_Input	
112	PG8 *	I/O	GPIO_Input	
113	VSS	Power		
114	VDD	Power		
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
122	PA11	I/O	USB_OTG_FS_DM	
123	PA12	I/O	USB_OTG_FS_DP	
125	VCAP_2	Power		
126	VSS	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
127	VDD	Power		
131	PI0 *	I/O	GPIO_Output	
132	PI1 *	I/O	GPIO_Output	
133	PI2 *	I/O	GPIO_Output	
134	PI3 *	I/O	GPIO_Output	
135	VSS	Power		
136	VDD	Power		
141	PC12 *	I/O	GPIO_Output	
142	PD0 *	I/O	GPIO_Input	
143	PD1 *	I/O	GPIO_Input	
144	PD2 *	I/O	GPIO_Input	
145	PD3 *	I/O	GPIO_Input	
146	PD4 *	I/O	GPIO_Input	
147	PD5	I/O	USART2_TX	
148	VSS	Power		
149	VDD	Power		
150	PD6 *	I/O	GPIO_Input	
151	PD7 *	I/O	GPIO_Input	
158	VSS	Power		
159	VDD	Power		
166	BOOT0	Boot		
169	PE0 *	I/O	GPIO_Output	
170	PE1 *	I/O	GPIO_Output	
171	PDR_ON	Reset		
172	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN4

mode: IN5

mode: IN8

mode: IN9

mode: IN10

mode: IN12

mode: IN13

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 5 ***
Sampling Time	3 Cycles
Rank	**2 ***
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. CRC

mode: Activated

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.4. RTC

mode: Activate Clock Source

5.4.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

5.5. SYS

Timebase Source: SysTick

5.6. TIM1

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**168-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.7. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8400-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.10. USB_OTG_FS

Mode: Host_Only

5.10.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Signal start of frame	Disabled

5.11. FATFS

mode: USB Disk

5.11.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId

FS_LOCK (Number of files opened simultaneously)	2

5.11.2. IPs instances:

USBH:

USBH instance	USB Host MSC FS
Use dma template	Disabled

5.12. USB_HOST

Class for FS IP: Mass Storage Host Class

5.12.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	2
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG2	GPIO_EXTI2	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	
	PG3	GPIO_EXTI3	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	
	PG4	GPIO_EXTI4	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PI0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PI1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PI2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PI3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line2 interrupt	true	1	0
EXTI line3 interrupt	true	3	0
EXTI line4 interrupt	true	4	0
TIM2 global interrupt	true	1	0
DMA2 stream2 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429IITx
Datasheet	024030_Rev9

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Tray_Loader
Project Folder	E:\2021 WORKS\PROJECTS\Tray Loader\Cubemx
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.21.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report