MANIPAL
ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

MANIPAL SCHOOL OF INFORMATION SCIENCES

(A Constituent unit of MAHE, Manipal)

Implementation of DDR4 using System Verilog

Reg. Number	Name	Branch
201038006	Tejaswini Holla K	VLSI Design
201038031	Rajat Raju Chaudhari	VLSI Design
201038049	Konda Rohith	VLSI Design

Under the guidance of

Dr Chaitanya CVS
Assistant Professor,
Manipal School of Information Sciences,
MAHE, MANIPAL

24/01/2021

DECLARATION

We declare that this mini project, submitted for the evaluation of course work of Mini Project to Manipal School of Information Sciences, is (our original work implementing an existing idea/concept/code) conducted under the supervision of my guide Assistant Professor **Dr Chaitanya CVS** and panel members, Associate Professor **Prashanth Kumar Shetty**. References, help and material obtained from other sources have been duly acknowledged.

ABSTRACT

The DDR4 SDRAM is the latest Double-Data-Rate Fourth Generation Synchronous Dynamic Random Access Memory with the advantages of large capacity, high speed, low power consumption and good stability. In order to solve the data cache problem of the ultra-high-speed sampling and processing system there are is a good research going on to fill in the void created between the performances of processors and the memory access [3] This project mainly introduces the characteristics and working principle of DDR4, introduces the DDR4 read-write controller module in detail and finally the results of the operations (read / write) which will be performed on the memory will be mentioned.

Keywords

DDR4 SDRAM, Rank, System Verilog, Memory Controller, DIMMs.

Contents

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

DDR	Double Data Rate
DDR3	Double Data Rate Version 3
DDR4	Double Data Rate Version 4
DRAM	Dynamic Random-Access Memory
SDRAM	Synchronous Dynamic Random-Access Memory
I/O	Input/output
PC	Personal Computers
Mb	Mega bits
Gb	Giga bits
V	Volts
t_{RRD}	Active to Active Command Delay
t_{RCD}	Active to Read Delay
t_{RAS}	Active to Precharge Delay
t_{MRD}	MRS Command cycle Time
t_{REFI}	Average refresh Interval time
CAL	Command Address Latency
DLL	Delay locked loop
DQ	Data Strobe
DQS	Differential Data Strobe
ODT	On-Die Termination
FIFO	First In First Out
CRC	Cyclic Redundancy Check
DBI	Data Bus Inversion
CKE	Clock Enable
CAS	Command Address Store
RAS	Row Address Strobe
MRS	Mode Register Set
DM	Data Mask
MT	Mega Transfer
MPR	Multi Purpose register

1. Introduction

With the high increase in development of the semiconductor processor's industry, major importance given to operation speed and capacity of the memory device. The DDR controller is an extension of old traditional memory controller synchronous DRAM (SDRAM). The DDR controller can transact the data on both rising and falling edges of the clock cycles. Thereby, double the transfer of data rate in the memory device. The cost of DDR memory is low, because it is most used in PC's, storage and buffers.

Implementation of DDR SDRAM using System Verilog for a higher coverage [2] has been carried out before which will be extended to DDR4 specifically in here.

The main changes of DDR4 SDRAM are supply voltage, higher data rate, higher densities, more banks, faster bursts access and higher system reliability compared to the previous versions mentioned in the table below, these would be the objective going ahead [2].

Features	**Comparison between DDR3 and DDR4**		
	DDR3	***DDR4 x16***	***DDR4 Advantage***
Voltage (core and I/O)	1.5 V	1.2V	Reduces Memory Power Demand
Prefetch	8n	8n	Same Prefetch but parallel bank Group
Density	512 Mb – 8 Gb	2 – 16 Gb	Better enablement for large capacity memory systems
Data Rate	800, 1066,1333, 1600,1866, 2133	1600,1866, 2133, 2400, 2667, 3200	Higher Bandwidth
Internal Banks	8	16	More Banks
Bank Groups	0	2	Faster Burst Access

Table 1: Comparison between DDR3 and DDR4 [4]

2. Material and methods

The Specification sheets as given by different manufacturers such as Micron Technology Inc., Samsung provide all details of DDR4 SDRAM. The one which is being referred is that by the Micron Technology Inc [1].

IEEE papers mentioned in the reference section [2] [3] [4] would give a sufficient detail on each of the blocks and its working. Moreover, video lectures on www.nptel.com (referred as on 10- Dec- 2020) on memory architecture would also suffice the need.

2.1 Block Diagram

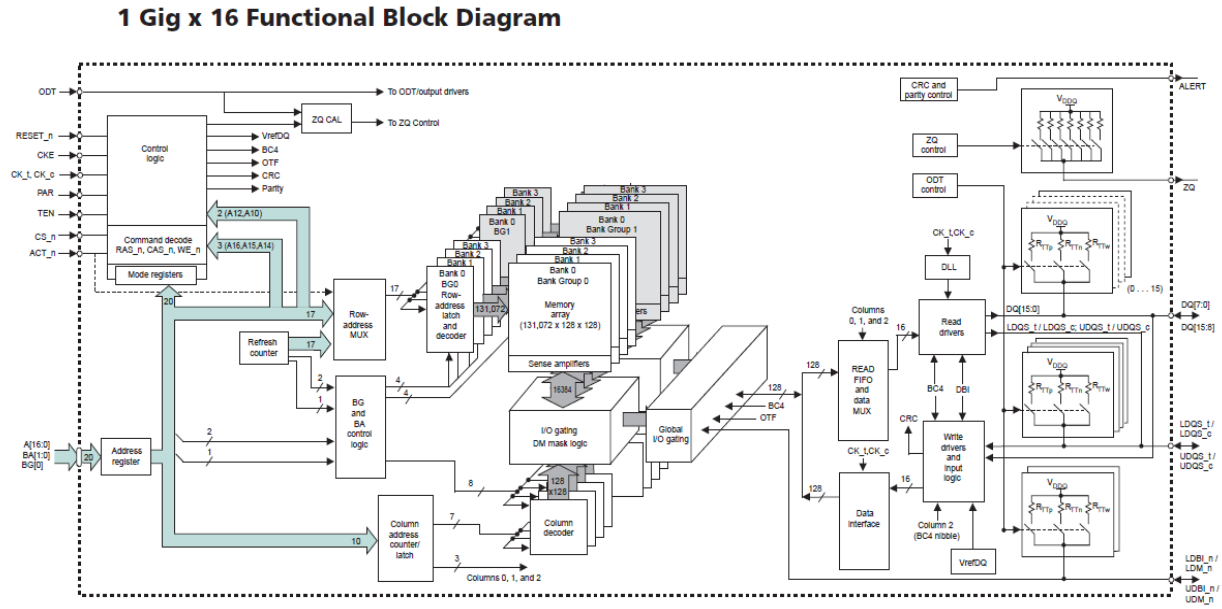

Figure 1: Block Diagram for 1Gb - x16 DDR4 [1]

The above block diagram will be broken down into modules. Starting with just one bank with the read and write functionality only. Then integrating multiple banks to form a bank group. Before this a Memory controller consisting of command queue, response queue and schedular need to be implemented.

In the process, the modules will be upgraded to implement DDR4 specific signals and sufficient details will be provided to allow the work to be reproduced by an independent researcher.

2.1.1 Memory Cell

Memory cell is the smallest unit which stores the data as the charge on the capacitor of a transistor. The selection of this transistor is done by the use of word line and bitline. The

intersection of the word line and the bitline gives the unit cell to which data is written. It is similar to a cell of excel sheet.

2.1.2 Wordline

Wordline is the command that is fed into the sense amplifiers which activate the particular row of the particular bank. Wordline therefore is the first command which activates the address within a bank.

2.1.3 Bitline

The column address of a data is address as the bitline. This is fed into the column decoder which then intersects with the activated row to pinpoint the transistor to which data has to be stored/read from.

2.1.4 Sense Amplifiers

These are the row buffers which first hold the data from coming in from the memory controller consisting of the wordline and the particular row which need to be activated.

2.1.5 DRAM Arrays

The collection of Rows and columns is called a DRAM array.

2.1.6 Bank

Bank is a collection of DRAM Arrays. The number of DRAM arrays depends on the size. It can be imagined as a sheet in Excel.

2.1.7 Bank Group

A collection of multiple Bank in one is a Bank Group. It can be imagined as a Workbook consisting of multiple sheets in Excel.

2.1.8 Control Logic

Control logic is the memory controller which converts the physical address given from the I/O pins to logical address consisting of the required signals like PRE, ACT, CAS etc. and vice versa. It gives these commands to channel which in turn is connected to the bank groups.

2.1.9 Column Decoder

This decodes the column address which in received from the column buffer to activate the corresponding bitline of a Bank in a Bank Group.

2.1.10 Refresh Counter

As stated, above data is stored in memory as a charge on the capacitor connected to the transistor. The charge on the capacitor gets degraded based on temperature of the DRAM.

For a temperature below 85 degree Celsius the charge retention time is 64ms and above that it is 32ms. Thus, the memory has to be refreshed within this time so avoid loss of data.

Refresh is reading the data from memory and writing it back and should be done for all rows of all banks in a bank group. This charges the capacitor to full charge and thus avoids loss of data. DRAM is not available for any other operation while the Refresh goes on.

3. Finite State Diagram

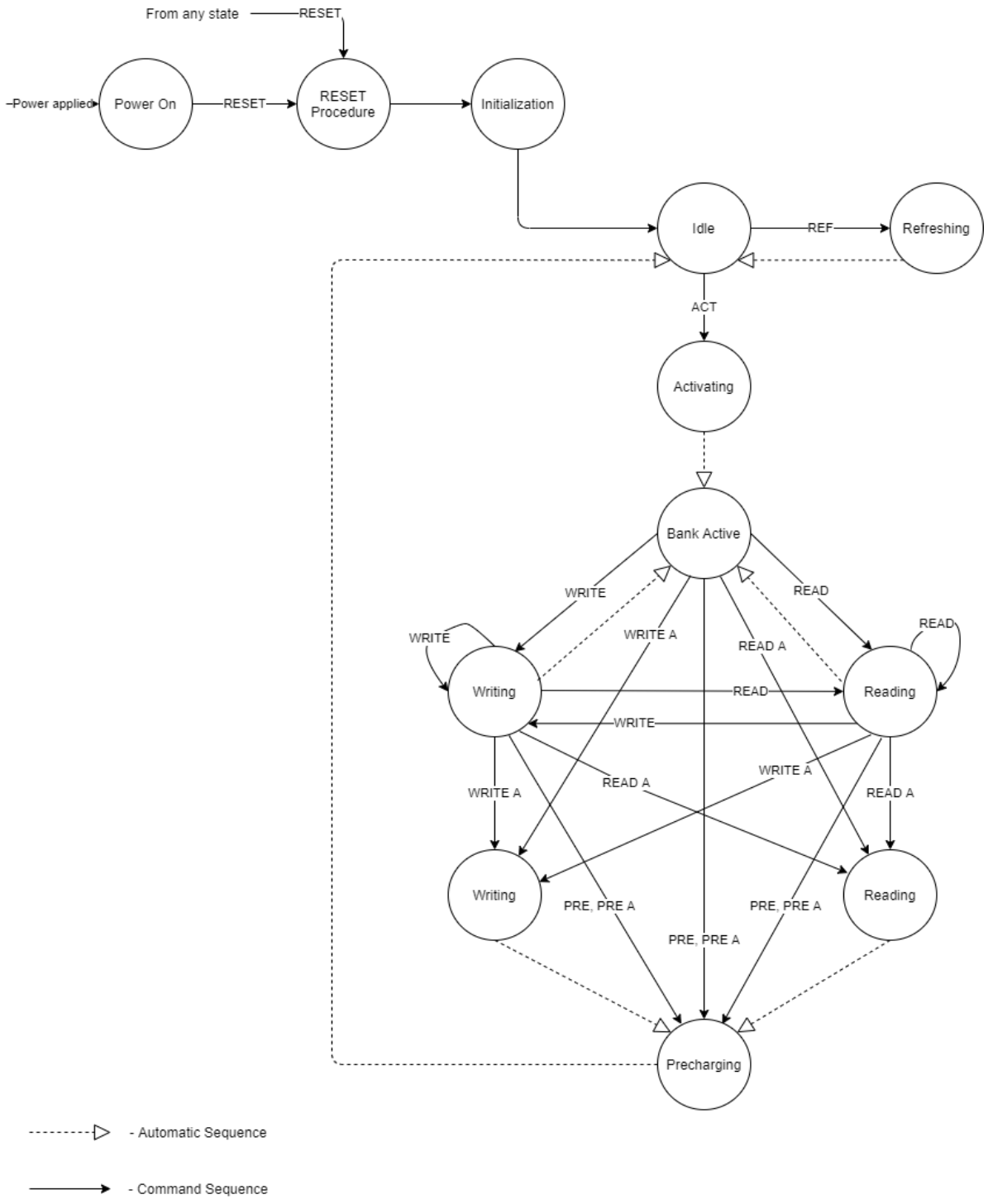

Figure 2: Finite State Machine for DDR4 Implementation

Command	Description
ACT	Activate
PRE	Precharge
PREA	Precharge all
READ	RD, Read Data
READA	Read and Precharge
WRITE	WR, Write data
WRITEA	Write and Precharge
RESET	Start reset procedure

Table 2: State diagram command definition

2.3 Signals and Commands

In order to perform any operation on the DRAM a set of signals and commands need to be executed. To read or write data to or from the DRAM, first the DRAM row must be precharged. Then, an activation command must be issued. After successful activation, the data in the required row will be transferred to the sense amplifiers. The required data is then read from the sense amplifiers by using the column addresses. The following are the main signals to be considered for DDR4 operation

Symbol	Type	Description
A [16:0]	Input	Address Inputs: Provides the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed.
ACT_n	Input	Command input: ACT_n indicates an ACTIVATE command.

BA [1:0]	Input	Bank address inputs: Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied.
BG	Input	Bank group address inputs: Define the bank group to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied.
CK_t, CK_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations
CS_n	Input	Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	Input data mask: DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. UDM_n is associated with DQ [15:8]; LDM_n is associated with DQ [7:0].
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered.
RESET_n	Input	Active LOW asynchronous reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	I/O	Data input/output: Bidirectional data bus. Represents the DQ [15:0] for the x16 configuration.
DBI_n, UDBI_n, LDBI_n	I/O	DBI input/output: Data bus inversion. UDBI_n and LDBI_n is the input/output signal used for data bus inversion in the x16

		configuration. UDBI_n is associated with DQ [15:8], and LDBI_n is associated with DQ [7:0].
DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	I/O	Data strobe: Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ [7:0]; UDQS corresponds to the data on DQ [15:8].

Table 3: DDR4 signals and descriptions

- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair.
- The term "_n" is used to represent a signal that is active LOW.

4. Architecture of SDRAM DDR4 Controller

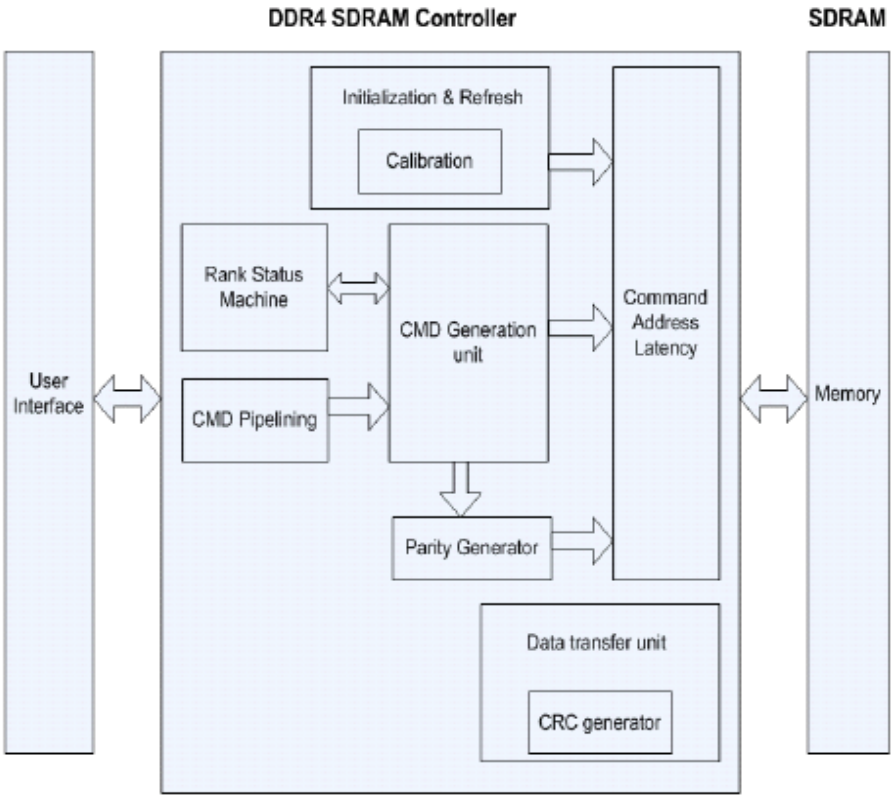

Figure 3: DDR4 SDRAM Controller architecture

A. Rank status machine

In the controller we propose a Bank management unit (we called Rank status machine) which tracks the present state of each memory bank in the original DRAM. This provides greater flexibility to perform parallel read write command processing. The rank status machine architecture is shown.

There are 4 Bank groups status processor, and each Bank group contains 4 banks status processor, so total 16 banks can be managed at one time. Each status processor contains specific timing counter. The status is: bank active, readable, writeable, rechargeable and row address. This ensures read-to-write and write-to-read bus turnaround time; active-to-precharge, activate delay between different banks and bank groups. When a command is sent to DDR4; timing constraint's counters corresponding to that command start to count and updated the status upon counting. For an example if a bank "x" in DDR4 is in idle state and a activate command is issued to the DDR4. The timing constraints related to activate command are t_{RRD} (active-to- active command delay), t_{RCD} (active-to-read/write delay), t_{RAS} (active-to-precharge delay) etc. In rank status machine corresponding bank "x" status processor starts

counting of these times i.e. t_{RRD}, t_{RCD}, t_{RAS} etc. after issuing activate command. At beginning the bank "x" status was bank active =0, readable =0, writeable =0, prechargeable =0. After the t_{RCD} time counts bank "x" status updated as bank active =1, readable =1, writeable =1, prechargeable =0.

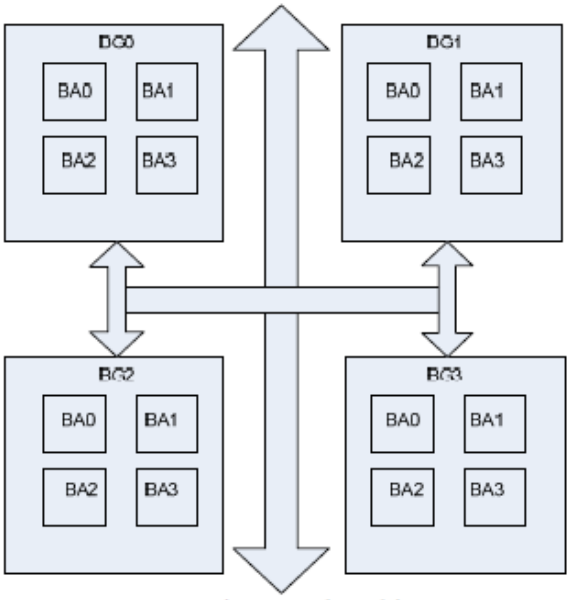

Figure 4: Rank Status Machine

DDR4 introduces new specifications for read to read or write to write delay time for read or writes to banks of different Bank group and same Bank groups respectively.

The full bandwidth of DDR4 cannot be used, until Bank group interleaving access is not employed [4]. To achieve the better performance the controller can performs the bank interleaving operations by monitoring rank status.

B. CMD pipelining

Today's most of system shares the common RAM (Such as multiple processor, GPU, GPIO shares the DRAM). So, the controller queues up multiple commands from different peripherals using command pipeline. The command pipeline is used for optimal bandwidth utilization. Command pipeline is used by the Command generation unit to pre-process the target bank for read or write operation such as active and precharge.

C. Command address latency

Command-to-Address Latency (CAL) function offers by DDR4 memory that can be used to save power. Basically, CAL is the delay between enable a Chip select and command/Address in clock cycles which is defined by mode register. Before issuing a command, it provides the

DRAM time to active the CMD receivers. The receivers can be latched, whenever the command and the address are latched. In case of providing consecutive commands, the receiver will have enabled by DRAM for the period of command sequence.

D. Calibration Unit

Calibration Unit performs write levelling, read levelling and ZQ calibration. DDR4 memory used fly-by topology for better signal integrity. To reduce the number of stubs and their length this topology is used. Despite benefiting, it causes skew problem between clock and strobe at every DRAM on the DIMM module. Hence, to solve the skew problem memory controller uses the 'write levelling' feature and feedback from the DDR4 SDRAM to adjust the data strobe to clock relationship [4]. This feature can compensate for unbalanced loading on the board for write and read operations. Calibration unit put the DDR4 into write levelling state by writing mode register MR1 of DDR4. The write strobe DQS is repeatedly delayed in small increments by the Delay Locked Loop (DLL). DDR4 samples the CLK with the rising edge of DQS and provide feedback on DQ. During this protocol, each set of DQ is output with a "0" until the rising edge is detected by the DQS at which time the DQ will be output with a "1". The calibration unit will detect these "1" on the DQ bus and then knows the correct DQS compensation to align the DQS and CLK on the write path. Once all DQS have been adjusted, these compensation values of DLL stored for each DQS for future usage. Then the memory controller sends another MRS command to exit the write level mode. As DDR4 write levelling manages the DQS/DQ on write data, the DDR4 read levelling manages the DQS/DQ on read data. DDR4 read levelling is to compensate the imbalanced loading on the read path. First the memory controller puts the DDR4 memory devices into MPR mode by writing to the MR3 register. This puts the DDR4 memory devices into the read levelling mode which outputs a training pattern of consecutive "01" on each memory read command. Since the memory controller knows that data stream, so it will adjust the internal DQS delay capturing the DQ using DQS. Memory controller repeats these calibration reads until read data capture at memory controller is optimized.

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. The ZQ calibration accounts the voltage and temperature variation on DRAM output driver.

E. Command Generation Unit

The command generator accepts user commands from the CMD pipelining unit. When the unit receives a single request, from pipelining unit request is processed immediately. For specified read or write request, Command Generation Unit lookup in the rank status to ensure the timing constraints for each previous memory transaction is met up before start new transaction. It also checks for availability of target bank for read or write operation from the rank status. Bank availability means the requested row in corresponding bank is active. If the requested bank is not active then it generates the necessary precharge and active command to activate the bank in DDR4. The command generation unit halt itself from throwing next command until the timing requirements of DDR4 are met. Upon availability of the bank; the requested read or write command is send to the DDR4 and internal rank status machine so that rank can update itself each time when a new command is throwing to the DDR4. If there are outstanding requests from two or more queues, the Command generation unit process the requests in look-ahead way. While processing the active request from pipeline if there are any unsatisfied timing constraints which lead the controller to stall the transaction, controller then check the next upcoming request from queue. Command generation unit check the next requests bank address to find out the upcoming requests bank whether it is in active and activated row does match with the requested row address or not. If the condition does not met then command generation unit perform necessary precharge activate sequence to active that bank, so that when the request will be active the request will incur minimum stall time. Such deliberately bank active of future requests utilize the active requests stall time. This opportunistically look-ahead activates improve overall throughput.

F. Data Transfer Unit

Data transfer unit consists of a read FIFO and a write FIFO. The read FIFO receives data from the DDR4 and passes that data to the user. The write FIFO receives write data from the user interface and passes that data to the DDR4. Read data from DDR4 arrive at the controller at both positive and negative edge of clock. The burst length of DDR4 is 8. Read FIFO captures these data in 4 clock cycles and provides the user read data in a single clock cycle on next positive edge of clock. Similarly write FIFO loads the user write data in a single clock and send to the DDR4 in next 4 clocks both at positive and negative edge. During the write data transfer to DDR4 it also added up CRC code at trail of each burst.

G. CRC Generator

As speed increased data prone to error. To solve Data reliability issue during WRITE operations, DDR4 included Cyclic Redundancy Check (CRC) along with DBI. DDR4 uses an 8-bit CRC header error control. The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1.

DRAM generates checksum in each write burst per Data Strobe lane. CRC use 72 bits of data and all unallocated bits are 1s. DRAM compares the checksum. If two checksums do not match then DRAM flags an error.

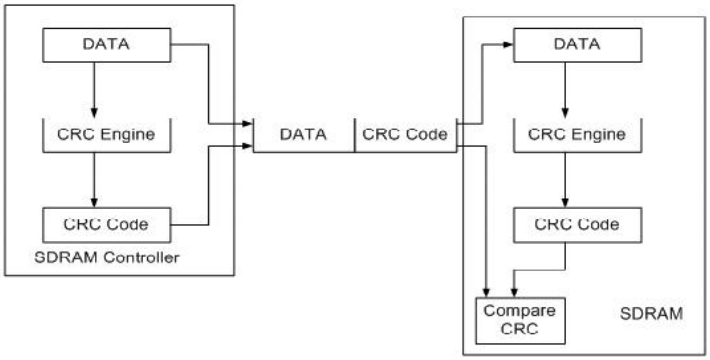

Figure 5: CRC Generator

H. Initialization and Refresh Unit

Initialization and Refresh Unit performs the power up initialization and periodic refresh. After power up or reset the DDR4 must be initialized before start read or write transaction. The reset pin of DDR4 is kept low by the controller for 100ns to begin the initialization process. To active DDR4 clock, reset pin set to high and CKE pin set to low for 5100us. Then CKE pin drive to high. After t_{XPR} period of time when DRAM is initialized Mode Register Set commands are issued for proper mode of operation such as burst length, additive latency, cas latency etc. After setting the mode register the Initialization and refresh unit switch on the calibration unit to perform the read and write levelling. Upon completion of coalition the DDR4 is ready for normal operation. It has a t_{REFI} counter, which counts DDR4 refresh interval. On each t_{REFI} count the controller issues refresh command to DDR4. Figure 6 shows the reset and initialization waveform sequence.

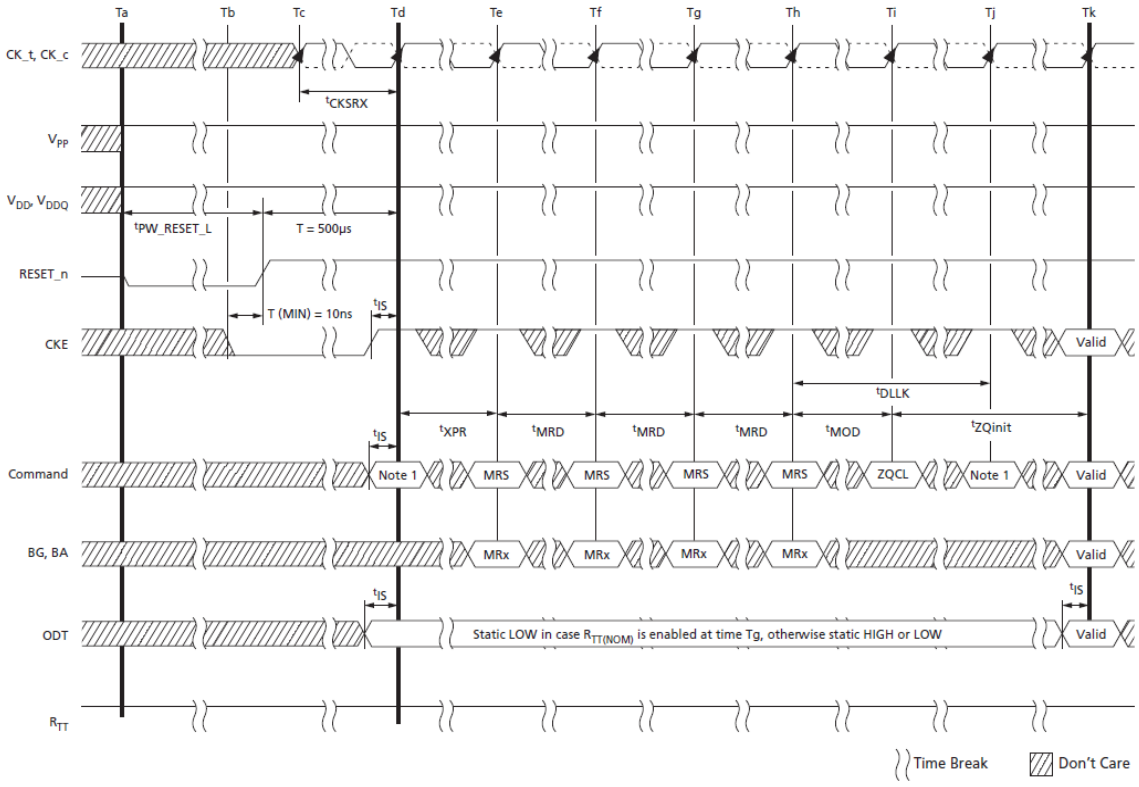

Figure 6: Reset and Initialization sequence

5. Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MR) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued.[1]

The MRS command cycle time, t_{MRD}, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands.

Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply t_{MRD} timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- CMD address latency
- CA parity latency mode
- V_{REFDQ} training value
- V_{REFDQ} training mode
- V_{REFDQ} training range

The address pin mapping for mode registers is shown in figure 7. The RAS_n, CAS_n, WE_n signals are set to a default LOW during mode register set. The bank_group_select and bank_select signals are used for selecting the required mode registers.

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Figure 7: Address pin mapping for mode register

a. Mode Register 0

This register is selected by setting the bank_group_select and bank_select as 000. This register can be used for setting functionalities like:

- Burst Length, Type, and Order

  Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

- CAS Latency

  CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL +CL.

- Test Mode
- Write Recovery (WR)/READ-to-PRECHARGE
- DLL RESET

  The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, ^{t}DLLK must be met before functions requiring the DLL can be used. Such as READ commands or synchronous ODT operations, for example.

For default operation, the value for Mode Register 0 is set as 20’b00000000000000000000.

b. Mode Register 1

This register is selected by setting the bank_group_select and bank_select as 001. This register can be used for setting functionalities like:

- DLL Enable/DLL Disable

  The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is

automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, ^{t}DLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON}.

During t_{DLLK}, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when $R_{TT(WR)}$ is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the $R_{TT(NOM)}$ bits MR1[9,6,2] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set $R_{TT\ (WR),}$ MR2[10:9] = 00.

- Output Driver Impedance Control
- ODT $R_{TT(NOM)}$ Values
- Additive Latency

  The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency is controlled by the sum of the AL and CAS latency register settings. WRITE latency is controlled by the sum of the AL and CAS WRITE latency register settings.
- Write Leveling
- Output Disable

  The device outputs may be enabled/disabled by MR1[12] bit.
- Termination Data Strobe

  Supported only on x8 devices.

For default operation, the value for Mode Register 1 is set as 20’b00100000000000000000.

c. Mode Register 2

This register is selected by setting the bank_group_select and bank_select as 010. This register can be used for setting functionalities like:

- CAS WRITE Latency

  CAS WRITE latency is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

- Low-Power Auto Self Refresh

  Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the I_{DD6} current for a given temperature range.

- Dynamic ODT
- Write Cyclic Redundancy Check Data Bus

  When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

For default operation, the value for Mode Register 2 is set as 20'b01000000000000000000.

d. Mode Register 3

This register is selected by setting the bank_group_select and bank_select as 011. This register can be used for setting functionalities like:

- Multipurpose Register

  The multipurpose register (MPR) is used for several features:

  • Readout of the contents of the MRn registers

  • WRITE and READ system patterns used for data bus calibration

  • Readout of the error frame when the command address parity feature is enabled

  To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and ^{t}RP met). After MPR is

enabled, any subsequent Read or ReadA commands will be redirected to a specific mode register. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

- WRITE Command Latency When CRC/DM is Enabled

  The WRITE command latency must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4^{n}CK is used, 5^{n}CK or 6^{n}CK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666 MT/s then 5^{n}CK is used, 4^{n}CK or 6^{n}CK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6^{n}CK is used; 4^{n}CK or 5^{n}CK are not allowed.

- Fine Granularity Refresh Mode

  This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening t_{RFC} and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

- Temperature Sensor Status

  This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

- Per-DRAM Addressability

  This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or V_{REF} values on DRAM devices within a given rank.

- Gear-Down Mode

  The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating

the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

For default operation, the value for Mode Register 3 is set as 20'b01100000000000000000.

e. Mode Register 4

This register is selected by setting the bank_group_select and bank_select as 100. This register can be used for setting functionalities like:

- Hard Post Package Repair Mode

  The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether hPPR mode is available (A7 = 1) or not available (A7 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

- Soft Post Package Repair Mode

  The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

- WRITE Preamble

  Programmable WRITE preamble, t_{WPRE}, can be set to 1^tCK or 2^tCK via the MR4 register. The 1^tCK setting is similar to DDR3. However, when operating in 2^tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^tCK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

- READ Preamble

  Programmable READ preamble t_{RPRE} can be set to 1^tCK or 2^tCK via the MR4 register. Both the 1^tCK and 2^tCK DDR4 preamble settings are different from that

defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

- READ Preamble Training

  Programmable READ preamble training can be set to 1^{t}CK or 2^{t}CK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

- Temperature-Controlled Refresh

  When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than t_{REFI} of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of -40°C to 85°C, while the extended temperature range covers -40°C to 105°C.

- Command Address Latency

  COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register according to the t_{CAL}(ns)/t_{CK}(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

- Internal V_{REF} Monitor

  This mode enables output of internally generated V_{REFDQ} for monitoring on DQ0, DQ1, DQ2, and DQ3. May be used during V_{REFDQ} training and test. While in this mode, R_{TT} should be set to High-Z. V_{REF_time} must be increased by 10ns if DQ load is 0pF, plus an additional 15ns per pF of loading. This measurement is for verification purposes and is NOT an external voltage supply pin.

- Maximum Power Savings Mode

  This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the

MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

For default operation, the value for Mode Register 4 is set as 20'b10000000000000000000.

f. Mode Register 5

This register is selected by setting the bank_group_select and bank_select as 101. This register can be used for setting functionalities like:

- Data Bus Inversion

  The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled.

- Data Mask

  The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled.

- CA Parity Persistent Error Mode

  Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

- ODT Input Buffer for Power-Down

  This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. However, the device may provide RTT(Park) termination depending on the MR settings. This is primarily for additional power savings.

- CA Parity Error Status

  The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

- CRC Error Status

  The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

- CA Parity Latency Mode

  CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16 , CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

For default operation, the value for Mode Register 5 is set as 20'b10100000000000000000.

g. Mode Register 6

This register is selected by setting the bank_group_select and bank_select as 110. This register can be used for setting functionalities like:

- Data Rate Programming

  The device controller must program the correct data rate according to the operating frequency.

- V_{REFDQ} Calibration Enable

  V_{REFDQ} calibration is where the device internally generates its own V_{REFDQ} to be used by the DQ input receivers. The V_{REFDQ} value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal V_{REFDQ} level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conjunction with V_{REFDQ} adjustments to optimize and verify the data

eye. Enabling V_{REFDQ} calibration must be used whenever values are being written to the MR6[6:0] register.

- V_{REFDQ} Calibration Range

  The device defines two V_{REFDQ} calibration ranges: Range 1 and Range 2. Range 1 supports V_{REFDQ} between 60% and 92% of V_{DDQ} while Range 2 supports V_{REFDQ} between 45% and 77% of V_{DDQ}, as seen in V_{REFDQ} Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

- V_{REFDQ} Calibration Value

  Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V_{REFDQ}.

For default operation, the value for Mode Register 6 is set as 20’b11000000010000000000.

6. Implementation of DDR4 Controller

The implementation was done in accordance with the FSM as mentioned in the Micron specification sheet [1].

There are 9 major states of operation that can be implemented via SystemVerilog.

The above FSM in figure 2 is being used to implement both the open page policy and the close page policy.

a. Open Page Policy: Here after the address is received, if the new location to be accessed is a different row then, after the completion of current operation the state is changed o PRECHARGE where the data from the sense amplifiers is written back into the row before the activation of the new row as mentioned in the address.

b. Closed Page Policy: In this, as shown in the FSM represented by the dotted lines after READ and WRITE operation, the state automatically moves to the PRECHARGE state before the next command is received regardless of the address.

- The Activate command is used to open (activate) a row in a particular bank for subsequent access. The values on the BG[1:0] inputs select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[16:0] selects the row within the bank.

- The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (^{t}RP) after the precharge command is issued. After a bank is precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

  The auto precharge feature is engaged when a Read or Write command is issued with A10 High.

- During Refresh command (REF) is used during normal operation of the device. This command is nonpersistent, so it must be issued each time a refresh is required. The

device requires Refresh cycles at an average periodic interval. Refresh happens every 32ms if the temperature is above 85 degree centigrade and for every 64 ms for below 85 degree centigrade.

- Idle state is defined as all banks are closed, no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied, as well as all self-refresh exit and power-down exit parameters are satisfied.

- During Initialization default values of the Mode registers are set which are defined as in the Micron Specification [1]. Also, a Sequence of commands is followed depending on the state of the memory.

- When the reset command is issued the device is forced into initialization state where the initialization sequence is followed to boot up the device.

- Write/Write_A: These states are used to write the data into the row buffers(sense amps) and the into the memory. The major difference in the two states is that Write command is used in an open page policy whereas Write_A is used in a closed page policy.

- Read/Read_A: These states are used to read the data from the memory and then into the row buffer (sense amps). The major difference in the two states is that read command is used in an open page policy whereas Read_A is used in a closed page policy

Appropriate operation based on the signal received in the address and based on the mode register operations pre-loaded initially are being done in the state.

Figure 8 shows the command truth table based on which the operations were performed. ‘V’ stands for Valid signal, CA is the column address, BG is the bank group address, BA is the bank select address, H is HIGH, L is LOW and X stands for Don’t care.

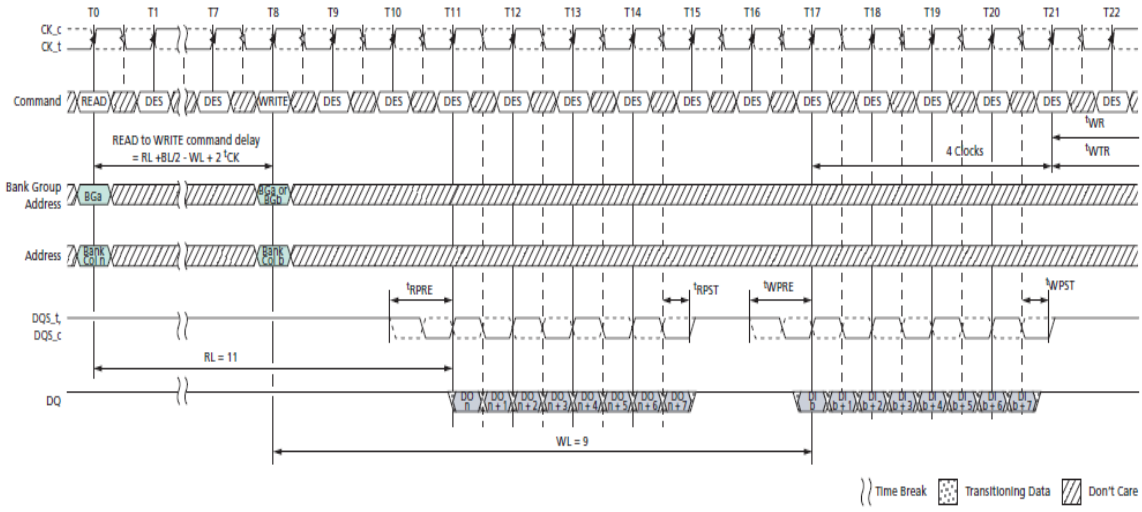

Figure 8: Read and Write operation with BC8

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC_n	A[13, 11]	A10/AP	A[9:0]
MODE REGISTER SET		MRS	H	H	L	H	L	L	L	BG	BA	V	OP code			
REFRESH		REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V
Self refresh entry		SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V
Self refresh exit		SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X
					L	H	H	H	H	V	V	V	V	V	V	V
Single-bank PRECHARGE		PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V
PRECHARGE all banks		PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V
Reserved for future use		RFU	H	H	L	H	L	H	H	RFU						
Bank ACTIVATE		ACT	H	H	L	L	Row address (RA)			BG	BA	V	Row address (RA)			
WRITE	BL8 fixed, BC4 fixed	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA
	BC4OTF	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA
	BL8OTF	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA
WRITE with auto precharge	BL8 fixed, BC4 fixed	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA
	BC4OTF	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA
	BL8OTF	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA
READ	BL8 fixed, BC4 fixed	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA
	BC4OTF	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA
	BL8OTF	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA
READ with auto precharge	BL8 fixed, BC4 fixed	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA
	BC4OTF	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA
	BL8OTF	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA
NO OPERATION		NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X
Power-down entry		PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X
Power-down exit		PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	H	L	X	X	X	X	X	H	X
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	H	L	X	X	X	X	X	L	X

Table 4: Command Truth Table

Memory Size Implemented

The memory implemented is of the size 1024 Mega x 16 or 16 Giga bits. Where each location can store a data corresponding to 16 bits.

There are 2 group of banks each having 4 banks in a x16 DDR4. Each bank of each bank group will consist of 2^{17} number of rows and 2^{10} number of columns.

Parameter	4096 Meg x 4	2048 Meg x 8	1024 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	256K (A[17:0])	128K (A[16:0])	128K (A[16:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B	1KB	2KB

Note: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Table 5: Memory size implementation

7. Results

The Cadence NCSim tool was used for the simulation purposes and the following operations were performed.

- Data is written in a bank of a particular bank group following the necessary steps like PRECHARGE, delay etc.
- The above data is read and displayed back (read operation on memory)
- Stored multiple data in multiple banks of single/multiple bank groups.
- Read Multiple data from multiple banks of single/multiple bank group.

Figure 9 shows the waveform obtained for the read and write operations. Initially the ACT_n (activate) signal is LOW and the address sent is to access the row 0 of bank 0 of bank group 0. As no data is present in the bank the value of row buffer will be X. Next the write enable signal WE-n/A15 is set an LOW and the ACT_n signal is set as HIGH which indicates that a WRITE operation has to be done. A data FF00 is sent over the data bus DQ and the column address is sent over the address pins A9_0 while setting the CAS_n/A15 pin as LOW. This data is written into the row buffer at the column specified, i.e., column 0. Next, the WE_n/A14 is set as HIGH which indicates READ operation. The data from the row buffer is then transferred to the data bus DQ.

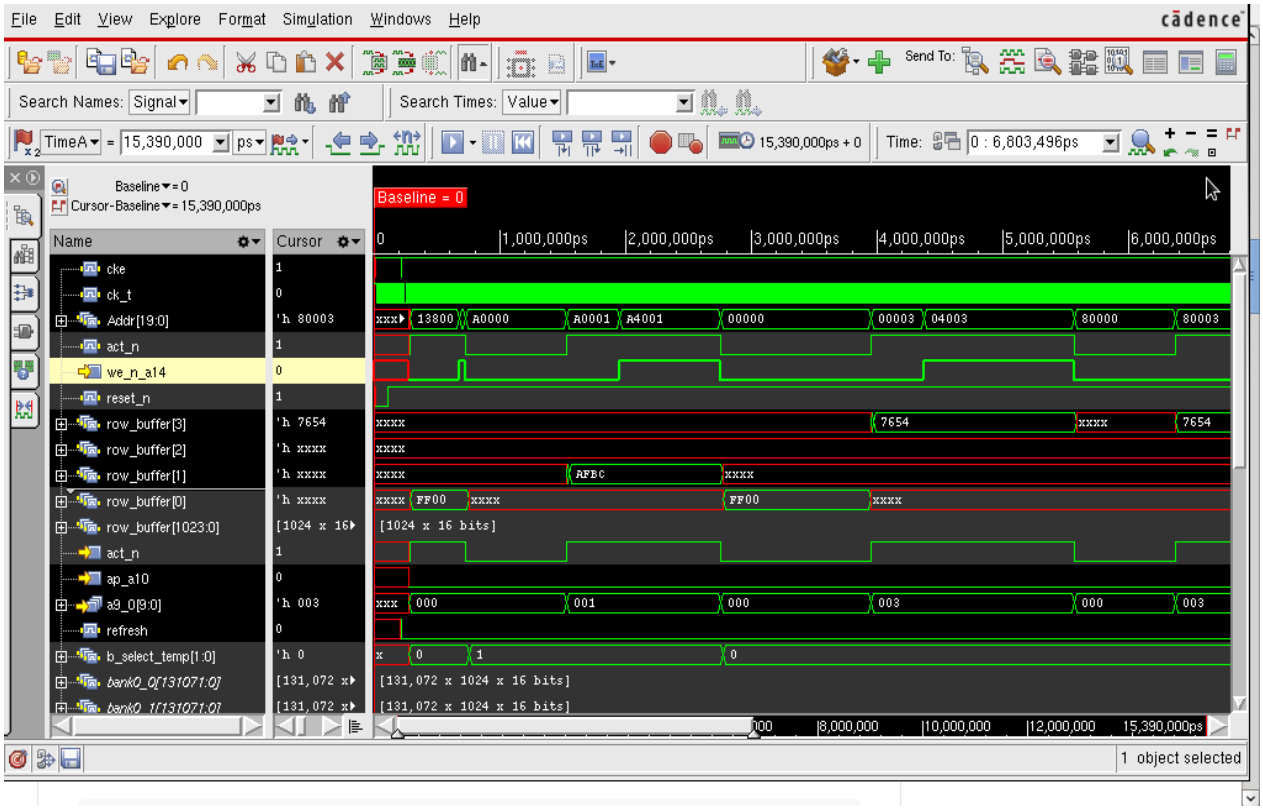

Figure 9: Read-Write Operations

The change in the bank can also be noticed in figure 9. When the address is changed to access the new row of a new bank, that is, row 0 of bank 1 of bank group 1, the state will first be changed to PRECHARGE, as seen in figure 13 (where 7 represents PRECHARGE state), before activating the new row.

The waveform for a single read and write operation is shown below in figure 10. During the REFRESH and INITIALIZATION sequence, the clock will be disabled when clock enable (CKE) is set to LOW. This is also observed here.

.

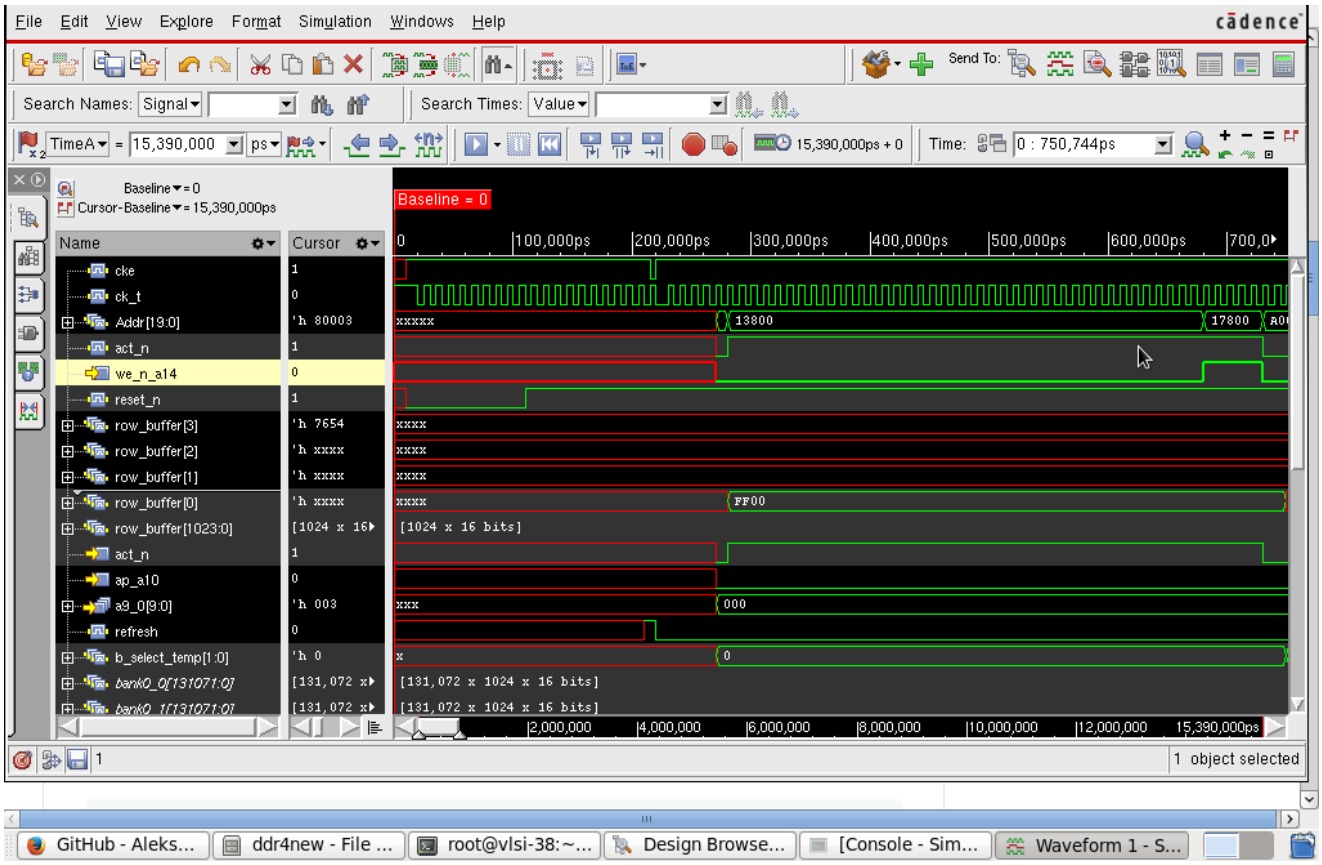

Figure 10: Single read-write operation

The changes that happen in all the signals can be observed in figure 11. Figure 12 shows the states that have been implemented. The state transition and the timing parameters implemented can be seen in figure 13.

The data will be written back into the memory during the PRECHARGE operation. In figures 14 and 15, the data that has been written back into the memory can be observed. Since the testing has been done for 3 data READ and WRITE this data has been written into the memory.

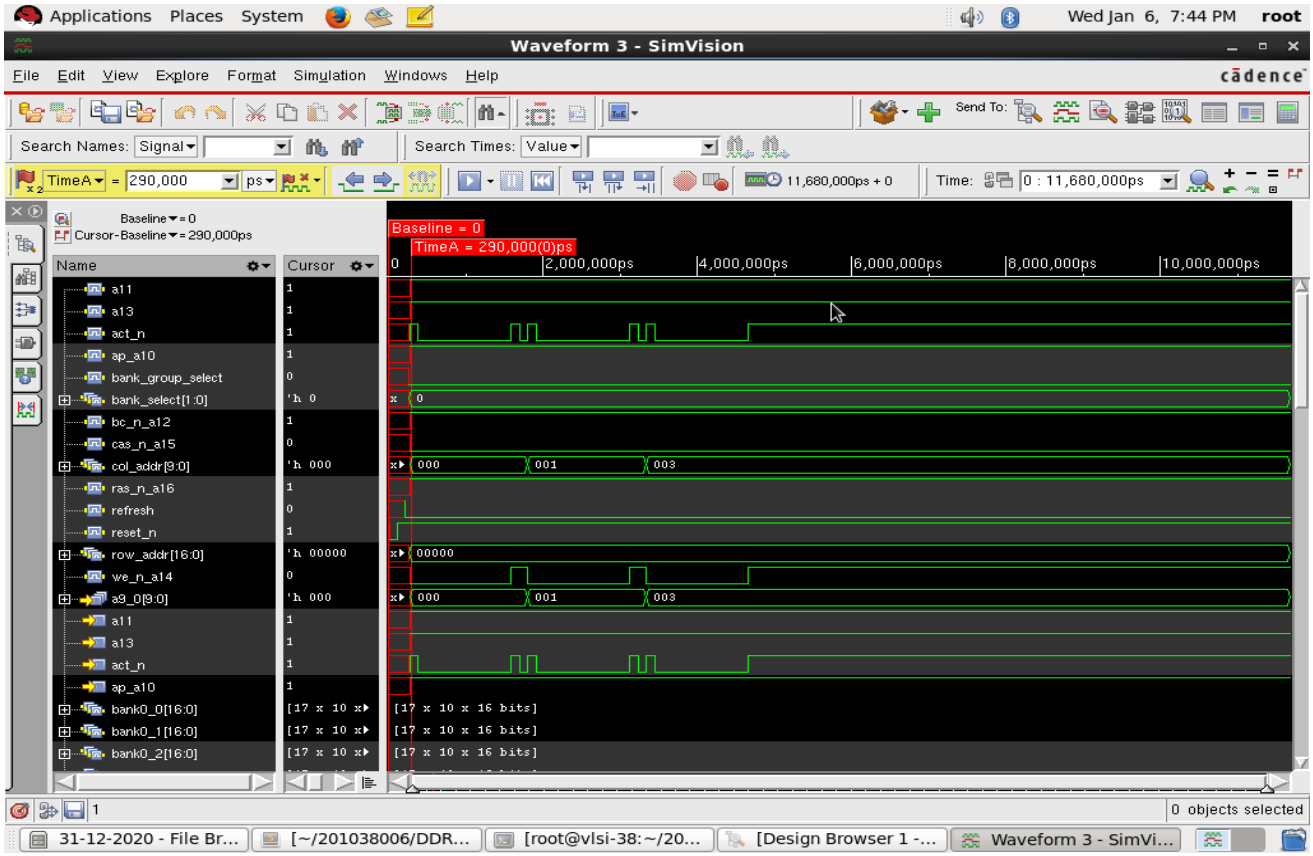

Figure 11: All signals

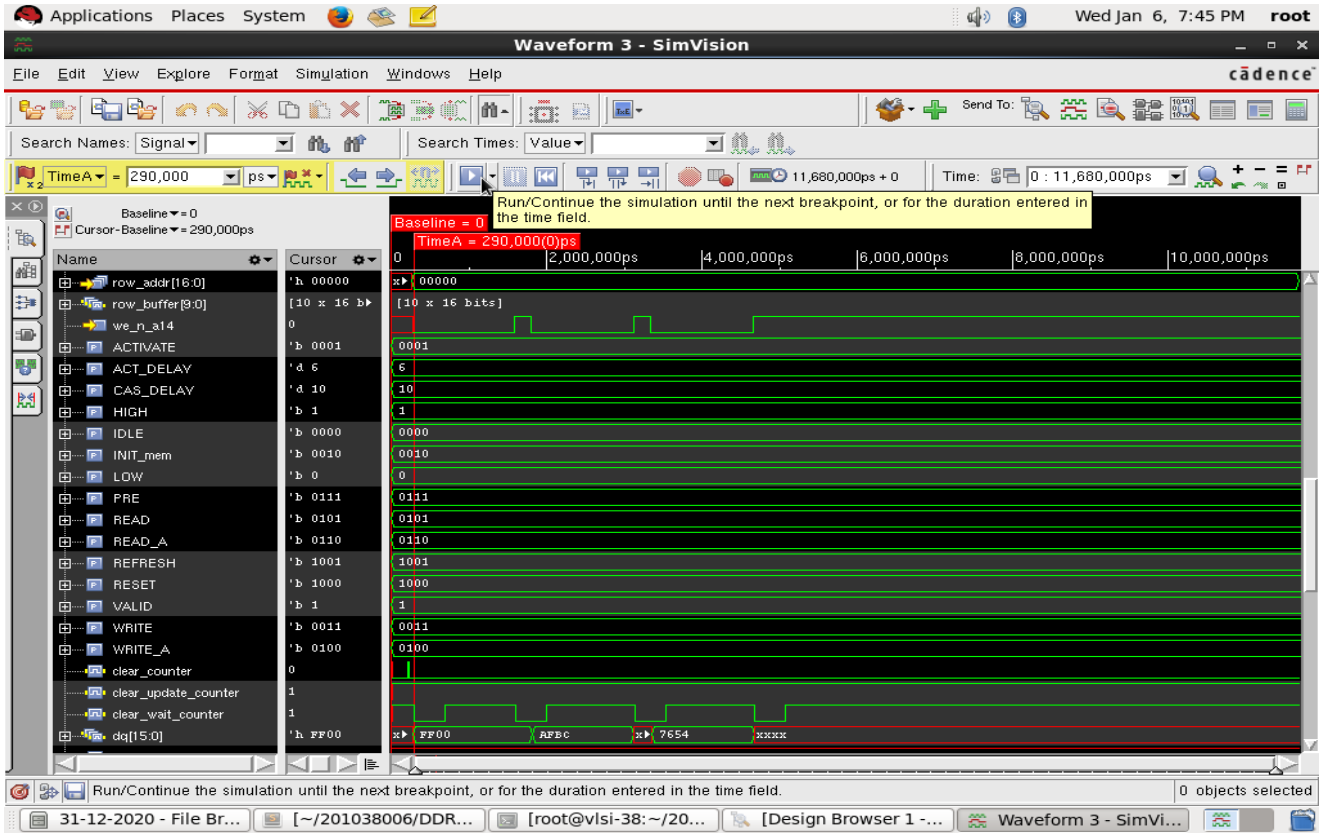

Figure 12: States and timing parameters

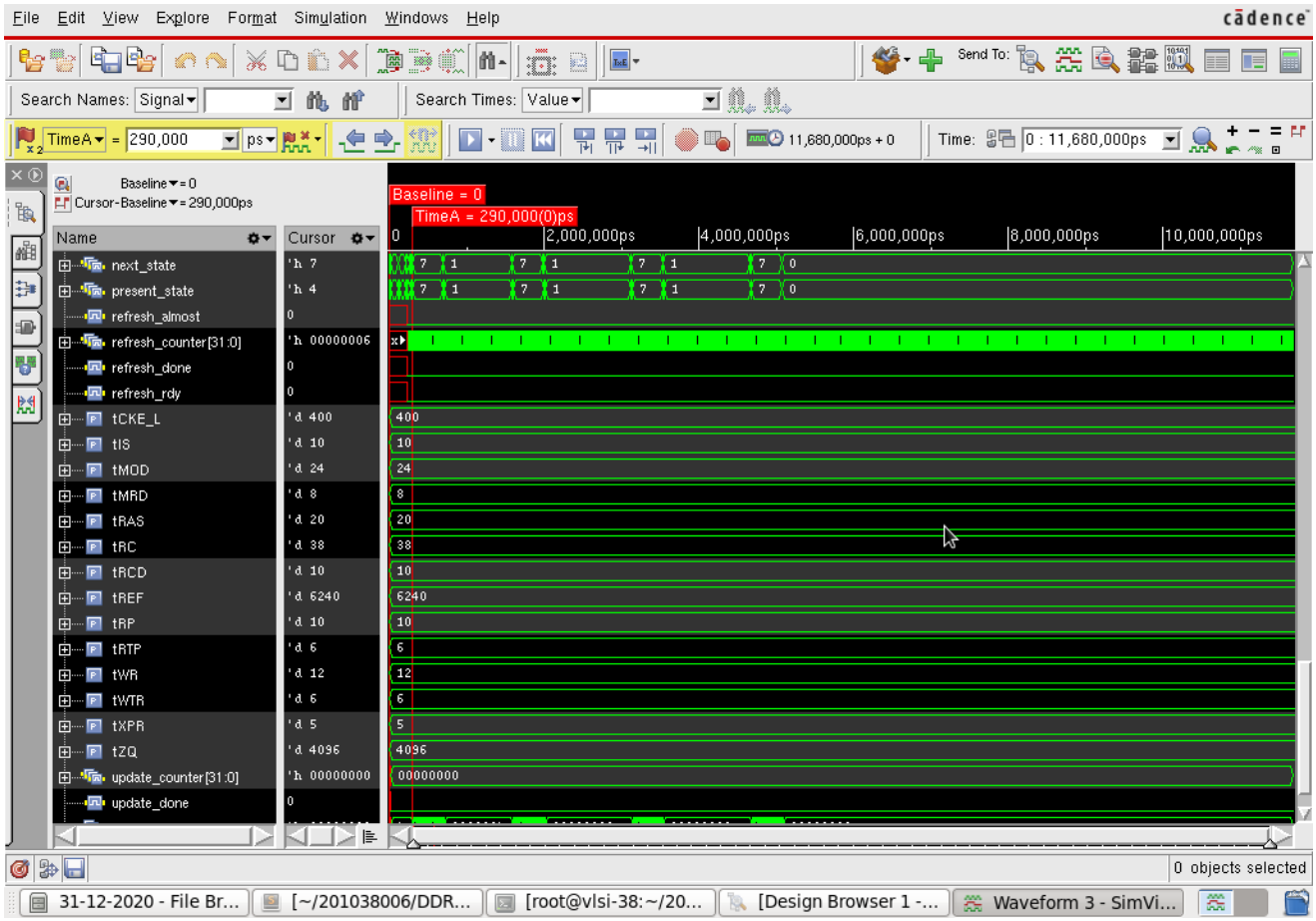

Figure 13: State transition and timing parameters

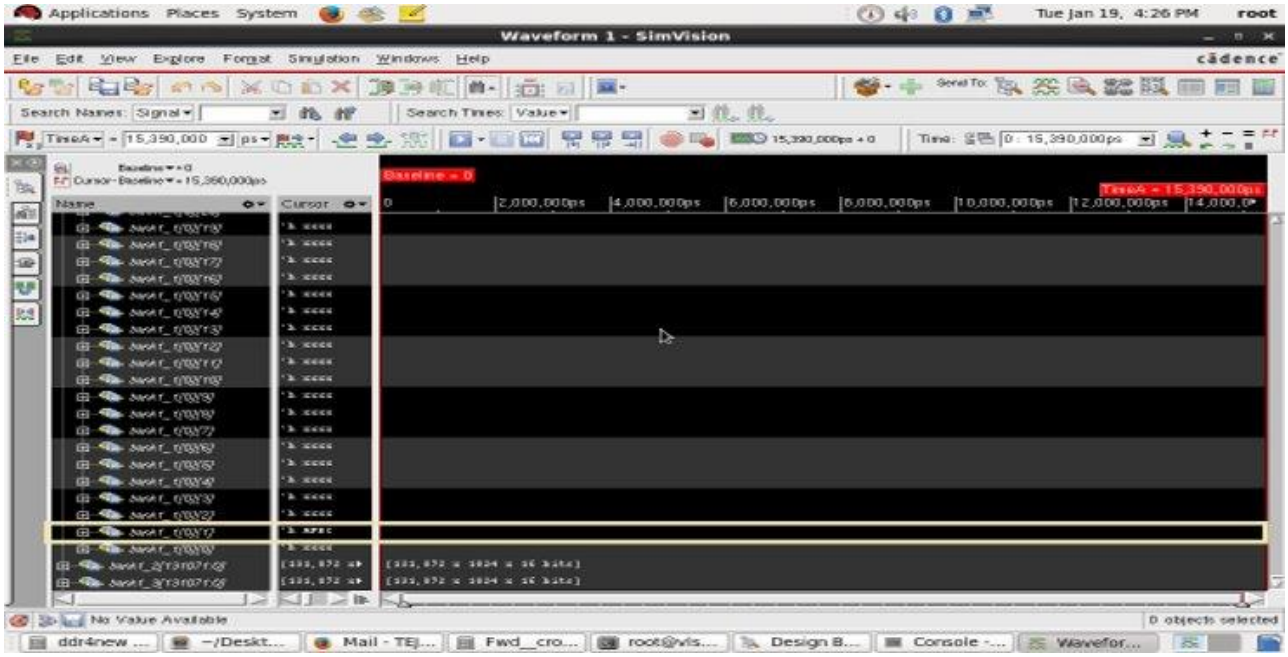

Figure 14: Data written in memory

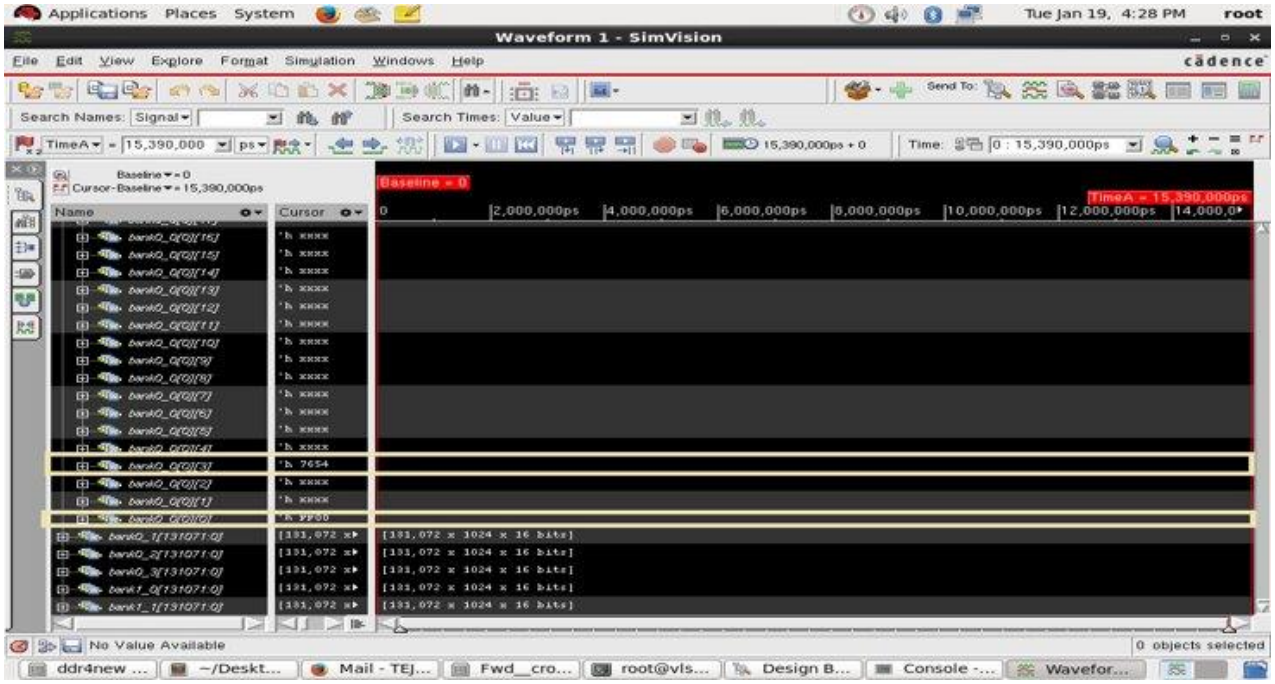

Figure 15: Data written in memory

For ease of observing the output, the state transition, the address and the data WRITE and READ was printed on the console as seen in figures 16 and 17.

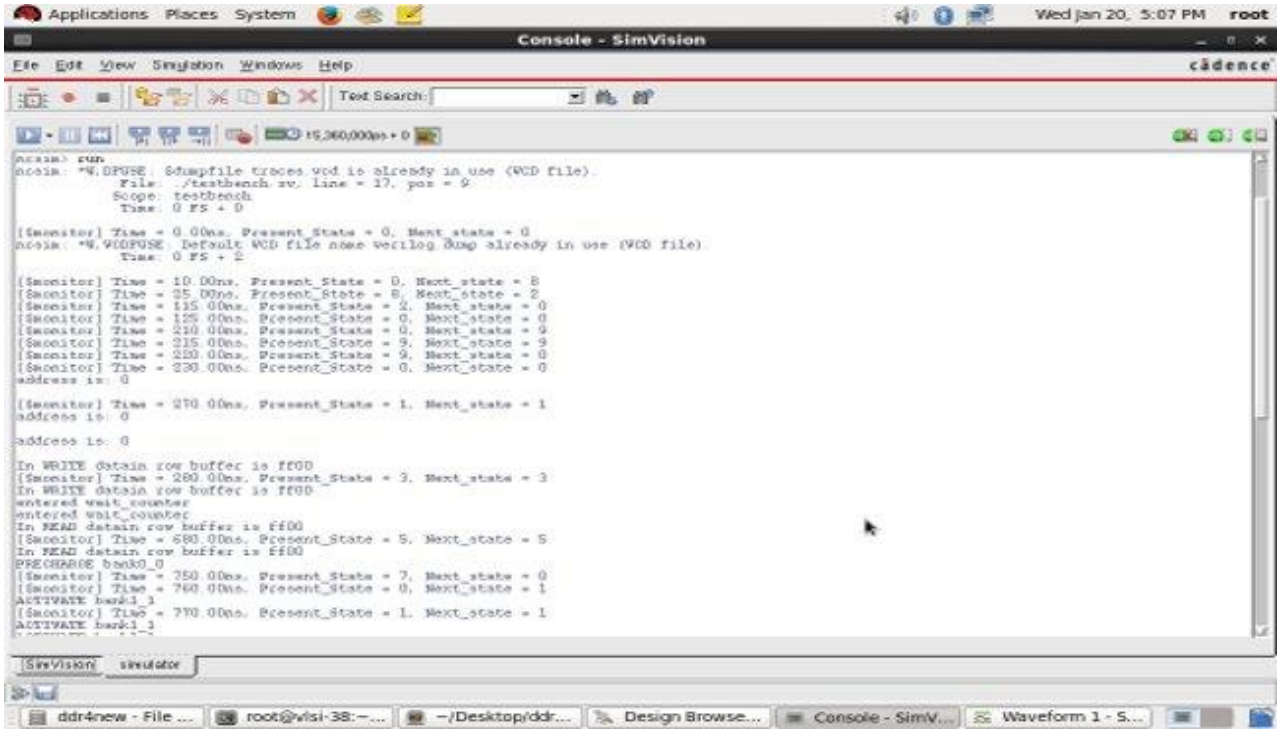

Figure 16: Console output 1

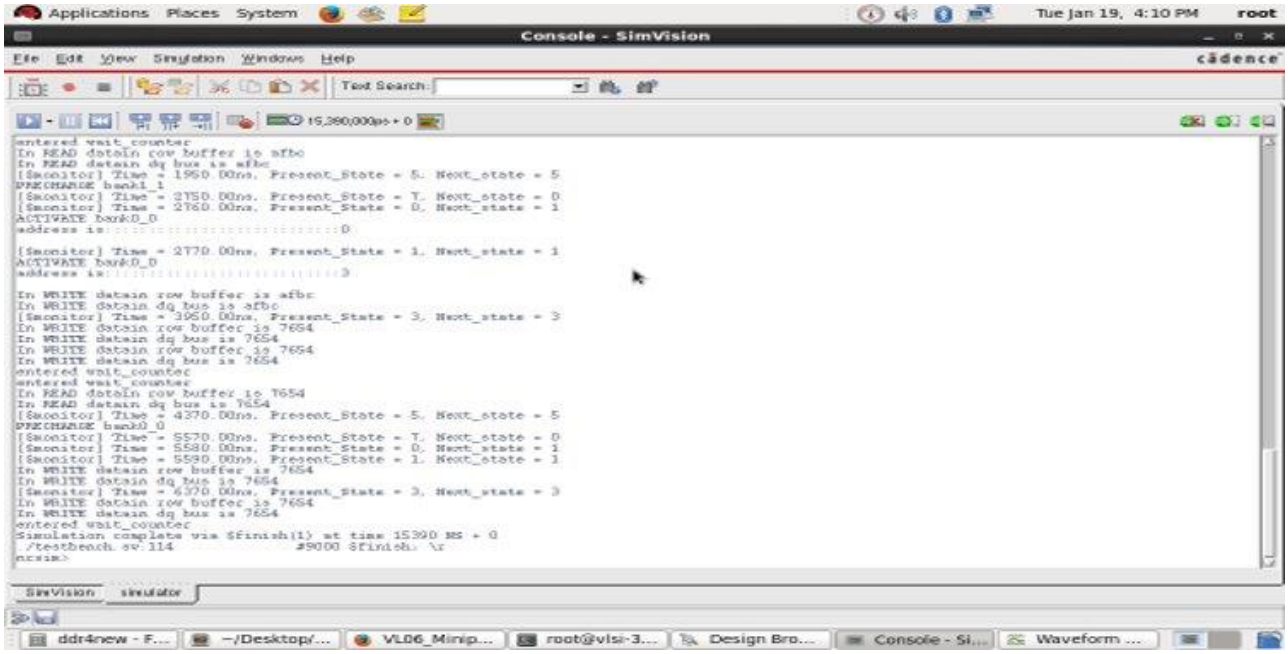

Figure 17: Console output 2

Figure 18 gives the consolidated output including all the signals and the clocks.

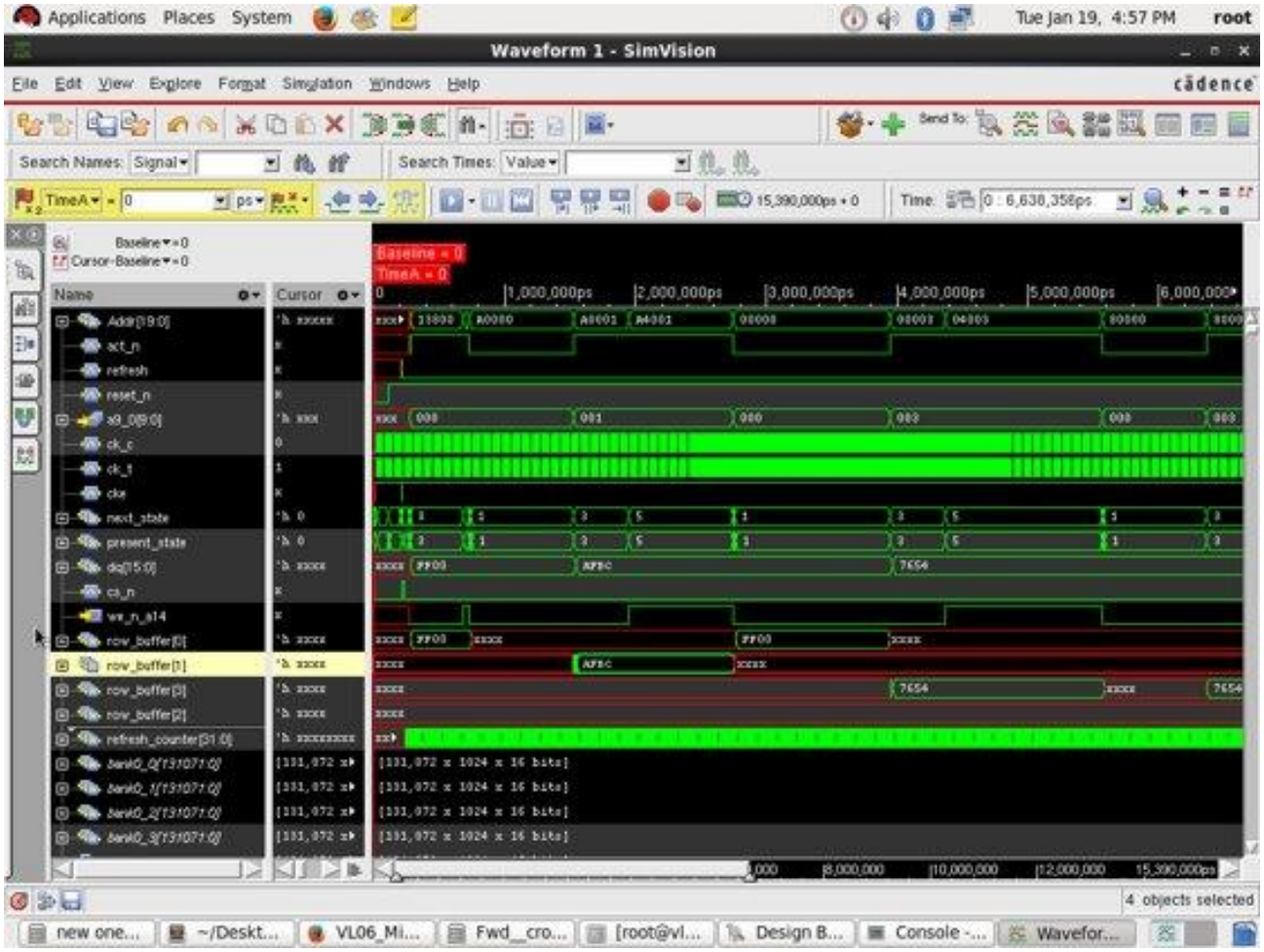

Figure 18: Final output

8. Discussion

The results thus obtained can be used to find any bottle necks if present in the architecture. The major one being the error detections and handling. Improved power performance along with much higher speed of operations and reduced size so that it can be used along with devices of any size and type. This would decrease the gap between the performance of a processor and the memory which is a major constraint today as processor operates at a higher speed but due to the complex designs of the memory and delays between read / write increases this gap.

9. Conclusions

The proposed architecture has been designed and implemented using SystemVerilog according to DDR4 SDRAM Micron Technology Inc. specification. DDR4 has reduced power consumption whereas its transfer rate is more above of its predecessor i.e., DDR3, DDR2, DDR. Its application will be more widely used from low power mobile computing device to high density servers.

10. Scope for further work

- The major drawback is the complex schematic with the use of large number of buffers. That increases the delay. Hence easier schematic reducing the delay can be worked on.
- Error handling in DDR4 is not available. Detection is possible but not handling this can be one of the major works that can be carried out in future to improve the overall performance.

11. References

[1] Micron Technology Inc. Double Data Rate controller SDRAM data sheet.

[2] Pavan Kumar M, Dr Subodh Kumar Panda "*Design and Verification of DDR SDRAM Memory Controller Using System Verilog for Higher Coverage*" Proceedings of the International Conference on Intelligent Computing and Control Systems (ICICCS 2019)

[3] Jia Zheng, Kai Yan, Yue Zhang, Zengping Chen "*Design and Implementation of DDR4 SDRAM Controller Based on FPGA*" 2nd IEEE Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC 2018)

[4] Md. Ashraful Islam, Md. Yeasin Arafath, and Md. Jahid Hasan "*Design of DDR4 SDRAM Controller*" 8th International Conference on Electrical and Computer Engineering20-22 December 2014, Dhaka, Bangladesh

[5] Website referred as on 10 - December -2020 *www.nptel.ac.in/courses/106/106/106106134/*