Pipelinening: Report

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Statistics before Pipelining:

Program	Instructions Executed	Clock Cycles Taken	Speed of Processor
1-even.asm	64	320	0.2
2-prime.asm	6	30	0.2
3.descending.asm	315	1575	0.2
4-histogram.asm	145	715	0.2
5-fibonnaci.asm	76	380	0.2
6-arithematic.asm	47	235	0.2
evenorodd.asm	6	30	0.2
descending.asm	277	1385	0.2

Statistics after Pipelining:

Program	Instructions Executed	Clock Cycles Taken	Speed of Processor	Data Hazards	Control Hazards
1-even.asm	126	167	0.7545	38	69
2-prime.asm	9	17	0.5294	4	3
3.descending.asm	413	561	0.7362	145	204
4-histogram.asm	203	368	0.5516	162	60
5-fibonnaci.asm	117	132	0.8864	12	48
6-arithematic.asm	68	78	0.8718	7	21
evenorodd.asm	6	16	0.375	6	0
descending.asm	513	639	0.8028	122	264

Observations:

1. The number of cycles taken by the processor decreased dramatically, resulting in an increase in the processor speed.
2. More complicated programs, i.e, programs with higher number of read and write instructions and high branching encounter a higher number of data hazards (RAW hazard) and control hazards
3. Stalling the processor due to mentioned data and control hazards (due to RAW hazards or branching condition being true) increases the number of cycles taken by the processor.