CS-303

COMPUTER ORGANIZATION

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. $10 \times 1 = 10$

(i) The Von-Neumann bottleneck is a problem, which occurs due to

(A) small size main memory
(B) speed disparity between CPU and main memory
(C) high speed CPU
(D) malfunctioning of any unit in CPU

(ii) The maximum number of additions and subtractions are required for which of the following multiplier numbers in Booth's algorithm

(A) 01000 1111 (B) 0111 1000
(C) 0000 1111 (D) 0101 0101

(iii) To construct an n-line common bus using MUX for k registers of n bits each, the number of MUXs and size of each MUX are

(A) k and nx 1 (B) n and 2^k
(C) n and kx 1 (D) k and 2^n

(iv) The associative access mechanism is followed in

(A) main memory (B) cache memory
(C) magnetic disk (D) both (A) and (B)

(v) The users view of memory is supported by

(A) paging (B) segmentation
(C) both (D) none of these

(vi) The largest delay in accessing data on disk is due to

(A) seek time (B) rotation time
(C) data transfer time (D) none of these

(vii) A computer uses words of size 32-bit. The instruction

(A) may or may not be one byte length
(B) must always be fetched in one cycle with 2 bytes in the cycle
(C) must always be fetched in two cycles with one byte in each cycle
(D) must be of 2 bytes length

(viii) The CPI value for RISC processor is

(A) 1 (B) 2
(C) 3 (D) none of these

(ix) In DMA the term cycle stealing means

(A) controller gets opportunity to transfer only one word in a timeslot
(B) CPU releases the bus and DMA controller can use endlessly
(C) 100 bytes are allowed to be transferred
(D) none of these

(x) Address of memory location for fetching data needs to be deposited in memory in

(A) MAR (B) MBR
(C) IR (D) status register

(xi) Size of virtual memory is equivalent to the size of

(A) hard disk (B) CPU
(C) floppy disk (D) none of these

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. (a) Explain the difference between full associative and direct mapped cache mapping technique. 3

   (b) Explain "write through" and "write back" policies in cache. 2

3. Explain IEEE single precision formats for representing –10.5. 3+2

4. Why is DMA mode of data transfer used? What are different types of DMA controllers and how do they differ in their functioning? 2+3

5. (a) What is virtual memory? Why it's called virtual? 2

   (b) What do you mean by Logical address space and Physical address space? 3

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

6. (a) Design the bus connection with a CPU to connect four RAM chips of size 256×8 bits each and a ROM chip of 512×8 bit size. Assume that CPU has 8-bit data bus and 16-bit address bus. 9

   (b) Write down difference between Dynamic RAM and Static RAM. 6

7. (a) What do you mean by memory-mapped I/O and I/O-mapped I/O? 4

   (b) Design and describe a 4-bit ALU and its operations. 4+4

   (c) Explain with diagram the daisy chaining priority interrupts technique. 3

8. (a) What is pipelining? Describe pipeline hazards. 1

   (b) What are the advantages of microprogramming control over hardware control? 3

(c) A disk pack has 20 surfaces. Storage area on each surface has an inner diameter of 20 cm and outer diameter of 30 cm. Maximum storage density on any track is 2000 bits/cm and minimum spacing between tracks is 0.50 mm. 3+5

(i) What is the storage capacity of the pack?

(ii)What is the data transfer rate in bytes per second at a rotational speed of 3600 rpm?

(d) Compare between centralized and distributed architecture. Which is the best architecture among them and why? 3

9. (a) A cache has 64 KB capacity, 128-Byte lines and is 4-way Set-Associative. The CPU generates 32-bit address for accessing data in the memory. 2+2+2

(i) How many Lines and Sets does the cache have?

(ii) How many entries are required for tag?

(iii) How many bits of tags are required in each entry in the tag array?

(b) A hierarchical Cache-Main Memory subsystem has the following specifications: 4+3+2

(i) Cache Memory Access Time 80 ns

(ii) Main Memory Access Time 150 ns

(iii) Hit ratio of Cache Memory is 0.9

Calculate the following:

(a) Average access time of the memory system

(b) Efficiency of the memory system

(c) Define addressing mode