Junyan Su

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https://sujunyan.github.io/

EDUCATION

Sept.2015-Jun.2019 **ShanghaiTech University** **Shanghai, China**
B.E. Candidate in Computer Science and Technology
GPA: **3.83 /4.0** Ranking : **3/95**

Aug.2018-May 2019 **University of California at Berkeley** **CA, USA**
Concurrent Enrollment Student at College of Engineering

Aug.2019-present **Washington University in St. Louis** **MO, USA**
Ph.D. student in Systems Science and Mathematics

RESEARCH INTERESTS

Control Theory
Optimal Control
Optimization

PUBLICATIONS

- **J. Su**, Y. Zha, K. Wang, M.E. Villanueva, R. Paulen, B. Houska.
  Interval Superposition Arithmetic for Guaranteed Parameter Estimation
  Dynamics and Control of Process Systems, including Biosystems,2019 [pdf]

HONORS & AWARDS

2016,2017 Scholarship for Academic Excellence, ShanghaiTech University

Oct.13 2017 Most Innovative Robot in Rescue Robot Competition,
IEEE International Symposium on Safety, Security and Rescue Robotics

RESEARCH EXPERIENCE

Jun.2018-Aug.2018 **Carnegie Mellon University** **Pittsburgh, PA, USA**
Robotics Institute Summer Scholars Program
Advisors: Prof. Howie Choset & Lu Li
To design one logic-circuit-level layout with Verilog to fetch data from multiple sensors and reduce CPU intervention time.

Sept.2017-May 2018 **Robomasters 2018** **Nanjing,China**
Advisor: Prof. Andre Rosendo
RoboMaster is one international robotics competition. The competition is like multiplayer online battle arena (MOBA) video game. Each team will build their own robots that serve different functionality.

May 2018-Jan.2019 **A Software for Interval Superposition Model** **Shanghai,China**
Advisor: Prof. Boris Houska
Our software package provides a tool to construct enclosures of the image set of nonlinear functions easily and efficiently, which is needed by a wide variety of numerical computing and control algorithms.

COURSE PROJECTS

- Lego Pick & Place Assembler [website].
- Turtlebot with Robotic Arm Delivery [website].
- A Don't-Touch-Me Robot [website]
- Completed and passed all the points in the [Pintos project]

- Optimal 800MHz 6-Bit “Absolute-value Detector”
  In this project, I and my teammate implemented a CMOS level circuit “Absolute-value Detector” with Cadence Virtuoso. We achieved the minimum delay compared with other teams in the course.

TECHNICAL SKILLS

Programming Languages: C/C++, Python
Scientific Tools: MATLAB, Mathematica, Julia, ROS
Hardware Design:pSoC, STM32xx,Verilog,Cadence Virtuoso
Office Applications: LaTeX

TEACHING

Feb.2017-Jun.2017 Teaching Assistant of *Introduction to Information Science and Technology*

Sept.2017-Jan.2018 Teaching Assistant of *Electric Circuits*