Junyan Su

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https://sujunyan.github.io/

EDUCATION

Sept.2015-Present **ShanghaiTech University** **Shanghai, China**
B.E. Candidate in Computer Science and Technology
GPA: **3.81 /4.0** Ranking : **3/95**

Aug.2018 - Present **University of California,** **Berkeley,CA,USA**
Concurrent Enrollment Student at College of Engineering

RESEARCH INTERESTS

Optimal Control
Locomotion
Bio-inspired Robotics

PUBLICATIONS

- **J. Su**, Y. Zha, K. Wang, M.E. Villanueva, R. Paulen, B. Houska.
  Interval Superposition Arithmetic for Guaranteed Parameter Estimation
  Dynamics and Control of Process Systems, including Biosystems,2019 [pdf]
- **J. Su.**
  Hardware Acceleration for Sensor Data Fetch,
  Carnegie Mellon Robotics Institute Summer Scholars Working Papers Journal Vol.6, pp. 129-132, 2018 [pdf]

HONORS & AWARDS

2016,2017 Scholarship for Academic Excellence, ShanghaiTech University

Oct.13 2017 Most Innovative Robot in Rescue Robot Competition,
IEEE International Symposium on Safety, Security and Rescue Robotics

RESEARCH EXPERIENCE

June-Aug. 2018 **Carnegie Mellon University** **Pittsburgh, PA, USA**
Robotics Institute Summer Scholars Program
Advisors: Prof. Howie Choset & Lu Li
To design one logic-circuit-level layout with Verilog to fetch data from multiple sensors and reduce CPU intervention time.
Responsibilities:

- Designed a logic circuit to collect sensor data via I^2C which is a widely-used protocol for sensor data collection.
- Tested its performance on a multi-sensor system(4 hall sensors and 1 IMU).
- Compared the intervention time and efficiency of data collection between the traditional design (CPU version) and the proposed design.

Achievements:

- Reduced the CPU intervention time from 2000 microseconds to 5 microseconds.
- Doubled the sampling rate of data fetch and enhanced the accuracy of Mahony Filter within +/-0.5 degree.
- In the future, the layout can be integrated into an IP core (semiconductor intellectual property core) for further application.
- Write a paper[1] to summarize the work.

[1] **J. Su.**
Hardware Acceleration for Sensor Data Fetch,
Carnegie Mellon Robotics Institute Summer Scholars Working Papers Journal Vol.6, pp. 129-132, 2018 [pdf]

Sept. 2017 - May 2018 **Robomasters 2018** **Nanjing,China**

Advisor: Prof. Andre Rosendo

RoboMaster is one international robotics competition. The competition is like multiplayer online battle arena (MOBA) video game. Each team will build their own robots that serve different functionality.

Responsibilities:

- Lead the team for the embeded systems development and the electronics design.
- Designed the outlooks and tactical systems of different robots based on demands, including 3 infantry robots, 1 engineer robot, 1 hero robot, 1 supply robot, 1 aerial robot and 1 sentry robot.
- Built hardware structures (with stm32F4xx) of different robots to satisfy various demands.
- Utilized FreeRTOS framework for multi-thread programming, implemented functions on driver level, control level and command level, respectively.

May 2018 - Present **A Software for Interval Superposition Model** **Shanghai,China**

Advisor: Prof. Boris Houska

Our software package provides a tool to construct enclosures of the image set of nonlinear functions easily and efficiently, which is needed by a wide variety of numerical computing and control algorithms.

Responsibilities:

- Developing a software package for intervel superposition arithmetic.[2]
- Implemented an application for Guaranteed Parameter Estimation and submitted a paper[3]

[2] Y. Zha, M.E. Villanueva, B. Houska. Interval superposition arithmetic.
Technical report, 2018. [pdf]

[3] **J. Su**, Y. Zha, K. Wang, M.E. Villanueva, R. Paulen, B. Houska.
Interval Superposition Arithmetic for Guaranteed Parameter Estimation
Dynamics and Control of Process Systems, including Biosystems,2019 [pdf]

COURSE PROJECTS

- Lego Pick & Place Assembler [website].
- Turtlebot with Robotic Arm Delivery [website].
- A Don't-Touch-Me Robot [website]
- Completed and passed all the points in the [Pintos project]
- Optimal 800MHz 6-Bit "Absolute-value Detector"
  In this project, I and my teammate implemented a CMOS level circuit "Absolute-value Detector" with Cadence Virtuoso. We achieved the minimum delay compared with other teams in the course.

TECHNICAL SKILLS

Programming Languages: C/C++, Python
Scientific Tools: MATLAB, Mathematica, Julia, ROS
Hardware Design:pSoC, STM32xx,Verilog,Cadence Virtuoso
Office Applications: LaTeX

TEACHING

Feb. - Jun. 2017 Teaching Assistant of *Introduction to Information Science and Technology*

Responsibilities:

- Assisted professor in grading programming and writing assignments
- Helped students in the lab : corrected their mistakes and gave lecture about how to complete the lab.
- Hosted office hours to answer questions from students

Sept. 2017 - Jan. 2018 Teaching Assistant of *Electric Circuits*

Responsibilities:

- Helped students in the lab : correct their mistakes and give lecture about how to finish the lab.
- Hosted office hours to answer questions from students
- Provided guidance and direction to enhance understanding of the course material
- Designed one of the final projects

Standardized Tests

GRE Verbal 153 + Quantitative 167 + AW 3

TOEFL Total 101 (Reading 29, Listening 26, Speaking 21, Writing 25)

COURSES

CATEGORY	COURSE	GRADES
Computer Science	Data Structures	A+
	Computer Architecture	A
	Introduction to Algorithms	A
	Operating System	A-
	Introduction to Robotics	In Progress
Electronic Engineering	Electric Circuits	A
	Signal and Systems	A
	Introduction to Control	A+
	Signal Detection and Estimation	A
	Integrated Digital Circuits	A+
	Linear System Theory	A
	Mechatronics Design	A
Mathematics	Calculus	A
	Linear Algebra	A
	Probability and Statistics	A+
	Discrete Mathematics	A
	Convex Optimization	B