Traffic Light Controller Using FPGA Implementation

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***Abstract*— The traffic in road crossings /junctions is controlled by switching ON/OFF Red, Green & Yellow lights in a particular sequence. The Traffic Light Controller is designed to generate a sequence of digital data called switching sequences that can be used to control the traffic lights of a typical four roads junction in a fixed sequence. It plays more and more important role in modern management and control of urban traffic to reduce the accident and traffic jam in road. It is a sequential machine to be analyzed and programmed through a multistep process. The device that involves an analysis of existing sequential machines in traffic lights controllers, timing and synchronization and introduction of operation and flashing light synthesis sequence. The methods that are used in this project are design the circuit, write a coding, simulation, synthesis and implement in hardware. In this project, ALTERA QUARTUS II Software is chosen to design a schematic using schematic edit, writes a coding using Verilog HDL (Hardware Description Language) text editor and implements the circuit on FPGA BOARD.**

I. INTRODUCTION

Traffic congestion is a severe problem in many modern cities around the world. Traffic congestion has been causing many critical problems and challenges in the major and most populated cities. To travel to different places within the city is becoming more difficult for the travelers in traffic. Due to these congestion problems, people lose time, miss opportunities, and get frustrated. Traffic congestion directly impacts the companies. Due to traffic congestions there is a loss in productivity from workers, trade opportunities are lost, delivery gets delayed, and thereby the costs goes on increasing. To solve these congestion problems, we have to build new facilities & infrastructure but at the same time make it smart. The only disadvantage of making new roads on facilities is that it makes the surroundings more congested. So for that reason we need to change the system ratherthan making new infrastructure twice. Therefore many countries are working to manage their existing transportation systems to improve mobility, safety and traffic flows in order to reduce the demand of vehicle use.

Therefore, many researches about traffic light system have been done in order to overcome some complicated traffic phenomenon but existent research had been limited about present traffic system inwell- travelled traffic scenarios. The time of allocation is fixed from east to west or opposite way and from north to south way in crossroads. Field Programmable Gate Arrays (FPGAs) are extensively used in rapid prototyping and verification of a conceptual design and also used in electronic systems when the mask-production of a custom IC becomes prohibitively expensive due to the small quantity.

Many system designs that used to be built in custom silicon VLSI are now implemented in Field Programmable Gate Arrays. This is because of the high cost of building a mask production of a custom VLSI especially for small quantity.

II. DESIGN OF TRAFFIC LIGHT CONTROLLER

Traffic Light Controller can be designed by starting with some assumptions. At first the North traffic will be allowed to move and then traffic in the East, South and West direction will be allowed to move in sequence. The advantage of writing Traffic Light Controller program is that in a program, modifications as per requirements can be done easily i.e., suppose the traffic on main road should be allowed for more time and for side roads the traffic should be allowed for less time;then the clock is divided in such a way that for main road the clock period will be more and for side roads the clock period will be less, this is because the main road traffic is heavy when compared to the side road traffic. In general TLC System will be having three lights (red, green and yellow) in each direction where red light stands for traffic to be stopped, green light stands for traffic to be allowed and yellow light stands for traffic is going to be stopped in few seconds.

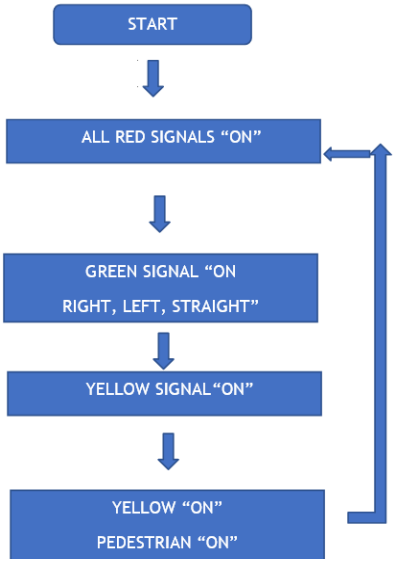

Figure 1: Block Diagram

III. WORKING AND STATE DIAGRAM

First of all the directions are red. When the STATE 0 is ON the signal of North direction is green, east is yellow remaining all the directions are Red. Later the controller is switched to state S1 where the East direction is allowed green signal, south direction has a yellow signal and remaining all direction stand with red signal. Next by switching the State to S2 South direction has green signal, west direction has a yellow signal and remaining are red. Finally during S3 state green is on for the West direction, yellow again for the north direction and red in remaining directions. The traffic light is designed using a Verilog HDL and is and is implemented using FPGA.

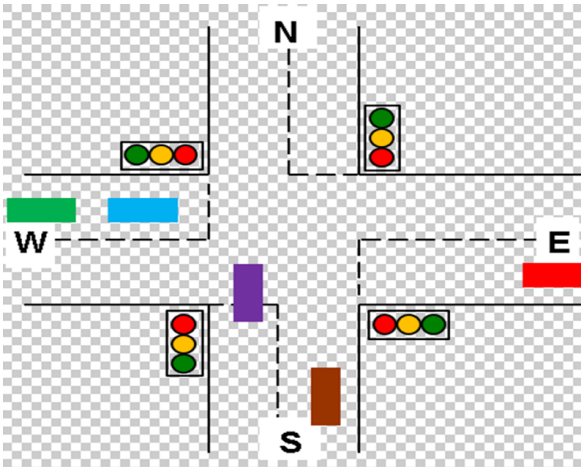

Figure 2 Basic Traffic Signal Structure

In this structure, there are four traffic signals, represented by R1(towards north) , R2(towards east) , R3(towards south) and R4(towards west) to be controlled. All the four signals have same priority as they all are main roads.

The state diagram for the traffic light controller is as shown in figure 3.

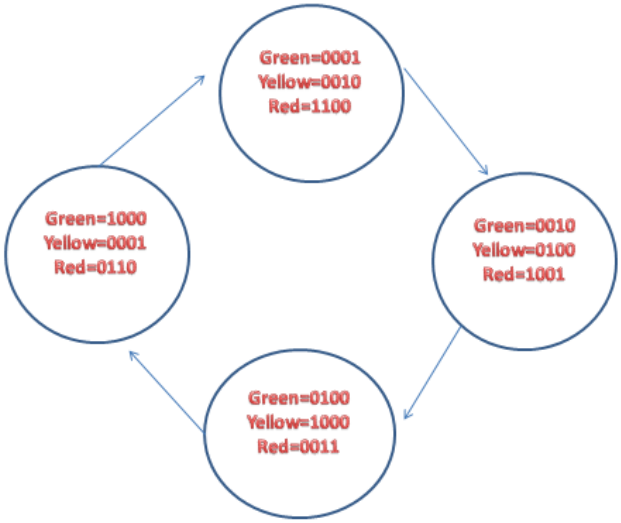

Figure 3: State Diagram

In the TLC state diagram, there are 4 states, S0, S1, S2 and S3 and are given with the following digital inputs as mentioned in fig 3.We assume bit 0 as light for north direction, bit 1 as light for east direction, bit 2 as light for south direction and bit 3 as light for west direction. In state 0 , north is provided green light and east with yellow and remaining with red.

In state 1, east direction is given green light and south with yellow light and remaining all are red.

In state 2, south direction is given green light and west direction is given yellow signal and rest all stand with red light.

In final state that is in state 3, west direction is given green signal and north is given yellow signal and rest all directions stand with the red signal.

IV. VERILOG HDL CODE

```
module prjctr(state,reset,grn,ylw,rd,an);
   input[1:0] state;
  input reset;
   output reg [3:0]grn,ylw,rd;
  output reg [3:0]an;
   always@(reset or state)
 begin
if(reset==0)
begin
grn=4'b0000;
ylw=4'b0000;
rd=4'b1111;
```

```
end
else
case (state)
2'b00:
begin
grn=4'b0001;
ylw=4'b0010;
rd=4'b1100;
end
2'b01:
begin
grn=4'b0010;
ylw=4'b0100;
rd=4'b1001;
end
2'b10:
begin
grn=4'b0100;
ylw=4'b1000;
rd=4'b0011;
end
default:
begin
grn=4'b1000;
ylw=4'b0001;
rd=4'b0110;
end
endcase
an=4'b1110;
end
endmodule
```

Test bench :

```
module tb;
 reg [1:0] state;
 reg reset;
        wire [4:1] grn;
 wire [4:1] ylw;
 wire [4:1] rd;
 prjctr uut (
        .state(state),
        .reset(reset),
        .grn(grn),
        .ylw(ylw),
        .rd(rd)
 );
    initial begin
        state = 2'b00;
        reset = 1;
        #100;
      state = 2'b01;
        reset = 0;
        #100;
        state = 2'b01;
        reset = 1;
        #100;
        state = 2'b10;
        reset = 1;
        #100;
        state = 2'b11;
        reset = 1;
        #100;
        state = 2'b00;
        reset = 1;
        #100;
      state = 2'b01;
        reset = 1;
        #100;
        state = 2'b10;
        reset = 1;
        #100;
        state = 2'b11;
        reset = 1;
        #100;
        state = 2'b00;
        reset = 1;
        #100;
    end
   endmodule
```

V. RESULTS

Pin Assignments:

sw[0]:reset

sw[1]:state[0]

sw[2]:state[1]

LEDR[0]:rd[0]

LEDR[1]:rd[1]

LEDR[2]:rd[2]

LEDR[3]:rd[3]

LEDG[0]:grn[0]

LEDG[1]:grn[1]

LEDG[2]:grn[2]

LEDG[3]:grn[3]

LEDG[4]:ylw[0]

LEDG[5]:ylw[1]

LEDG[6]:ylw[2]

LEDG[7]:ylw[3]

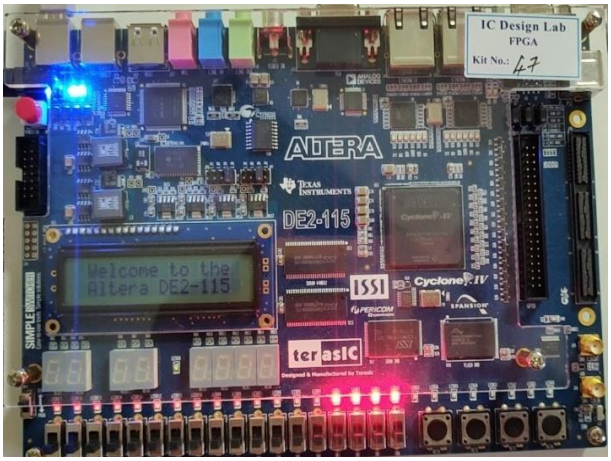

Figure 4: INITIAL

Figure 5 North Direction

Figure 6: EAST GREEN

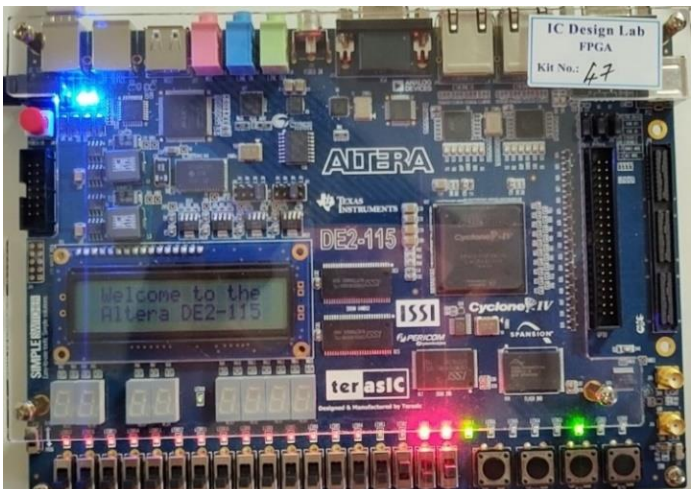

Figure 7: SOUTH GREEN

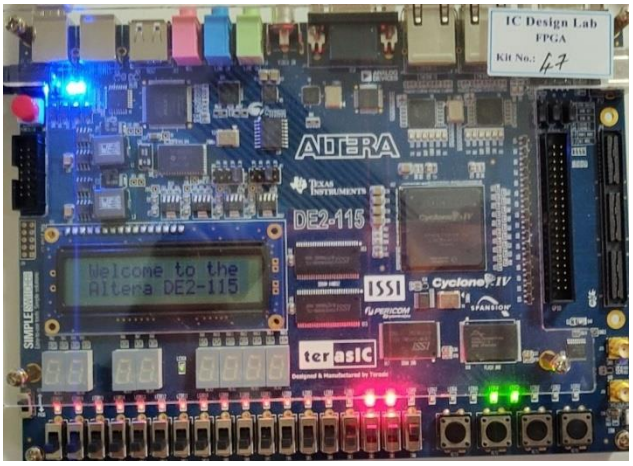

Figure 8: WEST GREEN

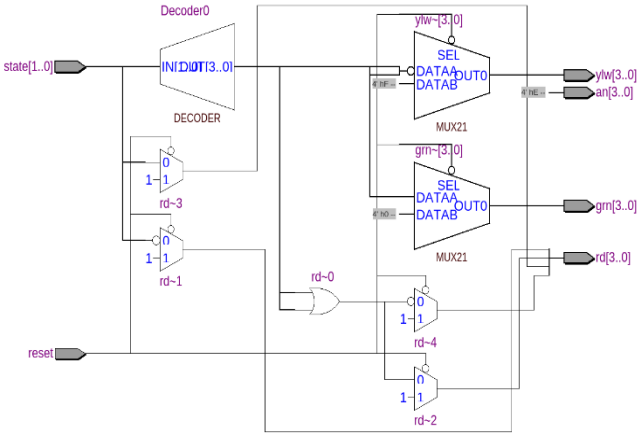

FIGURE 9. Circuit Diagram of TLC

VI. CONCLUSION

A four way traffic light controller circuit is formed using synchronus sequential circuits and using FPGA implemetation.

VII. REFERENCE

[1]https://en.wikipedia.org/wiki/Traffic_light_control_and_coordination

[2]https://www.academia.edu/21200096/DESIGN_AND_IMPLEMENTATION_OF_TRAFFIC_LIGHTS_CONTROLLER_USING_FPGA_A_Project_Based_Laboratory_Report_in_partial_fulfilment_for_the_award_of_III_IV_B._Tech_-I_Semester_Submitted_by_Lab_Instructor

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[4]https://www.fpga4student.com/2016/11/verilog-code-for-traffic-light-system.html